
Re: How to place text in copper pour on top and/or bottom etch

5 messages

Tech Support <TechSupport@ema-eda.com>

Thu, Feb 20, 2020 at 8:28 AM

Reply-To: Tech Support <TechSupport@ema-eda.com>

To: "davidwaskevich@gmail.com" <davidwaskevich@gmail.com>

Hi David Waskevich,

Your EMA support ticket #54973 has been assigned to a technical support engineer. They should be in contact with you shortly.

You can view your ticket, as well as add comments at the link below:

<https://techsupport.ema-eda.com/helpdesk/tickets/54973>

Or, simply reply to this email.

Best Regards,
Nathan Amidon

On Wed, 19 Feb at 6:45 PM , David Waskevich <davidwaskevich@gmail.com> wrote:

Hello EMA support - I'm trying to place text in copper (part number, board revision, etc) on the top and/or bottom etch layers. The text needs to go inside a copper pour. What's the best way to do this? Note - placing this information on the silkscreen layer is straightforward since there's no etch involved and I know the correct method to do this ... but I want to also put information in the copper etch itself (maybe even a logo/graphic at some point in the future:-)).

I've tried the following, but please let me know if I missed an easier method (since both methods have drawbacks which are explained below):

1. I used ADD|Text to add the text to the Top Etch layer. This seemed easy and PCB Editor accommodated by "voiding" the copper pour with a rectangle and placing the text (in etch) inside the box (which is exactly what I wanted). This did not generate any DRC errors or warnings and looked fine to me. However, this caused DFM violations at the board house when I went to have the board fabricated since the "bounding box" did not leave enough clearance between the text and the border of the voided rectangle. This is not really a concern since it's not a circuit short but the fabrication house didn't like it (and, to be fair, they have no way of knowing my intent or that it's not a problem). Here's what it looks like:

2. I used Outline|Keepout to place a rectangle on Top Route Keepout layer. This created a void in the copper pour (which seemed logical to me and what I expected/hoped for). Then, I used ADD|Text to place the text (in copper on Top Etch layer) inside the keepout shape. This takes care of the spacing issue, but now I get a DRC error in PCB Editor. I've pasted in a screen shot below with the DRC visible while hovering my mouse on the marker. In case it's too small to read, the error says "DRC error "Line to Route Keepout Spacing" Top Constraint Value: 0 mil, Actual value: 0 mil". I have no idea what this DRC means. I went to the constraint manager and found the offending constraint, but don't know how to edit the property to make the DRC error go away. If this is the best way to do what I want, can you tell me how to modify the constraints to make the DRC go away? I don't want to just "waive" the DRC, I'd rather know how to fix it. Here are some screen shots of the second method:

Thanks,

..... David

Tech Support <TechSupport@ema-eda.com>
Reply-To: Tech Support <TechSupport@ema-eda.com>
To: "davidwaskevich@gmail.com" <davidwaskevich@gmail.com>

Mon, Feb 24, 2020 at 7:40 AM

Hi David,

Your ticket regarding the spacing around your text has been assigned to me.
The constraint that is used for the text is the Line to Shape spacing. Increasing this value to give the desired clearance around the text would also affect the spacing between your traces and shapes.
From the menu select Shape>Manual Isolation/Cavity>Rectangular
Select the shape then draw the rectangular void around the text.

Will this meet your needs?

Best Regards,
Ron Guthrie
[Quoted text hidden]

FRISTPROJECT_COPY_void.brd
265K

Tech Support <TechSupport@ema-eda.com>
Reply-To: Tech Support <TechSupport@ema-eda.com>
To: "davidwaskevich@gmail.com" <davidwaskevich@gmail.com>

Mon, Mar 2, 2020 at 8:09 AM

Hi David,

I am following up on this ticket to see if you have any questions or if this case can be closed now.

Best Regards,
Ron Guthrie
[Quoted text hidden]

Tech Support <TechSupport@ema-eda.com>
Reply-To: Tech Support <TechSupport@ema-eda.com>
To: "davidwaskevich@gmail.com" <davidwaskevich@gmail.com>

Wed, Mar 4, 2020 at 7:08 AM

Hi David,

Your understanding of this is correct.
This is an image of your board as you sent it to me.

Increasing the line to shape spacing would increase the space around the text as shown below, but you will notice that the trace also has an increased space.

Best Regards,
Ron Guthrie

On Tue, 3 Mar at 9:36 PM , David Waskevich <davidwaskevich@gmail.com> wrote:
Hi Ron - thanks for your reply (and sorry for my delay in responding). I believe your suggestion to use Shape>Manual Isolation/Cavity is exactly what I was looking for (thanks!).

But, let me just make sure I understand completely ... I think you're saying that I should *not* loosen the constraint for "line to shape" spacing as I was asking since this would affect other aspects of the design/layout that I might not want to change ... correct? And, rather than loosening the constraint, I should use the Shape>Manual Isolation/Cavity method instead.

Do I have this right?

Thanks,

.... David

Tech Support <TechSupport@ema-eda.com>
Reply-To: Tech Support <TechSupport@ema-eda.com>
To: "davidwaskevich@gmail.com" <davidwaskevich@gmail.com>

Wed, Mar 4, 2020 at 2:56 PM

Hi David,

I've provided answers below.

Best Regards,
Ron Guthrie

On Wed, 4 Mar at 3:09 PM , David Waskevich <davidwaskevich@gmail.com> wrote:
Hi Ron - thanks again for your prompt and helpful feedback ... I really appreciate it. I'm pretty sure that I now understand the impact of changing the "line to shape" constraint (which is not what I want to do in this case).

I've confirmed that your suggestion works (thanks a lot for that advice) but let me return to my other approach (#2 method in my original post) for a moment:

1) Why doesn't "Outline|Keepout" do what I want? It seemed like it would but it causes the DRC error I described in the original post when text is placed inside.

Keepout areas are used to define areas that should not contain anything. So text within a keepout is causing a violation. The opening in the shape is created because of the keepout.

2) Why/how is it different than your solution of using "Shape>Manual Isolation/Cavity"?

The solution that I suggested is different in that it creates an opening in the shape only. It is not a keepout so anything can still be placed within that area.

3) How would I have known to use your method (Shape|Manual Isolation|Cavity) instead of using the "Outline|Keepout" area?

That isn't something that you would have known. It comes down to experience. I have used the software for over 20 years.

4) Why does the "Outline|Keepout" generate the DRC error when text is placed inside?

As described above a keepout area is an area that should not have anything in it.

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5) I don't quite understand the DRC error or how to clear it. How would I (if I wanted to) change the Constraint Manager to eliminate the DRC error in the second method (details of the DRC are described in the original post above)?

There are no constraint settings to avoid the DRC of an object within a keepout area. To "clear" the DRC, from the menu you can select Check>Waive DRC>Waive then select the DRC

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Right mouse click then select Done. The DRC will then be made invisible. The DRC will still exist but you have identified it as acceptable so it is no longer visible.

Note: Full disclosure here on route keepout areas. There can be exceptions to a keepout area. You can assign properties to a route keepout shape to specify the objects that you will allow to be inside of the keepout. The properties are self explanatory and they are PINS_ALLOWED, ROUTES_ALLOWED, SHAPES_ALLOWED and VIAS_ALLOWED

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