TouchController Orcad design notes

My Library and downloaded symbols/footprints folders:

- C:\Users\djjw\Documents\Orcad\Library
- C:\Users\djjw\Documents\Orcad\PSoC symbols and footprints
- Add these paths to padpath and psmpath in Orcad PCB Editor under Setup|User Preferences|Paths|Library

Notes (after completing my attempt and then watching other tutorials):

- Create board outline using the automatic tool that includes a "keep-in" (set Design Edge Clearance to something like 20 mils)
- Reset the X-Y origin to the bottom left corner of the board outline (Setup|Change Origin)
- Use the Setup|Design Parameter|Text to change text size (Block numbers)
- To update the PCB layout from a schematic change, use the current board file as the "input" board file and then assign a new output file (like next Rev … or maybe even it would work to overwrite the input file)
- Use AutoSilkscreen
- Learn to use Z-Copy (what's it for?)
- Use the General Edit, Etch Edit, Placement Edit and Shape Edit modes
- Use the Design Workflow menu items
- Use Shape|Global Dynamic Shape Parameters to set the shape fill (hatch, solid, etc), clearances (10 mil maybe?) and thermal reliefs (10-20 mil maybe)
- For text in copper, I can't figure out how to prevent a DRC error, but it makes sense to place a KeepOut and then place text inside.
- To change a lot of things (like text size of RefDes or line widths for instance), use the Edit|Change Objects menu item. Then use the Options panel to adjust the property and then just go around and click on the items you want to change.
- To change the copper pour spacing, use Shape|Global Dynamic Parameters

Components needed:

- CY8C4014LQI-422
  - Cypress or UltraLibrarian?
  - The zip download from www.cypress.com is wrong … it contains 4000S
  - I pulled the 4014 from the CY8CKIT-040 .dsn file
- SMT:
  - Need to decide if I'm gonna use 0603 or 0805
  - Resistor, Capacitor, LED
- Push button switch
  - My smt switch?
- SPDT slider switch
  - 3-pin thru-hole
- 8-pin dual row female headers

    -
- 5-pin single row male header
    -
- 2-pin header with zero-ohm jumper
- Test point(s)
- Ground clip

touchcontroller-1-2.drl
ncdrill.log
nc_tools_auto.txt

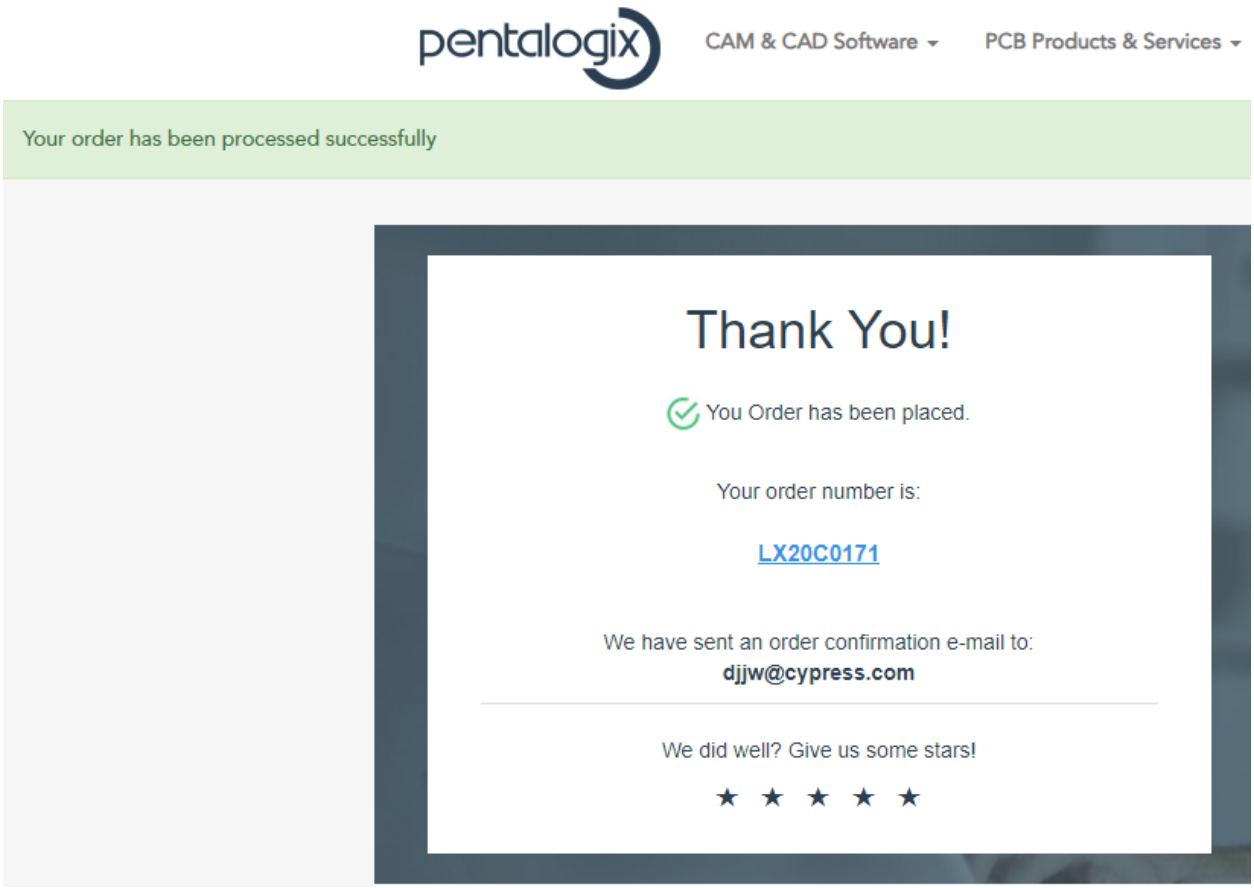
Quick Turn PCB prototypes:

- Pentalogix - 1 (800) 238-1920 - https://www.pentalogix.com/cart
- PCB Unlimited
- Chicago Circuits
- Advanced Circuits (4PCB)
- Online Electronics
- Sunstone - https://www.sunstone.com/ - 1-800-228-8198
- Seed Fusion ($4.90 for 100x100mm)

Sunstone:

- **File Name:** DFM0125373-2020-001.zip
- **File Size:** 29 Kb
- DFM Subitted Successfully

- **Your DFM Job Name is: DFM0125373-2020-001**


pentalogix
CAM & CAD Software
PCB Products & Services
Your order has been processed successfully
Thank You!
You Order has been placed.
Your order number is:
LX20C0171
We have sent an order confirmation e-mail to:
djjw@cypress.com
We did well? Give us some stars!
★ ★ ★ ★ ★

7.4.10 Ground Plane

When designing the ground plane, follow these guidelines:

- Ground surrounding the sensors should be in a hatch pattern. If you are using ground or driven-shield planes in both top and bottom layers of the PCB, you should use a 25 percent hatching on the top layer (7-mil line, 45-mil spacing), and 17 percent on the bottom layer (7-mil line, 70-mil spacing).
- For the other parts of the board not related to CapSense, solid ground should be present as much as possible.
- The ground planes on different layers should be stitched together as much as possible, depending on the PCB manufacturing costs. Higher amount of stitching results in lower ground inductance, and brings the chip ground closer to the supply ground. This is important especially when there is high current sinking through the ground, such as when the radio is operational.
- Every ground plane used for CapSense should be star-connected to a central point, and this central point should be the sole return path to the supply ground. Specifically:
  - The hatch ground for all sensors must terminate at the central point
  - The ground plane for C_{MOD}, C_{INTX} must terminate at the central point
  - The ground plane for C_{SH_TANK} must terminate at the central point

Figure 7-23 explains the star connection. The central point for different families is mentioned in Table 7-4.

Figure 7-23. Star Connection for Ground

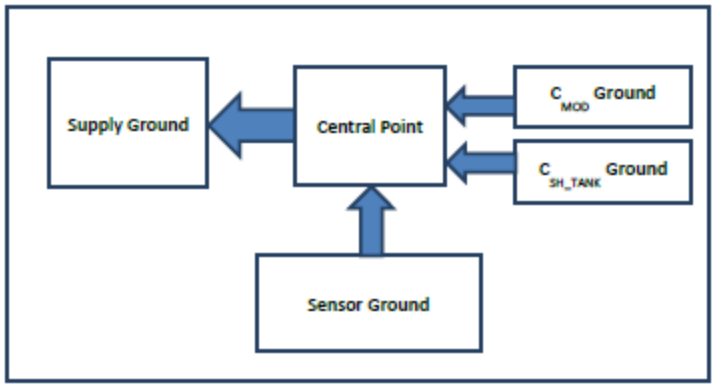


Table 7-4. Central Point for Star Connection

Family	Central Point
PSoC 4000	VSS pin
PSoC 4100/4100M	VSS pin
PSoC 4200/4200M/4200L/PSoC 4-S/PSoC 4100PS	VSS pin
PSoC 4100-BL	E-pad
PSoC 4200-BL	E-pad

- All the ground planes for CapSense should have an inductance of less than 0.2 nH from the central point. To achieve this, place the C_{MOD}, C_{INTx}, and C_{SH_TANK} capacitor pads close to the chip, and keep their ground planes thick enough.

7.4.10.1 Using Packages Without E-pad

When not using the E-pad, the VSS pin should be the central point and the sole return path to the supply ground.

High-level layout diagrams of the top and bottom layers of a board when using a chip without the E-pad are shown in Figure 7-24 and Figure 7-25.

Figure 7-24. PCB Top Layer Layout Using a Chip Without E-pad

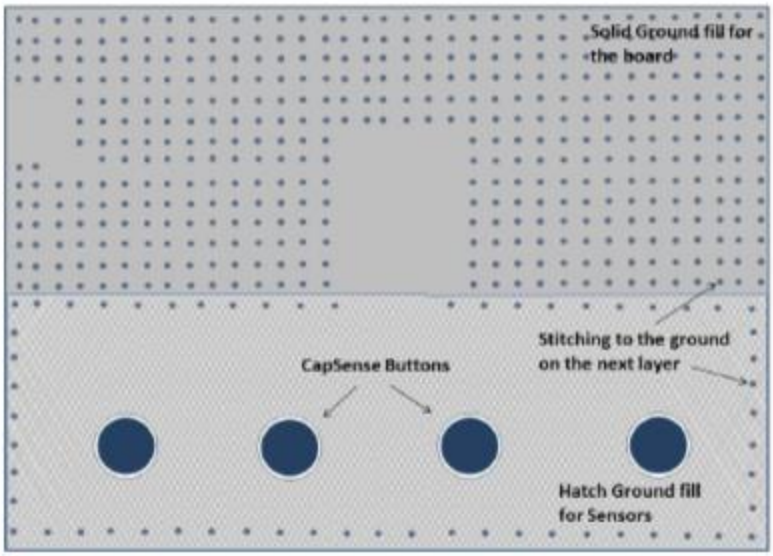
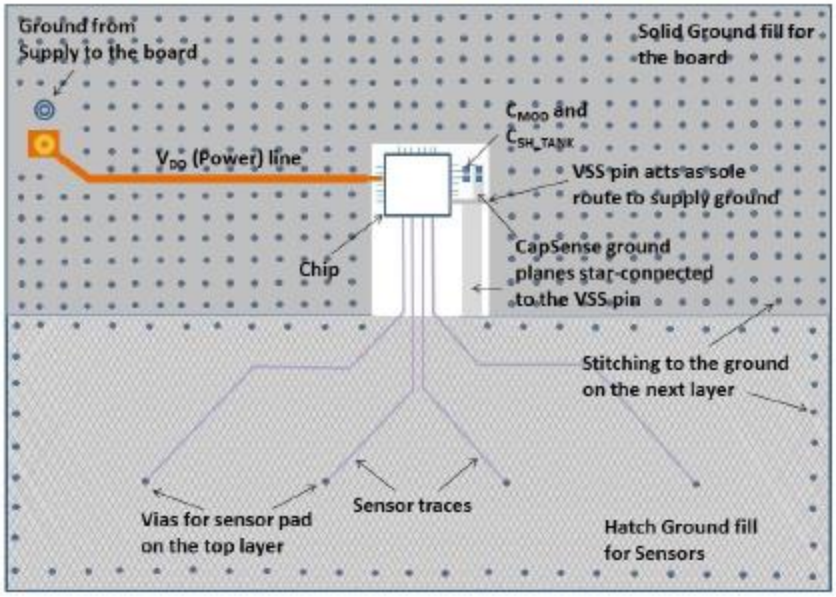


Figure 7-25. PCB Bottom Layer Layout Using a Chip Without E-pad



7.4.10.2 Using Packages with E-pad

If you are using packages with E-pad, the following guidelines must be followed:

- The E-pad must be the central point and the sole return path to the supply ground.
- The E-pad must have vias underneath to connect to the next layers for additional grounding. Usually unfilled vias are used in a design for cost purposes, but silver-epoxy filled vias are recommended for the best performance as they result in the lowest inductance in the ground path.

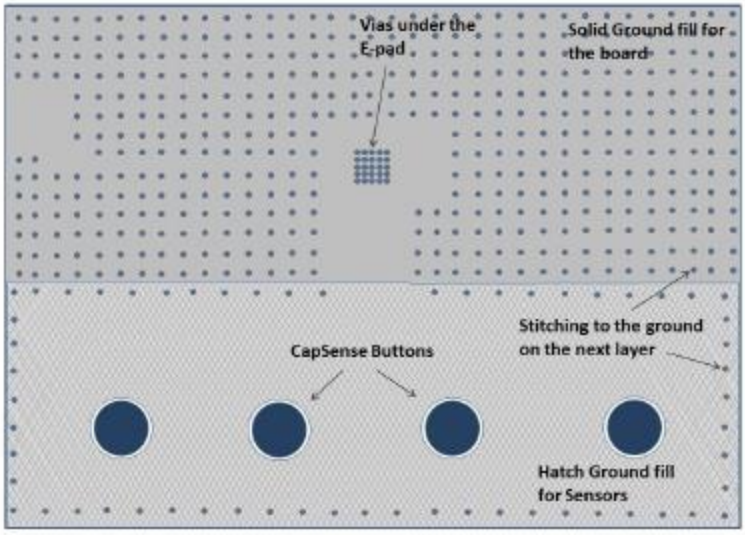
7.4.10.3 Using PSoC 4 BLE Chips

In the case of PSoC 4 BLE chips in the QFN package (with E-pad):

- The general guidelines of ground plane (discussed above) apply.
- The E-pad usage guidelines of Section 7.4.10.2 apply.
- The VSSA pin should be connected to the E-pad below the chip itself.
- The vias underneath the E-pad are recommended to be 5 x 5 vias of 10-mil size.

High-level layout diagrams of the top and bottom layers of a board when using PSoC 4 BLE chips are shown in Figure 7-26 and Figure 7-27.

Figure 7-26. PCB Top Layer Layout with PSoC 4 BLE (with E-pad)



UltraLibrarian and Samacsys downloaded parts:
C:\Users\djjw\AppData\Roaming\SPB_Data\cdssetup\OrCAD_Capture\17.4.0\downloaded_parts\allegropcb

Shannon's adding libraries and parts
https://resources.orcad.com/orcad-capture-tutorials/orcad-capture-tutorial-02-adding-libraries-and-parts

Shannon's assigning footprints tutorial
https://resources.orcad.com/orcad-pcb-editor-tutorials/orcad-pcb-editor-tutorial-01-assigning-footprints-to-your-components

https://www.ema-eda.com/resources/library/orcad-pcb-editor-tutorial-01assigning-footprints-your-components

Shannon's searching for and placing parts in schematic

https://resources.orcad.com/orcad-capture-tutorials/orcad-capture-tutorial-03-searching-and-placing-parts

Shannon's ultralibrarian tutorial
https://www.ema-eda.com/products/orcad/ultra-librarian-for-orcad

SnapEDA
https://www.youtube.com/watch?v=7FTulXYuA-4

Parallel Systems CIS database tutorial
https://www.youtube.com/watch?v=qTzcHqxomOE

Parallel Systems title block tutorial
https://resources.orcad.com/all-videos/title-block

Parallel Systems export to intelligent pdf
https://www.youtube.com/watch?v=7kpMb-jw3ow

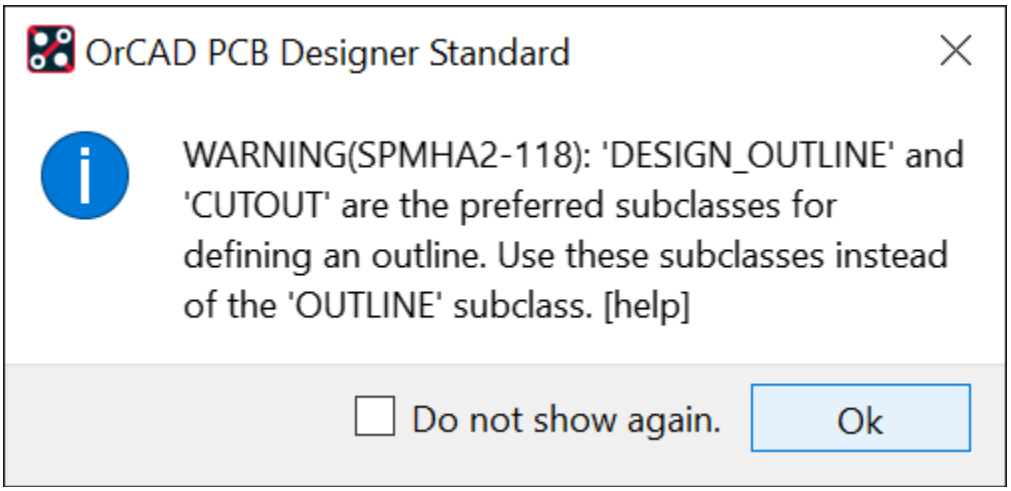
David,

I have attached Layout template for (2,4&6) layer design. You can use the template based on the layer count.

Things to cake care while using this Layout Template:

- As per the requirement please draw the board outline in Active Class – Board Geometry & Subclass – Outline.
- Import Logic on to the design(netlist)
- Please do the changes if any special requirement (Impedance, Soldermask, Silk) is needed in Fab details for Fabricator in Layer -DETAIL1
- Constrains can be changed based on the design requirement.

Regards
PRAO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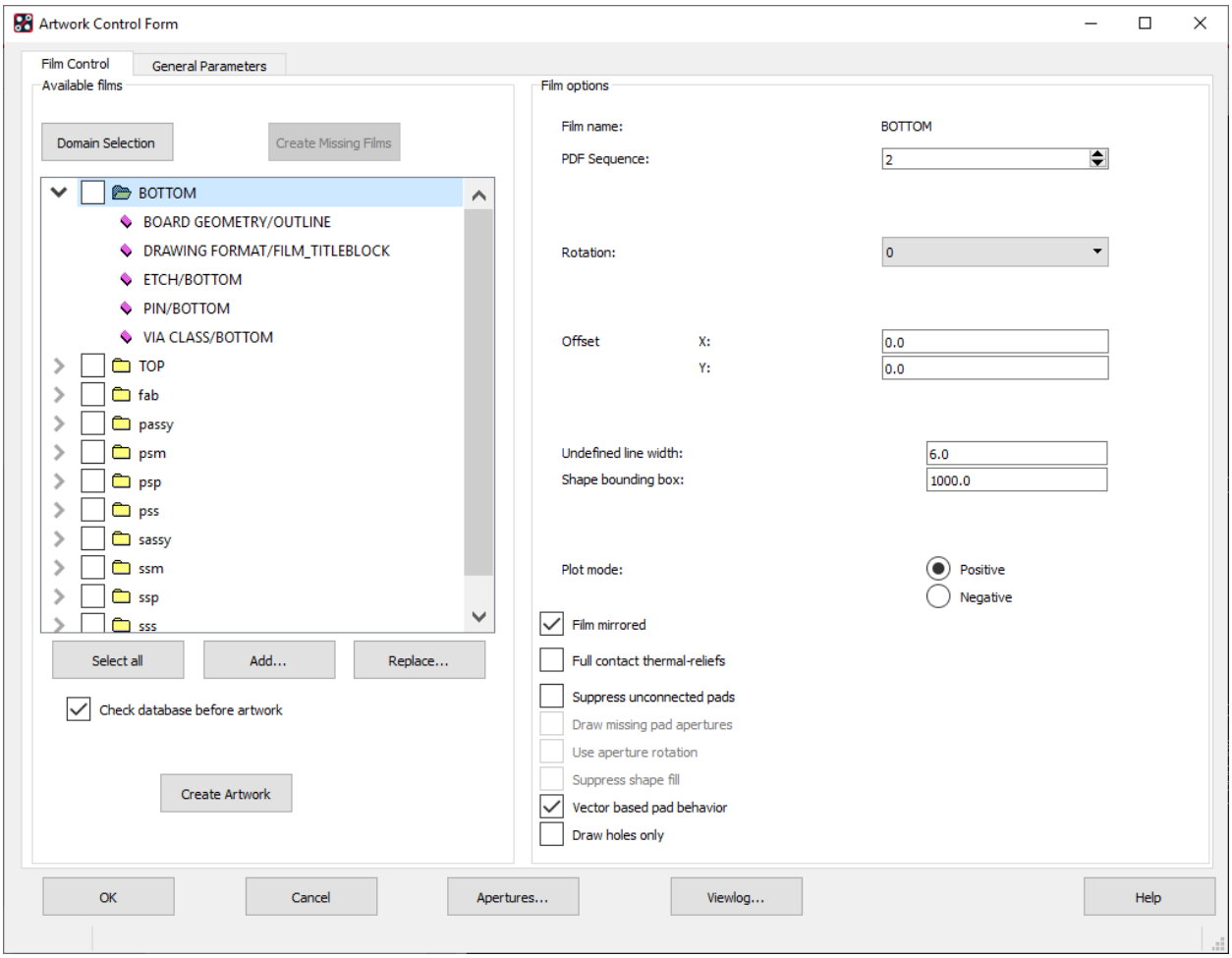
Ok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Film Control
General Parameters
Available films
Domain Selection
Create Missing Films
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BOARD GEOMETRY/OUTLINE
DRAWING FORMAT/FILM_TITLEBLOCK
ETCH/BOTTOM
PIN/BOTTOM
VIA CLASS/BOTTOM
TOP
fab
passy
psm
psp
pss
sassy
ssm
ssp
sss
Select all
Add...
Replace...
Check database before artwork
Create Artwork
Film options
Film name:
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PDF Sequence:
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Rotation:
0
Offset
X:
0.0
Y:
0.0
Undefined line width:
6.0
Shape bounding box:
1000.0
Plot mode:
Positive
Negative
Film mirrored
Full contact thermal-reliefs
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Draw missing pad apertures
Use aperture rotation
Suppress shape fill
Vector based pad behavior
Draw holes only
OK
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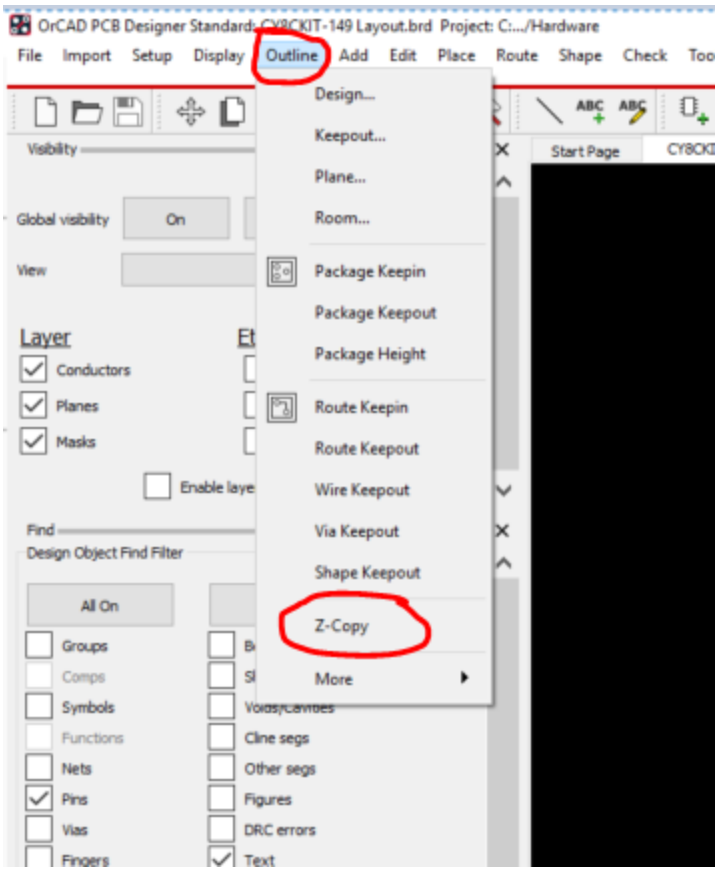
Viewlog...
Help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Keepout...
Plane...
Room...
Package Keepin
Package Keepout
Package Height
Route Keepin
Route Keepout
Wire Keepout
Via Keepout
Shape Keepout
Z-Copy
More
Visibility
Global visibility
On
View
Layer
Conductors
Planes
Masks
Find
Design Object Find Filter
All On
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Comps
Symbols
Functions
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Pins
Vias
Fingers
Cline segs
Other segs
Figures
DRC errors
Text
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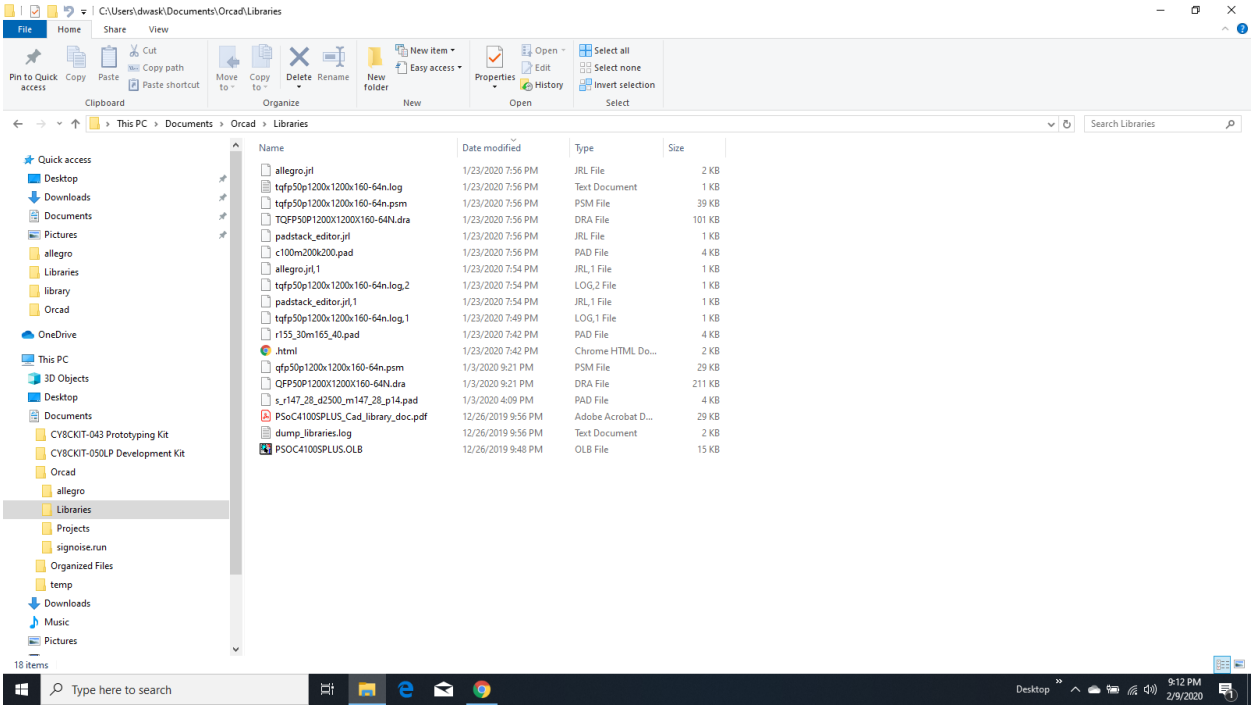
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File Home Share View
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Copy
Paste
Cut
Copy path
Paste shortcut
Clipboard
Move to
Copy to
Delete
Rename
Organize
New folder
New item
Easy access
New
Properties
Open
Edit
History
Open
Select all
Select none
Invert selection
Select
This PC › Documents › Orcad › Libraries
Search Libraries
Quick access
Desktop
Downloads
Documents
Pictures
allegro
Libraries
library
Orcad
OneDrive
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18 items
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Desktop
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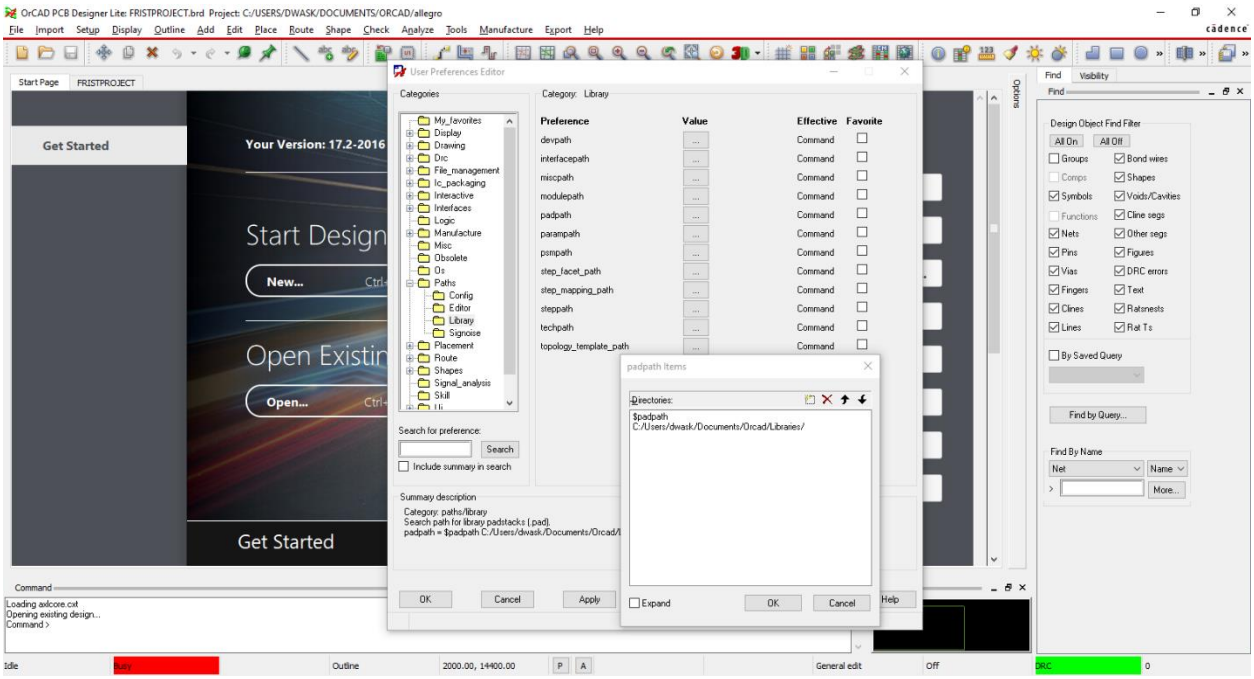
2/9/2020


OrCAD PCB Designer Lite: FRISTPROJECT.brd Project: C:/USERS/DWASK/DOCUMENTS/ORCAD/allegro
File Import Setup Display Outline Add Edit Place Route Shape Check Analyze Tools Manufacture Export Help
cadence
Start Page
FRISTPROJECT
Get Started
Your Version: 17.2-2016
Start Design
New...
Open Existin
Open...
Get Started
User Preferences Editor
Categories
Category: Library
Preference
Value
Effective
Favorite
devpath
interfacepath
miscpath
modulepath
padpath
parampath
psmpath
step_facet_path
step_mapping_path
steppath
techpath
topology_template_path
Command
Loading axlcore.cxt
Opening existing design...
Command >
padpath Items
Directories:
$padpath
C:/Users/dwask/Documents/Orcad/Libraries/
Expand
OK
Cancel
Apply
Help
Find
Visibility
Design Object Find Filter
All On
All Off
Find by Query...
Find By Name
Net
Name
More...
Idle
Ruby
Outline
2000.00, 14400.00
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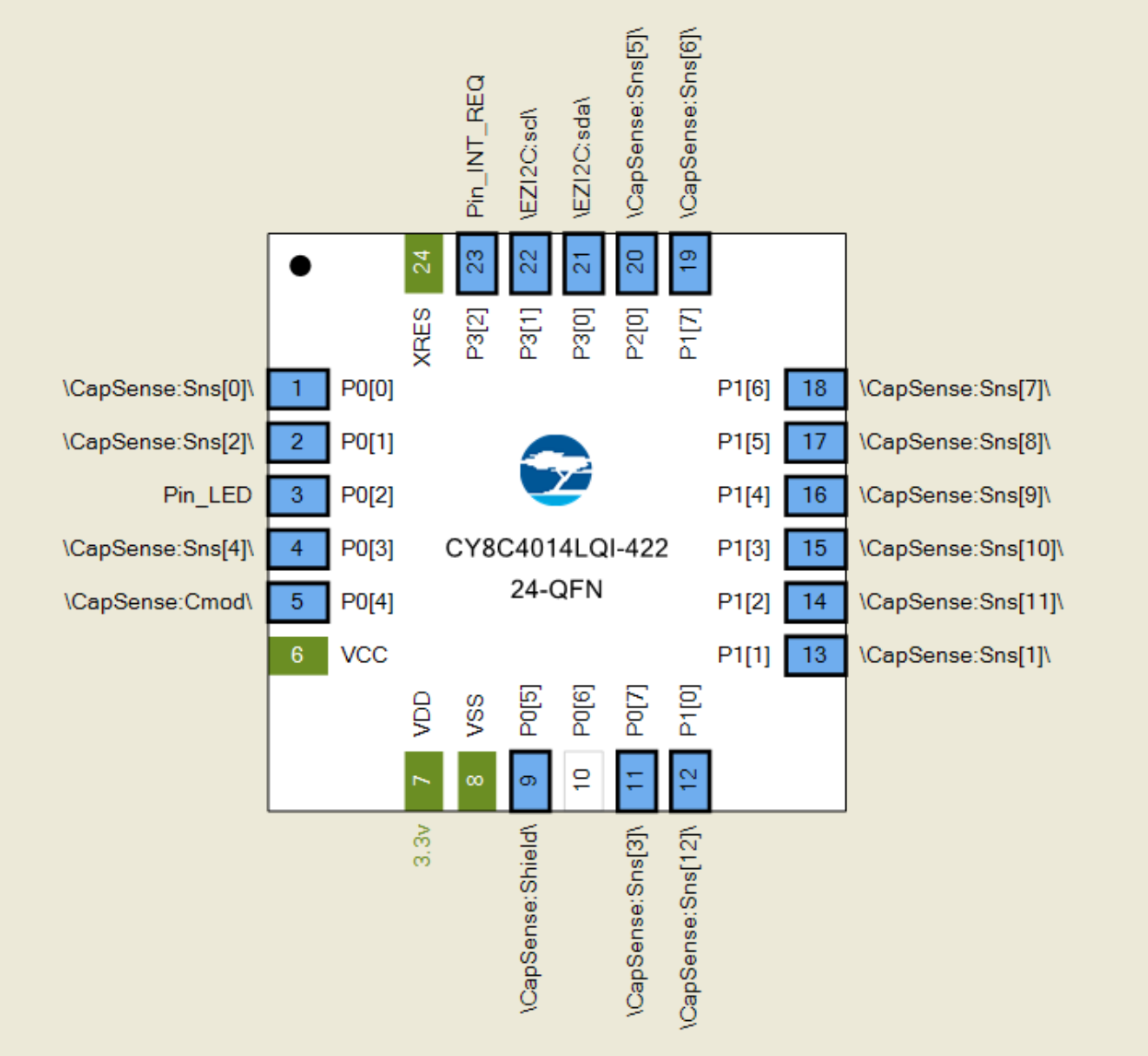
DRC
0



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> Sending response DoneOpenBoard
Opened connection with Capture.
No element found.
last pick: 731.00 -1324.00
Symbol "Cy_Fab_Filmtitle" Selected
last pick: 186.00 1218.00
No element found.
Can not select unplaced component J2.
Can not select unplaced component J2.
No element found.
Can not select unplaced component J2.

Can not select unplaced component J2.
Can not select unplaced component J2.
Can not select unplaced component J2.
No element found.
Can not select unplaced component J2.
Can not select unplaced component J2.
Select elements to place using tree view.
Placing J2 / CON5_BLKCON100VHTM1SQW1005_MINI / BLKCON100VHTM1SQW1005 on Top.
last pick: -625.00 3089.00
Select elements to place using tree view.
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last pick: 152.00 3106.00
Select elements to place using tree view.
last pick: -609.00 3102.00
last pick: -595.00 2909.00
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last pick: -623.00 2734.00
Select elements to place using tree view.
Select elements to place using tree view.
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last pick: 118.00 3084.00
Select elements to place using tree view.
Select elements to place using tree view.
Select elements to place using tree view.
Revising design for compatibility with current software.
Placing U1 / PSOC 4S0_1_QFN50P400X400X60-25N / QFN50P400X400X60-25N on Top.
(SPMHUT-48): Scaled value has been rounded off.
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Select elements to place using tree view.
Revising design for compatibility with current software.
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last pick: -636.00 2817.00
Select elements to place using tree view.

Select elements to place using tree view.
Select elements to place using tree view.
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last pick: -585.00 1311.00
Select elements to place using tree view.
Placing J6 / HEADER 2/SM_BLKCON100VHTM1SQW_1 / BLKCON100VHTM1SQW1002 on Top.
last pick: 220.00 2863.00
Select elements to place using tree view.
Placing J5 / CON8A_BLKCON100VHTM2OEW2008_CON / BLKCON100VHTM2OEW2008 on Top.
last pick: -710.00 1620.00
Select elements to place using tree view.
Revising design for compatibility with current software.
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last pick: 212.00 2142.00
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Select elements to place using tree view.
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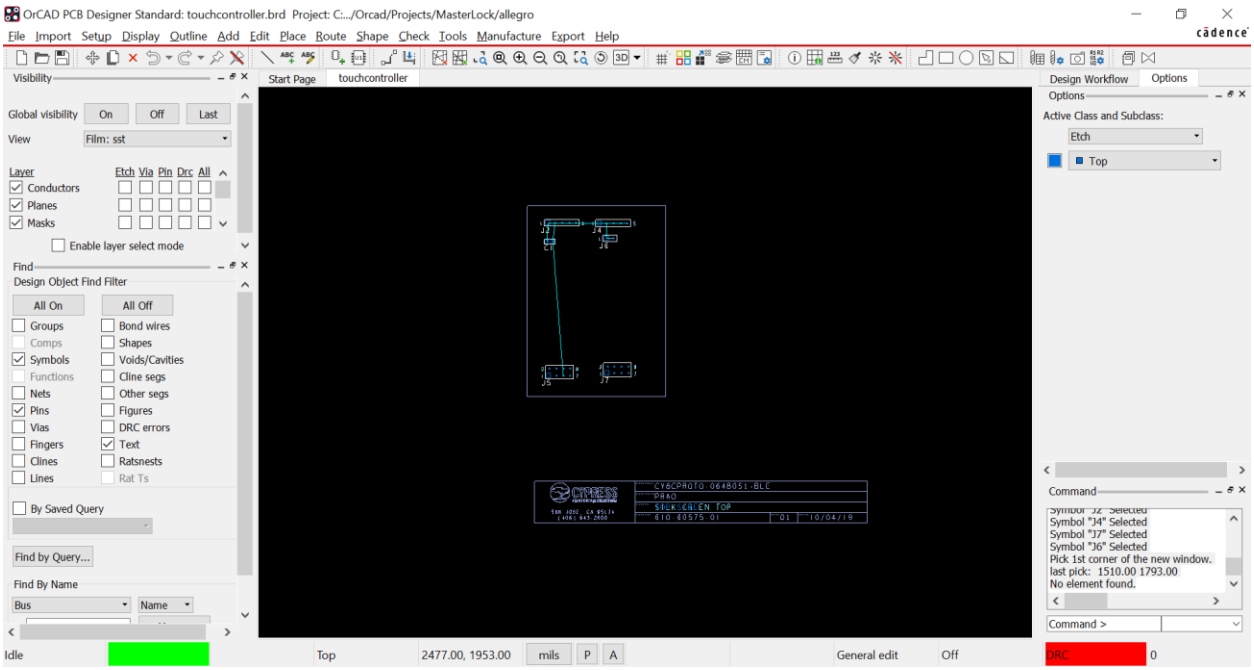
Select elements to place using tree view.



Loading axlcore.cxt
Opening existing design...
> Sending response DoneOpenBoard
Opened connection with Capture.
Enter shape outline.
Pick first point of the next shape.
last pick: 8200.00 11050.00
Pick first point of the next shape.
Enter shape outline.
Pick to complete the window.
Select elements to place using tree view.
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Select elements to place using tree view.
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Select elements to place using tree view.
Placing C1 / CAP NP_SMC0805_1 UF / SMC0805 on Top.
last pick: 8550.00 10625.00
Select elements to place using tree view.
Placing J1 / HEADER 2/SM_BLKCON100VHTM1SQW10 / BLKCON100VHTM1SQW1002 on Top.
Spin the element(s).
last angle: +270.000 Degrees
last pick: 8550.00 10375.00
Select elements to place using tree view.
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last pick: 8575.00 8625.00
Select elements to place using tree view.
Placing J7 / CON8A_BLKCON100VHTM2OEW2008_CON / BLKCON100VHTM2OEW2008 on Top.
last pick: 9400.00 8650.00
Select elements to place using tree view.
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last pick: 9050.00 9725.00
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last pick: 9350.00 9750.00
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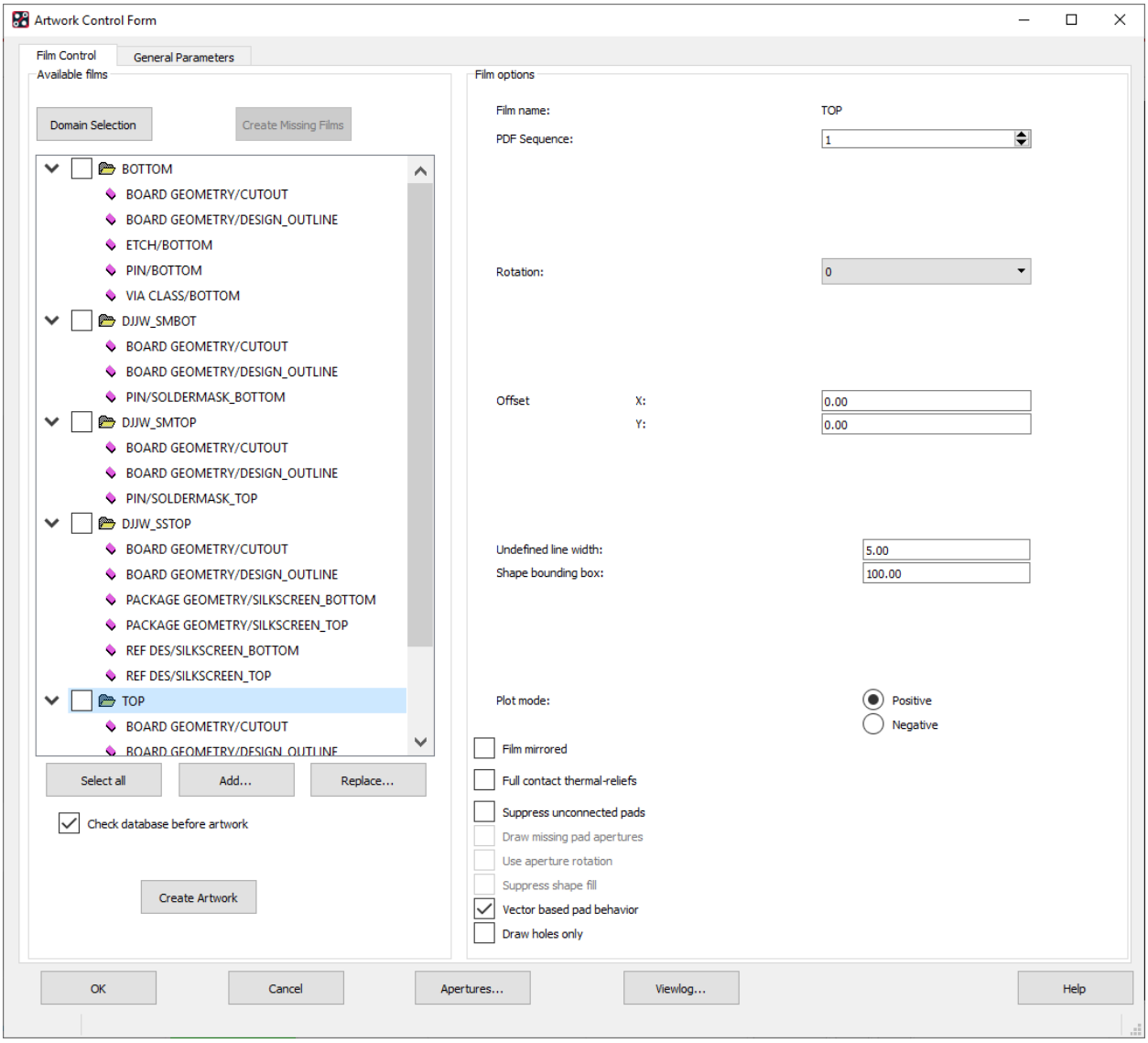
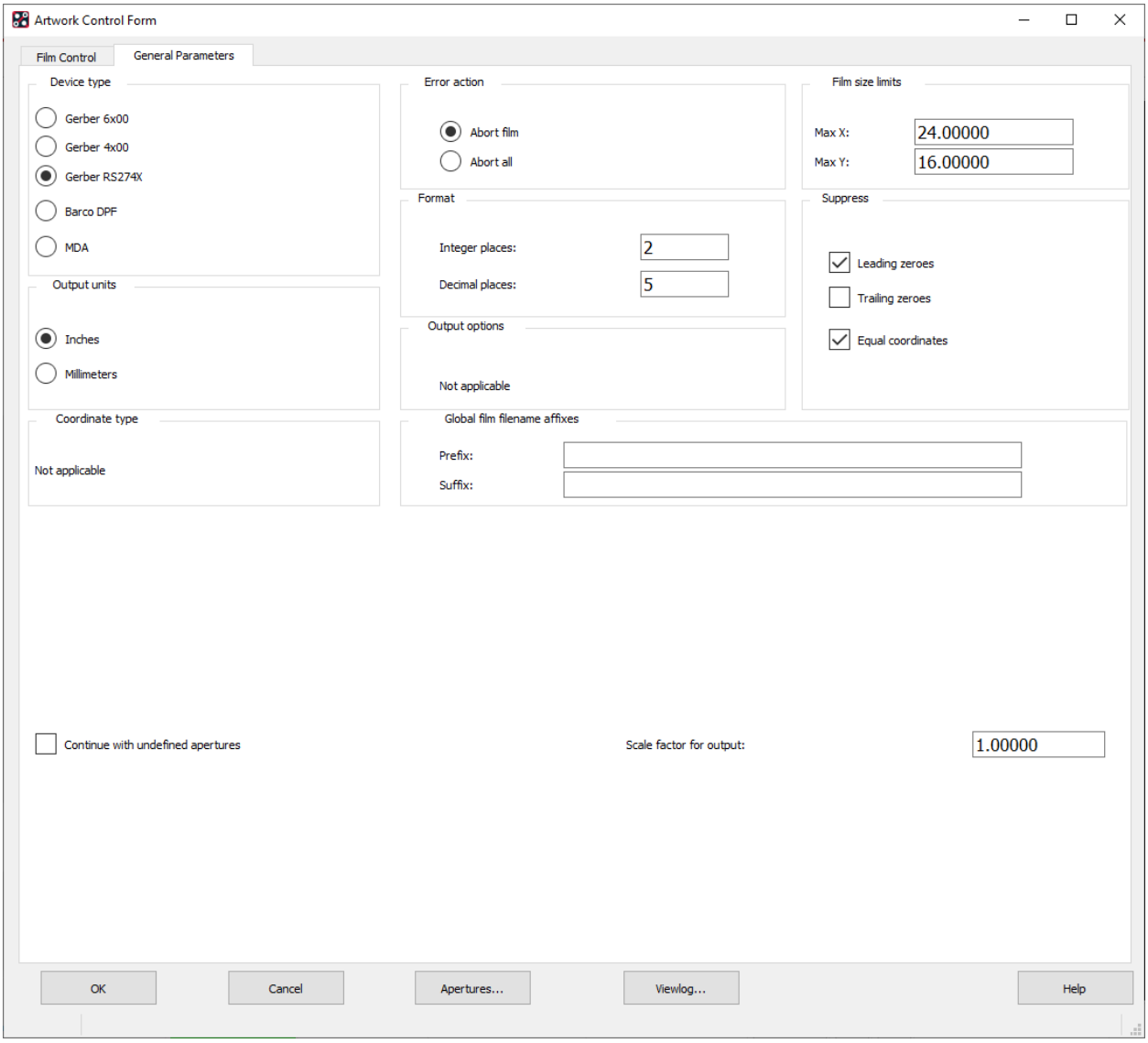
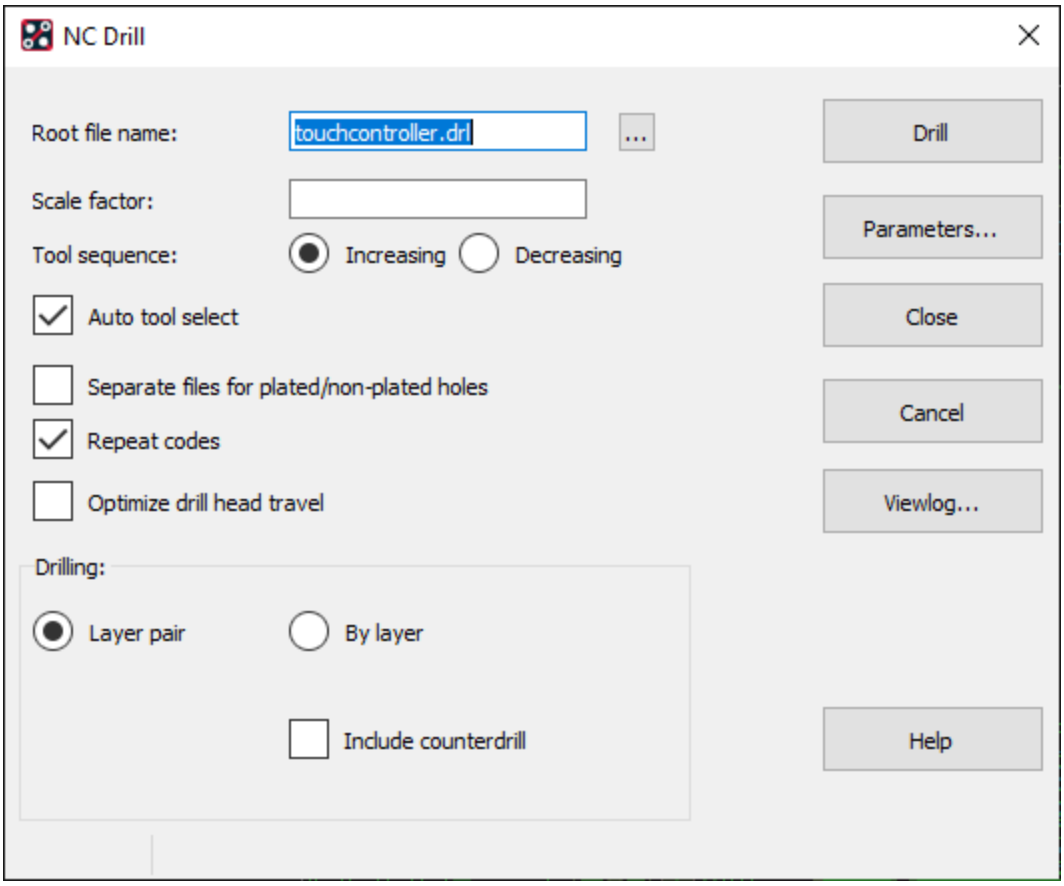
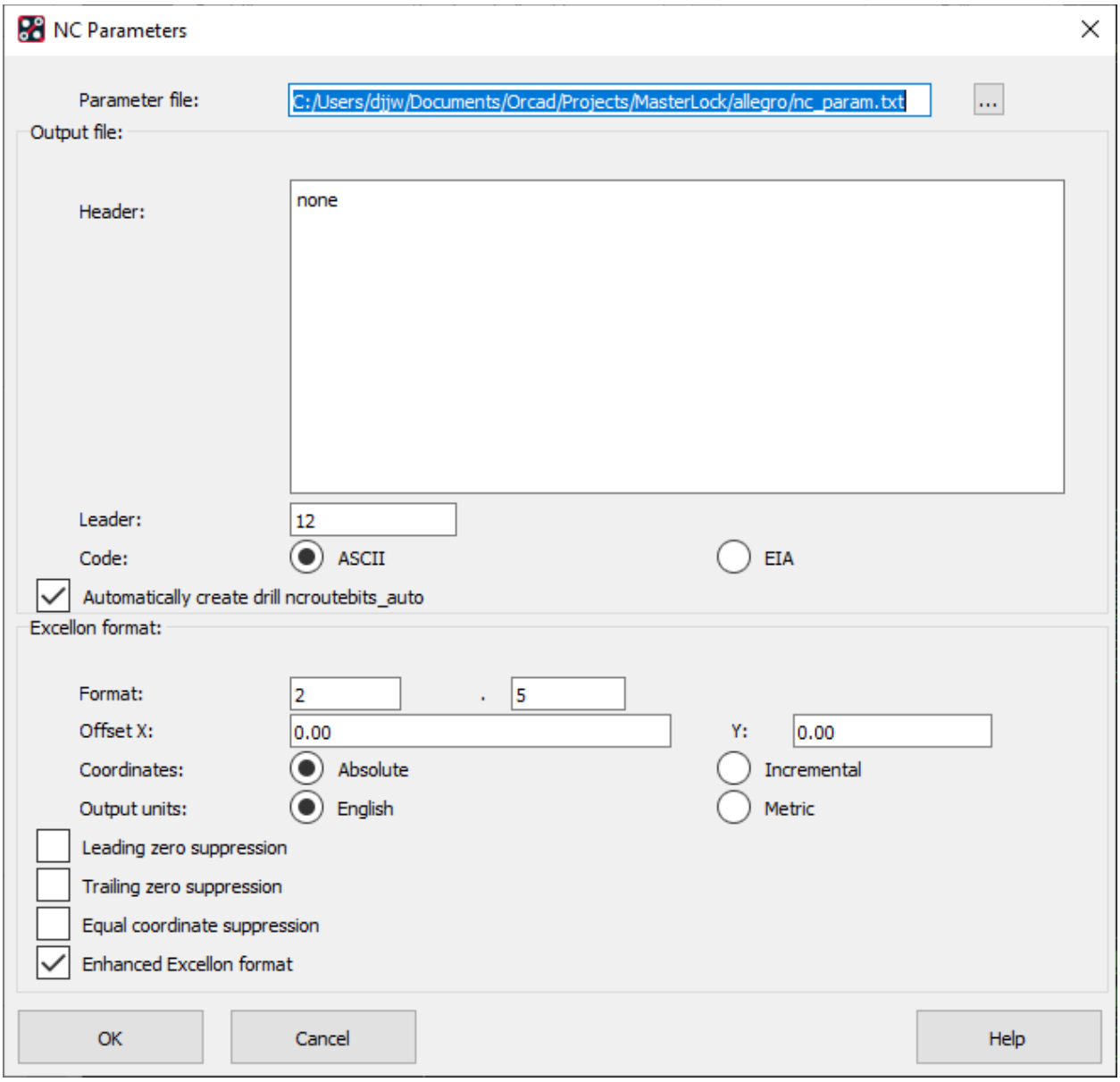

Artwork Control Form
Film Control
General Parameters
Available films
Domain Selection
Create Missing Films
BOTTOM
BOARD GEOMETRY/CUTOUT
BOARD GEOMETRY/DESIGN_OUTLINE
ETCH/BOTTOM
PIN/BOTTOM
VIA CLASS/BOTTOM
DJJW_SMBOT
BOARD GEOMETRY/CUTOUT
BOARD GEOMETRY/DESIGN_OUTLINE
PIN/SOLDERMASK_BOTTOM
DJJW_SMTOP
BOARD GEOMETRY/CUTOUT
BOARD GEOMETRY/DESIGN_OUTLINE
PIN/SOLDERMASK_TOP
DJJW_SSTOP
BOARD GEOMETRY/CUTOUT
BOARD GEOMETRY/DESIGN_OUTLINE
PACKAGE GEOMETRY/SILKSCREEN_BOTTOM
PACKAGE GEOMETRY/SILKSCREEN_TOP
REF DES/SILKSCREEN_BOTTOM
REF DES/SILKSCREEN_TOP
TOP
BOARD GEOMETRY/CUTOUT
Select all
Add...
Replace...
Check database before artwork
Create Artwork
Film options
Film name:
TOP
PDF Sequence:
1
Rotation:
0
Offset
X:
0.00
Y:
0.00
Undefined line width:
5.00
Shape bounding box:
100.00
Plot mode:
Positive
Negative
Film mirrored
Full contact thermal-reliefs
Suppress unconnected pads
Draw missing pad apertures
Use aperture rotation
Suppress shape fill
Vector based pad behavior
Draw holes only
OK
Cancel
Apertures...
Viewlog...
Help


Artwork Control Form
Film Control
General Parameters
Device type
Gerber 6x00
Gerber 4x00
Gerber RS274X
Barco DPF
MDA
Output units
Inches
Millimeters
Coordinate type
Not applicable
Error action
Abort film
Abort all
Format
Integer places:
2
Decimal places:
5
Output options
Not applicable
Film size limits
Max X:
24.00000
Max Y:
16.00000
Suppress
Leading zeroes
Trailing zeroes
Equal coordinates
Global film filename affixes
Prefix:
Suffix:
Continue with undefined apertures
Scale factor for output:
1.00000
OK
Cancel
Apertures...
Viewlog...
Help


NC Drill
Root file name:
touchcontroller.drl
...
Drill
Scale factor:
Parameters...
Tool sequence:
Increasing
Decreasing
Auto tool select
Close
Separate files for plated/non-plated holes
Cancel
Repeat codes
Optimize drill head travel
Viewlog...
Drilling:
Layer pair
By layer
Include counterdrill
Help



What files do you need to manufacture my US Quickturn PCBs?
The following files need to be compressed into one ZIP file and uploaded through the US Quickturn PCBs web site at order placement. Our web application will only accept one ZIP file per order. Your file set needs to be complete with the following data:
1. Gerber files in 274X or 274D formats. (274D format will require an aperture list or environment file)
2. Excellon2 NC drill file.
3. Drill tool list specifying finished hole sizes, hole quantities, and plated/non-plated holes.

https://www.sunstone.com/pcb-products/pcb-manufacturing/file-requirements

Supported Design File Types:

- Gerber files (**RS274-X preferred**) including
  - Excellon Drill Files
  - Drill Tool List (sometimes embedded in Drill File)
  - Top and Bottom Copper Layers (positive polarity)
  - Inner layers (polarity based on design)
  - Top and Bottom Soldermask (negative polarity - presence of data will represent the absence of soldermask on the board. Outline only will cover the board entirely with soldermask)
  - Top and Bottom Silkscreen (positive polarity)
  - Board Outline (if not already present on another layer)
  - Aperture / D-Code List (if file set is not RD274-X compliant)
  - Readme file or fabrication drawing with file information to match your uploaded files listing the Gerber layers and the NC drill files in the order they will be built.
  - Material layer stack up (dielectric thicknesses and copper weight requirements) if requesting a non-standard stack up.
  - **Any additional PCB files will be ignored for an Engineering Level = Limited Review order.**
- Native Design Files submitted from:
  - EAGLE
  - Altium (Protel)
  - OrCAD (with .MAX file extension)
  - Ultiboard (National Instruments' Circuit Design Suite)
  - IVEX
  - PCB123

If your needs go beyond our **Limited Review** Engineering Level capabilities, chose Engineering Level = Full Review (NRE) in the OneQuote form. Your files will undergo a design review by our Pre-engineering team looking for manufacturability and insure that the print notes, PO notes and other files included are read and followed. This will also allow Sunstone to make small edits to the files to improve manufacturability and NRE charges will apply.

Positive Polarity *- When the elements drawn in the CAD file represent the copper / silk or soldermask features with the polygons (usually colored). i.e if the colored portion of the file layer represents the data portrayed it is considered positive polarity*

General Requirements for Drill File Submission

- Must be submitted in Excellon format
- Must be ASCII text viewable. Please open with "Word" or "notepad" to verify a numeric list of X & Y coordinates. (There should be no strange graphical characters).
- PCB drill files should not contain "G01", "G54" or and reference to "D" codes when opened in a text editor. (This indicates a Gerber format and is most likely a drill drawing rather than an NC file).
- Properly formatted PCB Drill files have sizes separated with "T" codes that indicate tool numbers. (T01, T02, etc.)
- A tool report with the drill sizes necessary (if not contained in the drill file header).
- Include a fab drawing, NC Drill File, or Gerber file for slots and / or cutouts. This file should define the slot or cutout size, shape and location.
  - To achieve a plated slot or cutout place the feature on the drill layer and include an outerlayer pad at least the size of the slot or cutout to be plated. Maximum diameter for a plated feature is 0.250"
  - Non-plated slots or cutouts should be placed on the outline layer. There is no limit to the size or shape.
  - The largest drill size available is a 0.250". All holes >0.250" are considered a cutout as they require additional programming and drill time.

STANDARD OPERATING PROCESS:

- All PCB holes are viewed from the top layer of the board.
- All holes will be treated as through holes unless specifically indicated otherwise and indicated on the OneQuote order.

RESTRICTIONS FOR LIMITED REVIEW BOARDS:

- No blind or buried vias are supported.
- Holes marked in the files as non-plated through holes cannot be guaranteed to remain unplated. (removing the copper pad on the top and bottom layer of the hole will provide the best opportunity to achieve non-plated holes).
- All holes > 0.250" will be non-plated and must be ordered as a cutout to maintain the correct size.
- Spacing between holes at least 0.012" (edge to edge). Holes that do not meet this requirement will be placed on hold until resolved.
  - For "perforation holes" between boards Sunstone may remove or decrease diameter to increase the distance between holes.
- Limit number of holes to less than 50 per square inch.

- Sunstone cannot create the drill file from a Gerber file, fab document or drawing. Please include an Excellon formatted file.
- Specified holes < 0.018" will be treated as vias and drilled approximately the same size as specified in the drill file.
- Smallest drill size available for ValueProto PCBs is a 0.0135". Any holes smaller than 0.0135" will be increased to this size.
- Slots or cutouts are not available for a ValueProto PCB.
- Holes that overlap the board edge (**castellated holes**) cannot be guaranteed to meet IPC standards with a **Limited Review** selection. The holes may not be centered in the route path, plating may be removed from the barrel during routing and there may be excess copper on the board edges around the drilled holes. If you require conformance to IPC requirement, please select an Full Review (NRE).

PERIMETER PCB ROUTING DETAILS (INDIVIDUAL)

Sunstone will program the circuit board routing from the outline of the PCB. The outline must be continuous with overall board dimension calculated from the center of the outline.

- The standard tolerance for online product for the dimensions is +/- 0.010".
- Copper backset of 0.020" is recommended to prevent damage of the copper features during the routing process.
- Round or odd shapes are allowed if the guidelines are followed.

PCB ROUTING RESTRICTIONS

- Limit of 1 router pass to the outside perimeter of the PCB drawn with a continuous line.
- Connected or panelized boards (submitted as such in files) will not be cut apart by Sunstone.
  - Sunstone recommends that you separate these boards that you wish to cut apart by at least 0.100"
  - Tools such as a Dremel, rotary cutter or small saw work well to cut these boards apart.
- Breakaway or perforation holes in your design: please maintain at least 0.010" edge to edge spacing between these holes (minimum hole size 0.0135")
- Inside chamfer are not recommended. (Inside cut made usually at 45º angle to the adjacent edge). If necessary please allow for a 0.093" diameter router (inside radiuses and copper to board edge).

Perimeter PCB Routing Details:

Our process will program the circuit board routing automatically by reading the path of your outline. The outline must be a continuous line. The board dimensions are determined from the center of the line used to draw the outline and will be routed to a +/- 0.010" tolerance. You should leave 0.020" space from the routed edge of the board to the nearest copper feature.

PCB Routing Restrictions:

1. Limit to 1 pass of outside board perimeter using a continuous line.
2. If you are adding your own break away or perf holes, please leave at least 0.010" between holes.
3. Inside Chamfer or an inside cut made usually at a 45 degree angle to the adjacent edges are not recommended. If necessary to your design, please allow for a 0.093" diameter router on the inside radius.

This checklist is a tool to help ensure that you have the correct Gerber PCB layout guidelines before submitting your order.

Gerber PCB File Submission:

- My files are contained in a single compressed file (.zip) containing only the required files
- Once my order is put into process no additional changes to the files will be permitted.

Gerber Layer File Preparation:

- Preview files in a Gerber viewer prior to submission to insure that the files have exported as you expected.
- Verify that the board design fits into the Sunstone manufacturing Capabilities
- Gerber files format is either RS274X (embedded apertures) or RS274D (with aperture list separately)
- All external layers (top and bottom) are *positive polarity*
- Files do not require manual merging
- Power / Ground / mounting holes have sufficient clearance to the copper layers to prevent shorting.

Single SIded - 1 layer Boards: PLEASE PREVIEW ALL 1-Layer Files

- Preview files as if viewed looking through the top (component) layer side.
- Right Reading copper text is drawn on the single side (+silk screen if applicable)
- Single sided boards (**Limited Review** - Prototype) will contain plated through holes (pads will be added to the opposite side)

Multilayer Boards:

- Internal layers are individual layers (either positive or negative polarity) that do not require merging.
- Internal ground layers contain sufficient clearances for all holes including non-plated and mounting holes.
- Ground and Power layers are marked to indicate proper polarity

Board Outline:

- Cut shape is drawn around board perimeter using a continuous line.

Drill Setup:

- ASCII text file provided showing the X and Y coordinates of the holes.
- My NC drill file is NOT a Gerber layer or drawing.
- Separate tool size list included or the tool sizes are listed within the header of my Excellon drill file.

Slot / Cutouts:

- These features are indicated on the outline layer.
- The minimum width for a plated slot is 0.020"
- The minimum width for a non-plated slot is 0.031"

Solder Mask

- Top and Bottom (as required) files have been included
- Solder mask swell is at least 0.008" larger than the copper features to keep solder mask off of copper features.

Silk Screen:

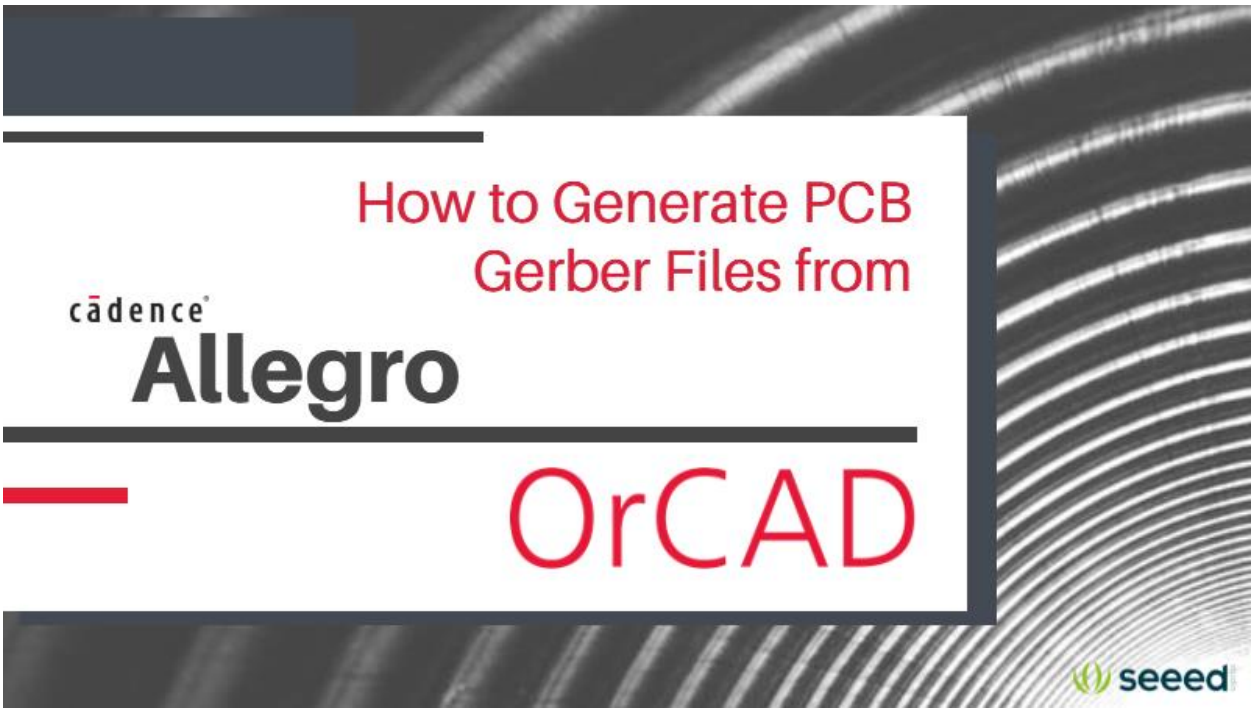
- Top and Bottom (as required) files included
- Silk screen is drawn with a minimum 0.006" aperture line width to ensure legibility.

Native File Upload:

- For EAGLE Users: please include a readme with your object layers defined. If these are not documented:
  - Top silk layer: Sunstone will default to object layer 21 (tplace) and 25 (tnames)
  - Bottom silk layer: Sunstone will default to object layer 22 (bplace) and 26 (bnames)
  - All midlayer object layer selections MUST be documented in your file set.

How to Generate PCB Gerber Files from Cadence Allegro/OrCAD – the Easy Way

By Carmen Zheng 2 months ago



Cadence Allegro and OrCad are the oddballs of the PCB EDA software giants. The software takes a bottom-up approach using various tools to make individual parts from pads to the final PCB layout. Those used to more beginner-friendly and self-explanatory programs such as KiCad and Eagle may be driven crazy by OrCad/Allegro's counter-intuitive design flow and excessive right-clicking (me included). On the other hand, despite the steep learning curve, those weaned on the software find the level of customization and detail appealing, and develop a better overall understanding into what makes a printed circuit board and, more importantly, how this is communicated in the production files. It's probably for this reason why OrCad/Allegro is still very popular and is often the software of choice for schools and businesses.

This comes at a price though, for both the user and PCB fab houses, particularly when it comes to exporting Gerber files for manufacture. The number of steps involved to just export a set of Gerber files leaves us craving a CAM file feature like in Autodesk Eagle. And we can't help give off a little sigh every time we see

the *.art* extension. But actually, the export method has a lot in common with Eagle and is difficult to get wrong with this method.

While the built-in documentation is comprehensive, simple, up-to-date and jargon-free guides for OrCad/Allegro are rather scarce. Methods for exporting Gerber files from OrCad/Allegro vary and are sometimes incomplete or not fit for the purpose of sending off the data to be manufactured for example with the Seeed Fusion service.

We once had an entire class of students fumble with problems with board outlines and just getting the bare minimum data to us was a pain. Even the professor was struggling.

Seeed Fusion Customer Service Operative

So, if you are struggling to export PCB Gerber files from OrCad or Cadence Allegro successfully, we hope this guide will help you with your woes once and for all.

To begin with, what we and most PCB fab houses typically need is contained in the list below:

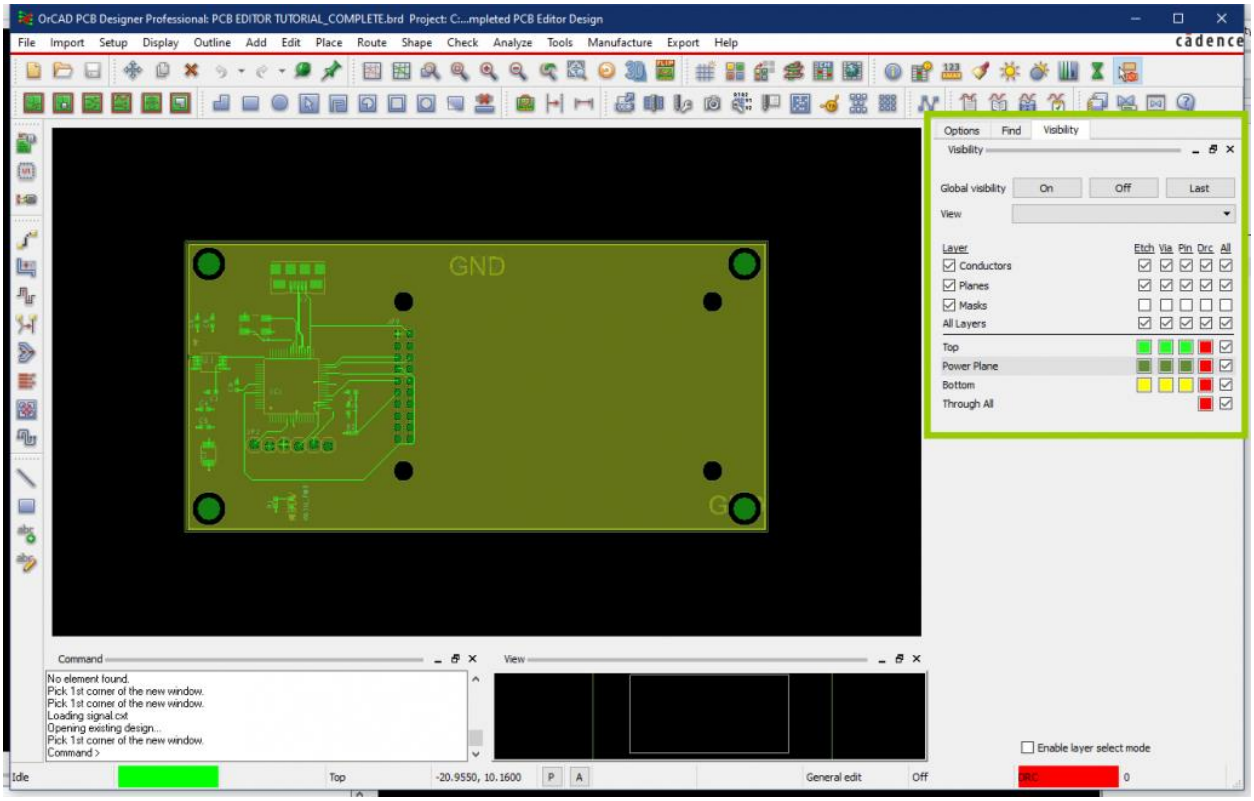
Gerber/Drill Layer	OrCAD/Allegro Subclass	
Top Silkscreen (optional)	GE – Silkscreen_Top	.G
	CO – Silkscreen_Top	
Top Solder Mask	SU – Soldermask_Top	.G
Top Copper	SU – Top	.G
Outline/Mechanical	GE – Design_Outline	.G
	GE – Cutout	
Bottom Silkscreen (optional)	GE – Silkscreen_Bottom	.G
	CO – Silkscreen_Bottom	
Bottom Solder Mask	SU – Soldermask_Bottom	.G
Bottom Copper	SU – Bottom	.G

Drill File	NC Drill	.D
Top Paste (for stencils)	SU – Pastemask_Top	.G
Bottom Paste (for stencils)	SU – Pastemask_Bottom	.G

Apart from the silkscreen layers, all the other layers are pretty much essential for a typical two-layer board. For multilayer boards, make sure you export all the copper layers as necessary. If you need the paste layers to make PCB stencils, you can export them in a similar way.

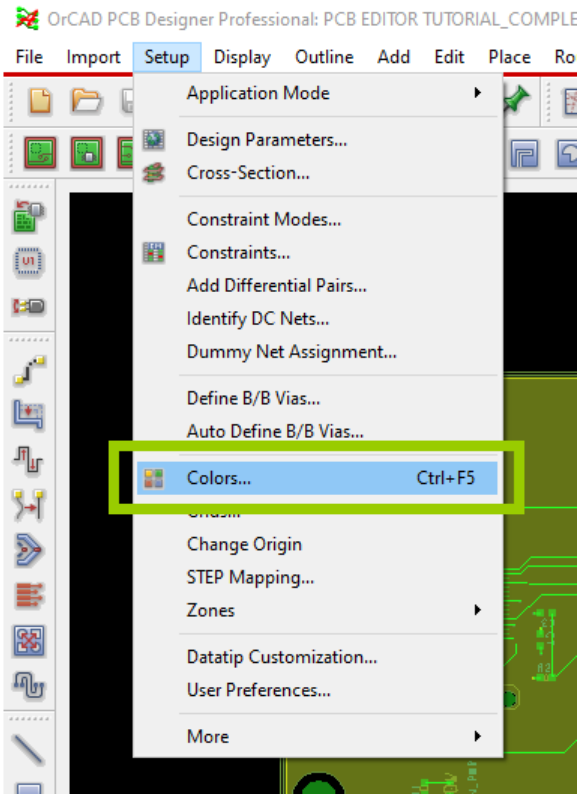
In OrCad/Allegro, these Gerber 'layers' are referred to as '*films*', a reference to how photo imageable films are used to print the pattern onto the board.

Before we export these, we'll make some data-sets containing the essential features. These are based on *Views* that you may already be familiar with while making the layout since they are useful in switching between the many layers.



By default, the ***Visibility*** panel is on the right of the screen when modifying a .brd file. Here you can select different subclasses of the PCB to display on the main

window. What we want to do is group sets of features for each of the respective Gerber layers in a *View*. At first, the *Views* drop-down box may be empty. But we can add some by doing the following:

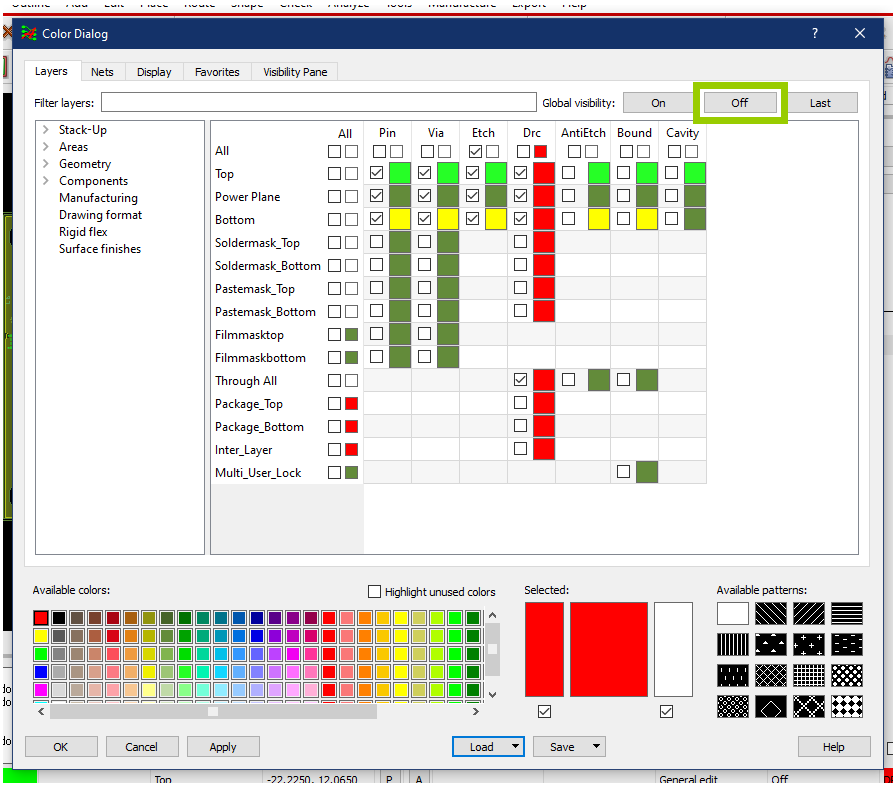


Go to ***Setup*** on the main toolbar and ***Colors…*** to open up the *Color Dialog* or press ***Ctrl+F5*** for the shortcut. Don't be put off by the sheer number of options and boxes. OrCad/Allegro has a wealth of features for many advanced and specialized designs that we'll probably never use. As one becomes more familiar with PCB design, these other features may come in handy.

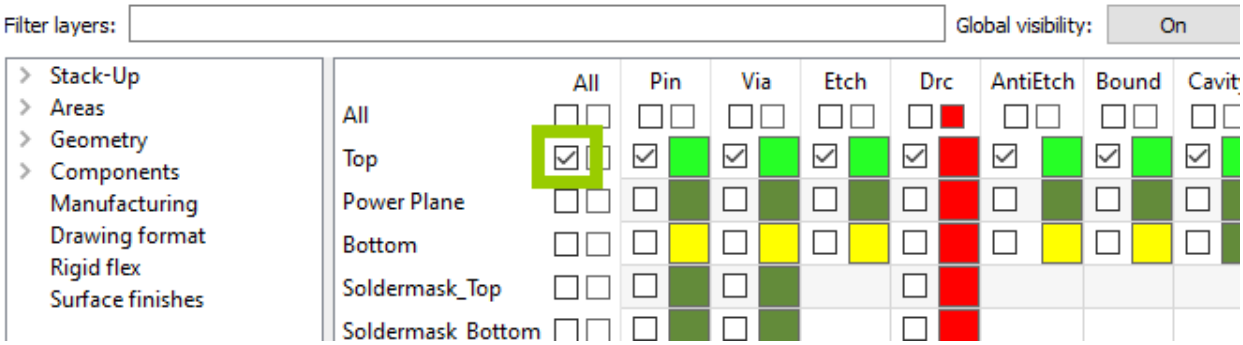
Stack-up is the class that appears when the dialog is opened up. Here the information, or objects, for the copper, solder mask and paste layers are available. Repeat the below instructions for each layer to group the necessary objects and save them into a *View*.

1. Open the *Color Dialog* window by going ***Setup*** -> ***Colors…***

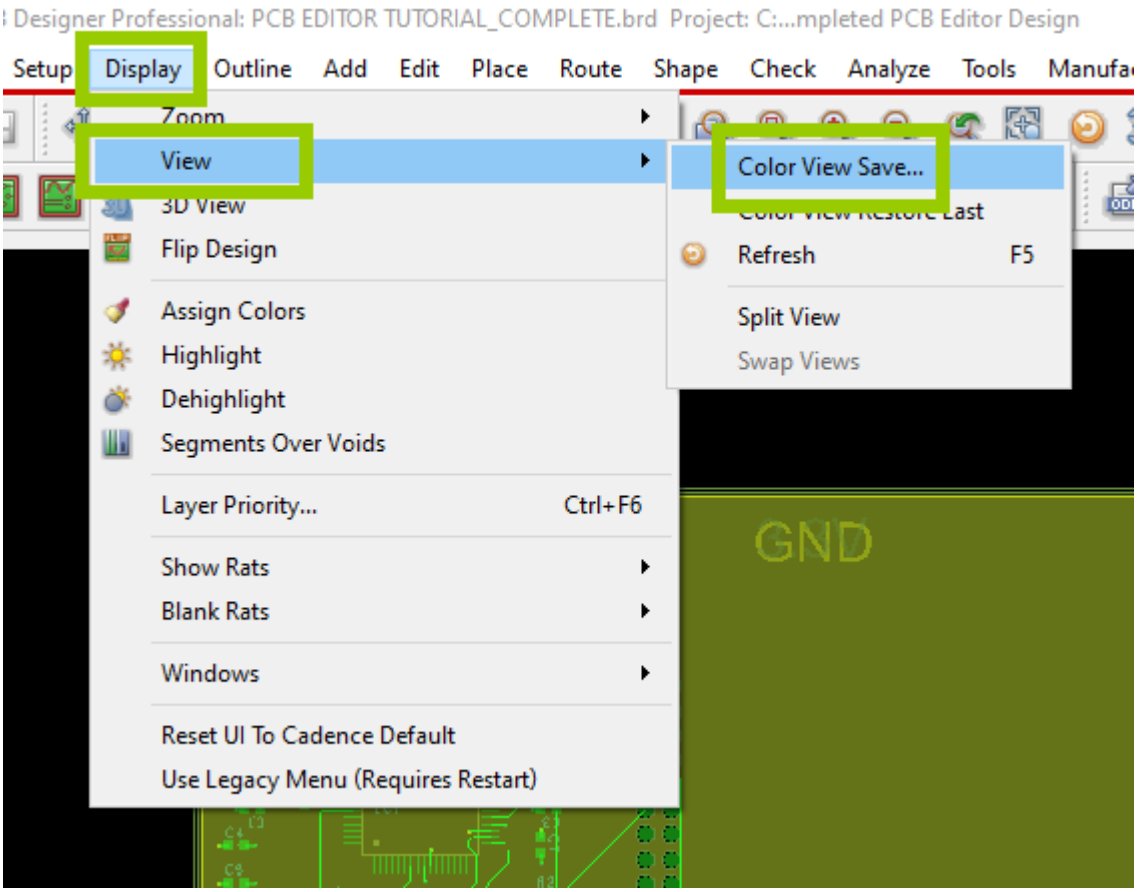
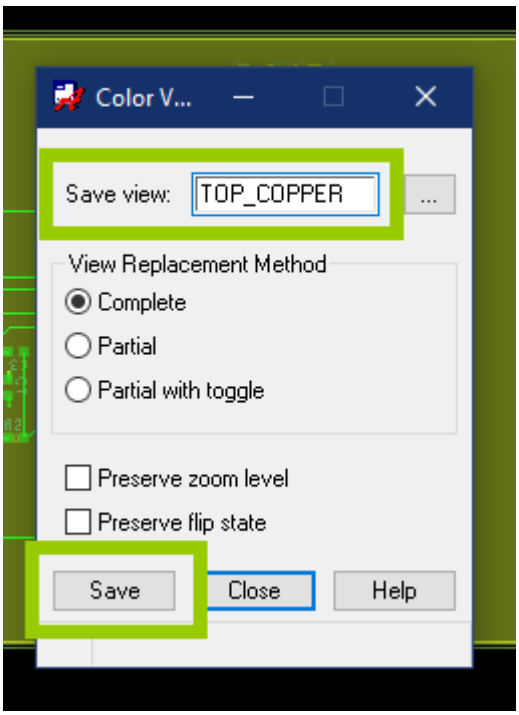
2. Turn off all layers by setting *Global Visibility:* ***Off*** on the top right.



Then, click the leftmost ***All*** checkbox by the corresponding sub-class for the layer you are making (e.g. Paste Top). This selects all the boxes to the right and these objects will appear on the main window. Click ok to exit.



Save this view by going to ***Display*** on the main toolbar -> ***View*** -> ***Color View Save…*** Then give the layer a name (you can refer to the table before), click save and close the window.

- 
Designer Professional: PCB EDITOR TUTORIAL_COMPLETE.brd Project: C:...mpleted PCB Editor Design
Setup
Display
Outline
Add
Edit
Place
Route
Shape
Check
Analyze
Tools
Zoom
View
3D View
Flip Design
Assign Colors
Highlight
Dehighlight
Segments Over Voids
Layer Priority... Ctrl+F6
Show Rats
Blank Rats
Windows
Reset UI To Cadence Default
Use Legacy Menu (Requires Restart)
Color View Save...
Refresh F5
Split View
Swap Views
GND
- 
Color V...
Save view: TOP_COPPER
...
View Replacement Method
Complete
Partial
Partial with toggle
Preserve zoom level
Preserve flip state
Save
Close
Help

Repeat this for the other layers, both top and bottom for a two-layer board, remembering to uncheck all other layers each time.

Copper Layers (repeat for bottom):
– ***Stack-Up*** -> ***Soldermask_Top***

Solder mask Layers (repeat for bottom):
– ***Stack-Up*** -> ***Soldermask_Top***

Paste Layers (repeat for bottom):
– ***Stack-Up*** -> ***Pastemask_Top***

For the silkscreen layers, they consist of two parts: the component outline and the designator or reference. The former is located under *Stack-Up* class like before but the designators are located under *Components*.

Silkscreen (repeat for bottom):
– ***Geometry*** -> ***Silkscreen_Top*** – For component outlines
– ***Components*** -> ***Silkscreen_Top*** – For component designators

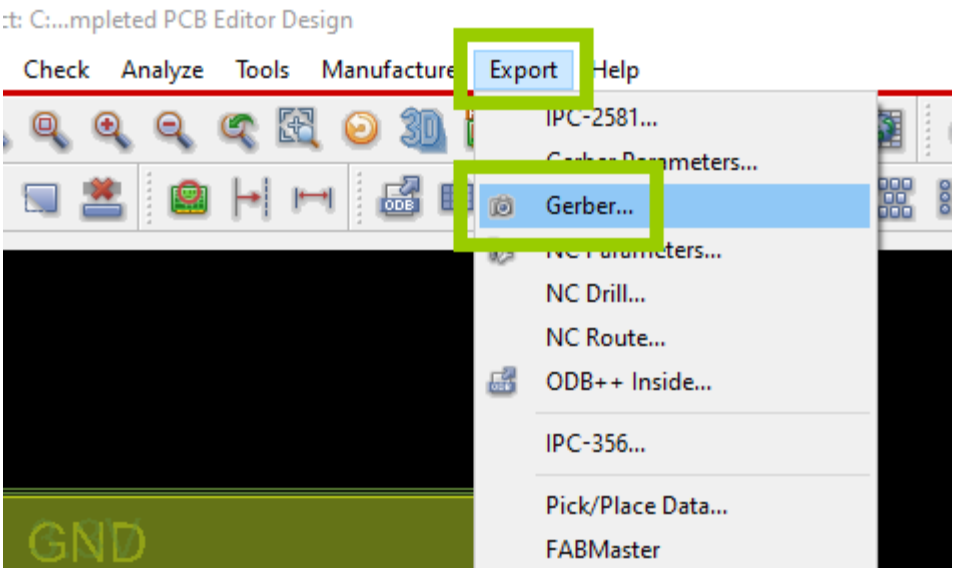
For the board outline, we personally prefer that all the mechanical elements such as cutouts, v-cuts and the board outline be included in the outline Gerber layer. This avoids confusion and is clearer for the engineers reviewing the files. To do this make a view that includes the following:

Outline Layer:
– ***Geometry*** -> ***Design_Outline***
– ***Geometry*** -> ***Cutout***

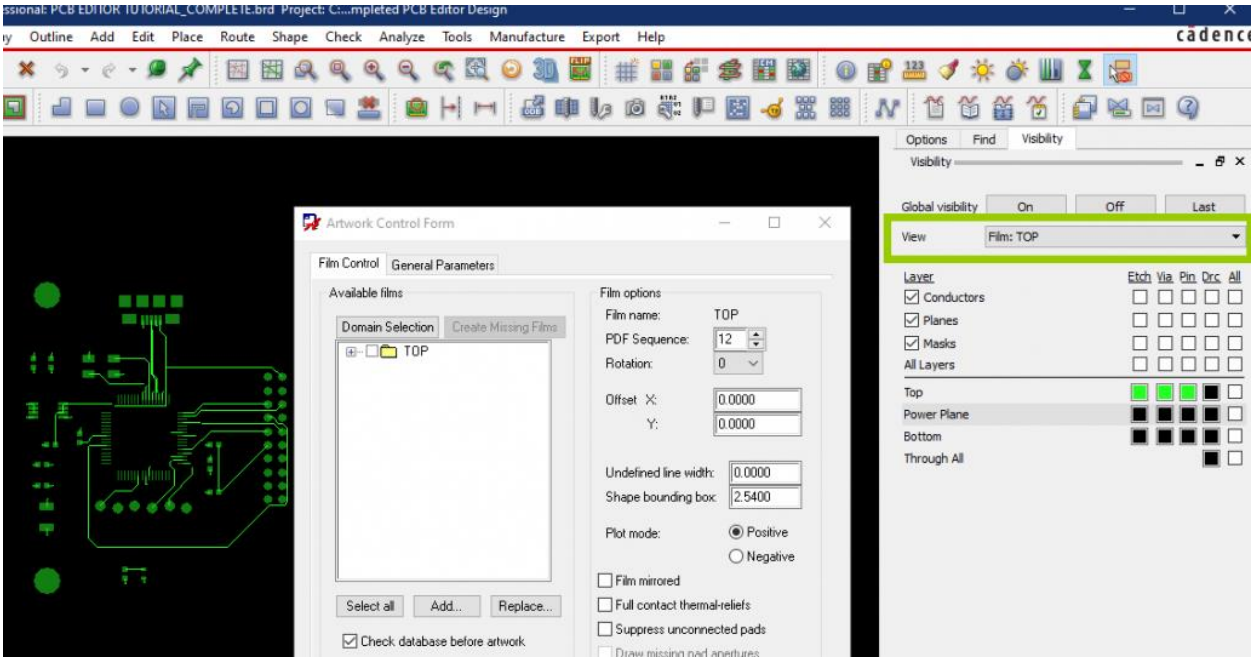
And if there are features drawn in other sub-classes they should also be included. Some manufacturers ask that the board outline be included in the other layers as well. If that is the case then you can just select these subclasses as well when creating the other layers.

Now that we have our views saved, they will appear in the *Views* drop-down list. These are useful in reviewing your design in terms of manufacturing data. We will use these to create the films and export the Gerber files for the fabricator.

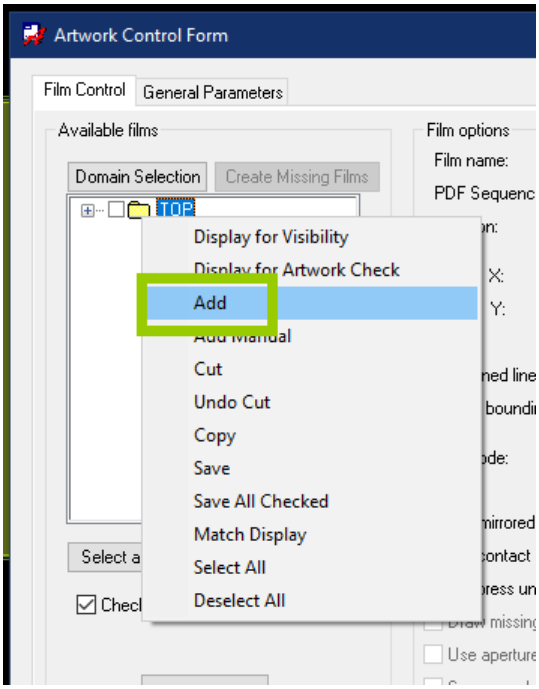
On the main toolbar, go to ***Export*** -> ***Gerber…*** and the *Artwork Control Form* window will appear.



With this window open, select the view for the layer you want to create the Gerber file for in the main window.

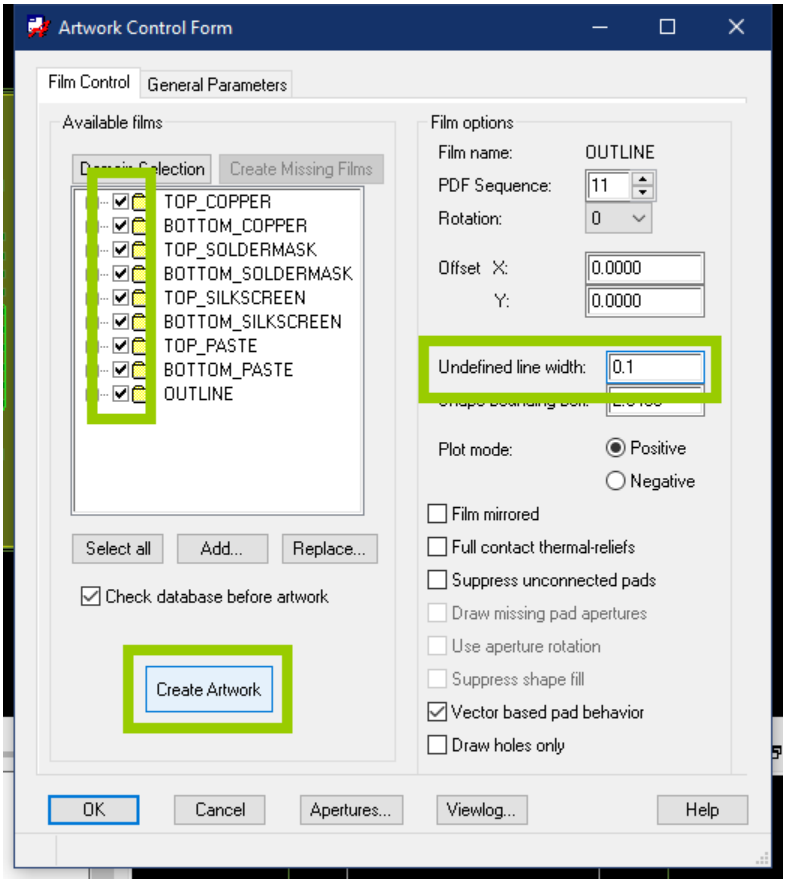


Then in the Artwork Control Form window, right-click a folder already present in the ***Film Control*** tab under ***Domain Selection*** and select ***Add.***



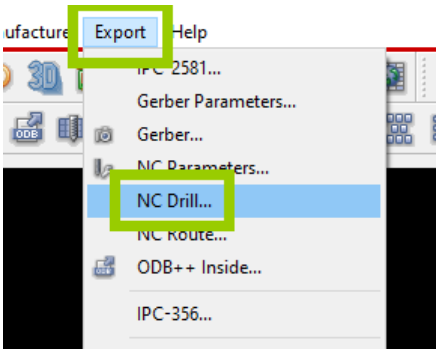
Enter a name for the Gerber file and select ok. Spaces are not allowed.

Change the ***Undefined Line Width*** to 0.1mm.

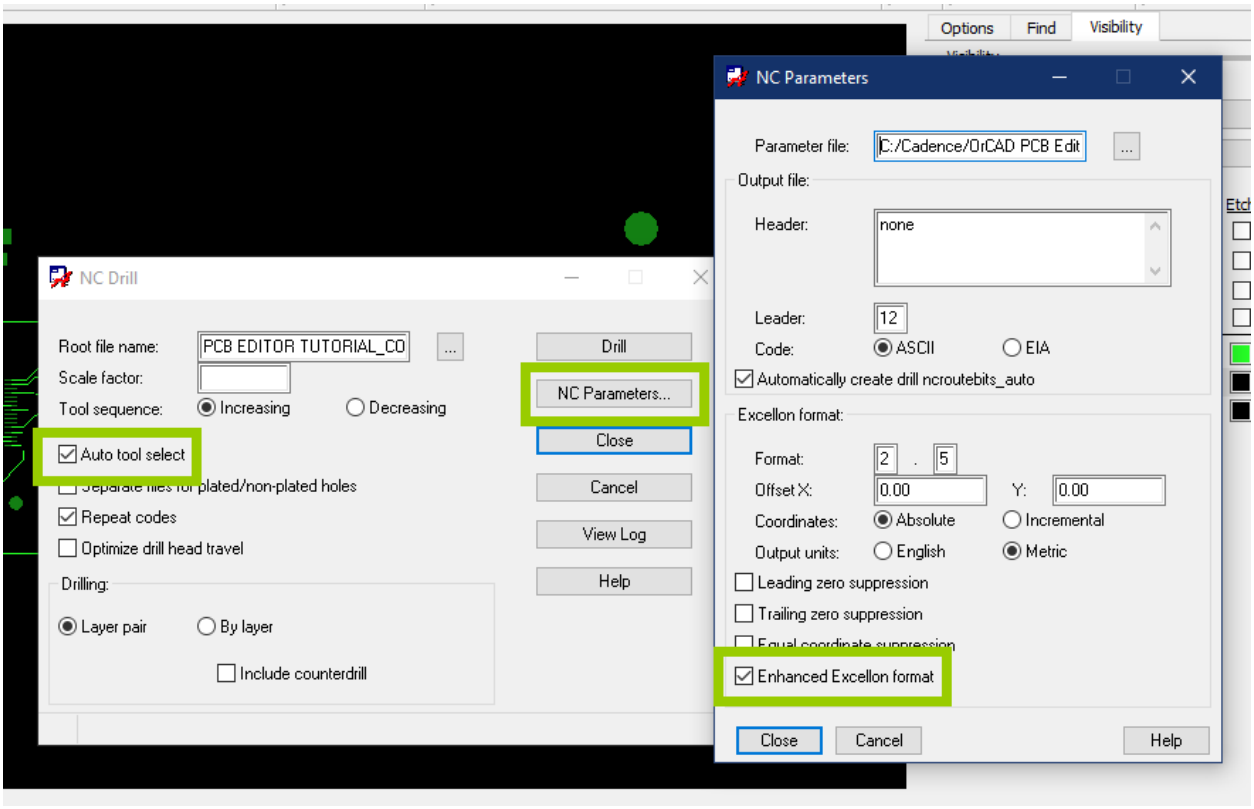


Repeat steps 2-5 for all the Gerber files and once done, select all the layers you just created and click the ***Create Artwork*** button. The software will generate your Gerber files in the same directory as your design file and in a folder called *artwork*, and display a log file. But we're not done yet. We still need to generate the NC Drill file in Excellon format to indicate where all the drill holes on the PCB need to be and of what size.

To do this go to ***Export*** -> ***NC Drill*** and a new window will appear.



By default, OrCad/Allegro does not export the drill file in Excellon format so we need to check the ***Auto tool select*** option and go to ***NC Parameters***. Check the ***Enhanced Excellon format*** option in the new window and close it.



Back in the *NC Drill* window, click ***Drill***and the drill file will be generated and placed in the same directory as the Gerber files.

All done! Package the Gerber and drill files together (without all the other stuff) into a .rar or .zip file and give them a final check in a separate Gerber viewer software. Once everything is verified, hand them over to your preferred manufacturer and wait for your PCBs to arrive.

Common Problems:

Missing solder mask and drill layers: Often we just receive just Top, Bottom and Outline files but at the bare minimum, we also need the solder mask and drill hole files. The absence of either of these files could be misinterpreted as meaning they are not needed, which could be disastrous. We have a hunch that this problem is encouraged by some documentation that splits the generation of these files into separate steps, which causes the other layers to easily be missed. Don’t fall for this trap.

No Board Outline: Happens a lot, not just with OrCad/Allegro. Make sure the outline is drawn in the Board Outline subclass and this is selected in the view.

No Drill File: Unlike the artwork files, the drill file is exported in the project directory and by default is named after the project file so it can easily be missed. Find the file with the .drl extension and make sure it is included in the package.

Incorrect file extensions: Not actually a problem since the extension is just a label to tell us which file is which. It has nothing to do with the format of the files but many manufacturers request that standard extensions are used. OrCad/Allegro does not have the option to add a unique extension for each file but so long as the names clearly indicate the respective layers then you should be fine. If you really want, you can just change the extensions directly by renaming the files.

Too many files: OrCad/Allegro exports all files in the same directory as the .brd file, including a lot of log files. Just trying to find all the manufacturing files can be a pain so please don't send all of this to the fabricator. No one wants to waste time going through each file trying to guess what information is important.

At Seeed Fusion, you just need to upload this package onto the website and fill in some parameters to get your PCBs manufactured. With the instant and live online quoting platform, there is no need to wait around for prices. Seeed has over ten years of experience in manufacturing and supply chain management in the heart of China, so your boards are in safe and professional hands. Get a competitive quote online now starting from just $4.90 for ten pieces. And if you need assembly as well, Seeed provides a complete turnkey service with full online BOM quoting, components procurement and in-house assembly for prototyping to mass production needs.

Try with our 5 pieces free assembly offer – just pay for components and the PCB. No assembly fees, operation fees or materials fees and shipping is free for all PCBA orders.

2 THOUGHTS ON “HOW TO GENERATE PCB GERBER FILES FROM CADENCE ALLEGRO/ORCAD – THE EASY WAY”

1.  **Edison517** says:

   December 13, 2019 at 2:36 am

   I have been using Allegro 17.2 daily for the last 2 years, and it still makes me want to rip my hair out at how complicated Cadence makes things. I started out with Eagle, went to Altium (still my favorite, by far), use Circuit Maker (Altium lite), and currently Cadence.

   You’re tutorial is right, but could be simplified a little, by just using the Artwork Control Form and just setting up the layers you want (unless you don’t know which layers you need, but that’s another story).

   In my limited experience, Cadence is NOT worth the money they charge for their software. It’s bloatware, it crashes, the program doesn’t operate like any/every other piece of Windows software, and things are hidden everywhere, or the same operation can be completed 5 diff ways, just cluttering things up.

   Just my $0.02.

   1.  **Carmen Zheng** says:

      December 13, 2019 at 8:25 pm

      Can’t help feel slightly sorry for you. We don’t have a lot of experience using it but I was surprised how difficult it was just to even install and find out how to open the PCB editor. Despite that, we often encounter beginners using Cadence to design their first PCB.

Order Details

Date: Mon, 17 Feb 2020 12:03:42 -0600

Status: Complete

Product

Price

Qty

Total

US PROTOTYPE PCBS 4-PACK

- Days expedited: 0
- Part Number: 2020-001
- Revision: -
- # of Layer: 2
- Board Length: 2
- Board Width: 2.75
- Special Instructions: Placing order per instructions from Greg. Also, per Greg, DFM submission was ok (i.e. no problems with board).

$25.00
4

$100.00

Subtotal:

$100.00

Shipping:FedEx Ground Home Delivery

$13.02

Order Total:

$113.02

View all my orders | Reorder | Order Invoice

Chrome sites visited while trying to select vendor:
Note – ordered from Pentalogix (Greg Delaney 800-238-1920 x504)
Also called Chicago Circuits (Dave 877-722-0317) … $150 for panel, 2-day turn
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