CSE 4560 Embedded Systems

Due: Oct. 5th, 2022

Microcontroller/Memory Address

1. Answer the following questions for MSP-432 processor with detailed calculations.
(a) How many different addresses are available for peripherals?
Range: 0x4000 0000 to 0x5FFF FFFF
Total number: 0x2000 0000 or 536,870,912 different addresses

(b) How many different addresses are available for ports?
Total number: 0x0400 or 1,024 different addresses

(c) Suppose an LED is connected to Port 2, Pin 5. Determine the memory address of Port 2.
Memory address: 0x4000_4C03

(d) How many Bytes can be written in the ROM region? How many 32 bit words can be written in the ROM region?
ROM region size: 32KB
32 bit word size: 4B
32 bit words in ROM: 8K words

Microcontroller/UART Peripheral

2. Suppose that a sender and a receiver exchange data via UART with following configuration:

Baud rate = 115200 bits/s
1 start bit, 2 stop bits, 8 data bits, 1 parity bit
16 clock periods used for sampling 1 bit

Answer the following questions:
(a) What is the required clock frequency?
Clk Frequency: 1.8432MHz

(b) Suppose a 48 MHz clock. What is a suitable division factor to generate the needed clock in sub-question (a)?
Suitable division factor: $\frac{48MHz}{1.8432MHz} = 26.0417$

(c) How long does it take to transfer 10 MBytes of data?
Time: 694.44 seconds or about 11 minutes

Interrupt and Polling

3. An external event is sensed using polling with period *P*. It takes 100 cycles to process the event. Processor frequency is 48 MHz. Before starting a new period, the previous polling task should have finished. The relative deadline for processing an event is 10*μs*.

(a) Determine the range of feasible polling periods?
Feasible polling periods: From 2.083*μs* to 7.917*μs*

(b) Suppose now that an unrelated interrupt may occur and the interrupt has higher priority than the code for processing the polling event. Including all overhead, it takes 40 cycles to process the interrupt. The minimum time between two subsequent interrupts is *T*. Suppose that *T* is larger than 140 cycles. Determine the range of feasible polling periods.
Feasible polling periods: From 2.917*μs* to 7.083*μs*