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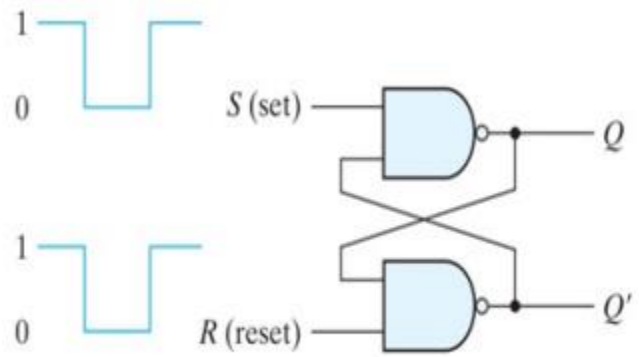
5/1/2022

Lab 9: Flip-flops and Counter

Objective: To implement a RS latch and a binary counter with D-type flip flops.

Provided: 74X374 (D flip-flops), 7400 (quad 2-input NAND), breadboard.

9.1 Experiment: RS Latch



(a) Logic diagram

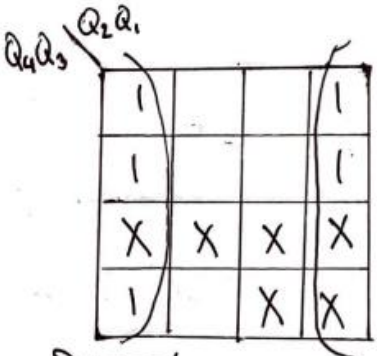
S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	(forbidden)

(b) Function table

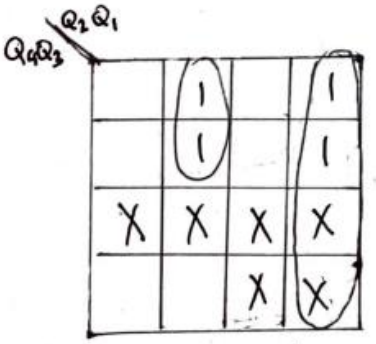
Input S=0 R=0 is undesirable or forbidden because the output Q=1 Qprime=1 is an invalid state.

9.2 Experiment: Binary Counter

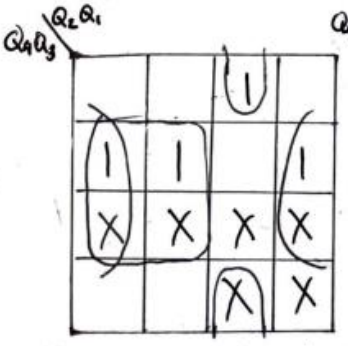
Present State				Next State				Unused
$Q_4(t)$	$Q_3(t)$	$Q_2(t)$	$Q_1(t)$	D_4 $Q_4(t+1)$	D_3 $Q_3(t+1)$	D_2 $Q_2(t+1)$	D_1 $Q_1(t+1)$	
0	0	0	0	0	0	0	1	1010
0	0	0	1	0	0	1	0	1011
0	0	1	0	0	0	1	1	1100
0	0	1	1	0	1	0	0	1101
0	1	0	0	0	1	0	1	1110
0	1	0	1	0	1	1	0	1111
0	1	1	0	0	1	1	1	Don't Cares
0	1	1	1	1	0	0	0	
1	0	0	0	1	0	0	1	
1	0	0	1	0	0	0	0	



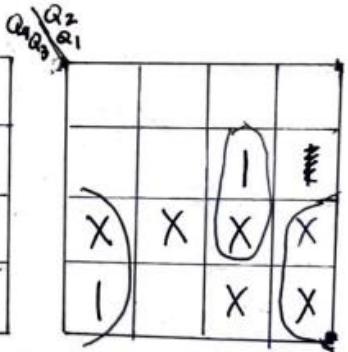
$D_1 = Q_1'$



$D_2 = Q_2 Q_1' + Q_4' Q_2' Q_1$



$D_3 = Q_3 Q_2' + Q_3 Q_1' + Q_3' Q_2 Q_1$



$D_4 = Q_4 Q_1' + Q_3 Q_2 Q_1$

Circuit Diagram: