Nitish Kumar

Lovely Professional University Punjab
+91 7032153437 nitishwork77@gmail.com https://github.com/ntsh1314/ntsh13141
https://www.linkedin.com/in/nitish-kumar-ponnakanti-0a1171307

Summary

- Motivated and enthusiastic engineer in both Electronics and software technologies, skilled in programming languages like C,C++,JAVA, Verilog HDL with hands on experience in tools like Cadence virtuoso, Xilinx Vivado and VS code. depth at problem-solving and debugging, with a passion for learning new technologies. Eager to contribute to team to drive successful project outcomes.

Education

Lovely Professional University **2021 – 2025**
Bachelor of Technology in ECE *CGPA 7.6/10*

Narayana jr college **2019 – 2021**
11th 12th *Percentage 93/100*

ZPPHS Dakkili **2018 – 2019**
10th *CGPA 9.7/10*

Industrial training

VLS | *Coincnet, Bangalore* **Feb'2022-Mar'2022**

- Designed all basic gates using Verilog HDL, and analysed output Graph on EDA playground
- Implemented the basic gates on Xilinx Vivado in Verilog HDL, Analysed output graph and design layout
- Implemented the gates on FPGA board with Xilinx Vivado, and analysed verified the outputs with respect to inputs

Projects

SRAM 6T,7T,9T | *VLSI, Cadence Virtuoso* **November 2023**

∗ Designed SRAM 6T 7T 9T on cadence Virtuoso in RedHat Linux .
∗ Compared the 6t,7t and 9t SRAM in terms delay,power consumption, power dissipation, Area.
∗ Compared the SRAM with DRAM and its advantages and benfits of SRAM over DRAM
∗ Analysed Power and Area in Cadence Virtuoso and Submitted the report

Vending Machine | *Verilog HDL, Xilinx Vivado* **March 2024**

∗ Developed a Vending Machine using Verilog HDL, Implemented using FPGA.
∗ Used Mealy and Moore concepts for and implementation .
∗ A three product Vending machine including with the feature of returning the balance amount was designed
∗ Analysed output graph with various test cases and outputs in FPGA with various inputs and submitted the report

Car parking System | *Verilog HDL, Cadence NCSIM* **Marc 2023**

∗ Developed a Car parking system using Verilog HDL, on candence NCSIM.
∗ Used Mealy and Moore concepts for and implementation and representation.
∗ Developed the feature of displaying the vacancy in Parking slot
∗ Closing and opening gates at entrance and exit depending upon the vacancies

Fire Detecting Alarm | *Analog Electronics Designing* **November 2022**

∗ Designed the Fire Detecting Alarm Using BC547 NPN transistor.
∗ This project can detect the Fire, and Alarm and red light will get turned on when ever the fire is detected
∗ Here transistors are used as switch, in which when fire is detected the positive pulse will fed to transistor base and transistor get by which the alarm can glow

Inventory Management System t | *Java, GUI, Swing* **November 2023**

∗ Developed an Inventory management system using Java and interface using swing in which application will help to get the list of the stocks present in the inventory.
∗ Login page where user can select the Username and password by his own choice, and login using the same which will create different data base to the, different users
∗ Created the Application in which every user can see the amount of stock lefts and how much sold and they can make the changes which can be reflect back in database.
∗ For the database we are used the JAVA File handling .

Medical Store Management System | *C++* **November 2022**

∗ Designed a sample Medical store billing system using CPP to get the total bill for the user for the purchased medicines.
∗ Used Sample data based on our assumption which was included by the developers only.
∗ Implemented object-oriented programming practices and Processed user input and generate the bill and amount that should need to pay.
∗ Created two login pages for the costumer and for the Store manager where both can login by creating there account and individual database will be allocated .

Technical Skills

Languages: Verilog HDL, Java, C, CPP, HTML/CSS, SQL.
EDA Tools: Cadence Virtuoso, Xilinx Vivado.
Developer Tools: VS Code, Eclipse, Oracle.
Technologies/Frameworks: Linux, VLSI, Microsoft 365.

Relevant Coursework

- Digital Electronics
- Analog Electronics
- Re-configurable architecture for VLSI
- System Designing using Verilog
- Database Management
- Artificial Intelligence
- Data Structures

Achievements

∗ Achieved Five star rating on hackerrank C++ Programming.
∗ Achieved Five star rating on hackerrank DSA Problem solving.
∗ Achieved 90 percentile in JEE mains 2021.

Certifications

∗ Awarded with a certification by MindLuster for completing VERILOG course Dec'2023.
∗ Awarded with a certification by MindLuster for completing JAVA 11 course Dec'2023.
∗ Awarded with a certification by Coincnet for completing VLSI course.

Extracurricular Activities

· Represented Rawanda country in One-world event in LPU on march'2023
· Demonstrated the presentation about IOT in speaking event in LPU on September 2021
· Participated in NGO Campaign on plating tress and donating poor on May 2022
· Participated in chess State level armature on September 2018