Nitish Kumar

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Summary

Motivated and enthusiastic engineer in both Electronics and software technologies, skilled in programming languages like C,C++,JAVA, Verilog HDL with hands on experience in tools like Cadence virtuoso, Xilinx Vivado and VS code. depth at problem-solving and debugging, with a passion for learning new technologies. Eager to contribute to team to drive successful project outcomes.

Education

11th 12th

Lovely Professional University 2021 - 2025Bachelor of Technology in ECE CGPA 7.6/10

Narayana jr college 2019 - 2021

ZPPHS Dakkili 2018 - 2019

10thCGPA 9.7/10

Industrial training

VLSI | Coincret, Bangalore

Feb'2022-Apr'2022

Percentage 93/100

- Designed all basic gates using Verilog HDL, and analysed output Graph on EDA playground with synopsis VCS tool
- Implemented all logic gates on Xilinx Vivado in Verilog HDL, Analysed output graph and logic designs
- Synthesised all logic gates on FPGA board on Xilinx Vivado, and verified the outputs with respect to random inputs

Projects

SRAM 6T,7T,9T | VLSI, Cadence Virtuoso

November 2023

- * Designed SRAM 6T 7T 9T on cadence Virtuoso in RedHat Linux .
- * Compared the 6t,7t and 9t SRAM in terms delay, power consumption, power dissipation, Area.
- * Compared the SRAM with DRAM and its advantages and benefits of SRAM over DRAM
- * Used 90mm technology to design SRAM and used pmos1v and nmos1v.
- * Analysed Power and Area in Cadence Virtuoso

Vending Machine | Verilog HDL, Xilinx Vivado

March 2024

- * Developed a Vending Machine using Verilog HDL, Implemented on FPGA.
- * Used Mealy and Moore concepts for implementation and to represent the flow diagram.
- * A three product Vending machine including with the feature of returning the balance amount was designed
- * Analysed output graph with various test cases and outputs in FPGA with various inputs and submitted the report
- * If the amount inserted was less than the price then it will display for the remaining amount inserted to dispense the selected item

Car parking System | Verilog HDL, Cadence NCSIM

Marc 2023

- * Developed a Car parking system using Verilog HDL, on cadence NCSIM.
- * Used Mealy and Moore concepts for and implementation and representation.
- * Developed the feature of displaying the vacancy in Parking slot
- * The sensor will activate to detect the car, if car was detected and vacancies are left then it let the vehicle in.
- * while its leaving at exit gate, if the car was detected again by the sensor then it let the vehicle out.

Fire Detecting Alarm | Analog Electronics Designing

November 2022

- * Designed the Fire Detecting Alarm Using BC547 NPN transistor.
- * This project can detect the Fire, and sound the Alarm and blink the red light when the fire is detected
- * Here transistors are used as switch, when fire is detected the positive pulse will fed to transistor base and transistor gets active by which the alarm can ring

- * Developed an Inventory management system using Java and interface using swing in which application will help to get the list of the stocks present in the inventory.
- * Login page where user can select the Username and password by his own choice, and login using the same which will create different data base to the, different users
- * Created the Application in which every user can see the amount of stock lefts and how much sold and they can make the changes which can be reflect back in database.
- * For the database we are used the JAVA File handling .

Medical Store Management System $\mid C++$

November 2022

- * Designed a sample Medical store billing system using CPP to get the total bill for the user for the purchased medicines.
- * Used Sample data based on our assumption which was included by the user or client.
- * Implemented object-oriented programming practices and Processed user input and generate the bill amount that need to pay.
- * Created two login pages for the costumer and for the Store manager where both can login by creating there account and individual database will be allocated .

Technical Skills

Languages: Verilog HDL, Java, C, CPP, HTML/CSS, SQL.

EDA Tools: Cadence Virtuoso, Xilinx Vivado. **Developer Tools**: VS Code, Eclipse, Oracle.

Technologies/Frameworks: Linux, VLSI, Microsoft 365.

Relevant Coursework

- Digital Electronics
- Analog Electronics
- Re-configurable architecture for VLSI
- System Designing using Verilog

- Database Management
- Artificial Intelligence
- Data Structures

Achievements

- * Achieved Five star rating on hackerrank for C++ Programming.
- * Achieved Five star rating on hackerrank for DSA Problem solving.
- * Achieved Five star rating on hackerrank for SQL .
- * Achieved 90 percentile in JEE mains 2021.

Certifications

- * Awarded with a certificate by MindLuster for completing VERILOG course Dec'2023.
- * Awarded with a certificate by MindLuster for completing JAVA 11 course Dec'2023.
- * Awarded with a certification by Coincnet for completing VLSI course.

Extracurricular Activities

- · Represented Rawanda country at One-world event in LPU on march'2023
- · Demonstrated the presentation about IOT in speaking event at LPU on September 2021
- · Participated in NGO Campaign on plating tress and donating poor on May 2022
- · Participated in chess State level armature on September 2018