This set of Digital Electronic Circuits Interview Questions and Answers focuses on “1’s,2’s,9’s & 10’s Complements-2”.

1. If the number of bits in the sum exceeds the number of bits in each added numbers, it results in _____
a) Successor
b) Overflow
c) Underflow
d) Predecessor

Answer: b
Explanation: If the number of bits in the sum exceeds the number of bits in each added numbers, it results in overflow and is also known as excess-one. In case of any arithmetic operation, if the result has less number of bits than the operands, then it is known as underflow condition.

2. An overflow is a _____
a) Hardware problem
b) Software problem
c) User input problem
d) Input Output Error

Answer: b
Explanation: An overflow is a software problem which occurs when the processor cannot handle the result properly when it produces an out of the range output.

3. An overflow occurs in _____
a) MSD position
b) LSD position
c) Middle position
d) Signed Bit

Answer: a
Explanation: An overflow occurs at the Most Significant Digit position. It occurs when the processor cannot handle the result properly when it produces an out of the range output.

4. Logic circuitry is used to detect _____
a) Underflow
b) MSD
c) Overflow
d) LSD

Answer: c
Explanation: To check the overflow logic circuitry is used in each case. Overflow occurs when the processor cannot handle the result properly when it produces an out of the range output.

5. 1’s complement can be easily obtained by using _____
a) Comparator
b) Inverter
c) Adder
d) Subtractor

Answer: b
Explanation: With the help of inverter the 1’s complement is easily obtained. Since, during the operation of 1’s complement 1 is converted into 0 and vice-versa and this is well suited for the inverter.

6. The advantage of 2’s complement system is that _____
a) Only one arithmetic operation is required
b) Two arithmetic operations are required
c) No arithmetic operations are required
d) Different Arithmetic operations are required

Answer: a
Explanation: The advantage of 2’s complement is that only one arithmetic operation is required

for 2’s complement’s operation and that is only addition. Just by adding a 1 bit to 1’s complement, we get 2’s complement.

7. The 1’s complements requires _____
a) One operation
b) Two operations
c) Three operations
d) Combined Operations

Answer: a
Explanation: Only one operation is required for 1’s complement operation. This includes only inversion of 1’s to 0’s and 0’s to 1’s.

8. Which one is used for logical manipulations?
a) 2’s complement
b) 9’s complement
c) 1’s complement
d) 10’s complement

Answer: c
Explanation: For logical manipulations, 1’s complement is used, as all logical operations take place with binary numbers.

9. For arithmetic operations only _____
a) 1’s complement is used
b) 2’s complement
c) 10’s complement
d) 9’s complement

Answer: b
Explanation: Only 2’s complement is used for arithmetic operations, as it is more fast.

10. The addition of +19 and +43 results as _____ in 2’s complement system.
a) 11001010
b) 101011010
c) 00101010
d) 0111110

Answer: d
Explanation: The decimal numbers are converted to their respective binary equivalent and then the binary addition rules are applied.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Number System – 1”.

1. Any signed negative binary number is recognised by its _____
a) MSB
b) LSB
c) Byte
d) Nibble

Answer: a
Explanation: Any negative number is recognized by its MSB (Most Significant Bit).
If it’s 1, then ít’s negative, else if it’s 0, then positive.

2. The parameter through which 16 distinct values can be represented is known as _____
a) Bit
b) Byte
c) Word
d) Nibble

Answer: c
Explanation: It can be represented up to 16 different values with the help of a Word. Nibble is a combination of four bits and Byte is a combination of 8 bits. It is “word” that is said to be a collection of 16-bits on most of the systems.

3. If the decimal number is a fraction then its binary equivalent is obtained by _____ the number continuously by 2.
a) Dividing
b) Multiplying
c) Adding
d) Subtracting

Answer: b
Explanation: On multiplying the decimal number continuously by 2, the binary equivalent is obtained by the collection of the integer part. However, if it's an integer, then it's binary equivalent is determined by dividing the number by 2 and collecting the remainders.

4. The representation of octal number (532.2)8 in decimal is _____
a) (346.25)10
b) (532.864)10
c) (340.67)10
d) (531.668)10

Answer: a
Explanation: Octal to Decimal conversion is obtained by multiplying 8 to the power of base index along with the value at that index position.
$(532.2)8 = 5 * 8^{2} + 3 * 8^{1} + 2 * 8^{0} + 2 * 8^{-1} = (346.25)10$

5. The decimal equivalent of the binary number (1011.011)2 is _____
a) (11.375)10
b) (10.123)10
c) (11.175)10
d) (9.23)10

Answer: a
Explanation: Binary to Decimal conversion is obtained by multiplying 2 to the power of base index along with the value at that index position.
$1 * 2^{3} + 0 * 2^{2} + 1 * 2^{1} + 1*2^{0} + 0 * 2^{-1} + 1 * 2^{-2} + 1 * 2^{-3} = (11.375)10$
Hence, $(1011.011)2 = (11.375)10$

6. An important drawback of binary system is _____
a) It requires very large string of 1's and 0's to represent a decimal number
b) It requires sparingly small string of 1's and 0's to represent a decimal number
c) It requires large string of 1's and small string of 0's to represent a decimal number
d) It requires small string of 1's and large string of 0's to represent a decimal number

Answer: a
Explanation: The most vital drawback of binary system is that it requires very large string of 1's and 0's to represent a decimal number. Hence, Hexadecimal systems are used by processors for calculation purposes as it compresses the long binary strings into small parts.

7. The decimal equivalent of the octal number $(645)_{8}$ is _____
a) $(450)_{10}$
b) $(451)_{10}$
c) $(421)_{10}$
d) $(501)_{10}$

Answer: c
Explanation: Octal to Decimal conversion is obtained by multiplying 8 to the power of base index along with the value at that index position.
The decimal equivalent of the octal number $(645)_{8}$ is $6 * 8^{2} + 4 * 8^{1} + 5 * 8^{0} = 6 * 64 + 4 * 8 + 5 = 384 + 32 + 5 = (421)_{10}$.

8. The largest two digit hexadecimal number is _____
a) (FE)16
b) (FD)16
c) (FF)16

d) (EF)16

Answer: c
Explanation: (FE)16 is 254 in decimal system, while (FD)16 is 253. (EF)16 is 239 in decimal system. And, (FF)16 is 255. Thus, The largest two-digit hexadecimal number is (FF)16.

9. Representation of hexadecimal number (6DE)H in decimal:
a) $6 * 16^2 + 13 * 16^1 + 14 * 16^0$
b) $6 * 16^2 + 12 * 16^1 + 13 * 16^0$
c) $6 * 16^2 + 11 * 16^1 + 14 * 16^0$
d) $6 * 16^2 + 14 * 16^1 + 15 * 16^0$

Answer: a
Explanation: Hexadecimal to Decimal conversion is obtained by multiplying 16 to the power of base index along with the value at that index position.
In hexadecimal number D & E represents 13 & 14 respectively.
So, 6DE = $6 * 16^2 + 13 * 16^1 + 14 * 16^0$.

10. The quantity of double word is _____
a) 16 bits
b) 32 bits
c) 4 bits
d) 8 bits

Answer: b
Explanation: One word means 16 bits, Thus, the quantity of double word is 32 bits.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “1’s, 2’s, 9’s & 10’s Complements – 1”.

1. 1’s complement of 1011101 is _____
a) 0101110
b) 1001101
c) 0100010
d) 1100101

Answer: c
Explanation: 1’s complement of a binary number is obtained by reversing the binary bits. All the 1’s to 0’s and 0’s to 1’s.

Thus, 1’s complement of 1011101 = 0100010.

2. 2’s complement of 11001011 is _____
a) 01010111
b) 11010100
c) 00110101
d) 11100010

Answer: c
Explanation: 2’s complement of a binary number is obtained by finding the 1’s complement of the number and then adding 1 to it.
2’s complement of 11001011 = 00110100 + 1 = 00110101.

3. On subtracting (01010)2 from (11110)2 using 1’s complement, we get _____
a) 01001
b) 11010
c) 10101
d) 10100

Answer: d
Explanation: Steps For Subtraction using 1’s complement are:
-> 1’s complement of the subtrahend is determined and added to the minuend.
-> If the result has a carry, then it is dropped and 1 is added to the last bit of the result.

-> Else, if there is no carry, then 1’s complement of the result is found out and a ‘-’ sign preceeds the result.

```
                                        1 1 1
                     Minuend -          1 1 1 1 0
 1’s complement of subtrahend -         1 0 1 0 1
                                       ___________
                  Carry over -     1    1 0 0 1 1
                                            1
                                       ___________
                                        1 0 1 0 0
```

4. On subtracting (010110)2 from (1011001)2 using 2’s complement, we get _____
a) 0111001
b) 1100101
c) 0110110
d) 1000011

Answer: d
Explanation: Steps For Subtraction using 2’s complement are:
-> 2’s complement of the subtrahend is determined and added to the minuend.
-> If the result has a carry, then it is dropped and the result is positive.
-> Else, if there is no carry, then 2’s complement of the result is found out and a ‘-’ sign preceeds the result.

```
      1’s complement of subtrahend -        1 1 0 1 0 0 1
                                           _______________
                                            1 1 1
                         Minuend -          1 0 1 1 0 0 1
      2’s complement of subtrahend -        1 1 0 1 0 1 0
                                           _______________

                        Carry over -    1   1 0 0 0 0 1 1
```

```
Answer: 1000011
```

5. On subtracting (001100)2 from (101001)2 using 2’s complement, we get _____
a) 1101100
b) 011101
c) 11010101
d) 11010111

Answer: b
Explanation: Steps For Subtraction using 2’s complement are:
-> 2’s complement of the subtrahend is determined and added to the minuend.
-> If the result has a carry, then it is dropped and the result is positive.
-> Else, if there is no carry, then 2’s complement of the result is found out and a ‘-’ sign preceeds the result.

```
      1’s complement of subtrahend -        1 1 0 0 1 1
                                           _______________
                         Minuend -          1 0 1 0 0 1
      2’s complement of subtrahend -        1 1 0 1 0 0
                                           _______________
                        Carry over -    1   0 1 1 1 0 1
```

```
Answer: 011101
```

6. On addition of 28 and 18 using 2’s complement, we get _____
a) 00101110
b) 0101110
c) 00101111
d) 1001111

Answer: b
Explanation: Steps for Binary Addition Using 2’s complement:
-> The binary equivalent of the two numbers are obtained and added using the rules of binary addition.

```
Augend -        0   0 1 1 1 0 0

Addend -        0   0 1 0 0 1 0
               ________________
                0   1 0 1 1 1 0
```

```
Answer: 0  1 0 1 1 1 0
```

7. On addition of +38 and -20 using 2’s complement, we get _____
a) 11110001
b) 100001110
c) 010010
d) 110101011

Answer: c
Explanation: Steps for Binary Addition Using 2’s complement:
-> The 2’s complement of the addend is found out and added to the first number.
-> The result is the 2’s complement of the sum obtained.

```
                     Augend -          0 1 0 0 1 1 0
2’s Complement of Subtrahend:          1 1 0 1 1 0 0
                                     _________________
                               1       0 0 1 0 0 1 0
```

```
Answer: 0 1 0 0 1 0
```

8. On addition of -46 and +28 using 2’s complement, we get _____
a) -10010
b) -00101
c) 01011
d) 0100101

Answer: a
Explanation: The BCD form is written of the two given numbers, in their signed form. After which, normal binary addition is performed.
Augend is 28 and Subtrahend is -46.

```
                           Augend -          0 0 1 1 1 0 0   .....(a)
      2’s Complement of Subtrahend:          1 0 1 0 0 1 0   .....(b)
                                           _________________
               Addiing (a) and (b):          1 1 0 1 1 1 0
Since, there is no carry, so answer will be negative
and 2's complement of the above result is determined.
                                             0 0 1 0 0 0 1
                                       +               1
                                         _________________
                                           0 0 1 0 0 1 0
```

```
Answer: - 1 0 0 1 0
```

9. On addition of -33 and -40 using 2’s complement, we get _____
a) 1001110
b) -110101
c) 0110001
d) -1001001

Answer: d
Explanation: The BCD form is written of the two given numbers, in their signed form. After

which, normal binary addition is performed.
Augend is -40 and Subtrahend is -33.

```
                          Augend -          1    0 1 0 0 0 0 1   .....(a)
      2's Complement of Subtrahend:         1    1 0 1 1 0 0 1   .....(b)

                                           ____________________
               Addiing (a) and (b):        1 0   1 0 0 1 0 0 0
Since, there is no carry, so answer will be negative
and 2's complement of the above result is determined.
                                              1 0 0 1 0 0 0
                                         +              1
                                           ________________
                                              1 0 0 1 0 0 1
 Answer: -1001001
```

10. On subtracting +28 from +29 using 2's complement, we get _____
a) 11111010
b) 111111001
c) 100001
d) 1

Answer: d
Explanation: Steps For Subtraction using 2's complement are:
-> 2's complement of the subtrahend is determined and added to the minuend.
-> If the result has a carry, then it is dropped and the result is positive.
-> Else, if there is no carry, then 2's complement of the result is found out and a '-' sign preceeds the result.

```
         1's complement of subtrahend -        1 0 0 0 1 1
                             Minuend -        0 1 1 1 0 1
         2's complement of subtrahend -        1 0 0 1 0 0
                                              ____________________

                           Carry over -    1   0 0 0 0 0 1

Answer: 000001 = 1
```

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on "Number System – 2".

1. The given hexadecimal number (1E.53)16 is equivalent to _____
a) (35.684)8
b) (36.246)8
c) (34.340)8
d) (35.599)8

Answer: b
Explanation: First, the hexadecimal number is converted to it's equivalent binary form, by writing the binary equivalent of each digit in form of 4 bits. Then, the binary equivalent bits are grouped in terms of 3 bits and then for each of the 3-bits, the respective digit is written. Thus, the octal equivalent is obtained.
(1E.53)16 = (0001 1110.0101 0011)2
= (00011110.01010011)2
= (011110.010100110)2
= (011 110.010 100 110)2
= (36.246)8.

2. The octal number (651.124)8 is equivalent to _____
a) (1A9.2A)16
b) (1B0.10)16
c) (1A8.A3)16
d) (1B0.B0)16

Answer: a
Explanation: First, the octal number is converted to it's equivalent binary form, by writing the

binary equivalent of each digit in form of 3 bits. Then, the binary equivalent bits are grouped in terms of 4 bits and then for each of the 4-bits, the respective digit is written. Thus, the hexadecimal equivalent is obtained.
(651.124)8 = (110 101 001.001 010 100)2
= (110101001.001010100)2
= (0001 1010 1001.0010 1010)2
= (1A9.2A)16.

3. The octal equivalent of the decimal number (417)10 is _____
a) (641)8
b) (619)8
c) (640)8
d) (598)8

Answer: a
Explanation: Octal equivalent of decimal number is obtained by dividing the number by 8 and collecting the remainders in reverse order.
8 | 417
8 | 52 — 1
8 | 6 – 4
So, (417)10 = (641)8.

4. Convert the hexadecimal number (1E2)16 to decimal.
a) 480
b) 483
c) 482
d) 484

Answer: c
Explanation: Hexadecimal to Decimal conversion is obtained by multiplying 16 to the power of base index along with the value at that index position.
(1E2)16 = $1 * 16^{2} + 14 * 16^{1} + 2 * 16^{0}$ (Since, E = 14)
= 256 + 224 + 2 = (482)10.

5. (170)10 is equivalent to _____
a) (FD)16
b) (DF)16
c) (AA)16
d) (AF)16

Answer: c
Explanation: Hexadecimal equivalent of decimal number is obtained by dividing the number by 16 and collecting the remainders in reverse order.
16 | 170
16 | 10 – 10
Hence, (170)10 = (AA)16.

6. Convert (214)8 into decimal.
a) (140)10
b) (141)10
c) (142)10
d) (130)10

Answer: a
Explanation: Octal to Decimal conversion is obtained by multiplying 8 to the power of base index along with the value at that index position.
(214)8 = $2 * 8v + 1 * 8^{1} + 4 * 8^{0}$
= 128 + 8 + 4 = (140)10.

7. Convert (0.345)10 into an octal number.
a) (0.16050)8
b) (0.26050)8
c) (0.19450)8
d) (0.24040)8

Answer: b
Explanation: Converting decimal fraction into octal number is achieved by multiplying the fraction part by 8 everytime and collecting the integer part of the result, unless the result is 1.
0.345*8 = 2.76 2
0.760*8 = 6.08 6
00.08*8 = 0.64 0
0.640*8 = 5.12 5
0.120*8 = 0.96 0
So, (0.345)10 = (0.26050)8.

8. Convert the binary number (01011.1011)2 into decimal.
a) (11.6875)10
b) (11.5874)10
c) (10.9876)10
d) (10.7893)10

Answer: a
Explanation: Binary to Decimal conversion is obtained by multiplying 2 to the power of base index along with the value at that index position.
$(01011)2 = 0 * 2^4 + 1 * 2^3 + 0 * 2^2 + 1 * 2^1 + 1 * 2^0 = 11$
$(1011)2 = 1 * 2^{-1} + 0 * 2^{-2} + 1 * 2^{-3} + 1 * 2^{-4} = 0.6875$
So, (01011.1011)2 = (11.6875)10.

9. Octal to binary conversion: (24)8 =?
a) (111101)2
b) (010100)2
c) (111100)2
d) (101010)2

Answer: b
Explanation: Each digit of the octal number is expressed in terms of group of 3 bits. Thus, the binary equivalent of the octal number is obtained.
(24)8 = (010100)2.

10. Convert binary to octal: (110110001010)2 =?
a) (5512)8
b) (6612)8
c) (4532)8
d) (6745)8

Answer: b
Explanation: The binary equivalent is segregated into groups of 3 bits, starting from left. And then for each group, the respective digit is written. Thus, the octal equivalent is obtained.
(110110001010)2 = (6612)8.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Arithmetic Operation”

1. What is the addition of the binary numbers 11011011010 and 010100101?
a) 0111001000
b) 1100110110
c) 11101111111
d) 10011010011

Answer: c
Explanation: The rules for Binary Addition are :
0 + 0 = 0
0 + 1 = 1
1 + 0 = 1
1 + 1 = 0 (Carry 1)

```
        1

   1 1 0 1 1 0 1 1 0 1 0
```

```
 + 0 0 0 1 0 1 0 0 1 0 1
  _____________________
   1 1 1 0 1 1 1 1 1 1 1
  _____________________
```

2. Perform binary addition: 101101 + 011011 = ?
a) 011010
b) 1010100
c) 101110
d) 1001000

Answer: d
Explanation:The rules for Binary Addition are :
0 + 0 = 0
0 + 1 = 1
1 + 0 = 1
1 + 1 = 0 (Carry 1)

```
 1 1 1 1 1 1
   1 0 1 1 0 1
 + 0 1 1 0 1 1
 _______________
 1 0 0 1 0 0 0
 _______________
```

Therefore, the addition of 101101 + 011011 = 1001000.

3. Perform binary subtraction: 101111 – 010101 = ?
a) 100100
b) 010101
c) 011010
d) 011001

Answer: c
Explanation: The rules for Binary Subtraction are :
0 – 0 = 0
0 – 1 = 1 (Borrow 1)
1 – 0 = 1
1 – 1 = 0

```
   1 0 1 1 1 1
 - 0 1 0 1 0 1
  ____________
   0 1 1 0 1 0
  ____________
```

Therefore, The subtraction of 101111 – 010101 = 011010.

4. Binary subtraction of 100101 – 011110 is?
a) 000111
b) 111000
c) 010101
d) 101010

Answer: a
Explanation: The rules for Binary Subtraction are :
0 – 0 = 0
0 – 1 = 1 (Borrow 1)
1 – 0 = 1
1 – 1 = 0

```
  1 0 0 1 0 1
- 0 1 1 1 1 0
  ___________
  0 0 0 1 1 1
  ___________
```

Therefore, The subtraction of 100101 – 011110 = 000111.

5. Perform multiplication of the binary numbers: 01001 × 01011 = ?
a) 001100011
b) 110011100
c) 010100110
d) 101010111

Answer: a
Explanation: The rules for binary multiplication are:
0 * 0 = 0
0 * 1 = 0
1 * 0 = 0
1 * 1 = 1

```
              0 1 0 0 1
            x 0 1 0 1 1
            ___________
              0 1 0 0 1
            0 1 0 0 1 0
          0 0 0 0 0 0 0
        0 1 0 0 1 0 0 0
      0 0 0 0 0 0 0 0 0
    ___________________
      0 0 1 1 0 0 0 1 1
    ___________________
```

Therefore, 01001 × 01011 = 001100011.

6. 100101 × 0110 = ?
a) 1011001111
b) 0100110011
c) 101111110
d) 0110100101

Answer: c
Explanation: The rules for binary multiplication are:
0 * 0 = 0
0 * 1 = 0
1 * 0 = 0
1 * 1 = 1

```
                    1 0 0 1 0 1
                x       0 1 1 0
                  _____________
                    0 0 0 0 0 0
                  1 0 0 1 0 1 0
                1 0 0 1 0 1 0 0
              0 0 0 0 0 0 0 0 0
            _____________________
              0 1 1 0 1 1 1 1 0
            _____________________
```

Therefore, 100101 x 0110 = 011011110.

7. On multiplication of (10.10) and (01.01), we get _____
a) 101.0010
b) 0010.101
c) 011.0010

d) 110.0011

Answer: c
Explanation: The rules for binary multiplication are:
0 * 0 = 0
0 * 1 = 0
1 * 0 = 0
1 * 1 = 1

```
          1 0.1 0
      x   0 1.0 1
        ___________
          1 0 1 0
        0 0 0 0 0
      1 0 1 0 0 0
    0 0 0 0 0 0 0
  ________________
  0 1 1.0 0 1 0
  ____________________
```

Therefore, 10.10 x 01.01 = 011.0010.

8. Divide the binary numbers: 111101 ÷ 1001 and find the remainder.
a) 0010
b) 1010
c) 1100
d) 0111

Answer: d
Explanation: Binary Division is accomplished using long division method.

```
1 0 0 1 ) 1 1 1 1 0 1 ( 1 1
          1 0 0 1
          ___________
          0 1 1 0 0
            1 0 0 1
          ___________
            0 1 1 1
```

Therefore, the remainder of 111101 ÷ 1001 = 0111.

9. Divide the binary number (011010000) by (0101) and find the quotient.
a) 100011
b) 101001
c) 110010
d) 010001

Answer: b
Explanation:

```
0 1 0 1 ) 0 1 1 0 1 0 0 0 0 ( 0 1 0 1 1 1
          0 0 0 0
          ____________________
          0 1 1 0 1
          0 0 1 0 1
          _______________
          0 1 0 0 0 0
          0 0 0 0 0 0
          ____________________
              1 0 0 0 0
              0 0 1 0 1
           ________________
                0 1 0 1 1 0
                0 0 0 1 0 1
             ____________________
```

```
          1 0 0 0 1 0
          0 0 0 1 0 1
_____________________________
            1 1 1 0 1 0
            0 0 0 1 0 1
_____________________________
              1 0 1 0 1
              0 0 1 0 1
_____________________________
              1 0 0 0 0
```

Therefore, the quotient of 011010000 ÷ 1001 = 101001.

10. Binary subtraction of 101101 – 001011 = ?
a) 100010
b) 010110
c) 110101
d) 101100

Answer: a
Explanation: The rules for binary subtraction are:
0 – 0 = 0
0 – 1 = 1 (Borrow 1)
1 – 0 = 1
1 – 1 = 0

```
  1 0 1 1 0 1
- 0 0 1 0 1 1
  ____________
  1 0 0 0 1 0
  ____________
```

Therefore, the subtraction of 101101 – 001011 = 100010.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Binary Coded Decimal(BCD)”.

1. Binary coded decimal is a combination of _____
a) Two binary digits
b) Three binary digits
c) Four binary digits
d) Five binary digits

Answer: c
Explanation: Binary coded decimal is a combination of 4 binary digits. For example-8421.

2. The decimal number 10 is represented in its BCD form as _____
a) 10100000
b) 01010111
c) 00010000
d) 00101011

Answer: c
Explanation: The decimal number 10 is represented in its BCD form as 0001 0000, in accordance to 8421 for each of the two digits.

3. Add the two BCD numbers: 1001 + 0100 = ?
a) 10101111
b) 01010000
c) 00010011
d) 00101011

Answer: c
Explanation: Firstly, Add the 1001 and 0100. We get 1101 as output but it’s not in BCD form. So, we add 0110 (i.e. 6) with 1101. As a result we get 10011 and it’s BCD form is 0001 0011.

4. Carry out BCD subtraction for (68) – (61) using 10’s complement method.
a) 00000111
b) 01110000
c) 100000111
d) 011111000

Answer: a
Explanation: First the two numbers are converted into their respective BCD form using 8421 sequence. Then binary subtraction is carried out.

5. Code is a symbolic representation of _____ information.
a) Continuous
b) Discrete
c) Analog
d) Both continuous and discrete

Answer: b
Explanation: Code is a symbolic representation of discrete information, which may be present in the form of numbers, letters or physical quantities. Mostly, it is represented using a particular number system like decimal or binary and such like.

6. When numbers, letters or words are represented by a special group of symbols, this process is called _____
a) Decoding
b) Encoding
c) Digitizing
d) Inverting

Answer: b
Explanation: When numbers, letters or words are represented by a special group of symbols, this process is called encoding. Encoding in the sense of fetching the codes or words in a computer. It is done to secure the transmission of information.

7. A three digit decimal number requires _____ for representation in the conventional BCD format.
a) 3 bits
b) 6 bits
c) 12 bits
d) 24 bits

Answer: c
Explanation: The number of bits needed to represent a given decimal number is always greater than the number of bits required for a straight binary encoding of the same. Hence, a three digit decimal number requires 12 bits for representation in BCD format.

8. How many bits would be required to encode decimal numbers 0 to 9999 in straight binary codes?
a) 12
b) 14
c) 16
d) 18

Answer: b
Explanation: Total number of decimals to be represented = 10000 = $10^4 = 2^n$ (where n is the number of bits required) = $2^{13.29}$. Therefore, the number of bits required for straight binary encoding = 14.

9. The excess-3 code for 597 is given by _____
a) 100011001010
b) 100010100111
c) 010110010111
d) 010110101101

Answer: a
Explanation: The addition of ‘3’ to each digit yields the three new digits ‘8’, ’12’ and ’10’.

Hence, the corresponding four-bit binary equivalents are 100011001010, in accordance to 8421 format.

10. The decimal equivalent of the excess-3 number 110010100011.01110101 is _____
a) 970.42
b) 1253.75
c) 861.75
d) 1132.87

Answer: a
Explanation: The conversion of binary numbers into digits '1100', '1010', '0011', '0111' and '0101' gives '12', '5', '3', '7' and '5' respectively. Hence, the decimal number is 970.42.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on "Karnaugh Map".

1. A Karnaugh map (K-map) is an abstract form of _____ diagram organized as a matrix of squares.
a) Venn Diagram
b) Cycle Diagram
c) Block diagram
d) Triangular Diagram

Answer: a
Explanation: A Karnaugh map (K-map) is an abstract form of Venn diagram organized as a matrix of squares, where each square represents a Maxterm or a Minterm.

2. There are _____ cells in a 4-variable K-map.
a) 12
b) 16
c) 18
d) 8

Answer: b
Explanation: There are 16 = (2^4) cells in a 4-variable K-map.

3. The K-map based Boolean reduction is based on the following Unifying Theorem: A + A' = 1.
a) Impact
b) Non Impact
c) Force
d) Complementarity

Answer: b
Explanation: The given expression A +A' = 1 is based on non-impact unifying theorem.

4. Each product term of a group, w'.x.y' and w.y, represents the _____ in that group.
a) Input
b) POS
c) Sum-of-Minterms
d) Sum of Maxterms

Answer: c
Explanation: In a minterm, each variable w, x or y appears once either as the variable itself or as the inverse. So, the given expression satisfies the property of Sum of Minterm.

5. The prime implicant which has at least one element that is not present in any other implicant is known as _____
a) Essential Prime Implicant
b) Implicant
c) Complement
d) Prime Complement

Answer: a
Explanation: Essential prime implicants are prime implicants that cover an output of the function that no combination of other prime implicants is able to cover.

6. Product-of-Sums expressions can be implemented using _____
a) 2-level OR-AND logic circuits
b) 2-level NOR logic circuits
c) 2-level XOR logic circuits
d) Both 2-level OR-AND and NOR logic circuits

Answer: d
Explanation: Product-of-Sums expressions can be implemented using 2-level OR-AND & NOR logic circuits.

7. Each group of adjacent Minterms (group size in powers of twos) corresponds to a possible product term of the given _____
a) Function
b) Value
c) Set
d) Word

Answer: a
Explanation: Each group of adjacent Minterms (group size in powers of twos) corresponds to a possible product term of the given function.

8. Don’t care conditions can be used for simplifying Boolean expressions in _____
a) Registers
b) Terms
c) K-maps
d) Latches

Answer: c
Explanation: Don’t care conditions can be used for simplifying Boolean expressions in K-maps which helps in pairing with 1/0.

9. It should be kept in mind that don’t care terms should be used along with the terms that are present in _____
a) Minterms
b) Expressions
c) K-Map
d) Latches

Answer: a
Explanation: It should be kept in mind that don’t care terms should be used along with the terms that are present in minterms as well as maxterms which reduces the complexity of the boolean expression.

10. Using the transformation method you can realize any POS realization of OR-AND with only.
a) XOR
b) NAND
c) AND
d) NOR

Answer: d
Explanation: Using the transformation method we can realize any POS realization of OR-AND with only NOR.

11. There are many situations in logic design in which simplification of logic expression is possible in terms of XOR and _____ operations.
a) X-NOR
b) XOR
c) NOR
d) NAND

Answer: a
Explanation: There are many situations in logic design in which simplification of logic expression is possible in terms of XOR and XNOR operations.
Expression of XOR : AB’ + A’B
Expression of XNOR : AB + A’B’

12. These logic gates are widely used in _____ design and therefore are available in IC form.
a) Sampling
b) Digital
c) Analog
d) Systems

Answer: b
Explanation: These logic gates(XOR, XNOR, NOR) are widely used in digital design and therefore are available in IC form as digital circuits deal with data transmission in the form of binary digits.

13. In case of XOR/XNOR simplification we have to look for the following _____
a) Diagonal Adjacencies
b) Offset Adjacencies
c) Straight Adjacencies
d) Both diagonal and offset adjencies

Answer: d
Explanation: In case of XOR/XNOR simplification we have to look for the following diagonal and offset adjacencies. XOR gives output 1 when odd number of 1s are present in input while XNOR gives output 1 when even number of 1s or all 0s are present in input.

14. Entries known as _____ mapping.
a) Diagonal
b) Straight
c) K
d) Boolean

Answer: a
Explanation: Entries known as diagonal mapping. The diagonal mapping holds true when for any relation, there is a projection of product on the factor.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Sum of Products and Products of Sum”.

1. The logical sum of two or more logical product terms is called _____
a) SOP
b) POS
c) OR operation
d) NAND operation

Answer: a
Explanation: The logical sum of two or more logical product terms, is called SOP (i.e. sum of product). The logical product of two or more logical sum terms is called POS (i.e. product of sums).

2. The expression Y=AB+BC+AC shows the _____ operation.
a) EX-OR
b) SOP
c) POS
d) NOR

Answer: b
Explanation: The given expression has the operation product as well as the sum of that. So, it shows SOP operation. POS will be the product of sum terms.

3. The expression Y=(A+B)(B+C)(C+A) shows the _____ operation.
a) AND
b) POS
c) SOP
d) NAND

Answer: b
Explanation: The given expression has the operation sum as well as the product of that. So, it shows POS(product of sum) operation. SOP will be the sum of product terms.

4. A product term containing all K variables of the function in either complemented or uncomplemented form is called a _____
a) Minterm
b) Maxterm
c) Midterm
d) ∑ term

Answer: a
Explanation: A product term containing all K variables of the function in either complemented or uncomplemented form is called a minterm. A sum term containing all K variables of the function in either complemented or uncomplemented form is called a maxterm.

5. According to the property of minterm, how many combination will have value equal to 1 for K input variables?
a) 0
b) 1
c) 2
d) 3

Answer: b
Explanation: The main property of a minterm is that it possesses the value 1 for only one combination of K input variables and the remaining will have the value 0.

6. The canonical sum of product form of the function y(A,B) = A + B is _____
a) AB + BB + A'A
b) AB + AB' + A'B
c) BA + BA' + A'B'
d) AB' + A'B + A'B'

Answer: b
Explanation: A + B = A.1 + B.1 = A(B + B') + B(A + A') = AB + AB' + BA +BA' = AB + AB' + A'B = AB + AB' + A'B.

7. A variable on its own or in its complemented form is known as a _____
a) Product Term
b) Literal
c) Sum Term
d) Word

Answer: b
Explanation: A literal is a single logic variable or its complement. For example — X, Y, A', Z, X' etc.

8. Maxterm is the sum of _____ of the corresponding Minterm with its literal complemented.
a) Terms
b) Words
c) Numbers
d) Nibble

Answer: a
Explanation: Maxterm is the sum of terms of the corresponding Minterm with its literal complemented.

9. Canonical form is a unique way of representing _____
a) SOP
b) Minterm
c) Boolean Expressions
d) POS

Answer: c
Explanation: Boolean Expressions are represented through a canonical form. An example of canonical form is A'B'C' + AB'C + ABC'.

10. There are _____ Minterms for 3 variables (a, b, c).
a) 0
b) 2
c) 8
d) 1

Answer: c
Explanation: Minterm is given by 2^n . So, 2^3 = 8 minterms are required.

11. _____ expressions can be implemented using either (1) 2-level AND-OR logic circuits or (2) 2-level NAND logic circuits.
a) POS
b) Literals
c) SOP
d) POS

Answer: c
Explanation: SOP expressions can be implemented using either (1) 2-level AND-OR logic circuits or (2) 2-level NAND logic circuits.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on "Boolean Logic Operations".

1. In boolean algebra, the OR operation is performed by which properties?
a) Associative properties
b) Commutative properties
c) Distributive properties
d) All of the Mentioned

Answer: d
Explanation: The expression for Associative property is given by A+(B+C) = (A+B)+C & A*(B*C) = (A*B)*C.
The expression for Commutative property is given by A+B = B+A & A*B = B*A.
The expression for Distributive property is given by A+BC=(A+B)(A+C) & A(B+C) = AB+AC.

2. The expression for Absorption law is given by _____
a) A + AB = A
b) A + AB = B
c) AB + AA' = A
d) A + B = B + A

Answer: a
Explanation: The expression for Absorption Law is given by: A+AB = A.
Proof: A + AB = A(1+B) = A (Since 1 + B = 1 as per 1's Property).

3. According to boolean law: A + 1 = ?
a) 1
b) A
c) 0
d) A'

Answer: a
Explanation: A + 1 = 1, as per 1's Property.

4. The involution of A is equal to _____
a) A
b) A'
c) 1
d) 0

Answer: a
Explanation: The involution of A means double inversion of A (i.e. A”) and is equal to A.
Proof: ((A)’)’ = A

5. A(A + B) = ?
a) AB
b) 1
c) (1 + AB)
d) A

Answer: d
Explanation: A(A + B) = AA + AB (By Distributive Property) = A + AB (A.A = A By Commutative Property) = A(1 + B) = A*1 (1 + B = 1 by 1’s Property) = A.

6. DeMorgan’s theorem states that _____
a) (AB)’ = A’ + B’
b) (A + B)’ = A’ * B
c) A’ + B’ = A’B’
d) (AB)’ = A’ + B

Answer: a
Explanation: The DeMorgan’s law states that (AB)’ = A’ + B’ & (A + B)’ = A’ * B’, as per the Dual Property.

7. (A + B)(A’ * B’) = ?
a) 1
b) 0
c) AB
d) AB’

Answer: b
Explanation: The DeMorgan’s law states that (AB)’ = A’ + B’ & (A + B)’ = A’ * B’, as per the Dual Property.

8. Complement of the expression A’B + CD’ is _____
a) (A’ + B)(C’ + D)
b) (A + B’)(C’ + D)
c) (A’ + B)(C’ + D)
d) (A + B’)(C + D’)

Answer: b
Explanation: (A’B + CD’)’ = (A’B)'(CD’)’ (By DeMorgan’s Theorem) = (A” + B’)(C’ + D”) (By DeMorgan’s Theorem) = (A + B’)(C’ + D).

9. Simplify Y = AB’ + (A’ + B)C.
a) AB’ + C
b) AB + AC
c) A’B + AC’
d) AB + A

Answer: a
Explanation: Y = AB’ + (A’ + B)C = AB’ + (AB’)’C = (AB’ + C)(AB’ + AB’) = (AB’ + C).1 = (AB’ + C).

10. The boolean function A + BC is a reduced form of _____
a) AB + BC
b) (A + B)(A + C)
c) A’B + AB’C
d) (A + C)B

Answer: b
Explanation: (A + B)(A + C) = AA + AC + AB + BC = A + AC + AB + BC (By Commutative Property) = A(1 + C + B) + BC = A + BC (1 + B + C =1 By 1’s Property).

This set of Digital Electronic Circuits Questions and Answers for freshers focuses on “Quine-McCluskey or Tabular Method of Minimization of Logic Functions”.

1. The output of an EX-NOR gate is 1. Which input combination is correct?
a) A = 1, B = 0
b) A = 0, B = 1
c) A = 0, B = 0
d) A = 0, B’ = 1

Answer: c
Explanation: The output of EX-NOR gate is given by AB + A’B’. So, for A = 0 and B = 0 the output will be 1.

2. In which of the following gates the output is 1 if and only if at least one input is 1?
a) AND
b) NOR
c) NAND
d) OR

Answer: d
Explanation: In or gate we need at least one bit to be equal to 1 to generate the output as 1 because OR means any of the condition out of two is equal to 1 which means if at least one input is 1 then it shows output as 1.

3. The time required for a gate or inverter to change its state is called _____
a) Rise time
b) Decay time
c) Propagation time
d) Charging time

Answer: c
Explanation: The time required for a gate or inverter to change its state is called propagation time.

4. What is the minimum number of two input NAND gates used to perform the function of two input OR gates?
a) One
b) Two
c) Three
d) Four

Answer: c
Explanation: Y = A + B. This is the equation of OR gate. We require 3 NAND gates to create OR gate. We can also write,
1st, 2nd and 3rd NAND operations as: Y = ((NOT A) AND (NOT B))’ = A’’ + B’’ = (A+B).

5. Odd parity of word can be conveniently tested by _____
a) OR gate
b) AND gate
c) NAND gate
d) XOR gate

Answer: d
Explanation: Odd parity of word can be conveniently tested by XOR gate, since, XOR outputs 1 only when the input has odd number of 1’s.

6. The number of full and half adders are required to add 16-bit number is _____
a) 8 half adders, 8 full adders
b) 1 half adders, 15 full adders
c) 16 half adders, 0 full adders
d) 4 half adders, 12 full adders

Answer: b
Explanation: Half adder has two inputs and two outputs whereas Full Adder has 3 inputs and 2 outputs. One half adder can add the least significant bit of the two numbers whereas full adders are required to add the remaining 15 bits as they all involve adding carries.

7. Which of the following will give the sum of full adders as output?
a) Three point major circuit
b) Three bit parity checker
c) Three bit comparator
d) Three bit counter

Answer: d
Explanation: Counters are used for counting purposes in ascending or descending order. Three bit counter will give the sum of full adders as output.

8. Which of the following gate is known as coincidence detector?
a) AND gate
b) OR gate
c) NOR gate
d) NAND gate

Answer: a
Explanation: AND gate is known as coincidence detector due to multiplicity behaviour, as it outputs 1 only when all the inputs are 1.

9. An OR gate can be imagined as _____
a) Switches connected in series
b) Switches connected in parallel
c) MOS transistor connected in series
d) BJT transistor connected in series

Answer: b
Explanation: OR gate means addition of two inputs, which outputs when any of the input is high. Due to this reason, it is imagined as switches connected in parallel.

10. How many full adders are required to construct an m-bit parallel adder?
a) m/2
b) m
c) m-1
d) m+1

Answer: c
Explanation: We need adder for every bit. So we should need m bit adders. A full adder adds a carry bit to two inputs and produces an output and a carry. But the most significant bits can use a half adder which differs from the full adder as in that it has no carry input, so we need m-1 full adders and 1 half adder in m bit parallel adder.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Logic Gates and Networks – 1”.

1. The output of a logic gate is 1 when all the input are at logic 0 as shown below:

INPUT		**OUTPUT**
A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

INPUT		**OUTPUT**
A	B	C
0	0	1
0	1	0
1	0	0
1	1	1

The gate is either _____
a) A NAND or an EX-OR

b) An OR or an EX-NOR
c) An AND or an EX-OR
d) A NOR or an EX-NOR

Answer: d
Explanation: The output of a logic gate is 1 when all inputs are at logic 0. The gate is NOR. The output of a logic gate is 1 when all inputs are at logic 0 or all inputs are at logic 1, then it is EX-NOR. (The truth tables for NOR and EX-NOR Gates are shown in the above table).

2. The code where all successive numbers differ from their preceding number by single bit is _____
a) Alphanumeric Code
b) BCD
c) Excess 3
d) Gray

Answer: d
Explanation: The code where all successive numbers differ from their preceding number by single bit is gray code. It is an unweighted code. The most important characteristic of this code is that only a single bit change occurs when going from one code number to next. BCD Code is one in which decimal digits are represented by a group of 4-bits each, whereas, in Excess-3 Code, the decimal numbers are incremented by 3 and then written in their BCD format.

3. The following switching functions are to be implemented using a decoder:
f1 = ∑m(1, 2, 4, 8, 10, 14) f2 = ∑m(2, 5, 9, 11) f3 = ∑m(2, 4, 5, 6, 7)
The minimum configuration of decoder will be _____
a) 2 to 4 line
b) 3 to 8 line
c) 4 to 16 line
d) 5 to 32 line

Answer: c
Explanation: 4 to 16 line decoder as the minterms are ranging from 1 to 14.

4. How many AND gates are required to realize Y = CD + EF + G?
a) 4
b) 5
c) 3
d) 2

Answer: d
Explanation: To realize Y = CD + EF + G, two AND gates are required and two OR gates are required.

5. The NOR gate output will be high if the two inputs are _____
a) 00
b) 01
c) 10
d) 11

Answer: a
Explanation: In 01, 10 or 11 output is low if any of the I/P is high. So, the correct option will be 00.

6. How many two-input AND and OR gates are required to realize Y = CD+EF+G?
a) 2, 2
b) 2, 3
c) 3, 3
d) 3, 2

Answer: a
Explanation: Y = CD + EF + G
The number of two input AND gate = 2
The number of two input OR gate = 2.

7. A universal logic gate is one which can be used to generate any logic function. Which of the following is a universal logic gate?
a) OR
b) AND
c) XOR
d) NAND

Answer: d
Explanation: An Universal Logic Gate is one which can generate any logic function and also the three basic gates: AND, OR and NOT. Thus, NOR and NAND can generate any logic function and are thus Universal Logic Gates.

8. A full adder logic circuit will have _____
a) Two inputs and one output
b) Three inputs and three outputs
c) Two inputs and two outputs
d) Three inputs and two outputs

Answer: d
Explanation: A full adder circuit will add two bits and it will also accounts the carry input generated in the previous stage. Thus three inputs and two outputs (Sum and Carry) are there. In case of half adder circuit, there are only two inputs bits and two outputs (SUM and CARRY).

9. How many two input AND gates and two input OR gates are required to realize Y = BD + CE + AB?
a) 3, 2
b) 4, 2
c) 1, 1
d) 2, 3

Answer: a
Explanation: There are three product terms. So, three AND gates of two inputs are required. As only two input OR gates are available, so two OR gates are required to get the logical sum of three product terms.

10. Which of the following are known as universal gates?
a) NAND & NOR
b) AND & OR
c) XOR & OR
d) EX-NOR & XOR

Answer: a
Explanation: The NAND & NOR gates are known as universal gates because any digital circuit can be realized completely by using either of these two gates, and also they can generate the 3 basic gates AND, OR and NOT.

11. The gates required to build a half adder are _____
a) EX-OR gate and NOR gate
b) EX-OR gate and OR gate
c) EX-OR gate and AND gate
d) EX-NOR gate and AND gate

Answer: c
Explanation: The gates required to build a half adder are EX-OR gate and AND gate. EX-OR outputs the SUM of the two input bits whereas AND outputs the CARRY of the two input bits.

This set of Digital Electronic Circuits Interview Questions and Answers for freshers focuses on “Logic Gates and Networks-2”.

1. A single transistor can be used to build which of the following digital logic gates?
a) AND gates
b) OR gates
c) NOT gates
d) NAND gates

Answer: c
Explanation: A transistor can be used as a switch. That is when base is low collector is high (input zero, output one) and base is high collector is low (input 1, output 0).

2. How many truth table entries are necessary for a four-input circuit?
a) 4
b) 8
c) 12
d) 16

Answer: d
Explanation: For 4 inputs: 2^4 = 16 truth table entries are necessary.

3. Which input values will cause an AND logic gate to produce a HIGH output?
a) At least one input is HIGH
b) At least one input is LOW
c) All inputs are HIGH
d) All inputs are LOW

Answer: c
Explanation: For AND gate, the output is high only when both inputs are high. That's why the high output in AND will occurs only when all the inputs are high. However, in case of OR gate, if atleast one input is high, the output will be high.

4. Exclusive-OR (XOR) logic gates can be constructed from what other logic gates?
a) OR gates only
b) AND gates and NOT gates
c) AND gates, OR gates, and NOT gates
d) OR gates and NOT gates

Answer: c
Explanation: Expression for XOR is: A.(B')+(A').B
So in the above expression, the following logic gates are used: AND, OR, NOT.
Thus, 2 AND gates with two-inputs and 1 OR gate with two-inputs will be required for constructing a XOR gate.

5. The basic logic gate whose output is the complement of the input is the _____
a) OR gate
b) AND gate
c) INVERTER gate
d) XOR gate

Answer: c
Explanation: It is also called NOT gate and it simply inverts the input, such that 1 becomes 0 and 0 becomes 1.

6. The AND function can be used to _____ and the OR function can be used to _____
a) Enable, disable
b) Disable, enable
c) Synchronize, energize
d) Detect, invert

Answer: a
Explanation: The AND gate and OR gate are used for enabling and disabling respectively because of their multiplicity and additivity property. The AND gate outputs 1 when all inputs are at logic 1, whereas the OR gate outputs 0 when all inputs are at logic 0.

7. The dependency notation ">=1" inside a block stands for which operation?
a) OR
b) XOR
c) AND
d) XNOR

Answer: a
Explanation: The dependency notation “>=1” inside a block stands for OR operation.

8. If we use an AND gate to inhibit a signal from passing one of the inputs must be _____
a) LOW
b) HIGH
c) Inverted
d) Floating

Answer: a
Explanation: AND gate means A*B and OR gate means A+B and to inhibit means to get low signal, one of the input must be low. It means (0*1=0 or 1*0=0) we will get low output signal. Thus, AND gate outputs 1 only when all inputs are at logic level 1 else it outputs 0.

9. Logic gate circuits contain predictable gate functions that open theirs _____
a) Outputs
b) Inputs
c) Pre-state
d) Impedance state

Answer: b
Explanation: Logic gate circuits contain predictable gate functions that open their inputs because we are free to give any types of inputs.

10. How many NAND circuits are contained in a 7400 NAND IC?
a) 1
b) 2
c) 4
d) 8

Answer: c
Explanation: 7400 IC’s pin has total 14 pin. Pin no 7 use for GND and pin no 14 used for +vcc and remaining pins used for connections. For a NAND gate two inputs are required and one output is obtained means for NAND gate 3 pin connections are required. Thus, a 7400IC contains 4 NAND gates with each having 3 pins. Therefore, total 12 pins dedicated for the NAND operation. Rest 2 pins for power supply.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Digital Integrated Circuits – 1”.

1. Which of the following logic families has the highest maximum clock frequency?
a) S-TTL
b) AS-TTL
c) HS-TTL
d) HCMOS

Answer: b
Explanation: AS-TTL (Advanced Schottky) has a maximum clock frequency of 105 MHz. S-TTL (Schottky High Speed TTL) has 100 MHz. Found nothing as HS-TTL. There are H and S separate TTL. HCMOS has 50 MHz clock frequency.

2. Why is the fan-out of CMOS gates frequency dependent?
a) Each CMOS input gate has a specific propagation time and this limits the number of different gates that can be connected to the output of a CMOS gate
b) When the frequency reaches the critical value the gate will only be capable of delivering 70% of the normal output voltage and consequently the output power will be one-half of normal and this defines the upper operating frequency
c) The higher number of gates attached to the output the more frequently they will have to be serviced thus reducing the frequency at which each will be serviced with an input signal
d) The input gates of the FETs are predominantly capacitive and as the signal frequency increases the capacitive loading also increases thereby limiting the number of loads that may be attached to the output of the driving gate

Answer: d
Explanation: Fan out is the measure of maximum number of inputs that a single logic gate

output can drive. Actually power dissipation in CMOS circuits depends on clock frequency. As the frequency increases Pd also increases so fan-out depends on frequency.

3. Logic circuits that are designated as buffers, drivers or buffers/drivers are designed to have _____
a) A greater current/voltage capability than an ordinary logic circuit
b) Greater input current/voltage capability than an ordinary logic circuit
c) A smaller output current/voltage capability than an ordinary logic
d) Greater the input and output current/voltage capability than an ordinary logic circuit

Answer: a
Explanation: Buffer circuits are usually incorporated to isolate the input from the output. Logic circuits that are designated as buffers, drivers or buffer/drivers are designed to have a greater current/voltage capability than an ordinary logic circuit.

4. Which of the following will not normally be found on a data sheet?
a) Minimum HIGH level output voltage
b) Maximum LOW level output voltage
c) Minimum LOW level output voltage
d) Maximum HIGH level input current

Answer: c
Explanation: Minimum LOW level output voltage will not normally be found on a data sheet.

5. Which of the following logic families has the shortest propagation delay?
a) S-TTL
b) AS-TTL
c) HS-TTL
d) HCMOS

Answer: b
Explanation: AS-TTL (Advanced Schottky) has a maximum clock frequency that is 105 MHz. So, the propagation delay will be given by 1/105 sec which is the lowest one. It is followed by S-TTL and HCMOS in terms of increasing propagation delay.

6. What is the static charge that can be stored by your body as you walk across a carpet?
a) 300 volts
b) 3000 volts
c) 30000 volts
d) Over 30000 volts

Answer: d
Explanation: When a person walks across a carpeted or tile floor electric charge builds up in the body due to the friction between shoes and floor material. If the friction static is greater the voltage potential develop in the body will be greater. You start act as a capacitor. This is called Electrostatic discharge. The potential static charge that can develop from walking on tile floors is greater than 15000 volts while carpeted floors can generate in excess of 30000 volts.

7. What must be done to interface TTL to CMOS?
a) A dropping resistor must be used on the CMOS of 12 V supply to reduce it to 5 V for the TTL
b) As long as the CMOS supply voltage is 5 V they can be interfaced (however, the fan-out of the TTL is limited to five CMOS gates)
c) A 5 V zener diode must be placed across the inputs of the TTL gates in order to protect them from the higher output voltages of the CMOS gates
d) A pull-up resistor must be used between the TTL output-CMOS input node and Vcc; the value of RP will depend on the number of CMOS gates connected to the node

Answer: d
Explanation: To interface TTL to CMOS a pull-up resistor must be used between the TTL output-CMOS input node and Vcc. A pull-up resistor is used to avoid the floating state on the input node of the CMOS, thus using a small amount of current. The value of RP will depend on the number of CMOS gates connected to the node.

8. What causes low-power Schottky TTL to use less power than the 74XX series TTL?
a) The Schottky-clamped transistor

b) A larger value resistor
c) The Schottky-clamped MOSFET
d) A small value resistor

Answer: b
Explanation: A larger value resistor causes low power low-power Schottky TTL to use less power than the 74XX series TTL.

9. What are the major differences between the 5400 and 7400 series of ICs?
a) The 5400 series are military grade and require tighter supply voltages and temperatures
b) The 5400 series are military grade and allow for a wider range of supply voltages and temperatures
c) The 7400 series are an improvement over the original 5400s
d) The 7400 series was originally developed by Texas Instruments and the 5400 series was brought out by National Semiconductors after TI's patents expired as a second supply source

Answer: b
Explanation: The 5400 series are military grade and allow for a wider range of supply voltages and temperatures, these are the major differences between the 5400 and 7400 series of ICs. Also, the working temperature range of 5400 series is -50 to 125C while that for 7400 is 0 to 70C.

10. Which of the following statements apply to CMOS devices?
a) The devices should not be inserted into circuits with the power on
b) All tools, test equipment and metal workbenches should be tied to earth ground
c) The devices should be stored and shipped in antistatic tubes or conductive foam
d) All of the Mentioned

Answer: d
Explanation: For CMOS devices, all the mentioned statements are applicable. The devices should not be inserted into circuits with the power on. All tools, test equipment and metal workbenches should be tied to earth ground. Also, the devices should be stored and shipped in antistatic tubes or conductive foam.

This set of Digital Electronic/Circuits Interview Questions and Answers for experienced focuses on "Digital Integrated Circuits – 3".

1. MOS families includes _____
a) PMOS and NMOS
b) CMOS and NMOS
c) PMOS, NMOS and CMOS
d) EMOS, NMOS and PMOS

Answer: c
Explanation: Metal Oxide Semiconductor families includes PMOS, NMOS and CMOS.

2. CMOS refers to _____
a) Continuous Metal Oxide Semiconductor
b) Complementary Metal Oxide Semiconductor
c) Centred Metal Oxide Semiconductor
d) Concrete Metal Oxide Semiconductor

Answer: b
Explanation: CMOS refers to Complementary Metal Oxide Semiconductor.

3. Propagation delay is defined as _____
a) the time taken for the output of a gate to change after the inputs have changed
b) the time taken for the input of a gate to change after the outputs have changed
c) the time taken for the input of a gate to change after the intermediates have changed
d) the time taken for the output of a gate to change after the intermediates have changed

Answer: a
Explanation: Propagation delay is defined as the time taken for the output of a gate to change after the inputs have changed.

4. Propagation delay times can be divided as _____
a) t(PLH) and t(LPH)
b) t(LPH) and t(PHL)
c) t(PLH) and t(PHL)
d) t(HPL) and t(LPH)

Answer: c
Explanation: Propagation delay times can be divided as: t(PLH) and t(PHL). t(PLH) stands for propagation from low to high and t(PHL) stands for propagation from high to low.

5. The delay times are measured between the _____ % voltage levels of the input and output waveforms.
a) 50
b) 75
c) 25
d) 100

Answer: a
Explanation: Propagation delay is the time taken by the output to change it's state when the input changes. The average of the two propagation delays is given by (t1 + t2)/2, which gives the intermediate value. So, the delay times are measured between the 50% voltage levels of the input and output waveforms.

6. Power Dissipation in DIC is expressed in _____
a) Watts or kilowatts
b) Milliwatts or nanowatts
c) DB
d) Mdb

Answer: b
Explanation: Power Dissipation in DIC is expressed in milliwatts or nanowatts.

7. Fan-in is defined as _____
a) the number of outputs connected to gate without any degradation in the voltage levels
b) the number of inputs connected to gate without any degradation in the voltage levels
c) the number of outputs connected to gate with degradation in the voltage levels
d) the number of inputs connected to gate with degradation in the voltage levels

Answer: b
Explanation: Fan-in is defined as the maximum number of inputs that can be connected to the output of a gate without any degradation in the voltage levels. For example, an eight-input gate requires one Unit Load per input. It's fan-in is 8.

8. The maximum noise voltage that may appear at the input of a logic gate without changing the logical state of its output is termed as _____
a) Noise Margin
b) Noise Immunity
c) White Noise
d) Signal to Noise Ratio

Answer: b
Explanation: The maximum noise voltage that may appear at the input of a logic gate without changing the logical state of its output is termed as noise immunity.

9. Depending upon the flow of current from the output of one logic circuit to the input of another the logic families can be divides into _____ categories.
a) 2
b) 3
c) 4
d) 5

Answer: a
Explanation: Depending upon the flow of current from the output of one logic circuit to the input of another the logic families can be divides into two categories and they are current sourcing

and current sinking. Source means from where the current originates or exits while Sink means where the current enters or is accepted.

10. Fan-in and Fan-out are the characteristics of _____
a) Registers
b) Logic families
c) Sequential Circuits
d) Combinational Circuits

Answer: b
Explanation: Fan-in and Fan-out are the characteristics of logic families. Fan-in is the measure of maximum number of inputs that a single gate output can drive or accept. Whereas, Fan-out means the maximum number of inputs that can be fed by a single output.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Register-Transistor Logic(RTL)”.

1. All input of NOR as low produces result as _____
a) Low
b) Mid
c) High
d) Floating

Answer: c
Explanation: All input of NOR as low produces the result as high, whereas, rest all conditions produce output as low.

2. In RTL NOR gate, the output is at logic 1 only when all the inputs are at _____
a) logic 0
b) logic 1
c) +10V
d) Floating

Answer: a
Explanation: RTL NOR gate behaves as NOR gate and the output of NOR gate will be 1 only when all the inputs are at logic 0 and in rest conditions of the input, the output is 0.

3. Resistor–transistor logic (RTL) is a class of digital circuits built using _____ as the input network and _____ as switching devices.
a) Resistors, bipolar junction transistors (BJTs)
b) Bipolar junction transistors (BJTs), Resistors
c) Capacitors, resistors
d) Resistors, capacitors

Answer: a
Explanation: Resistor–transistor logic (RTL) is a class of digital circuits built using resistors as the input network and bipolar junction transistors (BJTs) as switching devices.

4. RTL consists of a common emitter stage with a _____ connected between the base and the input voltage source.
a) collector
b) base resistor
c) capacitor
d) inductor

Answer: b
Explanation: RTL consist of a common emitter stage with a base resistor connected between the base and the input voltage source. The role of base resistor is to expand the negligible transistor input voltage range (about 0.7 V) to the logical “1” level (about 3.5 V) by converting the input voltage into a current. Thus, base resistor plays a major role in biasing of the transistor.

5. The role of the _____ is to convert the collector current into a voltage in RTL.
a) Collector resistor
b) Base resistor

c) Capacitor
d) Inductor

Answer: a
Explanation: The role of the collector resistor is to convert the collector current into a voltage; its resistance is chosen high enough to saturate the transistor and low enough to obtain low output resistance. Base Resistor is to provide the necessary biasing to the base of the transistor in order to activate it.

6. The limitations of the one transistor RTL NOR gate are overcome by _____
a) Two-transistor RTL implementation
b) Three-transistor RTL implementation
c) Multi-transistor RTL implementation
d) Four-transistor RTL implementation

Answer: c
Explanation: The limitations of the one transistor RTL NOR gate are overcome by the use of multi transistor RTL. It consists of a set of parallel connected transistor switches driven by the logic inputs.

7. The primary advantage of RTL technology was that _____
a) It results as low power dissipation
b) It uses a minimum number of resistors
c) It uses a minimum number of transistors
d) It operates swiftly

Answer: c
Explanation: The primary advantage of RTL technology was that it uses a minimum number of transistors. It consists of registers in large amount and it results in as high power dissipation. The resistors act as the input network and the transistors performs the switching operation.

8. The disadvantage of RTL is that _____
a) It uses a maximum number of resistors
b) It results in high power dissipation
c) High noise creation
d) It uses a minimum number of transistors

Answer: b
Explanation: The disadvantage of RTL is its high power dissipation when the transistor is switched on by current flowing in the collector and base resistor. This requires that more current be supplied to and heat be removed from RTL circuits. In contrast, TTL circuits with “totem-pole” output stage minimize both of these requirements.

9. TTL circuits with “totem-pole” output stage minimize _____
a) The power dissipation in RTL
b) The time consumption in RTL
c) The speed of transferring rate in RTL
d) Propagation delay in RTL

Answer: a
Explanation: TTL circuits with “totem-pole” output stage minimize the power dissipation and heating effect in RTL.

10. The minimum number of transistors can be used by 2 input AND gate is _____
a) 2
b) 3
c) 4
d) 5

Answer: a
Explanation: The minimum number of transistors can be used by 2 input AND gate is 2 and maximum up to 3.

his set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Diode-Transistor Logic(DTL)”.

1. Diode–transistor logic (DTL) is the direct ancestor of _____
a) Register-transistor logic
b) Transistor–transistor logic
c) High threshold logic
d) Emitter Coupled Logic

Answer: b
Explanation: Diode–transistor logic (DTL) is a class of digital circuits that is the direct ancestor of transistor–transistor logic. To overcome the shortcomings of DTL, TTL came into existence.

2. In DTL logic gating function is performed by _____
a) Diode
b) Transistor
c) Inductor
d) Capacitor

Answer: a
Explanation: Diode serves as the input network and the switching operation is performed by the transistor.

3. In DTL amplifying function is performed by _____
a) Diode
b) Transistor
c) Inductor
d) Capacitor

Answer: b
Explanation: The amplifying and switching function is performed by a transistor and the diode acts an input network in DTL.

4. How many stages a DTL consist of?
a) 2
b) 3
c) 4
d) 5

Answer: b
Explanation: The DTL circuit shown in the picture consists of three stages: an input diode logic stage, an intermediate level shifting stage and an output common-emitter amplifier stage.

5. The full form of CTDL is _____
a) Complemented transistor diode logic
b) Complemented transistor direct logic
c) Complementary transistor diode logic
d) Complementary transistor direct logic

Answer: a
Explanation: The full form of CTDL is Complemented transistor diode logic.

6. The DTL propagation delay is relatively _____
a) Large
b) Small
c) Moderate
d) Negligible

Answer: a
Explanation: Propagation delay refers to the time taken by the output to change it’s state when the input is altered. When the transistor goes into saturation from all inputs being high charge is stored in the base region. When it comes out of saturation (one input goes low) this charge has to be removed and will dominate the propagation time which results as a large propagation delay. Thus, it has small clock frequency.

7. The way to speed up DTL is to add an across intermediate resister is _____
a) Small “speed-up” capacitor
b) Large “speed-up” capacitor

c) Small “speed-up” transistor
d) Large ” speed-up” transistor

Answer: a
Explanation: One way to speed up DTL is to add a small “speed-up” capacitor across intermediate resister. The capacitor helps to turn off the transistor by removing the stored base charge; the capacitor also helps to turn on the transistor by increasing the initial base drive.

8. The process to avoid saturating the switching transistor is performed by _____
a) Baker clamp
b) James R. Biard
c) Chris Brown
d) Totem-Pole

Answer: a
Explanation: Another way to speed up DTL other than adding a small “speed-up” capacitor across intermediate resister is to avoid saturating the switching transistor which can be done with a Baker clamp. The name Baker clamp is given at the name of Richard H. Baker, who described it in his 1956 technical report “Maximum Efficiency Switching Circuits”.

9. A major advantage of DTL over the earlier resistor–transistor logic is the _____
a) Increased fan out
b) Increased fan in
c) Decreased fan out
d) Decreased fan in

Answer: b
Explanation: A major advantage over the earlier resistor–transistor logic is the increased fan in. Fan-in is the measure of the maximum number of inputs that a single gate output can accept.

10. To increase fan-out of the gate in DTL _____
a) An additional capacitor may be used
b) An additional resister may be used
c) An additional transistor and diode may be used
d) Only an additional diode may be used

Answer: c
Explanation: To increase fan-out of the gate in DTL, an additional transistor and diode may be used. Here, the fan out means the number of maximum input that a single gate output can feed.

11. A disadvantage of DTL is _____
a) The input transistor to the resister
b) The input resister to the transistor
c) The increased fan-in
d) The increased fan-out

Answer: b
Explanation: A disadvantage of DTL is the input resistor to the transistor and its presence tends to slow the circuit down. Hence limiting the speed at which the transistor is able to switch states. Thus, the propagation delay increases.

This set of Digital Electronic/Circuits Questions and Answers for experienced focuses on “Digital Integrated Circuits-2”.

1. SSI refers to _____
a) Small Scale Integration
b) Short Scale Integration
c) Small Set Integration
d) Short Set Integration

Answer: a
Explanation: SSI refers to Small Scale Integration.

2. Small Scale Integration(SSI) refers to ICs with _____ gates on the same chip.
a) Fewer than 10
b) Greater than 10

c) Equal to 10
d) Greater than 50

Answer: a
Explanation: Small Scale Integration(SSI) refers to ICs with fewer than 10 gates on the same chip.

3. MSI means _____
a) Merged Scale Integration
b) Main Scale Integration
c) Medium Scale Integration
d) Main Set Integration

Answer: c
Explanation: MSI means Medium Scale Integration.

4. MSI includes _____ gates per chip.
a) 12 to 100
b) 13 to 50
c) greater than 10
d) greater than 100

Answer: a
Explanation: Medium Scale Integration includes 12 to 100 gates per chip.

5. LSI means _____ and refers to _____ gates per chip.
a) Long Scale Integration, more than 10 upto 10000
b) Large Scale Integration, more than 100 upto 5000
c) Large Short Integration, less than 10 and greater than 5000
d) Long Short Integration, more than 10 upto 10000

Answer: b
Explanation: The full form of LSI is Large Scale Integration and refers to more than 100 upto 5000 gates per chip.

6. Integrated circuits are classified as _____
a) Large, Small and Medium
b) Very Large, Small and Linear
c) Linear and Digital
d) Non-Linear and Digital

Answer: c
Explanation: Integrated circuits are classified as Linear and Digital. Linear operates with continuous and digital refers to discrete signals.

7. According to the IC fabrication process logic families can be divided into two broad categories as _____
a) RTL and TTL
b) HTL and MOS
c) ECL and DTL
d) Bipolar and MOS

Answer: d
Explanation: According to the IC fabrication process logic families can be divided into two broad categories as: Bipolar and Metal-oxide semiconductor. The mentioned all others are part of bipolar. Bipolar IC fabrication refers to TTL logic where MOS refers to CMOS logic.

8. The full form of DIP is _____
a) Dual-in-Long Package
b) Dual-in-Line Package
c) Double Integrated Package
d) Double-in-Line Package

Answer: b
Explanation: The full form of DIP is Dual-in-Line Package.

9. LCC refers to _____
a) Longest Chip Carrier
b) Leadless Chip Carrier
c) Leaded Chip Carrier
d) Large Chip Carrier

Answer: b
Explanation: LCC refers to Leadless Chip Carrier.

10. PGA refers to _____
a) Plastic Grid Array
b) Pin Grid Array
c) Pin Greater Array
d) Plastic Greater Array

Answer: b
Explanation: PGA refers to Pin Grid Array.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Digital Circuits Questions and Answers – Transistor Transistor Logic(TTL or T^2L)”.

1. Transistor–transistor logic (TTL) is a class of digital circuits built from _____
a) JFET only
b) Bipolar junction transistors (BJT)
c) Resistors
d) Bipolar junction transistors (BJT) and resistors

Answer: d
Explanation: Transistor–transistor logic (TTL) is a class of digital circuits built from bipolar junction transistors (BJT) and resistors. However, resistors have a small role to play and both logic gating and amplifying functions are performed by the transistors.

2. TTL is called transistor–transistor logic because both the logic gating function and the amplifying function are performed by _____
a) Resistors
b) Bipolar junction transistors
c) One transistor
d) Resistors and transistors respectively

Answer: b
Explanation: TTL is called transistor–transistor logic because both the logic gating function and the amplifying function are performed by bipolar junction transistors (BJTs).

3. TTL was invented in 1961 by _____
a) Baker clamp
b) James L. Buie
c) Chris Brown
d) Frank Wanlass

Answer: b
Explanation: TTL was invented in 1961 by James L Buie.

4. The full form of TCTL is _____
a) Transistor-coupled transistor logic
b) Transistor-capacitor transistor logic
c) Transistor-complemented transistor logic
d) Transistor-complementary transistor logic

Answer: a
Explanation: The full form of TCTL is transistor-coupled transistor logic.

5. The _____ ancestor to the first personal computers.
a) PARAM 1
b) SATYAM 1
c) KENBAK 1

d) MITS Altair

Answer: c
Explanation: The KENBAK 1, ancestor to the first personal computers.

6. TTL inputs are the emitters of a _____
a) Transistor-transistor logic
b) Multiple-emitter transistor
c) Resistor-transistor logic
d) Diode-transistor logic

Answer: b
Explanation: TTL inputs are the emitters of a multiple-emitter transistor.

7. TTL is a _____
a) Current sinking
b) Current sourcing
c) Voltage sinking
d) Voltage sourcing

Answer: a
Explanation: Like DTL, TTL is a current-sinking logic since a current must be drawn from inputs to bring them to a logic 0 level. Current Sink means it accepts current coming out from a source.

8. Standard TTL circuits operate with a __ volt power supply.
a) 2
b) 4
c) 5
d) 3

Answer: c
Explanation: Standard TTL circuits operate with a 5-volt power supply.

9. TTL devices consume substantially _____ power than equivalent CMOS devices at rest.
a) Less
b) More
c) Equal
d) Very High

Answer: b
Explanation: TTL devices consume substantially more power than equivalent CMOS devices at rest. Thus, CMOS devices are faster than TTL devices.

10. A TTL gate may operate inadvertently as an _____
a) Digital amplifier
b) Analog amplifier
c) Inverter
d) Regulator

Answer: b
Explanation: A TTL gate may operate inadvertently as an analog amplifier if the input is connected to a slowly changing input signal that traverses the unspecified region from 0.7V to 3.3V.

11. The speed of _____ circuits is limited by the tendency of common emitter circuits to go into saturation.
a) TTL
b) ECL
c) RTL
d) DTL

Answer: a
Explanation: The speed of TTL circuits is limited by the tendency of common emitter circuits to go into saturation due to the injection of minority carriers into the collector region. Hence, it functions slowly compared to CMOS devices.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Emitter-Coupled Logic(ECL)”.

1. The full form of ECL is _____
a) Emitter-collector logic
b) Emitter-complementary logic
c) Emitter-coupled logic
d) Emitter-cored logic

Answer: c
Explanation: The full form of ECL is emitter-coupled logic.

2. Which logic is the fastest of all the logic families?
a) TTL
b) ECL
c) HTL
d) DTL

Answer: b
Explanation: ECL is the fastest of all the logic families because of the emitters of many transistors are coupled together which results in the highest transmission rate.

3. The full form of CML is _____
a) Complementary mode logic
b) Current mode logic
c) Collector mode logic
d) Collector Mixed Logic

Answer: c
Explanation: The full form of CML is Collector Mode Logic.

4. Sometimes ECL can also be named as _____
a) EEL
b) CEL
c) CML
d) CCL

Answer: c
Explanation: ECL (Emitter Coupled Logic) can also be named as CML(Collector Mode Logic).

5. In an ECL the output is taken from _____
a) Emitter
b) Base
c) Collector
d) Junction of emitter and base

Answer: c
Explanation: Though, the emitter and collector of the ECL are coupled together. So, the output will be taken from a collector.

6. The ECL behaves as _____
a) NOT gate
b) NOR gate
c) NAND gate
d) AND gate

Answer: b
Explanation: The ECL behaves as NOR gate because if any of the input voltages go high as compared to the reference voltage, the output is low and the output is high only when all the input voltages are low.

7. In ECL the fanout capability is _____
a) High
b) Low
c) Zero
d) Sometimes high and sometimes low

Answer: a
Explanation: If the input impedance is high and the output resistance is low; as a result, the transistors change states quickly, gate delays are low, and the fanout capability is high. Fan-out is the measure of the maximum number of inputs that a single gate output can accept.

8. ECL's major disadvantage is that _____
a) It requires more power
b) It's fanout capability is high
c) It creates more noise
d) It is slow

Answer: a
Explanation: ECL's major disadvantage is that each gate continuously draws current, which means it requires (and dissipates) significantly more power than those of other logic families. But ECL logic gates have clock frequency. Thus, they have a fast operation.

9. The full form of SCFL is _____
a) Source-collector logic
b) Source-coupled logic
c) Source-complementary logic
d) Source Cored Logic

Answer: b
Explanation: The full form of SCFL is source-coupled logic.

10. The equivalent of emitter-coupled logic made out of FETs is called _____
a) CML
b) SCFL
c) FECL
d) EFCL

Answer: b
Explanation: The equivalent of emitter-coupled logic made out of FETs is called Source-coupled logic(SCFL). Like ECL, SCL is also the fastest among the logic families.

11. ECL was invented in _____ by _____
a) 1956, Baker clamp
b) 1976, James R. Biard
c) 1956, Hannon S. Yourke
d) 1976, Yourke

Answer: c
Explanation: ECL was invented in August 1956 at IBM by Hannon S Yourke.

12. At the time of invention, an ECL was called as _____
a) Source-coupled logic
b) Current Mode Logic
c) Current-steering logic
d) Emitter-coupled logic

Answer: c
Explanation: At the time of invention, an ECL was called a current-steering logic because it involved current switching.

13. The ECL circuits usually operates with _____
a) Negative voltage
b) Positive voltage
c) Grounded voltage
d) High Voltage

Answer: a
Explanation: The ECL circuits usually operate with negative power supplies (positive end of the supply is connected to ground), in comparison to other logic families in which negative end of the supply is grounded. It is done mainly to minimize the influence of the power supply

variations on the logic levels as ECL is more sensitive to noise on the VCC and relatively immune to noise on VEE.

14. Low-voltage positive emitter-coupled logic (LVPECL) is a power optimized version of _____
a) ECL
b) VECL
c) PECL
d) LECL

Answer: c
Explanation: Low voltage positive emitter coupled logic (LVPECL) is a power optimized version of PECL using a +3.3 V instead of 5 V supply.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Integrated-injection Logic(I^{2L})”.

1. The full form of IIL is _____
a) Injection integrated logic
b) Integrated inspected logic
c) Integrated injection logic
d) Injection Inspected Logic

Answer: c
Explanation: The full form of IIL is Integrated injection logic. It is made up of multiple bipolar junction transistors and had a speed comparable to TTl and power consumption equivalent to CMOS.

2. Integrated injection logic is a class of digital circuits built with _____
a) Single collector BJT
b) Double emitter BJT
c) Multiple emitter BJT
d) Multiple collector BJT

Answer: d
Explanation: Integrated injection logic is a class of digital circuits built with multiple collector bipolar junction transistors (BJT).

3. IIL has _____ noise immunity.
a) High
b) Low
c) Neutral
d) Nil

Answer: a
Explanation: The full form of IIL is Integrated injection logic. It is made up of multiple bipolar junction transistors and had speed comparable to TTl and power consumption equivalent to CMOS. IIL has high noise immunity because it operates by current instead of voltage.

4. IIL is sometimes also known as _____
a) Single transistor logic
b) Multiple transistor logic
c) Merged transistor logic
d) Mixed Transistor Logic

Answer: c
Explanation: The full form of IIL is Integrated injection logic. It is made up of multiple bipolar junction transistors and had speed comparable to TTl and power consumption equivalent to CMOS. IIL is sometimes also known as merged transistor logic.

5. Integrated Injection logic cannot be denoted as _____
a) IIL
b) I2L
c) I^{2L}
d) I TWO L

Answer: d
Explanation: The full form of IIL is Integrated injection logic. It is made up of multiple bipolar junction transistors and had speed comparable to TTl and power consumption equivalent to CMOS. Integrated Injection logic can be denoted as IIL, I^{2L} and I2L as well.

6. The heart of an I2L circuit is the _____
a) Common collector open emitter inverter
b) Common emitter open collector inverter
c) Open emitter common collector inverter
d) Open Emitter Open Collector Inverter

Answer: b
Explanation: The heart of an I2L circuit is the common emitter open collector inverter. The emitter is connected to the ground, with the base having an input behaving as either current sink or high impedance floating condition. The output of an inverter is connected to the collector.

7. In Integrated Injection, logic input is supplied to the _____
a) Emitter
b) Base
c) Collector
d) Collector Emitter

Answer: b
Explanation: In IIL, the input is supplied to the base as either a current sink (low logic level) or as a high impedance floating condition (high logic level). The output of an inverter is connected to the collector.

8. In Integrated Injection, logic output is received through the _____
a) Emitter
b) Base
c) Collector
d) Base Emitter Junction

Answer: c
Explanation: In Integrated Injection logic output is received through the collector. The output of an inverter is connected at the collector.

9. When the outputs of two inverters are wired together the result is _____
a) A two-input NOR gate
b) A single-input NOR gate
c) A two-input NAND gate
d) A single-input NAND gate

Answer: a
Explanation: When the outputs of two inverters are wired together then the result is a two-input NOR gate because the configuration (NOT A) AND (NOT B) is equivalent to NOT (A OR B). In a NOR gate, the output is high only when all of its input are at logic 0 else, the output is low.

10. IIL was commonly used before the advent of CMOS logic by company _____
a) Samsung
b) Nokia
c) Motorola
d) Apple

Answer: c
Explanation: I2L is relatively simple to construct on an integrated circuit and was commonly used before the advent of CMOS logic by companies such as Motorola.

11. Which company introduced one of the first consumer-grade digital watches (the Black Watch) which used I2L technology?
a) Cambridge Consultants Pvt Ltd
b) Sinclair Radionics Ltd
c) National Research and Development Council
d) Westminster

Answer: b
Explanation: Sinclair Radionics Ltd introduced one of the first consumer-grade digital watches (the Black Watch) in August 1975, which used I2L technology.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “MOS Digital Integrated Circuits”.

1. The full form of MOS is _____
a) Metal oxide semiconductor
b) Metal oxygen semiconductor
c) Metallic oxide semiconductor
d) Metallic oxygen semiconductor

Answer: a
Explanation: The full form of MOS is “Metal Oxide Semiconductor”. It is a type of transistor having 3 layers: a metal conductor, an insulating silicon layer and a semiconductor silicon layer.

2. What are the types of MOSFET devices available?
a) P-type enhancement type MOSFET
b) N-type enhancement type MOSFET
c) Depletion type MOSFET
d) All of the mentioned

Answer: d
Explanation: MOSFET are of two types: enhancement and depletion type. Further, these are classified into n-type and p-type device. The depletion type is switched on without the application of gate bias voltage and the enhancement type is switched on with the application of gate voltage.

3. Which insulating layer used in the fabrication of MOSFET?
a) Aluminium oxide
b) Silicon Nitride
c) Silicon dioxide
d) Aluminium Nitrate

Answer: c
Explanation: Silicon dioxide is used as an insulating layer in the fabrication of MOSFET. It gives an extremely high input resistance in the order of 10^{10} to 10^{15} Ω for MOSFET.

4. Which of the following plays an important role in improving the device performance of MOSFET?
a) Dielectric constant
b) Threshold voltage
c) Power supply voltage
d) Gate to drain voltage

Answer: b
Explanation: In MOSFET, the threshold voltage is typically 3 to 6V. This large voltage is not compatible with the supply of 5V which is used in digital ICs. So, for the improvement of the device’s performance the magnitude of threshold voltage should be reduced.

5. A technique used to reduce the magnitude of threshold voltage of MOSFET is the _____
a) Use of complementary MOSFET
b) Use of Silicon nitride
c) Using thin film technology
d) Increasing potential of the channel

Answer: b
Explanation: Silicon nitride is sandwiched between two SiO2 layer and provide necessary barrier. The dielectric constant of Si3N4 is 7.5, whereas that of SiO2 is 4. This increase in overall dielectric constant reduces threshold voltage.

6. What is used to higher the speed of operation in MOSFET fabrication?
a) Ceramic gate

b) Silicon dioxide
c) Silicon nitride
d) Poly silicon gate

Answer: d
Explanation: In conventional metal gate small overlap capacitance is present, which lowers the speed of operation. With the presence of self aligning property of the poly silicon gate it eliminates this capacitance. Using a process called ion-implantation, polysilicon, the drain and the source get doped. However, the thin oxide under silicon gate acting as a mask for the process and thus develops the gate aligning property.

7. Find the sequence of steps involved in fabrication of poly silicon gate MOSFET?

```
Step 1: Entire wafer surface of a Si3N4 is coated and is etched away with the help of mas
source, gate and drain.
Step 2: The contact areas are defined using photolithographic process.
Step 3: Selective etching of Si3N4 and growth of thin oxide.
Step 4: The deposition of poly silicon gate.
Step 5: The growth of thick oxide is called field oxide and P implantation.
Step 6: The metallization and interconnection between substrate and source.
```

a) 1->5->3->4->2->6
b) 1->3->4->2->5->6
c) 1->5->4->3->2->6
d) 1->4->2->5->3->6

Answer: a
Explanation: These steps are the sequence of steps involved in fabrication of poly silicon gate MOSFET. With the help of poly silicon gate doping, it highers the speed of operation of the MOSFET.

8. Why MOSFET is preferred over BJT in IC components?
a) MOSFET has low packing density
b) MOSFET has medium packing density
c) MOSFET has high packing density
d) MOSFET has no packing density

Answer: a
Explanation: MOSFET is preferred over BJT because of its low packaging density. Thus, more number of MOSFET memory cells can be accommodated in a particular area as compared to BJT.

9. Critical defects per unit chip area are _____ for a MOS transistor.
a) High
b) Low
c) Neutral
d) Very High

Answer: b
Explanation: Critical defects per unit chip area is low for a MOS transistor because it involves fewer steps in the fabrication of a MOS transistor. Also, MOSFET has low packaging density.

10. MOS is being used in _____
a) LSI
b) VLSI
c) MSI
d) Both LSI and VLSI

Answer: d
Explanation: Since more transistor and circuitry functions can be achieved on a single chip with MOS technology that is why MOS is being used in LSI and VLSI. LSI stands for Large Scale Integration and VLSI stands for Very Large Scale Integration.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Characteristics of CMOS”.

1. The full form of CMOS is _____
a) Capacitive metal oxide semiconductor
b) Capacitive metallic oxide semiconductor
c) Complementary metal oxide semiconductor
d) Complemented metal oxide semiconductor

Answer: c
Explanation: The full form of CMOS is complementary metal oxide semiconductor. In this type of device, both n-type and p-type transistors are used in a complementary way.

2. The full form of COS-MOS is _____
a) Complementary symmetry metal oxide semiconductor
b) Complementary systematic metal oxide semiconductor
c) Capacitive symmetry metal oxide semiconductor
d) Complemented systematic metal oxide semiconductor

Answer: a
Explanation: The full form of COS-MOS is complementary systematic metal oxide semiconductor. In this type of device, both n-type and p-type transistors are used in a complementary way. Usually, the transistors used are MOSFETs.

3. CMOS is also sometimes referred to as _____
a) Capacitive metal oxide semiconductor
b) Capacitive symmetry metal oxide semiconductor
c) Complementary symmetry metal oxide semiconductor
d) Complemented symmetry metal oxide semiconductor

Answer: c
Explanation: CMOS is also sometimes referred to as complementary systematic metal oxide–semiconductor (COS-MOS). In this type of device, both n-type and p-type transistors are used in a complementary way. Usually, the transistors used are MOSFETs.

4. CMOS technology is used in _____
a) Inverter
b) Microprocessor
c) Digital logic
d) Both microprocessor and digital logic

Answer: d
Explanation: CMOS technology is used in Microprocessor, Microcontroller, static RAM and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors (CMOS sensor), data converters and highly integrated transceivers for many types of communication.

5. Two important characteristics of CMOS devices are _____
a) High noise immunity
b) Low static power consumption
c) High resistivity
d) Both high noise immunity and low static power consumption

Answer: d
Explanation: Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Since one transistor of the pair is always off and the series combination draws significant power only momentarily during switching between on and off states. Also, the performance of CMOS is not altered with the presence of noise and thus it has high noise immunity.

6. CMOS behaves as a/an _____
a) Adder
b) Subtractor
c) Inverter
d) Comparator

Answer: c
Explanation: Since, the outputs of the PMOS and NMOS transistors are complementary such

that when the input is low, the output is high and when the input is high, the output is low. Because of this behaviour of input and output, the CMOS circuit's output is the inverse of the input. Whereas, adders and subtractors are combinational circuits.

7. An important characteristic of a CMOS circuit is the _____
a) Noise immunity
b) Duality
c) Symmetricity
d) Noise Margin

Answer: b
Explanation: An important characteristic of a CMOS circuit is the duality that exists between its PMOS transistors and NMOS transistors. Due to the presence of two different types of transistors, the device has a complementary function.

8. CMOS logic dissipates _____ power than NMOS logic circuits.
a) More
b) Less
c) Equal
d) Very High

Answer: b
Explanation: CMOS logic dissipates less power than NMOS logic circuits because CMOS dissipates power only when switching ("dynamic power"). Thus, CMOS has less power consumption and is more efficient.

9. Semiconductors are made of _____
a) Ge and Si
b) Si and Pb
c) Ge and Pb
d) Pb and Au

Answer: a
Explanation: Semiconductors are made of Silicon (Si) and Germanium (Ge). Semiconductors are devices having conductivity between conductors and insulators.

10. Which chip were the first RTC and CMOS RAM chip to be used in early IBM computers, capable of storing a total of 64 bytes?
a) The Samsung 146818
b) The Samsung 146819
c) The Motorola 146818
d) The Motorola 146819

Answer: c
Explanation: The Motorola 146818 was the first RTC and CMOS RAM chip to be used in early IBM computers; capable of storing a total of 64 bytes.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on "BiCMOS Logic Circuits".

1. BiCMOS is an evolved semiconductor technology that integrates two formerly separate semiconductor technologies those of the _____
a) CMOS and FET
b) MOSFET and CMOS
c) BJT and CMOS
d) BJT and MOSFET

Answer: c
Explanation: BiCMOS is an evolved semiconductor technology that integrates two formerly separate semiconductor technologies those of the BJT and CMOS. CMOS ensures low power dissipation, smaller noise margin and higher packaging density, while BJT offers high switching speed and improved noise performance.

2. We use BJT in BiCMOS because of its _____
a) High speed

b) High gain
c) Low output resistance
d) All of the Mentioned

Answer: d
Explanation: Bipolar junction transistors offer high speed, high gain and low output resistance, which are excellent properties for high-frequency analog amplifiers. It also offers high switching speed and improved noise performance.

3. We use CMOS transistor in BiCMOS because of its _____
a) High input resistance
b) Simple construction
c) Low power logic gates
d) All of the Mentioned

Answer: d
Explanation: CMOS ensures low power dissipation, smaller noise margin and higher packaging density. It also offers high input resistance and is excellent for constructing simple, low-power logic gates.

4. When was BiCMOS technology introduced?
a) 1990
b) 1991
c) 1992
d) 1989

Answer: a
Explanation: BiCMOS technology was introduced in 1990s. BiCMOS is an evolved semiconductor technology that integrates two formerly separate semiconductor technologies those of the BJT and CMOS. CMOS ensures low power dissipation, smaller noise margin and higher packaging density, while BJT offers high switching speed and improved noise performance.

5. On which technology the Pentium is based?
a) MOSFET
b) CMOS
c) BiCMOS
d) BJT

Answer: c
Explanation: The Pentium technology is based on BiCMOS technology because BiCMOS circuits use the characteristics of each type of transistor most appropriately. CMOS ensures low power dissipation, smaller noise margin and higher packaging density, while BJT offers high switching speed and improved noise performance.

6. The advantage of BiCMOS circuit is that it gives _____
a) Large fan-out
b) Large fan-in
c) Small fan-in
d) Small fan-out

Answer: a
Explanation: Fan-out is the measure of the maximum number of inputs that a single gate output can feed. BiCMOS circuits are particularly useful for logic with large fan-out (large capacitive load).

7. How many members a BiCMOS family have?
a) 5
b) 6
c) 7
d) 8

Answer: a
Explanation: BICMOS is a combination of both CMOS and BJT technology. The BiCMOS family has mainly 5 members and those are ABT logic, ALB logic, ALVT logic, BCT logic and LVT logic.

8. What is LVT logic?
a) Lower threshold voltage
b) Lower supply threshold voltage
c) Lower supply voltage while retaining TTL logic levels
d) All of the Mentioned

Answer: c
Explanation: LVT stands for Low Voltage BiCMOS Technology which is an integration of less power dissipation and less noise of CMOS along with the high switching speed and output drive of BJT. LVT logic is nothing but the lower supply voltage while retaining TTL logic levels.

9. What does ALVT mean?
a) All lower supply voltage while retaining TTL logic levels
b) ABT lower supply voltage while retaining TTL logic levels
c) Advanced version of LVT logic
d) All version of LVT logic

Answer: c
Explanation: ALVT stands for Advanced Low Voltage BiCMOS Technology (ALVT). It is a faster version of LVT family. It is an integration of less power dissipation and less noise of CMOS along with the high switching speed and output drive of BJT.

10. The full form of PTL is _____
a) Pull transistor logic
b) Push transistor logic
c) Pass transistor logic
d) Post Transistor Logic

Answer: c
Explanation: The full form of PTL is “pass transistor logic”. It combines different logic families to design an integrated circuit. Thus, it reduces the number of transistors used by scraping off the unnecessary transistors.

11. CVSL means _____
a) Complementary Voltage Switch Logic
b) Cascode Voltage Switch Logic
c) Complemented Voltage Switch Logic
d) Cascade Voltage Switch Logic

Answer: c
Explanation: Cascode Voltage Switch Logic (CVSL) refers to a CMOS-type logic family which is designed for certain advantages. It requires mainly N-channel MOSFET transistors to implement the logic using true and complementary input signals and also needs two P-channel transistors at the top to pull one of the outputs high.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Compatibility or Interfacing”.

1. Compatibility refers to _____
a) The output of a circuit should match with the input of another circuit
b) The output of a circuit should match with the input of the same circuit
c) The input of a circuit should match with the output of another circuit
d) The input of a circuit should match with the output of same circuit

Answer: a
Explanation: The output(s) of a circuit or a system should match the input(s) of another circuit or system that has different electrical characteristics. This is referred to as compatibility.

2. The method of connecting a driving device to a loading device is known as _____
a) Compatibility
b) Interface
c) Sourcing
d) Sinking

Answer: b
Explanation: The method of connecting a driving device to a loading device is known as interface. The output(s) of a circuit or a system should match the input(s) of another circuit or system that has different electrical characteristics. This is referred to as compatibility.

3. The first CML logic was introduced by General Electric in _____
a) 1960
b) 1981
c) 1961
d) 1990

Answer: c
Explanation: CML stands for Current Mode Logic. The first CML logic was introduced by General Electric in 1961.

4. Commercial ECL families are not nearly as popular as TTL and CMOS mainly because they _____
a) Produces too much noise
b) Consume too much power
c) Have high fan-in
d) Have high fan-out

Answer: b
Explanation: Commercial ECL families are not nearly as popular as TTL and CMOS mainly because they consume too much power. CMOS consumes the least power while TTL provides high speed.

5. The key to propagation delay in bipolar logic family is to prevent the transistors in a gate from _____
a) Fan-in
b) Fan-out
c) Saturation
d) Cut-off

Answer: c
Explanation: The key to propagation delay in bipolar logic family is to prevent the transistors in a gate from saturation. In Saturation mode, the transistor is in “ON”mode, where it seems like a short circuit between collector and emitter.

6. Schottky families prevent the saturating using _____
a) Transistors
b) Schottky transistors
c) Diodes
d) Schottky diodes

Answer: d
Explanation: Schottky families prevent the saturating using Schottky diodes across the base-collector junctions of transistors. In Saturation mode, the transistor is in “ON”mode, where it seems like a short circuit between collector and emitter.

7. The basic idea of basic CML circuit came from an _____
a) Inverter
b) Buffer
c) Transistor
d) Both inverter and buffer

Answer: d
Explanation: CML is Current Mode Logic in which data is transmitted at high speed of Mbps. Since this circuit has both inverting and non-inverting output. So, It behaves like an inverter/ buffer.

8. The full form of MECL is _____
a) Mono emitter coupled logic
b) Motorola emitter coupled logic
c) Motorola emitter capacitor logic

d) Both mono emitter and motorola coupled logic

Answer: b
Explanation: The full form of MECL is Motorola emitter coupled logic. ECL is a high speed BJT. It uses BJT differential amplifier with single input and restricted current to avoid the transistor going into saturation and thus turning off operation.

9. Motorola has offered MECL circuits in _____ logic families.
a) 3
b) 4
c) 5
d) 6

Answer: c
Explanation: Motorola has offered MECL circuits in five logic families: MECL I, MECL II, MECL III, MECL 10000 (MECL 10K) and MECL 10H000 (MECL 10KH). The full form of MECL is Motorola emitter coupled logic. ECL is a high speed BJT. It uses BJT differential amplifier with single input and restricted current to avoid the transistor going into saturation and thus turning off operation.

10. The latest entrant to the ECL family is _____
a) ECL 10K
b) ECL 100K
c) ECL 1000K
d) ECL 10000K

Answer: b
Explanation: The latest entrant to the ECL family is ECL 100K, having 6-digit part numbers. This family offers functions, in general, different from those offered by 10K series. This family operates with a reduced power supply voltage -4.5 V, has shorter propagation delay of 0.75 ns, and transition time of 0.7 ns. However, the power consumption per gate is about 40 mW.

11. All input of NOR as low produces result as _____
a) Low
b) Mid
c) High
d) High Impedance

Answer: c
Explanation: According to the properties of NOR gate, if all the input of NOR as low produces a result as high. While if any input of NOR is high, then it produces low output.

12. In RTL NOR gate, the output is at logic 1 only when all the inputs are at _____
a) logic 0
b) logic 1
c) +10v
d) floating

Answer: a
Explanation: RTL NOR gate behaves as NOR gate and the output of NOR gate will be 1 only when all the inputs are at logic 0. The output of NOR will be 0 if any of the input is 1.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Half Adder & Full Adder”.

1. In parts of the processor, adders are used to calculate _____
a) Addresses
b) Table indices
c) Increment and decrement operators
d) All of the Mentioned

Answer: d
Explanation: Adders are used to perform the operation of addition. Thus, in parts of the processor, adders are used to calculate addresses, table indices, increment and decrement operators, and similar operations.

2. Total number of inputs in a half adder is _____
a) 2
b) 3
c) 4
d) 1

Answer: a
Explanation: Total number of inputs in a half adder is two. Since an EXOR gates has 2 inputs and carry is connected with the input of EXOR gates. The output of half-adder is also 2, them being, SUM and CARRY. The output of EXOR gives SUM and that of AND gives carry.

3. In which operation carry is obtained?
a) Subtraction
b) Addition
c) Multiplication
d) Both addition and subtraction

Answer: b
Explanation: In addition, carry is obtained. For example: 1 0 1 + 1 1 1 = 1 0 0; in this example carry is obtained after 1st addition (i.e. 1 + 1 = 1 0). In subtraction, borrow is obtained. Like, 0 – 1 = 1 (borrow 1).

4. If A and B are the inputs of a half adder, the sum is given by _____
a) A AND B
b) A OR B
c) A XOR B
d) A EX-NOR B

Answer: c
Explanation: If A and B are the inputs of a half adder, the sum is given by A XOR B, while the carry is given by A AND B.

5. If A and B are the inputs of a half adder, the carry is given by _____
a) A AND B
b) A OR B
c) A XOR B
d) A EX-NOR B

Answer: a
Explanation: If A and B are the inputs of a half adder, the carry is given by: A(AND)B, while the sum is given by A XOR B.

6. Half-adders have a major limitation in that they cannot _____
a) Accept a carry bit from a present stage
b) Accept a carry bit from a next stage
c) Accept a carry bit from a previous stage
d) Accept a carry bit from the following stages

Answer: c
Explanation: Half-adders have a major limitation in that they cannot accept a carry bit from a previous stage, meaning that they cannot be chained together to add multi-bit numbers. However, the two output bits of a half-adder can also represent the result A+B=3 as sum and carry both being high.

7. The difference between half adder and full adder is _____
a) Half adder has two inputs while full adder has four inputs
b) Half adder has one output while full adder has two outputs
c) Half adder has two inputs while full adder has three inputs
d) All of the Mentioned

Answer: c
Explanation: Half adder has two inputs while full adder has three outputs; this is the difference between them, while both have two outputs SUM and CARRY.

8. If A, B and C are the inputs of a full adder then the sum is given by _____
a) A AND B AND C
b) A OR B AND C
c) A XOR B XOR C
d) A OR B OR C

Answer: c
Explanation: If A, B and C are the inputs of a full adder then the sum is given by A XOR B XOR C.

9. If A, B and C are the inputs of a full adder then the carry is given by _____
a) A AND B OR (A OR B) AND C
b) A OR B OR (A AND B) C
c) (A AND B) OR (A AND B)C
d) A XOR B XOR (A XOR B) AND C

Answer: a
Explanation: If A, B and C are the inputs of a full adder then the carry is given by A AND B OR (A OR B) AND C, which is equivalent to (A AND B) OR (B AND C) OR (C AND A).

10. How many AND, OR and EXOR gates are required for the configuration of full adder?
a) 1, 2, 2
b) 2, 1, 2
c) 3, 1, 2
d) 4, 0, 1

Answer: b
Explanation: There are 2 AND, 1 OR and 2 EXOR gates required for the configuration of full adder, provided using half adder. Otherwise, configuration of full adder would require 3 AND, 2 OR and 2 EXOR.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Introduction of Arithmetic Operation”.

1. The basic building blocks of the arithmetic unit in digital computers are _____
a) Subtractors
b) Adders
c) Multiplexer
d) Comparator

Answer: b
Explanation: The basic building blocks of the arithmetic unit in digital computers are adders. Since a parallel adder is constructed with a number of full-adder circuits connected in cascade. By controlling the data inputs to the parallel adder, it is possible to obtain different types of arithmetic operations.

2. A digital system consists of _____ types of circuits.
a) 2
b) 3
c) 4
d) 5

Answer: a
Explanation: A digital system consists of two types of circuits and these are a combinational and sequential logic circuit. Combinational circuits are the ones which do not depend on previous inputs while Sequential circuits depend on past inputs.

3. In a combinational circuit, the output at any time depends only on the _____ at that time.
a) Voltage
b) Intermediate values
c) Input values
d) Clock pulses

Answer: c
Explanation: In a combinational circuit, the output at any time depends only on the input values at that time and not on past or intermediate values.

4. In a sequential circuit, the output at any time depends only on the input values at that time.
a) Past output values
b) Intermediate values
c) Both past output and present input
d) Present input values

Answer: c
Explanation: In a sequential circuit, the output at any time depends on the present input values as well as past output values. It also depends on clock pulses depending on whether it's synchronous or asynchronous sequential circuits.

5. Procedure for the design of combinational circuits are:

```
A. From the word description of the problem, identify the inputs and outputs and draw a b
B. Draw the truth table such that it completely describes the operation of the circuit fo
combinations of inputs.
C. Simplify the switching expression(s) for the output(s).
D. Implement the simplified expression using logic gates.
E. Write down the switching expression(s) for the output(s).
```

a) B, C, D, E, A
b) A, D, E, B, C
c) A, B, E, C, D
d) B, A, E, C, D

Answer: c
Explanation: Combinational circuits are the ones which do not depend on previous inputs and depends only on the present values. The given arrangement A, B, E, C, D is the right sequence for the designing of the combinational circuits.

6. All logic operations can be obtained by means of _____
a) AND and NAND operations
b) OR and NOR operations
c) OR and NOT operations
d) NAND and NOR operations

Answer: d
Explanation: Since the logic gates NOR and NAND are known as universal logic gates, therefore it can be used to design all the three basic gates AND, OR and NOT. Thus, it means that any operations can be obtained by implementation of these gates.

7. The design of an ALU is based on _____
a) Sequential logic
b) Combinational logic
c) Multiplexing
d) De-Multiplexing

Answer: b
Explanation: The design of an ALU is based on combinational logic. Because the unit has a regular pattern, it can be broken into identical stages connected in cascade through carries.

8. If the two numbers are unsigned, the bit conditions of interest are the _____ carry and a possible _____ result.
a) Input, zero
b) Output, one
c) Input, one
d) Output, zero

Answer: d
Explanation: If the two numbers are unsigned, the bit conditions of interest are the output carry and a possible zero result.

9. If the two numbers include a sign bit in the highest order position, the bit conditions of interest are the sign of the result, a zero indication and _____
a) An underflow condition
b) A neutral condition
c) An overflow condition
d) One indication

Answer: c
Explanation: If the two numbers include a sign bit in the highest order position, the bit conditions of interest are the sign of the result, a zero indication and an overflow condition.

10. The flag bits in an ALU is defined as _____
a) The total number of registers
b) The status bit conditions
c) The total number of control lines
d) All of the Mentioned

Answer: b
Explanation: In an ALU, status bit conditions are sometimes called condition code bits or flag bits. It is so called because they tend to represent the status of the respect flags after any operation.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Procedure for the Design of Combinational Circuits”.

1. The basic building blocks of the arithmetic unit in a digital computers are _____
a) Subtractors
b) Adders
c) Multiplexer
d) Comparator

Answer: b
Explanation: The basic building blocks of the arithmetic unit in a digital computers are adders. Since, a parallel adder is constructed with a number of full-adder circuits connected in cascade. By controlling the data inputs to the parallel adder, it is possible to obtain different types of arithmetic operations.

2. A digital system consists of _____ types of circuits.
a) 2
b) 3
c) 4
d) 5

Answer: a
Explanation: A digital system consists of two types of circuits and these are combinational and sequential logic circuit. Combinational circuits are the ones which do not depend on previous inputs while Sequential circuits depend on past inputs.

3. In a combinational circuit, the output at any time depends only on the _____ at that time.
a) Voltage
b) Intermediate values
c) Input values
d) Clock pulses

Answer: c
Explanation: In a combinational circuit, the output at any time depends only on the input values at that time and not on past or intermediate values.

4. In a sequential circuit, the output at any time depends only on the input values at that time.
a) Past output values
b) Intermediate values
c) Both past output and present input
d) Present input values

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A. From the word description of the problem, identify the inputs and outputs and draw a b
B. Draw the truth table such that it completely describes the operation of the circuit fo
combinations of inputs.
C. Simplify the switching expression(s) for the output(s).
D. Implement the simplified expression using logic gates.
E. Write down the switching expression(s) for the output(s).

a) B, C, D, E, A
b) A, D, E, B, C
c) A, B, E, C, D
d) B, A, E, C, D

Answer: c
Explanation: Combinational circuits are the ones which do not depend on previous inputs and depends only on the present values. The given arrangement in option c is the right sequence for the designing of the combinational circuits.

6. All logic operations can be obtained by means of _____
a) AND and NAND operations
b) OR and NOR operations
c) OR and NOT operations
d) NAND and NOR operations

Answer: d
Explanation: Since, the logic gates NOR and NAND are known as universal logic gates, therefore it can be used to design all the three basic gates AND, OR and NOT. Thus, it means that any operations can be obtained by implementation of these gates.

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d) De-Multiplexing

Answer: b
Explanation: The design of an ALU is based on combinational logic. Because the unit has a regular pattern, it can be broken into identical stages connected in cascade through carries.

8. If the two numbers are unsigned, the bit conditions of interest are the _____ carry and a possible _____ result.
a) Input, zero
b) Output, one
c) Input, one
d) Output, zero

Answer: d
Explanation: If the two numbers are unsigned, the bit conditions of interest are the output carry and a possible zero result.

9. If the two numbers include a sign bit in the highest order position, the bit conditions of interest are the sign of the result, a zero indication and _____
a) An underflow condition
b) A neutral condition
c) An overflow condition
d) One indication

Answer: c
Explanation: If the two numbers include a sign bit in the highest order position, the bit conditions of interest are the sign of the result, a zero indication and an overflow condition.

10. The flag bits in an ALU is defined as _____
a) The total number of registers
b) The status bit conditions
c) The total number of control lines
d) All of the Mentioned

Answer: b
Explanation: In an ALU, status bit conditions are sometimes called condition code bits or flag bits. It is so called because they tend to represent the status of the respect flags after any operation.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Half & Full Subtractor”.

1. Half subtractor is used to perform subtraction of _____
a) 2 bits
b) 3 bits
c) 4 bits
d) 5 bits

Answer: a
Explanation: Half subtractor is a combinational circuit which is used to perform subtraction of two bits, namely minuend and subtrahend and produces two outputs, borrow and difference.

2. For subtracting 1 from 0, we use to take a _____ from neighbouring bits.
a) Carry
b) Borrow
c) Input
d) Output

Answer: b
Explanation: For subtracting 1 from 0, we use to take a borrow from neighbouring bits because carry is taken into consideration during addition process.

3. How many outputs are required for the implementation of a subtractor?
a) 1
b) 2
c) 3
d) 4

Answer: b
Explanation: There are two outputs required for the implementation of a subtractor. One for the difference and another for borrow.

4. Let the input of a subtractor is A and B then what the output will be if A = B?
a) 0
b) 1
c) A
d) B

Answer: a
Explanation: The output for A = B will be 0. If A = B, it means that A = B = 0 or A = B = 1. In both of the situation subtractor gives 0 as the output.

5. Let A and B is the input of a subtractor then the output will be _____
a) A XOR B
b) A AND B
c) A OR B
d) A EXNOR B

Answer: a
Explanation: The subtractor has two outputs BORROW and DIFFERENCE. Since the difference

output of a subtractor is given by AB’ + BA’ and this is the output of a XOR gate. So, the final difference output is AB’ + BA’.

6. Let A and B is the input of a subtractor then the borrow will be _____
a) A AND B’
b) A’ AND B
c) A OR B
d) A AND B

Answer: b
Explanation: The borrow of a subtractor is received through AND gate whose one input is inverted. On that basis the borrow will be (A’ AND B).

7. What does minuend and subtrahend denotes in a subtractor?
a) Their corresponding bits of input
b) Its outputs
c) Its inputs
d) Borrow bits

Answer: c
Explanation: Minuend and subtrahend are the two bits of input of a subtractor. If A and B are the two inputs of a subtractor then A is called minuend and B as subtrahend.

8. Full subtractor is used to perform subtraction of _____
a) 2 bits
b) 3 bits
c) 4 bits
d) 8 bits

Answer: b
Explanation: Full subtractor is used to perform subtraction of 3 bits, namely minuend bit, subtrahend bit and borrow from the previous stage. However, it also produces 2 outputs BORROW and DIFFERENCE.

9. The full subtractor can be implemented using _____
a) Two XOR and an OR gates
b) Two half subtractors and an OR gate
c) Two multiplexers and an AND gate
d) Two comparators and an AND gate

Answer: b
Explanation: A full subtractor has 3 input bits and two outputs bits BORROW and DIFFERENCE. The full subtractor can be implemented using two half subtractors and an OR gate.

10. The output of a subtractor is given by (if A, B and X are the inputs).
a) A AND B XOR X
b) A XOR B XOR X
c) A OR B NOR X
d) A NOR B XOR X

Answer: b
Explanation: The difference output of a subtractor is given by (if A, B and X are the inputs) A XOR B XOR X.

11. The output of a full subtractor is same as _____
a) Half adder
b) Full adder
c) Half subtractor
d) Decoder

Answer: b
Explanation: The sum and difference output of a full adder and a full subtractor are same. If A, B and C are the input of a full adder and a full subtractor then the output will be given by (A XOR B XOR C), respectively.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “K-Map Simplification”.

1. Which statement below best describes a Karnaugh map?
a) It is simply a rearranged truth table
b) The Karnaugh map eliminates the need for using NAND and NOR gates
c) Variable complements can be eliminated by using Karnaugh maps
d) A Karnaugh map can be used to replace Boolean rules

Answer: a
Explanation: K-map is simply a rearranged truth table. It is a pictorial representation of truth table having a specific number of cells or squares, where each cell represents a Maxterm or a Minterm.

2. Which of the examples below expresses the commutative law of multiplication?
a) A + B = B + A
b) A • B = B + A
c) A • (B • C) = (A • B) • C
d) A • B = B • A

Answer: d
Explanation: The commutative law of multiplication is (A * B) = (B * A).
The commutative law of addition is (A + B) = (B + A).

3. The Boolean expression Y = (AB)’ is logically equivalent to what single gate?
a) NAND
b) NOR
c) AND
d) OR

Answer: a
Explanation: If A and B are the input for AND gate the output is obtained as AB and after inversion we get (AB)’, which is the expression of NAND gate. NAND gate produces high output when any of the input is 0 and produces low output when all inputs are 1.

4. The observation that a bubbled input OR gate is interchangeable with a bubbled output AND gate is referred to as _____
a) A Karnaugh map
b) DeMorgan’s second theorem
c) The commutative law of addition
d) The associative law of multiplication

Answer: b
Explanation: DeMorgan’s Law: ~(P+Q) <=> (~P).(~Q) Also,
~(P.Q) <=> (~P)+(~Q).

5. The systematic reduction of logic circuits is accomplished by _____
a) Symbolic reduction
b) TTL logic
c) Using Boolean algebra
d) Using a truth table

Answer: c
Explanation: The systematic reduction of logic circuits is accomplished by using boolean algebra.

6. Each “1” entry in a K-map square represents _____
a) A HIGH for each input truth table condition that produces a HIGH output
b) A HIGH output on the truth table for all LOW input combinations
c) A LOW output for all possible HIGH input conditions
d) A DON’T CARE condition for all possible input truth table combinations

Answer: a
Explanation: Each “1” entry in a K-map square represents a HIGH for each input truth table condition that produces a HIGH output. Thus, it represents a minterm.

7. Each “0” entry in a K-map square represents _____
a) A HIGH for each input truth table condition that produces a HIGH output
b) A HIGH output on the truth table for all LOW input combinations
c) A LOW output for all possible HIGH input conditions
d) A DON’T CARE condition for all possible input truth table combinations

Answer: a
Explanation: Each “0” entry in a K-map square represents a LOW output for all possible HIGH input conditions. Thus, it represents Maxterm.

8. Which of the following statements accurately represents the two BEST methods of logic circuit simplification?
a) Actual circuit trial and error evaluation and waveform analysis
b) Karnaugh mapping and circuit waveform analysis
c) Boolean algebra and Karnaugh mapping
d) Boolean algebra and actual circuit trial and error evaluation

Answer: c
Explanation: The two BEST methods of logic circuit simplification are Boolean algebra and Karnaugh mapping. Boolean Algebra uses the Laws of Boolean Algebra for minimization of Boolean expressions while Karnaugh Map is a pictorial representation and reduction of the Boolean expression.

9. Looping on a K-map always results in the elimination of _____
a) Variables within the loop that appear only in their complemented form
b) Variables that remain unchanged within the loop
c) Variables within the loop that appear in both complemented and uncomplemented form
d) Variables within the loop that appear only in their uncomplemented form

Answer: c
Explanation: Looping on a K-map always results in the elimination of variables within the loop that appear in both complemented and uncomplemented form.

10. Which of the following expressions is in the sum-of-products form?
a) (A + B)(C + D)
b) (A * B)(C * D)
c) A* B *(CD)
d) A * B + C * D

Answer: d
Explanation: Sum of product means that it is the sum of all product terms. Thus, the number is multiplied first and then it is added: A * B + C * D.

11. Which of the following is an important feature of the sum-of-products form of expressions?
a) All logic circuits are reduced to nothing more than simple AND and OR operations
b) The delay times are greatly reduced over other forms
c) No signal must pass through more than two gates, not including inverters
d) The maximum number of gates that any signal must pass through is reduced by a factor of two

Answer: a
Explanation: An important feature of the sum-of-products form of expressions in the given option is that all logic circuits are reduced to nothing more than simple AND and OR operations. Sum Of Product means it is the sum of product terms containing variables in complemented as well as uncomplemented forms.

12. Which of the following expressions is in the product-of-sums form?
a) (A + B)(C + D)
b) (AB)(CD)
c) AB(CD)
d) AB + CD

Answer: a
Explanation: (A + B)(C + D) represents the product-of-sums form.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Controlled Inverter”.

1. Controlled inverter is also known as _____
a) Controlled buffer
b) NOT gate
c) Both controlled buffer and NOT gate
d) Controlled gate

Answer: c
Explanation: Controlled inverter is also known as controlled buffer and NOT gate as well. It is used between output and a bus so that one can control whether the output is fed to the bus or not.

2. Why XOR gate is called an inverter?
a) Because of the same input
b) Because of the same output
c) It behaves like a NOT gate
d) It behaves like a AND gate

Answer: c
Explanation: The XOR (Exclusive Or) gate has a true output when the two inputs are different. When one input is true, the output is the inversion of the other. When one input is false, the output is the non-inversion of the other.

3. Controlled buffers can be useful _____
a) To control the circuit’s output into the bus
b) In comparison of component’s output with its input
c) In increasing the output from its low input
d) All of the Mentioned

Answer: a
Explanation: Controlled buffers can be useful when you have a wire (often called a bus) whose value should match the output of one of several components. By placing a controlled buffer between each component output and the bus, you can control whether that component’s output is fed onto the bus or not.

4. A logic circuit that provides a HIGH output for both inputs HIGH or both inputs LOW is _____
a) Ex-NOR gate
b) OR gate
c) Ex-OR gate
d) NAND gate

Answer: a
Explanation: EX-OR gate gives 1 if both inputs are different means 0 or 1 and gives 0 if both are same and EX-NOR is opposite of EX-OR gate, so it provides a HIGH output for both inputs HIGH or both inputs are LOW. Thus, EX-NOR produces output for even number of 1’s or all 0s, while EXOR produces output for odd number of 1’s.

5. What is the first thing you will need if you are going to use a macro-function?
a) A complicated design project
b) An experienced design engineer
c) Good documentation
d) Experience in HDL

Answer: d
Explanation: HDL stands for Hardware Description Language. In order to use a macro function, one needs to have experience in HDL for representing the structure and behaviour of digital circuits.

6. What is the major difference between half-adders and full-adders?
a) Full-adders are made up of two half-adders
b) Full adders can handle double-digit numbers
c) Full adders have a carry input capability

d) Half adders can handle only single-digit numbers

Answer: c
Explanation: Half adders have only two inputs A and B. When we add two 4 bit binary number like 0001 and 0011, then half adder can not be used because if the first bit of both the numbers is 1, then the sum would be 0 and carry would be 1. But this carry can not be added with the second bits addition of the number. So, half adders are useless. But in full adders, one more carry input is present, so that, if carry of one stage is present, it can be added with the next stage as it is done in normal addition. So, therefore, full adders have a carry input capability.

7. The binary subtraction of 0 – 0 = ?
a) Difference = 0, borrow = 0
b) Difference = 1, borrow = 0
c) Difference = 1, borrow = 1
d) Difference = 0, borrow = 1

Answer: a
Explanation: The binary subtraction of 0 – 0 = 0. Thus, it’s difference is 0 as well as it’s borrow.

8. How many basic binary subtraction operations are possible?
a) 1
b) 4
c) 3
d) 2

Answer: b
Explanation: 4 basic binary subtraction operations (0-0, 1-0, 0-1, 1-1) are possible.
0 – 0 = 0
0 – 1 = 1 (Borrow 1)
1 – 0 = 1
1 – 1 = 0

9. When performing subtraction by addition in the 2’s-complement system is?
a) The minuend and the subtrahend are both changed to the 2’s-complement
b) The minuend is changed to 2’s-complement and the subtrahend is left in its original form
c) The minuend is left in its original form and the subtrahend is changed to its 2’s-complement
d) The minuend and subtrahend are both left in their original form

Answer: c
Explanation: When performing subtraction by addition in the 2’s-complement system, the minuend is left in its original form and the subtrahend is changed to its 2’s-complement. It is then added to the minuend. If the result has carry, then it’s dropped and that’s the final answer. Else, if the result has no carry, then the result is again converted to it’s 2’s complement form and that’s the final answer with a ‘negative’ sign.

10. What are the two types of basic adder circuits?
a) Sum and carry
b) Half-adder and full-adder
c) Asynchronous and synchronous
d) One and two’s-complement

Answer: b
Explanation: There are two types of adder circuits: half-adder and full-adder. Half-Adder has 2 inputs while Full-Adder has 3 inputs. Whereas, both have two outputs SUM and CARRY.

11. Which of the following is correct for full adders?
a) Full adders have the capability of directly adding decimal numbers
b) Full adders are used to make half adders
c) Full adders are limited to two inputs since there are only two binary digits
d) In a parallel full adder, the first stage may be a half adder

Answer: d
Explanation: By using maximum of two half adders we can make a full adder for the first stage of a Parallel Full adder.

12. The selector inputs to an arithmetic/logic unit (ALU) determine the _____
a) Selection of the IC
b) Arithmetic or logic function
c) Data word selection
d) Clock frequency to be used

Answer: b
Explanation: An ALU performs basic arithmetic and logic operations and stores it in the accumulator. Examples of arithmetic operations are addition, subtraction, multiplication, and division. Examples of logic operations are comparisons of values such as NOT, AND and OR and any logical operations.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “4-Bit Parallel Adder/Subtractor – 1”.

1. Controlled inverter is also known as _____
a) Controlled buffer
b) NOT gate
c) Both controlled buffer and NOT gate
d) Controlled gate

Answer: c
Explanation: Controlled inverter is also known as controlled buffer and NOT gate as well. It is used between output and a bus so that one can control whether the output is fed to the bus or not.

2. Why XOR gate is called an inverter?
a) Because of the same input
b) Because of the same output
c) It behaves like a NOT gate
d) It behaves like a AND gate

Answer: c
Explanation: The XOR (Exclusive Or) gate has a true output when the two inputs are different. When one input is true, the output is the inversion of the other. When one input is false, the output is the non-inversion of the other.

3. Controlled buffers can be useful _____
a) To control the circuit’s output into the bus
b) In comparison of component’s output with its input
c) In increasing the output from its low input
d) All of the Mentioned

Answer: a
Explanation: Controlled buffers can be useful when you have a wire (often called a bus) whose value should match the output of one of several components. By placing a controlled buffer between each component output and the bus, you can control whether that component’s output is fed onto the bus or not.

4. A logic circuit that provides a HIGH output for both inputs HIGH or both inputs LOW is _____
a) Ex-NOR gate
b) OR gate
c) Ex-OR gate
d) NAND gate

Answer: a
Explanation: EX-OR gate gives 1 if both inputs are different means 0 or 1 and gives 0 if both are same and EX-NOR is opposite of EX-OR gate, so it provides a HIGH output for both inputs HIGH or both inputs are LOW. Thus, EX-NOR produces output for even number of 1’s or all 0s, while EXOR produces output for odd number of 1’s.

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b) An experienced design engineer

c) Good documentation
d) Experience in HDL

Answer: d
Explanation: HDL stands for Hardware Description Language. In order to use a macro function, one needs to have experience in HDL for representing the structure and behaviour of digital circuits.

6. What is the major difference between half-adders and full-adders?
a) Full-adders are made up of two half-adders
b) Full adders can handle double-digit numbers
c) Full adders have a carry input capability
d) Half adders can handle only single-digit numbers

Answer: c
Explanation: Half adders have only two inputs A and B. When we add two 4 bit binary number like 0001 and 0011, then half adder can not be used because if the first bit of both the numbers is 1, then the sum would be 0 and carry would be 1. But this carry can not be added with the second bits addition of the number. So, half adders are useless. But in full adders, one more carry input is present, so that, if carry of one stage is present, it can be added with the next stage as it is done in normal addition. So, therefore, full adders have a carry input capability.

7. The binary subtraction of 0 – 0 =?
a) Difference = 0, borrow = 0
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Explanation: The binary subtraction of 0 – 0 = 0. Thus, it’s difference is 0 as well as it’s borrow.

8. How many basic binary subtraction operations are possible?
a) 1
b) 4
c) 3
d) 2

Answer: b
Explanation: 4 basic binary subtraction operations (0-0, 1-0, 0-1, 1-1) are possible.
0 – 0 = 0
0 – 1 = 1 (Borrow 1)
1 – 0 = 1
1 – 1 = 0

9. When performing subtraction by addition in the 2’s-complement system _____
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c) The minuend is left in its original form and the subtrahend is changed to its 2’s-complement
d) The minuend and subtrahend are both left in their original form

Answer: c
Explanation: When performing subtraction by addition in the 2’s-complement system, the minuend is left in its original form and the subtrahend is changed to its 2’s-complement. It is then added to the minuend. If the result has carry, then it’s dropped and that’s the final answer. Else, if the result has no carry, then the result is again converted to it’s 2’s complement form and that’s the final answer with a ‘negative’ sign.

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c) Asynchronous and synchronous
d) One and two’s-complement

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Explanation: There are two types of adder circuits: half-adder and full-adder. Half-Adder has 2 inputs while Full-Adder has 3 inputs. Whereas, both have two outputs SUM and CARRY.

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b) Full adders are used to make half adders
c) Full adders are limited to two inputs since there are only two binary digits
d) In a parallel full adder, the first stage may be a half adder

Answer: d
Explanation: By using maximum of two half adders we can make a full adder for the first stage of a Parallel Full adder.

12. The selector inputs to an arithmetic/logic unit (ALU) determine the _____
a) Selection of the IC
b) Arithmetic or logic function
c) Data word selection
d) Clock frequency to be used

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Explanation: An ALU performs basic arithmetic and logic operations and stores it in the accumulator. Examples of arithmetic operations are addition, subtraction, multiplication, and division. Examples of logic operations are comparisons of values such as NOT, AND and OR and any logical operations.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Fast Adder & Serial Adder – 1”.

1. The inverter can be produced with how many NAND gates?
a) 2
b) 1
c) 3
d) 4

Answer: b
Explanation: The inverter can be produced with the help of single NAND gate, because we can send a single input twice through the same NAND gate together, thus producing the inverted version of the input as output. It works as an inverter.

2. One positive pulse with tw = 75 µs is applied to one of the inputs of an exclusive-OR circuit. A second positive pulse with tw = 15 µs is applied to the other input beginning 20 µs after the leading edge of the first pulse. Which statement describes the output’s relation with the inputs?

a) The exclusive-OR output is a 20 s pulse followed by a 40 s pulse, with a separation of 15 s between the pulses
b) The exclusive-OR output is a 20 s pulse followed by a 15 s pulse, with a separation of 40 s between the pulses
c) The exclusive-OR output is a 15 s pulse followed by a 40 s pulse
d) The exclusive-OR output is a 20 s pulse followed by a 15 s pulse, followed by a 40 s pulse

Answer: d
Explanation: When both the input pulses are high or low X-OR output is low. But when one of the input is high and another is low or vice-versa, output is high. In this problem for the first 20uS one input is high and another is low. So, obviously output is a high. for next 15uS both the input is high so output is low and for remaining 40uS(75-20-15) first input is still high and second one is low so output is high.

3. How many NOT gates are required to implement the Boolean expression: X = AB’C + A’BC?
a) 2
b) 3
c) 4
d) 5

Answer: a
Explanation: Since in the given expression two inputs are complemented. So, we require two NOT gate at the input. A NOT gate is a basic gate which accepts a single input and produces a single output, which is the inverted version of the input.

4. The carry look ahead adder is based on the principle of looking at the lower order bits of _____ and _____ if a high order carry is generated.
a) Addend, minuend
b) Minuend, subtrahend
c) Addend, minuend
d) Augend, addend

Answer: d
Explanation: The carry look ahead adder is based on the principle of looking at the lower order bits of the augend and addend if a high order carry is generated. A carry look ahead adder is a type of adder which reduces the propagation delay.

5. What are carry generate combinations?
a) If all the input are same then a carry is generated
b) If all of the output are independent of the inputs
c) If all of the input are dependent on the output
d) If all of the output are dependent on the input

Answer: b
Explanation: If the input is either 0, 0, 0 or 0, 0, 1 then the output will be 0 (i.e. independent of input) and if the input is either 1, 1, 0 or 1, 1, 1 then the output is 1 (i.e independent of input). Such situation is known as carry generate combinations.

6. In serial addition, the addition is carried out _____
a) 3 bit per second
b) Byte by byte
c) Bit by bit
d) All bits at the same time

Answer: c
Explanation: In serial addition, the addition is carried out bit by bit.

7. How many shift registers are used in a 4 bit serial adder?
a) 4
b) 3
c) 2
d) 5

Answer: c
Explanation: There are two shift registers are used in a 4-bit serial adder, which is used to store the numbers to be added serially. Serial addition takes place bit by bit.

8. A D flip-flop is used in a 4-bit serial adder, why?
a) It is used to invert the input of the full adder
b) It is used to store the output of the full adder
c) It is used to store the carry output of the full adder
d) It is used to store the sum output of the full adder

Answer: c
Explanation: The D flip-flop, i.e. carry flip-flop, is used to store the carry output of the full adder so that it can be added to the next significant position of the numbers in the registers.

9. What is ripple carry adder?
a) The carry output of the lower order stage is connected to the carry input of the next higher order stage
b) The carry input of the lower order stage is connected to the carry output of the next higher order stage
c) The carry output of the higher order stage is connected to the carry input of the next lower order stage
d) The carry input of the higher order stage is connected to the carry output of the lower order

stage

Answer: a
Explanation: When the carry output of the lower order stage is connected to the carry input of the next higher order stage, such types of connection is called ripple carry adder in a 4-bit binary parallel adder.

10. If minuend = 0, subtrahend = 1 and borrow input = 1 in a full subtractor then the borrow output will be _____
a) 0
b) 1
c) Floating
d) High Impedance

Answer: b
Explanation: If minuend = 0, subtrahend = 1 and borrow input = 1 in a full subtractor then the borrow output will be 1. Because on subtracting 0 and 1, one borrow is taken and it proceeds till the next step (i.e 0 – 1 – 1 = 0, borrow = 1).

This set of Digital Electronic/Circuits Test focuses on “4-Bit Parallel Adder/Subtractor – 2”.

1. For a 4-bit parallel adder, if the carry-in is connected to a logical HIGH, the result is _____
a) The same as if the carry-in is tied LOW since the least significant carry-in is ignored
b) That carry-out will always be HIGH
c) A one will be added to the final result
d) The carry-out is ignored

Answer: c
Explanation: For a 4-bit parallel adder, if the carry-in is connected to a logical HIGH, one will be added to the final result as a result because carry-in gives output as 1.

2. Fast-look-ahead carry circuits found in most 4-bit full-adder circuits which _____
a) Determine sign and magnitude
b) Reduce propagation delay
c) Add a 1 to complemented inputs
d) Increase ripple delay

Answer: b
Explanation: A carry-lookahead adder (CLA) is a type of adder used in digital logic. A carry-lookahead adder improves speed by reducing the amount of time required to determine carry bits. It reduces the propagation delay by making the hardware more complex. The ripple carry design is converted in such a way that carry over a group of bits of the adder becomes 2-level logic.

3. One way to make a four-bit adder to perform subtraction is by _____
a) Inverting the output
b) Inverting the carry-in
c) Inverting the B inputs
d) Grounding the B inputs

Answer: c
Explanation: A adder is a digital circuit which adds bits along with a carry bit from a previous stage, thus producing 2 outputs SUM and CARRY. Since, a four bit adder has four A, four B and a carry at the input end. So, for subtraction to be performed, all the Bs terminal should be inverted.

4. What distinguishes the look-ahead-carry adder?
a) It is slower than the ripple-carry adder
b) It is easier to implement logically than a full adder
c) It is faster than a ripple-carry adder
d) It requires advance knowledge of the final answer

Answer: c
Explanation: It is faster than ripple carry adder as it reduces the propagation delay by

converting the ripple carry in such a way that the carry over a group of bits of the adder becomes 2-level logic.

5. Carry lookahead logic uses the concepts of _____
a) Inverting the inputs
b) Complementing the outputs
c) Generating and propagating carries
d) Ripple factor

Answer: c
Explanation: Look Ahead Carry Adder is a type of digital circuit which reduces the propagation delay. Carry lookahead logic uses the concepts of generating and propagating carries. Although in the context of a carry lookahead adder, it is most natural to think of generating and propagating in the context of binary addition, the concepts can be used more generally than this.

6. What is one disadvantage of the ripple-carry adder?
a) The interconnections are more complex
b) More stages are required to a full adder
c) It is slow due to propagation time
d) All of the Mentioned

Answer: c
Explanation: The main disadvantage in using this type of adders is that the time delay increases as for each adder to add the carry should be generated in the previous adder, and for that to add the carry from the one before is required. However, this disadvantage is taken care of in Carry Look Ahead adder in which the ripple carry is converted in such a way that the carry over a group of bits of the adder becomes 2-level logic.

7. The carry propagation delay in 4-bit full-adder circuits _____
a) Is cumulative for each stage and limits the speed at which arithmetic operations are performed
b) Is normally not a consideration because the delays are usually in the nanosecond range
c) Decreases in direct ratio to the total number of full-adder stages
d) Increases in direct ratio to the total number of full-adder stages but is not a factor in limiting the speed of arithmetic operations

Answer: a
Explanation: A full adder is a digital circuit with 3 inputs and two outputs SUM and CARRY. The carry propagation delay in 4-bit full-adder circuits is cumulative for each stage and limits the speed at which arithmetic operations are performed.

8. What is Manchester carry chain?
a) Is a chain of controlled inverter
b) Variation of a carry-lookahead adder
c) Variation of a full-adder
d) Variation of a ripple carry adder

Answer: b
Explanation: The Manchester carry chain is a variation of the carry-lookahead adder that uses shared logic to lower the transistor count. However, the carry generating logic depends on the logic to generate the carries in the past.

9. The main disadvantage of Manchester carry chain is _____
a) Ripple factor
b) Propagation delay
c) Capacitive load
d) Both propagation delay and capacitive load

Answer: d
Explanation: Propagation delay is the measure of time taken by the output to go to the next state when the input is altered. One of the major downsides of the Manchester carry chain is that the capacitive load of all of these outputs, together with the resistance of the transistors causes the propagation delay to increase much more quickly than a regular carry lookahead.

10. The summing outputs of a half or full-adder are designated by which Greek symbol?
a) Omega
b) Theta
c) Lambda
d) Sigma

Answer: d
Explanation: The summing outputs of a half or full-adder are designated by “sigma” which is a Greek symbol. This same symbol is used to signify the Minterms in case of an SOP expression.

11. Why is a fast-look-ahead carry circuit used in the 7483 4-bit full-adder?
a) To decrease the cost
b) To make it smaller
c) To slow down the circuit
d) To speed up the circuit

Answer: d
Explanation: A Carry Look Ahead (CLA) Adder is a type of adder that reduce the propagation delay. A fast Carry Look Ahead Adder is more fast than a normal CLA. Since, it is easy to implement and can be implemented on any types of chip and have the capability to reduce propagation delay, which helps in increasing the speed of 7483 4-bit full-adder.

This set of Digital Electronic/Circuits Quiz focuses on “Fast Adder & Serial Adder – 2”.

1. A serial subtractor can be obtained by converting the serial adder by using the _____

a) 1’s complement system
b) 2’s complement system
c) 10’s complement
d) 9’s complement

Answer: b
Explanation: A serial subtractor can be obtained by converting the serial adder by using the 2’s complement system. 9’s complement and 10’s complement are used for decimal numbers while adders deal with binary numbers.

2. The hexadecimal number (4B)16 is transmitted as an 8-bit word in parallel. What is the time required for this transmission if the clock frequency is 2.25 MHz?
a) 444 ns
b) 444 s
c) 3.55 s
d) 3.55 ms

Answer: a
Explanation: Because the clock pulse of 4-bit transmits the data of 8-bit word in parallel mode and this transmission is done at 2.25 MHz frequency. We know that: f=1/t and we can find the time required for this transmission by the clock pulse.
Therefore, time = (1/2.25) = 0.4444 us = 444.44 ns ~ 444ns.

3. Internally, a computer’s binary data are always transmitted on parallel channels which is commonly referred to as the _____
a) Parallel bus
b) Serial bus
c) Data bus
d) Memory bus

Answer: c
Explanation: A process consists of 3 types of buses: Control Bus, Data Bus and Address Bus. A computer’s data is always in the binary form which is stored in the bus that transmits the data on any channels. It doesn’t matter that it’s in parallel or serial.

4. What is the frequency of a clock waveform if the period of that waveform is 1.25sec?
a) 8 kHz
b) 0.8 kHz
c) 0.8 MHz

d) 8 MHz

Answer: c
Explanation: By using the formula of frequency, we can find the frequency of clock waveform.
Time period(t) of the waveform is = 1.25microseconds
f=1/t
Where ‘t’ is the time taken by the clock waveform;
f=(1/1.25)
so, f=0.8 MHz.

5. Why is parallel data transmission preferred over serial data transmission for most applications?
a) It is much slower
b) It is cheaper
c) More people use it
d) It is much faster

Answer: d
Explanation: Parallel data transmission preferred over serial data transmission for most applications because it is much faster as bits are transmitted simultaneously, whereas in serial data transmission, bits are transmitted one by one.

6. With surface-mount technology (SMT), the devices should _____
a) Utilize transistor outline connections
b) Mount directly
c) Have parallel connecting pins
d) Require holes and pads

Answer: b
Explanation: Surface-mount technology (SMT) is a method for producing electronic circuits in which the components are mounted or placed directly onto the surface of printed circuit boards (PCBs). An electronic device so made is called a surface-mount device (SMD). In the industry, it has largely replaced the through-hole technology construction method of fitting components with wire leads into holes in the circuit board. Both technologies can be used on the same board for components not suited to surface mounting such as large transformers and heat-sinked power semiconductors.

7. In most applications, transistor switches used in place of relays?
a) They consume less power
b) They are faster
c) They are quieter and smaller
d) All of the Mentioned

Answer: d
Explanation: Transistors are of less consuming power, faster, quieter, smaller and its implementation is too easy. So, in most applications transistor switches are more preferred. And also, transistors can be current-controlled or voltage-controlled depending on our choice.

8. What can a relay provide between the triggering source and the output that semiconductor switching devices cannot?
a) Total isolation
b) Faster
c) Higher current rating
d) Total isolation and higher current rating

Answer: d
Explanation: A relay provides total isolation and higher current rating between the triggering source and the output that semiconductor switching devices cannot provide. This is why relays are used to drive high watt appliances at offices or other buildings.

9. The serial format for transmitting binary information uses _____
a) A single conductor
b) Multiple conductors
c) Infrared technology
d) Fiber-optic

Answer: a
Explanation: A conductor accepts the whole data and arranges it in a serial manner, which is transmitted as binary information. In serial transmission, data is transmitted bit by bit while in parallel transmission data is transmitted simultaneously.

10. Serial communication can be sped up by _____
a) Using silver or gold conductors instead of copper
b) Using high-speed clock signals
c) Adjusting the duty cycle of the binary information
d) Using silver or gold conductors instead of copper and high-speed clock signals

Answer: b
Explanation: For any serial data transmission there is required of continuously data supply and if the input supply (i.e. high speed clock signals) in a high amount the speed of serial communication can be increased. In serial communication, data is transmitted bit by bit. So the use of high speed clock pulses would make the process faster.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “BCD Adder”.

1. The decimal number system represents the decimal number in the form of _____
a) Hexadecimal
b) Binary coded
c) Octal
d) Decimal

Answer: b
Explanation: Binary-coded decimal (BCD) is a class of binary encodings of decimal numbers where each decimal digit is represented by a fixed number of bits, usually four or eight. Hexadecimal and Octal are number systems having base 16 and 8 respectively.

2. 2^9 input circuit will have total of _____
a) 32 entries
b) 128 entries
c) 256 entries
d) 512 entries

Answer: d
Explanation: 2^9 input circuit would have 512(2*2*2*2*2*2*2*2*2 = 512) entries.

3. BCD adder can be constructed with 3 IC packages each of _____
a) 2 bits
b) 3 bits
c) 4 bits
d) 5 bits

Answer: c
Explanation: Binary-coded decimal (BCD) is a class of binary encodings of decimal numbers where each decimal digit is represented by a fixed number of bits, usually four or eight. BCD adder can be constructed with 3 IC packages. Each of 4-bit adders is an MSI(Medium scale Integration) function and 3 gates for the correction logic need one SSI (Small Scale Integration) package.

4. The output sum of two decimal digits can be represented in _____
a) Gray Code
b) Excess-3
c) BCD
d) Hexadecimal

Answer: c
Explanation: The output sum of two decimal digits can be represented in BCD(Binary-coded decimal). Binary-coded decimal (BCD) is a class of binary encodings of decimal numbers where each decimal digit is represented by a fixed number of bits, usually four or eight.

5. The addition of two decimal digits in BCD can be done through _____
a) BCD adder
b) Full adder
c) Ripple carry adder
d) Carry look ahead

Answer: a
Explanation: The addition of two decimal digits in BCD can be done through BCD adder. Every input inserted, in addition by the user converted into binary and then proceed for the addition. Whereas, Full Adder, Ripple Carry Adder and Carry Look Adder are for the addition of binary bits.

6. 3 bits full adder contains _____
a) 3 combinational inputs
b) 4 combinational inputs
c) 6 combinational inputs
d) 8 combinational inputs

Answer: d
Explanation: 3 bits full adder contains $2^3 = 8$ combinational inputs.

7. The simplified expression of full adder carry is _____
a) c = xy+xz+yz
b) c = xy+xz
c) c = xy+yz
d) c = x+y+z

Answer: a
Explanation: A full adder is a combinational circuit having 3 inputs and 2 outputs, namely SUM and CARRY. The simplified expression of full adder carry is c = xy+xz+yz.

8. Complement of F' gives back _____
a) F'
b) F
c) FF
d) FF'

Answer: b
Explanation: Complement means inversion. So, complement of F' gives back F, as per the Law of Involution.

9. Decimal digit in BCD can be represented by _____
a) 1 input line
b) 2 input lines
c) 3 input lines
d) 4 input lines

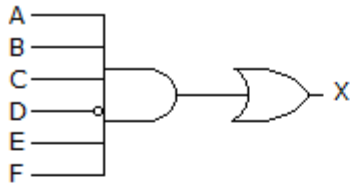
Answer: d
Explanation: Binary-coded decimal (BCD) is a class of binary encodings of decimal numbers where each decimal digit is represented by a fixed number of bits, usually four or eight. Decimal digit in BCD can be represented by 4 input lines. Since it is constructed with 4-bits.

10. The number of logic gates and the way of their interconnections can be classified as _____
a) Logical network
b) System network
c) Circuit network
d) Gate network

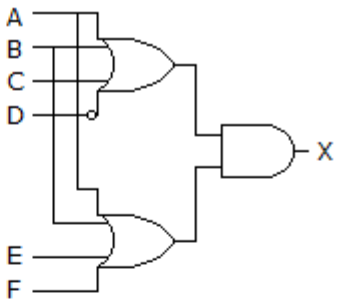
Answer: a
Explanation: The number of different levels of logic gates is represented in a fashion which is known as a logical network.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on "Combinational Circuits".

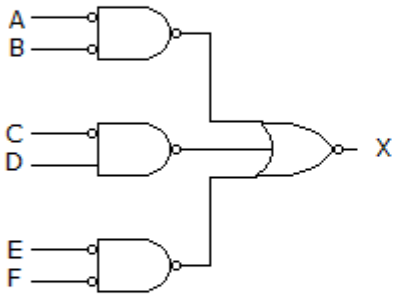
1. Which of the circuits in figure (a to d) is the sum-of-products implementation of figure (e)?



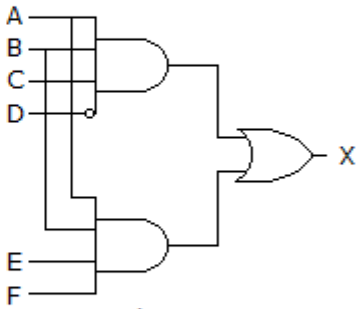
a.



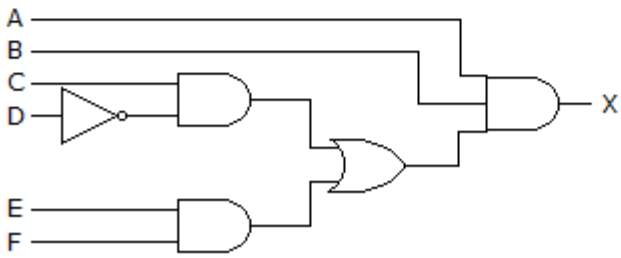
b.



c.



d.

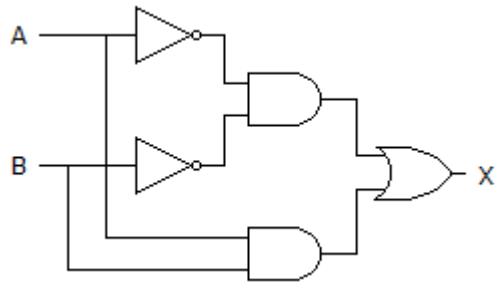


e.

a) a
b) b
c) c
d) d

Answer: d
Explanation: SOP means Sum Of Products form which represents the sum of product terms having variables in complemented as well as in uncomplemented form. Here, the diagram of d contains the OR gate followed by the AND gates, so it is in SOP form.

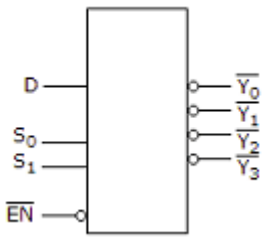
2. Which of the following logic expressions represents the logic diagram shown?



a) X=AB’+A’B
b) X=(AB)’+AB
c) X=(AB)’+A’B’
d) X=A’B’+AB

Answer: d
Explanation: 1st output of AND gate is = A’B’
2nd AND gate’s output is = AB and,
OR gate’s output is = (A’B’)+(AB) = AB + A’B’.

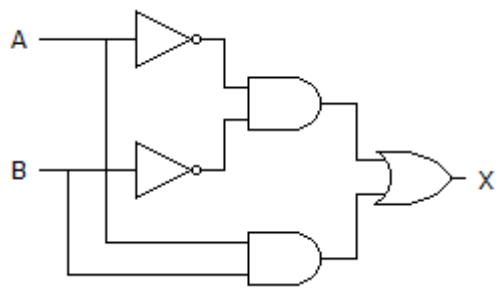
3. The device shown here is most likely a _____



a) Comparator
b) Multiplexer
c) Inverter
d) Demultiplexer

Answer: d
Explanation: The given diagram is demultiplexer, because it takes single input & gives many outputs. A demultiplexer is a combinational circuit that takes a single output and latches it to multiple outputs depending on the select lines.

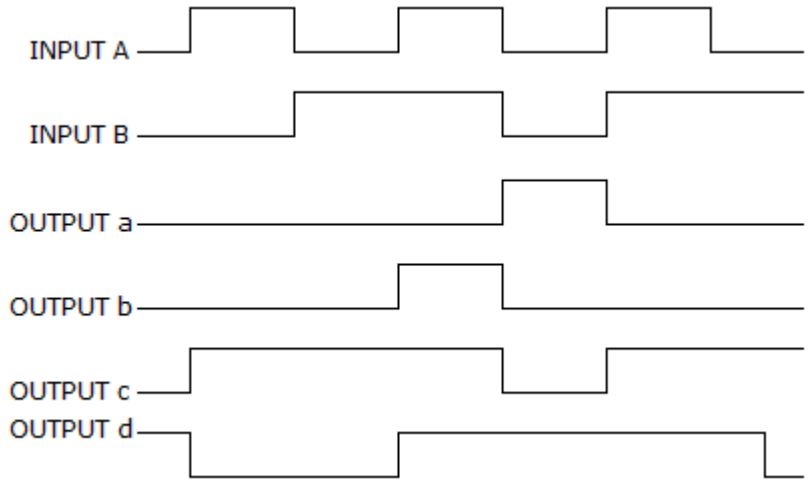
4. What type of logic circuit is represented by the figure shown below?



a) XOR
b) XNOR
c) AND
d) XAND

Answer: b
Explanation: After solving the circuit we get (A’B’)+AB as output, which is XNOR operation. Thus, it will produce 1 when inputs are even number of 1s or all 0s, and produce 0 when input is odd number of 1s.

5. For a two-input XNOR gate, with the input waveforms as shown below, which output waveform is correct?



a) d
b) a
c) c
d) b

Answer: a
Explanation: When both inputs are same then the o/p is high for a XNOR gate.
i.e., A B O/P
0 0 1
0 1 0
1 0 0
1 1 1.
Thus, it will produce 1 when inputs are even number of 1s or all 0s, and produce 0 when input is odd number of 1s.

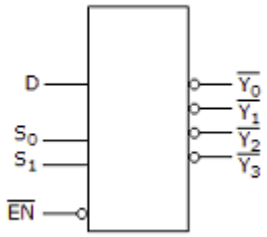
6. Which of the following combinations of logic gates can decode binary 1101?
a) One 4-input AND gate
b) One 4-input AND gate, one inverter
c) One 4-input AND gate, one OR gate
d) One 4-input NAND gate, one inverter

Answer: b
Explanation: For decoding any number output must be high for that code and this is possible in One 4-input NAND gate, one inverter option only. A decoder is a combinational circuit that converts binary data to n-coded data upto 2^n outputs.

7. What is the indication of a short to ground in the output of a driving gate?
a) Only the output of the defective gate is affected
b) There is a signal loss to all load gates
c) The node may be stuck in either the HIGH or the LOW state
d) The affected node will be stuck in the HIGH state

Answer: b
Explanation: Short to ground in the output of a driving gate indicates of a signal loss to all load gates. This results in information being disrupted and loss of data.

8. For the device shown here, assume the D input is LOW, both S inputs are LOW and the input is LOW. What is the status of the Y’ outputs?



a) All are HIGH
b) All are LOW
c) All but Y0 are LOW
d) All but Y0 are HIGH

Answer: d
Explanation: In the given diagram, S0 and S1 are selection bits. So,
I/P S0 S1 O/P
D = 0 0 0 Y0
D = 0 0 1 Y1
D = 0 1 0 Y2
D = 0 1 1 Y3
Hence, inputs are S0 and S1 are Low means 0, so output is Y0 and rest all are HIGH.

9. The carry propagation can be expressed as _____
a) Cp = AB
b) Cp = A + B
c) All but Y0 are LOW
d) All but Y0 are HIGH

Answer: b
Explanation: This happens in parallel adders (where we try to add numbers in parallel via more than one adders). A carry propagation occurs when carry from one adder needs to be forwarded to other adder and that second adder is holding the computation (addition) because carry from first adder has not come yet. So, there is a slight delay for second adder and this is known as carry propagation.

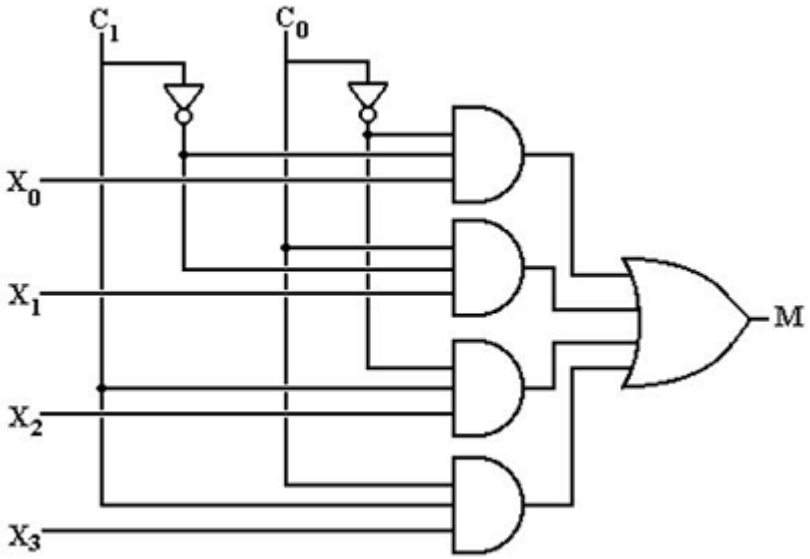
10. 3 bits full adder contains _____
a) 3 combinational inputs
b) 4 combinational inputs
c) 6 combinational inputs
d) 8 combinational inputs

Answer: d
Explanation: Full Adder is a combinational circuit with 3 input bits and 2 output bits CARRY and SUM. Three bits full adder requires $2^3 = 8$ combinational circuits.

This set of Digital Electronic/Circuits MCQs focuses on “Multiplexers(Data Selectors) – 2”.

1. 4 to 1 MUX would have _____
a) 2 inputs
b) 3 inputs
c) 4 inputs
d) 5 inputs

Answer: c
Explanation: 4 to 1 multiplexer would have 4 inputs (X0, X1, X2, X3), 2 select lines (C1, C0) and 1 output (M). It can be observed from this diagram:



2. The two input MUX would have _____
a) 1 select line
b) 2 select lines
c) 4 select lines
d) 3 select lines

Answer: a

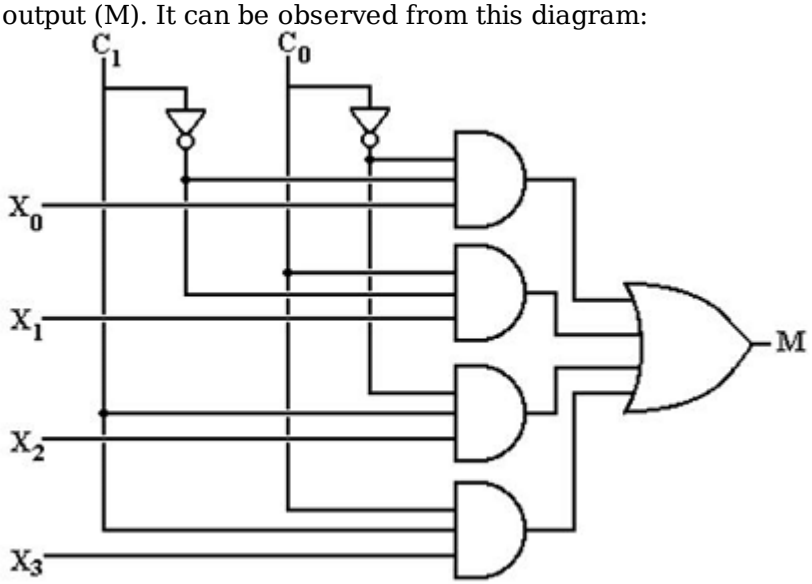
Explanation: The two input multiplexer would have n select lines in 2^n . Thus n =1. Therefore, it has 1 select line.

3. A combinational circuit that selects one from many inputs are _____
a) Encoder
b) Decoder
c) Demultiplexer
d) Multiplexer

Answer: d
Explanation: A combinational circuit that selects one from many inputs is known as Multiplexer. Whereas, a combinational circuit that divides one input into multiple outputs is known as Demultiplexer.

4. 4 to 1 MUX would have _____
a) 1 output
b) 2 outputs
c) 3 outputs
d) 4 outputs

Answer: a
Explanation: 4 to 1 multiplexer would have 4 inputs (X0, X1, X2, X3), 2 select lines (C1, C0) and 1 output (M). It can be observed from this diagram:



5. Which of the following circuit can be used as parallel to serial converter?
a) Multiplexer

b) Demultiplexer
c) Decoder
d) Digital counter

Answer: a
Explanation: A combinational circuit that selects one from many inputs is known as Multiplexer. In multiplexer, different inputs are inserted parallely and then it gives one output which is in serial form.

6. A combinational circuit is one in which the output depends on the _____
a) Input combination at the time
b) Input combination and the previous output
c) Input combination at that time and the previous input combination
d) Present output and the previous output

Answer: a
Explanation: A combinational circuit is one in which the output depends on the input combination at the time, whereas, a sequential circuit is one in which the output depends on present input as well past outputs.

7. Without any additional circuitry an 8:1 MUX can be used to obtain _____
a) Some but not all Boolean functions of 3 variables
b) All function of 3 variables but none of 4 variables
c) All functions of 3 variables and some but not all of 4 variables
d) All functions of 4 variables

Answer: d
Explanation: A 2^n:1 MUX can implement all logic functions of (n+1) variables without any additional circuitry. Thus 8:1 MUX can implement all logic functions of (3+1) variables, for 4 variables there are 16 possible combinations. So to use 8:1 MUX use 3 inputs as select lines of MUX and the 4th input as input of MUX.

8. A basic multiplexer principle can be demonstrated through the use of a _____
a) Single-pole relay
b) DPDT switch
c) Rotary switch
d) Linear stepper

Answer: c
Explanation: A combinational circuit that selects one from many inputs is known as Multiplexer. A basic multiplexer principle can be demonstrated through the use of a rotary switch. Because rotary switch gives one output corresponding to their inputs.

9. One multiplexer can take the place of _____
a) Several SSI logic gates
b) Combinational logic circuits
c) Several Ex-NOR gates
d) Several SSI logic gates or combinational logic circuits

Answer: d
Explanation: A combinational circuit that selects one from many inputs is known as Multiplexer. One multiplexer can take the place of several SSI logic gates or combinational logic circuits because it has a lot of functions to perform different operations.

10. The inputs/outputs of an analog multiplexer/demultiplexer are _____
a) Bidirectional
b) Unidirectional
c) Even parity
d) Binary-coded decimal

Answer: a
Explanation: One multiplexer can be used as demultiplexer. Hence, it is called bidirectional or two-way transmission.

11. If enable input is high then the multiplexer is _____
a) Enable
b) Disable
c) Saturation
d) High Impedance

Answer: b
Explanation: If enable input is high then the multiplexer is disabled because enable input is in inverted mode always (i.e. E').

12. What is data routing in a multiplexer?
a) It spreads the information to the control unit
b) It can be used to route data from one of several source to destination
c) It is an application of multiplexer
d) It can be used to route data and it is an application of multiplexer

Answer: d
Explanation: Multiplexing means passing more than one data through the same channel. Data routing is an application of multiplexer and it can be used to route data from one of several source to destination.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on "Multiplexers (Data Selectors) – 1".

1. What is a multiplexer?
a) It is a type of decoder which decodes several inputs and gives one output
b) A multiplexer is a device which converts many signals into one
c) It takes one input and results into many output
d) It is a type of encoder which decodes several inputs and gives one output

Answer: b
Explanation: A multiplexer (or MUX) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line, depending on the active select lines.

2. Which combinational circuit is renowned for selecting a single input from multiple inputs & directing the binary information to output line?
a) Data Selector
b) Data distributor
c) Both data selector and data distributor
d) DeMultiplexer

Answer: a
Explanation: Data Selector is another name of Multiplexer. A multiplexer (or MUX) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line, depending on the active select lines.

3. It is possible for an enable or strobe input to undergo an expansion of two or more MUX ICs to the digital multiplexer with the proficiency of large number of _____
a) Inputs
b) Outputs
c) Selection lines
d) Enable lines

Answer: a
Explanation: It is possible for an enable or strobe input to undergo an expansion of two or more MUX ICs to the digital multiplexer with the proficiency of large number of inputs.

4. Which is the major functioning responsibility of the multiplexing combinational circuit?
a) Decoding the binary information
b) Generation of all minterms in an output function with OR-gate
c) Generation of selected path between multiple sources and a single destination
d) Encoding of binary information

Answer: c
Explanation: The major functioning responsibility of the multiplexing combinational circuit is generation of selected path between multiple sources and a single destination because it makes the circuit too flexible. A multiplexer (or MUX) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line, depending on the active select lines.

5. What is the function of an enable input on a multiplexer chip?
a) To apply Vcc
b) To connect ground
c) To active the entire chip
d) To active one half of the chip

Answer: c
Explanation: Enable input is used to active the chip, when enable is high the chip works (ACTIVE), when enable is low the chip does not work (MEMORY). However, Enable can be Active-High or Active-Low, indicating it is active either when it is connected to VCC or GND respectively.

6. One multiplexer can take the place of _____
a) Several SSI logic gates
b) Combinational logic circuits
c) Several Ex-NOR gates
d) Several SSI logic gates or combinational logic circuits

Answer: d
Explanation: A multiplexer (or MUX) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line, depending on the active select lines. Since many operational behaviour can be performed by using a multiplexer. Whereas, a combinational circuit is a combination of many logic gates which makes the circuit more complex.

7. A digital multiplexer is a combinational circuit that selects _____
a) One digital information from several sources and transmits the selected one
b) Many digital information and convert them into one
c) Many decimal inputs and transmits the selected information
d) Many decimal outputs and accepts the selected information

Answer: a
Explanation: A digital multiplexer is a combinational circuit that selects one digital information from several sources and transmits the selected information on a single output line depending on the status of the select lines. That is why it is also known as a data selector.

8. In a multiplexer, the selection of a particular input line is controlled by _____
a) Data controller
b) Selected lines
c) Logic gates
d) Both data controller and selected lines

Answer: b
Explanation: The selection of a particular input line is controlled by a set of selected lines in a multiplexer, which helps to select a particular input from several sources.

9. If the number of n selected input lines is equal to 2^m then it requires _____ select lines.
a) 2
b) m
c) n
d) 2^n

Answer: b
Explanation: If the number of n selected input lines is equal to 2^m then it requires m select lines to select one of m select lines.

10. How many select lines would be required for an 8-line-to-1-line multiplexer?
a) 2

b) 4
c) 8
d) 3

Answer: d

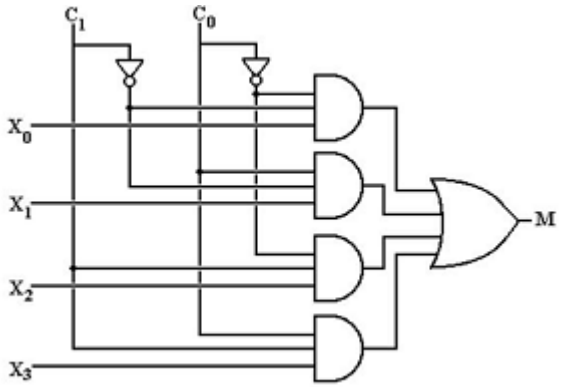
Explanation: 2^n input lines, n control lines and 1 output line available for MUX. Here, 8 input lines mean 2^3 inputs. So, 3 control lines are possible. Depending on the status of the select lines, the input is selected and fed to the output.

11. A basic multiplexer principle can be demonstrated through the use of a _____
a) Single-pole relay
b) DPDT switch
c) Rotary switch
d) Linear stepper

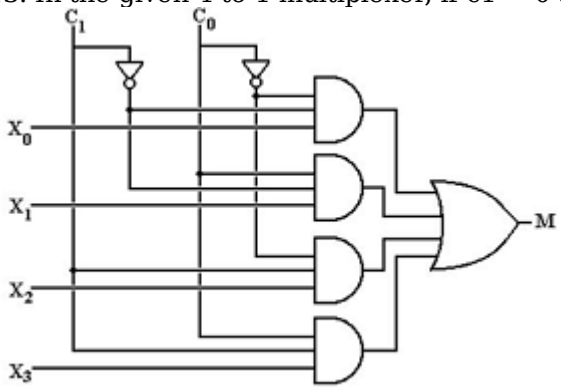
Answer: c
Explanation: A basic multiplexer principle can be demonstrated through the use of a rotary switch. Since its behaviour is similar to the multiplexer. There are around 10 digits out of which one is selected one at a time and fed to the output.

12. How many NOT gates are required for the construction of a 4-to-1 multiplexer?
a) 3
b) 4
c) 2
d) 5

Answer: c
Explanation: There are two NOT gates required for the construction of 4-to-1 multiplexer. x0, x1, x2 and x3 are the inputs and C1 and C0 are the select lines and M is the output.
The diagram of a 4-to-1 multiplexer is shown below:



13. In the given 4-to-1 multiplexer, if c1 = 0 and c0 = 1 then the output M is _____



a) X0
b) X1
c) X2
d) X3

Answer: b
Explanation: The output will be X1, because c1 = 0 and c0 = 1 results into 1 which further results as X1. And rest of the AND gates gives output as 0.

14. The enable input is also known as _____
a) Select input
b) Decoded input
c) Strobe
d) Sink

Answer: c
Explanation: The enable input is also known as strobe which is used to cascade two or more multiplexer ICs to construct a multiplexer with a larger number of inputs. Enable input activates the multiplexer to operate.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Liquid Crystal Displays”.

1. The full form of LCD is _____
a) Liquid Crystal Display
b) Liquid Crystalline Display
c) Logical Crystal Display
d) Logical Crystalline Display

Answer: a
Explanation: The full form of LCD is “Liquid Crystal Display”. They provide thinner displays as compared to Cathode Ray Tubes.

2. The optical properties of liquid crystals depend on the direction of _____
a) Air
b) Solid
c) Light

d) Water

Answer: c
Explanation: The optical properties of liquid crystals depend on the direction of light travels through a layer of the material.

3. By which properties, the orientation of molecules in a layer of liquid crystals can be changed?
a) Magnetic field
b) Electric field
c) Electromagnetic field
d) Gallois field

Answer: b
Explanation: In LCD, the electric field is induced by a small electric voltage applied across it; Due to which the orientation of molecules in a layer of liquid crystals can be changed.

4. Electro-optical effect is produced in _____
a) LED
b) LCD
c) OFC
d) OLED

Answer: b
Explanation: An electric field (induced by a small electric voltage) can change the orientation of molecules in a layer of liquid crystal and thus affect its optical properties. Such a process is termed an electro-optical effect, and it forms the basis for LCDs.

5. The direction of electric field in an LCD is determined by _____
a) the molecule’s chemical structure
b) Crystalline surface structure
c) Molecular Orbital Theory
d) Quantum Cellular Automata

Answer: a
Explanation: For LCDs, the change in optical properties results from orienting the molecular axes either along or perpendicular to the applied electric field, the preferred direction being determined by the details of the molecule’s chemical structure.

6. The first LCDs became commercially available in _____
a) 1950s
b) 1980s
c) 1960s
d) 1970s

Answer: c
Explanation: The first LCDs became commercially available in the late 1960s and were based on a light-scattering effect known as the dynamic scattering mode.

7. LCDs operate from a voltage ranges from _____
a) 3 to 15V
b) 10 to 15V
c) 10V
d) 5V

Answer: a
Explanation: LCDs operate from a voltage ranges from 3 to 15V rms. They provide thinner displays as compared to Cathode Ray Tubes.

8. LCDs operate from a frequency ranges from _____
a) 10Hz to 60Hz
b) 50Hz to 70Hz
c) 30Hz to 60Hz
d) None of the Mentioned

Answer: c
Explanation: LCDs operate from a frequency ranges from 30Hz to 60Hz. LCDs operate from a voltage ranges from 3 to 15V rms. They provide thinner displays as compared to Cathode Ray Tubes.

9. In 7 segment display, how many LEDs are used?
a) 8
b) 7
c) 10
d) 9

Answer: b
Explanation: There are 7 LEDs used in a 7 segment display. 7 segment displays are used for displaying decimal numerals which are comparatively convenient to dot matrix displays.

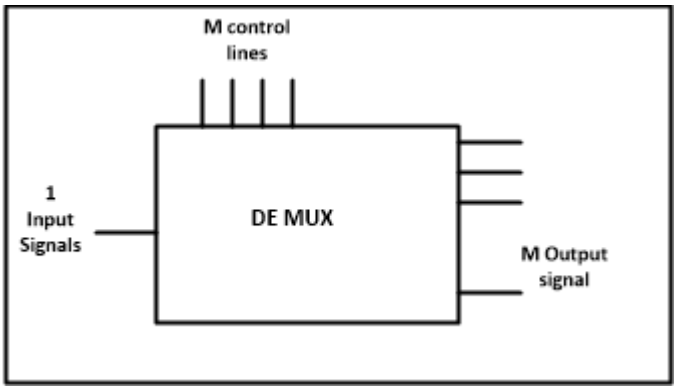
10. What is the backplane in LCD?
a) The ac voltage applied between segment and a common element
b) The dc voltage applied between segment and a common element
c) The amount of power consumed
d) For adjusting the intensity of the LCD

Answer: a
Explanation: The ac voltage applied between the segment and a common element is called the backplane(bp). In which each segment is driven by an EX-OR gate.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Demultiplexers (Data Distributors) – 1”.

1. The word demultiplex means _____
a) One into many
b) Many into one
c) Distributor
d) One into many as well as Distributor

Answer: d
Explanation: The word demultiplex means “one into many” and distributor. A demultiplexer sends a single input to multiple outputs, depending on the select lines. It is clear from the diagram:



2. Why is a demultiplexer called a data distributor?
a) The input will be distributed to one of the outputs
b) One of the inputs will be selected for the output
c) The output will be distributed to one of the inputs
d) Single input to Single Output

Answer: a
Explanation: A demultiplexer sends a single input to multiple outputs, depending on the select lines. For one input, the demultiplexer gives several outputs. That is why it is called a data distributor.

3. Most demultiplexers facilitate which type of conversion?
a) Decimal-to-hexadecimal
b) Single input, multiple outputs
c) AC to DC
d) Odd parity to even parity

Answer: b
Explanation: A demultiplexer sends a single input to multiple outputs, depending on the select lines. Demultiplexer converts single input into multiple outputs.

4. In 1-to-4 demultiplexer, how many select lines are required?
a) 2
b) 3
c) 4
d) 5

Answer: a

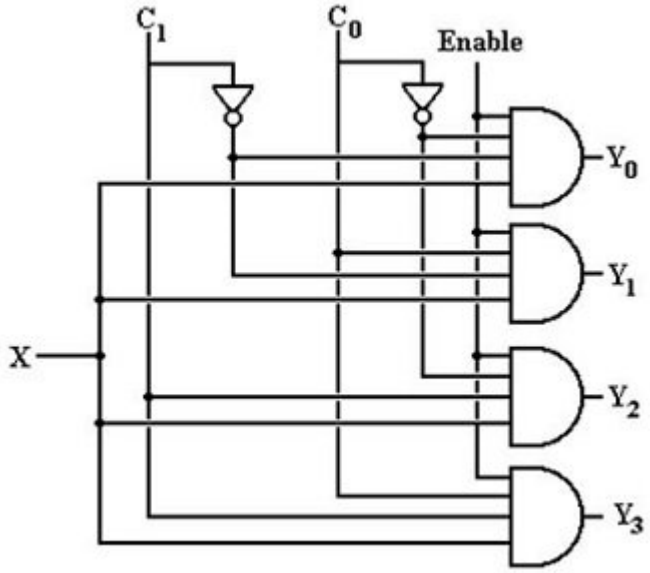
Explanation: The formula for total no. of outputs is given by 2^n , where n is the no. of select lines. Therefore, for 1:4 demultiplexer, 2 select lines are required.

5. In a multiplexer the output depends on its _____
a) Data inputs
b) Select inputs
c) Select outputs
d) Enable pin

Answer: b
Explanation: A demultiplexer sends a single input to multiple outputs, depending on the select lines. As the select input changes, the output of the multiplexer varies according to that input.

6. In 1-to-4 multiplexer, if C1 = 0 & C2 = 1, then the output will be _____
a) Y0
b) Y1
c) Y2
d) Y3

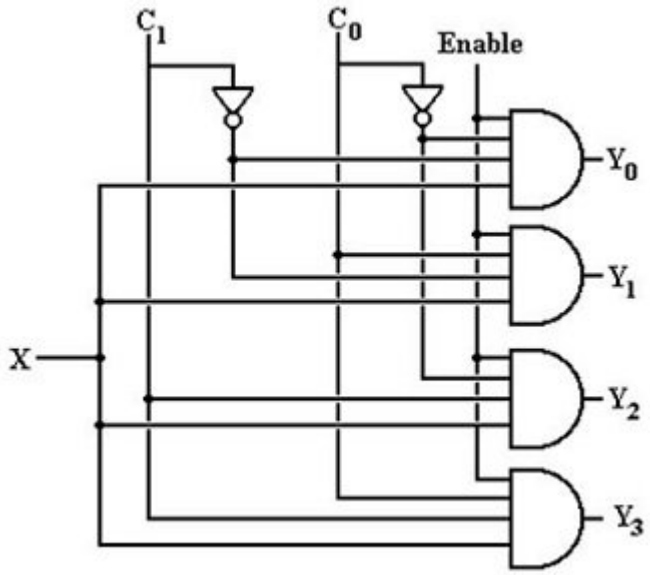
Answer: b
Explanation: It can be calculated from the figure shown below:



For C0 =1 and C1 =0, Y1 will be the output as 0 and 1 are the bit combinations of 1.

7. In 1-to-4 multiplexer, if C1 = 1 & C2 = 1, then the output will be _____
a) Y0
b) Y1
c) Y2
d) Y3

Answer: d
Explanation: It can be calculated from the figure shown below:



For C0 =1 and C1 =0, Y3 will be the output as 0 and 1 are the bit combinations of 1.

8. How many select lines are required for a 1-to-8 demultiplexer?
a) 2
b) 3
c) 4
d) 5

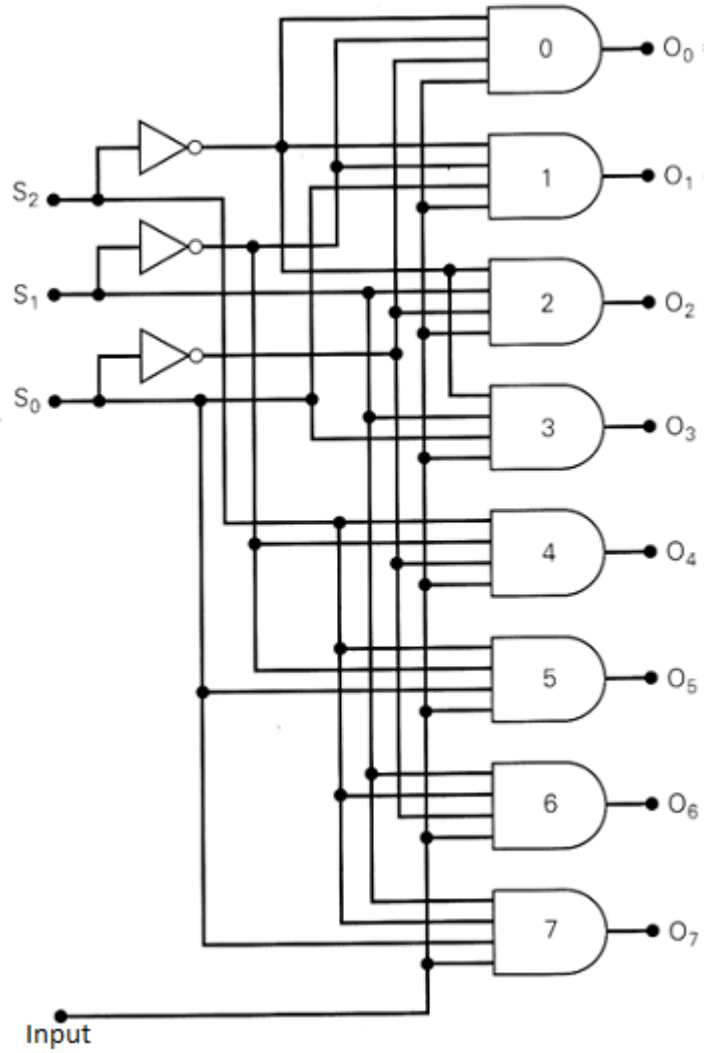
Answer: b

Explanation: The formula for total no. of outputs is given by 2^n , where n is the no. of select lines. In this case n = 3 since $2^3 = 8$.

9. How many AND gates are required for a 1-to-8 multiplexer?
a) 2
b) 6
c) 8
d) 5

Answer: c
Explanation: The number of AND gates required will be equal to the number of outputs in a demultiplexer, which are 8.

10. The output Q4 of this 1-to-8 demultiplexer is _____



a) $Q2.(Q1)'.Q0.I$

b) Q2.Q1.(Q0)’.I
c) Q2.(Q1)’.(Q0)’.I
d) Q2.(Q1).Q0.I

Answer: c
Explanation: The output Y4 = Q2.(Q1)’.(Q0)’.I. since the bit combinations of 4 are 100.

11. Which IC is used for the implementation of 1-to-16 DEMUX?
a) IC 74154
b) IC 74155
c) IC 74139
d) IC 74138

Answer: a
Explanation: IC 74154 is used for the implementation of 1-to-16 DEMUX, whose output is inverted input.

This set of Digital Electronic/Circuits Multiple Choice Questions & Answers focuses on “Demultiplexers(Data Distributors) – 2”.

1. Why is a demultiplexer called a data distributor?
a) The input will be distributed to one of the outputs
b) One of the inputs will be selected for the output
c) The output will be distributed to one of the inputs
d) Single input gives single output

Answer: a
Explanation: A demultiplexer sends a single input to multiple outputs, depending on the select lines. For one input, the demultiplexer gives several outputs. That is why it is called a data distributor.

2. Most demultiplexers facilitate which type of conversion?
a) Decimal-to-hexadecimal
b) Single input, multiple outputs
c) AC to DC
d) Odd parity to even parity

Answer: b
Explanation: A demultiplexer sends a single input to multiple outputs, depending on the select lines. Demultiplexer converts single input into multiple outputs.

3. In 1-to-4 demultiplexer, how many select lines are required?
a) 2
b) 3
c) 4
d) 5

Answer: a

Explanation: The formula for total no. of outputs is given by 2^n , where n is the no. of select lines. Therefore, for 1:4 demultiplexer, 2 select lines are required.

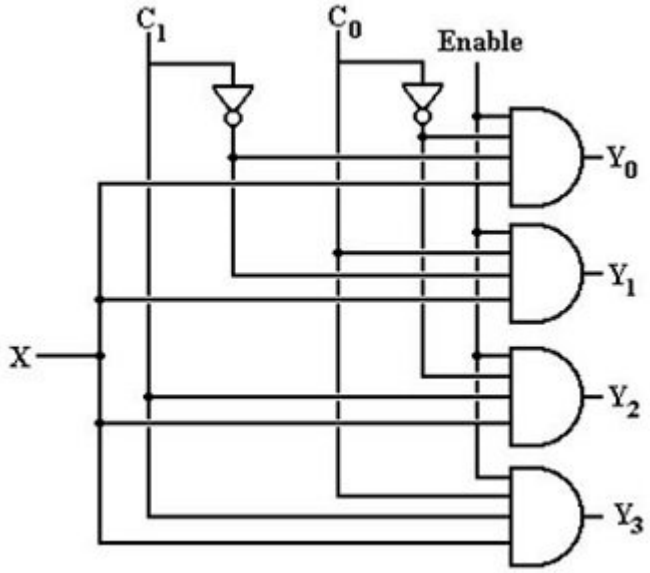
4. In a multiplexer the output depends on its _____
a) Data inputs
b) Select inputs
c) Select outputs
d) Enable pin

Answer: b
Explanation: A demultiplexer sends a single input to multiple outputs, depending on the select lines. As the select input changes, the output of the multiplexer varies according to that input.

5. In 1-to-4 multiplexer, if C1 = 1 & C2 = 1, then the output will be _____
a) Y0
b) Y1
c) Y2

d) Y3

Answer: d
Explanation: It can be calculated from the figure shown below:



For C0 =1 and C1 =1, Y3 will be the output as 0 and 1 are the bit combinations of 1.

6. How many select lines are required for a 1-to-8 demultiplexer?
a) 2

b) 3
c) 4
d) 5

Answer: b

Explanation: The formula for total no. of outputs is given by 2^n , where n is the no. of select lines. In this case n = 3 since $2^3 = 8$.

7. How many AND gates are required for a 1-to-8 multiplexer?
a) 2
b) 6
c) 8
d) 5

Answer: c
Explanation: The number of AND gates required will be equal to the number of outputs in a demultiplexer, which are 8.

8. Which IC is used for the implementation of 1-to-16 DEMUX?
a) IC 74154
b) IC 74155
c) IC 74139
d) IC 74138

Answer: a
Explanation: IC 74154 is used for the implementation of 1-to-16 DEMUX, whose output is inverted input.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Encoders”.

1. How many inputs will a decimal-to-BCD encoder have?
a) 4
b) 8
c) 10
d) 16

Answer: c

Explanation: An encoder is a combinational circuit encoding the information of 2^n input lines to n output lines, thus producing the binary equivalent of the input. Thus, a Decimal-to-bcd converter has decimal values as inputs which range from 0-9. So, a total of 10 inputs are there in a decimal-to-BCD encoder.

2. How many outputs will a decimal-to-BCD encoder have?
a) 4
b) 8
c) 12
d) 16

Answer: a

Explanation: An encoder is a combinational circuit encoding the information of 2^n input lines to n output lines, thus producing the binary equivalent of the input. Thus, a decimal to BCD encoder has 4 outputs.

3. How is an encoder different from a decoder?
a) The output of an encoder is a binary code for 1-of-N input
b) The output of a decoder is a binary code for 1-of-N input
c) The output of an encoder is a binary code for N-of-1 output
d) The output of a decoder is a binary code for N-of-1 output

Answer: a

Explanation: An encoder is a combinational circuit encoding the information of 2^n input lines to n output lines, thus producing the binary equivalent of the input. It performs the opposite

operation of a decoder which results in 2^n outputs from n inputs. Thus, an encoder different from a decoder because of the output of an encoder is a binary code for 1-of-N input.

4. If we record any music in any recorder, such types of process is called _____
a) Multiplexing
b) Encoding
c) Decoding
d) Demultiplexing

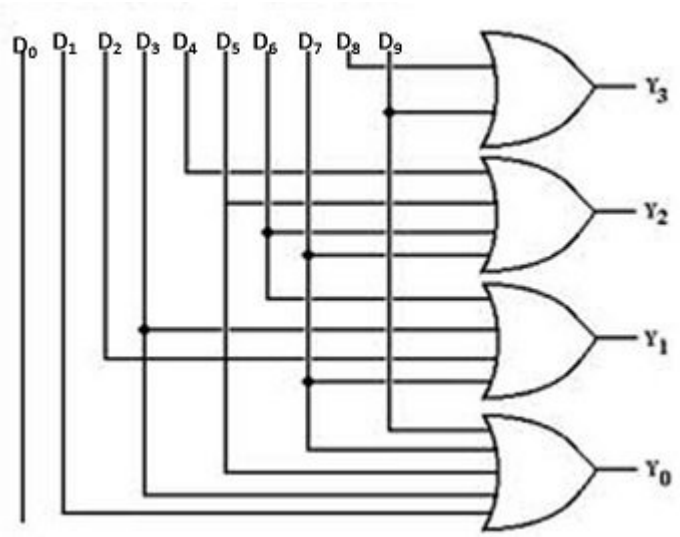
Answer: b
Explanation: If we record any music in any recorder, it means that we are giving data to a recorder. So, such process is called encoding. Getting back the music from the recorded data is known as decoding.

5. Can an encoder be a transducer?
a) Yes
b) No
c) May or may not be
d) Both are not even related slightly

Answer: a
Explanation: Of course, a transducer is a device that has the capability to emit data as well as to accept. Transducer converts signal from one form of energy to another.

6. How many OR gates are required for a Decimal-to-bcd encoder?
a) 2
b) 10
c) 3
d) 4

Answer: d
Explanation: An encoder is a combinational circuit encoding the information of 2^n input lines to n output lines, thus producing the binary equivalent of the input.
This is clear from the diagram that it requires 4 OR gates:



7. How many OR gates are required for an octal-to-binary encoder?
a) 3
b) 2
c) 8
d) 10

Answer: a

Explanation: An encoder is a combinational circuit encoding the information of 2^n input lines to n output lines, thus producing the binary equivalent of the input. Thus, in octal to binary encoder there are 8 ($=2^3$) inputs, thus 3 output lines.

8. For 8-bit input encoder how many combinations are possible?
a) 8
b) 2^8
c) 4
d) 2^4

Answer: b

Explanation: An encoder is a combinational circuit encoding the information of 2^n input lines to n output lines, thus producing the binary equivalent of the input. There are 2^8 combinations are possible for an 8-bit input encoder but out of which only 8 are used using 3 output lines. It is a disadvantage of encoder.

9. The discrepancy of 0 output due to all inputs being 0 or D0, being 0 is resolved by using additional input known as _____
a) Enable
b) Disable
c) Strobe
d) Clock

Answer: a
Explanation: Such problems are resolved by using enable input, which behaves as active if it gets 0 as input since it is an active-low pin.

10. Can an encoder be called a multiplexer?
a) No
b) Yes
c) Sometimes
d) Never

Answer: b
Explanation: A multiplexer or MUX is a combination circuit that contains more than one input line, one output line and more than one selection line. Whereas, an encoder is also considered a type of multiplexer but without a single output line and without any selection lines.

11. If two inputs are active on a priority encoder, which will be coded on the output?
a) The higher value
b) The lower value
c) Neither of the inputs
d) Both of the inputs

Answer: a

Explanation: An encoder is a combinational circuit encoding the information of 2^n input lines to n output lines, thus producing the binary equivalent of the input. If two inputs are active on a priority encoder, the input of higher value will be coded in the output.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Parity Generators/Checkers – 1”.

1. How many outputs are present in a BCD decoder?
a) 4
b) 5
c) 15
d) 10

Answer: d
Explanation: A binary decoder is a combinational logic circuit which decodes binary information from n-inputs to a maximum of 2^n outputs. A BCD to Decimal decoder has 10 number of outputs because the decimal digit’s range is from 0 to 9.

2. Which digital system translates coded characters into a more useful form?
a) Encoder
b) Display
c) Counter
d) Decoder

Answer: d
Explanation: A binary decoder is a combinational logic circuit which decodes binary information from n-inputs to a maximum of 2^n outputs. Decoder converts the coded characters into our required data form.

3. What control signals may be necessary to operate a 1-line-to-16 line decoder?
a) Flasher circuit control signal
b) A LOW on all gate enable inputs
c) Input from a hexadecimal counter
d) A HIGH on all gate enable circuits

Answer: b
Explanation: A LOW on all gate enable inputs is necessary to operate a 1-line-to-16 line decoder because enable pins are usually, active-low pins.

4. How many inputs are required for a 1-of-10 BCD decoder?
a) 4
b) 8
c) 10
d) 2

Answer: a
Explanation: A binary decoder is a combinational logic circuit which decodes binary information from n-inputs to a maximum of 2^n outputs. Therefore, for a BCD to decimal decoder, No. of inputs = 4 such that number of outputs is $<= 2^n$.

5. A BCD decoder will have how many rows in its truth table?
a) 10
b) 9
c) 8
d) 3

Answer: a
Explanation: A binary decoder is a combinational logic circuit which decodes binary information from n-inputs to a maximum of 2^n outputs. Thus, BCD decoder will have 10 rows as it’s input ranges from 0 to 9.

6. How many possible outputs would a decoder have with a 6-bit binary input?
a) 32
b) 64
c) 128
d) 16

Answer: c
Explanation: The possible outputs would be: $2^n = 64$ (Since n = 6 here).

7. Which is the way to convert BCD to binary using the hardware approach?
a) By using MSI IC circuits
b) By using a keyboard encoder
c) By using an ALU
d) By using UART

Answer: a
Explanation: One way to convert BCD to binary using the hardware approach is MSI (medium scale integration) IC circuits.

8. How many inputs are required for a 1-of-16 decoder?
a) 2
b) 16
c) 8
d) 4

Answer: d
Explanation: A binary decoder is a combinational logic circuit which decodes binary information

from n-inputs to a maximum of 2^n outputs. Here, number of outputs = 16.
$16 = 2^4 = 2^n$. Thus, number of inputs is 4.

9. A truth table with output columns numbered 0–15 may be for which type of decoder IC?
a) Hexadecimal 1-of-16
b) Dual octal outputs
c) Binary-to-hexadecimal
d) Hexadecimal-to-binary

Answer: a
Explanation: A binary decoder is a combinational logic circuit that decodes binary information from n-inputs to a maximum of 2^n outputs. A truth table with output columns numbered 0–15 may be for Hexadecimal 1-of-16. Because hexadecimal occupies less space in a system.

10. How can the active condition (HIGH or LOW) or the decoder output be determined from the logic symbol?
a) A bubble indicates active-HIGH
b) A bubble indicates active-LOW
c) A triangle indicates active-HIGH
d) A triangle indicates active-LOW

Answer: b
Explanation: A bubble indicates active-LOW in a decoder always. Enable pin of the decoder is usually active-LOW and is triggered on the input being at 0.

This set of Digital Electronic/Circuits online test focuses on “Parity Generators/Checkers – 2”.

1. Which error detection method uses one’s complement arithmetic?
a) Simple parity check
b) Two-dimensional parity check
c) CRC
d) Checksum

Answer: d
Explanation: A checksum is an error detection method used for the purpose of detecting errors that may have been incorporated during transmission. The checksum can be generated simply by adding bits. Hence, one’s complement arithmetic uses checksum.

2. Which error detection method consists of just one redundant bit per data unit?
a) Simple parity check
b) Two-dimensional parity check
c) CRC
d) Checksum

Answer: a
Explanation: A parity checker is an error detection method used for the purpose of detecting errors that may have been incorporated during transmission. Simple parity check method consists of just one redundant bit per data unit. It is again classified as even parity and odd parity.

3. How many types of parity bits are found?
a) 2
b) 3
c) 4
d) 1

Answer: a
Explanation: There are two types of parity bits, namely even parity and odd parity. In even parity, a 1 bit is added in order to make a group of data bits have even number of 1s. While, in odd parity, a 1 bit is added in order to make a group of data bits have odd number of 1s.

4. What is a parity bit?
a) An error detection is achieved by adding an extra bit
b) After addition, the carry is found

c) Bit generated during data transmission
d) After addition, the total number of bits

Answer: a
Explanation: A simple form of error detection is achieved by adding an extra bit to the transmitted word. The additional bit is known as parity bits.

5. The BCD number 101011 has _____ priority.
a) Even
b) Odd
c) Both even and odd
d) Undefined

Answer: a
Explanation: The given BCD number 101011 has even priority because it has an even number of 1's (i.e. 4).

6. Which error detection method involves polynomials?
a) Simple parity check
b) CRC
c) Two-dimensional parity check
d) Checksum

Answer: b
Explanation: Cyclic Redundancy Check(CRC) involves parity check polynomials. In the even parity case of CRC, the 1-bit is generated by checking the polynomial x+1.

7. The odd parity output of decimal number 9 is _____
a) 0
b) 1
c) 1001
d) 0011

Answer: b
Explanation: The odd parity output of decimal number 9 is 1 because the BCD number for 9 is 1001 and it has even number of 1's.

8. If odd parity is used for ASCII error detection, the number of 0s per 8-bit symbol is _____
a) Indeterminate
b) 42
c) Even
d) Odd

Answer: a
Explanation: Odd parity bit is 1 when the group of data bits consists of even number of 1s. So to make the group of data bits have odd number of 1s, 1 extra bit is added. If odd parity is used for ASCII error detection, the number of 0s per 8-bit symbol is indeterminate because it is applicable only for 6-bit symbol.

9. Which error detection method can detect a single-bit error?
a) Simple parity check
b) Two-dimensional parity check
c) CRC
d) Checksum

Answer: b
Explanation: A single-bit error can be detected by using two-dimensional parity check method. Since it converts the 4-bit number into 8-bit and count the number of one's.

10. Which gates are ideal for checking the parity bits?
a) AND
b) NAND
c) EX-OR
d) EX-NOR

Answer: c
Explanation: Exclusive-OR gates are ideal for checking the parity of a binary number because they produce an output when the input has an odd number of 1's. Therefore, an even-parity input to an EX-OR gate produces a low output, while an odd parity input produces a high output. While, in case of AND, it produces high output when all inputs are 1 else low. Whereas, NAND, does the opposite, by producing low output when all inputs are 1 else high.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on "Magnitude Comparator".

1. All the comparisons made by comparator is done using _____
a) 1 circuit
b) 2 circuits
c) 3 circuits
d) 4 circuits

Answer: a
Explanation: A comparator is a combinational circuit that takes two numbers as input in binary form and results whether one input is greater, lesser or equal to the other input. Because, all the input is compared to each other, therefore it is possible only by using 1 circuit.

2. One that is not the outcome of magnitude comparator is _____
a) a > b
b) a – b
c) a < b
d) a = b

Answer: b
Explanation: A comparator is a combinational circuit that takes two numbers as input in binary form and results whether one input is greater, lesser or equal to the other input. In a digital comparator, only 3 outputs are possible (i.e. A = B, A > B, A < B). So, a – b is an incorrect option.

3. If two numbers are not equal then binary variable will be _____
a) 0
b) 1
c) A
d) B

Answer: a
Explanation: A comparator is a combinational circuit that takes two numbers as input in binary form and results whether one input is greater, lesser or equal to the other input. In a digital comparator, only 3 outputs are possible (i.e. A = B, A >B, A < B). Other than this, the output will be 0.

4. How many inputs are required for a digital comparator?
a) 1
b) 2
c) 3
d) 4

Answer: a
Explanation: A comparator is a combinational circuit that takes two numbers as input in binary form and results whether one input is greater, lesser or equal to the other input. Thus, there are two inputs required for a digital comparator (i.e. A & B).

5. In a comparator, if we get input as A>B then the output will be _____
a) 1
b) 0
c) A
d) B

Answer: a
Explanation: A comparator is a combinational circuit that takes two numbers as input in binary

form and results whether one input is greater, lesser or equal to the other input. If A > B, it means that it satisfies one of the condition among three. Hence the output will be 1.

6. Which one is a basic comparator?
a) XOR
b) XNOR
c) AND
d) NAND

Answer: a
Explanation: Generally, an XNOR outputs high for even number of 1s or all 0s and outputs low for otherwise. Thus, an XNOR gate is a basic comparator, because its output is “1” only if its two input bits are equal.

7. Comparators are used in _____
a) Memory
b) CPU
c) Motherboard
d) Hard drive

Answer: b
Explanation: Comparators are used in the central processing unit (CPUs). Because all the arithmetic and logical operations are performed in the ALU(Arithmetic Logic Unit) part of the CPU.

8. A circuit that compares two numbers and determines their magnitude is called _____
a) Height comparator
b) Size comparator
c) Comparator
d) Magnitude comparator

Answer: d
Explanation: A comparator is a combinational circuit that takes two numbers as input in binary form and results whether one input is greater, lesser or equal to the other input. A circuit that compares two numbers and determine their magnitude is called magnitude comparator.

9. A procedure that specifies finite set of steps is called _____
a) Algorithm
b) Flow chart
c) Chart
d) Venn diagram

Answer: a
Explanation: A procedure that specifies finite set of steps is called algorithm, While a flowchart is a pictorial representation of the algorithm.

10. How many types of digital comparators are?
a) 1
b) 2
c) 3
d) 4

Answer: b
Explanation: There are two main types of Digital Comparator available and these are: Identity Comparator & Magnitude Comparator. Identity Comparator checks only the equality of the inputs and thus has one output terminal. While Magnitude Comparator checks for greater than, less than as well as equality of the inputs, and thus has 3 output terminals.

11. An identify comparator is defined as a digital comparator which has _____
a) Only one output terminal
b) Two output terminals
c) Three output terminals
d) No output terminal

Answer: a
Explanation: An Identity Comparator is a digital comparator that has only one output terminal for when A = B either “HIGH” A = B = 1 or “LOW” A = B = 0.

12. A magnitude comparator is defined as a digital comparator which has _____
a) Only one output terminal
b) Two output terminals
c) Three output terminals
d) No output terminal

Answer: c
Explanation: A Magnitude Comparator is a digital comparator which has three output terminals, one each for equality, A = B greater than, A > B and less than A < B.

13. The purpose of a Digital Comparator is _____
a) To convert analog input into digital
b) To create different outputs
c) To add a set of different numbers
d) To compare a set of variables or unknown numbers

Answer: d
Explanation: A comparator is a combinational circuit that takes two numbers as input in binary form and results whether one input is greater, lesser or equal to the other input. The purpose of a Digital Comparator is to compare a set of variables or unknown numbers, for example A (A1, A2, A3, …. An, etc) against that of a constant or unknown value such as B (B1, B2, B3, …. Bn, etc) and produce an output condition or flag depending upon the result of the comparison.

14. TTL 74LS85 is a _____
a) 1-bit digital comparator
b) 4-bit magnitude comparator
c) 8-bit magnitude comparator
d) 8-bit word comparator

Answer: b
Explanation: TTL 74LS85 is a 4-bit magnitude comparator.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Code Converters”.

1. A code converter is a logic circuit that _____
a) Inverts the given input
b) Converts into decimal number
c) Converts data of one type into another type
d) Converts to octal

Answer: c
Explanation: A code converter is a logic circuit that changes data presented in one type of binary code to another type of binary code.

2. Use the weighting factors to convert the following BCD numbers to binary _____

```
0101 0011 & 0010 0110 1000
```

a) 01010011 001001101000
b) 11010100 100001100000
c) 110101 100001100
d) 101011 001100001

Answer: c
Explanation: Firstly, convert every 4 sets of binary to decimal from the given: 0101=5, 0011=3. Then convert 53 to binary, which will give 110101. Again, do the same with the next 4 set of binary digits.

3. The primary use for Gray code is _____
a) Coded representation of a shaft’s mechanical position
b) Turning on/off software switches

c) To represent the correct ASCII code to indicate the angular position of a shaft on rotating machinery
d) To convert the angular position of a shaft on rotating machinery into hexadecimal code

Answer: a
Explanation: Gray code is useful because only one bit changes at a time, which is implemented easily in Coded representation of a shaft's mechanical position. In Gray Code, every sequence of successive bits differs by 1 bit only.

4. Code is a symbolic representation of _____
a) Discrete information
b) Continuous information
c) Decimal information into binary
d) Binary information into decimal

Answer: a
Explanation: Code is a symbolic representation of discrete information. Codes can be anything like numbers, letter or words, written in terms of group of symbols.

5. One way to convert BCD to binary using the hardware approach is _____
a) With MSI IC circuits
b) With a keyboard encoder
c) With an ALU
d) UART

Answer: a
Explanation: One way to convert BCD to binary using the hardware approach is MSI IC (i.e. medium scale integration) circuits.

6. Why is the Gray code more practical to use when coding the position of a rotating shaft?
a) All digits change between counts
b) Two digits change between counts
c) Only one digit changes between counts
d) Alternate digit changes between counts

Answer: c
Explanation: The Gray code is more practical to use when coding the position of a rotating shaft because only one digit changes between counts that is reflected to the next count.

7. Reflected binary code is also known as _____
a) BCD code
b) Binary code
c) ASCII code
d) Gray Code

Answer: d
Explanation: The reflected binary code is also known as gray code because one digit reflected to the next bit. In Gray Code, every sequence of successive bits differs by 1 bit only.

8. Why do we use gray codes?
a) To count the no of bits changes
b) To rotate a shaft
c) Error correction
d) Error Detection

Answer: c
Explanation: Today, Gray codes are widely used to facilitate error correction in digital communications such as digital terrestrial television and some cable TV systems.

9. Earlier, reflected binary codes were applied to _____
a) Binary addition
b) 2's complement
c) Mathematical puzzles
d) Binary multiplication

Answer: c
Explanation: The reflected binary code is also known as gray code because one digit reflected to the next bit. In Gray Code, every sequence of successive bits differs by 1 bit only. Reflected binary codes were applied to mathematical puzzles before they became known to engineers.

10. The binary representation of BCD number 00101001 (decimal 29) is _____
a) 0011101
b) 0110101
c) 1101001
d) 0101011

Answer: a
Explanation: The given BCD number 00101001 has three 1s. So, it can be rewritten as 0000001-1, 0001000-8, 0010100-20 and after addition, we get 0011101 as output.

11. Convert binary number into gray code: 100101.
a) 101101
b) 001110
c) 110111
d) 111001

Answer: c
Explanation: : Conversion from Binary To Gray Code:

```
1 (XOR) 0 (XOR)  0 (XOR)  1 (XOR)  0 (XOR)  1

        ↓        ↓        ↓        ↓        ↓

1       1        0        1        1        1
```

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Latches”.

1. A latch is an example of a _____
a) Monostable multivibrator
b) Astable multivibrator
c) Bistable multivibrator
d) 555 timer

Answer: c
Explanation: A latch is an example of a bistable multivibrator. A Bistable multivibrator is one in which the circuit is stable in either of two states. It can be flipped from one state to the other state and vice-versa.

2. Latch is a device with _____
a) One stable state
b) Two stable state
c) Three stable state
d) Infinite stable states

Answer: b
Explanation: Since a latch works on the principal of bistable multivibrator. A Bistable multivibrator is one in which the circuit is stable in either of two states. It can be flipped from one state to the other state and vice-versa. So a latch has two stable states.

3. Why latches are called memory devices?
a) It has capability to stare 8 bits of data
b) It has internal memory of 4 bit
c) It can store one bit of data
d) It can store infinite amount of data

Answer: c
Explanation: Latches can be memory devices, and can store one bit of data for as long as the device is powered. Once device is turned off, the memory gets refreshed.

4. Two stable states of latches are _____
a) Astable & Monostable
b) Low input & high output
c) High output & low output
d) Low output & high input

Answer: c
Explanation: A latch has two stable states, following the principle of Bistable Multivibrator. There are two stable states of latches and these states are high-output and low-output.

5. How many types of latches are _____
a) 4
b) 3
c) 2
d) 5

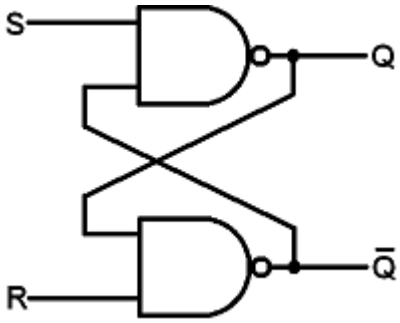
Answer: a
Explanation: There are four types of latches: SR latch, D latch, JK latch and T latch. D latch is a modified form of SR latch whereas, T latch is an advanced form of JK latch.

6. The full form of SR is _____
a) System rated
b) Set reset
c) Set ready
d) Set Rated

Answer: b
Explanation: The full form of SR is set/reset. It is a type of latch having two stable states.

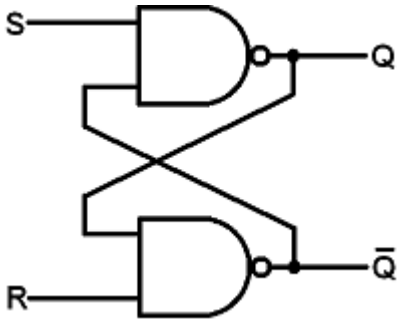
7. The SR latch consists of _____
a) 1 input
b) 2 inputs
c) 3 inputs
d) 4 inputs

Answer: b
Explanation: SR or Set-Reset latch is the simplest type of bistable multivibrator having two stable states.
The diagram of SR latch is shown below:



8. The outputs of SR latch are _____
a) x and y
b) a and b
c) s and r
d) q and q’

Answer: d
Explanation: SR or Set-Reset latch is the simplest type of bistable multivibrator having two stable states. The inputs of SR latch are s and r while outputs are q and q’. It is clear from the diagram:



9. The NAND latch works when both inputs are _____
a) 1
b) 0
c) Inverted
d) Don’t cares

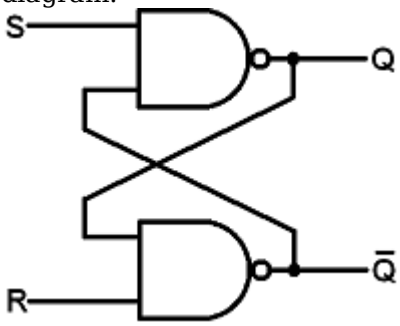
Answer: a
Explanation: The NAND latch works when both inputs are 1. Since both of the inputs are inverted in a NAND latch.

10. The first step of the analysis procedure of SR latch is to _____
a) label inputs
b) label outputs
c) label states
d) label tables

Answer: b
Explanation: All flip flops have at least one output labeled Q (i.e. inverted). This is so because the flip flops have inverting gates inside them, hence in order to have both Q and Q complement available, we have atleast one output labelled.

11. The inputs of SR latch are _____
a) x and y
b) a and b
c) s and r
d) j and k

Answer: c
Explanation: SR or Set-Reset latch is the simplest type of bistable multivibrator having two stable states. The inputs of SR latch are s and r while outputs are q and q'. It is clear from the diagram:



12. When a high is applied to the Set line of an SR latch, then _____
a) Q output goes high
b) Q' output goes high
c) Q output goes low
d) Both Q and Q' go high

Answer: a
Explanation: S input of an SR latch is directly connected to the output Q. So when a high is applied Q output goes high and Q' low.

13. When both inputs of SR latches are low, the latch _____
a) Q output goes high
b) Q’ output goes high
c) It remains in its previously set or reset state
d) it goes to its next set or reset state

Answer: c
Explanation: When both inputs of SR latches are low, the latch remains in it’s present state. There is no change in output.

14. When both inputs of SR latches are high, the latch goes _____
a) Unstable
b) Stable
c) Metastable
d) Bistable

Answer: c
Explanation: When both gates are identical and this is “metastable”, and the device will be in an undefined state for an indefinite period.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Flip Flops – 1”.

1. Latches constructed with NOR and NAND gates tend to remain in the latched condition due to which configuration feature?
a) Low input voltages
b) Synchronous operation
c) Gate impedance
d) Cross coupling

Answer: d
Explanation: Latch is a type of bistable multivibrator having two stable states. Both inputs of a latch are directly connected to the other’s output. Such types of structure is called cross coupling and due to which latches remain in the latched condition.

2. One example of the use of an S-R flip-flop is as _____
a) Transition pulse generator
b) Racer
c) Switch debouncer
d) Astable oscillator

Answer: c
Explanation: The SR flip-flop is very effective in removing the effects of switch bounce, which is the unwanted noise caused during the switching of electronic devices.

3. The truth table for an S-R flip-flop has how many VALID entries?
a) 1
b) 2
c) 3
d) 4

Answer: c
Explanation: The SR flip-flop actually has three inputs, Set, Reset and its current state. The Invalid or Undefined State occurs at both S and R being at 1.

4. When both inputs of a J-K flip-flop cycle, the output will _____
a) Be invalid
b) Change
c) Not change
d) Toggle

Answer: c
Explanation: After one cycle the value of each input comes to the same value. Eg: Assume J=0 and K=1. After 1 cycle, it becomes as J=0->1->0(1 cycle complete) and K=1->0->1(1 cycle complete). The J & K flip-flop has 4 stable states: Latch, Reset, Set and Toggle.

5. Which of the following is correct for a gated D-type flip-flop?
a) The Q output is either SET or RESET as soon as the D input goes HIGH or LOW
b) The output complement follows the input when enabled
c) Only one of the inputs can be HIGH at a time
d) The output toggles if one of the inputs is held HIGH

Answer: a
Explanation: In D flip flop, when the clock is high then the output depends on the input otherwise reminds previous output. In a state of clock high, when D is high the output Q also high, if D is '0' then output is also zero. Like SR flip-flop, the D-flip-flop also have an invalid state at both inputs being 1.

6. A basic S-R flip-flop can be constructed by cross-coupling of which basic logic gates?
a) AND or OR gates
b) XOR or XNOR gates
c) NOR or NAND gates
d) AND or NOR gates

Answer: c
Explanation: The basic S-R flip-flop can be constructed by cross coupling of NOR or NAND gates. Cross coupling means the output of second gate is fed to the input of first gate and vice-versa.

7. The logic circuits whose outputs at any instant of time depends only on the present input but also on the past outputs are called _____
a) Combinational circuits
b) Sequential circuits
c) Latches
d) Flip-flops

Answer: b
Explanation: In sequential circuits, the output signals are fed back to the input side. So, The circuits whose outputs at any instant of time depends only on the present input but also on the past outputs are called sequential circuits. Unlike sequential circuits, if output depends only on the present state, then it's known as combinational circuits.

8. Whose operations are more faster among the following?
a) Combinational circuits
b) Sequential circuits
c) Latches
d) Flip-flops

Answer: a
Explanation: Combinational circuits are often faster than sequential circuits. Since the combinational circuits do not require memory elements whereas the sequential circuits need memory devices to perform their operations in sequence. Latches and Flip-flops come under sequential circuits.

9. How many types of sequential circuits are?
a) 2
b) 3
c) 4
d) 5

Answer: a
Explanation: There are two type of sequential circuits viz., (i) synchronous or clocked and (ii) asynchronous or unclocked. Synchronous Sequential Circuits are triggered in the presence of a clock signal, whereas, Asynchronous Sequential Circuits function in the absence of a clock signal.

10. The sequential circuit is also called _____
a) Flip-flop
b) Latch
c) Strobe
d) Adder

Answer: b
Explanation: The sequential circuit is also called a latch because both are a memory cell, which are capable of storing one bit of information.

11. The basic latch consists of _____
a) Two inverters
b) Two comparators
c) Two amplifiers
d) Two adders

Answer: a
Explanation: The basic latch consists of two inverters. It is in the sense that if the output Q = 0 then the second output Q' = 1 and vice versa.

12. In S-R flip-flop, if Q = 0 the output is said to be _____
a) Set
b) Reset
c) Previous state
d) Current state

Answer: b
Explanation: In S-R flip-flop, if Q = 0 the output is said to be reset and set for Q = 1.

13. The output of latches will remain in set/reset untill _____
a) The trigger pulse is given to change the state
b) Any pulse given to go into previous state
c) They don't get any pulse more
d) The pulse is edge-triggered

Answer: a
Explanation: The output of latches will remain in set/reset untill the trigger pulse is given to change the state.

14. What is a trigger pulse?
a) A pulse that starts a cycle of operation
b) A pulse that reverses the cycle of operation
c) A pulse that prevents a cycle of operation
d) A pulse that enhances a cycle of operation

Answer: a
Explanation: Trigger pulse is defined as a pulse that starts a cycle of operation.

15. The circuits of NOR based S-R latch classified as asynchronous sequential circuits, why?
a) Because of inverted outputs
b) Because of triggering functionality
c) Because of cross-coupled connection
d) Because of inverted outputs & triggering functionality

Answer: c
Explanation: The cross-coupled connections from the output of one gate to the input of the other gate constitute a feedback path. For this reason, the circuits of NOR based S-R latch classified as asynchronous sequential circuits. Moreover, they are referred to as asynchronous because they function in the absence of a clock pulse.

This set of Digital Electronic/Circuits online quiz focuses on "Flip Flops – 2".

1. What is an ambiguous condition in a NAND based S'-R' latch?
a) S'=0, R'=1
b) S'=1, R'=0
c) S'=1, R'=1
d) S'=0, R'=0

Answer: d
Explanation: In a NAND based S-R latch, If S'=0 & R'=0 then both the outputs (i.e. Q & Q') goes HIGH and this condition is called an ambiguous/forbidden state. This state is also known as an Invalid state as the system goes into an unexpected situation.

2. In a NAND based S’-R’ latch, if S’=1 & R’=1 then the state of the latch is _____
a) No change
b) Set
c) Reset
d) Forbidden

Answer: a
Explanation: In a NAND based S’-R, latch if S’=1 & R’=1 then there is no any change in the state. It remains in its prior state. This state is used for the storage of data.

3. A NAND based S’-R’ latch can be converted into S-R latch by placing _____
a) A D latch at each of its input
b) An inverter at each of its input
c) It can never be converted
d) Both a D latch and an inverter at its input

Answer: d
Explanation: A NAND based S’-R’ latch can be converted into S-R latch by placing either a D latch or an inverter at its input as it’s operations will be complementary.

4. One major difference between a NAND based S’-R’ latch & a NOR based S-R latch is _____
a) The inputs of NOR latch are 0 but 1 for NAND latch
b) The inputs of NOR latch are 1 but 0 for NAND latch
c) The output of NAND latch becomes set if S’=0 & R’=1 and vice versa for NOR latch
d) The output of NOR latch is 1 but 0 for NAND latch

Answer: a
Explanation: Due to inverted input of NAND based S’-R’ latch, the inputs of NOR latch are 0 but 1 for NAND latch.

5. The characteristic equation of S-R latch is _____
a) Q(n+1) = (S + Q(n))R’
b) Q(n+1) = SR + Q(n)R
c) Q(n+1) = S’R + Q(n)R
d) Q(n+1) = S’R + Q'(n)R

Answer: a
Explanation: A characteristic equation is needed when a specific gate requires a specific output in order to satisfy the truth table. The characteristic equation of S-R latch is Q(n+1) = (S + Q(n))R’.

6. The difference between a flip-flop & latch is _____
a) Both are same
b) Flip-flop consist of an extra output
c) Latches has one input but flip-flop has two
d) Latch has two inputs but flip-flop has one

Answer: c
Explanation: Flip-flop is a modified version of latch. To determine the changes in states, an additional control input is provided to the latch.

7. How many types of flip-flops are?
a) 2
b) 3
c) 4
d) 5

Answer: c
Explanation: There are 4 types of flip-flops, viz., S-R, J-K, D, and T. D flip-flop is an advanced version of S-R flip-flop, while T flip-flop is an advanced version of J-K flip-flop.

8. The S-R flip flop consist of _____
a) 4 AND gates
b) Two additional AND gates

c) An additional clock input
d) 3 AND gates

Answer: b
Explanation: The S-R flip flop consists of two additional AND gates at the S and R inputs of S-R latch.

9. What is one disadvantage of an S-R flip-flop?
a) It has no Enable input
b) It has a RACE condition
c) It has no clock input
d) Invalid State

Answer: d
Explanation: The main drawback of s-r flip flop is invalid output when both the inputs are high, which is referred to as Invalid State.

10. One example of the use of an S-R flip-flop is as _____
a) Racer
b) Stable oscillator
c) Binary storage register
d) Transition pulse generator

Answer: c
Explanation: S-R refers to set-reset. So, it is used to store two values 0 and 1. Hence, it is referred to as binary storage element. It functions as memory storage during the No Change State.

11. When is a flip-flop said to be transparent?
a) When the Q output is opposite the input
b) When the Q output follows the input
c) When you can see through the IC packaging
d) When the Q output is complementary of the input

Answer: b
Explanation: Flip-flop have the property of responding immediately to the changes in its inputs. This property is called transparency.

12. On a positive edge-triggered S-R flip-flop, the outputs reflect the input condition when _____
a) The clock pulse is LOW
b) The clock pulse is HIGH
c) The clock pulse transitions from LOW to HIGH
d) The clock pulse transitions from HIGH to LOW

Answer: c
Explanation: Edge triggered device will follow when there is transition. It is a positive edge triggered when transition takes place from low to high, while, it is negative edge triggered when the transition takes place from high to low.

13. What is the hold condition of a flip-flop?
a) Both S and R inputs activated
b) No active S or R input
c) Only S is active
d) Only R is active

Answer: b
Explanation: The hold condition in a flip-flop is obtained when both of the inputs are LOW. It is the No Change State or Memory Storage state if a flip-flop.

14. If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____
a) SET
b) RESET
c) Clear

d) Invalid

Answer: b
Explanation: If S=0, R=1, the flip flop is at reset condition. Then at S=0, R=0, there is no change. So, it remains in reset. If S=1, R=0, the flip flop is at the set condition.

15. The circuit that is primarily responsible for certain flip-flops to be designated as edge-triggered is the _____
a) Edge-detection circuit
b) NOR latch
c) NAND latch
d) Pulse-steering circuit

Answer: a
Explanation: The circuit that is primarily responsible for certain flip-flops to be designated as edge-triggered is the edge-detection circuit.

This set of Digital Electronic/Circuits question bank focuses on “Flip Flops – 3”.

1. Which circuit is generated from D flip-flop due to addition of an inverter by causing reduction in the number of inputs?
a) Gated JK-latch
b) Gated SR-latch
c) Gated T-latch
d) Gated D-latch

Answer: d
Explanation: Since, both inputs of the D flip-flop are connected through an inverter. And this causes reduction in the number of inputs.

2. The characteristic of J-K flip-flop is similar to _____
a) S-R flip-flop
b) D flip-flop
c) T flip-flop
d) Gated T flip-flop

Answer: a
Explanation: In an S-R flip-flop, S refers to “SET” whereas R refers to “RESET”. The same behaviour is shown by J-K flip-flop.

3. A J-K flip-flop can be obtained from the clocked S-R flip-flop by augmenting _____
a) Two AND gates
b) Two NAND gates
c) Two NOT gates
d) Two OR gates

Answer: a
Explanation: A J-K flip-flop can be obtained from the clocked S-R flip-flop by augmenting two AND gates.

4. How is a J-K flip-flop made to toggle?
a) J = 0, K = 0
b) J = 1, K = 0
c) J = 0, K = 1
d) J = 1, K = 1

Answer: d
Explanation: When j=k=1 then the race condition is occurs that means both output wants to be HIGH. Hence, there is toggle condition is occurs, where 0 becomes 1 and 1 becomes 0. That is device is either set or reset.

5. The phenomenon of interpreting unwanted signals on J and K while Cp (clock pulse) is HIGH is called _____
a) Parity error checking
b) Ones catching
c) Digital discrimination

d) Digital filtering

Answer: b
Explanation: Ones catching means that the input transitioned to a 1 and back very briefly (unintentionally due to a glitch), but the flip-flop responded and latched it in anyway, i.e., it caught the 1. Similarly for 0's catching.

6. In J-K flip-flop, "no change" condition appears when _____
a) J = 1, K = 1
b) J = 1, K = 0
c) J = 0, K = 1
d) J = 0, K = 0

Answer: d
Explanation: If J = 0, K = 0, the output remains unchanged. This is the memory storing state.

7. A J-K flip-flop with J = 1 and K = 1 has a 20 kHz clock input. The Q output is _____
a) Constantly LOW
b) Constantly HIGH
c) A 20 kHz square wave
d) A 10 kHz square wave

Answer: d
Explanation: The flip flop is sensitive only to the positive or negative edge of the clock pulse. So, the flip-flop toggles whenever the clock is falling/rising at edge. This triggering of flip-flop during the transition state, is known as Edge-triggered flip-flop. Thus, the output curve has a time period twice that of the clock. Frequency is inversely related to time period and hence frequency gets halved.

8. What is the significance of the J and K terminals on the J-K flip-flop?
a) There is no known significance in their designations
b) The J represents "jump," which is how the Q output reacts whenever the clock goes high and the J input is also HIGH
c) The letters were chosen in honour of Jack Kilby, the inventory of the integrated circuit
d) All of the other letters of the alphabet are already in use

Answer: c
Explanation: The letters J & K were chosen in honour of Jack Kilby, the inventory of the integrated circuit. In J&K flip-flops, the invalid state problem is resolved, thus leading to the toggling of states.

9. On a J-K flip-flop, when is the flip-flop in a hold condition?
a) J = 0, K = 0
b) J = 1, K = 0
c) J = 0, K = 1
d) J = 1, K = 1

Answer: a
Explanation: At J=0 k=0 output continues to be in the same state. This is the memory storing state.

10. Two J-K flip-flops with their J-K inputs tied HIGH are cascaded to be used as counters. After four input clock pulses, the binary count is _____
a) 00
b) 11
c) 01
d) 10

Answer: a
Explanation: Every O/P repeats after its mod. Here mod is 4 (because 2 flip-flops are used. So mod = 2^2 = 4). So after 4 clock pulses the O/P repeats i.e. 00.

11. Four J-K flip-flops are cascaded with their J-K inputs tied HIGH. If the input frequency (fin) to the first flip-flop is 32 kHz, the output frequency (fout) is _____
a) 1 kHz

b) 2 kHz
c) 4 kHz
d) 16 kHz

Answer: b
Explanation: 32/2=16:-first flip-flop, 16/2=8:- second flip-flop, 8/2=4:- third flip-flop, 4/2=2:- fourth flip-flop. Since the output frequency is determined on basis of the 4^{th} flip-flop.

12. Determine the output frequency for a frequency division circuit that contains 12 flip-flops with an input clock frequency of 20.48 MHz.
a) 10.24 kHz
b) 5 kHz
c) 30.24 kHz
d) 15 kHz

Answer: b
Explanation: 12 flip flops = 2^{12} = 4096
Input Clock frequency = $20.48*10^{6}$ = 20480000
Output Clock frequency = 20480000/4096 = 5000 i.e., 5 kHz.

13. How many flip-flops are in the 7475 IC?
a) 2
b) 1
c) 4
d) 8

Answer: c
Explanation: There are 4 flip-flops used in 7475 IC and those are D flip-flops only.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “D Flip Flop”.

1. In D flip-flop, D stands for _____
a) Distant
b) Data
c) Desired
d) Delay

Answer: b
Explanation: The D of D-flip-flop stands for “data”. It stores the value on the data line.

2. The D flip-flop has _____ input.
a) 1
b) 2
c) 3
d) 4

Answer: a
Explanation: The D flip-flop has one input. The D of D-flip-flop stands for “data”. It stores the value on the data line.

3. The D flip-flop has _____ output/outputs.
a) 2
b) 3
c) 4
d) 1

Answer: a
Explanation: The D flip-flop has two outputs: Q and Q complement. The D flip-flop has one input. The D of D-flip-flop stands for “data”. It stores the value on the data line.

4. A D flip-flop can be constructed from an _____ flip-flop.
a) S-R
b) J-K
c) T

d) S-K

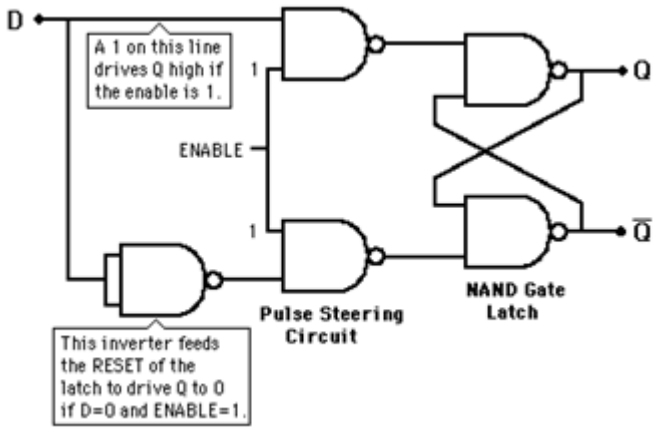
Answer: a
Explanation: A D flip-flop can be constructed from an S-R flip-flop by inserting an inverter between S and R and assigning the symbol D to the S input.

5. In D flip-flop, if clock input is LOW, the D input _____
a) Has no effect
b) Goes high
c) Goes low
d) Has effect

Answer: a
Explanation: In D flip-flop, if clock input is LOW, the D input has no effect, since the set and reset inputs of the NAND flip-flop are kept HIGH.

6. In D flip-flop, if clock input is HIGH & D=1, then output is _____
a) 0
b) 1
c) Forbidden
d) Toggle

Answer: a
Explanation: If clock input is HIGH & D=1, then output is 0. It can be observed from this diagram:



7. Which statement describes the BEST operation of a negative-edge-triggered D flip-flop?
a) The logic level at the D input is transferred to Q on NGT of CLK
b) The Q output is ALWAYS identical to the CLK input if the D input is HIGH
c) The Q output is ALWAYS identical to the D input when CLK = PGT
d) The Q output is ALWAYS identical to the D input

Answer: a
Explanation: By the truth table of D flip flop, we can observe that Q always depends on D. Hence, for every negative trigger pulse, the logic at input D is shifted to Output Q.

D Flip-flop

Symbol

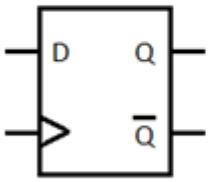


Table of truth:

clk	D	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	Q	$\overline{Q}$
1	0	0	1
1	1	1	0

8. Which of the following is correct for a gated D flip-flop?
a) The output toggles if one of the inputs is held HIGH
b) Only one of the inputs can be HIGH at a time
c) The output complement follows the input when enabled
d) Q output follows the input D when the enable is HIGH

Answer: d
Explanation: If clock is high then the D flip-flop operate and we know that input is equals to output in case of D flip-flop. It stores the value on the data line.

9. With regard to a D latch _____
a) The Q output follows the D input when EN is LOW
b) The Q output is opposite the D input when EN is LOW

c) The Q output follows the D input when EN is HIGH
d) The Q output is HIGH regardless of EN’s input state

Answer: c
Explanation: Latch is nothing but flip flop which holds the o/p or i/p state. And in D flip-flop output follows the input. It stores the value on the data line.

10. Which of the following is correct for a D latch?
a) The output toggles if one of the inputs is held HIGH
b) Q output follows the input D when the enable is HIGH
c) Only one of the inputs can be HIGH at a time
d) The output complement follows the input when enabled

Answer: b
Explanation: If the clock is HIGH then the D flip-flop operates and we know that input equals to output in case of D flip flop. It stores the value on the data line.

11. Which of the following describes the operation of a positive edge-triggered D flip-flop?
a) If both inputs are HIGH, the output will toggle
b) The output will follow the input on the leading edge of the clock
c) When both inputs are LOW, an invalid state exists
d) The input is toggled into the flip-flop on the leading edge of the clock and is passed to the output on the trailing edge of the clock

Answer: b
Explanation: Edge-triggered flip-flop means the device will change state during the rising or falling edge of the clock pulse. The main phenomenon of the D flip-flop is that the o/p will follow the i/p when the enable pin is HIGH.

12. A D flip-flop utilizing a PGT clock is in the CLEAR state. Which of the following input actions will cause it to change states?
a) CLK = NGT, D = 0
b) CLK = PGT, D = 0
c) CLOCK NGT, D = 1
d) CLOCK PGT, D = 1

Answer: d
Explanation: PGT refers to Positive Going Transition and NGT refers to negative Going Transition. Earlier, the DFF is in a clear state (output is 0). So, if D = 1 then in the next stage output will be 1 and hence the stage will be changed.

13. A positive edge-triggered D flip-flop will store a 1 when _____
a) The D input is HIGH and the clock transitions from HIGH to LOW
b) The D input is HIGH and the clock transitions from LOW to HIGH
c) The D input is HIGH and the clock is LOW
d) The D input is HIGH and the clock is HIGH

Answer: b
Explanation: A positive edge-triggered D flip-flop will store a 1 when the D input is HIGH and the clock transitions from LOW to HIGH. While a negative edge-triggered D flip-flop will store a 0 when the D input is HIGH and the clock transitions from HIGH to LOW.

14. Why do the D flip-flops receive its designation or nomenclature as ‘Data Flip-flops’?
a) Due to its capability to receive data from flip-flop
b) Due to its capability to store data in flip-flop
c) Due to its capability to transfer the data into flip-flop
d) Due to erasing the data from the flip-flop

Answer: c
Explanation: Due to its capability to transfer the data into flip-flop. D-flip-flops stores the value on the data line.

15. The characteristic equation of D-flip-flop implies that _____
a) The next state is dependent on previous state
b) The next state is dependent on present state

c) The next state is independent of previous state
d) The next state is independent of present state

Answer: d
Explanation: A characteristic equation is needed when a specific gate requires a specific output in order to satisfy the truth table. The characteristic equation of D flip-flop is given by Q(n+1) = D; which indicates that the next state is independent of the present state.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Triggering of Flip Flops”.

1. The characteristic equation of J-K flip-flop is _____
a) Q(n+1)=JQ(n)+K’Q(n)
b) Q(n+1)=J’Q(n)+KQ'(n)
c) Q(n+1)=JQ'(n)+KQ(n)
d) Q(n+1)=JQ'(n)+K’Q(n)

Answer: d
Explanation: A characteristic equation is needed when a specific gate requires a specific output in order to satisfy the truth table. The characteristic equation of J-K flip-flop is given by: Q(n+1)=JQ'(n)+K’Q(n).

2. In a J-K flip-flop, if J=K the resulting flip-flop is referred to as _____
a) D flip-flop
b) S-R flip-flop
c) T flip-flop
d) S-K flip-flop

Answer: c
Explanation: In J-K flip-flop, if both the inputs are same then it behaves like T flip-flop.

3. In J-K flip-flop, the function K=J is used to realize _____
a) D flip-flop
b) S-R flip-flop
c) T flip-flop
d) S-K flip-flop

Answer: c
Explanation: T flip-flop allows the same inputs. So, in J-K flip-flop J=K then it will work as T flip-flop.

4. The only difference between a combinational circuit and a flip-flop is that _____
a) The flip-flop requires previous state
b) The flip-flop requires next state
c) The flip-flop requires a clock pulse
d) The flip-flop depends on the past as well as present states

Answer: c
Explanation: Both flip-flop and latches are memory elements with clock/control inputs. They depend on the past as well as present states. Whereas, in case of combinational circuits, they only depend on the present state.

5. How many stable states combinational circuits have?
a) 3
b) 4
c) 2
d) 5

Answer: c
Explanation: The two stable states of combinational circuits are 1 and 0. Whereas, in flip-flops there is an additional state known as Forbidden State.

6. The flip-flop is only activated by _____
a) Positive edge trigger
b) Negative edge trigger
c) Either positive or Negative edge trigger

d) Sinusoidal trigger

Answer: c
Explanation: Flip flops can be activated with either a positive or negative edge trigger.

7. The S-R latch composed of NAND gates is called an active low circuit because _____
a) It is only activated by a positive level trigger
b) It is only activated by a negative level trigger
c) It is only activated by either a positive or negative level trigger
d) It is only activated by sinusoidal trigger

Answer: b
Explanation: Active low indicates that only an input value of 0 sets or resets the circuit.

8. Both the J-K & the T flip-flop are derived from the basic _____
a) S-R flip-flop
b) S-R latch
c) D latch
d) D flip-flop

Answer: b
Explanation: The SR latch is the basic block for the D latch/flip flop from which the JK and T flip flops are derived. A latch is similar to a flip-flop, only without a clock input.

9. The flip-flops which has not any invalid states are _____
a) S-R, J-K, D
b) S-R, J-K, T
c) J-K, D, S-R
d) J-K, D, T

Answer: d
Explanation: Unlike the SR latch, these circuits have no invalid states. The SR latch or flip-flop has an invalid or forbidden state where no output could be determined.

10. What does the triangle on the clock input of a J-K flip-flop mean?
a) Level enabled
b) Edge triggered
c) Both Level enabled & Edge triggered
d) Level triggered

Answer: b
Explanation: The triangle on the clock input of a J-K flip-flop mean edge triggered. Whereas the absence of triangle symbol implies that the flip-flop is level-triggered.

11. What does the circle on the clock input of a J-K flip-flop mean?
a) Level enabled
b) Positive edge triggered
c) negative edge triggered
d) Level triggered

Answer: c
Explanation: The circle on the clock input of a J-K flip-flop mean negative edge triggered. Whereas the absence of triangle symbol implies that the flip-flop is level-triggered.

12. What does the direct line on the clock input of a J-K flip-flop mean?
a) Level enabled
b) Positive edge triggered
c) negative edge triggered
d) Level triggered

Answer: d
Explanation: The direct line on the clock input of a J-K flip-flop mean level triggered. Whereas the presence of triangle symbol implies that the flip-flop is edge-triggered.

13. What does the half circle on the clock input of a J-K flip-flop mean?
a) Level enabled

b) Positive edge triggered
c) negative edge triggered
d) Level triggered

Answer: d
Explanation: The half circle on the clock input of a J-K flip-flop mean level triggered. Whereas the presence of triangle symbol implies that the flip-flop is edge-triggered.

14. A J-K flip-flop with J = 1 and K = 1 has a 20 kHz clock input. The Q output is _____
a) Constantly LOW
b) Constantly HIGH
c) A 20 kHz square wave
d) A 10 kHz square wave

Answer: d
Explanation: As one flip flop is used so there are two states available. So, 20/2 = 10Hz frequency is available at the output.

15. On a positive edge-triggered S-R flip-flop, the outputs reflect the input condition when _____
a) The clock pulse is LOW
b) The clock pulse is HIGH
c) The clock pulse transitions from LOW to HIGH
d) The clock pulse transitions from HIGH to LOW

Answer: c
Explanation: Edge triggered device will follow the input condition when there is a transition. It is said to be positive edge triggered when transition occurs from LOW to HIGH. While it is said to be a negative edge triggered when a transition occurs from HIGH to LOW.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Master-Slave Flip-Flops”.

1. The asynchronous input can be used to set the flip-flop to the _____
a) 1 state
b) 0 state
c) either 1 or 0 state
d) forbidden State

Answer: c
Explanation: The asynchronous input can be used to set the flip-flop to the 1 state or clear the flip-flop to the 0 state at any time, regardless of the condition at the other inputs.

2. Input clock of RS flip-flop is given to _____
a) Input
b) Pulser
c) Output
d) Master slave flip-flop

Answer: b
Explanation: Pulser behaves like an arithmetic operator, to perform the operation or determination of corresponding states.

3. D flip-flop is a circuit having _____
a) 2 NAND gates
b) 3 NAND gates
c) 4 NAND gates
d) 5 NAND gates

Answer: c
Explanation: D flip-flop is a circuit having 4 NAND gates. Two of them are connected with each other.

4. In JK flip flop same input, i.e. at a particular time or during a clock pulse, the output will oscillate back and forth between 0 and 1. At the end of the clock pulse the value of output Q is uncertain. The situation is referred to as?

a) Conversion condition
b) Race around condition
c) Lock out state
d) Forbidden State

Answer: b
Explanation: A race around condition is a flaw in an electronic system or process whereby the output and result of the process is unexpectedly dependent on the sequence or timing of other events.

5. Master slave flip flop is also referred to as?
a) Level triggered flip flop
b) Pulse triggered flip flop
c) Edge triggered flip flop
d) Edge-Level triggered flip flop

Answer: b
Explanation: The term pulse triggered means the data is entered on the rising edge of the clock pulse, but the output does not reflect the change until the falling edge of the clock pulse.

6. In a positive edge triggered JK flip flop, a low J and low K produces?
a) High state
b) Low state
c) Toggle state
d) No Change State

Answer: d
Explanation: In JK Flip Flop if J = K = 0 then it holds its current state. There will be no change.

7. If one wants to design a binary counter, the preferred type of flip-flop is _____
a) D type
b) S-R type
c) Latch
d) J-K type

Answer: d
Explanation: If one wants to design a binary counter, the preferred type of flip-flop is J-K type because it has capability to recover from toggle condition. SR flip-flop is not suitable as it produces the “Invalid State”.

8. S-R type flip-flop can be converted into D type flip-flop if S is connected to R through _____
a) OR Gate
b) AND Gate
c) Inverter
d) Full Adder

Answer: c
Explanation: S-R type flip-flop can be converted into D type flip-flop if S is connected to R through an Inverter gate.

9. Which of the following flip-flops is free from the race around the problem?
a) T flip-flop
b) SR flip-flop
c) Master-Slave Flip-flop
d) D flip-flop

Answer: a
Explanation: T flip-flop is free from the race around condition because its output depends only on the input; hence there is no any problem creates as like toggle.

10. Which of the following is the Universal Flip-flop?
a) S-R flip-flop
b) J-K flip-flop
c) Master slave flip-flop

d) D Flip-flop

Answer: b
Explanation: There are lots of flip-flops can be prepared by using J-K flip-flop. So, the name is a universal flip-flop. Also, the JK flip-flop resolves the Forbidden State.

11. How many types of triggering take place in a flip flops?
a) 3
b) 2
c) 4
d) 5

Answer: a
Explanation: There are three types of triggering in a flip-flop, viz., level triggering, edge triggering and pulse triggering.

12. Flip-flops are _____
a) Stable devices
b) Astable devices
c) Bistable devices
d) Monostable devices

Answer: c
Explanation: Flip-flops are synchronous bistable devices known as bistable multivibrators as they have 2 stable states.

13. The term synchronous means _____
a) The output changes state only when any of the input is triggered
b) The output changes state only when the clock input is triggered
c) The output changes state only when the input is reversed
d) The output changes state only when the input follows it

Answer: b
Explanation: The term synchronous means the output changes state only when the clock input is triggered. That is, changes in the output occur in synchronization with the clock.

14. The S-R, J-K and D inputs are called _____
a) Asynchronous inputs
b) Synchronous inputs
c) Bidirectional inputs
d) Unidirectional inputs

Answer: b
Explanation: The S-R, J-K and D inputs are called synchronous inputs because data on these inputs are transferred to the flip-flop’s output only on the triggering edge or level triggering of the clock pulse. Moreover, flip-flops have a clock input whereas latches don’t. Hence, known as synchronous inputs.

15. The circuit that generates a spike in response to a momentary change of input signal is called _____
a) R-C differentiator circuit
b) L-R differentiator circuit
c) R-C integrator circuit
d) L-R integrator circuit

Answer: a
Explanation: The circuit that generates a spike in response to a momentary change of input signal is called R-C differentiator circuit.

This set of Digital Electronic/Circuits Questions & Answers for entrance exams focuses on “Realisation of one Flip-flop using other Flip-flops”.

1. To realise one flip-flop using another flip-flop along with a combinational circuit, known as _____
a) PREVIOUS state decoder
b) NEXT state decoder

c) MIDDLE state decoder
d) PRESENT state decoder

Answer: b
Explanation: To realise one flip-flop using another flip-flop along with a combinational circuit, known as NEXT state decoder which acts as like a flip-flop.

2. For realisation of JK flip-flop from SR flip-flop, the input J and K will be given as _____
a) External inputs to S and R
b) Internal inputs to S and R
c) External inputs to combinational circuit
d) Internal inputs to combinational circuit

Answer: a
Explanation: If a JK Flip Flop is required, the inputs are given to the combinational circuit and the output of the combinational circuit is connected to the inputs of the actual flip flop. So, J and K will be given as external inputs to S and R. As SR flip-flop have invalid state and JK flip-flop don't.

3. For realisation of JK flip-flop from SR flip-flop, if J=0 & K=0 then the input is _____
a) S=0, R=0
b) S=0, R=X
c) S=X, R=0
d) S=X, R=X

Answer: b
Explanation: If J=0 & K=0, the output will be as: Q(n)=0, Q(n+1)=0 and it is fed into both the AND gates which results as S=0 & R=X(i.e. don't care).

FF data inputs		*Output*	*S-R FF inputs*	
J	*K*	*Q*	*S*	*R*
0	0	0	0	X
0	1	0	0	X
1	0	0	1	0
1	1	0	1	0
0	1	1	0	1
1	1	1	0	1
0	0	1	X	0
1	0	1	X	0

4. For realisation of JK flip-flop from SR flip-flop, if J=1, K=0 & present state is 0(i.e. Q(n)=0) then excitation input will be _____
a) S=0, R=1
b) S=X, R=0
c) S=1, R=0
d) S=1, R=1

Answer: c
Explanation: If J=1, K=0 & present state is 0(i.e. Q(n)=0) then next state will be 1 which results excitation inputs as S=1 & R=0.

FF data inputs		*Output*	*S-R FF inputs*	
J	*K*	*Q*	*S*	*R*
0	0	0	0	X
0	1	0	0	X
1	0	0	1	0
1	1	0	1	0
0	1	1	0	1
1	1	1	0	1
0	0	1	X	0
1	0	1	X	0

5. For realisation of SR flip-flop from JK flip-flop, the excitation input will be obtained from _____
a) S and R
b) R input
c) J and K input
d) D input

Answer: c
Explanation: It is the reverse process of SR flip-flop to JK flip-flop. So, for realisation of SR flip-flop from JK flip-flop, the excitation input will be obtained from J and K.

6. For realisation of SR flip-flop from JK flip-flop, if S=1, R=0 & present state is 0 then next state will be _____
a) 1
b) 0
c) Don’t care
d) Toggle

Answer: a
Explanation: For JK flip-flop to SR flip-flop, if S=1, R=0 & present state is 0 then next state will be 1 because next stage is complement of present stage.

S-R Inputs		Outputs		J-K Inputs	
S	R	Qn	Qn+1	J	K
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	X	1
1	0	0	1	1	X
1	0	1	1	X	0
1	1	Invalid		Dont care	
1	1	Invalid		Dont care	

7. For realisation of SR flip-flop from JK flip-flop, if S=1, R=0 & present state is 0 then the excitation input will be _____
a) J=1, K=1

b) J=X, K=1
c) J=1, K=X
d) J=0, K=0

Answer: c
Explanation: For realisation of SR flip-flop from JK flip-flop, if S=1, R=0 & present state is 0 then the excitation input will be J=1, K=X.

S-R Inputs		Outputs		J-K Inputs	
S	R	Qn	Qn+1	J	K
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	X	1
1	0	0	1	1	X
1	0	1	1	X	0
1	1	Invalid		Dont care	
1	1	Invalid		Dont care	

8. The K-map simplification for realisation of SR flip-flop from JK flip-flop is _____
a) J=1, K=0
b) J=R, K=S
c) J=S, K=R
d) J=0, K=1

Answer: c
Explanation: The K-map simplification for realisation of SR flip-flop from JK flip-flop is given by: J=S, K=R.

9. For realisation of D flip-flop from SR flip-flop, the external input is given through _____
a) S
b) R
c) D
d) Both S and R

Answer: c
Explanation: For realisation of D flip-flop from SR flip-flop, S and R are the actual inputs of the flip flop which is connected together via NOT gate and it is called external input as D.

10. For D flip-flop to JK flip-flop, the characteristics equation is given by _____
a) D=JQ(p)'+Q(p)K'
b) D=JQ(p)'+KQ(p)'
c) D=JQ(p)+Q(p)K'
d) D=J'Q(p)+Q(p)K

Answer: a
Explanation: A characteristic equation is needed when a specific gate requires a specific output in order to satisfy the truth table. For D flip-flop to JK flip-flop, the characteristics equation is given by D=JQ(p)'+Q(p)K'.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on "Counters".

1. In digital logic, a counter is a device which _____
a) Counts the number of outputs
b) Stores the number of times a particular event or process has occurred
c) Stores the number of times a clock pulse rises and falls
d) Counts the number of inputs

Answer: b
Explanation: In digital logic and computing, a counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal.

2. A counter circuit is usually constructed of _____
a) A number of latches connected in cascade form
b) A number of NAND gates connected in cascade form
c) A number of flip-flops connected in cascade
d) A number of NOR gates connected in cascade form

Answer: c
Explanation: A counter circuit is usually constructed of a number of flip-flops connected in cascade. Preferably, JK Flip-flops are used to construct counters and registers.

3. What is the maximum possible range of bit-count specifically in n-bit binary counter consisting of 'n' number of flip-flops?
a) 0 to 2^n
b) 0 to $2^n + 1$
c) 0 to $2^n - 1$
d) 0 to $2^{n+1/2}$

Answer: c
Explanation: The maximum possible range of bit-count specifically in n-bit binary counter

consisting of ‘n’ number of flip-flops is 0 to 2^n -1. For say, there is a 2-bit counter, then it will count till 2^2 -1 = 3. Thus, it will count from 0 to 3.

4. How many types of the counter are there?
a) 2
b) 3
c) 4
d) 5

Answer: b
Explanation: Counters are of 3 types, namely, (i)asynchronous/synchronous, (ii)single and multi-mode & (iii)modulus counter. These further can be subdivided into Ring Counter, Johnson Counter, Cascade Counter, Up/Down Counter and such like.

5. A decimal counter has _____ states.
a) 5
b) 10
c) 15
d) 20

Answer: b
Explanation: Decimal counter is also known as 10 stage counter. So, it has 10 states. It is also known as Decade Counter counting from 0 to 9.

6. Ripple counters are also called _____
a) SSI counters
b) Asynchronous counters
c) Synchronous counters
d) VLSI counters

Answer: b
Explanation: Ripple counters are also called asynchronous counter. In Asynchronous counters, only the first flip-flop is connected to an external clock while the rest of the flip-flops have their preceding flip-flop output as clock to them.

7. Synchronous counter is a type of _____
a) SSI counters
b) LSI counters
c) MSI counters
d) VLSI counters

Answer: c
Explanation: Synchronous Counter is a Medium Scale Integrated (MSI). In Synchronous Counters, the clock pulse is supplied to all the flip-flops simultaneously.

8. Three decade counter would have _____
a) 2 BCD counters
b) 3 BCD counters
c) 4 BCD counters
d) 5 BCD counters

Answer: b
Explanation: Three decade counter has 30 states and a BCD counter has 10 states. So, it would require 3 BCD counters. Thus, a three decade counter will count from 0 to 29.

9. BCD counter is also known as _____
a) Parallel counter
b) Decade counter
c) Synchronous counter
d) VLSI counter

Answer: b
Explanation: BCD counter is also known as decade counter because both have the same number of stages and both count from 0 to 9.

10. The parallel outputs of a counter circuit represent the _____
a) Parallel data word
b) Clock frequency
c) Counter modulus
d) Clock count

Answer: d
Explanation: The parallel outputs of a counter circuit represent the clock count. A counter counts the number of times an event takes place in accordance to the clock pulse.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Asynchronous Down Counter”.

1. Which of the following statements are true?
a) Asynchronous events does not occur at the same time
b) Asynchronous events are controlled by a clock
c) Synchronous events does not need a clock to control them
d) Only asynchronous events need a control clock

Answer: a
Explanation: Asynchronous events does not occur at the same time because of propagation delay and they do need a clock pulse to trigger them. Whereas, synchronous events occur in presence of clock pulse.

2. A down counter using n-flip-flops count _____
a) Downward from a maximum count
b) Upward from a minimum count
c) Downward from a minimum to maximum count
d) Toggles between Up and Down count

Answer: a
Explanation: As the name suggests down counter means counting occurs from a higher value to lower value (i.e. (2^n – 1) to 0).

3. UP Counter is _____
a) It counts in upward manner
b) It count in down ward manner
c) It counts in both the direction
d) Toggles between Up and Down count

Answer: a

Explanation: UP counter counts in an upward manner from 0 to (2^n – 1).

4. DOWN counter is _____
a) It counts in upward manner
b) It count in downward manner
c) It counts in both the direction
d) Toggles between Up and Down count

Answer: b

Explanation: DOWN counter counts in a downward manner from (2^n – 1) to 0.

5. How many different states does a 3-bit asynchronous down counter have?
a) 2
b) 4
c) 6
d) 8

Answer: d

Explanation: In a n-bit counter, the total number of states = 2^n .

Therefore, in a 3-bit counter, the total number of states = 2^3 = 8 states.

6. In a down counter, which flip-flop doesn’t toggle when the inverted output of the preceeding flip-flop goes from HIGH to LOW.

a) MSB flip-flop
b) LSB flip-flop
c) Master slave flip-flop
d) Latch

Answer: b
Explanation: Since the LSB flip-flop changes its state at each negative transition of clock. That is why LSB flip-flop doesn’t have toggle.

7. In a 3-bit asynchronous down counter, the initial content is _____
a) 000
b) 111
c) 010
d) 101

Answer: a
Explanation: Initially, all the flip-flops are RESET. So, the initial content is 000. At the first negative transition of the clock, the counter content becomes 101.

8. In a 3-bit asynchronous down counter, at the first negative transition of the clock, the counter content becomes _____
a) 000
b) 111
c) 101
d) 010

Answer: b
Explanation: Since, in the down counter, the counter content is decremented by 1 for every negative transition. Hence, in a 3-bit asynchronous down counter, at the first negative transition of the clock, the counter content becomes 111.

9. In a 3-bit asynchronous down counter, at the first negative transition of the clock, the counter content becomes _____
a) 000
b) 111
c) 101
d) 010

Answer: c
Explanation: Since, in the down counter, the counter content is decremented by 1 for every negative transition. Hence, in a 3-bit asynchronous down counter, at the first negative transition of the clock, the counter content becomes 101.

10. The hexadecimal equivalent of 15,536 is _____
a) 3CB0
b) 3C66
c) 63C0
d) 6300

Answer: a
Explanation: You just divide the number by 16 at the end and store the remainder from bottom to top.

11. In order to check the CLR function of a counter _____
a) Apply the active level to the CLR input and check all of the Q outputs to see if they are all in their reset state
b) Ground the CLR input and check to be sure that all of the Q outputs are LOW
c) Connect the CLR input to Vcc and check to see if all of the Q outputs are HIGH
d) Connect the CLR to its correct active level while clocking the counter; check to make sure that all of the Q outputs are toggling

Answer: a
Explanation: CLR stands for clearing or resetting all states of flip-flop. In order to check the CLR function of a counter, apply the active level to the CLR input and check all of the Q outputs to see if they are all in their reset state.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Asynchronous Counter”.

1. How many natural states will there be in a 4-bit ripple counter?
a) 4
b) 8
c) 16
d) 32

Answer: c

Explanation: In an n-bit counter, the total number of states = 2^n .

Therefore, in a 4-bit counter, the total number of states = 2^4 = 16 states.

2. A ripple counter’s speed is limited by the propagation delay of _____
a) Each flip-flop
b) All flip-flops and gates
c) The flip-flops only with gates
d) Only circuit gates

Answer: a
Explanation: A ripple counter is something that is derived by other flip-flops. It’s like a series of Flip Flops. Output of one FF becomes the input of the next. Because ripple counter is composed of FF only and no gates are there other than FF, so only propagation delay of FF will be taken into account. Propagation delay refers to the amount of time taken in producing an output when the input is altered.

3. One of the major drawbacks to the use of asynchronous counters is that _____
a) Low-frequency applications are limited because of internal propagation delays
b) High-frequency applications are limited because of internal propagation delays
c) Asynchronous counters do not have major drawbacks and are suitable for use in high- and low-frequency counting applications
d) Asynchronous counters do not have propagation delays, which limits their use in high-frequency applications

Answer: b
Explanation: One of the major drawbacks to the use of asynchronous counters is that High-frequency applications are limited because of internal propagation delays. Propagation delay refers to the amount of time taken in producing an output when the input is altered.

4. Internal propagation delay of asynchronous counter is removed by _____
a) Ripple counter
b) Ring counter
c) Modulus counter
d) Synchronous counter

Answer: d
Explanation: Propagation delay refers to the amount of time taken in producing an output when the input is altered. Internal propagation delay of asynchronous counter is removed by synchronous counter because clock input is given to each flip-flop individually in synchronous counter.

5. What happens to the parallel output word in an asynchronous binary down counter whenever a clock pulse occurs?
a) The output increases by 1
b) The output decreases by 1
c) The output word increases by 2
d) The output word decreases by 2

Answer: b

Explanation: In an asynchronous counter, there isn’t any clock input. The output of 1 st flip-flop is given to second flip-flop as clock input. So, in case of binary down counter the output word decreases by 1.

6. How many flip-flops are required to construct a decade counter?
a) 4
b) 8
c) 5
d) 10

Answer: a
Explanation: Number of flip-flop required is calculated by this formula: $2^{(n-1)} <= N <= 2^n$. $2^4 = 16$ and $2^3 = 8$, therefore, 4 flip flops needed.

7. The terminal count of a typical modulus-10 binary counter is _____
a) 0000
b) 1010
c) 1001
d) 1111

Answer: c
Explanation: A binary counter counts or produces the equivalent binary number depending on the cycles of the clock input. Modulus-10 means count from 0 to 9. So, the terminal count is 9 (1001).

8. How many different states does a 3-bit asynchronous counter have?
a) 2
b) 4
c) 8
d) 16

Answer: c
Explanation: In a n-bit counter, the total number of states = 2^n .
Therefore, in a 3-bit counter, the total number of states = $2^3 = 8$ states.

9. A 5-bit asynchronous binary counter is made up of five flip-flops, each with a 12 ns propagation delay. The total propagation delay (tp(total)) is _____
a) 12 ms
b) 24 ns
c) 48 ns
d) 60 ns

Answer: d
Explanation: Since a counter is constructed using flip-flops, therefore, the propagation delay in the counter occurs only due to the flip-flops. Each bit has propagation delay = 12ns. So, 5 bits = 12ns * 5 = 60ns.

10. An asynchronous 4-bit binary down counter changes from count 2 to count 3. How many transitional states are required?
a) 1
b) 2
c) 8
d) 15

Answer: d
Explanation: Transitional state is given by $(2^n - 1)$. Since, it's a 4-bit counter, therefore, transition states = $2^4 - 1 = 15$. So, total transitional states are 15.

11. A 4-bit ripple counter consists of flip-flops, which each have a propagation delay from clock to Q output of 15 ns. For the counter to recycle from 1111 to 0000, it takes a total of _____
a) 15 ns
b) 30 ns
c) 45 ns
d) 60 ns

Answer: d
Explanation: Since a counter is constructed using flip-flops, therefore, the propagation delay in the counter occurs only due to the flip-flops. One bit change is 15 ns, so 4-bit change = 15 * 4 = 60.

12. Three cascaded decade counters will divide the input frequency by _____
a) 10
b) 20
c) 100
d) 1000

Answer: d
Explanation: Decade counter has 10 states. So, three decade counters are cascaded i.e. 10*10*10=1000 states.

13. A ripple counter's speed is limited by the propagation delay of _____
a) Each flip-flop
b) All flip-flops and gates
c) The flip-flops only with gates
d) Only circuit gates

Answer: a
Explanation: A ripple counter is something that is derived by other flip-flops. Its like a series of Flip Flops. Output of one FF becomes the input of the next. Because ripple counter is composed of FF only and no gates are there other than FF, so only propagation delay of FF will be taken into account. Propagation delay refers to the amount of time taken in producing an output when the input is altered.

14. A 4-bit counter has a maximum modulus of _____
a) 3
b) 6
c) 8
d) 16

Answer: d
Explanation: In a n-bit counter, the total number of states = 2^n .
Therefore, in a 4-bit counter, the total number of states = 2^4 = 16 states.

15. A principle regarding most display decoders is that when the correct input is present, the related output will switch _____
a) HIGH
b) To high impedance
c) To an open
d) LOW

Answer: d
Explanation: A principle regarding most display decoders is that when the correct input is present, the related output will switch LOW. Since it's an active-low device.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on "Counter ICs".

1. What is the difference between a 7490 and a 7493?
a) 7490 is a MOD-10, 7493 is a MOD-16
b) 7490 is a MOD-16, 7493 is a MOD-10
c) 7490 is a MOD-12, 7493 is a MOD-16
d) 7490 is a MOD-10, 7493 is a MOD-12

Answer: a
Explanation: The difference between a 7490 and a 7493 is that 7490 is a MOD-10, 7493 is a MOD-16 counter. Thus, 7490 traverses 10 states and 7493 traverses 16 states.

2. How many different states does a 2-bit asynchronous counter have?
a) 1
b) 4

c) 2
d) 8

Answer: b

Explanation: For a n-bit counter, total number of states = 2^n . Thus, for 2-bit counter, total number of states = 2^2 = 4.

3. A 12 MHz clock frequency is applied to a cascaded counter containing a modulus-5 counter, a modulus-8 counter, and a modulus-10 counter. The lowest output frequency possible is _____

a) 10 kHz
b) 20 kHz
c) 30 kHz
d) 60 kHz

Answer: c
Explanation: Cascaded counter containing a modulus-5 counter, a modulus-8 counter, and a modulus-10 counter. So, 5*8*10=400. Applied clock frequency = 12 MHz; hence, the lowest output frequency possible is 12MHz/400=30 kHz.

4. Which one is a 4-bit binary ripple counter?
a) IC 7493
b) IC 7490
c) IC 7491
d) IC 7492

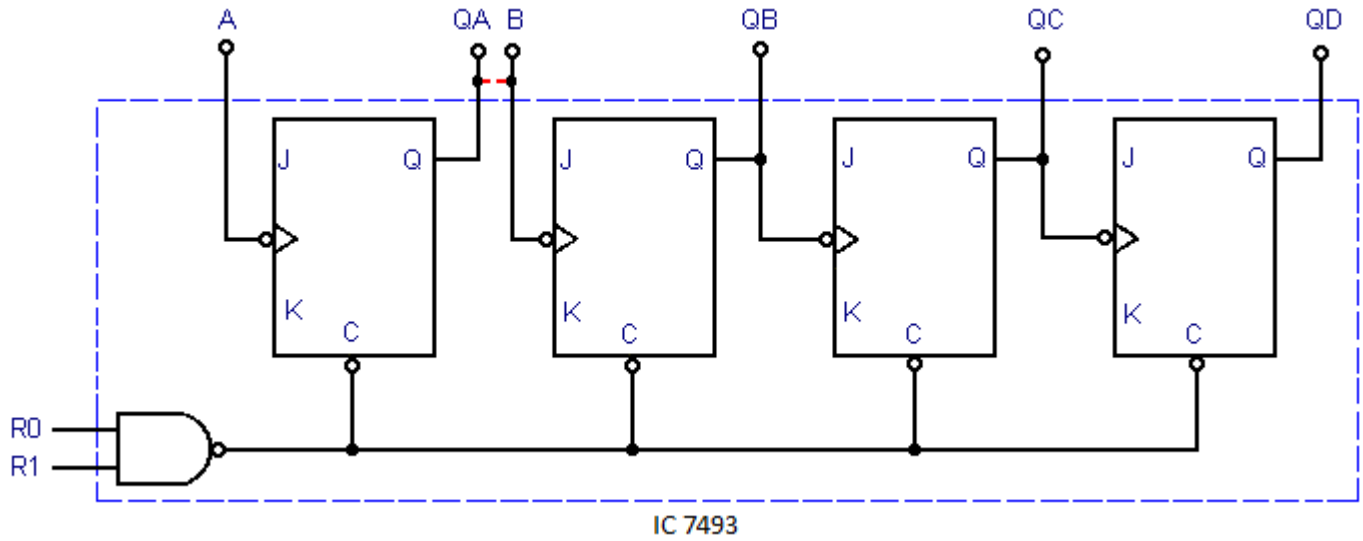
Answer: b

Explanation: IC 7493 is a 4-bit binary ripple counter. It is a MOD-16 counter with 2^4 = 16 states.

5. IC 7493 consist of _____
a) 4 S-R flip-flop
b) 4 J-K flip-flop
c) 4 master-slave flip-flop
d) 4 D flip-flop

Answer: c

Explanation: IC 7493 consist of 4 J-K master-slave flip-flop. It is a MOD-16 counter with 2^4 = 16 states.

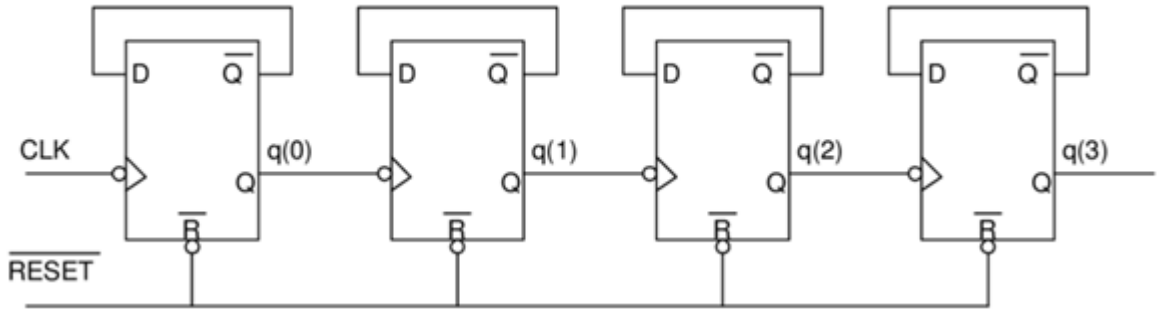


6. A reset input is used in IC 7493, why?
a) For increment of bit by 1
b) For decrement of bit by 1
c) For reset the counter
d) For setting the counter

Answer: c
Explanation: The reset inputs are used to reset the counter to 0000.

7. In a 4-bit binary ripple counter, four master-slave flip-flops are internally connected to provide a _____ bit counter.
a) Divide-by-2 & divide-by-6
b) Divide-by-6 & divide-by-8
c) Divide-by-2 & divide-by-8
d) Divide-by-4 & divide-by-8

Answer: c
Explanation: In a 4-bit binary ripple counter, four master-slave flip-flops are internally connected to provide a Divide-by-2 & divide-by-8 bit counter.



8. Which of the following is a decade counter?
a) IC 7493
b) IC 7490
c) IC 7491
d) IC 7492

Answer: b
Explanation: IC 7490 is called as decade counter or MOD-10. Thus, it has 10 states.

9. In a 4-bit decade counter, four master-slave flip-flops are internally connected to provide a _____ bit counter.
a) Divide-by-2 & divide-by-6
b) Divide-by-6 & divide-by-8
c) Divide-by-2 & divide-by-5
d) Divide-by-4 & divide-by-8

Answer: c
Explanation: In a decade counter, four master-slave flip-flops are internally connected to provide a Divide-by-2 & divide-by-5 bit counter.

10. Reset inputs are used in IC 7490, why?
a) For increment of bit by 1
b) For decrement of bit by 1
c) For reset the counter
d) For setting the counter

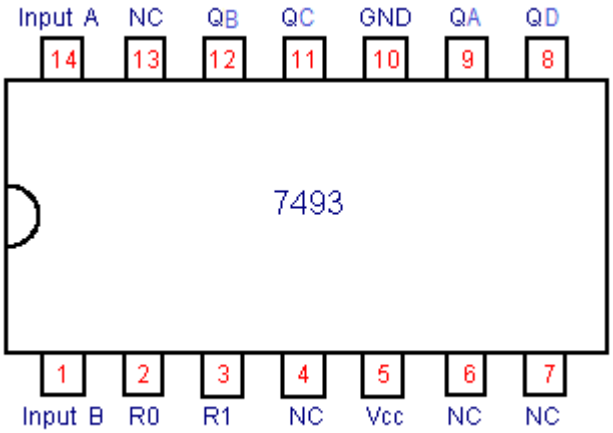
Answer: c
Explanation: The reset inputs are used to reset the counter to 0000.

11. The set inputs are used in a decade counter, why?
a) To set the counter to 0011
b) To set the counter to 1000
c) To set the counter to 1001
d) To set the counter to 0001

Answer: c
Explanation: The set inputs are used in a decade counter to set the counter to 1001 which is 9 in decimal, as a decade counter counts from 0 to 9.

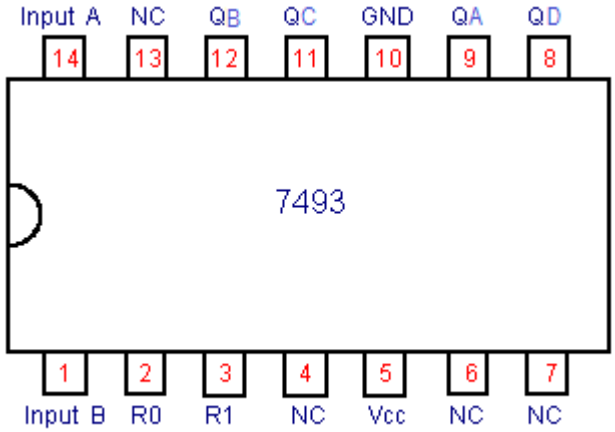
12. List which pins need to be connected together on a 7493 to make a MOD-12 counter.
a) 12 to 1, 11 to 3, 9 to 2
b) 12 to 1, 11 to 3, 12 to 2
c) 12 to 1, 11 to 3, 8 to 2
d) 12 to 1, 11 to 3, 1 to 2

Answer: c
Explanation: IC-7493 is a MOD-16 counter. So maximum, it can have 16 states. A MOD-12 counter will have 12-states. Thus, it is clear from the diagram shown below: 12 & 1 are clear pins, 11 & 3 are clock pins, 8 & 2 are input for 7493 FF.



13. Ripple counter IC has _____
a) 10 pins
b) 11 pins
c) 12 pins
d) 14 pins

Answer: d
Explanation: A ripple counter is of 4-bit and has 4 J-K flip-flops. Ripple counter IC has 14 pins.



14. Integrated-circuit counter chips are used in numerous applications including _____
a) Timing operations, counting operations, sequencing, and frequency multiplication
b) Timing operations, counting operations, sequencing, and frequency division
c) Timing operations, decoding operations, sequencing, and frequency multiplication
d) Data generation, counting operations, sequencing, and frequency multiplication

Answer: b
Explanation: There are no integrated circuit counter chips employed for frequency multiplication. In the rest of the options, frequency multiplication is mentioned which is not related to counters in anyway. So, they are not the correct answers. Thus, counters are used for timing operations, counting operations, sequencing and frequency division.

15. What is the difference between 7490 and a 7492?
a) 7490 is a MOD-12, 7492 is a MOD-10
b) 7490 is a MOD-12, 7492 is a MOD-16

c) 7490 is a MOD-16, 7492 is a MOD-10
d) 7490 is a MOD-10, 7492 is a MOD-12

Answer: d
Explanation: From the properties of both ICs, we have 7490 is a MOD-10, 7492 is a MOD-12. Thus, IC-7490 can have maximum 10 states, while IC-7492 can have maximum 12 states.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Counter Implementation and Applications”.

1. A ripple counter’s speed is limited by the propagation delay of _____
a) Each flip-flop
b) All flip-flops and gates
c) The flip-flops only with gates
d) Only circuit gates

Answer: a
Explanation: A ripple counter is something that is derived by other flip-flops. It’s like a series of Flip Flops. The output of one FF becomes the input of the next. Because ripple counter is composed of FF only and no gates are there other than FF, so only propagation delay of FF will be taken into account. Propagation delay refers to the amount of time taken in producing an output when the input is altered.

2. A 5-bit asynchronous binary counter is made up of five flip-flops, each with a 12 ns propagation delay. The total propagation delay (tp(tot)) is _____
a) 12 ms
b) 24 ns
c) 48 ns
d) 60 ns

Answer: d
Explanation: Since a counter is constructed using flip-flops, therefore, the propagation delay in the counter occurs only due to the flip-flops. Each bit has propagation delay = 12ns. So, 5 bits = 12ns * 5 = 60ns.

3. A 4-bit ripple counter consists of flip-flops, which each have a propagation delay from clock to Q output of 15 ns. For the counter to recycle from 1111 to 0000, it takes a total of _____
a) 15 ns
b) 30 ns
c) 45 ns
d) 60 ns

Answer: d
Explanation: Since a counter is constructed using flip-flops, therefore, the propagation delay in the counter occurs only due to the flip-flops. Each bit has propagation delay = 15ns. So, 4 bits = 15ns * 4 = 60ns.

4. A ripple counter’s speed is limited by the propagation delay of _____
a) Each flip-flop
b) All flip-flops and gates
c) The flip-flops only with gates
d) Only circuit gates

Answer: a
Explanation: A ripple counter is something that is derived by other flip-flops. Its like a series of Flip Flops. Output of one FF becomes the input of the next. Because ripple counter is composed of FF only and no gates are there other than FF, so only propagation delay of FF will be taken into account. Propagation delay refers to the amount of time taken in producing an output when the input is altered.

5. What is the maximum delay that can occur if four flip-flops are connected as a ripple counter and each flip-flop has propagation delays of tPHL = 22 ns and tPLH = 15 ns?
a) 15 ns
b) 22 ns
c) 60 ns

d) 88 ns

Answer: d
Explanation: Maximum propagation delay is the longest delay between an input changing value and the output changing value. Hence, 22 * n = 22*4 (Since there are 4 FFs) = 88ns.

6. The main drawback of a ripple counter is that _____
a) It has a cumulative settling time
b) It has a distributive settling time
c) It has a productive settling time
d) It has an associative settling time

Answer: a
Explanation: The main drawback of a ripple counter is that it has a cumulative settling time (i.e. another bit is transmitted just after one consequently).

7. A 4 bit modulo-16 ripple counter uses JK flip-flops. If the propagation delay of each flip-flop is 50 nsec, the maximum clock frequency that can be used is equal to _____
a) 20 MHz
b) 10 MHz
c) 5 MHz
d) 4 MHz

Answer: c
Explanation: Since a counter is constructed using flip-flops, therefore, the propagation delay in the counter occurs only due to the flip-flops. Each bit has propagation delay = 50ns. So, 4 bits or FFs = 50ns * 4 = 200ns. Clock frequency = 1/200ns = 5 MHz.

8. As the number of flip flops are increased, the total propagation delay of _____
a) Ripple counter increases but that of synchronous counter remains the same
b) Both ripple and synchronous counters increase
c) Both ripple and synchronous counters remain the same
d) Ripple counter remains the same but that of synchronous counter increases

Answer: a
Explanation: In ripple counter, the clock pulses are applied to one flip-flop only. Hence, as the number of flip-flops increases the delay increases. In the synchronous counter, clock pulses to all flip-flops are applied simultaneously.

9. A reliable method for eliminating decoder spikes is the technique called _____
a) Strobing
b) Feeding
c) Wagging
d) Waving

Answer: a
Explanation: A reliable method for eliminating decoder spikes is the technique called strobing. A strobe signal validates the availability of data on consecutive parallel lines.

10. A glitch that appears on the decoded output of a ripple counter is often difficult to see on an oscilloscope because of _____
a) It is a random event
b) It occurs less frequently than the normal decoded output
c) It is very fast
d) All of the Mentioned

Answer: d
Explanation: A glitch is a transition that occurs before a signal settles to a specific value. A glitch that appears on the decoded output of a ripple counter is often difficult to see on an oscilloscope because it is a random event and very fast and it occurs less frequently than the normal decoded output.

11. Assume a 4-bit ripple counter has a failure in the second flip-flop such that it “locks up”. The third and fourth stages will _____
a) Continue to count with correct outputs

b) Continue to count but have incorrect outputs
c) Stop counting
d) Turn into molten silicon

Answer: c
Explanation: The ripple counter would stop counting because next flip-flop's input depends on the output of the previous flip-flop.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on "Propagation Delay in Ripple Counter".

1. Modulus refers to _____
a) A method used to fabricate decade counter units
b) The modulus of elasticity, or the ability of a circuit to be stretched from one mode to another
c) An input on a counter that is used to set the counter state, such as UP/DOWN
d) The maximum number of states in a counter sequence

Answer: d
Explanation: Modulus is defined as the maximum number of stages/states a counter has. It is independent of the number of states the counter will actually traverse.

2. A sequential circuit design is used to _____
a) Count up
b) Count down
c) Decode an end count
d) Count in a random order

Answer: d
Explanation: A sequential circuit design is used to count in a random manner which is faster than the combinational circuit. It is used for storing data.

3. In general, when using a scope to troubleshoot digital systems, the instrument should be triggered by _____
a) The A channel or channel 1
b) The vertical input mode, when using more than one channel
c) The system clock
d) Line sync, in order to observe troublesome power line glitches

Answer: c
Explanation: All the information is sent from one end to another end through the clock pulse which behaves like a carrier. So, for troubleshooting it should be triggered by the same. Since the system clock is internally produced.

4. Which counters are often used whenever pulses are to be counted and the results displayed in decimal?
a) Synchronous
b) Bean
c) Decade
d) BCD

Answer: d
Explanation: BCD means Binary Coded Decimal, which means that decimal numbers coded of binary numbers. It displays the decimal equivalent of corresponding binary numbers.

5. The _____ counter in the Altera library has controls that allow it to count up or down, and perform synchronous parallel load and asynchronous cascading.
a) 74134
b) LPM
c) Synchronous
d) AHDL

Answer: b
Explanation: The library of parameterized modules (LPM) counter in the Altera library has controls that allow it to count up or down, and perform synchronous parallel load and asynchronous cascading.

6. The minimum number of flip-flops that can be used to construct a modulus-5 counter is _____
a) 3
b) 8
c) 5
d) 10

Answer: a
Explanation: The minimum number of flip-flops used in a counter is given by: $2^{(n-1)} <= N <= 2^n$.
Thus, for modulus-5 counter: $2^2 <= N <= 2^3$, where N = 5 and n = 3.

7. The duty cycle of the most significant bit from a 4-bit (0–9) BCD counter is _____
a) 20%
b) 50%
c) 10%
d) 80%

Answer: a
Explanation: There are 10 states, out of which MSB is high only for (1000, 1001) 2 times. Hence duty cycle is 2/10*100 = 20%. Since the duty cycle is the ratio of on-time to the total time.

8. Normally, the synchronous counter is designed using _____
a) S-R flip-flops
b) J-K flip-flops
c) D flip-flops
d) T flip-flops

Answer: b
Explanation: Since J-K flip-flops have options of recovery from toggle condition and by using less number of J-K flip-flops a synchronous counter can be designed. So, it is more preferred. Also, because JK-flip-flops resolves the problem of Forbidden States.

9. MOD-16 counter requires _____ no. of states.
a) 8
b) 4
c) 16
d) 32

Answer: c
Explanation: $2^n >= N >= 2^{(n-1)}$, by using this formula we get the value of N=16 for n=4.

10. What is a state diagram?
a) It provides the graphical representation of states
b) It provides exactly the same information as the state table
c) It is same as the truth table
d) It is similar to the characteristic equation

Answer: b
Explanation: The state diagram provides exactly the same information as the state table and is obtained directly from the state table.

11. High speed counter is _____
a) Ring counter
b) Ripple counter
c) Synchronous counter
d) Asynchronous counter

Answer: c
Explanation: Synchronous counter doesn’t have propagation delay. Propagation delay refers to the amount of time taken in producing the output when the input is altered.

12. Program counter in a digital computer _____
a) Counts the number of programs run in the machine

b) Counts the number of times a subroutine
c) Counts the number of time the loops are executed
d) Points the memory address of the current or the next instruction

Answer: d
Explanation: Program counter in a digital computer points the memory address of the current or the next instruction which is to be executed.

13. Fundamental mode is another name for _____
a) Level operation
b) Pulse operation
c) Clock operation
d) Edge operation

Answer: b
Explanation: Whatever the input given to the devices are in the form of pulses always. That is why it is known as a fundamental mode.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Registers”.

1. A register is defined as _____
a) The group of latches for storing one bit of information
b) The group of latches for storing n-bit of information
c) The group of flip-flops suitable for storing one bit of information
d) The group of flip-flops suitable for storing binary information

Answer: d
Explanation: A register is defined as the group of flip-flops suitable for storing binary information. Each flip-flop is a binary cell capable of storing one bit of information. The data in a register can be transferred from one flip-flop to another.

2. The register is a type of _____
a) Sequential circuit
b) Combinational circuit
c) CPU
d) Latches

Answer: a
Explanation: Register’s output depends on the past and present states of the inputs. The device which follows these properties is termed as a sequential circuit. Whereas, combinational circuits only depend on the present values of inputs.

3. How many types of registers are?
a) 2
b) 3
c) 4
d) 5

Answer: c
Explanation: There are 4 types of shift registers, viz., Serial-In/Serial-Out, Serial-In/Parallel-Out, Parallel-In/Serial-Out and Parallel-In/Parallel-Out.

4. The main difference between a register and a counter is _____
a) A register has no specific sequence of states
b) A counter has no specific sequence of states
c) A register has capability to store one bit of information but counter has n-bit
d) A register counts data

Answer: a
Explanation: The main difference between a register and a counter is that a register has no specific sequence of states except in certain specialised applications.

5. In D register, ‘D’ stands for _____
a) Delay
b) Decrement

c) Data
d) Decay

Answer: c
Explanation: D stands for “data” in case of flip-flops and not delay. Registers are made of a group of flip-flops.

6. Registers capable of shifting in one direction is _____
a) Universal shift register
b) Unidirectional shift register
c) Unipolar shift register
d) Unique shift register

Answer: b
Explanation: The register capable of shifting in one direction is unidirectional shift register. The register capable of shifting in both directions is known as a bidirectional shift register.

7. A register that is used to store binary information is called _____
a) Data register
b) Binary register
c) Shift register
d) D – Register

Answer: b
Explanation: A register that is used to store binary information is called a binary register. A register in which data can be shifted is called shift register.

8. A shift register is defined as _____
a) The register capable of shifting information to another register
b) The register capable of shifting information either to the right or to the left
c) The register capable of shifting information to the right only
d) The register capable of shifting information to the left only

Answer: b
Explanation: The register capable of shifting information either to the right or to the left is termed as shift register. A register in which data can be shifted only in one direction is called unidirectional shift register, while if data can shifted in both directions, it is known as a bidirectional shift register.

9. How many methods of shifting of data are available?
a) 2
b) 3
c) 4
d) 5

Answer: a
Explanation: There are two types of shifting of data are available and these are serial shifting & parallel shifting.

10. In serial shifting method, data shifting occurs _____
a) One bit at a time
b) simultaneously
c) Two bit at a time
d) Four bit at a time

Answer: a
Explanation: As the name suggests serial shifting, it means that data shifting will take place one bit at a time for each clock pulse in a serial fashion. While in parallel shifting, shifting will take place with all bits simultaneously for each clock pulse in a parallel fashion.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Up Down Counter”.

1. UP-DOWN counter is a combination of _____
a) Latches
b) Flip-flops

c) UP counter
d) Up counter & down counter

Answer: d
Explanation: As the name suggests UP-DOWN, it means that it has up-counter and down-counter as well. It alternatively counts up and down.

2. UP-DOWN counter is also known as _____
a) Dual counter
b) Multi counter
c) Multimode counter
d) Two Counter

Answer: c
Explanation: UP-DOWN counter is also known as multimode counter because it has capability of counting upward as well as downwards.

3. In an UP-counter, each flip-flop is triggered by _____
a) The output of the next flip-flop
b) The normal output of the preceding flip-flop
c) The clock pulse of the previous flip-flop
d) The inverted output of the preceding flip-flop

Answer: b
Explanation: In an UP-counter, each flip-flop is triggered by the normal output of the preceding flip-flop. UP-counter counts from 0 to a maximum value.

4. In DOWN-counter, each flip-flop is triggered by _____
a) The output of the next flip-flop
b) The normal output of the preceding flip-flop
c) The clock pulse of the previous flip-flop
d) The inverted output of the preceding flip-flop

Answer: d
Explanation: In DOWN-counter, each flip-flop is triggered by the inverted output of the preceding flip-flop. DOWN-counter counts from a maximum value to 0.

5. Binary counter that count incrementally and decrement is called _____
a) Up-down counter
b) LSI counters
c) Down counter
d) Up counter

Answer: a
Explanation: Binary counter that counts incrementally and decrement is called UP-DOWN counter/multimode counter. It alternately counts up and down.

6. Once an up-/down-counter begins its count sequence, it _____
a) Starts counting
b) Can be reversed
c) Can’t be reversed
d) Can be altered

Answer: d
Explanation: In up/down ripple counter once the counting begins, we can simply change the pulse M (mode control) M = 0 or 1 respectively for UP counter or Down counter.

7. In 4-bit up-down counter, how many flip-flops are required?
a) 2
b) 3
c) 4
d) 5

Answer: c
Explanation: An n-bit bit counter requires n number of FFs. In a 4-bit up-down counter, there are 4 J-K flip-flops required.

8. A modulus-10 counter must have _____
a) 10 flip-flops
b) 4 Flip-flops
c) 2 flip-flops
d) Synchronous clocking

Answer: b
Explanation: $2^{n-1} <= N <= 2^{n}$
For modulus-10 counter, N = 10. Therefore, $2^{3} <= 10 <= 2^{4}$. Thus, n = 4, and therefore, we require 4 FFs.

9. Which is not an example of a truncated modulus?
a) 8
b) 9
c) 11
d) 15

Answer: a
Explanation: An n-bit counter whose modulus is less than the maximum possible is called a truncated counter. Here, 9, 11 and 15 modulus counters are truncated counters. Whereas, modulus-8 is not a truncated counter.

10. The designation means that the _____
a) Up count is active-HIGH, the down count is active-LOW
b) Up count is active-LOW, the down count is active-HIGH
c) Up and down counts are both active-LOW
d) Up and down counts are both active-HIGH

Answer: a
Explanation: The designation means that the up count is active-HIGH, the down count is active-LOW. Active-High means that up-count would be triggered when clock is 1 else when clock is 0, down-count would be triggered, which is referred to as Active-low.

11. An asynchronous binary up counter, made from a series of leading edge-triggered flip-flops, can be changed to a down counter by _____
a) Taking the output on the other side of the flip-flops (instead of Q)
b) Clocking of each succeeding flip-flop from the other side (instead of Q)
c) Changing the flip-flops to trailing edge triggering
d) All of the Mentioned

Answer: d
Explanation: By all of the mentioned ideas, an asynchronous binary up counter, made from a series of leading edge-triggered flip-flops, can be changed to a down counter. Edge-triggered FFs refer to FFs being triggered during a clock transition from LOW to HIGH or HIGH to LOW.

12. A 4-bit binary up counter has an input clock frequency of 20 kHz. The frequency of the most significant bit is _____
a) 1.25 kHz
b) 2.50 kHz
c) 160 kHz
d) 320 kHz

Answer: a
Explanation: Input clock is given by 20/2 kHz. So, count on the basis of 10 kHz clock. And MSB changes on 8th stage; Hence, f = 10/8 = 1.25 kHz.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Shift Registers”.

1. Based on how binary information is entered or shifted out, shift registers are classified into _____ categories.
a) 2
b) 3
c) 4
d) 5

Answer: c
Explanation: The registers in which data can be shifted serially or parallelly are known as shift registers. Based on how binary information is entered or shifted out, shift registers are classified into 4 categories, viz., Serial-In/Serial-Out(SISO), Serial-In/Parallel-Out (SIPO), Parallel-In/Serial-Out (PISO), Parallel-In/Parallel-Out (PIPO).

2. The full form of SIPO is _____
a) Serial-in Parallel-out
b) Parallel-in Serial-out
c) Serial-in Serial-out
d) Serial-In Peripheral-Out

Answer: a
Explanation: SIPO is always known as Serial-in Parallel-out.

3. A shift register that will accept a parallel input or a bidirectional serial load and internal shift features is called as?
a) Tristate
b) End around
c) Universal
d) Conversion

Answer: c
Explanation: A shift register can shift it’s data either left or right. The universal shift register is capable of shifting data left, right and parallel load capabilities.

4. How can parallel data be taken out of a shift register simultaneously?
a) Use the Q output of the first FF
b) Use the Q output of the last FF
c) Tie all of the Q outputs together
d) Use the Q output of each FF

Answer: d
Explanation: Because no other flip-flops are connected with the output Q, therefore one can use the Q out of each FF to take out parallel data.

5. What is meant by the parallel load of a shift register?
a) All FFs are preset with data
b) Each FF is loaded with data, one at a time
c) Parallel shifting of data
d) All FFs are set with data

Answer: a
Explanation: At Preset condition, outputs of flip-flops will be 1. Preset = 1 means Q = 1, thus input is definitely 1.

6. The group of bits 11001 is serially shifted (right-most bit first) into a 5-bit parallel output shift register with an initial state 01110. After three clock pulses, the register contains _____

a) 01110
b) 00001
c) 00101
d) 00110

Answer: c
Explanation: LSB bit is inverted and feed back to MSB:
01110->initial
10111->first clock pulse
01011->second
00101->third.

7. Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first)
a) 1100
b) 0011

c) 0000
d) 1111

Answer: c
Explanation: In Serial-In/Serial-Out shift register, data will be shifted one at a time with every clock pulse. Therefore,
Wait | Store
1100 | 0000
110 | 0000 1st clock
11 | 0000 2nd clock.

8. A serial in/parallel out, 4-bit shift register initially contains all 1s. The data nibble 0111 is waiting to enter. After four clock pulses, the register contains _____
a) 0000
b) 1111
c) 0111
d) 1000

Answer: c
Explanation: In Serial-In/Parallel-Out shift register, data will be shifted all at a time with every clock pulse. Therefore,
Wait | Store
0111 | 0000
011 | 1000 1st clk
01 | 1100 2nd clk
0 | 1110 3rd clk
X | 1111 4th clk.

9. With a 200 kHz clock frequency, eight bits can be serially entered into a shift register in _____
a) 4 µs
b) 40 µs
c) 400 µs
d) 40 ms

Answer: b
Explanation: f = 200 KHZ; T = (1/200) m sec = (1/0.2) micro-sec = 5 micro-sec;
In serial transmission, data enters one bit at a time. After 8 clock cycles only 8 bit will be loaded = 8 * 5 = 40 micro-sec.

10. An 8-bit serial in/serial out shift register is used with a clock frequency of 2 MHz to achieve a time delay (td) of _____
a) 16 us
b) 8 us
c) 4 us
d) 2 us

Answer: c
Explanation: One clock period is = ($^{1}/_{2}$) micro-s = 0.5 microseconds. In serial transmission, data enters one bit at a time. So, the total delay = 0.5*8 = 4 micro seconds time is required to transmit information of 8 bits.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Universal Shift Registers”.

1. A sequence of equally spaced timing pulses may be easily generated by which type of counter circuit?
a) Ring shift
b) Clock
c) Johnson
d) Binary

Answer: a
Explanation: In Ring counter, the feedback of the output of the FF is fed to the same FF's input. Thus, it generates equally spaced timing pulses.

2. A bidirectional 4-bit shift register is storing the nibble 1101. Its input is HIGH. The nibble 1011 is waiting to be entered on the serial data-input line. After three clock pulses, the shift register is storing _____
a) 1101
b) 0111
c) 0001
d) 1110

Answer: b
Explanation: Mode is high means it's a right shift register. Then after 3 clock pulses enter bits are 011 and remained bit in register is 1. Therefore, 0111 is the required solution.
1011 | 1101
101 | 1110 -> 1 st clock pulse
10 | 1111 -> 2 nd clock pulse
1 | 0111 -> 3 rd clock pulse.

3. To operate correctly, starting a ring shift counter requires _____
a) Clearing all the flip-flops
b) Presetting one flip-flop and clearing all others
c) Clearing one flip-flop and presetting all others
d) Presetting all the flip-flops

Answer: b
Explanation: In Ring counter, the feedback of the output of the FF is fed to the same FF's input. To operate correctly, starting a ring shift counter requires presetting one flip-flop and clearing all others so that it can shift to the next bit.

4. A 4-bit shift register that receives 4 bits of parallel data will shift to the _____ by _____ position for each clock pulse.
a) Right, one
b) Right, two
c) Left, one
d) Left, three

Answer: a
Explanation: If register shifts towards left then it shift by a bit to the left and if register shifts right then it shift to the right by one bit. Since, it receives parallel data, then by default, it will shift to right by one position.

5. How many clock pulses will be required to completely load serially a 5-bit shift register?
a) 2
b) 3
c) 4
d) 5

Answer: d
Explanation: A register is a collection of FFS. To load a bit, we require 1 clock pulse for 1 shift register. So, for 5-bit shift register we would require of 5 clock pulses.

6. How is a strobe signal used when serially loading a shift register?
a) To turn the register on and off
b) To control the number of clocks
c) To determine which output Qs are used
d) To determine the FFs that will be used

Answer: b
Explanation: A strobe is used to validate the availability of data on the data line. It (an auxiliary signal used to help synchronize the real data in an electrical bus when the bus components have no common clock) signal is used to control the number of clocks during serially loading a shift register.

7. An 8-bit serial in/serial out shift register is used with a clock frequency of 150 kHz. What is the time delay between the serial input and the Q3 output?
a) 1.67 s
b) 26.67 s
c) 26.7 ms
d) 267 ms

Answer: b
Explanation: In serial-sifting, one bit of data is shifted one at a time. From Q0 to Q3 total of 4 bit shifting takes place. Therefore, 4/150kHz = 26.67 microseconds.

8. What are the three output conditions of a three-state buffer?
a) HIGH, LOW, float
b) High-Z, 0, float
c) Negative, positive, 0
d) 1, Low-Z, float

Answer: a
Explanation: Three conditions of a three-state buffer are HIGH, LOW & float.

9. The primary purpose of a three-state buffer is usually _____
a) To provide isolation between the input device and the data bus
b) To provide the sink or source current required by any device connected to its output without loading down the output device
c) Temporary data storage
d) To control data flow

Answer: a
Explanation: The primary purpose of a three-state buffer is usually to provide isolation between the input device or peripheral devices and the data bus. Three conditions of a three-state buffer are HIGH, LOW & float.

10. What is the difference between a ring shift counter and a Johnson shift counter?
a) There is no difference
b) A ring is faster
c) The feedback is reversed
d) The Johnson is faster

Answer: c
Explanation: A ring counter is a shift register (a cascade connection of flip-flops) with the output of the last one connected to the input of the first, that is, in a ring. Whereas, a Johnson counter (or switchtail ring counter, twisted-ring counter, walking-ring counter, or Moebius counter) is a modified ring counter, where the output from the last stage is inverted and fed back as input to the first stage.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Shift Register Counters”.

1. What is a recirculating register?
a) Serial out connected to serial in
b) All Q outputs connected together
c) A register that can be used over again
d) Parallel out connected to Parallel in

Answer: a
Explanation: A recirculating register is a register whose serial output is connected to the serial input in a circulated manner.

2. When is it important to use a three-state buffer?
a) When two or more outputs are connected to the same input
b) When all outputs are normally HIGH
c) When all outputs are normally LOW
d) When two or more outputs are connected to two or more inputs

Answer: a
Explanation: When two or more outputs are connected to the same input, in such situation we use of tristate buffer always because it has the capability to take upto three inputs. A buffer is a circuit where the output follows the input.

3. A bidirectional 4-bit shift register is storing the nibble 1110. Its input is LOW. The nibble 0111 is waiting to be entered on the serial data-input line. After two clock pulses, the shift register is storing _____
a) 1110
b) 0111
c) 1000
d) 1001

Answer: d
Explanation: Given,

```
Stored nibble | waiting nibble
         0111 | 1110, Initially
          111 | 1100, 1st pulse
           11 | 1001, 2nd pulse.
```

4. In a parallel in/parallel out shift register, D0 = 1, D1 = 1, D2 = 1, and D3 = 0. After three clock pulses, the data outputs are _____
a) 1110
b) 0001
c) 1100
d) 1000

Answer: b
Explanation: Parallel in parallel out gives the same output as input. Thus, after three clock pulses, the data outputs are 0001.

5. The group of bits 10110111 is serially shifted (right-most bit first) into an 8-bit parallel output shift register with an initial state 11110000. After two clock pulses, the register contains _____
a) 10111000
b) 10110111
c) 11110000
d) 11111100

Answer: d
Explanation: After first clock pulse, the register contains 11111000. After second clock pulse, the register would contain 11111100. Since the bits are shifted to the right at every clock pulse.

6. By adding recirculating lines to a 4-bit parallel-in serial-out shift register, it becomes a _____ _____ and _____ out register.
a) Parallel-in, serial, parallel
b) Serial-in, parallel, serial
c) Series-parallel-in, series, parallel
d) Bidirectional in, parallel, series

Answer: a
Explanation: One bit shifting takes place just after the output obtained on every register. Hence, by adding recirculating lines to a 4-bit parallel-in serial-out shift register, it becomes a Parallel-in, Serial, and Parallel-out register. Since, the bots can be inputted all at the same time, while the data can be outputted either one at a time or simultaneously.

7. What type of register would have a complete binary number shifted in one bit at a time and have all the stored bits shifted out one at a time?
a) Parallel-in Parallel-out
b) Parallel-in Serial-out
c) Serial-in Serial-out
d) Serial-in Parallel-out

Answer: c
Explanation: Serial-in Serial-out register would have a complete binary number shifted in one bit at a time and have all the stored bits shifted out one at a time. Since in serial transmission, bits are transmitted or received one at a time and not simultaneously.

8. In a 4-bit Johnson counter sequence, there are a total of how many states or bit patterns?
a) 1
b) 3
c) 4
d) 8

Answer: d
Explanation: In johnson counter, total number of states are determined by $2^N = 2*4 = 16$
Total Number of Used states = 2N = 2*4 = 8
Total Number of Unused states = 16 – 8 = 8.

9. If a 10-bit ring counter has an initial state 1101000000, what is the state after the second clock pulse?
a) 1101000000
b) 0011010000
c) 1100000000
d) 0000000000

Answer: b
Explanation: After shifting 2-bit we get the output as 0011010000 (Since two zeros are at 1^{st} position and 2^{nd} position which came from the last two bits). As in a ring counter, the bits rotate in clockwise direction.

10. How much storage capacity does each stage in a shift register represent?
a) One bit
b) Two bits
c) Four bits
d) Eight bits

Answer: a
Explanation: A register is made of flip-flops. And each flip-flop stores 1 bit of data. Thus, a shift register has the capability to store one bit and if another bit is to store, in such a situation it deletes the previous data and stores them.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Ring Counter”.

1. Ring shift and Johnson counters are _____
a) Synchronous counters
b) Asynchronous counters
c) True binary counters
d) Synchronous and true binary counters

Answer: a
Explanation: Synchronous counters are the counters being triggered in the presence of a clock pulse. Since all of the clock inputs are connected through a single clock pulse in ring shift and johnson counters. So, both are synchronous counters.

2. What is the difference between a shift-right register and a shift-left register?
a) There is no difference
b) The direction of the shift
c) Propagation delay
d) The clock input

Answer: b
Explanation: In shift-right register, shifting of bit takes place towards the right and towards left for shift-left register. Thus, both the registers vary in the shifting of their direction.

3. What is a transceiver circuit?
a) A buffer that transfers data from input to output
b) A buffer that transfers data from output to input
c) A buffer that can operate in both directions
d) A buffer that can operate in one direction

Answer: c
Explanation: A transceiver circuit is a buffer that can operate in both directions right as well as left.

4. A 74HC195 4-bit parallel access shift register can be used for _____
a) Serial in/serial out operation
b) Serial in/parallel out operation
c) Parallel in/serial out operation
d) All of the Mentioned

Answer: d
Explanation: 74HC195 is an IC, which can be used for all of the given operations, as well as for, parallel-in/parallel-out.

5. Which type of device may be used to interface a parallel data format with external equipment's serial format?
a) UART
b) Key matrix
c) Memory chip
d) Series in Parallel out

Answer: a
Explanation: UART means Universal Asynchronous Receiver/Transmitter which converts the bytes it receives from the computer along parallel circuits into a single serial bit stream for outbound transmission. And also receives data in serial form and converts it into parallel form and sent to the processor.

6. What is the function of a buffer circuit?
a) To provide an output that is inverted from that on the input
b) To provide an output that is equal to its input
c) To clean up the input
d) To clean up the output

Answer: b
Explanation: The function of a buffer circuit is to provide an output that is equal to its input. A transceiver circuit is a buffer that can operate in both directions right as well as left.

7. What is the preset condition for a ring shift counter?
a) All FFs set to 1
b) All FFs cleared to 0
c) A single 0, the rest 1
d) A single 1, the rest 0

Answer: d
Explanation: A ring shift counter is a counter in which the output of one FF connected to the input of the adjacent FF. In preset condition, all of the bits are 0 except first one.

8. Which is not characteristic of a shift register?
a) Serial in/parallel in
b) Serial in/parallel out
c) Parallel in/serial out
d) Parallel in/parallel out

Answer: a
Explanation: There is no such type of register present who doesn't have output end. Thus, Serial in/Parallel in is not a characteristic of a shift register. There has to be an output, be it serial or parallel.

9. To keep output data accurate, 4-bit series-in, parallel-out shift registers employ a _____
a) Divide-by-4 clock pulse
b) Sequence generator
c) Strobe line
d) Multiplexer

Answer: c
Explanation: In computer or memory technology, a strobe is a signal that is sent that validates data or other signals on adjacent parallel lines. Thus, in registers the strobe line is there to check the availability of data.

10. Another way to connect devices to a shared data bus is to use a _____
a) Circulating gate
b) Transceiver
c) Bidirectional encoder
d) Strobed latch

Answer: b
Explanation: A transceiver is a device comprising both a transmitter and a receiver which are combined and share common circuitry or a single housing. When no circuitry is common between transmit and receive functions, the device is a transmitter-receiver.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Introduction of Memory Devices – 1”.

1. Memory is a/an _____
a) Device to collect data from other computer
b) Block of data to keep data separately
c) Indispensable part of computer
d) Device to connect through all over the world

Answer: c
Explanation: Memory is an indispensable unit of a computer and microprocessor based systems which stores permanent or temporary data.

2. The instruction used in a program for executing them is stored in the _____
a) CPU
b) Control Unit
c) Memory
d) Microprocessor

Answer: c
Explanation: All of the program and the instructions are stored in the memory. The processor fetches it as and when required.

3. A flip flop stores _____
a) 10 bit of information
b) 1 bit of information
c) 2 bit of information
d) 3-bit information

Answer: b
Explanation: A flip-flop has capability to store 1 bit of information. It can be used further after erasing previous information.

4. A register is able to hold _____
a) Data
b) Word
c) Nibble
d) Both data and word

Answer: b
Explanation: Register is also a part of memory inside a computer. It stands there to hold a word. A word is a group of 16-bits or 2-bytes.

5. A register file holds _____
a) A large number of word of information
b) A small number of word of information
c) A large number of programs
d) A modest number of words of information

Answer: d
Explanation: A register file is different from a simple register because of capability to hold a modest number of words of information. A word is a group of 16-bits or 2-bytes.

6. The very first computer memory consisted of _____
a) A small display
b) A large memory storage equipment
c) An automatic keyboard input
d) An automatic mouse input

Answer: b
Explanation: The very first computer memory consisted of a minute magnetic toroid, which required large, bulky circuit boards stored in large cabinates.

7. A minute magnetic toroid is also called as _____
a) Large memory
b) Small memory
c) Core memory
d) Both small and large memory

Answer: c
Explanation: A minute magnetic toroid is also called as core memory which is made up of a semiconductor. A semiconductor is a device whose electrical conductivity lies between that of conductor and insulator.

8. Which one of the following has capability to store data in extremely high densities?
a) Register
b) Capacitor
c) Semiconductor
d) Flip-Flop

Answer: c
Explanation: Semiconductor has capability to store data in extremely high densities.

9. A large memory is compressed into a small one by using _____
a) LSI semiconductor
b) VLSI semiconductor
c) CDR semiconductor
d) SSI semiconductor

Answer: b
Explanation: VLSI (Very Large Scale Integration) semiconductor is used in modern computers to short the size of memory.

10. VLSI chip utilizes _____
a) NMOS
b) CMOS
c) BJT
d) All of the Mentioned

Answer: d
Explanation: VLSI (Very Large Scale Integration) is a memory chip which is made up of NMOS, CMOS, BJT, and BiCMOS. It can include 10,000 to 100,000 gates per IC.

11. CD-ROM refers to _____
a) Floppy disk
b) Compact Disk-Read Only Memory
c) Compressed Disk-Read Only Memory
d) Compressed Disk- Random Access Memory

Answer: b
Explanation: CD-ROM refers to Compact Disk-Read Only Memory.

12. Data stored in an electronic memory cell can be accessed at random and on demand using _____
a) Memory addressing
b) Direct addressing
c) Indirect addressing
d) Control Unit

Answer: b
Explanation: Direct addressing eliminates the need to process a large stream of irrelevant data in order to the desired data word.

13. The full form of PLD is _____
a) Programmable Large Device
b) Programmable Long Device
c) Programmable Logic Device
d) Programmable Lengthy Device

Answer: c
Explanation: The full form of PLD is Programmable Logic Device.

14. The evolution of PLD began with _____
a) EROM
b) RAM
c) PROM
d) EEPROM

Answer: a
Explanation: The evolution of PLD (Programmable Logic Device) began with Programmable Read Only Memory (i.e. PROM). Here, the ROM can be externally programmed as per the user.

15. A ROM is defined as _____
a) Read Out Memory
b) Read Once Memory
c) Read Only Memory
d) Read One Memory

Answer: c
Explanation: A ROM is defined as Read Only Memory which can read the instruction stored in a computer.

This set of Advanced Digital Electronic/Circuits Questions & Answers focuses on “Introduction of Memory Devices-4”.

1. Dynamic memory cells use _____ as the storage device.
a) The reactance of a transistor
b) The impedance of a transistor
c) The capacitance of a transistor
d) The inductance of a transistor

Answer: c
Explanation: Capacitance of a transistor prevents from loss of information in a dynamic memory cell.

2. To store 1-bit of information, how many transistor is/are used _____
a) 1
b) 2
c) 3
d) 4

Answer: a
Explanation: Only one bit transistor is needed to store 1-bit of information.

3. Static memory holds data as long as _____
a) AC power is applied
b) DC power is applied
c) Capacitor is fully charged
d) High Conductivity

Answer: b
Explanation: In any semiconductor equipment, AC power can't be supplied directly. So, static memory holds the data as long as DC power is applied.

4. The example of dynamic memory is _____
a) CCD
b) Semiconductor dynamic RAM
c) Both CCD and semiconductor dynamic RAM
d) Floppy-Disk

Answer: c
Explanation: The examples of dynamic memories are CCD and semiconductor dynamic RAM because of the contents of both the memories changes with time.

5. In dynamic memory, CCD stands for _____
a) Charged Count Devices
b) Change Coupled Devices
c) Charge Coupled Devices
d) Charged Compact Disk

Answer: b
Explanation: In dynamic memory, CCD stands for Charge Coupled Devices.

6. Volatile memory refers to _____
a) The memory whose loosed data is achieved again when power to the memory circuit is removed
b) The memory which looses data when power to the memory circuit is removed
c) The memory which looses data when power to the memory circuit is applied
d) The memory whose loosed data is achieved again when power to the memory circuit is applied

Answer: b
Explanation: Volatile means 'liable to change rapidly' and volatile memory refers to the memory which looses data rapidly when power to the memory circuit is removed. Thus, it looks after it's data as long as it is powered. Non-volatile means 'not volatile' and non-volatile memory refers to the memory which retains the data even if there is a break in the power supply.

7. Non-volatile memory refers to _____
a) The memory whose loosed data is retained again when power to the memory circuit is removed/applied
b) The memory which looses data when power to the memory circuit is removed
c) The memory which looses data when power to the memory circuit is applied
d) The memory whose loosed data is achieved again when power to the memory circuit is applied

Answer: a
Explanation: Volatile means 'liable to change rapidly' and volatile memory refers to the memory which looses data rapidly when power to the memory circuit is removed. Thus, it looks after it's data as long as it is powered. Non-volatile means 'not volatile' and non-volatile memory refers to the memory which retains the data even if there is a break in the power supply.

8. The example of non-volatile memory device is _____
a) Magnetic Core Memory
b) Read Only Memory
c) Random Access Memory
d) Both Magnetic Core Memory and Read Only Memory

Answer: d
Explanation: Non-volatile means 'not volatile' and non-volatile memory refers to the memory

which retains the data even if there is a break in the power supply. The examples of non-volatile memory devices are Magnetic Core Memory & ROM because both have capability to retain the data.

9. Based on material used for construction, memory devices are classifieds into _____ categories.
a) 2
b) 3
c) 4
d) 5

Answer: a
Explanation: Based on material used for construction, memory devices are classifieds into two categories, viz., Magnetic and Semiconductor memory. Magnetic recording is the process of storing data magnetically. Hard disk, floppy disk, magnetic tape are examples of magnetic recording process.

10. Magnetic recording is the process of _____
a) Storing data symmetrically
b) Storing data sequentially
c) Storing data magnetically
d) Both storing data symmetrically and

Answer: c
Explanation: Based on material used for construction, memory devices are classifieds into two categories, viz., Magnetic and Semiconductor memory. Magnetic recording is the process of storing data magnetically. Hard disk, floppy disk, magnetic tape are examples of the magnetic recording process.

11. Magnetic drum is a storage medium using _____
a) The surface of a jumping magnetic drum
b) The surface of a rotating magnetic drum
c) The surface of a stopped magnetic drum
d) The surface of a moving magnetic drum

Answer: b
Explanation: Magnetic drum is a storage medium using the surface of a rotating magnetic drum which have tendency to hold the data.

12. Magnetic core is the digital memory in which data is stored magnetically in individual cores operated by _____
a) Up and down select wires
b) Row and column select wires
c) Serial and parallel select wires
d) Up and Serial select wires

Answer: b
Explanation: Magnetic core is the digital memory in which data is stored magnetically in individual cores operated by row and column select wires, with data obtained from sense wire.

13. By which technology, semiconductor memories are constructed?
a) PLD
b) LSI
c) VLSI
d) Both LSI and VLSI

Answer: d
Explanation: Generally, semiconductor memories are constructed using Large Scale Integration (LSI) or Very Large Scale Integration (VLSI) because these are made up of NMOS, CMOS, BJT, etc.

This set of Digital Electronic Circuits Questions & Answers for campus interviews focuses on “Introduction of Memory Devices-5”.

1. When two or more devices try to write data in a bus simultaneously, is known as _____
a) Bus collisions
b) Address multiplexing
c) Address decoding
d) Bus contention

Answer: d
Explanation: Bus contention is an undesirable state of the bus of a computer, in which more than one memory mapped device or the CPU is attempting to place output values onto the bus at once.

2. A memory is a collection of _____
a) Unit cells
b) Storage cells
c) Data cells
d) Binary cells

Answer: b
Explanation: A memory is a collection of storage cells with associated circuits needed to transfer information.

3. To transfer the information from input to output and vice versa, the cells used are _____
a) Storage cells
b) Data cells
c) Unit cells
d) Both data and unit cells

Answer: a
Explanation: To transfer the information from input to output and vice versa, the cells used are called storage cells. The storage cells stores data in the form of binary information.

4. The data stored in a group of bits is called _____
a) Nibble
b) Word
c) Byte
d) Address

Answer: b
Explanation: The data stored in a group of bits is called word. Usually, a word is a group of 16-bits or 2-bytes.

5. Each word consist of a sequence of _____
a) Letters
b) Binary numbers
c) Hexadecimal numbers
d) Gray codes

Answer: b
Explanation: Each word consists of a sequence of 0s and 1s (i.e. binary numbers). Usually, a word is a group of 16-bits or 2-bytes.

6. Each word stored in a memory location is represented by _____
a) RAM
b) ROM
c) Storage class
d) Address

Answer: d
Explanation: Each word stored in a memory location is represented by address. Usually, a word is a group of 16-bits or 2-bytes.

7. The group of each 8-bit is called _____
a) Nibble

b) Flag
c) Byte
d) Word

Answer: c
Explanation: 1 byte = 8-bit, 4-bits = 1 nibble and 16-bits = 1 word.

8. The capacity of a memory unit is _____
a) The number of binary input stored
b) The number of words stored
c) The number of bytes stored
d) All of the Mentioned

Answer: c
Explanation: The total number of bytes that can be stored, is the maximum capacity of a memory unit. However, memory unit is the smallest unit of a processor.

9. The communication between memory and its environment is achieved through _____
a) Control lines
b) Data input/output lines
c) Address selection lines
d) All of the Mentioned

Answer: d
Explanation: Firstly, the data input is needed to transfer the information and it is passed through the address lines and then controlled by control lines. The control lines are responsible for the timing and control of the signals sent and received.

10. One of the most important specifications on magnetic media is the _____
a) Polarity reversal rate
b) Tracks per inch
c) Data transfer rate
d) Rotation speed

Answer: c
Explanation: The rate of data transfer depends on the properties of magnetic media.

This set of Digital Electronic/Circuits assessment questions focuses on “Introduction of Memory Devices-2”.

1. The full form of ROM is _____
a) Read Outside Memory
b) Read Out Memory
c) Read Only Memory
d) Read One Memory

Answer: c
Explanation: The full form of ROM is Read Only Memory.

2. ROM consist of _____
a) NOR and OR arrays
b) NAND and NOR arrays
c) NAND and OR arrays
d) NOR and AND arrays

Answer: c
Explanation: ROM consists of NAND and OR arrays which can be programmed by the user to implement combinational & sequential functions. Combinational Operations like that of adders and subtractors and Sequential Functions like that of storing in the memory.

3. For reprogrammability, PLDs use _____
a) PROM
b) EPROM
c) CDROM
d) PLA

Answer: b
Explanation: For reprogrammability, PLDs use EPROM (i.e. Erasable PROM). It erases the previous program and starts uploading a new one. However, data is erased by exposing it to UV-light, which is a tedious and time-consuming process.

4. The full form of PROM is _____
a) Previous Read Only Memory
b) Programmable Read Out Memory
c) Programmable Read Only Memory
d) Previous Read Out Memory

Answer: c
Explanation: The full form of PROM is Programmable Read Only Memory, where the ROM can be programmed by the user.

5. The full form of EPROM is _____
a) Easy Programmable Read Only Memory
b) Erasable Programmable Read Only Memory
c) Eradicate Programmable Read Only Memory
d) Easy Programmable Read Out Memory

Answer: b
Explanation: The full form of EPROM is Erasable Programmable Read Only Memory, where the ROM can be erased and re-used by the user.

6. PLDs with programmable AND and fixed OR arrays are called _____
a) PAL
b) PLA
c) APL
d) PPL

Answer: a
Explanation: PLDs with programmable AND and fixed OR arrays are called PAL (i.e. Programmable Array Logic). However, PAL is less flexible but has higher speed.

7. When both the AND and OR are programmable, such PLDs are known as _____
a) PAL
b) PPL
c) PLA
d) APL

Answer: c
Explanation: When both the AND and OR are programmable, such PLDs are known as PLA (i.e. Programmable Logic Array). However, PLA is more flexible but has less speed.

8. ASIC stands for _____
a) Application Special Integrated Circuits
b) Applied Special Integrated Circuits
c) Application Specific Integrated Circuits
d) Applied Specific Integrated Circuits

Answer: c
Explanation: In digital electronics, ASIC stands for Application Specific Integrated Circuits. It is a customized integrated circuit which is produced for a specific use and not for a common-purpose.

9. The programmability and high density of PLDs make them useful in the design of _____
a) ISAC
b) ASIC
c) SACC
d) CISF

Answer: b
Explanation: The programmability and high density of PLDs make them useful in the design of

ASIC (i.e. Application Specific Integrated Circuits) where design changes can be more rapidly and inexpensively.

10. FPGA stands for _____
a) Full Programmable Gate Array
b) Full Programmable Genuine Array
c) First Programmable Gate Array
d) Field Programmable Gate Array

Answer: d
Explanation: In digital electronics, FPGA stands for Field Programmable Gate Array. This type of integrated circuit is for general-purpose which is configured by the user as per their requirement.

11. Which of the following is a reprogrammable gate array?
a) EPROM
b) FPGA
c) Both EPROM and FPGA
d) ROM

Answer: c
Explanation: Both FPGA and EPROM are reprogrammable gate array.

12. The difference between FPGA and PLD is that _____
a) FPGA is slower than PLD
b) FPGA has high power dissipation
c) FPGA incorporates logic blocks
d) All of the Mentioned

Answer: c
Explanation: The difference between FPGA and PLD is that FPGA incorporates logic blocks instead of fixed AND-OR gates and is faster with low power dissipation. FPGAs are designed for having higher gate count whereas, PLDs are used for lesser gate counts.

This set of Digital Electronic/Circuits Puzzles focuses on “Introduction of Memory Devices-3”.

1. Memories are classified into _____ categories.
a) 3
b) 4
c) 5
d) 6

Answer: c
Explanation: Memory is typically classified of 2 types: Primary and Secondary. These are further classified into 5 types of memories and these are Secondary, RAM, Dynamic/Static, Volatile/Non-volatile, Magnetic/Semiconductor Memory.

2. Secondary memory is also known as _____
a) Registers
b) Main Memory
c) RAM
d) Both registers and main memory

Answer: d
Explanation: Secondary memory is also known as Registers/Main Memory. In secondary memory, data is usually stored for a long-term.

3. In a computer, registers are present _____
a) Within control unit
b) Within RAM
c) Within ROM
d) Within CPU

Answer: d
Explanation: In a computer, registers are present within the CPU to store data temporarily during arithmetic and logical operations and during the functioning of the ALU.

4. Which of the following has the lowest access time?
a) RAM
b) ROM
c) Registers
d) Flag

Answer: c
Explanation: Registers has the lowest access time, as they are available inside the CPU. Registers are present within the CPU to store data temporarily during arithmetic and logical operations and during the functioning of the ALU.

5. Main memories of a computer, usually made up of _____
a) Registers
b) Semiconductors
c) Counters
d) PLDs

Answer: b
Explanation: Main memories of a computer, usually made up of semiconductors which are available external to the CPU to store program and data during execution of a program. Registers are present within the CPU to store data temporarily during arithmetic and logical operations and during the functioning of the ALU.

6. As the storage capacity of the main memory is inadequate, which memory is used to enhance it?
a) Secondary Memory
b) Auxiliary Memory
c) Static Memory
d) Both Secondary Memory and Auxiliary Memory

Answer: d
Explanation: As the storage capacity of the main memory is inadequate, Secondary memory is used to enhance it and it is also known as auxiliary memory. Secondary memory is also known as Registers/Main Memory. In secondary memory, data is usually stored for a long-term.

7. Which memories are if magnetic memory type?
a) Main Memory
b) Secondary Memory
c) Static Memory
d) Volatile Memory

Answer: b
Explanation: Usually, secondary memories are of magnetic memory type that are used to store large type quantities of data. In secondary memory, data is usually stored for a long-term.

8. Which of the following comes under secondary memory/ies?
a) Floppy disk
b) Magnetic drum
c) Hard disk
d) All of the Mentioned

Answer: d
Explanation: All of the mentioned equipments are of external storage which is known as secondary memories. In secondary memory, data is usually stored for a long-term.

9. Based on method of access, memory devices are classified into _____ categories.
a) 2
b) 3
c) 4
d) 5

Answer: a
Explanation: Based on the method of access, memory devices are classified into two categories and these are sequential access memory and RAM. A sequential access memory is one in which a particular memory location is accessed sequentially.

10. A sequential access memory is one in which _____
a) A particular memory location is accessed rapidly
b) A particular memory location is accessed sequentially
c) A particular memory location is accessed serially
d) A particular memory location is accessed parallely

Answer: b
Explanation: A sequential access memory is one in which A particular memory location is accessed sequentially (i.e. the ith memory location is accessed only after sequencing through previous (i-1) memory locations).

11. An example of sequential access memory is _____
a) Floppy disk
b) Hard disk
c) Magnetic tape memory
d) RAM

Answer: c
Explanation: A sequential access memory is one in which a particular memory location is accessed sequentially. In magnetic tape memory, data is accessed sequentially.

12. A Random Access Memory is one in which _____
a) Any location can be accessed sequentially
b) Any location can be accessed randomly
c) Any location can be accessed serially
d) Any location can be accessed parallely

Answer: b
Explanation: A Random Access Memory is one in which any location can be accessed randomly.

13. An example of RAM is _____
a) Floppy disk
b) Hard disk
c) Magnetic tape memory
d) Semiconductor RAM

Answer: d
Explanation: A Random Access Memory is one in which any location can be accessed randomly. A semiconductor RAM is too much fast and can occupy any space in the memory location.

14. A static memory is one in which _____
a) Content changes with time
b) Content doesn’t changes with time
c) Memory is static always
d) Memory is dynamic always

Answer: d
Explanation: A static memory is one in which content doesn’t changes with time (i.e. stable). Dynamic memory is one in which content changes with time (i.e. unstable).

15. A dynamic memory is one in which _____
a) Content changes with time
b) Content doesn’t changes with time
c) Memory is static always
d) Memory is dynamic always

Answer: d
Explanation: A static memory is one in which content doesn’t change with time (i.e. stable). Dynamic memory is one in which content changes with time (i.e. unstable).

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Read Only Memory (ROM) – 1”.

1. Which of the following has the capability to store the information permanently?
a) RAM
b) ROM

c) Storage cells
d) Both RAM and ROM

Answer: b
Explanation: ROM (Read Only Memory) has the capability to store the information permanently. RAM provides random access to memory. Storage cells are responsible for the transfer of data from and into the memory.

2. ROM has the capability to perform _____
a) Write operation only
b) Read operation only
c) Both write and read operation
d) Erase operation

Answer: b
Explanation: ROM means “Read Only Memory”. Hence, it has the capability to perform read operation only. No write or erase operation could be performed in the ROM.

3. Since, ROM has the capability to read the information only then also it has been designed, why?
a) For controlling purpose
b) For loading purpose
c) For booting purpose
d) For erasing purpose

Answer: c
Explanation: ROM means “Read Only Memory”. Hence, it has capability to perform read operation only. No write or erase operation could be performed in the ROM. It has designed to provide the computer with resident programmes and for booting purpose.

4. The ROM is a _____
a) Sequential circuit
b) Combinational circuit
c) Magnetic circuit
d) Static circuit

Answer: b
Explanation: ROM is a combination of different ICs. So, it is a combinational circuit. It depends on present input and not past states.

5. ROM is made up of _____
a) NAND and OR gates
b) NOR and decoder
c) Decoder and OR gates
d) NAND and decoder

Answer: c
Explanation: ROM (Read Only Memory) has the capability to store the information permanently. ROM is made up of decoder and OR gates within a single IC package.

6. Why are ROMs called non-volatile memory?
a) They lose memory when power is removed
b) They do not lose memory when power is removed
c) They lose memory when power is supplied
d) They do not lose memory when power is supplied

Answer: b
Explanation: Volatile memory stores data as long as it is powered. ROMs are called non-volatile memory because of they do not lose memory when power is removed.

7. In ROM, each bit is a combination of the address variables is called _____
a) Memory unit
b) Storage class
c) Data word
d) Address

Answer: d
Explanation: In ROM, each bit combination that comes out of the output lines is called data word. Usually, a word consists of 16-bits or 2-bytes.

8. Which is not a removable drive?
a) Zip
b) Hard disk
c) Super Disk
d) Jaz

Answer: c
Explanation: Hard disk is present inside a computer. So, it is not a removable drive.

9. In ROM, each bit combination that comes out of the output lines is called _____
a) Memory unit
b) Storage class
c) Data word
d) Address

Answer: c
Explanation: In ROM, each bit combination that comes out of the output lines is called data word. Usually, a word consists of 16-bits or 2-bytes.

10. VLSI chip utilizes _____
a) NMOS
b) CMOS
c) BJT
d) All of the Mentioned

Answer: d
Explanation: Very Large Scale Integration (VLSI) (ranging from 10,000 to 100,000 gates per IC) is a memory chip which is made up of NMOS, CMOS, BJT, and BiCMOS.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Programmable Read Only Memory -1”.

1. The time from the beginning of a read cycle to the end of tACS/tAA is called as _____
a) Write enable time
b) Data hold
c) Read cycle time
d) Access time

Answer: d
Explanation: The time from the beginning of a read cycle to the end of tACS/tAA is called as access time. It is the time in which data is fetched from the storage.

2. Why did PROM introduced?
a) To increase the storage capacity
b) To increase the address locations
c) To provide flexibility
d) To reduce the size

Answer: c
Explanation: In order to provide some flexibility in the possible applications of ROM, PROM is introduced. PROM stands for Programmable ROM, in which the ROM is programmed by the user.

3. Which of the following is programmed electrically by the user?
a) ROM
b) EPROM
c) PROM
d) EEPROM

Answer: c
Explanation: Programmable ROMs can be programmed electrically by the user but can’t be reprogrammed. EEPROMs can be electrically erased and re-programmed by the user.

4. PROMs are available in _____
a) Bipolar and MOSFET technologies
b) MOSFET and FET technologies
c) FET and bipolar technologies
d) MOS and bipolar technologies

Answer: d
Explanation: PROMs (Programmable ROMs) can be programmed electrically by the user but can't be reprogrammed. PROMs are available in both bipolar and MOS (Metal Oxide Semiconductor) technologies.

5. The bit capacity of a memory that has 2048 addresses and can store 8 bits at each address is _____
a) 4096
b) 16384
c) 32768
d) 8129

Answer: b
Explanation: 1 address can store 8 bits. Therefore, total capacity of a memory having n addresses = 8 * n.
Therefore, for 2048 addresses,
total capacity of a memory = 2048 * 8 = 16384 bits.

6. How many 8 k × 1 RAMs are required to achieve a memory with a word capacity of 8 k and a word length of eight bits?
a) Eight
b) Two
c) One
d) Four

Answer: a
Explanation: RAM stands for Random Access Memory in which any memory address can be accessed in any order. It requires word of length 8 bits. So, one word needs of 1 bit and 8 bit requires 8 bits.

7. Which of the following best describes the fusible-link PROM?
a) Manufacturer-programmable, reprogrammable
b) Manufacturer-programmable, one-time programmable
c) User-programmable, reprogrammable
d) User-programmable, one-time programmable

Answer: d
Explanation: The fusible-link PROM is user programmable and one time programmable. It means that a written program can not be reprogrammed. EPROMs can be erased and re-programmed.

8. How can ultraviolet erasable PROMs be recognized?
a) There is a small window on the chip
b) They will have a small violet dot next to the #1 pin
c) Their part number always starts with a "U", such as in U12
d) They are not readily identifiable, since they must always be kept under a small cover

Answer: a
Explanation: An ultraviolet erasable PROMs have small window on the chip with black marked. Such type of PROMS are called EPROMS which are cleared by exposing it to UV radiation. They are re-programmable.

9. Which part of a Flash memory architecture manages all chip functions?
a) Program verify code
b) Floating-gate MOSFET
c) Command code
d) Input/Output pins

Answer: b
Explanation: MOSFET technology is the best one in the manufacturing of chip because it has high flexibility and storage capacity. Thus, Floating-Gate MOSFET part of a Flash Memory architecture manages all chip functions.

10. How much locations an 8-bit address code can select in memory?
a) 8 locations
b) 256 locations
c) 65,536 locations
d) 131,072 locations

Answer: b
Explanation: An 8 bit address code requires 32 memory locations and it can hold maximum upto $32 * 8 = 256 \text{ locations} = 2^8$.

11. What is a fusing process?
a) It is a process by which data is passed to the memory
b) It is a process by which data is read through the memory
c) It is a process by which programs are burnout to the diode/transistors
d) It is a process by which data is fetched through the memory

Answer: c
Explanation: Fusing is a process by which programs are burnout to the diode/transistors and it can not be reprogrammed if any error occurs.

12. Fusing process is _____
a) Reversible
b) Irreversible
c) Synchronous
d) Asynchronous

Answer: b
Explanation: Since, any program cannot be reprogrammed in a PROM, so this process is irreversible as PROMs are programmed using the Fusing process. Fusing is a process by which programs are burnout to the diode/transistors and it can not be reprogrammed if any error occurs.

13. The cell type used inside a PROM is _____
a) Link cells
b) Metal cells
c) Fuse cells
d) Electric cells

Answer: c
Explanation: The cell type used inside a PROM is fuse cells by which a program is burnout. Fusing is a process by which programs are burnout to the diode/transistors and it can not be reprogrammed if any error occurs.

14. How many types of fuse technologies are used in PROMs?
a) 2
b) 3
c) 4
d) 5

Answer: b
Explanation: Fusing is a process by which programs are burnout to the diode/transistors and it can not be reprogrammed if any error occurs. Three types of fuse technologies are used in PROMs and these are: (i) Metal links, (ii) Silicon links, & (iii) p-n junctions.

15. Metal links are made up of _____
a) Polycrystalline
b) Magnesium sulphide
c) Nichrome
d) Silicon dioxide

Answer: c
Explanation: Metal links are made up of Nichrome materials.

This set of Digital Electronic/Circuits Aptitude Test focuses on “Read Only Memory(ROM)-3”.

1. ROM may be programmed in _____ ways.
a) 2
b) 3
c) 4
d) 5

Answer: a
Explanation: ROM may be programmed in two different ways: (i) Mask Programming & (ii) PROM. Mask Programming is done by the manufacture. Whereas, PROM(Programmable ROM) is programmed by the user.

2. Which programming is done during the manufacturing process?
a) Mask Programming
b) PROM
c) Both PROM and mask programming
d) EPROM

Answer: a
Explanation: Mask ROM is permanently programmed during the manufacturing process. Whereas, PROM(Programmable ROM) is programmed by the user.

3. A photographic negative is called a _____
a) Photo
b) Negative
c) Mask
d) Virtual image

Answer: c
Explanation: A photographic negative is called a mask is used to control the electrical connections on the chip.

4. Mask programming is also known as _____
a) EPROM
b) PROM
c) Custom programming
d) Both PROM and EPROM

Answer: c
Explanation: Mask programming is also known as custom programming. Mask ROM is permanently programmed during the manufacturing process. Whereas, PROM(Programmable ROM) is programmed by the user.

5. The total storage capacity of 16 * 8 ROM is _____
a) 8 bits
b) 16 bits
c) 128 bits
d) 64 bits

Answer: c
Explanation: ROM stands for Read Only Memory in which data is stored permanently and wherefrom data can only be read and rarely modified. The total storage capacity of 16 * 8 ROM is 128 bits (i.e. 16 * 8 = 128).

6. Which IC is a typical MSI/TTL based?
a) IC 74187
b) IC 74189
c) IC 74188
d) IC 74186

Answer: a
Explanation: MSI/TTL stands for Medium Scale Integration of Transistor-Transistor Logic. IC 74187 is a typical MSI/TTL based.

7. IC 74187 is of _____
a) 512 bits
b) 1024 bits
c) 256 bits
d) 68 bits

Answer: b
Explanation: IC 74187 is of 1024 bits because it is organised as 256 * 4. Thus, it has 256 rows and 4 columns.

8. How many rows and columns are present in IC 74187?
a) 128, 3
b) 128, 4
c) 256, 3
d) 256, 4

Answer: d
Explanation: IC 74187 is organised as 256 * 4, hence it has 256 rows and 4 columns.
IC 74187 is of 1024 bits because it is organized as 256 * 4.

9. Which of the following IC is of 256 bit?
a) IC 74187
b) IC 74189
c) IC 74188
d) IC 74186

Answer: c
Explanation: IC 74188 is of 256 bits. Since, it is organised as 32 * 8 = 256. Thus, it has 32 rows and 8 columns.

10. Which IC is known as bipolar ROM?
a) IC 74187
b) IC 74189
c) IC 74188
d) IC 74186

Answer: c
Explanation: IC 74188 is known as bipolar ROM since it is made up of TTL logic.

11. How many address location a bipolar ROM has?
a) 16
b) 32
c) 64
d) 8

Answer: b
Explanation: Bipolar ROM means IC 74188 and it is organized as 32 * 8. Thus, it has 32 rows and 8 columns. So, it has 32 address locations and each of which has 8 bits of storage.

12. Which of the following is known as MOS static ROM?
a) TMS 45276
b) TMS 45278
c) TMS 45279
d) TMS 45275

Answer: a
Explanation: TMS 45276 is known as MOS static ROM and it is made up of MOSFETs.

13. TMS 45276 is of _____
a) 32 KB
b) 56 KB
c) 8 bits

d) 4 bytes

Answer: a
Explanation: TMS 45276 is known as MOS static ROM and it is made up of MOSFETs. In ROM, the data remains even when the power is switched off. TMS 45276 is of 32 KB.

14. Which of the following has the capability to store the highest bits of data?
a) TMS 45276
b) IC 74188
c) IC 74187
d) IC 74185

Answer: a
Explanation: TMS 45276 has the capability to store the highest bits of data because of 32768 * 8 = 12,62,144 organization.

15. What does CS mean in a chip?
a) Storing Capacity
b) Custom Select
c) Chip Select
d) Custom Storage

Answer: c
Explanation: CS means chip select and with the help of CS a chip is activated/deactivated. It is used for enabling or disabling the function of the chip.

16. ROMs are used to _____
a) Store bootstrap program
b) Character generation
c) Code conversion
d) All of the Mentioned

Answer: d
Explanation: ROM stands for Read Only Memory in which data is permanently stored, even when the power is turned off. It is used to store bootstrap program, character generation and code conversion.

This set of tricky Digital Electronic/Circuits questions and answers focuses on “Read Only Memory(ROM) – 2”.

1. The MOS technology based semiconductor ROMs are classified into _____ categories.
a) 2
b) 3
c) 4
d) 5

Answer: b
Explanation: The MOS technology based semiconductor ROMs are classified into three categories: Mask ROM, PROM,& EPROM. PROM stands for Programmable Read Only Memory in which the ROM can be externally programmed by the user. EPROM stands for Erasable Programmable Read Only Memory, where the ROM and be cleared and re-programmed.

2. MOS ROM is constructed using _____
a) FETs
b) Transistors
c) MOSFETs
d) BJTs

Answer: c
Explanation: MOS ROM is made up of MOSFETs. MOSFETs are Metal Oxide Semiconductor Field Effect Transistors.

3. The full form of EEPROM is _____
a) Erasable Electrically Programmable ROMs
b) Electrically Erasable Programmable ROMs
c) Electrically Erasable Programming ROMs

d) Electrically Erasable Programmed ROMs

Answer: b
Explanation: The full form of EEPROM is Electrically Erasable Programmable ROMs. In EPROM (Erasable Programmable ROMs), the ROM is cleared by exposing it to UV radiation and also it's a tedious process. Whereas, in EEPROM, the ROM can be cleared electrically and thus is less time consuming and more efficient.

4. Which of the following best describes EPROMs?
a) EPROMs can be programmed only once
b) EPROMs can be erased by UV
c) EPROMs can be erased by shorting all inputs to the ground
d) EPROMs can be erased electrically

Answer: b
Explanation: EPROM (Erasable Programmable ROMs), the ROM is cleared by exposing it to UV radiation and also it's a tedious process. Whereas, in EEPROM, the ROM can be cleared electrically and thus is less time consuming and more efficient.

5. The Width of a processor's data path is measured in bits. Which of the following are common data paths?
a) 8 bits
b) 12 bits
c) 16 bits
d) 32 bits

Answer: a
Explanation: In generalised form, the data paths are of 8 bits. The data path, also known as data bus, is the channel through which the processor sends and receives data.

6. What type of memory is not directly addressable by the CPU and requires special software called EMS (expanded memory specification)?
a) Extended
b) Expanded
c) Base
d) Conventional

Answer: b
Explanation: Expanded memory is not directly addressable by the CPU. Expanded memory is the additional memory which is incorporated beyond the parent memory limit of the processor.

7. Which bus is used for input and output in case of microprocessor operation?
a) Address bus
b) System bus
c) Control bus
d) Data bus

Answer: c
Explanation: The input and output are used to control the function of a microprocessor. Hence, the control bus is used to transfer the input and output signal from microprocessor to external peripherals and or from external peripherals to microprocessor.

8. What is the major difference between DRAM and SRAM?
a) Dynamic RAMs are always active; static RAMs must reset between data read/write cycles
b) SRAMs can hold data via a static charge, even with power off
c) The only difference is the terminal from which the data is removed—from the FET Drain or Source
d) DRAMs must be periodically refreshed

Answer: d
Explanation: DRAMs must be periodically refreshed so that it can store the new information. DRAMs are slower compared to SRAMs as the access time for SRAM is less than that of DRAM.

9. Which of the following is not a part of Hard disk?
a) Platter
b) Read/Write
c) Valve
d) Spindle

Answer: c
Explanation: A valve is a device that regulates, directs or controls the flow of a fluid (gases, liquids, fluidized solids, or slurries) by opening, closing, or partially obstructing various passageways. So, it is not a part of hard disk.

10. Which ROM can be erased by an electrical signal?
a) ROM
b) Mask ROM
c) EPROM
d) EEPROM

Answer: d
Explanation: In EPROM (Erasable Programmable ROMs), the ROM is cleared by exposing it to UV radiation and also it's a tedious process. Whereas, in EEPROM, the ROM can be cleared electrically and thus is less time consuming and more efficient.

11. In the floppy drive, data is written to and read from the disk via a magnetic _____ head mechanism.
a) Cluster
b) Read/Write
c) Cylinder
d) Recordable

Answer: b
Explanation: A floppy disk is a removable disk used for storing data via magnetic facilities. In the floppy drive, data is written to and read from the disk via a magnetic read/write head mechanism.

12. What does the term "random access" mean in terms of memory?
a) Any address can be accessed in systematic order
b) Any address can be accessed in any order
c) Addresses must be accessed in a specific order
d) Any address can be accessed in reverse order

Answer: b
Explanation: "Random access" mean which can be accessed randomly and in other words any address can be accessed in any order.

13. Which type of ROM has to be custom built by the factory?
a) EEPROM
b) Mask ROM
c) EPROM
d) PROM

Answer: b
Explanation: All types of ROM are programmable and can be programmed as per requirement but the mask ROM is always programmed for specific application and it can't be reprogrammed. PROM stands for Programmable Read Only Memory in which the ROM can be externally programmed by the user. EPROM stands for Erasable Programmable Read Only Memory, where the ROM and be cleared and re-programmed.

14. The computer's main memory is _____
a) Hard drive and RAM
b) CD-ROM and hard drive
c) RAM and ROM
d) CMOS and hard drive

Answer: c
Explanation: The computer's main memory is RAM and ROM because all the storage related

operation are performed by the data present in RAM/ROM. RAM stands for Random Access Memory where any address can accessed in any order. ROM stands for Read Only Memory wherefrom data can only be read.

15. A major disadvantage of the mask ROM is that _____
a) It is time consuming to change the stored data when system requirements change
b) It is very expensive to change the stored data when system requirements change
c) It cannot be reprogrammed if stored data needs to be changed
d) It has an extremely short life expectancy and requires frequent replacement

Answer: c
Explanation: A major disadvantage of the mask ROM is that it cannot be reprogrammed if stored data needs to be changed. PROM stands for Programmable Read Only Memory in which the ROM can be externally programmed by the user. EPROM stands for Erasable Programmable Read Only Memory, where the ROM and be cleared and re-programmed.

This set of Digital Electronic/Circuits Problems focuses on “Programmable Read Only Memory-2”.

1. Silicon links are made up of _____
a) Polycrystalline silicon
b) Polycrystalline magnesium
c) Nichrome
d) Silicon dioxide

Answer: a
Explanation: Metal links are made up of Nichrome materials. Silicon links are made up of polycrystalline silicon.

2. During programming p-n junction is _____
a) Avalanche reverse biased
b) Avalanche forward biased
c) Zener reverse biased
d) Zener reverse biased

Answer: a
Explanation: The sudden heavy flow of electrons in the reverse direction and heat cause aluminium ions to migrate. So, during programming p-n junction is avalanche reversed biased.

3. The full form of FAMOS is _____
a) Floating Gate Avalanche Injection MOS
b) Float Gate Avalanche Injection MOS
c) Floating Gate Avalanche Induction MOS
d) Float Gate Avalanche Induction MOS

Answer: a
Explanation: The full form of FAMOS is Floating Gate Avalanche Injection MOS. It is a floating gate transistor in which the trapped electrons is responsible for the dropping of the voltage.

4. PROM is programmed by _____
a) EPROM programmer
b) EEPROM programmer
c) PROM programmer
d) ROM programmer

Answer: c
Explanation: PROM is programmed by plugging it into a special device called PROM programmer. The ROM cannot be clear and hence PROM is a one-time programmable device.

5. The PROM starts out with _____
a) 1s
b) 0s
c) Null
d) Both 1s and 0s

Answer: b
Explanation: PROM is a one-time programmable device, which is programmed by the user. The PROM starts out with all 0s. These current pulses blow the fuse links, thus creating the desire pattern.

6. For the implementation of PROM, which IC is used?
a) IC 74187
b) IC 74186
c) IC 74185
d) IC 74184

Answer: b
Explanation: For implementation of PROM, IC 74186 is used. IC 74186 is of 512 bits (62 * 8 = 512). Thus, it has 62 rows and 8 columns.

7. IC 74186 is of _____
a) 1024 bits
b) 32 bits
c) 512 bits
d) 64 bits

Answer: c
Explanation: IC 74186 is of 512 bits (62 * 8 = 512). Thus, it has 62 rows and 8 columns.

8. How many memory locations are addressed using 18 address bits?
a) 165,667
b) 245,784
c) 262,144
d) 212,342

Answer: c
Explanation: For n address bits, the memory location will consist of 2^n bits. Using 18 address bits, 2^{18} = 262,144 (= 256 K) words are addressed.

9. How many address bits are needed to operate a 2K * 8-bit memory?
a) 10
b) 11
c) 12
d) 13

Answer: b
Explanation: For n address bits, the memory location will consist of 2^n bits. Thus, for 2K, only 11 address bits are required, because 2^{11} = 2K.

10. What is the bit storage capacity of a ROM with a 1024 × 8 organization?
a) 1024
b) 4096
c) 2048
d) 8192

Answer: d
Explanation: For n address bits, the memory location will consist of 2^n bits. 1024 = 2^{10} . So, $2^{10} * 2^3$ = 1024 * 8 = 8192 bit.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Erasable Programmable Read Only Memory”.

1. EPROM uses an array of _____
a) p-channel enhancement type MOSFET
b) n-channel enhancement type MOSFET
c) p-channel depletion type MOSFET
d) n-channel depletion type MOSFET

Answer: b
Explanation: EPROMs are Erasable Programmable ROMs which can be erased using UV radiation and re-programmed. EPROM uses an array of n-channel enhancement type MOSFET with an insulated gate structure.

2. The EPROM was invented by _____
a) Wen Tsing Chow
b) Dov Frohman
c) Luis O Brian
d) J P Longwell

Answer: b
Explanation: The EPROM was invented by Dov Frohman of Intel in 1971. EPROMs are Erasable Programmable ROMs which can be erased using UV radiation and re-programmed.

3. Address decoding for dynamic memory chip control may also be used for _____
a) Chip selection and address location
b) Read and write control
c) Controlling refresh circuits
d) Memory mapping

Answer: a
Explanation: Address decoding for dynamic memory chip control may also be used for chip selection and address location. Chip Selection enables or disables the functioning of the chip.

4. Which of the following describes the action of storing a bit of data in a mask ROM?
a) A 0 is stored by connecting the gate of a MOS cell to the address line
b) A 0 is stored in a bipolar cell by shorting the base connection to the address line
c) A 1 is stored by connecting the gate of a MOS cell to the address line
d) A 1 is stored in a bipolar cell by opening the base connection to the address line

Answer: c
Explanation: The action of storing a bit of data in a mask ROM is that when a 1 is stored by connecting the gate of a MOS cell to the address line. Mask ROMs are programmed by the manufacturer and are custom made as per the user.

5. The check sum method of testing a ROM _____
a) Allows data errors to be pinpointed to a specific memory location
b) Provides a means for locating and correcting data errors in specific memory locations
c) Indicates if the data in more than one memory location is incorrect
d) Simply indicates that the contents of the ROM are incorrect

Answer: d
Explanation: If checking of a sum method goes wrong, it simply indicates that the contents of the ROM are incorrect.

6. The initial values in all the cells of an EPROM is _____
a) 0
b) 1
c) Both 0 and 1
d) Alternate 0s and 1s

Answer: b
Explanation: The initial values in all the cells of an EPROM is 1.

7. To store 0 in such a cell, the floating point must be _____
a) Reprogrammed
b) Restarted
c) Charged
d) Power off

Answer: c
Explanation: EPROMs are Erasable Programmable ROMs which can be erased using UV radiation and re-programmed. To store 0 in the cell of an EPROM, the floating point must be charged.

8. The major disadvantage of RAM is?
a) Its access speed is too slow
b) Its matrix size is too big
c) It is volatile
d) High power consumption

Answer: c
Explanation: RAM is volatile memory. Thus, RAM stores the data as long as it is powered on and once the power goes out, it loses its data.

9. Which one of the following is used for the fabrication of MOS EPROM?
a) TMS 2513
b) TMS 2515
c) TMS 2516
d) TMS 2518

Answer: c
Explanation: EPROMs are Erasable Programmable ROMs which can be erased using UV radiation and re-programmed. TMS 2516 is a MOS EPROM device.

10. How many addresses a MOS EPROM have?
a) 1024
b) 512
c) 2516
d) 256

Answer: c
Explanation: EPROMs are Erasable Programmable ROMs which can be erased using UV radiation and re-programmed. MOS EPROM (i.e. TMS 2516) has 2048 ($2^{11} = 2048$) addresses.

11. To read from the memory, the select input and the power down/program input must be _____
a) HIGH
b) LOW
c) Sometimes HIGH and sometimes LOW
d) Alternate HIGH and LOW

Answer: b
Explanation: To read from the memory, the select input and the power down/program input must be LOW.

12. ROMs retain data when _____
a) Power is on
b) Power is off
c) System is down
d) All of the Mentioned

Answer: d
Explanation: ROM retains the data when power is off/on/down because it has to read the data from memory only and it is done in every condition. It is non-volatile memory.

13. Suppose that a certain semiconductor memory chip has a capacity of 8K × 8. How many bytes could be stored in this device?
a) 8,000
b) 65,536
c) 8,192
d) 64,000

Answer: c
Explanation: 8K = 8 * 1024 = 8192.

14. When a RAM module passes the checker board test it is _____
a) Able to read and write only 0s
b) Faulty
c) Probably good

d) Able to read and write only 1s

Answer: c
Explanation: When a RAM module passes the checker board test it is probably good. It is a volatile memory. Thus, RAM stores the data as long as it is powered on and once the power goes out, it loses its data.

15. What is the difference between static RAM and dynamic RAM?
a) Static RAM must be refreshed, dynamic RAM does not
b) There is no difference
c) Dynamic RAM must be refreshed, static RAM does not
d) SRAM is slower than DRAM

Answer: c
Explanation: Dynamic RAM must be refreshed because it made up of capacitor, and capacitor required refresh. Static RAM made up of flip flop and it doesn't required a refresh.

This set of tough Digital Electronic/Circuits Questions focuses on "Random Access Memory-2".

1. The memory capacity of a static RAM varies from _____
a) 32 bit to 64 bit
b) 64 bit to 1024 bit
c) 64 bit to 1 Mega bit
d) 512 bit to 1 Mega bit

Answer: c
Explanation: Static RAM(SRAM) is faster than dynamic RAM(DRAM) as the access time for DRAM is more compared to that of SRAM. The memory capacity of a static RAM varies from 64 bits to 1 Mega bit.

2. The input data bit is written into the cell by setting _____
a) The flip-flop for 1
b) Resetting the flip-flop
c) The flip-flop for HIGH
d) Both the flip-flop for 1 and resetting the flip-flop

Answer: d
Explanation: The input data bit (1 or 0) is written into the cell by setting the flip-flop for 1 and the resetting the flip-flop for a 0 when the R/W' line is low, R/W is active-low pin.

3. When the READ/(WRITE)' line is HIGH then the flip-flop is _____
a) Activated
b) Deactivated
c) Unaffected
d) Both activated and deactivated

Answer: c
Explanation: When the READ/(WRITE)' line is HIGH then the flip-flop is unaffected since it's an active low pin. It means that the stored bit (data) is gated to the data out line.

4. The flip-flop in static memory cell can be constructed using _____
a) Capacitor or MOSFET
b) FET or JFET
c) Capacitor or BJT
d) BJT or MOSFET

Answer: d
Explanation: The flip-flop in the static memory cell can be constructed using Bipolar Junction Transistor (BJT) and MOSFETs because of it's storing capability. Also, it's access time is less and it is faster in operation.

5. Which of the following IC is TTL based static RAM?
a) IC 7488
b) IC 7489
c) IC 7487
d) IC 2114

Answer: b
Explanation: The flip-flop in the static memory cell can be constructed using Bipolar Junction Transistor (BJT) and MOSFETs because of it’s storing capability. Also, it’s access time is less and it is faster in operation. In IC 7489, TTL is used which is static RAM.

6. IC 7489 is of _____
a) 32 bit
b) 64 bit
c) 512 bit
d) 1024 bit

Answer: b
Explanation: The arrangement of IC 7489 is 16 * 4 = 64 bits. Thus, it has 16 columns and 4 rows.

7. Data is written in IC 7489 through _____
a) Chip select
b) Enable
c) Data input
d) Memory enable

Answer: c
Explanation: Data can be written into the memory via the data inputs by supplying an address to the SELECT inputs and holding both the memory enable and write enable LOW.

8. The first practical form of Random Access Memory (RAM) was the _____
a) Cathode tube
b) Data tube
c) Memory tube
d) Select tube

Answer: c
Explanation: Data can be written into the memory via the data inputs by supplying an address to the SELECT inputs and holding both the memory enable and write enable LOW since it’s an active-low pin.

9. Magnetic-core memory was invented in _____
a) 1946
b) 1948
c) 1947
d) 1945

Answer: c
Explanation: Magnetic-core memory was invented in 1947 and developed up until the mid-1970s. It became a widespread form of random-access memory, relying on an array of magnetized rings. RAM is a volatile memory, therefore it stores data as long as power is on. RAM is also known as RWM (i.e. Read Write Memory).

10. Which of the following RAM is volatile in nature?
a) SRAM
b) DRAM
c) EEPROM
d) Both SRAM and DRAM

Answer: d
Explanation: RAM is a volatile memory, therefore it stores data as long as power is on. RAM is also known as RWM (i.e. Read Write Memory). Both static and dynamic RAM are considered volatile, as their state is lost or reset when power is removed from the system.

11. Which one of the following IC is of 4KB?
a) IC 7488
b) IC 7489
c) IC 7487
d) IC 2114

Answer: d
Explanation: IC 2114 is of 4KB and it is a static RAM. Both static and dynamic RAM are considered volatile, as their state is lost or reset when power is removed from the system.

12. Which of the following IC implements the static MOS RAM?
a) TMS 4015
b) TMS 4014
c) TMS 4016
d) TMS 2114

Answer: c
Explanation: The IC TMS 4016 is a 2KB static MOS RAM. There are eleven address inputs available to select the 2014 locations.

13. What types of arrangements a TMS 4016 has?
a) 1024 * 4
b) 1024 * 8
c) 2048 * 4
d) 2048 * 8

Answer: d
Explanation: The IC TMS 4016 is a 2KB static MOS RAM. There are eleven address inputs available to select the 2014 locations.
Therefore, arrangements in TMS 4016 = 2048 * 8 = 2KB.

14. How many address inputs are available in TMS 4016?
a) 10
b) 9
c) 12
d) 11

Answer: d
Explanation: The IC TMS 4016 is a 2KB static MOS RAM. There are eleven address inputs available to select the 2014 locations.

15. In TMS 4016, the data in/data out are _____
a) Unidirectional
b) Parallel
c) Serial
d) Bidirectional

Answer: d
Explanation: In TMS 4016, the data in/data out are bidirectional terminal. It means that the input/output can be transmitted or received through the same terminal.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Random Access Memory – 1”.

1. What is the access time?
a) The time taken to move a stored word from one bit to other bits after applying the address bits
b) The time taken to write a word after applying the address bits
c) The time taken to read a stored word after applying the address bits
d) The time taken to erase a stored word after applying the address bits

Answer: c
Explanation: The access time is the time taken to read a stored word after applying the address bits in a MOS EPROM. It is the time required to fetch data from the memory.

2. What are the typical values of tOE?
a) 10 to 20 ns for bipolar
b) 25 to 100 ns for NMOS
c) 12 to 50 ns for CMOS
d) All of the Mentioned

Answer: d
Explanation: The access time is the time taken to read a stored word after applying the address bits in a MOS EPROM. It is the time required to fetch data from the memory. The typical values of tOE (i.e. access time) are 10 to 20 ns for bipolar, 25 to 100 ns for NMOS and 12 to 50 ns for CMOS.

3. Which of the following is not a type of memory?
a) RAM
b) FPROM
c) EEPROM
d) ROM

Answer: c
Explanation: EEPROM (Electrical Erasable Programmable ROM) is not a type of memory because it is used for erasing purpose only. Through EEPROM, data can be erased electrically, thereby consuming less time.

4. The chip by which both the operation of read and write is performed _____
a) RAM
b) ROM
c) PROM
d) EPROM

Answer: a
Explanation: A Random Access Memory (RAM) is a volatile chip memory in which both the read and write operations can be performed. Since it is volatile, therefore it stores data as long as power is on.

5. RAM is also known as _____
a) RWM
b) MBR
c) MAR
d) ROM

Answer: a
Explanation: A Random Access Memory (RAM) is a volatile chip memory in which both the read and write operations can be performed. Since it is volatile, therefore it stores data as long as power is on. RAM is also known as RWM (i.e. Read Write Memory).

6. If a RAM chip has n address input lines then it can access memory locations upto _____
a) $2^{(n-1)}$
b) $2^{(n+1)}$
c) 2^{n}
d) 2^{2n}

Answer: c
Explanation: RAM is a volatile memory, therefore it stores data as long as power is on. RAM is also known as RWM (i.e. Read Write Memory). If a RAM chip has n address input lines then it can access memory locations upto 2^{n} .

7. The n-bit address is placed in the _____
a) MBR
b) MAR
c) RAM
d) ROM

Answer: b
Explanation: The n-bit address is placed in the Memory Address Register (MAR) to select one of 2^{n} memory locations. It stores the address of the instruction which is to be executed next.

8. Which of the following control signals are selected for read and write operations in a RAM?
a) Data buffer
b) Chip select

c) Read and write
d) Memory

Answer: c
Explanation: Read and write are control signals that are used to enable memory for read and write operations respectively.

9. Computers invariably use RAM for _____
a) High complexity
b) High resolution
c) High speed main memory
d) High flexibility

Answer: c
Explanation: RAM is a volatile memory, therefore it stores data as long as power is on. RAM is also known as RWM (i.e. Read Write Memory). Computers invariably use RAM for their high high-speed main memory and then use backup or slower-speed memories to hold auxiliary data.

10. How many types of RAMs are?
a) 2
b) 3
c) 4
d) 5

Answer: a
Explanation: There are two types of RAM and these are static and dynamic. Static RAM(SRAM) is faster than dynamic RAM(DRAM) as the access time for DRAM is more compared to that of SRAM.

11. Static RAM employs _____
a) BJT or MOSFET
b) FET or JFET
c) Capacitor or BJT
d) BJT or MOS

Answer: d
Explanation: Static RAM employs bipolar or MOS flip-flops because both the semiconductor has storing capacity. Thus, it’s access time is less and it is faster in operation.

12. Dynamic RAM employs _____
a) Capacitor or MOSFET
b) FET or JFET
c) Capacitor or BJT
d) BJT or MOS

Answer: a
Explanation: Dynamic RAM employs a capacitor or MOSFET. Thus, it’s access time is more and it is slower in operation.

13. Which one of the following is volatile in nature?
a) ROM
b) EROM
c) PROM
d) RAM

Answer: d
Explanation: RAM is a volatile memory, therefore it stores data as long as power is on. RAM is also known as RWM (i.e. Read Write Memory). RAMs are volatile because the stored data will be lost once the d.c. power applied to the flip-flops is removed.

14. The magnetic core memories have been replaced by semiconductor RAMs, why?
a) Semiconductor RAMs are highly flexible
b) Semiconductor RAMs have highest storing capacity
c) Semiconductor RAMs are smaller in size
d) All of the Mentioned

Answer: d
Explanation: RAM is a volatile memory, therefore it stores data as long as power is on. RAM is also known as RWM (i.e. Read Write Memory). The magnetic core memories have been replaced by semiconductor RAMs because of smaller in size, high storing capacity as well as flexibility.

15. The data written in flip-flop remains stored as long as _____
a) D.C. power is supplied
b) D.C. power is removed
c) A.C. power is supplied
d) A.C. power is removed

Answer: a
Explanation: Since flip-flops are made up of semiconductor materials. So, it can't accept A.C. source and the data written in flip-flop remains stored as long as the dc power is maintained.

This set of tough Digital Electronic/Circuits questions and answers focuses on "Random Access Memory-3".

1. Dynamic RAM is more preferable than static RAM, why?
a) DRAM is of the lowest cost, lowest density
b) DRAM is of the highest cost, reduced size
c) DRAM is of the lowest cost, highest density
d) DRAM is more flexible and lowest storage capacity

Answer: c
Explanation: The Dynamic Random Access Memory is the lowest cost, highest density random access memory available. Nowadays, computers use DRAM for main memory. However, it's access time is more compared to SRAM.

2. The memory size of DRAM is _____
a) 1 to 100 MB
b) 512 to 1024 MB
c) 64 to 512 MB
d) 16 to 256 MB

Answer: d
Explanation: The Dynamic Random Access Memory is the lowest cost, highest density random access memory available. Nowadays, computers use DRAM for main memory. However, it's access time is more compared to SRAM. The memory size of DRAM lies between 16 to 256 MB.

3. The DRAM stores its binary information on _____
a) MOSFET
b) Transistor
c) Capacitor
d) BJT

Answer: c
Explanation: Capacitor has high storing capability only, so DRAM stores its binary information in the form of electric charges on capacitors. However, DRAM takes more time time to access data.

4. Most modern operating systems employ a method of extending RAM capacity, known as _____
a) Magnetic memory
b) Virtual memory
c) Storage memory
d) Static memory

Answer: b
Explanation: Most modern operating systems employ a method of extending RAM capacity, known as virtual memory. Virtual memory is seen as part of main memory but is actually a secondary memory.

5. DRAM uses of integrated MOS capacitors as _____ instead of a flip-flop.
a) Storage cell
b) Memory cell
c) Dynamic cell
d) Static cell

Answer: b
Explanation: DRAM uses of integrated MOS capacitors as memory cell instead of a flip-flop. The advantage of this cell is that it allows very large memory arrays to be constructed on a chip at a lower cost per bit than in static memories.

6. What is the disadvantage of MOS capacitor in DRAM?
a) It can't hold the data till a long period
b) It doesn't holds the charge till a long period
c) It is highly densed
d) It is not flexible

Answer: b
Explanation: The disadvantage of MOS capacitor in DRAM is that it can't hold the stored charge over a long period of time and it has to be refreshed every few millisecond. Thus, DRAM is slow in operation.

7. The dynamic RAM offers _____
a) High power consumption, large storage capacity
b) Reduced power consumption, large storage capacity
c) Reduced power consumption, short storage capacity
d) High power consumption, short storage capacity

Answer: b
Explanation: The dynamic RAM offers reduced power consumption and large storage capacity in a single memory chip. With the availability of such high packing density memory ICs, the capacity of memory will continue to grow. However, it's access time is more and thus operation is slow.

8. The main memory of a PC is made of _____
a) Cache
b) Dynamic RAM
c) Static RAM
d) Both cache and dynamic RAM

Answer: d
Explanation: The main memory of a PC is made of cache and DRAM. DRAM offers reduced power consumption and large storage capacity in a single memory chip.

9. Virtual memory consists of _____
a) SRAM
b) DRAM
c) Magnetic memory
d) Main Memory

Answer: a
Explanation: Most modern operating systems employ a method of extending RAM capacity, known as virtual memory which consists of SRAM.

10. Dynamic RAM is used as main memory in a computer system as _____
a) It has a lower cell density
b) It needs refreshing circuitry
c) Consumes less power
d) Has higher speed

Answer: d
Explanation: Dynamic RAM is used as main memory in a computer system as it has a higher speed due to the presence of MOSFET technology. However, it's access time is more compared to SRAM and operation is slow.

11. Cache memory acts between _____
a) RAM and ROM
b) CPU and RAM
c) CPU and Hard Disk
d) CPU and ROM

Answer: b
Explanation: In a computer, cache memory acts between CPU and RAM.

12. Which characteristic of RAM memory makes it not suitable for permanent storage?
a) Unreliable
b) Too slow
c) Too bulky
d) It is volatile

Answer: d
Explanation: RAM is volatile. Therefore, it stores data only as long as the d.c power is on.

13. Why do a DRAM employ the address multiplexing technique?
a) To reduce the number of memory locations
b) To increase the number of memory locations
c) To reduce the number of address lines
d) To increase the number of address lines

Answer: c
Explanation: A Dynamic RAM usually employs a technique called address multiplexing to reduce the number of address lines and thus the number of input/output pins on the IC package.

14. An address multiplexing in DRAM is of _____ bits.
a) 10240
b) 15289
c) 16384
d) 17654

Answer: c
Explanation: A Dynamic RAM usually employs a technique called address multiplexing to reduce the number of address lines and thus the number of input/output pins on the IC package.
Address multiplexing has 2^{14} = 16384 bits.

15. What is a sense amplifier?
a) It is an amplifier which converts ac current into dc current
b) It is an amplifier which lowers the input voltage
c) It is an amplifier which increases the input voltage
d) It is an amplifier which converts the low voltage to a sufficient voltage

Answer: d
Explanation: A sense amplifier for each column is necessary to convert from the low voltage and low energy to a sufficient level on the I/O data line.

This set of Basic Digital Electronic/Circuits Interview questions and answers focuses on “Random Access Memory-4”.

1. DRAM is fabricated by using IC _____
a) 2114
b) 7489
c) 4116
d) 2776

Answer: c
Explanation: DRAM is Dynamic RAM which takes more access time compared to SRAM and is thus, slower in operation comparatively. Although, in general it offers high speed and is used in most computers nowadays. DRAM is fabricated by using IC 4116.

2. IC 4116 is of _____ storage memory.
a) 16 KB

b) 32 KB
c) 64 MB
d) 2 KB

Answer: a
Explanation: IC 4116 is a DRAM of 16 KB storage memory. It requires three supply voltages (+5V, -5V, and +12V) to operate the IC unit.

3. How many supply voltage IC 4116 requires to operate the IC unit?
a) 3
b) 2
c) 1
d) 4

Answer: a
Explanation: IC 4116 is a DRAM of 16 KB storage memory. It requires three supply voltages (+5V, -5V, and +12V) to operate the IC unit.

4. The full form of PSRAM is _____
a) Plugged Static RAM
b) Plugged Stored RAM
c) Pseudo Stored RAM
d) Pseudo Static RAM

Answer: d
Explanation: The full form of PSRAM is Pseudo Static RAM. It is a dynamic RAM which is implemented as a SRAM.

5. Pseudo static RAM is a _____
a) Static RAM
b) Dynamic RAM
c) Cache
d) ROM

Answer: b
Explanation: The full form of PSRAM is Pseudo Static RAM. It is a dynamic RAM having built-in fresh logic, which is implemented as an SRAM.

6. When PSRAM is performing internal refresh _____
a) The read operation is performed
b) The write operation is performed
c) It can not be accessed for read or write
d) The voltage goes HIGH

Answer: c
Explanation: The full form of PSRAM is Pseudo Static RAM. It is a dynamic RAM having built-in fresh logic, which is implemented as a SRAM. So, it can not be accessed for read or write during the refresh operation.

7. RAMs are utilized in the computer as _____
a) Scratch-pad
b) Buffer
c) Main memory
d) All of the Mentioned

Answer: d
Explanation: RAMs are utilized in the computer as a scratch-pad, buffer and main memories. These are the applications of RAMs. Mostly, these RAMs are DRAMs as they provide high speed.

8. The advantages of RAMs are _____
a) Non destructive read out
b) Fast operating speed
c) Low power dissipation
d) All of the Mentioned

Answer: d
Explanation: The advantages of RAM are Non-destructive read out, Fast operating speed and Low power dissipation.

9. Which one is more economical?
a) ROM
b) RAM
c) EROM
d) PROM

Answer: b
Explanation: RAM is more economical than ROM because MOS memories are more economical than the magnetic core for small and medium sized systems.

10. Which one is self-compatible?
a) ROM
b) RAM
c) EROM
d) PROM

Answer: b
Explanation: As semiconductor memories enjoy common interface and technology between sensing and decoding circuitry and the storage element itself, so RAMs are self-compatible. Also, they provide high speed and fast operation.

11. The memory which is used for storing programs and data currently being processed by the CPU is called _____
a) PROM
b) Main Memory
c) Non-volatile memory
d) Mass memory

Answer: a
Explanation: PROM has the capability to store the data due to the presence of MOSFET which is processed by the CPU. It is one-time programmable by the user.

12. CD-ROM is a _____
a) Memory register
b) Magnetic memory
c) Semiconductor memory
d) Non-volatile memory

Answer: d
Explanation: CD-ROM is a non-volatile memory. Once a program is uploaded in it then it can’t be erasable. Thus, it stores the data permanently.

13. A place which is used as storage location in a computer _____
a) A bit
b) A record
c) An address
d) A byte

Answer: c
Explanation: A storage location of a computer is an address/memory location, used to store instructions and data.

14. Which of the following is not a primary storage device?
a) Optical disk
b) Magnetic tape
c) Magnetic disk
d) RAM

Answer: d
Explanation: RAM (i.e. Random Access Memory) is not a primary storage device.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Programmable Logic Array”.

1. What is memory decoding?
a) The process of Memory IC used in a digital system is overloaded with data
b) The process of Memory IC used in a digital system is selected for the range of address assigned
c) The process of Memory IC used in a digital system is selected for the range of data assigned

d) The process of Memory IC used in a digital system is overloaded with data allocated in memory cell

Answer: b
Explanation: The Memory IC used in a digital system is selected or enabled only for the range of addresses assigned to it and this process is called memory decoding. It decodes the memory to be selected for a specific address.

2. The first step in the design of memory decoder is _____
a) Selection of a EPROM
b) Selection of a RAM
c) Address assignment
d) Data insertion

Answer: c
Explanation: Memory decoder decodes the memory to be selected for a specific address. The first step in the design of memory decoder is address assignment in non-overlapped manner.

3. How many address bits are required to select memory location in the Memory decoder?
a) 4 KB
b) 8 KB
c) 12 KB
d) 16 KB

Answer: c
Explanation: Memory decoder decodes the memory to be selected for a specific address. Since the given EPROM and RAM are of 4 KB (4 * 1024 = 4096) capacity, it requires 12 address bit to select one of the 4096 memory locations.

4. How memory expansion is done?
a) By increasing the supply voltage of the Memory ICs
b) By decreasing the supply voltage of the Memory ICs
c) By connecting Memory ICs together
d) By separating Memory ICs

Answer: c
Explanation: Memory ICs can be connected together to expand the number of memory words or the number of bits per word.

5. IC 4116 is organised as _____
a) 512 * 4
b) 16 * 1
c) 32 * 4
d) 64 * 2

Answer: c
Explanation: IC 4116 is organised as 16 * 1 K which has capability to store 16 KB.

6. To construct 16K * 4-bit memory, how many 4116 ICs are required?
a) 1
b) 2
c) 3
d) 4

Answer: d
Explanation: Since, IC 4116 is organised as 16K * 1, which can store about 16KB data. So, four ICs are required for 16K * 4 memory implementation.

7. How many 1024 * 1 RAM chips are required to construct a 1024 * 8 memory system?
a) 4
b) 6
c) 8
d) 12

Answer: c
Explanation: One 1024 * 1 RAM chips is of 1-bit. SO, for construction of 1024 * 8 RAM chip of 8-bits, it will require 8 chips.

8. How many 16K * 4 RAMs are required to achieve a memory with a capacity of 64K and a word length of 8 bits?
a) 2
b) 4
c) 6
d) 8

Answer: d
Explanation: 16K * 4 = 64K RAM is of 64K. Therefore, for a word of length 8-bits,
64 * 8 = 512K RAM required. Thus, number of 16K * 4 RAMs = 512/64 = 8.

9. The full form of PLD is _____
a) Programmable Load Devices
b) Programmable Logic Data
c) Programmable Logic Devices
d) Programmable Loaded Devices

Answer: c
Explanation: The full form of PLD is Programmable Logic Devices. It is a collection of gates, flip-flops and registers on a single chip.

10. PLD contains a large number of _____
a) Flip-flops
b) Gates
c) Registers
d) All of the Mentioned

Answer: d
Explanation: Programmable Logic Devices is a collection of a large number of gates, flip-flops, registers that are interconnected on the chip. Thus, it is used for designing logic circuits.

11. Logic circuits can also be designed using _____
a) RAM
b) ROM
c) PLD
d) PLA

Answer: c
Explanation: Programmable Logic Devices is a collection of large number of gates, flip-flops, registers that are interconnected on the chip. Thus, it is used for designing logic circuits.

12. In PLD, there are provisions to perform interconnections of the gates internally, because of _____
a) High reliability
b) High conductivity
c) The desired logic implementation
d) The desired output

Answer: c
Explanation: Programmable Logic Devices is a collection of a large number of gates, flip-flops,

registers that are interconnected on the chip. In PLD, there are provisions to perform interconnections of the gates internally so that the desired logic can be implemented.

13. Why antifuses are implemented in a PLD?
a) To protect from high voltage
b) To increase the memory
c) To implement the programmes
d) As a switching devices

Answer: c
Explanation: Programmable Logic Devices is a collection of a large number of gates, flip-flops, registers that are interconnected on the chip. Programming is accomplished by using antifuses in a PLD and it is fabricated at the cross points of the gates.

14. How many types of PLD is?
a) 2
b) 3
c) 4
d) 5

Answer: a
Explanation: There are two types of PLD, viz., devices with fixed architecture and devices with a flexible architecture. The main categories of PLDs are PROM, PAL and PLA.

15. PLA refers to _____
a) Programmable Loaded Array
b) Programmable Array Logic
c) Programmable Logic Array
d) Programmed Array Logic

Answer: c
Explanation: PLA refers to Programmable Logic Array. It is a type of PLD having programmable AND and OR gates.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Programmable Array Logic”.

1. The inputs in the PLD is given through _____
a) NAND gates
b) OR gates
c) NOR gates
d) AND gates

Answer: d
Explanation: The inputs in the PLD is given through AND gate followed by inverting & non-inverting buffer. PLDs are Programmable Logic Devices consisting of logic gates, flip-flops and registers connected together on a single chip. Thus, it can be categorised into PROM, PAL and PLA.

2. PAL refers to _____
a) Programmable Array Loaded
b) Programmable Logic Array
c) Programmable Array Logic
d) Programmable AND Logic

Answer: c
Explanation: PAL refers to Programmable Array Logic consisting of programmable AND gates and fixed OR gates.

3. Outputs of the AND gate in PLD is known as _____
a) Input lines
b) Output lines
c) Strobe lines
d) Control lines

Answer: b
Explanation: Outputs of the AND gate in PLD is known as output lines.

4. PLA contains _____
a) AND and OR arrays
b) NAND and OR arrays
c) NOT and AND arrays
d) NOR and OR arrays

Answer: a
Explanation: Programmable Logic Array is a type of fixed architecture logic devices with programmable AND gates followed by programmable OR gates. It is a kind of PLD.

5. PLA is used to implement _____
a) A complex sequential circuit
b) A simple sequential circuit
c) A complex combinational circuit
d) A simple combinational circuit

Answer: c
Explanation: Since, PLA is a combination of programmable AND and OR gates. So, it is used to implement complex combinational circuit.

6. A PLA is similar to a ROM in concept except that _____
a) It hasn’t capability to read only
b) It hasn’t capability to read or write operation
c) It doesn’t provide full decoding to the variables
d) It hasn’t capability to write only

Answer: c
Explanation: A PLA is similar to a ROM in concept except that it doesn’t provide full decoding to the variables and doesn’t generate all the minterms as in the ROM. Programmable Logic Array is a type of fixed architecture logic devices with programmable AND gates followed by programmable OR gates. It is a kind of PLD.

7. For programmable logic functions, which type of PLD should be used?
a) PLA
b) PAL
c) CPLD
d) SLD

Answer: b
Explanation: Since PAL consists of programmable AND gates and fixed OR gates and also circuitry working is less.

8. The complex programmable logic device contains several PLD blocks and _____
a) A language compiler
b) AND/OR arrays
c) Global interconnection matrix
d) Field-programmable switches

Answer: c
Explanation: The complex programmable logic device contains several PLD blocks and a global interconnection matrix by which it communicates through several devices. It is also known as Field-Programmable Gate Arrays (FPGAs).

9. Which type of device FPGA are?
a) SLD
b) SROM
c) EPROM
d) PLD

Answer: d
Explanation: Field-Programmable Gate Arrays (FPGAs) are reprogrammable silicon chips. In contrast to processors that you find in your PC, programming an FPGA rewires the chip itself to

implement your functionality rather than run a software application. Thus, FPGAs are PLD devices.

10. The difference between a PAL & a PLA is _____
a) PALs and PLAs are the same thing
b) The PLA has a programmable OR plane and a programmable AND plane, while the PAL only has a programmable AND plane
c) The PAL has a programmable OR plane and a programmable AND plane, while the PLA only has a programmable AND plane
d) The PAL has more possible product terms than the PLA

Answer: b
Explanation: The main difference between a PAL & PLA is that PLA has a programmable OR plane and a programmable AND plane, while the PAL only has a programmable AND plane and a fixed OR plane.

11. If a PAL has been programmed once _____
a) Its logic capacity is lost
b) Its outputs are only active HIGH
c) Its outputs are only active LOW
d) It cannot be reprogrammed

Answer: d
Explanation: PAL only has a programmable AND plane and a fixed OR plane. Since, PAL is dynamic in nature. So, it can’t be reprogrammed.

12. The FPGA refers to _____
a) First programmable Gate Array
b) Field Programmable Gate Array
c) First Program Gate Array
d) Field Program Gate Array

Answer: b
Explanation: The FPGA refers to Field Programmable Gate Array. Field-Programmable Gate Arrays (FPGAs) are reprogrammable silicon chips. In contrast to processors that you find in your PC, programming an FPGA rewires the chip itself to implement your functionality rather than run a software application. Thus, FPGAs are PLD devices.

13. The full form of VLSI is _____
a) Very Long Single Integration
b) Very Least Scale Integration
c) Very Large Scale Integration
d) Very Long Scale Integration

Answer: c
Explanation: The full form of VLSI is Very Large Scale Integration in which FPGA is implemented.

14. In FPGA, vertical and horizontal directions are separated by _____
a) A line
b) A channel
c) A strobe
d) A flip-flop

Answer: b
Explanation: The FPGA refers to Field Programmable Gate Array. Field-Programmable Gate Arrays (FPGAs) are reprogrammable silicon chips. Vertical and horizontal directions is separated by a channel in an FPGA which determines the location of the output.

15. Applications of PLAs are _____
a) Registered PALs
b) Configurable PALs
c) PAL programming
d) All of the Mentioned

Answer: d
Explanation: Applications of PLAs are Registered PALs, Configurable PALs, and PAL programming and these are performed by using an extra flip-flop with PAL.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Introduction to hardware description language”.

1. The full form of HDL is _____
a) Higher Descriptive Language
b) Higher Definition Language
c) Hardware Description Language
d) High Descriptive Language

Answer: c
Explanation: The full form of HDL is Hardware Description Language.

2. The full form of VHDL is _____
a) Very High Descriptive Language
b) Verilog Hardware Description Language
c) Variable Definition Language
d) None of the Mentioned

Answer: b
Explanation: The full form of VHDL is Verilog Hardware Description Language.

3. VHSIC stands for _____
a) Very High Speed Integrated Circuits
b) Very Higher Speed Integration Circuits
c) Variable High Speed Integrated Circuits
d) Variable Higher Speed Integration Circuits

Answer: a
Explanation: VHSIC stands for Very High Speed Integrated Circuits.

4. VHDL is being used for _____
a) Documentation
b) Verification
c) Synthesis of large digital design
d) All of the Mentioned

Answer: d
Explanation: The full form of VHDL is Verilog Hardware Description Language. The acronym of VHDL itself captures the entire theme of the language and it describes the hardware in the same manner as does the schematic. So, it is used as documentation, verification and synthesis of large digital designs.

5. The use of VHDL can be done in _____ ways.
a) 2
b) 3
c) 4
d) 5

Answer: b
Explanation: The VHDL has three coding styles are: (i) data flow, (ii) structural, (iii) behavioural.

6. At high frequencies when the sampling interval is too long in a frequency counter _____
a) The counter works fine
b) The counter undercounts the frequency
c) The measurement is less precise
d) The counter overflows

Answer: d
Explanation: Let the sampling time be 1 sec. This means the counter will count the number of pulses from the unknown signal for 1sec duration and would display it after 1 sec. thus if the

signal is of 800 Hz, at the end of 1 sec, counter would have counted up to 800. Thus, in case of high frequencies and high sampling time, counter might count beyond its limit and overflows.

7. The output frequency related to the sampling interval of a frequency counter as _____
a) Directly with the sampling interval
b) Inversely with the sampling interval
c) More precision with longer sampling interval
d) Less precision with longer sampling interval

Answer: c
Explanation: Sampling interval means a particular frequency range in which the device operates correctly. Thus, more precision is produced with longer sampling interval.

8. In an HDL application of a stepper motor, what is done next after an up/down counter is built?
a) Build the sequencer
b) Test it on a simulator
c) Test the decoder
d) Design an intermediate integer variable

Answer: b
Explanation: Simulator is a software which is used in the testing of the stepper motor using up/down counter.

9. In a digital clock application, the basic frequency must be divided down as _____
a) 1 Hz
b) 60 Hz
c) 100 Hz
d) 1000 Hz

Answer: a
Explanation: Minimum count is 1 sec and time = 1/freq. So, t = 1/1 = 1Hz.

10. What does the data signal do in the keypad application?
a) The row and column encoded data
b) The ring encoded data
c) The freeze locator data
d) The ring counter data

Answer: a
Explanation: The data signal arranges the information with the help of data flow in row and column manner. It encodes the data to be sent.

11. When a key is pressed, what does the ring counter in the HDL keypad application do?
a) Count to find the row
b) Freeze
c) Count to find the column
d) Start the D flip-flop

Answer: a
Explanation: The data signal arranges the information with the help of data flow in row and column manner. It encodes the data to be sent. When a key is pressed the ring counter in the HDL scans the information provided by the user and counts to find the row.

12. A step which should be followed in project management is known as _____
a) Overall definition
b) System documentation
c) Synthesis and testing
d) System integration

Answer: b
Explanation: System documentation is the second step of project management in which a result of the system is noted simultaneously.

13. In the keypad application, the preset state of the ring counter define _____
a) The NANDing of the columns
b) The NANDing of the rows
c) The proper output of the column encoder
d) The proper output of the row encoder

Answer: d
Explanation: When a key is pressed the ring counter in the HDL scans the information provided by the user and counts to find the row. The preset state of the ring counter define the proper output of the row encoder.

14. A major block which is not a part of an HDL frequency counter _____
a) Timing and control unit
b) Decoder/display
c) Display register
d) Bit shifter

Answer: d
Explanation: Bit shifter is part of a register in which bit shifting takes place bit-by-bit either left or right.

15. A stepper motor HDL application must include _____
a) Sequencers and multiplexers
b) Types and bits
c) Counters and decoders
d) Variables and processes

Answer: c
Explanation: A stepper motor (also referred to as step or stepping motor) is an electromechanical device achieving mechanical movements through the conversion of electrical pulses. A stepper motor HDL application must include counters and decoders for position control. It is tested on the simulator.

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuses on “Multivibrators”.

1. A multivibrator is an electronic circuit used to implement _____
a) Oscillator
b) Timer
c) Flip-flop
d) All of the Mentioned

Answer: d
Explanation: A multivibrator is an electronic circuit used to implement a variety of simple two-state systems and two state systems are an oscillator, timer, flip-flop. It produces an output when triggered.

2. Multivibrators are characterized by _____
a) Registers
b) Capacitors
c) Transistors
d) All of the Mentioned

Answer: d
Explanation: A multivibrator is an electronic circuit used to implement a variety of simple two-state systems and two state systems are an oscillator, timer, flip-flop. It produces an output when triggered. Multivibrators are characterized by amplifying devices (transistors) and cross coupled devices (registers, capacitors).

3. How many types of multivibrators are?
a) 2
b) 4
c) 5
d) 3

Answer: d
Explanation: There are three types of multivibrator circuits depending on the circuit operation: (i) Astable, (ii) Bistable, and (iii) Monostable. Astable multivibrator is internally triggered, whereas the other two types are externally triggered.

4. Astable multivibrator is _____ in any state.
a) Stable
b) Unstable
c) Saturated
d) Both Stable & Saturated

Answer: b
Explanation: Astable multivibrator, in which the circuit is not stable in either state i.e. it continually switches from one state to the other. It is internally triggered and does not have any stable state.

5. Monostable multivibrator is/has _____ state.
a) Stable
b) Unstable
c) One stable and another unstable
d) Independent

Answer: b
Explanation: Monostable multivibrator, in which one of the states is stable, but the other state is unstable (transient). A trigger pulse causes the circuit to enter the unstable state. After entering the unstable state, the circuit will return to the stable state after a set time.

6. Bistable multivibrator is _____ in any state.
a) Stable
b) Unstable
c) Saturated
d) Independent

Answer: a
Explanation: Bistable multivibrator is a type of multivibrator having two stable states. The circuit is stable in either state. It can be flipped from one state to the other by an external trigger pulse.

7. Bistable circuit is also known as _____
a) Latch
b) Gate
c) Flip-flop
d) Bidirectional circuit

Answer: c
Explanation: Bistable multivibrator circuit has the capability to store 1-bit of information. So, it is also known as flip-flop. Like Flip-flop, Bistable circuit also has 2 states.

8. Astable circuit acts as a/an _____
a) Amplifier
b) Oscillator
c) Relaxation oscillator
d) Multiplexer

Answer: c
Explanation: Astable circuit continually switches from one state to the other. It keeps oscillating between unstable states. Hence, it functions as a relaxation oscillator.

9. In an astable multivibrator, the amplifying elements are _____
a) FET
b) JFET
c) OP-AMP
d) All of the Mentioned

Answer: d
Explanation: Astable multivibrators are made with FET, JFET, OP-AMP or other types of amplifier. Astable circuit continually switches from one state to the other. It keeps oscillating between unstable states.

10. Monostable multivibrator can also be termed as _____
a) Full astable multivibrator
b) Half astable multivibrator
c) Half bistable multivibrator
d) Full bistable multivibrator

Answer: b
Explanation: Since, astable multivibrator is unstable and changes their states continually (It means that it can have both the states), whereas in monostable multivibrator, one of the states is stable, but the other state is unstable. SO Monostable Multivibrator is also known as Half-Astable Multivibrator.

11. The classic multivibrator circuit is known as _____
a) Metal-coupled multivibrator
b) Plate-coupled multivibrator
c) Parallel-plate coupled multivibrator
d) Alternate-plate coupled multivibrator

Answer: b
Explanation: The classic multivibrator circuit (also called a plate-coupled multivibrator) is first described by Henri Abraham and Eugene Bloch.