

This set of Microprocessors Interview Questions and Answers focuses on "Instruction Set of 8086/8088 - 2".

1. The instruction, "INC" increases the contents of the specified register or memory location by

- a) 2
- b) 0
- c) 1
- d) 3

Answer: c

Explanation: This instruction adds 1 to the contents of the operand and so increments by 1.

2. The instruction that subtracts 1 from the contents of the specified register/memory location is

- a) INC
- b) SUBB
- c) SUB
- d) DEC

Answer: d

Explanation: The DEC instruction decrements the contents of a specified register/memory location by 1.

3. The instruction that enables subtraction with borrow is

- a) DEC
- b) SUB
- c) SBB
- d) None of the mentioned

Answer: c

Explanation: The SBB instruction subtracts the source operand and the borrow flag from the destination operand.

4. The flag that acts as Borrow flag in the instruction, SBB is

- a) direction flag
- b) carry flag
- c) parity flag
- d) trap flag

Answer: b

Explanation: If borrow exists in the subtraction operation performed then carry flag is set.

5. In general, the source operand of an instruction can be

- a) memory location
- b) register
- c) immediate data
- d) all of the mentioned

Answer: d

Explanation: The source operand is the element which is data or data stored memory location on which operation is performed.

6. In general, the destination operand of an instruction can be

- a) memory location
- b) register
- c) immediate data
- d) memory location and register

Answer: d

Explanation: Since the destination should be able to store the data, immediate data cannot be considered as a destination operand.

7. The instruction, CMP to compare source and destination operands it performs

- a) addition

- b) subtraction
- c) division
- d) multiplication

Answer: b

Explanation: For comparison, the instruction CMP subtracts source operand from destination operand.

8. During comparison operation, the result of comparing or subtraction is stored in

- a) memory
- b) registers
- c) stack
- d) no where

Answer: d

Explanation: The result of subtraction operation is not stored anywhere during a comparison.

9. The instruction that converts the result in an unpacked decimal digits is

- a) AAA
- b) AAS
- c) AAM
- d) All of the mentioned

Answer: d

Explanation: All the ASCII adjust instructions give result in unpacked decimal form and so are called as "Unpacked BCD arithmetic instructions".

10. Which of the following is a mnemonic?

- a) ADD
- b) ADC
- c) AAA
- d) ADD & ADC

Answer: c

Explanation: AAA is a mnemonic. It doesn't have either a source or destination operand.

11. The instruction in which adjustment is made before performing the operation is

- a) AAA
- b) AAS
- c) AAM
- d) AAD

Answer: d

Explanation: The AAD instruction converts two unpacked BCD digits in AH and AL to the equivalent binary number in AL. This adjustment must be made before dividing the two unpacked BCD digits.

12. The expansion of DAA is

- a) decimal adjust after addition
- b) decimal adjust before addition
- c) decimal adjust accumulator
- d) decimal adjust auxiliary

Answer: c

Explanation: This instruction performs conversion operation.

13. The instruction that is used to convert the result of the addition of two packed BCD numbers to a valid BCD number is

- a) DAA
- b) DAS
- c) AAA
- d) AAS

Answer: a

Explanation: In this conversion, the result has to be only in AL.

14. The ROR instruction rotates the contents of the destination operand to
- a) left
 - b) right
 - c) left and then right
 - d) right and then left

Answer: b

Explanation: ROR stands for Rotate Right without carry. so, the instruction rotates right.

To practice all areas of Microprocessors for Interviews, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Addressing Modes of 8086".

1. The instruction, MOV AX, 0005H belongs to the address mode
- a) register
 - b) direct
 - c) immediate
 - d) register relative

Answer: c

Explanation: In Immediate addressing mode, immediate data is a part of instruction and appears in the form of successive byte or bytes.

2. The instruction, MOV AX, 1234H is an example of
- a) register addressing mode
 - b) direct addressing mode
 - c) immediate addressing mode
 - d) based indexed addressing mode

Answer: c

Explanation: Since immediate data is present in the instruction.

3. The instruction, MOV AX, [2500H] is an example of
- a) immediate addressing mode
 - b) direct addressing mode
 - c) indirect addressing mode
 - d) register addressing mode

Answer: b

Explanation: Since the address is directly specified in the instruction as a part of it.

4. If the data is present in a register and it is referred using the particular register, then it is
- a) direct addressing mode
 - b) register addressing mode
 - c) indexed addressing mode
 - d) immediate addressing mode

Answer: b

Explanation: Since register is used to refer the address.

5. The instruction, MOV AX,[BX] is an example of
- a) direct addressing mode
 - b) register addressing mode
 - c) register relative addressing mode
 - d) register indirect addressing mode

Answer: d

Explanation: Since the register used to refer to the address is accessed indirectly.

6. If the offset of the operand is stored in one of the index registers, then it is
- a) based indexed addressing mode
 - b) relative based indexed addressing mode
 - c) indexed addressing mode
 - d) none of the mentioned

Answer: c

Explanation: In the indexed addressing mode, the offset of an operand is stored and in the rest of them, address is stored.

7. The addressing mode that is used in unconditional branch instructions is

- a) intrasegment direct addressing mode
- b) intrasegment indirect addressing mode
- c) intrasegment direct and indirect addressing mode
- d) intersegment direct addressing mode

Answer: b

Explanation: In intrasegment indirect mode, the branch address is found as the content of a register or a memory location.

8. If the location to which the control is to be transferred lies in a different segment other than the current one, then the mode is called

- a) intrasegment mode
- b) intersegment direct mode
- c) intersegment indirect mode
- d) intersegment direct and indirect mode

Answer: d

Explanation: In intersegment mode, the control to be transferred lies in a different segment.

9. The instruction, JMP 5000H:2000H; is an example of

- a) intrasegment direct mode
- b) intrasegment indirect mode
- c) intersegment direct mode
- d) intersegment indirect mode

Answer: c

Explanation: Since in intersegment direct mode, the address to which the control is to be transferred is in a different segment.

10. The contents of a base register are added to the contents of index register in

- a) indexed addressing mode
- b) based indexed addressing mode
- c) relative based indexed addressing mode
- d) based indexed and relative based indexed addressing mode

Answer: d

Explanation: The effective address is formed by adding the contents of both base and index registers to a default segment.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessors Questions and Answers for Freshers focuses on "Instruction Set of 8086/8088 - 3".

1. The mnemonic that is placed before the arithmetic operation is performed is

- a) AAA
- b) AAS
- c) AAM
- d) AAD

Answer: d

Explanation: The AAD instruction converts two unpacked BCD digits in AH and AL to the equivalent binary number in AL.

2. The Carry flag is undefined after performing the operation

- a) AAA
- b) ADC
- c) AAM
- d) AAD

Answer: d

Explanation: Since the operation, AAD is performed before division operation is performed, the carry flag, auxiliary flag and overflow flag are undefined.

3. The instruction that performs logical AND operation and the result of the operation is not available is

- a) AAA
- b) AND
- c) TEST
- d) XOR

Answer: c

Explanation: In the TEST instruction, the logical AND operation is performed and the result is not stored but flags are affected.

4. In the RCL instruction, the contents of the destination operand undergo function as

- a) carry flag is pushed into LSB & MSB is pushed into the carry flag
- b) carry flag is pushed into MSB & LSB is pushed into the carry flag
- c) auxiliary flag is pushed into LSB & MSB is pushed into the carry flag
- d) parity flag is pushed into MSB & LSB is pushed into the carry flag

Answer: a

Explanation: In RCL(Rotate right through carry), for each operation, the carry flag is pushed into LSB and the MSB of the operand is pushed into carry flag.

5. The instruction that is used as prefix to an instruction to execute it repeatedly until the CX register becomes zero is

- a) SCAS
- b) REP
- c) CMPS
- d) STOS

Answer: b

Explanation: The instruction to which the REP is prefix, is executed repeatedly until CX register becomes zero. When CX becomes zero, the execution proceeds to the next instruction in sequence.

6. Match the following

- | | |
|-------------|--|
| A) MOVSB/SW | 1) loads AL/AX register by content of a string |
| B) CMPS | 2) moves a string of bytes stored in source to destination |
| C) SCAS | 3) compares two strings of bytes or words whose length is stored in CX |
| D) LODS | 4) scans a string of bytes or words |

- a) A-3,B-4,C-2,D-1
- b) A-2,B-1,C-4,D-3
- c) A-2,B-3,C-1,D-4
- d) A-2,B-3,C-4,D-1

Answer: d

Explanation: By using the string instructions, the operations on strings can be performed.

7. The instructions that are used to call a subroutine from the main program and return to the main program after execution of called function are

- a) CALL, JMP
- b) JMP, IRET
- c) CALL, RET
- d) JMP, RET

Answer: c

Explanation: At each CALL instruction, the IP and CS of the next instruction are pushed onto the stack, before the control is transferred to the procedure. At the end of the procedure, the RET instruction must be executed to retrieve the stored contents of IP & CS registers from a stack.

8. The instruction that unconditionally transfers the control of execution to the specified address is
- a) CALL
 - b) JMP
 - c) RET
 - d) IRET

Answer: b

Explanation: In this the control transfers to the address specified in the instruction and flags are not affected by this instruction.

9. Which instruction cannot force the 8086 processor out of 'halt' state?
- a) Interrupt request
 - b) Reset
 - c) Both interrupt request and reset
 - d) Hold

Answer: d

Explanation: Only an interrupt request or Reset will force the 8086 processor to come out of the 'halt' state.

10. NOP instruction introduces
- a) Address
 - b) Delay
 - c) Memory location
 - d) None of the mentioned

Answer: b

Explanation: NOP is the No operation. It means that the processor performs no operation for the clock cycle and thus there exists a delay.

11. Which of the following is not a machine controlled instruction?
- a) HLT
 - b) CLC
 - c) LOCK
 - d) ESC

Answer: b

Explanation: Since CLC is a flag manipulation instruction where CLC stands for Clear Carry Flag.

To practice all areas of Microprocessors for Freshers, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Machine Language Instruction Formats".

1. Operation code field is present in :
- a) programming language instruction
 - b) assembly language instruction
 - c) machine language instruction
 - d) none of the mentioned

Answer: c

Explanation: Machine language instruction format has one or more fields. The first one is the operation code field.

2. A machine language instruction format consists of
- a) Operand field
 - b) Operation code field
 - c) Operation code field & operand field
 - d) none of the mentioned

Answer: c

Explanation: Machine language instruction format has both the fields.

3. The length of the one-byte instruction is

- a) 2 bytes
- b) 1 byte
- c) 3 bytes
- d) 4 bytes

Answer: b

Explanation: This format is only one byte long.

4. The instruction format 'register to register' has a length of

- a) 2 bytes
- b) 1 byte
- c) 3 bytes
- d) 4 bytes

Answer: a

Explanation: This format is 2 bytes long.

5. The R/M field in a machine instruction format specifies

- a) another register
- b) another memory location
- c) other operands
- d) all of the mentioned

Answer: d

Explanation: The LSBs(least significant bits) from 0 to 3 represent R/M field that specifies another register or memory location i.e. the other operand.

6. In a machine instruction format, S-bit is the

- a) status bit
- b) sign bit
- c) sign extension bit
- d) none of the mentioned

Answer: c

Explanation: The S-bit known as sign extension bit is used along with W-bit to show the type of operation.

7. The bit which is used by the 'REP' instruction is

- a) W-bit
- b) S-bit
- c) V-bit
- d) Z-bit

Answer: d

Explanation: The Z-bit is used by the REP instruction to control the loop.

8. If a W-bit value is '1' then the operand is of

- a) 8 bits
- b) 4 bits
- c) 16 bits
- d) 2 bits

Answer: c

Explanation: If W-bit is '1' then the operand is of 16-bits, and if it is '0' then the operand is of 8-bits.

9. The instructions which after execution transfer control to the next instruction in the sequence are called

- a) Sequential control flow instructions
- b) control transfer instructions
- c) Sequential control flow & control transfer instructions
- d) none of the mentioned

Answer: a

Explanation: The sequential control flow instructions follow sequence order in their execution.

10. The instructions that transfer the control to some predefined address or the address specified in the instruction are called as
- a) sequential control flow instructions
 - b) control transfer instructions
 - c) sequential control flow & control transfer instructions
 - d) none of the mentioned

Answer: b

Explanation: The control transfer instructions transfer control to the specified address.

11. The instruction "JUMP" belongs to
- a) sequential control flow instructions
 - b) control transfer instructions
 - c) branch instructions
 - d) control transfer & branch instructions

Answer: d

Explanation: The JUMP instruction transfers the control to the address located in the instruction.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Instruction Set of 8086/8088 - 1".

1. The instruction that is used to transfer the data from source operand to destination operand is
- a) data copy/transfer instruction
 - b) branch instruction
 - c) arithmetic/logical instruction
 - d) string instruction

Answer: a

Explanation: These instructions are used to copy and transfer the instructions.

2. Which of the following is not a data copy/transfer instruction?
- a) MOV
 - b) PUSH
 - c) DAS
 - d) POP

Answer: c

Explanation: DAS (Decimal Adjust after Subtraction) is an arithmetic instruction.

3. The instructions that involve various string manipulation operations are
- a) branch instructions
 - b) flag manipulation instructions
 - c) shift and rotate instructions
 - d) string instructions

Answer: d

Explanation: The string instructions perform operations on strings such as load, move, scan, compare etc.

4. Which of the following instruction is not valid?
- a) MOV AX, BX
 - b) MOV DS, 5000H
 - c) MOV AX, 5000H
 - d) PUSH AX

Answer: b

Explanation: Both the source and destination operands cannot be memory locations except for string instructions.

5. In PUSH instruction, after each execution of the instruction, the stack pointer is
- a) incremented by 1

- b) decremented by 1
- c) incremented by 2
- d) decremented by 2

Answer: d

Explanation: The actual current stack-top is always occupied by the previously pushed data. So, the push operation decrements SP by 2 and then stores the two bytes contents of the operand onto the stack.

6. The instruction that pushes the contents of the specified register/memory location on to the stack is
- a) PUSHF
 - b) POPF
 - c) PUSH
 - d) POP

Answer: c

Explanation: Since PUSH operation transfers data to stack from a register or memory location.

7. In POP instruction, after each execution of the instruction, the stack pointer is
- a) incremented by 1
 - b) decremented by 1
 - c) incremented by 2
 - d) decremented by 2

Answer: c

Explanation: The actual current stack top is popped into the specific operand as the contents of stack top memory is stored in AL&SP and further contents of the memory location pointed to by SP are copied to AH & SP.

8. The instructions that are used for reading an input port and writing an output port respectively are
- a) MOV, XCHG
 - b) MOV, IN
 - c) IN, MOV
 - d) IN, OUT

Answer: d

Explanation: The address of the input/output port may be specified directly or indirectly.

Example for input port: IN AX, DX; This instruction reads data from a 16-bit port whose address is in DX and stores it in AX

Example for output port: OUT 03H, AL; This sends data available in AL to a port whose address is 03H.

9. The instruction that is used for finding out the codes in case of code conversion problems is
- a) XCHG
 - b) XLAT
 - c) XOR
 - d) JCXZ

Answer: b

Explanation: The translate(XLAT) instruction is used to find codes.

10. The instruction that loads effective address formed by destination operand into the specified source register is
- a) LEA
 - b) LDS
 - c) LES
 - d) LAHF

Answer: a

Explanation: The instruction, LEA loads effective address and is more useful for assembly language rather than for machine language.

11. The instruction that loads the AH register with the lower byte of the flag register is
- a) SAHF
 - b) AH
 - c) LAHF
 - d) PUSHF

Answer: c

Explanation: The instruction LAHF(Load AH from a lower byte of Flag) may be used to observe the status of all the condition code flags(except overflow flag) at a time.

12. The instruction that pushes the flag register on to the stack is
- a) PUSH
 - b) POP
 - c) PUSHF
 - d) POPF

Answer: c

Explanation: The instruction PUSHF(push flags to stack) pushes the flag register on to the stack.

13. The instruction that loads the flag register completely from the word contents of the memory location is
- a) PUSH
 - b) POP
 - c) PUSHF
 - d) POPF

Answer: d

Explanation: POPF is pop flags to stack.

14. The instruction that adds immediate data/contents of the memory location specified in an instruction/register to the contents of another register/memory location is
- a) SUB
 - b) ADD
 - c) MUL
 - d) DIV

Answer: b

Explanation: ADD instruction adds the data.

15. The instruction that supports addition when carry exists is
- a) ADD
 - b) ADC
 - c) ADD & ADC
 - d) None of the mentioned

Answer: b

Explanation: ADC(Add with Carry) instruction performs the same operation as ADD operation, but adds the carry flag bit to the result.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Assembler Directives and Operators".

1. The assembler directives which are the hints using some predefined alphabetical strings are given to
- a) processor
 - b) memory
 - c) assembler
 - d) processor & assembler

Answer: c

Explanation: These directives help the assembler to correctly understand the assembly language programs to prepare the codes.

2. The directive used to inform the assembler, the names of the logical segments to be assumed for different segments used in the program is

- a) ASSUME
- b) SEGMENT
- c) SHORT
- d) DB

Answer: a

Explanation: In ALP, each segment is given a name by using the directive ASSUME

SYNTAX: ASSUME segment:segment_name

Eg: ASSUME CS:Code

here CS is the Code segment and code is the name assumed to the segment.

3. Match the following

- | | |
|-------|--|
| a) DB | 1) used to direct the assembler to reserve only 10-bytes |
| b) DT | 2) used to direct the assembler to reserve only 4 words |
| c) DW | 3) used to direct the assembler to reserve byte or bytes |
| d) DQ | 4) used to direct the assembler to reserve words |
-
- a) a-3, b-2, c-4, d-1
 - b) a-2, b-3, c-1, d-4
 - c) a-3, b-1, c-2, d-4
 - d) a-3, b-1, c-4, d-2

Answer: d

Explanation: These directives are used for allocating memory locations in the available memory.

4. The directive that marks the end of an assembly language program is

- a) ENDS
- b) END
- c) ENDS & END
- d) None of the mentioned

Answer: b

Explanation: The directive END is used to denote the completion of the program.

5. The directive that marks the end of a logical segment is

- a) ENDS
- b) END
- c) ENDS & END
- d) None of the mentioned

Answer: a

Explanation: The directive ENDS is used to end a segment where as the directive END is used to end the program.

6. The directive that updates the location counter to the next even address while executing a series of instructions is

- a) EVN
- b) EVEN
- c) EVNE
- d) EQU

Answer: b

Explanation: The directive updates location counter to next even address if the current location counter contents are not even.

7. The directive that directs the assembler to start the memory allotment for a particular segment/block/code from the declared address is

- a) OFFSET
- b) LABEL
- c) ORG
- d) GROUP

Answer: c

Explanation: If an ORG is written then the assembler initiates the location counter to keep the track of allotted address for the module as mentioned in the directive.

If the directive is not present, then the location counter is initialized to 0000H.

8. The directive that marks the starting of the logical segment is

- a) SEG
- b) SEGMENT
- c) SEG & SEGMENT
- d) PROC

Answer: b

Explanation: The directive SEGMENT indicates the beginning of the segment.

9. The recurrence of the numerical values or constants in a program code is reduced by

- a) ASSUME
- b) LOCAL
- c) LABEL
- d) EQU

Answer: d

Explanation: In this, the recurring/repeating value is assigned with a label. The label is placed instead of the numerical value in the entire program code.

10. The labels or constants that can be used by any module in the program is possible when they are declared as

- a) PUBLIC
- b) LOCAL
- c) GLOBAL
- d) Either PUBLIC or GLOBAL

Answer: c

Explanation: The labels, constants, variables, procedures declared as GLOBAL can be used by any module in the program.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessors Technical Interview Questions & Answers focuses on “Do’s and Don’ts While Using Instructions”.

1. The logic required for implementing a program can be expressed in terms of

- a) flowchart
- b) algorithm
- c) flowchart & algorithm
- d) none of the mentioned

Answer: c

Explanation: The logic required for implementing a program must be visualized clearly which is possible by flowchart and algorithm.

2. The operands, source and destination in an instruction cannot be

- a) register, register
- b) memory location, memory location
- c) memory location, register
- d) immediate data, register

Answer: b

Explanation: Only one memory operand can be specified in one instruction.

3. The instruction that is not possible among the following is

- a) MOV AX, BX
- b) MOV AX, [BX].
- c) MOV 55H, BL
- d) MOV AL, 55H

Answer: c

Explanation: 8-bit or 16-bit operand cannot be used as a destination operand.

4. The instruction that is not possible among the following is

- a) MOV AX, [BX].
- b) MOV AX, 5555H
- c) MOV AX, [SI].
- d) MOV [SI], [DI].

Answer: d

Explanation: Both the operands cannot be memory operands.

5. Both the operands source and destination of an instruction cannot be

- a) register, register
- b) immediate data, register
- c) register, immediate data
- d) immediate data, memory location

Answer: c

Explanation: Since destination operand should not be immediate data.

6. The registers that cannot be used as operands for arithmetic and logical instructions are

- a) general purpose registers
- b) pointers
- c) index registers
- d) segment registers

Answer: d

Explanation: Segment registers are not allowed as operands for arithmetic and logical instructions.

7. The operands of an instruction cannot be

- a) registers
- b) memory operands and immediate operands
- c) immediate operands
- d) memory operands

Answer: b

Explanation: Both the operands should not be immediate operands and memory operands.

To practice all technical interview questions on Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Stack".

1. The Stack follows the sequence

- a) first-in-first-out
- b) first-in-last-out
- c) last-in-first-out
- d) last-in-last-out

Answer: c

Explanation: The stack follows last-in-first-out sequence.

2. If the processor is executing the main program that calls a subroutine, then after executing the main program up to the CALL instruction, the control will be transferred to

- a) address of main program
- b) subroutine address
- c) address of CALL instruction
- d) none of the mentioned

Answer: b

Explanation: Since subroutine is called, to start the execution of the subroutine, the control is transferred to the subroutine address.

3. The stack is useful for

- a) storing the register status of the processor

- b) temporary storage of data
- c) storing contents of registers temporarily inside the CPU
- d) all of the mentioned

Answer: d

Explanation: Stack is used for temporary storage of contents of registers and memory locations, status of registers.

4. The Stack is accessed using
- a) SP register
 - b) SS register
 - c) SP and SS register
 - d) None of the mentioned

Answer: c

Explanation: The stack is accessed using a pointer that is implemented using SP and SS registers.

5. As the storing of data words onto the stack is increased, the stack pointer is
- a) incremented by 1
 - b) decremented by 1
 - c) incremented by 2
 - d) decremented by 2

Answer: d

Explanation: The data is stored from top address of the stack and is decremented by 2.

6. While retrieving data from the stack, the stack pointer is
- a) incremented by 1
 - b) incremented by 2
 - c) decremented by 1
 - d) decremented by 2

Answer: b

Explanation: The data in the stack, may again be transferred back from a stack to register. At that time, the stack pointer is incremented by 2.

7. The process of storing the data in the stack is called the stack.
- a) pulling into
 - b) pulling out
 - c) pushing into
 - d) popping into

Answer: c

Explanation: The data is pushed into the stack while loading the stack.

8. The reverse process of transferring the data back from the stack to the CPU register is known as
- a) pulling out the stack
 - b) pushing out the stack
 - c) popping out the stack
 - d) popping off the stack

Answer: d

Explanation: The data retrieved from stack is called popping off.

9. The books arranged one on the other on a table is an example of
- a) queue
 - b) queue and first-in-first out
 - c) stack
 - d) stack and last-in-first-out

Answer: d

Explanation: If the books are arranged one on the other, then the book that is placed last will be the first out.

10. The PID temperature controller using 8086 has

- a) data flow
- b) data flow and uses queue
- c) sequential flow
- d) sequential flow and uses stack

Answer: d

Explanation: Since PID temperature controller has steps that need to be sequentially executed such as sampling the output, conversion of a signal with ADC, finding errors, deriving control signals and applying the control signal to control flow of energy.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Stack Structure of 8086/8088".

1. The stack pointer register contains

- a) address of the stack segment
- b) pointer address of the stack segment
- c) offset of address of stack segment
- d) data present in the stack segment

Answer: c

Explanation: The stack pointer register contains the offset of the address of the stack segment.

2. The stack segment register contains

- a) address of the stack segment
- b) base address of the stack segment
- c) pointer address of the stack segment
- d) data in the stack segment

Answer: b

Explanation: The stack segment register contains base address of the stack segment in the memory. The stack pointer register (SP) and stack segment register (SS) together address the stack-top.

3. PUSH operation

- a) decrements SP
- b) increments SP
- c) decrements SS
- d) increments SS

Answer: a

Explanation: Each PUSH operation decrements the SP (Stack Pointer) register.

4. POP operation

- a) decrements SP
- b) increments SP
- c) decrements SS
- d) increments SS

Answer: b

Explanation: Each POP operation increments the SP (Stack Pointer) register.

5. The register or memory location that is pushed into the stack at the end must be

- a) popped off last
- b) pushed off first
- c) popped off first
- d) pushed off last

Answer: c

Explanation: The data can be retrieved by POP operation and as in stack, the data that is pushed at the end must be popped off first.

6. In the instruction, ASSUME CS : CODE, DS : DATA, SS : STACK the ASSUME directive directs to the assembler the

- a) address of the stack segment
- b) pointer address of the stack segment
- c) name of the stack segment
- d) name of the stack, code and data segments

Answer: d

Explanation: The directive ASSUME facilitates to name the segments with the desired name that is not a mnemonic or keyword.

7. When a stack segment is initialised then
- a) SS and SP are initialised
 - b) only SS is initialised
 - c) only SP is initialised
 - d) SS and SP need not be initialised

Answer: a

Explanation: Though the Stack segment is initialised, the SS and SP pointers must be initialised.

8. The number of PUSH instructions and POP instructions in a subroutine must be
- a) PUSH instructions must be greater than POP instructions
 - b) POP instructions must be greater than PUSH instructions
 - c) Both must be equal
 - d) Instructions may be any kind

Answer: c

Explanation: The number of PUSH instructions must be equal to the number of POP instructions.

9. 8086 does not support
- a) Arithmetic operations
 - b) logical operations
 - c) BCD operations
 - d) Direct BCD packed multiplication

Answer: d

Explanation: The 8086 microprocessor does not support direct BCD packed operations.

10. For 8086 microprocessor, the stack segment may have a memory block of a maximum of
- a) 32K bytes
 - b) 64K bytes
 - c) 16K bytes
 - d) NONE

Answer: b

Explanation: In 8086 microprocessor, the memory segments each have a memory of 64K bytes. To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Programming With An Assembler".

1. The disadvantage of machine level programming is
- a) time consuming
 - b) chances of error are more
 - c) debugging is difficult
 - d) all of the mentioned

Answer: d

Explanation: The machine level programming is complicated.

2. The coded object modules of the program to be assembled are present in
- a) .ASM file
 - b) .OBJ file
 - c) .EXE file
 - d) .OBJECT file

Answer: b

Explanation: .OBJ file is created with same name as source file and extension .OBJ. It contains the coded object modules of the program to be assembled.

3. The advantages of assembly level programming are

- a) flexibility of programming is more
- b) chances of error are less
- c) debugging is easy
- d) all of the mentioned

Answer: d

Explanation: The assembly level programming is more advantageous than the machine level programming.

4. The extension that is essential for every assembly level program is

- a) .ASP
- b) .ALP
- c) .ASM
- d) .PGM

Answer: c

Explanation: All the files should have the extension, .ASM.

5. The directory that is under work must have the files that are related to

- a) Norton's editor
- b) Assembler
- c) Linker
- d) All of the mentioned

Answer: d

Explanation: Before starting the process of entering a small program on PC, ensure that all the files namely Norton's editor, assembler, linker and debugger are available in the same directory in which work is been done.

6. The listing file is identified by

- a) source file name
- b) extension .LSF
- c) source file name and an extension .LSF
- d) source file name and an extension .LST

Answer: d

Explanation: The listing file is automatically generated in the assembly process and is identified by the entered or source file name and an extension .LST.

7. The extension file that is must for a file to be accepted by the LINK as a valid object file is

- a) .OBJ file
- b) .EXE file
- c) .MASM file
- d) DEBUG file

Answer: a

Explanation: The .OBJ extension is a must for a file to be accepted by the LINK as a valid object file.

8. The listing file contains

- a) total offset map of a source file
- b) offset address and labels
- c) memory allotments for different labels
- d) all of the mentioned

Answer: d

Explanation: The listing file contains total offset map of source file including labels, offset addresses, opcodes, memory allotments for different directives and labels and relocation information.

9. DEBUG.COM facilitates the
- a) debugging
 - b) trouble shooting
 - c) debugging and trouble shooting
 - d) debugging and assembling

Answer: c

Explanation: DEBUG.COM is a DOS utility that facilitates the debugging and trouble shooting.

10. DEBUG is able to troubleshoot only
- a) .EXE files
 - b) .OBJ files
 - c) .EXE file and .OBJ file
 - d) .EXE flie and .LST file

Answer: a

Explanation: The DEBUG may be used either to debug a source program or to observe the results of execution of an .EXE file.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Interrupts and Interrupt Service Routines".

1. While CPU is executing a program, an interrupt exists then it
- a) follows the next instruction in the program
 - b) jumps to instruction in other registers
 - c) breaks the normal sequence of execution of instructions
 - d) stops executing the program

Answer: c

Explanation: An interrupt function is to break the sequence of operation.

2. An interrupt breaks the execution of instructions and diverts its execution to
- a) Interrupt service routine
 - b) Counter word register
 - c) Execution unit
 - d) control unit

Answer: a

Explanation: An interrupt transfers the control to interrupt service routine (ISR). After executing ISR, the control is transferred back again to the main program.

3. While executing the main program, if two or more interrupts occur, then the sequence of appearance of interrupts is called
- a) multi-interrupt
 - b) nested interrupt
 - c) interrupt within interrupt
 - d) nested interrupt and interrupt within interrupt

Answer: d

Explanation: If an interrupt occurs while executing a program, and the processor is executing the interrupt, if one more interrupt occurs again, then it is called a nested interrupt.

4. Whenever a number of devices interrupt a CPU at a time, and if the processor is able to handle them properly, it is said to have
- a) interrupt handling ability
 - b) interrupt processing ability
 - c) multiple interrupt processing ability
 - d) multiple interrupt executing ability

Answer: c

Explanation: The processor if handles more devices as interrupts then it has multiple interrupt processing ability.

5. NMI stands for
- a) nonmaskable interrupt
 - b) nonmultiple interrupt
 - c) nonmovable interrupt
 - d) none of the mentioned

Answer: a

Explanation: NMI is the acronym for nonmaskable interrupt.

7. If any interrupt request given to an input pin cannot be disabled by any means then the input pin is called
- a) maskable interrupt
 - b) nonmaskable interrupt
 - c) maskable interrupt and nonmaskable interrupt
 - d) none of the mentioned

Answer: b

Explanation: A nonmaskable interrupt input pin is one which means that any interrupt request at NMI (nonmaskable interrupt) input cannot be masked or disabled by any means.

8. The INTR interrupt may be
- a) maskable
 - b) nonmaskable
 - c) maskable and nonmaskable
 - d) none of the mentioned

Answer: a

Explanation: the INTR (interrupt request) is maskable or can be disabled.

9. The Programmable interrupt controller is required to
- a) handle one interrupt request
 - b) handle one or more interrupt requests at a time
 - c) handle one or more interrupt requests with a delay
 - d) handle no interrupt request

Answer: b

Explanation: If more than one interrupt request (INTR) occurs at a time, then an external chip called programmable interrupt controller is required to handle them.

10. The INTR interrupt may be masked using the flag
- a) direction flag
 - b) overflow flag
 - c) interrupt flag
 - d) sign flag

Answer: c

Explanation: If a microprocessor wants to serve any interrupt then interrupt flag, IF=1. If interrupt flag, IF=0, then the processor ignores the service.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Interrupt Cycle of 8086/8088".

1. If an interrupt is generated from outside the processor then it is an
- a) internal interrupt
 - b) external interrupt
 - c) interrupt
 - d) none of the mentioned

Answer: b

Explanation: If an external device or a signal interrupts the processor from outside then it is an external interrupt.

2. If the interrupt is generated by the execution of an interrupt instruction then it is
- a) internal interrupt

- b) external interrupt
- c) interrupt-in-interrupt
- d) none of the mentioned

Answer: a

Explanation: The internal interrupt is generated internally by the processor circuit or by the execution of an interrupt instruction.

3. Example of an external interrupt is

- a) divide by zero interrupt
- b) keyboard interrupt
- c) overflow interrupt
- d) type2 interrupt

Answer: b

Explanation: Since the keyboard is external to the processor, it is an external interrupt.

4. Example of an internal interrupt is

- a) divide by zero interrupt
- b) overflow interrupt
- c) interrupt due to INT
- d) all of the mentioned

Answer: d

Explanation: Since the interrupts occur within the processor itself, they are called internal interrupts.

5. The interrupt request that is independent of IF flag is

- a) NMI
- b) TRAP
- c) Divide by zero
- d) All of the mentioned

Answer: d

Explanation: These requests are independent of IF flag.

6. The type of the interrupt may be passed to the interrupt structure of CPU from

- a) interrupt service routine
- b) stack
- c) interrupt controller
- d) none of the mentioned

Answer: c

Explanation: After an interrupt is acknowledged, the CPU computes the vector address from the type of the interrupt that may be passed to the internal structure of the CPU from an interrupt controller in case of external interrupts.

7. During the execution of an interrupt, the data pushed into the stack is the content of

- a) IP
- b) CS
- c) PSW
- d) All of the mentioned

Answer: d

Explanation: The contents of IP, CS and PSW are pushed into the stack during the execution.

8. After every response to the single step interrupt the flag that is cleared is

- a) IF (Interrupt Flag)
- b) TF (Trap Flag)
- c) OF (Overflow Flag)
- d) None of the mentioned

Answer: b

Explanation: If the trap flag is set then the processor enters the single step execution mode. After the execution, the trap flag is cleared.

9. At the end of ISR, the instruction should be
- a) END
 - b) ENDS
 - c) IRET
 - d) INTR

Answer: c

Explanation: After the execution of the ISR, the control must go to the previous program (maybe main program) which was being executed. To execute it, IRET is placed at the end of ISR.

10. When the CPU executes IRET,
- a) contents of IP and CS are retrieved
 - b) the control transfers from ISR to main program
 - c) clears the trap flag
 - d) clears the interrupt flag

Answer: a

Explanation: When the instruction IRET is executed, the contents of flags, IP and CS which were saved at the stack by the CALL instruction are retrieved to the respective registers.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on “Non Maskable Interrupt and Maskable Interrupt (INTR)”.

1. The interrupt for which the processor has the highest priority among all the external interrupts is
- a) keyboard interrupt
 - b) TRAP
 - c) NMI
 - d) INT

Answer: c

Explanation: The Non-Maskable Interrupt input pin has the highest priority among all the external interrupts.

2. The interrupt for which the processor has highest priority among all the internal interrupts is
- a) keyboard interrupt
 - b) TRAP
 - c) NMI
 - d) INT

Answer: b

Explanation: TRAP is the internal interrupt that has highest priority among all the interrupts except the Divide By Zero (Type 0) exception.

3. In case of string instructions, the NMI interrupt will be served only after
- a) initialisation of string
 - b) execution of some part of the string
 - c) complete string is manipulated
 - d) the occurrence of the interrupt

Answer: c

Explanation: When NMI is activated, the current instruction being executed is completed and then NMI is served. In the case of string instructions, it is served after the complete string is manipulated.

4. The NMI pin should remain high for atleast
- a) 4 clock cycles
 - b) 3 clock cycles
 - c) 1 clock cycle
 - d) 2 clock cycles

Answer: d

Explanation: The NMI pin should remain high for atleast 2 clock cycles and need not be synchronized with the clock for being sensed.

5. The INTR signal can be masked by resetting the

- a) TRAP flag
- b) INTERRUPT flag
- c) MASK flag
- d) DIRECTION flag

Answer: b

Explanation: The INTR signal can be masked by resetting the interrupt flag.

6. For the INTR signal, to be responded to in the next instruction cycle, it must go _____ in the last clock cycle of the current instruction

- a) high
- b) low
- c) high or low
- d) unchanged

Answer: a

Explanation: The INTR signal must go high in the clock cycle of the current instruction in order to respond in the next instruction cycle.

7. The status of the pending interrupts is checked at

- a) the end of main program
- b) the end of all the interrupts executed
- c) the beginning of every interrupt
- d) the end of each instruction cycle

Answer: d

Explanation: At the end of each instruction, the status of the pending interrupts is checked.

8. Once the processor responds to an INTR signal, the IF is automatically

- a) set
- b) reset
- c) high
- d) low

Answer: b

Explanation: The IF is automatically reset when the processor responds to an INTR signal. If the processor wants to respond to any type of INTR signal further then, the IF should again be set.

9. If the pin LOCK (active low based) is low at the trailing edge of the first ALE pulse, then till the start of the next machine cycle, the pin LOCK (active low) is

- a) low
- b) high
- c) low or high
- d) none of the mentioned

Answer: a

Explanation: The pin LOCK (active low) remains low till the start of the next machine cycle.

10. With the trailing edge of the LOCK (active low), the INTA (active low) goes low and remains in it for

- a) 0 clock cycle
- b) 1 clock cycle
- c) 2 clock cycles
- d) 3 clock cycles

Answer: c

Explanation: The INTA (active low) goes low and remains low for two clock cycles before returning back to the high state.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Macros".

1. If a number of instructions are repeating through the main program, then to reduce the length of the program, _____ is used.
- a) procedure
 - b) subroutine
 - c) macro
 - d) none of the mentioned

Answer: c

Explanation: For a certain number of instructions that are repeated in the main program, when macro is defined then the code of a program is reduced by placing the name of the macro at which the set of instructions are needed to be repeated.

2. The process of assigning a label or macroname to the string is called
- a) initialising macro
 - b) initialising string macro
 - c) defining a string macro
 - d) defining a macro

Answer: d

Explanation: The process of assigning a label to the string is called defining a macro.

3. A macro within a macro is called
- a) macro-within-macro
 - b) nested macro
 - c) macro-in-macro
 - d) none of the mentioned

Answer: b

Explanation: A macro may be called from inside a macro. This type of macro is called nested macro.

4. A macro can be defined as
- a) beginning of a program
 - b) end of a program
 - c) after initialisation of program
 - d) anywhere in a program

Answer: d

Explanation: A macro can be defined anywhere in a program.

5. A macro can be used as _____
- a) in data segment
 - b) to represent directives
 - c) to represent statements
 - d) all of the mentioned

Answer: d

Explanation: A macro may be used in data segment and can also be used to represent statements and directives.

6. The end of a macro can be represented by the directive.
- a) END
 - b) ENDS
 - c) ENDM
 - d) ENDD

Answer: c

Explanation: The ENDM directive marks the end of the instructions or statements sequence assigned with the macro name.

7. Inserting the statements and instructions represented by macro, directly at the place of the macroname, in the program, is known as

- a) calling a macro
- b) inserting a macro
- c) initializing a macro
- d) none of the mentioned

Answer: a

Explanation: Inserting the statements and instructions at the place of macroname, in the program, is known as calling a macro.

8. The time required for execution of a macro is _____ that of the procedure.

- a) greater than
- b) less than
- c) equal to
- d) none of the mentioned

Answer: b

Explanation: The time required for execution of a macro is less than that of procedure as it does not contain CALL and RET instructions as the procedures do.

9. Which of the following statements is incorrect?

- a) complete code of instruction string is inserted at each place, wherever the macroname appears
- b) macro requires less time of execution than that of procedure
- c) macro uses stack memory
- d) macroname can be anything except registers and mnemonics

Answer: c

Explanation: Macro does not require stack memory and hence has less time for execution.

10. The beginning of the macro can be represented as

- a) START
- b) BEGIN
- c) MACRO
- d) None of the mentioned

Answer: c

Explanation: The beginning of the macro is represented as macroname followed by the directive MACRO.

SYNTAX: macroname MACRO

EXAMPLE: STRINGS MACRO.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on “Timings and Delays”.

1. If ‘n’ denotes the number of clock cycles and ‘T’ denotes period of the clock at which the microprocessor is running, then the duration of execution of loop once can be denoted by

- a) $n+T$
- b) $n-T$
- c) $n*T$
- d) n/T

Answer: c

Explanation: The duration of execution of the loop is the product of number of clock cycles and the period of the clock cycle at which microprocessor is running.

2. The number of instructions actually executed by the microprocessor depends on the

- a) stack
- b) loop count
- c) program counter
- d) time duration

Answer: b

Explanation: As the microprocessor executes each instruction corresponding loop counter value decreases and the microprocessor executes the instructions till the loop counter becomes zero.

3. In case of subroutines, the actual number of instructions executed by the processor depends on

- a) loop count
- b) length of interrupt service routine
- c) length of procedure
- d) none

Answer: c

Explanation: In case of subroutines or interrupt service routines, the number of instructions executed by the processor depends on the length of procedure (or subroutine) or length of interrupt service routine along with the main calling program.

4. The step included in generating delays is

- a) determining exact required delay
- b) selecting instructions for delay loop
- c) finding period of clock frequency
- d) all of the mentioned

Answer: d

Explanation: The delays can be generated step wise.

5. The Count, N can be defined as

- a) required delay/duration for execution
- b) duration of execution/required delay
- c) required delay/number of clock cycles
- d) required delay/period of clock frequency

Answer: a

Explanation: The count N can be defined as the required time delay by the duration for execution of the loop once.

Count, $N = \text{required delay (Td)}/\text{duration for execution of the loop once (n*T)}$.

6. In the instruction set,

```
        MOV CX, BA03H
WAIT:   DEC CX
        NOP
        JNZ WAIT
        RET
```

if the zeroth condition is satisfied then, for execution, the JNZ instruction takes

- a) 1 clock cycle
- b) 2 clock cycles
- c) 3 clock cycles
- d) 4 clock cycles

Answer: d

Explanation: The JNZ instruction takes only 4 clock cycles if the zeroth condition is satisfied.

7. In the instruction set,

```
        MOV CX, BA03H
WAIT:   DEC CX
        NOP
        JNZ WAIT
        RET
```

if the zeroth condition is not satisfied, then the JNZ instruction takes

- a) 2 clock cycles
- b) 8 clock cycles
- c) 16 clock cycles
- d) 64 clock cycles

Answer: c

Explanation: The JNZ instruction takes 16 clock cycles if the zeroth condition is not satisfied.

8. The maximum count value of 16-bit count register puts a limitation on

- a) memory usage
- b) storage of address of registers
- c) to generate clock pulse
- d) to generate maximum delay

Answer: d

Explanation: The maximum count value of 16-bit count register is FFFFH. This may put the limitation on the maximum delay that can be generated using the instructions.

9. When large delays are required, then to serve the purpose

- a) one or more count registers can be used
- b) one or more shift registers can be used
- c) one or more pointer registers can be used
- d) one or more index registers can be used

Answer: a

Explanation: One or more count registers can be used to serve large delays.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessors Interview Questions and Answers for freshers focuses on "Interrupt Programming, Passing Parameters to Procedures, Handling Programs of Size More Than 64KB".

1. The method of defining the interrupt service routine for software is

- a) same as that of hardware
- b) difficult than hardware
- c) easier than software
- d) none of the mentioned

Answer: a

Explanation: For both software and hardware, the method of defining the interrupt service routine is the same.

2. While programming for any type of interrupt, the interrupt vector table is set

- a) externally
- b) through a program
- c) either externally or through the program
- d) externally and through the program

Answer: c

Explanation: The programmer must, either externally or through the program, set the interrupt vector table for that type preferably with the CS and IP addresses of the interrupt service routine.

3. To execute a program one should

- a) assemble the program
- b) link the program
- c) apply external pulse
- d) all of the mentioned

Answer: d

Explanation: To execute a program, first assemble it, link it and then execute it. After execution, a new file RESULT is created in the directory. Then external pulse is applied to IRQ2 pin, and this will again cause the execution of ISR into the file.

4. Procedures are also known as

- a) macros
- b) segment
- c) subroutines
- d) none

Answer: c

Explanation: Procedures are also known as subroutines.

5. Procedures, for their execution, require

- a) input data
- b) output data
- c) constants
- d) input data or constants

Answer: d

Explanation: Procedures require input data or constants for their execution. Their data or constants may be passed to the subroutine by the main program.

6. The technique that is used to pass the data or parameter to procedures in assembly language program is by using

- a) global declared variable
- b) registers
- c) stack
- d) all of the mentioned

Answer: d

Explanation: The techniques that are used to pass the data or parameter to procedures are by using global declared variable, registers of CPU, memory locations, stack, PUBLIC & EXTRN.

7. If a procedure is interactive, then

- a) it accepts inputs directly from input devices
- b) it uses global declared variable technique
- c) it uses stack
- d) it uses memory locations

Answer: a

Explanation: If a procedure is interactive, then it accepts the inputs directly from input devices.

8. For passing the parameters to procedures using the PUBLIC & EXTRN directives, it must be declared PUBLIC in the

- a) subroutine
- b) procedure
- c) main routine
- d) main routine and subroutine

Answer: c

Explanation: For passing the parameters to procedures, it must be declared PUBLIC in the main routine and the same should be declared EXTRN in the procedure.

9. The technique to estimate the size of an executable program, before it is assembled and linked is

- a) memory location technique
- b) global variable technique
- c) stack
- d) none

Answer: d

Explanation: There is no technique to estimate the size of an executable program before it is assembled and linked.

10. To estimate the size of an executable program before it is assembled and linked, the programming methodology concerned is by writing

- a) programs with more than one segment for data and code
- b) programs with FAR subroutines each of size up to 64KB
- c) programs with more than one segment for stack
- d) all of the mentioned

Answer: d

Explanation: By writing programs with more than one segment for data, code or stack or by

writing programs with FAR subroutines each of size 64KB, the size of an executable program can be estimated.

To practice all areas of Microprocessors for Interviews, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Semiconductor Memory Interfacing".

1. The semiconductor memories are organised as _____ dimension(s) of array of memory locations.
- a) one dimensional
 - b) two dimensional
 - c) three dimensional
 - d) none

Answer: b

Explanation: The semiconductor memories are organised as two dimensions of an array which consists of rows and columns.

2. If a location is selected, then all the bits in it are accessible using a group of conductors called
- a) control bus
 - b) address bus
 - c) data bus
 - d) either address bus or data bus

Answer: c

Explanation: The bits in a selected location are accessible using data bus.

3. To address a memory location out of N memory locations, the number of address lines required is
- a) $\log N$ (to the base 2)
 - b) $\log N$ (to the base 10)
 - c) $\log N$ (to the base e)
 - d) $\log (2N)$ (to the base e)

Answer: a

Explanation: For n memory locations, $\log n$ (to the base of 2) address lines are required. For addressing 4K bytes of memory, 12 address lines are required since $\log(4KB) = \log(4 \times 1024) = \log(2^{12}) = 12$.

4. If the microprocessor has 10 address lines, then the number of memory locations it is able to address is
- a) 512
 - b) 1024
 - c) 2048
 - d) none

Answer: b

Explanation: Since for n address lines, the number of memory locations able to address is 2^n .

5. In static memory, the upper 8-bit bank of an available 16-bit memory chip is called
- a) upper address memory bank
 - b) even address memory bank
 - c) static upper memory
 - d) odd address memory bank

Answer: d

Explanation: In static memory, the upper 8-bit bank is called odd address memory bank.

6. In static memory, the lower 8-bit bank of an available 16-bit memory chip is called
- a) lower address memory bank
 - b) even address memory bank
 - c) static lower memory bank
 - d) odd address memory bank

Answer: b

Explanation: In static memory, the lower 8-bit bank is called even address memory bank.

7. In most of the cases, the method used for decoding that may be used to minimise the required hardware is

- a) absolute decoding
- b) non-linear decoding
- c) linear decoding
- d) none

Answer: c

Explanation: In general, linear decoding is used to minimise the required hardware.

8. To obtain 16-bit data bus width, the two 4K*8 chips of RAM and ROM are arranged in

- a) parallel
- b) serial
- c) both serial and parallel
- d) neither serial nor parallel

Answer: a

Explanation: The two 4K*8 chips of RAM and ROM are arranged in parallel.

9. If (address line) $A_0=0$ then, the status of address and memory are

- a) address is even and memory is in ROM
- b) address is odd and memory is in ROM
- c) address is even and memory is in RAM
- d) address is odd and memory is in RAM

Answer: c

Explanation: If $A_0=0$ then address is even and is in RAM. If $A_0=1$ then, address is odd and is in RAM.

10. If at a time A_0 and BHE (active low) both are zero then, the chip(s) selected will be

- a) RAM
- b) ROM
- c) RAM and ROM
- d) ONLY RAM

Answer: c

Explanation: If at a time A_0 and BHE (active low) both are zero, then both RAM and ROM are selected.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Dynamic RAM Interfacing".

1. The advantage of dynamic RAM is

- a) high packing density
- b) low cost
- c) less power consumption
- d) all of the mentioned

Answer: d

Explanation: The dynamic RAM is advantageous than the static RAM as it has a higher packing density, lower cost and less power consumption.

2. Whenever a large memory is required in a microcomputer system, the memory subsystem is generally designed using

- a) Static RAM
- b) Dynamic RAM
- c) Both static and dynamic RAM
- d) ROM

Answer: b

Explanation: Dynamic RAM is preferred for large memory.

3. If a typical static RAM cell requires 6 transistors then corresponding dynamic RAM requires
- a) 1 transistor along with capacitance
 - b) 2 transistors along with resistance
 - c) 3 transistors along with diode
 - d) 2 transistors along with capacitance

Answer: a

Explanation: The hardware complexity of dynamic RAM is lesser than that of static RAM.

4. To store the charge as a representation of data, the basic dynamic RAM cell uses
- a) resistor
 - b) capacitor
 - c) diode
 - d) transistor

Answer: c

Explanation: The basic dynamic RAM cell uses capacitance to store the charge as a representation of data. This capacitor is manufactured as a diode that is reverse biased so that the storage capacitance is obtained.

5. The process of refreshing the data in the RAM to reduce the possibility of data loss is known as
- a) data cycle
 - b) regain cycle
 - c) retain cycle
 - d) refresh cycle

Answer: d

Explanation: The data storage in RAM which is capacitance (reverse-biased diode) may have a leakage current that tends to discharge the capacitor giving rise to possibility of data loss. To avoid this, the data must be refreshed after a fixed time interval regularly.

6. The field in which dynamic RAM is more complicated than static RAM is
- a) complexity
 - b) interfacing circuit
 - c) execution unit
 - d) cost

Answer: b

Explanation: The refresh mechanism and the additional hardware required makes the interfacing circuit of dynamic RAM more complicated than that of static RAM.

7. Memory refresh activity is
- a) initialised by processor
 - b) initialised by external bus master
 - c) initialised by refresh mechanism
 - d) initialised either by processor or by external bus

Answer: c

Explanation: The refresh operation is independent regular activity that is initialised and carried out by the refresh mechanism.

8. The number of memory chips that are enabled at a time for refresh activity is
- a) 2
 - b) 4
 - c) 8
 - d) more than 1

Answer: d

Explanation: More than one memory chip can be enabled at a time to refresh activity to reduce the number of total memory refresh cycles.

9. A timer that derives pulse for refreshing action or time for which a dynamic RAM cell can hold data charge level practically constant is
- a) constant timer

- b) data managing timer
- c) refresh timer
- d) qualitative timer

Answer: c

Explanation: Refresh timer derives a pulse for refreshing action after each refresh interval which can be qualitatively defined as the time for which a dynamic RAM cell can hold data charge level practically constant.

10. If 'n' denotes the number of rows that are to be refreshed in a single refresh interval, 'td' denotes the range of time it may take then, refresh time (tr) can be defined as

- a) $n \cdot t_d$
- b) t_d/n
- c) n/t_d
- d) t_d^n

Answer: b

Explanation: Refresh time is the ratio of time duration taken for refreshing to the number of rows that are refreshed. Refresh frequency is the reciprocal of refresh time.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Interfacing I/O Ports".

1. The device that enables the microprocessor to read data from the external devices is

- a) printer
- b) joystick
- c) display
- d) reader

Answer: b

Explanation: Since joystick is an input device, it reads data from the external devices.

2. The example of output device is

- a) CRT display
- b) 7-segment display
- c) Printer
- d) All of the mentioned

Answer: d

Explanation: The output device transfers data from the microprocessor to the external devices.

3. The input and output operations are respectively similar to the operations,

- a) read, read
- b) write, write
- c) read, write
- d) write, read

Answer: c

Explanation: The input activity is similar to read operation and the output activity is similar to write operation.

4. The operation, IOWR (active low) performs

- a) write operation on input data
- b) write operation on output data
- c) read operation on input data
- d) read operation on output data

Answer: b

Explanation: IOWR (active low) operation means writing data to an output device and not an input device.

5. The latch or IC 74LS373 acts as

- a) good input port

- b) bad input port
- c) good output port
- d) bad output port

Answer: c

Explanation: If the output port is to source large currents, the port lines must be buffered. So, the latch is used as it acts as a good output port.

6. While performing read operation, one must take care that much current should not be
- a) sourced from data lines
 - b) sinked from data lines
 - c) sourced or sinked from data lines
 - d) sinked from address lines

Answer: c

Explanation: More current should not be sourced or sinked from data lines while reading to avoid loading.

7. To avoid loading during read operation, the device used is
- a) latch
 - b) flipflop
 - c) buffer
 - d) tristate buffer

Answer: d

Explanation: A tristate buffer is used as an input device to overcome loading.

8. The chip 74LS245 is
- a) bidirectional buffer
 - b) 8-bit input port
 - c) one that has 8 buffers
 - d) all of the mentioned

Answer: d

Explanation: The chip 74LS245 is a bidirectional buffer that contains 8 buffers and may be used as an 8-bit input port. But while using as an input device, only one direction is useful.

9. In 74LS245, if DIR is 1, then the direction is from
- a) inputs to outputs
 - b) outputs to inputs
 - c) source to sink
 - d) sink to source

Answer: a

Explanation: If DIR is 1, then the direction is from A(inputs) to B(outputs).

10. In memory-mapped scheme, the devices are viewed as
- a) distinct I/O devices
 - b) memory locations
 - c) only input devices
 - d) only output devices

Answer: b

Explanation: In memory-mapped scheme, the devices are viewed as memory locations and are addressed likewise.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Modes of Operation of 8255".

1. In the I/O mode, the 8255 ports work as
- a) reset pins
 - b) set pins
 - c) programmable I/O ports
 - d) only output ports

Answer: c

Explanation: In the I/O mode, the 8255 ports work as programmable I/O ports.

2. In BSR mode, only port C can be used to

- a) set individual ports
- b) reset individual ports
- c) set and reset individual ports
- d) programmable I/O ports

Answer: c

Explanation: In BSR (Bit Set-Reset) Mode, port C can be used to set and reset its individual port bits.

3. The feature of mode 0 is

- a) any port can be used as input or output
- b) output ports are latched
- c) maximum of 4 ports are available
- d) all of the mentioned

Answer: d

Explanation: In mode 0, any port can be used as input or output and output ports are latched.

4. The strobed input/output mode is another name of

- a) mode 0
- b) mode 1
- c) mode 2
- d) none

Answer: b

Explanation: In this mode, the handshaking signals control the input or output action of the specified port.

5. If the value of the pin STB (Strobe Input) falls to low level, then

- a) input port is loaded into input latches
- b) input port is loaded into output latches
- c) output port is loaded into input latches
- d) output port is loaded into output latches

Answer: a

Explanation: If the value of the pin STB (Strobe Input) falls to low level, the input port is loaded into input latches.

6. The signal, SLCT in the direction of signal flow, OUT, indicates the selection of

- a) Control word register
- b) CPU
- c) Printer
- d) Ports

Answer: c

Explanation: This signal indicates that the printer is selected.

7. The pulse width of the signal INIT at the receiving terminal must be more than

- a) 10 microseconds
- b) 20 microseconds
- c) 40 microseconds
- d) 50 microseconds

Answer: d

Explanation: The pulse width of the signal must be more than 50microseconds at the receiving terminal.

8. The level of the signal ERROR(active low) becomes 'low' when the printer is in

- a) Paper end state
- b) Offline state
- c) Error state
- d) All of the mentioned

Answer: d

Explanation: The level of the signal ERROR(active low) becomes 'low' when the printer is in the Paper end state, Offline state and Error state.

9. The signals that are provided to maintain proper data flow and synchronization between the data transmitter and receiver are

- a) handshaking signals
- b) control signals
- c) input signals
- d) none

Answer: a

Explanation: Handshaking signals maintain proper data flow and synchronization.

10. The feature of mode 2 of 8255 is

- a) single 8-bit port is available
- b) both inputs and outputs are latched
- c) port C is used for generating handshake signals
- d) all of the mentioned

Answer: d

Explanation: In mode 2 of 8255, a single 8-bit port is available i.e group A.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "PIO 8255 (Programmable Input - Output Port)".

1. Programmable peripheral input-output port is another name for

- a) serial input-output port
- b) parallel input-output port
- c) serial input port
- d) parallel output port

Answer: b

Explanation: The parallel input-output port chip 8255 is also known as programmable peripheral input-output port.

2. Port C of 8255 can function independently as

- a) input port
- b) output port
- c) either input or output ports
- d) both input and output ports

Answer: c

Explanation: Port C can function independently either as input or as output ports.

3. All the functions of the ports of 8255 are achieved by programming the bits of an internal register called

- a) data bus control
- b) read logic control
- c) control word register
- d) none of the mentioned

Answer: c

Explanation: By programming the bits of control word register, the operations of the ports are specified.

4. The data bus buffer is controlled by

- a) control word register
- b) read/write control logic
- c) data bus
- d) none of the mentioned

Answer: b

Explanation: The data bus buffer is controlled by read/write control logic.

5. The input provided by the microprocessor to the read/write control logic is
- a) RESET
 - b) A1
 - c) WR(ACTIVE LOW)
 - d) All of the mentioned

Answer: d

Explanation: RD(ACTIVE LOW), WR(ACTIVE LOW), A1, A0, RESET are the inputs provided by the microprocessor to the read/write control logic of 8255.

6. The device that receives or transmits data upon the execution of input or output instructions by the microprocessor is
- a) control word register
 - b) read/write control logic
 - c) 3-state bidirectional buffer
 - d) none of the mentioned

Answer: c

Explanation: 3-state bidirectional buffer is used to receives or transmits data upon the execution of input or output instructions by the microprocessor.

7. The port that is used for the generation of handshake lines in mode 1 or mode 2 is
- a) port A
 - b) port B
 - c) port C Lower
 - d) port C Upper

Answer: d

Explanation: Port C upper is used for the generation of handshake lines in mode 1 or mode 2.

8. If A1=0, A0=1 then the input read cycle is performed from
- a) port A to data bus
 - b) port B to data bus
 - c) port C to data bus
 - d) CWR to data bus

Answer: b

Explanation: If A1=0, A0=1 then the input read cycle is performed from port B to data bus.

9. The function, 'data bus tristated' is performed when
- a) CS(active low) = 1
 - b) CS(active low) = 0
 - c) CS(active low) = 0, RD(active low) = 1, WR(active low) = 1
 - d) CS(active low) = 1 OR CS(active low) = 0, RD(active low) = 1, WR(active low) = 1

Answer: d

Explanation: The data bus is tristated when chip select pin=1 or chip select pin=0 and read and write signals are high i.e 1.

10. The pin that clears the control word register of 8255 when enabled is
- a) CLEAR
 - b) SET
 - c) RESET
 - d) CLK

Answer: c

Explanation: If reset pin is enabled then the control word register is cleared.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Programmable Interval Timer 8254".

1. The number of counters that are present in the programmable timer device 8254 is
- a) 1
 - b) 2

- c) 3
- d) 4

Answer: c

Explanation: There are three counters that can be used as either counters or delay generators.

2. The operation that can be performed on control word register is

- a) read operation
- b) write operation
- c) read and write operations
- d) none

Answer: b

Explanation: The control word register can only be written and cannot be read.

3. The mode that is used to interrupt the processor by setting a suitable terminal count is

- a) mode 0
- b) mode 1
- c) mode 2
- d) mode 3

Answer: a

Explanation: Mode 0 is also called as an interrupt on the terminal count.

4. In mode 2, if N is loaded as the count value, then after (N-1) cycles, the output becomes low for

- a) 1 clockcycle
- b) 2 clockcycles
- c) 3 clockcycles
- d) 4 clockcycles

Answer: a

Explanation: After (N-1) cycles, the output becomes low for only 1 clockcycle. If the count N is reloaded and again the output becomes high and remains so for (N-1) clock pulses.

5. The generation of a square wave is possible in the mode

- a) mode 1
- b) mode 2
- c) mode 3
- d) mode 4

Answer: c

Explanation: When the count N loaded is even, then for half of the count, the output remains high and for the remaining half it remains low. If the count loaded is odd, the first clock pulse decrements it by 1 resulting in an even count value.

6. In control word register, if SC1=0 and SC0=1, then the counter selected is

- a) counter 0
- b) counter 1
- c) counter 2
- d) none

Answer: b

Explanation: SC denotes select counter.

7. In control word format, if RL1=1, RL0=1 then the operation performed is

- a) read/load least significant byte only
- b) read/load most significant byte only
- c) read/load LSB first and then MSB
- d) read/load MSB first and then LSB

Answer: c

Explanation: To access 16 bit, first LSB is loaded first, and then MSB.

8. If BCD=0, then the operation is

- a) decimal count

- b) hexadecimal count
- c) binary count
- d) octal count

Answer: b

Explanation: If BCD=0 then hexadecimal count. If BCD=1, then the operation is BCD count.

9. The counter starts counting only if
- a) GATE signal is low
 - b) GATE signal is high
 - c) CLK signal is low
 - d) CLK signal is high

Answer: b

Explanation: If the GATE signal is enabled, then the counter starts counting.

10. The control word register contents are used for
- a) initializing the operating modes
 - b) selection of counters
 - c) choosing binary/BCD counters
 - d) all of the mentioned

Answer: d

Explanation: The control word register contents are used for

- i) initializing the operating modes (mode 0-mode 4)
- ii) selection of counters (counter0-counter2)
- iii) choosing binary or BCD counters
- iv) loading of the counter registers.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessors Puzzles focuses on “Interfacing Analog to Digital Data Converters”.

1. The time taken by the ADC from the active edge of SOC(start of conversion) pulse till the active edge of EOC(end of conversion) signal is called
- a) edge time
 - b) conversion time
 - c) conversion delay
 - d) time delay

Answer: c

Explanation: Broadly speaking, the time taken by the converter to calculate the equivalent digital data output from the moment of the start of conversion is called conversion delay.

2. The popular technique that is used in the integration of ADC chips is
- a) successive approximation
 - b) dual slope integration
 - c) successive approximation and dual slope integration
 - d) none

Answer: c

Explanation: Successive approximation and dual slope integration are the most popular techniques that are used in the integrated ADC chips.

3. The procedure of algorithm for interfacing ADC contain
- a) ensuring stability of analog input
 - b) issuing start of conversion pulse to ADC
 - c) reading digital data output of ADC as equivalent digital output
 - d) all of the mentioned

Answer: d

Explanation: The general algorithm for interfacing ADC contains ensuring the stability of analog input, issuing start of conversion pulse to ADC, reading end of conversion signal to mark the end of a conversion process, reading digital data output of ADC as equivalent digital output.

4. Which is the ADC among the following?

- a) AD 7523
- b) 74373
- c) 74245
- d) ICL7109

Answer: d

Explanation: AD 7523 is a DAC(Digital to analog converter), 74373 is a latch, 74245 is transceiver and ICL7109 is an ADC.

5. The conversion delay in a successive approximation of an ADC 0808/0809 is

- a) 100 milliseconds
- b) 100 microseconds
- c) 50 milliseconds
- d) 50 microseconds

Answer: b

Explanation: The conversion delay is 100microseconds which is low as compared to other converters.

6. The number of inputs that can be connected at a time to an ADC that is integrated with successive approximation is

- a) 4
- b) 2
- c) 8
- d) 16

Answer: c

Explanation: As these converters internally have 3:8 analog multiplexer, at a time 8 different analog inputs can be connected to the chip.

7. ADC 7109 integrated by Dual slope integration technique is used for

- a) low cost option
- b) slow practical applications
- c) low complexity
- d) all of the mentioned

Answer: d

Explanation: Compared to other 12-bit ADCs, it is of very low cost and useful for slow practical applications.

8. Which of the following is not one of the phases of the total conversion cycle?

- a) autozero phase
- b) conversion phase
- c) signal integrate phase
- d) disintegrate phase

Answer: b

Explanation: Autozero phase, signal integrate phase and disintegrate phase are the three phases of total conversion cycle.

9. Which of the following phase contain feedback loop in it?

- a) autozero phase
- b) signal integrate phase
- c) disintegrate phase
- d) none

Answer: a

Explanation: A feedback loop is closed around the system to charge the autozero capacitor to compensate for the offset voltages in the buffer amplifier, integrator and comparator.

10. In the signal integrate phase, the differential input voltage between IN LO(input low) and IN HI(input high) pins is integrated by the internal integrator for a fixed period of

- a) 256 clock cycles
- b) 1024 clock cycles

- c) 2048 clock cycles
- d) 4096 clock cycles

Answer: c

Explanation: The internal integrator needs 2048 clock cycles to integrate voltage difference between input low and input high.

To practice all Puzzles on Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessors Questions and Answers for Experienced people focuses on "Interfacing Digital to Analog Converters, Stepper Motor Interfacing and Control of High Power Devices Using 8255".

1. DAC (Digital to Analog Converter) finds application in

- a) digitally controlled gains
- b) motor speed controls
- c) programmable gain amplifiers
- d) all of the mentioned

Answer: d

Explanation: DAC is used in digitally controlled gains, motor speed controls and programmable gain amplifiers.

2. To save the DAC from negative transients the device connected between OUT1 and OUT2 of AD 7523 is

- a) p-n junction diode
- b) Zener
- c) FET
- d) BJT (Bipolar Junction transistor)

Answer: b

Explanation: Zener is connected between OUT1 and OUT2 pins of AD7523 to save from negative transients.

3. An operational amplifier connected to the output of AD 7523 is used

- a) to convert current output to output voltage
- b) to provide additional driving capability
- c) as current-to-voltage converter
- d) all of the mentioned

Answer: d

Explanation: An operational amplifier is used as a current-to-voltage converter to convert the current output to output voltage and also provides additional driving capability to the DAC.

4. The DAC 0800 has a settling time of

- a) 100 milliseconds
- b) 100 microseconds
- c) 50 milliseconds
- d) 50 microseconds

Answer: a

Explanation: DAC 0800 has a settling time of 100 milliseconds.

5. The device that is used to obtain an accurate position control of rotating shafts in terms of steps is

- a) DC motor
- b) AC motor
- c) Stepper motor
- d) Servo motor

Answer: c

Explanation: Stepper motor employs rotation of its shaft in terms of steps, rather than continuous rotation as in case of AC or DC motors.

6. The internal schematic of a typical stepper motor has

- a) 1 winding

- b) 2 windings
- c) 3 windings
- d) 4 windings

Answer: d

Explanation: The internal schematic of a typical stepper motor has 4 windings.

7. The number of pulses required for one complete rotation of the shaft of the stepper motor is equal to the

- a) number of internal teeth on a rotor
- b) number of internal teeth on a stator
- c) number of internal teeth on a rotor and stator
- d) number of external teeth on a stator

Answer: a

Explanation: The number of pulses required for one complete rotation of the shaft of the stepper motor is equal to the number of internal teeth on its rotor.

8. A simple scheme for rotating the shaft of a stepper motor is called

- a) rotating scheme
- b) shaft scheme
- c) wave scheme
- d) none

Answer: c

Explanation: In this scheme, the windings are applied with the required voltage pulses, in a cyclic fashion.

9. The firing angles of thyristors are controlled by

- a) pulse generating circuits
- b) relaxation oscillators
- c) microprocessor
- d) all of the mentioned

Answer: d

Explanation: In early days, the firing angles were controlled by a pulse generating circuits like relaxation oscillators and now, they are accurately fired using a microprocessor.

10. The Isolation transformers are generally used for

- a) protecting low power circuit
- b) isolation
- c) protecting low power circuit and isolation
- d) none

Answer: c

Explanation: Any switching component of a high power circuit may be sufficient to damage the microprocessor system. So, to protect the low power circuit isolation transformers are used. They are also used if isolation is necessary.

To practice all areas of Microprocessors for Experienced people, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Programmable Communication Interface 8251 USART".

1. Which of the following is not a mode of data transmission?

- a) simplex
- b) duplex
- c) semi duplex
- d) half duplex

Answer: c

Explanation: Basically, there are three modes of data transmission. simplex, duplex and half duplex.

2. If the data is transmitted only in one direction over a single communication channel, then it is of

- a) simplex mode
- b) duplex mode
- c) semi duplex mode
- d) half duplex mode

Answer: a

Explanation: In simplex mode, the data transmission is unidirectional. For example, a CPU may transmit data for a CRT display unit in this mode.

3. If the data transmission takes place in either direction, but at a time data may be transmitted only in one direction then, it is of

- a) simplex mode
- b) duplex mode
- c) semi duplex mode
- d) half duplex mode

Answer: d

Explanation: In half duplex mode, data transmission is bidirectional but not at a time. For example, Walkie-Talkie.

4. In 8251A, the pin that controls the rate at which the character is to be transmitted is

- a) TXC(active low)
- b) TXC(active high)
- c) TXD(active low)
- d) RXC(active low)

Answer: a

Explanation: Transmitter Clock Input (TXC(active low)) is a pin that controls the rate at which the character is to be transmitted.

5. TXD(Transmitted Data Output) pin carries serial stream of the transmitted data bits along with

- a) start bit
- b) stop bit
- c) parity bit
- d) all of the mentioned

Answer: d

Explanation: Transmitted Data Output pin carries a serial stream of the transmitted data bits along with other information like start bits, stop bits and parity bits etc.

6. The signal that may be used either to interrupt the CPU or polled by the CPU is

- a) TXRDY(Transmitter ready)
- b) RXRDY(Receiver ready output)
- c) DSR(active low)
- d) DTR(active low)

Answer: b

Explanation: RXRDY(Receiver ready output) may be used either to interrupt the CPU or polled by the CPU.

7. The disadvantage of RS-232C is

- a) limited speed of communication
- b) high-voltage level signaling
- c) big-size communication adapters
- d) all of the mentioned

Answer: d

Explanation: RS232C has been used for long and has a few disadvantages like limited speed of communication, high-voltage level signaling and big-size communication adapters.

8. The USB supports the signaling rate of

- a) full-speed USB 1.0 at rate of 12 Mbps
- b) high-speed USB 2.0 at rate of 480 Mbps
- c) super-speed USB 3.0 at rate of 596 Mbps

d) all of the mentioned

Answer: d

Explanation: The USB standards support the signaling rates. Also, USB signaling is implemented in a differential in low- and full-speed options.

9. The bit packet that commands the device either to receive data or transmit data in transmission of USB asynchronous communication is

- a) Handshake packet
- b) Token packet
- c) PRE packet
- d) Data packet

Answer: b

Explanation: The token packet is the second type of packet which commands the device either to receive data or transmit data.

10. High speed USB devices neglect

- a) Handshake packet
- b) Token packet
- c) PRE packet
- d) Data packet

Answer: c

Explanation: PRE packets are only of importance to low-speed USB devices.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on “the Keyboard/Display Controller 8279”.

1. The registers that store the keyboard and display modes and operations programmed by CPU are

- a) I/O control and data buffers
- b) Control and timing registers
- c) Return buffers
- d) Display address registers

Answer: b

Explanation: The control and timing register to store the keyboard and display modes and other operations programmed by CPU.

2. The sensor RAM acts as 8-byte first-in-first-out RAM in

- a) keyboard mode
- b) strobed input mode
- c) keyboard and strobed input mode
- d) scanned sensor matrix mode

Answer: c

Explanation: In this mode, each key code of the pressed key is entered in the order of the entry, and in the meantime, read by the CPU, till the RAM becomes empty.

3. The registers that hold the address of the word currently being written by the CPU from the display RAM are

- a) control and timing register
- b) control and timing register and timing control
- c) display RAM
- d) display address registers

Answer: d

Explanation: The display address registers holds the address of the word currently being written or read by the CPU to or from the display RAM.

4. When a key is pressed, a debounce logic comes into operation in

- a) scanned keyboard special error mode
- b) scanned keyboard with N-key rollover

- c) scanned keyboard mode with 2 key lockout
- d) sensor matrix mode

Answer: c

Explanation: In scanned keyboard mode with 2 key lockout mode of operation, when a key is pressed, a debounce logic comes into operation. During the next two scans, other keys are checked for closure and if no other key is pressed then the first pressed key is identified.

5. The mode that is programmed using “end interrupt/error mode set command” is
- a) scanned keyboard special error mode
 - b) scanned keyboard with N-key rollover
 - c) scanned keyboard mode with 2 key lockout
 - d) sensor matrix mode

Answer: a

Explanation: The scanned keyboard special error mode is programmed using end interrupt/error mode set command. This mode is valid only under the N-key rollover mode.

6. When a key is pressed, the debounce circuit waits for 2 keyboard scans and then checks whether the key is still depressed in
- a) scanned keyboard special error mode
 - b) scanned keyboard with N-key rollover
 - c) scanned keyboard mode with 2 key lockout
 - d) sensor matrix mode

Answer: b

Explanation: In this mode, When a key is pressed, the debounce circuit waits for 2 keyboard scans and then checks whether the key is still depressed. If it is still depressed, the code is entered in FIFO RAM.

7. The data that is entered from the left side of the display unit is of
- a) left entry mode
 - b) right entry mode
 - c) left and right entry modes
 - d) none

Answer: a

Explanation: The data that is entered from the left side of the display unit is of left entry mode, as in a type-writer the first character typed appears at the left-most position, while the subsequent characters appear successively to the right of the first one.

8. The FIFO status word is used to indicate the error in
- a) keyboard mode
 - b) strobed input mode
 - c) keyboard and strobed input mode
 - d) scanned sensor matrix mode

Answer: c

Explanation: Overrun error occurs when an already full FIFO has attempted an entry. Underrun error occurs when an empty FIFO read is attempted.

9. The flag that increments automatically after each read or write operation to the display RAM is
- a) IF
 - b) RF
 - c) AI
 - d) WF

Answer: c

Explanation: AI refers to auto increment flag.

10. If any change in sensor value is detected at the end of a sensor matrix scan, then the IRQ line
- a) goes low
 - b) goes high

- c) remains unchanged
- d) none

Answer: b

Explanation: In sensor matrix mode, the IRQ line goes high, if any change in sensor value is detected at the end of a sensor matrix scan or the sensor RAM has a previous entry to be read by the CPU.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on “DMA Transfers and Operations”.

1. The 8257 is able to accomplish the operation of
- a) verifying DMA operation
 - b) write operation
 - c) read operation
 - d) all of the mentioned

Answer: d

Explanation: The 8257 can accomplish three types of operations and they are

- i) verify DMA operation
- ii) write operation
- iii) read operation.

2. The bus is available when the DMA controller receives the signal
- a) HRQ
 - b) HLDA
 - c) DACK
 - d) All of the mentioned

Answer: b

Explanation: If the HLDA signal is received by the DMA controller, it indicates that the bus is available.

3. To indicate the I/O device that its request for the DMA transfer has been honored by the CPU, the DMA controller pulls
- a) HLDA signal
 - b) HRQ signal
 - c) DACK (active low)
 - d) DACK (active high)

Answer: c

Explanation: The DACK (active low) line of the used channel is pulled down by the DMA controller to indicate the I/O device that its request for the DMA transfer has been honored by the CPU.

4. If more than one channel requests service simultaneously, the transfer will occur as
- a) multi transfer
 - b) simultaneous transfer
 - c) burst transfer
 - d) none of the mentioned

Answer: c

Explanation: If more than one channel requests service simultaneously, then the transfer occurs as a burst or continuous transfer.

5. The continuous transfer may be interrupted by an external device by pulling down the signal
- a) HRQ
 - b) DACK (active low)
 - c) DACK (active high)
 - d) HLDA

Answer: d

Explanation: The burst or continuous transfer may be interrupted by an external device by pulling down the HLDA line.

6. The number of clock cycles required for an 8257 to complete a transfer is

- a) 2
- b) 4
- c) 8
- d) none of the mentioned

Answer: b

Explanation: The 8257 uses four clock cycles to complete a transfer.

7. In 8257, if each device connected to a channel is assigned to a fixed priority then it is said to be in

- a) rotating priority scheme
- b) fixed priority scheme
- c) rotating priority and fixed priority scheme
- d) none of the mentioned

Answer: b

Explanation: In this scheme, the DRQ3 has the lowest priority followed by DRQ2 and DRQ1. The DRQ0 has the highest priority.

8. The priority of the channels varies frequently in

- a) rotating priority scheme
- b) fixed priority scheme
- c) rotating priority and fixed priority scheme
- d) none of the mentioned

Answer: a

Explanation: In this scheme, the priorities assigned to the channels are not fixed.

9. The register of 8257 that can only be written in is

- a) DMA address register
- b) Terminal count register
- c) Mode set register
- d) Status register

Answer: c

Explanation: The selected register may be read or written depending on the instruction executed by the CPU. But only write operation can be performed on the mode set register.

10. The operation that can be performed on the status register is

- a) write operation
- b) read operation
- c) read and write operations
- d) none of the mentioned

Answer: b

Explanation: The status register can only be read.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "DMA Controller 8257".

1. In direct memory access mode, the data transfer takes place

- a) directly
- b) indirectly
- c) directly and indirectly
- d) none of the mentioned

Answer: a

Explanation: In direct memory access mode, the data may transfer directly without the interference from the CPU.

2. In 8257 (DMA), each of the four channels has
- a) a pair of two 8-bit registers
 - b) a pair of two 16-bit registers
 - c) one 16-bit register
 - d) one 8-bit register

Answer: b

Explanation: The DMA supports four channels, and each of the channels has a pair of two 16-bit registers, namely DMA address register and a terminal count register.

3. The common register(s) for all the four channels of 8257 is
- a) DMA address register
 - b) Terminal count register
 - c) Mode set register and status register
 - d) None of the mentioned

Answer: c

Explanation: The two common registers for all the four channels of DMA are mode set register and status register.

4. In 8257 register format, the selected channel is disabled after the terminal count condition is reached when
- a) Auto load is set
 - b) Auto load is reset
 - c) TC STOP bit is reset
 - d) TC STOP bit is set

Answer: d

Explanation: If the TC STOP bit is set, the selected channel is disabled after the terminal count condition is reached, and it further prevents any DMA cycle on the channel.

5. The IOR (active low) input line acts as output in
- a) slave mode
 - b) master mode
 - c) master and slave mode
 - d) none of the mentioned

Answer: b

Explanation: The IOR (active low) is an active low bidirectional tristate input line, that acts as input in the slave mode, and acts as output in the master mode. In master mode, this signal is used to read data from a peripheral during a memory write cycle.

6. The IOW (active low) in its slave mode loads the contents of a data bus to
- a) 8-bit mode register
 - b) upper/lower byte of 16-bit DMA address register
 - c) terminal count register
 - d) all of the mentioned

Answer: d

Explanation: In its slave mode, the IOW (active low) loads the contents of a data bus to 8-bit mode register, upper/lower byte of 16-bit DMA address register or terminal count register.

7. The pin that disables all the DMA channels by clearing the mode registers is
- a) MARK
 - b) CLEAR
 - c) RESET
 - d) READY

Answer: c

Explanation: The RESET pin which is asynchronous input disables all the DMA channels by clearing the mode registers, and tristate all the control lines.

8. The pin that requests the access of the system bus is
- a) HLDA
 - b) HRQ

- c) ADSTB
- d) None of the mentioned

Answer: b

Explanation: The hold request output requests the access of the system bus.

9. The pin that is used to write data to the addressed memory location, during DMA write operation is

- a) MEMR (active low)
- b) AEN
- c) MEMW (active low)
- d) IOW (active low)

Answer: c

Explanation: The MEMW (active low) is used to write data to the addressed memory location, during DMA write operation.

10. The pin that strobes the higher byte of the memory address, generated by the DMA controller into the latches is

- a) AEN
- b) ADSTB
- c) TC
- d) None of the mentioned

Answer: b

Explanation: The pin ADSTB strobes the higher byte of the memory address, generated by the DMA controller into the latches.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Programmable Interrupt Controller 8259A".

1. The number of hardware interrupts that the processor 8085 consists of is

- a) 1
- b) 3
- c) 5
- d) 7

Answer: c

Explanation: The processor 8085 has five hardware interrupt pins. Out of these five, four pins were allotted fixed vector addresses but the pin INTR was not allotted by vector address, rather an external device was supposed to hand over the type of the interrupt to the microprocessor.

2. The register that stores all the interrupt requests in it in order to serve them one by one on a priority basis is

- a) Interrupt Request Register
- b) In-Service Register
- c) Priority resolver
- d) Interrupt Mask Register

Answer: a

Explanation: The interrupts at IRQ input lines are handled by Interrupt Request Register internally.

3. The register that stores the bits required to mask the interrupt inputs is

- a) In-service register
- b) Priority resolver
- c) Interrupt Mask register
- d) None

Answer: c

Explanation: Also, Interrupt Mask Register operates on IRR(Interrupt Request Register) at the direction of the Priority Resolver.

4. The interrupt control logic
- a) manages interrupts
 - b) manages interrupt acknowledge signals
 - c) accepts interrupt acknowledge signal
 - d) all of the mentioned

Answer: d

Explanation: The interrupt control logic performs all the operations that are involved within the interrupts like accepting and managing interrupt acknowledge signals, interrupts.

5. In a cascaded mode, the number of vectored interrupts provided by 8259A is
- a) 4
 - b) 8
 - c) 16
 - d) 64

Answer: d

Explanation: A single 8259A provides 8 vectored interrupts. In cascade mode, 64 vectored interrupts can be provided.

6. When the PS(active low)/EN(active low) pin of 8259A used in buffered mode, then it can be used as a
- a) input to designate chip is master or slave
 - b) buffer enable
 - c) buffer disable
 - d) none

Answer: b

Explanation: When the pin is used in buffered mode, then it can be used as a buffer enable to control buffer transreceivers. If it is not used in buffered mode, then the pin is used as input to designate whether the chip is used as a master or a slave.

7. Once the ICW1 is loaded, then the initialization procedure involves
- a) edge sense circuit is reset
 - b) IMR is cleared
 - c) slave mode address is set to 7
 - d) all of the mentioned

Answer: d

Explanation: The initialization procedure involves

- i) edge sense circuit is reset.
- ii) IMR is cleared.
- iii) IR7 input is assigned the lowest priority.
- iv) slave mode address is set to 7
- v) special mask mode is cleared and the status read is set to IRR.

8. When non-specific EOI command is issued to 8259A it will automatically
- a) set the ISR
 - b) reset the ISR
 - c) set the INTR
 - d) reset the INTR

Answer: b

Explanation: When non-specific EOI command is issued to 8259A it will automatically reset the highest ISR.

9. In the application where all the interrupting devices are of equal priority, the mode used is
- a) Automatic rotation
 - b) Automatic EOI mode
 - c) Specific rotation
 - d) EOI

Answer: a

Explanation: The automatic rotation is used in the applications where all the interrupting devices are of equal priority.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Programmable DMA Interface 8237 -1".

1. The block of 8237 that decodes the various commands given to the 8237 by the CPU is
- a) timing and control block
 - b) program command control block
 - c) priority block
 - d) none of the mentioned

Answer: b

Explanation: The program control block decodes various commands given to the 8237 by the CPU before servicing a DMA request.

2. The priority between the DMA channels requesting the services can be resolved by
- a) timing and control block
 - b) program command control block
 - c) priority block
 - d) none of the mentioned

Answer: c

Explanation: The priority encoder block resolves the priority between the DMA channels requesting the services.

3. The register that holds the current memory address is
- a) current word register
 - b) current address register
 - c) base address register
 - d) command register

Answer: b

Explanation: The current address register holds the current memory address. The current address register is accessed during the DMA transfer.

4. The register that holds the data byte transfers to be carried out is
- a) current word register
 - b) current address register
 - c) base address register
 - d) command register

Answer: a

Explanation: The current word register is a 16-bit register that holds the data transfers. The word count is decremented after each transfer, and the new value is stored again in the register.

5. When the count becomes zero in the current word register then
- a) Input signal is enabled
 - b) Output signal is enabled
 - c) EOP (end of process) is generated
 - d) Start of process is generated

Answer: c

Explanation: When the count becomes zero, the EOP signal is generated. This can be written in successive bytes by the CPU, in program mode.

6. The current address register is programmed by the CPU as
- a) bit-wise
 - b) byte-wise
 - c) bit-wise and byte-wise
 - d) none of the mentioned

Answer: b

Explanation: The current address register is byte-wise programmed by the CPU, i.e. lower byte first and the higher byte later.

7. Which of these register's contents is used for auto-initialization (internally)?

- a) current word register
- b) current address register
- c) base address register
- d) command register

Answer: c

Explanation: The contents of base address register cannot be read by the CPU. These contents are used internally for auto-initialization.

8. The register that maintains an original copy of the respective initial current address register and current word register is

- a) mode register
- b) base address register
- c) command register
- d) mask register

Answer: b

Explanation: The base address register maintains an original copy of the current address register and current word register, before incrementing or decrementing.

9. The register that can be automatically incremented or decremented, after each DMA transfer is

- a) mask register
- b) mode register
- c) command register
- d) current address register

Answer: d

Explanation: The address is automatically incremented or decremented after each DMA transfer, and the resulting address value is again stored in the current address register.

10. Which of the following is a type of DMA transfer?

- a) memory read
- b) memory write
- c) verify transfer
- d) all of the mentioned

Answer: d

Explanation: Memory read, memory write and verify transfer are the three types of DMA transfer.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessors Question Paper focuses on "Programmable DMA Interface 8237-2".

1. Each bit in the request register is cleared by

- a) under program control
- b) generation of TC
- c) generation of an external EOP
- d) all of the mentioned

Answer: d

Explanation: In the request register, each bit is set or reset under program control or is cleared upon generation of a TC or an external EOP.

2. The register that holds the data during memory to memory data transfer is

- a) mode register
- b) temporary register
- c) command register
- d) mask register

Answer: b

Explanation: The temporary register holds the data during memory to memory data transfers.

After the completion of the transfer operation, the last word transferred remains in the temporary register, until it is cleared by a reset operation.

3. The register that keeps track of all the DMA channel pending requests and status of their terminal counts is

- a) mask register
- b) request register
- c) status register
- d) count register

Answer: c

Explanation: The status register keeps track of all the DMA channel pending requests, and status of their terminal counts. These are cleared upon reset.

4. The pin that clears the command, request and temporary registers, and internal first/last flipflop when it is set is

- a) CLEAR
- b) SET
- c) HLDA
- d) RESET

Answer: d

Explanation: A high on the reset pin clears the command, status, request and temporary registers, and also clears the internal first/last flipflop.

5. The DMA request input pin that has the highest priority is

- a) DREQ0
- b) DREQ1
- c) DREQ2
- d) DREQ3

Answer: a

Explanation: DREQ0 has the highest priority while DREQ3 has the lowest one. The priorities of the DREQ lines is programmable.

6. When interface 8237 does not have any valid pending DMA request then it is said to be in

- a) active state
- b) passive state
- c) idle state
- d) none of the mentioned

Answer: c

Explanation: If 8237 is in idle state, then CPU may program it in this state.

7. To complete a DMA transfer, a memory to memory transfer requires

- a) a read from memory cycle
- b) a write to memory cycle
- c) a read-from and write-to memory cycle
- d) none of the mentioned

Answer: c

Explanation: A memory to memory transfer is a two cycle operation and requires a read from and write-to memory cycle, to complete each DMA transfer.

8. In demand transfer mode of 8237, the device stops data transfer when

- a) a TC (terminal count) is reached
- b) an external EOP (active low) is detected
- c) the DREQ signal goes inactive
- d) all of the mentioned

Answer: d

Explanation: In demand transfer mode, the device continues transfers till a TC is reached or an external EOP is detected or the DREQ signal goes inactive.

9. The mode of 8237 in which the device transfers only one byte per request is

- a) block transfer mode

- b) single transfer mode
- c) demand transfer mode
- d) cascade mode

Answer: b

Explanation: In single mode, the device transfers only one byte per request. For each transfer, the DREQ must be active until the DACK is activated.

10. The transfer of a block of data from one set of memory address to another takes place in

- a) block transfer mode
- b) demand transfer mode
- c) memory to memory transfer mode
- d) cascade mode

Answer: c

Explanation: To perform the transfer of a block of data from one set of a memory address to another one, this transfer mode is used.

11. Which of the following command is used to make all the internal registers of 8237 clear?

- a) clear first/last flipflop
- b) master clear command
- c) clear mask register
- d) none of the mentioned

Answer: b

Explanation: Using master clear command, all the internal registers of 8237 are cleared, while all the bits of the mask register are set.

To practice all questions papers on Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on “Salient Features of 80286”.

1. The 80286 is able to address the physical memory of

- a) 8 MB
- b) 16 MB
- c) 24 MB
- d) 64 MB

Answer: b

Explanation: The 80286 with its 24-bit address bus is able to address 16 Mbytes of physical memory.

2. The 80286 is able to operate with the clock frequency of

- a) 12.5 MHz
- b) 10 MHz
- c) 8 MHz
- d) all of the mentioned

Answer: d

Explanation: Various versions of 80286 are available that run on 12.5 MHz, 10 MHz and 8 MHz clock frequencies.

3. The management of the memory system required to ensure the smooth execution of the running process is done by

- a) control unit
- b) memory
- c) memory management unit
- d) bus interface unit

Answer: c

Explanation: The memory management which is an important task of the operating system is now supported by a hardware unit called a memory management unit.

4. The fetching of the program from secondary memory to place it in physical memory, during the execution of CPU is called

- a) mapping
- b) swapping in
- c) swapping out
- d) pipelining

Answer: b

Explanation: Whenever the portion of a program is required for execution by the CPU, it is fetched from the secondary memory and placed in the physical memory. This is called swapping in of the program.

5. The process of making the physical memory free by storing the portion of program and partial results in the secondary storage called

- a) mapping
- b) swapping in
- c) swapping out
- d) pipelining

Answer: c

Explanation: In swapping out, a portion of the program or important partial results required for further execution, may be saved back on secondary storage to make the physical memory free, for further execution of another required portion of the program.

6. The memory that is considered as a large logical memory space, that is not available physically is

- a) logical memory
- b) auxiliary memory
- c) imaginary memory
- d) virtual memory

Answer: d

Explanation: To the user, there exists a very large logical memory space, which is actually not available called virtual memory. This does not exist physically in a system. It is however, possible to map a large virtual memory space onto the real physical memory.

7. Memory management deals with

- a) data protection
- b) unauthorized access prevention
- c) segmented memory
- d) all of the mentioned

Answer: d

Explanation: The important aspects of memory management are data protection, unauthorized access prevention, and segmented memory.

8. The memory management and protection mechanisms are disabled when the 80286 is operated in

- a) normal mode
- b) real address mode
- c) virtual address mode
- d) all of the mentioned

Answer: b

Explanation: In real address mode of 80286, all the memory management and protection mechanisms are disabled.

9. The memory management and protection mechanisms are enabled with advanced instruction set when 80286 is operated in

- a) normal mode
- b) real address mode
- c) virtual address mode
- d) all of the mentioned

Answer: c

Explanation: In virtual address mode, 80286 works with all of its memory management and protection capabilities, with the advanced instruction set.

10. The 80286 is an upward object code compatible with 8086 or 8088 when operated in
- a) normal mode
 - b) real address mode
 - c) virtual address mode
 - d) real and virtual address mode

Answer: d

Explanation: The 80286 is operated in two modes, namely real address mode and virtual address mode. In both the modes, the 80286 is compatible with 8086/8088.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on “High Storage Capacity Memory Devices”.

1. The basic principle of floppy disks involve
- a) magnetic data reading
 - b) magnetic data recording
 - c) magnetic data recording and reading
 - d) none of the mentioned

Answer: c

Explanation: Whatever their physical sizes and storage formats, all the floppies incorporate the basic principles of magnetic data recording and reading.

2. In floppy disk, the small hole that enables the drive to identify the beginning of a track and its first sector is
- a) inner hole
 - b) key hole
 - c) index hole
 - d) start hole

Answer: c

Explanation: The small hole called index hole, enables the drive to identify the beginning of a track and its first sector.

3. Inside its jacket, the floppy media is rotated at the speed of
- a) 200 RPM
 - b) 300 RPM
 - c) 150 RPM
 - d) 50 RPM

Answer: b

Explanation: The floppy media is rotated at the speed of 300 RPM (Revolution Per Minute) inside its jacket.

4. The Double Density Double Sided disks on each side are organized with
- a) 20 tracks
 - b) 30 tracks
 - c) 40 tracks
 - d) 50 tracks

Answer: c

Explanation: The Double Density Double Sided (DDDS) disks are organized with 40 tracks on each side of the disk.

5. The magnetic recording technique used for storing data onto the disks (floppy disks) is called
- a) return to zero
 - b) non-return to zero
 - c) return to zero and Non-return to zero
 - d) none of the mentioned

Answer: b

Explanation: In this technique, the magnetic flux on the disk surface never returns to zero, i.e. no erase operation is carried out.

6. For reading the disks DVD uses

- a) blue laser
- b) white laser
- c) red laser
- d) green laser

Answer: c

Explanation: A DVD is an optical disk that uses a red laser for reading the disks.

7. For reading the disks, the blue ray disk uses

- a) high frequency red laser
- b) low frequency red laser
- c) high frequency blue laser
- d) low frequency blue laser

Answer: c

Explanation: The blue ray disk uses a high frequency blue laser with a small wavelength to read the disk.

8. A blue ray disk can store data upto _____ per layer.

- a) 25 KB
- b) 25 MB
- c) 25 TB
- d) 25 GB

Answer: d

Explanation: A blue ray disk can store data upto 25 GB per layer and is popularly used for storing long duration videos like movies.

9. DVDRW is for

- a) read-write DVD
- b) rewriteable DVD
- c) recordable DVD
- d) none of the mentioned

Answer: b

Explanation: DVDRW is for rewriteable DVD and DVDR is for recordable DVD.

10. The HDD is also called as

- a) hard disk
- b) hard drive
- c) fixed disk
- d) all of the mentioned

Answer: d

Explanation: The Hard Disk Drive is also called as a hard disk, hard drive, fixed drive, fixed disk or fixed disk drive.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Internal Architecture of 80286".

1. The CPU of 80286 contains

- a) 16-bit general purpose registers
- b) 16-bit segment registers
- c) status and control register
- d) all of the mentioned

Answer: d

Explanation: The CPU of 80286 contains the same set of registers as in 8086.

2. The bits that are modified according to the result of the execution of logical and arithmetic instructions are called

- a) byte addressable bit
- b) control flag bits
- c) status flag bit
- d) none of the mentioned

Answer: c

Explanation: The flag register bits, D0, D2, D4, D6, D7 and D11 are modified according to the result of the execution of logical and arithmetic instructions. These are called as status flag bits.

3. The flags that are used for controlling machine operation are called

- a) status flags
- b) control flags
- c) machine controlled flags
- d) all of the mentioned

Answer: b

Explanation: The flags such as trap flag (TF) and Interrupt flag (IF) bits are used for controlling the machine operation, and thus they are called control flags.

4. The additional field that is available in 80286 is

- a) I/O Privilege field
- b) nested task flag
- c) protection enable
- d) all of the mentioned

Answer: d

Explanation: The additional fields available in 80286 flag register are, I/O Privilege field, nested task flag, protection enable, and monitor processor extension.

5. Which of the block is not considered as a block of an architecture of 80286?

- a) address unit
- b) bus unit
- c) instruction unit
- d) control unit

Answer: d

Explanation: The CPU may be viewed to contain four functional parts and they are

- i) Address Unit
- ii) Bus Unit
- iii) Instruction Unit
- iv) Execution Unit.

6. The unit that is responsible for calculating the address of instructions, and data that the CPU wants to access is

- a) bus unit
- b) address unit
- c) instruction unit
- d) control unit

Answer: b

Explanation: The address unit is responsible for calculating the address of instructions, and data that the CPU wants to access. Also, the address lines derived by this unit may be used to address different peripherals.

7. The process of fetching the instructions in advance, and storing in the queue is called

- a) mapping
- b) swapping
- c) instruction pipelining
- d) storing

Answer: c

Explanation: The instructions are fetched in advance and stored in a queue to enable faster execution of the instructions. This concept is known as instruction pipelining.

8. The CPU must flush out the prefetched instructions immediately following the branch instruction in

- a) conditional branch
- b) unconditional branch
- c) conditional and unconditional branches
- d) none of the mentioned

Answer: b

Explanation: In case of unconditional branch, the CPU will have to flush out the prefetched instructions, immediately following the branch instruction.

9. The device that interfaces and control the internal data bus with the system bus is

- a) data interface
- b) controller interface
- c) data and control interface
- d) data transreceiver

Answer: d

Explanation: The data transreceivers interface and control the internal data bus with the system bus.

10. The register bank of Execution Unit of 80286 is used as

- a) for storing data
- b) scratch pad
- c) special purpose registers
- d) all of the mentioned

Answer: d

Explanation: The execution unit contains the register bank, used for storing the data as scratch pad, or used as special purpose registers.

11. Which of the following is not an interrupt generated by 80286?

- a) software interrupts
- b) hardware or external interrupts
- c) INT instruction
- d) none of the mentioned

Answer: d

Explanation: The interrupts generated by 80286 may be divided into 3 categories as external or hardware interrupts, INT instruction or software interrupts and interrupts generated by exceptions.

12. For which of the following instruction does the return address point to instruction causing an exception?

- a) divide error exception
- b) bound range exceeded exception
- c) invalid opcode exception
- d) all of the mentioned

Answer: d

Explanation: For the instructions, divide error, bound range exceeded and invalid opcode exceptions, the return address points to the instruction causing exception.

13. The instruction that comes into action, if the trap flag is set is

- a) maskable interrupt
- b) non-maskable interrupt
- c) single step interrupt
- d) breakpoint interrupt

Answer: c

Explanation: Single step interrupt is an internal interrupt that comes into action if the trap flag (TF) is set.

14. The interrupt that has the highest priority among the following is

- a) Single step
- b) NMI (non-maskable interrupt)
- c) INTR
- d) Instruction exception

Answer: d

Explanation: The instruction exception has the highest priority followed by single step, NMI and INTR instruction.

15. The interrupt that has the lowest priority among the following is

- a) Processor extension segment overrun
- b) INTR
- c) INT instruction
- d) NMI

Answer: c

Explanation: The INT instruction has the lowest priority. The order of priority of interrupts from high to low is

- 1) instruction exception
- 2) single step
- 3) NMI
- 4) processor extension segment overrun
- 5) INTR
- 6) INT instruction.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Signal Descriptions of 80286".

1. The 80286 is available in the package as

- a) 68-pin PLCC (plastic leaded chip carrier)
- b) 68-pin LCC (lead less chip carrier)
- c) 68-pin PGA (pin grid array)
- d) all of the mentioned

Answer: d

Explanation: The 80286 is available in 68-pin PLCC (plastic leaded chip carrier), 68-pin LCC (lead less chip carrier) and 68-pin PGA (pin grid array) packages.

2. The clock frequency applied at the CLK pin is internally divided by

- a) 2
- b) 4
- c) 8
- d) 1

Answer: a

Explanation: The clock frequency is divided by two internally, and is used for deriving fundamental timings for basic operations of the circuit.

3. The 8 address lines, A23-A16 of 80286 are zero during

- a) memory transfer
- b) address transfer
- c) memory to processor transfer
- d) I/O transfer

Answer: d

Explanation: The address lines, A23-A16 are zero during I/O transfers.

4. The signals S1 (active low), S2 (active low) are
- a) output signals
 - b) indicate initiation of bus cycle
 - c) define type of bus cycle with M/IO (active low)
 - d) all of the mentioned

Answer: d

Explanation: The signals S1 (active low), S2 (active low) are active low status output signals, which indicate initiation of a bus cycle, and with M/IO (active low) and COD/INTA (active low), they define the type of the bus cycle.

5. If M/IO (active low) signal is '0' then it indicates
- a) I/O cycle
 - b) Memory cycle
 - c) I/O cycle or INTA cycle
 - d) I/O cycle or HALT cycle

Answer: c

Explanation: If M/IO (active low) signal is '0' then it indicates that an I/O cycle or INTA cycle is in the process, and if it is '1', it indicates that a memory or a HALT cycle is in progress.

6. The LOCK (active low) is activated automatically by hardware using
- a) XCHG signal
 - b) Interrupt acknowledge
 - c) Descriptor table access
 - d) All of the mentioned

Answer: d

Explanation: The lock pin is used to prevent the other masters from gaining the control of the bus, for the current and the following bus cycles. This pin is activated by a "LOCK" instruction prefix, or automatically by hardware during XCHG, interrupt acknowledge or descriptor table access.

7. The pin that is used to insert wait states in a bus cycle is
- a) WAIT
 - b) BHE (active low)
 - c) READY (active low)
 - d) WAIT(active low)

Answer: c

Explanation: The active low READY pin is used to insert wait states in a bus cycle, for interfacing low speed peripherals. This signal is neglected during HLDA cycle.

8. The minimum number of clock cycles required in an input pulse width of the RESET pin is
- a) 4
 - b) 2
 - c) 8
 - d) 16

Answer: d

Explanation: The active high RESET input clears the internal logic of 80286, and re-initializes it. The reset input pulse width should be at least 16 clock cycles.

9. To filter the output, a 0.047microfarads, 12V capacitor is connected between the pins
- a) CAP and ground
 - b) Output pin and ground
 - c) CAP and Vcc
 - d) NMI and ground

Answer: a

Explanation: A 0.047microfarads, 12V capacitor is connected between the CAP pin and ground, to filter the output of the internal substrate bias generator.

10. The signal that causes the 80286 to perform the processor extension interrupt while executing the WAIT and ESC instructions are

- a) BUSY (active low)
- b) PEACK (active low)
- c) PEREQ
- d) ERROR (active low)

Answer: d

Explanation: An active ERROR (active low) signal causes the 80286 to perform the processor extension interrupt while executing the WAIT and ESC instructions.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Real Addressing Mode".

1. The 80286 CPU acts just like that of 8086 when operated in
- a) real addressing mode
 - b) protected virtual address mode
 - c) real and protected virtual address modes
 - d) none of the mentioned

Answer: a

Explanation: In the real addressing mode of operation of 80286, it just acts as a fast 8086.

2. In real addressing mode, the 80286 addresses a physical memory of
- a) 16 MB
 - b) 8 MB
 - c) 2 MB
 - d) 1 MB

Answer: d

Explanation: In real addressing mode, the 80286 addresses a physical memory of 1 Mbytes using A0-A19. The lines A20-A23 are not used by the internal circuit of 80286 in this mode.

3. In real addressing mode, the 80286 operates at a speed
- a) faster than that of 8086
 - b) half of that of 8086
 - c) slower than that of 8086
 - d) same as that of 8086

Answer: a

Explanation: Because of extra pipelining and other circuit level improvements, in real address mode also, the 80286 operates at a much faster rate than 8086.

4. In physical memory, if the segment size limit is exceeded by the instruction or data then
- a) instruction is not executed
 - b) exception is generated
 - c) saves to next segment automatically
 - d) none of the mentioned

Answer: b

Explanation: An exception is generated if the segment size limit is exceeded by the instruction or the data.

5. The 80286 reserves fixed area of physical memory for
- a) system initialization
 - b) interrupt vector table
 - c) system initialization and interrupt vector table
 - d) none of the mentioned

Answer: c

Explanation: The 80286 reserves two fixed areas of physical memory for system initialization and interrupt vector table.

6. In the real mode, the memory that is reserved for interrupt vector table is
- a) first 2 KB of memory
 - b) first 1 KB of memory

- c) last 2 KB of memory
- d) last 1 KB of memory

Answer: b

Explanation: In the real mode, the first 1 Kbyte of memory starting from the address 00000H to 003FFH, is reserved for interrupt vector table.

7. In the real mode, the memory that is reserved for system initialization is

- a) from 004FFH to 0FFFFH
- b) from 004FFH to 05FFFFH
- c) from FFFF0H to FFFFFH
- d) from FFF00H to FFFFFH

Answer: c

Explanation: The addresses from FFFF0H to FFFFFH are reserved for system initialization, in real addressing mode.

8. When 80286 is reset, it always starts its execution in

- a) protected virtual addressing mode
- b) real addressing mode
- c) either real or protected virtual address modes
- d) none of the mentioned

Answer: b

Explanation: When 80286 is reset, it always starts its execution in real addressing mode.

9. The 80286 in real addressing mode performs

- a) initialization of IP
- b) enables interrupts
- c) sets up descriptor table
- d) all of the mentioned

Answer: d

Explanation: The 80286 in real addressing mode performs the following functions: it initializes IP and other registers of 80286, initializes the peripheral, enables interrupts, sets up descriptor tables, and then prepares it for entering the protected virtual address mode.

10. In real address mode, while addressing the physical memory, the 80286 uses the signal

- a) HLDA
- b) BHE (active low)
- c) CAP
- d) HOLD

Answer: b

Explanation: In real address mode, while addressing the physical memory, the 80286 uses BHE (active low) along with A0-A19.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Protected Virtual Address Mode (PVAM) -1".

1. The procedure of fetching the chosen program segments or data from the secondary storage into the physical memory is

- a) mapping
- b) swapping
- c) unswapping
- d) pipelining

Answer: b

Explanation: Swapping is the procedure of fetching the chosen program segments or data from the secondary storage into the physical memory.

2. The procedure of storing back the partial results on to the secondary storage is called

- a) mapping
- b) swapping

- c) unswapping
- d) pipelining

Answer: c

Explanation: The procedure of storing back the partial results or data back on to the secondary storage is called unswapping.

3. The ability of 80286 to address the virtual memory per task is

- a) 1MB
- b) 1GB
- c) 1TB
- d) none of the mentioned

Answer: b

Explanation: The 80286 is able to address 1Gbyte of virtual memory per task.

4. The branch instructions are handled by

- a) swapping mechanism
- b) unswapping mechanism
- c) operating system
- d) all of the mentioned

Answer: d

Explanation: The handling of branch instructions like JUMP and CALL is taken care of, by the swapping and unswapping mechanism, and operating system.

5. A descriptor contains information of

- a) program segment
- b) page
- c) regarding segment and its access rights
- d) all of the mentioned

Answer: d

Explanation: The segments or pages have been associated with a data structure known as a descriptor. The descriptor contains information on the page, and also carry relevant information regarding a segment, and its access rights.

6. The descriptors that are used for subroutines and interrupt service routines are

- a) data segment descriptors
- b) gate descriptors
- c) code segment descriptors
- d) system segment descriptors

Answer: b

Explanation: For data segment, the corresponding descriptor may be data segment descriptor and for code segment, there may be code segment descriptor. For subroutines and interrupt service routines there are gate descriptors.

7. A segment with low privilege level is not allowed to access another segment of

- a) low privilege level
- b) high privilege level
- c) low and high privilege level
- d) none of the mentioned

Answer: b

Explanation: A segment with low privilege level is not allowed to access another segment with high privilege level.

8. A descriptor is used to carry out

- a) transfer of control
- b) task switching
- c) to store privilege level and segment limit
- d) all of the mentioned

Answer: d

Explanation: A descriptor is used to carry out additional functions like transfer of control and task switching.

9. The descriptor that is used for special system data segments and control transfer operations is

- a) data segment descriptors
- b) gate descriptors
- c) code segment descriptors
- d) system segment descriptors

Answer: d

Explanation: The 80286 has system segment descriptor, that is used for special system data segments, and control transfer operations.

10. A code segment descriptor contains

- a) 16-bit segment limit
- b) 24-bit segment base address
- c) 8-bit access rights byte
- d) all of the mentioned

Answer: d

Explanation: A code or data segment descriptor contains 16-bit segment limit, 24-bit segment base address, 8-bit access rights byte and the remaining 16-bits are reserved by Intel for upward compatibility.

11. In access rights byte, if P (Present)=1, then the segment is mapped into

- a) physical memory
- b) virtual memory
- c) no mapping takes place
- d) none of the mentioned

Answer: a

Explanation: If P=1, then the segment is mapped into physical memory.

12. In access rights byte, to select system segment descriptor, the condition is

- a) S=1
- b) S=0
- c) S not equal to zero
- d) none of the mentioned

Answer: b

Explanation: If S (segment descriptor)=0, then system segment descriptor or gate descriptor is selected.

13. If S (segment descriptor)=1, then the descriptor selected is

- a) code segment descriptor
- b) data segment descriptor
- c) stack segment descriptor
- d) all of the mentioned

Answer: d

Explanation: If S=1, then code or data (including stack) segment descriptors are selected.

14. The memory of limit field is

- a) 2 bits
- b) 4 bits
- c) 8 bits
- d) 16 bits

Answer: d

Explanation: The limit field, which is the maximum allowed offset address, is of 16 bits.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers.](#)

This set of Advanced Microprocessors Questions and Answers focuses on "Protected Virtual Address Mode (PVAM) -2".

1. Which of the following is a type of system segment descriptor?

- a) system descriptor
- b) gate descriptor
- c) system descriptor and gate descriptor
- d) none of the mentioned

Answer: c

Explanation: The system segment descriptors are of seven types. The types 1 to 3 are called system descriptors and the types 4 to 7 are called gate descriptors.

2. Which of the following is a type of gate descriptor?

- a) call gate
- b) task gate
- c) interrupt gate
- d) all of the mentioned

Answer: d

Explanation: The gate descriptors are of four types namely, call gate, task gate, interrupt gate and trap gate.

3. The gate descriptor contains the information of

- a) destination of control transfer
- b) stack manipulations
- c) privilege level
- d) all of the mentioned

Answer: d

Explanation: The gate descriptor contains the information regarding the destination of control transfer, required stack manipulations, privilege level and its type.

4. The gate that is used to alter the privilege levels is

- a) call gate
- b) task gate
- c) interrupt gate
- d) trap gate

Answer: a

Explanation: Call gates are used to alter the privilege levels.

5. The gate that is used to specify a corresponding service routine is

- a) call gate and trap gate
- b) task gate and interrupt gate
- c) interrupt gate and trap gate
- d) task gate and trap gate

Answer: c

Explanation: Interrupt gates and trap gates are used to specify corresponding service routines.

6. The gate that is used to switch from one task to another is

- a) trap gate
- b) task gate
- c) task gate and trap gate
- d) none of the mentioned

Answer: b

Explanation: Task gate is used to switch from one task to another.

7. The gate that uses word count field is

- a) trap gate
- b) task gate
- c) interrupt gate
- d) call gate

Answer: d

Explanation: The word count field is only used by a call gate descriptor, to indicate the number of bytes to be transferred from the stack of the calling routine to the stack of the called routine.

8. The memory that maintains the most frequently required data for execution, in a high speed memory is called

- a) virtual memory
- b) physical memory
- c) cache memory
- d) ROM (read only memory)

Answer: c

Explanation: To minimize the time required for fetching the frequently required descriptor information, from the main memory, cache memory is used in which the most frequently required data for execution is stored.

9. The selector field consists of

- a) requested privilege level (RPL)
- b) table indicator
- c) index
- d) all of the mentioned

Answer: d

Explanation: In the protected mode, the contents of the segment registers are known as selectors. The selector field consists of three fields namely, RPL, table indicator (TI) and index.

10. If table indicator, TI=0, then the descriptor table selected is

- a) local descriptor table
- b) global descriptor table
- c) local and global descriptor table
- d) none of the mentioned

Answer: b

Explanation: The type of descriptor table is global if TI=0 and local if TI=1.

11. The instruction that is executed at privilege level zero (0) is

- a) LDT
- b) LGDT and LLDT
- c) GDT
- d) None of the mentioned

Answer: b

Explanation: The LGDT and LLDT instructions are privileged, and may be executed only at privilege level 0.

12. The instruction that loads a selector which refers to a local descriptor table, containing the base address and limit for LDT is

- a) LGT
- b) GDT
- c) LGDT
- d) LLDT

Answer: d

Explanation: The LLDT instruction loads a selector, which refers to a local descriptor table, containing the base address, and limit for LDT.

13. The descriptor that is used to store task gates, interrupt gates and trap gates is

- a) system descriptor table
- b) gate descriptor table
- c) interrupt descriptor table
- d) none of the mentioned

Answer: c

Explanation: The 80286 has a third type of descriptor table known as interrupt descriptor table, which is used to store task gates, interrupt gates and trap gates.

14. The number of interrupt descriptors that the interrupt descriptor table (IDT) handles is

- a) 16
- b) 64
- c) 128
- d) 256

Answer: d

Explanation: The IDT is able to handle upto 256 interrupt descriptors.

15. The number of bytes required for an interrupt in an IDT is

- a) 2
- b) 4
- c) 6
- d) 8

Answer: c

Explanation: Six bytes are required for each interrupt in an interrupt descriptor table.

To practice advanced questions and answers on all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Privilege".

1. By using privilege mechanism the protection from unauthorized accesses is done to

- a) operating system
- b) interrupt handlers
- c) system software
- d) all of the mentioned

Answer: d

Explanation: The operating system, interrupt handlers and other system softwares can be protected from unauthorized accesses in virtual address space of each task using the privilege mechanism.

2. The task privilege level at the instant of execution is called

- a) Descriptor privilege level (DPL)
- b) Current privilege level (CPL)
- c) Effective privilege level (EPL)
- d) None of the mentioned

Answer: b

Explanation: Any one of the four privilege levels may be used to execute a task. The task privilege level at that instant is called the Current Privilege Level (CPL).

3. Once the CPL is selected, it can be changed by

- a) hold
- b) transferring control using system descriptors
- c) transferring control using gate descriptors
- d) transferring control using interrupt descriptors

Answer: c

Explanation: Once the CPL is selected, it cannot be changed during the execution normally in a single code segment. It can only be changed by transferring the control, using gate descriptors, to a new segment.

4. The data segments defined in GDT (global descriptor table) and the LDT (local descriptor table) can be accessed by a task with

- a) privilege level 0
- b) privilege level 1
- c) privilege level 2
- d) privilege level 3

Answer: a

Explanation: A task executing at level 0, the most privileged level, can access all the data segments defined in GDT and the LDT of the task.

5. A task with privilege level 0, doesn't refer to all the lower level privilege descriptors in

- a) GDT (global descriptor table)
- b) LDT (local descriptor table)
- c) IDT (interrupt descriptor table)
- d) None of the mentioned

Answer: b

Explanation: The task with privilege level 0, refers to all the lower level privilege descriptors which apply to all the descriptors except the LDT descriptors.

6. The selector RPL that uses a less trusted privilege than the current privilege level for further use is known as

- a) Least task privilege level
- b) Descriptor privilege level
- c) Effective privilege level
- d) None of the mentioned

Answer: c

Explanation: A selector RPL uses a less trusted privilege than the current privilege level for further use. This is known as the Effective Privilege Level of the task.

7. The effective privilege level is

- a) maximum numeric of RPL and CPL
- b) minimum privilege of RPL and CPL
- c) numeric minimum and privilege maximum of RPL and CPL
- d) none of the mentioned

Answer: c

Explanation: The effective privilege level is minimum in numeric and maximum in the privilege of RPL and CPL.

8. The task requesting an access to a descriptor is allowed to access after checking the

- a) type of descriptor
- b) privilege level
- c) type of descriptor and privilege level
- d) corresponding segment

Answer: c

Explanation: The task requesting an access to a descriptor is allowed to access to it and to the corresponding segment, only after checking the type of the descriptor and privilege level(CPL, RPL, DPL).

9. A CALL instruction can reference only a code segment descriptor with

- a) DPL less privilege than CPL
- b) DPL equal privilege to CPL
- c) DPL greater privilege than CPL
- d) All of the mentioned

Answer: b

Explanation: A CALL or JUMP instruction can reference only a code segment descriptor with DPL equal to CPL of the task or a segment with a DPL of equal or greater privilege than CPL.

10. The RPL of a selector that referred to the code descriptor must have

- a) less privilege than CPL
- b) greater privilege than CPL
- c) equal privilege than CPL
- d) any privilege regarding CPL

Answer: c

Explanation: The RPL of a selector that referred to the code descriptor must have the same privilege as CPL.

11. The instruction that refers to only code segment descriptors with DPL equal to or less than the task CPL is

- a) CALL
- b) IRET
- c) ESC
- d) RET and IRET

Answer: d

Explanation: The RET and IRET instructions are to refer to only code segment descriptors with DPL equal to or less than the task CPL.

12. When a JUMP instruction references a Task State Segment(TSS) descriptor, then DPL must be

- a) equally privileged as CPL
- b) greater or equally privileged than CPL
- c) less or equally privileged than CPL
- d) less privileged than CPL

Answer: c

Explanation: When a CALL or JUMP instruction references a Task State Segment(TSS) descriptor, then DPL must be less or equally privileged than CPL.

13. The data segment access refers to

- a) loading DS
- b) loading ES
- c) loading SS
- d) all of the mentioned

Answer: d

Explanation: Loading DS, ES or SS for referring to a new descriptor comes under the data segment access.

14. An exception is generated when

- a) privilege test is negative
- b) an improper segment is referenced
- c) referenced segment is not present in physical memory
- d) all of the mentioned

Answer: d

Explanation: If the privilege test is negative or an improper segment is referenced then an exception 13 is generated. If the referenced segment is not present in physical memory, an exception 11 is generated.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Protection".

1. The mechanism to provide protection, that is accomplished with the help of read/write privileges is

- a) restricted use of segments
- b) restricted accesses to segments
- c) privileged instructions
- d) privileged operations

Answer: a

Explanation: The restricted use of segments is accomplished with the help of read/write privileges.

2. The Local descriptor table (LDT) and Global descriptor table (GDT) are present in

- a) privileged instruction check
- b) operation reference check
- c) segment load check
- d) none of the mentioned

Answer: c

Explanation: In restricted use of segments i.e. segment load check, the segment usages are restricted by classifying the corresponding descriptors, under LDT and GDT.

3. The mechanism that is accomplished using descriptor usages limitations and rules of privilege check is

- a) privileged instruction check
- b) operation reference check
- c) segment load check
- d) none of the mentioned

Answer: b

Explanation: Restricted accesses to segment, also called, operation reference check, is accomplished using descriptor usages limitations, and rules of privilege check.

4. The mechanism that is executed at certain privilege levels, determined by CPL (Current Privilege Level) and I/O privilege level (IOPL) is

- a) restricted use of segments
- b) restricted accesses to segments
- c) privileged instructions or operations
- d) none of the mentioned

Answer: c

Explanation: The privileged instructions or operations, also called, privileged instruction check, is executed at certain privilege levels, determined by CPL and I/O privilege level (IOPL), as defined by the flag register.

5. If CPL is not of the required privilege level, then the instructions that get affected is

- a) IRET
- b) POPF
- c) IRET and POPF
- d) None of the mentioned

Answer: c

Explanation: The IRET and POPF instructions do not perform any of their functions, if CPL is not of the required privilege level.

6. If CPL is greater than zero, then the instruction that remains unaffected is

- a) IRET
- b) POPF
- c) IF
- d) IRET and POPF

Answer: c

Explanation: IF remains unaffected if CPL is greater than zero. No exception is generated for this condition.

7. The condition, "CPL not equals to zero" satisfies when executing the instruction

- a) LIDT
- b) LGDT
- c) LTR
- d) All of the mentioned

Answer: d

Explanation: The condition, "CPL not equals to zero" satisfies, when executing the instructions, LIDT, LGDT, LTR, LMSW, CTS and HLT.

8. While executing the instruction IN/OUT, the condition of CPL is

- a) $CPL = 0$
- b) $CPL < IOPL$
- c) $CPL > IOPL$
- d) All of the mentioned

Answer: c

Explanation: The condition $CPL > IOPL$ exists, when executing the instructions, INs, IN, OUTS, OUT, STI, CLI and LOCK.

9. The instruction at which the exception is generated, but the processor extension registers contain the address of failing instruction is

- a) LTR
- b) INS
- c) CTS
- d) ESC

Answer: d

Explanation: At the ESC instruction, the exception is generated, but the processor extension registers contain the address of failing instruction.

10. The exception that has no error code on a stack is

- a) double exception detected
- b) processor extension segment overrun
- c) invalid task state segment
- d) stack segment overrun

Answer: b

Explanation: The processor extension segment overrun has no error code on the stack.

11. Which of the following is protected mode exception?

- a) double exception detected
- b) invalid task state segment
- c) stack segment overrun
- d) all of the mentioned

Answer: d

Explanation: Double exception detected, invalid task state segment, stack segment overrun, processor extension segment overrun, are the protected mode exceptions.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessors Interview Questions and Answers for Experienced people focuses on "80286 Minimum System Configuration, Interfacing Memory and I/O Devices With 80286".

1. Which of the following is a supporting chip of 80286?

- a) interrupt controller
- b) clock generator
- c) bus controller
- d) all of the mentioned

Answer: d

Explanation: The interrupt controller 8259A, clock generator 82C284, and bus controller 82C288 are the unavoidable members of the family, of supporting chips of 80286.

2. In minimum mode, the function of 80286 is

- a) data transfers to/from memory or I/O
- b) controls the data transfer of 80287
- c) controls the instruction execution of 80287
- d) all of the mentioned

Answer: d

Explanation: In a minimum mode, the 80286 carries out all the data transfers to/from memory or I/O, controls the data transfer, and instruction execution of 80287.

3. The signal that is applied to the decoding logic, to differentiate between interrupt, code fetch and data bus cycles is

- a) COD
- b) INTA (active low)
- c) M/IO (active low)
- d) All of the mentioned

Answer: d

Explanation: The COD, INTA (active low), M/IO (active low) signals are applied to the decoding logic, to differentiate between interrupt, I/O, code fetch, and data bus cycles.

4. By adding which of the following, the minimum mode of 80286 gives the multibus interface of 80286?

- a) bus controller
- b) bus arbiter
- c) interrupt controller
- d) all of the mentioned

Answer: b

Explanation: The addition of single chip 82C289 known as bus arbiter, to the configuration of 80286 minimum mode, gives the multibus structure of 80286.

5. The number of bus controllers that are used for interfacing of memory and I/O devices is

- a) 1
- b) 2
- c) 3
- d) none of the mentioned

Answer: b

Explanation: The interfacing of memory and I/O devices, uses two 82288 bus controllers, one each for local, and system bus.

6. If the 80286 need to use system bus, then the signal that is to be active is

- a) SRDY
- b) SRDYEN
- c) ARDYEN
- d) ARDY

Answer: c

Explanation: The ARDYEN pin is to be activated if the 80286 is to use the system bus. The SRDYEN pin is to be grounded.

7. If MBYTES input is high, then the pin serves as

- a) AEN
- b) CEN
- c) AEN and CEN
- d) None of the mentioned

Answer: a

Explanation: The MBYTES input selects the function of AEN/CEN pin. If MBYTES is high, the pin serves as AEN, else it serves as CEN. The CEN pin is used for selecting one of the available 82288s.

8. Latches are used in 80286 to

- a) demultiplex the address and data lines
- b) latch the address signals
- c) decode the select signals
- d) latch the address and decode the select signals

Answer: d

Explanation: The address and data lines are not multiplexed, hence no latches are required in 80286 system. Rather the addresses of the next bus cycle are displayed in advance, hence the latches are required for latching the address, and decode the signals.

9. The I/O port addresses, that are not used, while designing practical systems around 80286 are

- a) 0000H to 00FFH
- b) 00FFH to FFFFH
- c) 00F8H to 00FFH
- d) 0000H to FFFFH

Answer: c

Explanation: The I/O port addresses 00F8H to 00FFH are reserved by Intel, hence these should not be used while designing practical systems around 80286.

To practice all areas of Microprocessors for Interviews, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Special Operations".

1. Which of the following operation is not carried out by 80286?

- a) task switch operation
- b) halt
- c) processor reset
- d) none of the mentioned

Answer: d

Explanation: The 80286 carries out six operations. They are:

- 1. processor reset and initialization
- 2. task switch operation
- 3. pointer testing instructions
- 4. protected mode initialization
- 5. how to enter protected mode?
- 6. halt.

2. After completion of the first cycle, the first task is again scheduled for the next cycle. This process is known as

- a) repetition
- b) task switch operation
- c) processor initiation
- d) none of the mentioned

Answer: b

Explanation: After completion of the first cycle, the first task is again scheduled for the next cycle, and the process continues. The previous task that was incomplete, may be completed during its coming turns of the allotted CPU time slice. This switch-over operation from one task to another is called task switch operation.

3. The operation that is provided by the internal architecture, to save the execution state of a task is

- a) processor reset
- b) processor initialization
- c) task switch operation
- d) halt

Answer: c

Explanation: The 80286 internal architecture provides a task switch operation, to save the execution state of a task, and to load a new task to be executed.

4. The instruction that can be used to carry out task switch operation is

- a) software interrupt instruction
- b) exception
- c) external interrupt
- d) all of the mentioned

Answer: d

Explanation: A software interrupt instruction, exception or external interrupt, can also be used to carry out task switch operation.

5. The IRET instruction gets back the execution state of the previous task, if

- a) NT (nested task flag) = 1
- b) NT (nested task flag) = 0
- c) IF (interrupt flag) = 1
- d) IF (interrupt flag) = 0

Answer: a

Explanation: If NT = 1, the IRET instruction gets back the execution state of the previous task. Otherwise, the IRET instruction lets the current task continue, after popping the required values from the stack.

6. The NT flag is set by the task switch operation, that is initiated by

- a) CALL
- b) INT
- c) CALL & INT
- d) None of the mentioned

Answer: c

Explanation: The NT flag is set by CALL or INT initiated task switch operations.

7. The 80286 executes LMSW instruction to enter into

- a) real addressing mode
- b) protected mode
- c) real addressing and protected modes
- d) none of the mentioned

Answer: b

Explanation: To enter into protected mode, 80286 executes LMSW instruction, that sets PE flag.

8. The instruction that sets the zero flag, if the segment referred to, by the selector can be read is

- a) VERW
- b) VERR
- c) LSL
- d) LAR

Answer: b

Explanation: The VERR (VERify to Read) instruction sets the zero flag, if the segment referred to, by the selector, can be read.

9. The instruction that sets the zero flag, if the segment referred to by the selector, can be written as

- a) VERW
- b) APRL
- c) LSL
- d) LAR

Answer: a

Explanation: The VERW (VERify to Write) instruction sets the zero flag, if the segment referred to, by the selector can be written.

10. The instruction that reads the descriptor access rights byte into the register is

- a) VERW
- b) APRL
- c) LSL
- d) LAR

Answer: d

Explanation: The LAR (Load Access Rights) instruction reads the descriptor access rights byte into the register, if privilege rules allow.

11. The instruction that reads the segment limit into the register, if privilege rules and descriptor type allow is

- a) VERW
- b) APRL
- c) LSL
- d) LAR

Answer: c

Explanation: The LSL (Load Segment Limit) instruction reads the segment limit into the register, if privilege rules, and descriptor type allow.

12. The instruction that adjusts the RPL (Requested Privilege Level) of the selector, to the numeric maximum of current selector RPL value is

- a) LAR
- b) VERR
- c) LSL
- d) APRL

Answer: d

Explanation: The APRL (Adjust Requested Privilege Level) adjusts the RPL (Requested Privilege Level) of the selector to the numeric maximum of current selector RPL value, and the RPL value in the register.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessors Quiz focuses on "Instruction Set Features -2".

1. In 'Rotate source, count' instructions, if the CF is equal to MSB of operand (source) then

- a) TF is cleared
- b) OF is cleared
- c) TF is set
- d) OF is set

Answer: b

Explanation: If CF is equal to MSB of operand (source), the overflow flag is cleared, otherwise, it is set to 1.

2. The instruction that affects the flags is

- a) IMUL
- b) INSW
- c) INSB
- d) POP*A

Answer: a

Explanation: No flags are affected by the instructions, INSW, INSB and POP*A.

3. A general protection exception is generated, if the value of

- a) CPL is equal to that of IOPL
- b) CPL is less than that of IOPL
- c) CPL is greater than that of IOPL
- d) None of the mentioned

Answer: c

Explanation: When the value of CPL is greater than that of IOPL, a general protection exception is generated.

4. While executing the instruction, OUTSW, the SI is incremented by

- a) 1
- b) 2
- c) 3
- d) 4

Answer: b

Explanation: The SI is automatically incremented by 1 for byte (OUTSB) and 2 for word (OUTSW) operations.

5. The instruction that is used to exit the procedure is

- a) QUIT
- b) STOP
- c) LEAVE
- d) EXIT

Answer: c

Explanation: The instruction, LEAVE, is generally used with high level languages, to exit a procedure.

6. The instruction that determines the number of bytes, to be copied into the new stack frame, from the previous stack is

- a) ENTER
- b) BOUND
- c) CLTS
- d) LEAVE

Answer: a

Explanation: The ENTER instruction prepares a stack structure for parameters of a procedure to be executed further. This instruction determines the number of bytes to be copied, into the new stack frame, from the previous stack.

7. The instruction that is used to check whether a signed array offset is within the limit, defined for it by the starting and ending index is

- a) ENTER
- b) BOUND
- c) CLTS
- d) LEAVE

Answer: b

Explanation: The BOUND instruction is used to check whether a signed array offset is within the limit defined for it, by the starting and ending index.

8. The CLTS (Clear Task Switch Flag) instruction records every execution of WAIT and ESC and is trapped if the flag(s)

- a) PE (Protection Enable) and TS (task switch) flags are set
- b) Emulate Processor extension flag is set
- c) MP flag and task switched flag is set
- d) PE and MP flag is set

Answer: c

Explanation: The CLTS (Clear Task Switch Flag) instruction records every execution of WAIT and ESC, and is trapped, if the MP flag and task switched flag is set.

9. The instruction that determines whether the segment pointed to, by a 16-bit register, can be accessed from the current privilege level is

- a) RPL
- b) CPL
- c) ARPL
- d) VERR

Answer: d

Explanation: The VERR/VERW instructions determine whether the segment pointed to, by a 16-bit register, can be accessed from the current privilege level.

10. The instruction that loads 6 bytes from a memory block, pointed to by the effective address of the operand, into global descriptor table register is

- a) LLDT
- b) SGDT
- c) LGDT
- d) None of the mentioned

Answer: c

Explanation: The LGDT (load global descriptor table register) loads 6 bytes from a memory block, pointed to by the effective address of the operand, into global descriptor table register.

11. In LGDT instruction, while loading 6 bytes, the first word is loaded into the field of

- a) LIMIT field
- b) BASE field
- c) Either LIMIT or BASE field
- d) None of the mentioned

Answer: a

Explanation: While loading the 6 bytes, the first word is loaded into the LIMIT field of the descriptor table register. The next three bytes are loaded into the BASE field of the register, and the remaining byte is ignored.

To practice all areas of Microprocessors for Quizzes, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Instruction Set Features -1".

1. In which of these modes, the immediate operand is included in the instruction itself?

- a) register operand mode
- b) immediate operand mode
- c) register and immediate operand mode
- d) none of the mentioned

Answer: b

Explanation: In immediate operand mode, the immediate operand is included in the instruction itself.

2. In register address mode, the operand is stored in

- a) 8-bit general purpose register
- b) 16-bit general purpose register
- c) si or di
- d) all of the mentioned

Answer: d

Explanation: In register address mode, the operand is stored either in one of the 8-bit or 16-bit general purpose registers or in SI, DI, BX or BP.

3. In which of the following addressing mode, the offset is obtained by adding displacement and contents of one of the base registers?

- a) direct mode
- b) register mode
- c) based mode
- d) indexed mode

Answer: c

Explanation: In a based mode, the offset is obtained by adding displacement and contents of one of the base registers, either BX or BP.

4. In which of the following addressing mode, the offset is obtained by adding displacement, with the contents of SI?

- a) direct mode
- b) register mode
- c) based mode
- d) indexed mode

Answer: d

Explanation: In an indexed mode, the offset is obtained by adding displacement, with contents of an index register, either SI or DI.

5. The address of a location of the operand is calculated by adding the contents of any of the base registers, with the contents of any of index registers in

- a) based indexed mode with displacement
- b) based indexed mode
- c) based mode
- d) indexed mode

Answer: b

Explanation: In a based indexed mode, the operand is stored at a location, whose address is calculated by adding the contents of any of the base registers, with the contents of any of the index registers.

6. Which of the following is not a data type of 80286?

- a) Ordinal or unsigned
- b) ASCII
- c) Packed BCD
- d) None of the mentioned

Answer: d

Explanation: The 80286 supports seven data types. They are

- 1. integer
- 2. Ordinal (unsigned)
- 3. pointer
- 4. string
- 5. ASCII
- 6. BCD
- 7. Packed BCD.

7. The representation of 8-bit or 16-bit signed binary operands using 2's complement is a data type of

- a) Ordinal
- b) ASCII
- c) Packed BCD
- d) integer

Answer: d

Explanation: In integer data type, 8-bit or 16-bit signed binary operands are represented using 2's complement.

8. The instruction that pushes the general purpose registers, pointer and index registers on to the stack is

- a) POPF
- b) PUSH Imd
- c) PUSH*A
- d) PUSHF

Answer: c

Explanation: The PUSH*A instruction, pushes the general purpose registers, AX, CX, DX and BX, pointer and index registers, SP, BP, SI, DI, on to the stack.

9. While executing the PUSH*A instruction, the stack pointer is decremented by

- a) 1 bit
- b) 2 bits
- c) 4 bits
- d) 16 bits

Answer: b

Explanation: The stack pointer is decremented by 16 (eight 2-byte registers).

10. The statement that is true for the instruction POP*A is

- a) flags are unaffected
- b) no operands are required
- c) exceptions generated are same as that of PUSH*A
- d) all of the mentioned

Answer: d

Explanation: The POP*A instruction, pops all the contents of the registers DI, SI, BP, SP, BX, DX, CX and AX from the stack in this sequence, that is exactly opposite to that of pushing.

11. The instruction that multiplies the content of AL with a signed immediate operand is

- a) MUL
- b) SMUL
- c) IMUL
- d) None of the mentioned

Answer: c

Explanation: The IMUL instruction multiplies the content of AL with a signed immediate operand, and the signed 16-bit result is stored in AX.

12. The instruction that represents the 'rotate source, count' is

- a) RCL
- b) RCR
- c) ROR
- d) All of the mentioned

Answer: d

Explanation: The rotate source, count is a group of four instructions containing RCL, RCR, ROL, ROR.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessors test focuses on "Priority of Bus Use By 80286, Bus Hold and HLDA Sequence, Interrupt Acknowledge Sequence".

1. Which of the following is the highest priority usage among them?

- a) second transfer cycle of a processor extension data transfer
- b) third transfer cycle of a processor extension data transfer
- c) hold request
- d) second byte transfer of 2-byte transfer at an odd address

Answer: d

Explanation: The second byte transfer of 2-byte transfer at an odd address, is the highest priority usage among the given usages.

2. The highest priority usage than any other usage is

- a) transfer with LOCK (active low) signal
- b) hold request
- c) processor extension data transfer
- d) data transfer performed by EU (execution unit)

Answer: a

Explanation: The transfer with LOCK (active low) signal is the highest priority usage than any other usage.

3. The lowest priority usage among the following is

- a) hold request
- b) processor extension data transfer
- c) prefetch operation to fetch and arrange next instruction bytes in queue
- d) data transfer performed by EU for instruction execution

Answer: c

Explanation: The order of priority usages, starting from the highest one to the lowest one, is given as

- 1. transfer with LOCK (active low) signal
- 2. second byte transfer of 2-byte transfer at an odd address
- 3. second or third transfer cycle of a processor extension data transfer
- 4. HOLD request
- 5. processor extension data transfer
- 6. data transfer performed by EU (execution unit)
- 7. prefetch operation to fetch and arrange next instruction bytes in queue.

4. As a response to the valid bus hold request, the bus is pushed into

- a) TH (hold) state
- b) Ts (status) state
- c) Tc (command) state
- d) Ti (idle) state

Answer: a

Explanation: 80286 local bus is relinquished for another bus master if a valid bus hold request

is received at the HOLD input pin. As a response to a valid bus hold request, the bus is pushed into TH state.

5. The bus arbiter relinquishes

- a) Address
- b) M/IO (active low)
- c) COD/INTA (active low)
- d) All of the mentioned

Answer: d

Explanation: The address, M/IO (active low) and COD/INTA (active low) are relinquished by bus arbiter.

6. A valid HOLD request is ascertained only after the completion of

- a) 34 clockcycles
- b) 24 clockcycles and 80286 is SET
- c) 34 clockcycles and 80286 is SET
- d) 34 clockcycles and 80286 is RESET

Answer: d

Explanation: Only after 34 clockcycles, after the 80286 is reset, a valid HOLD request should be ascertained.

7. The master PIC 8259A decides which of its slave interrupt controllers is to return the vector address, as a response of

- a) first INTA (active low) pulse from 80286
- b) second INTA (active low) pulse from 80286
- c) third INTA (active low) pulse from 80286
- d) none of the mentioned

Answer: a

Explanation: In response to the first INTA (active low) pulse from 80286, the master PIC 8259A decides, which of its slave interrupt controllers is to return the vector address.

8. The slave (which is selected) sends the vector on data bus after the

- a) first INTA (active low) pulse from 80286
- b) second INTA (active low) pulse from 80286
- c) third INTA (active low) pulse from 80286
- d) none of the mentioned

Answer: b

Explanation: The interrupt acknowledge sequence consists of two INTA (active low) pulses. After the second pulse, the selected slave sends the vector on D0-D7 data lines, and 80286 reads it.

9. The signal of 82C288, that enables the cascade address drivers, during INTA cycles is

- a) DEN
- b) DT/R (active low)
- c) MCE
- d) MB

Answer: c

Explanation: The MCE (Master Cascade Enable) signal of 82C288 enables the cascade address drivers during INTA cycles, to select the slave using the local address bus.

10. The LOCK (active low) signal is activated during

- a) Ti of first INTA cycle
- b) Ts of first INTA cycle
- c) Th of second INTA cycle
- d) Ts of second INTA cycle

Answer: b

Explanation: The LOCK (active low) signal is activated during Ts of first INTA cycle.

11. The number of idle states (Ti), that is allowed between two INTA cycles, to meet the 8259A speed and cascade address output delay is

- a) 1
- b) 2
- c) 3
- d) 4

Answer: c

Explanation: The 80286 allows three idle states (Ti) between the two INTA cycles, to meet the 8259A speed and cascade address output delay.

To practice all areas of Microprocessors for tests, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessors MCQs focuses on “80287 Math Coprocessor -2”.

1. If the stack flag is set, and condition code bit C1=1, then the stack is

- a) full
- b) overflown
- c) underflown
- d) empty

Answer: b

Explanation: If the stack flag is set, and condition code bit C1=1, then the stack has overflown.

2. If the stack flag is set, and condition code bit C1=0, then the stack is

- a) full
- b) overflown
- c) underflown
- d) empty

Answer: c

Explanation: If the stack flag is set, and condition code bit C1=0, then the stack has underflown.

3. The bits that affect the result of arithmetic operations like ADD, SUB, MUL, DIV are

- a) condition code bits
- b) rounding control bits
- c) masking bits
- d) precision control bits

Answer: d

Explanation: The precision control bits affect ADD, SUB, MUL, DIV and SQRT results.

4. The precision is decided by the

- a) opcode
- b) extended precision format
- c) opcode or extended precision format
- d) none of the mentioned

Answer: c

Explanation: For other than the arithmetic instructions (like ADD, SUB, MUL, DIV and SQRT), the precision is decided by opcode or extended precision format.

5. If Numeric Processor Write (NPWR) active-low input pin is activated, then it enables a data transfer from

- a) memory to processor
- b) 80287 to 80286
- c) 80286 to 80287
- d) 8086 to 80287

Answer: c

Explanation: If Numeric Processor Write (NPWR) active-low input pin is activated, then it enables a data transfer from 80286 to 80287.

6. If Numeric Processor Read (NPRD) active-low input pin is activated, then it enables a data transfer from

- a) memory to processor
- b) 80287 to 80286

- c) 80286 to 80287
- d) 8086 to 80287

Answer: b

Explanation: If Numeric Processor Read (NPRD) active-low input pin is activated, then it enables a data transfer from 80287 to 80286.

7. Which of the input line(s) indicate that the CPU is performing an escape operation, and enables 80287 to execute the next instruction?

- a) NPWR (active low) and NPRD (active low)
- b) NPS1 and NPS2 (active low)
- c) NPS1 (active low) and NPS2
- d) CMD0 and CMD1

Answer: c

Explanation: The Numeric Processor select input lines, NPS1 (active low) and NPS2, indicate that the CPU is performing an escape operation, and enables 80287 to execute the next instruction.

8. For which pin of 80286 is the active low pin, BUSY of 80287, connected?

- a) ERROR (active low)
- b) BUSY (active low)
- c) HLDA
- d) TEST (active low)

Answer: d

Explanation: The BUSY (active low) is connected to the TEST (active low) pin of 80286.

9. If Clock Mode (CM) input pin is held low, then the CLK input is divided by

- a) 1
- b) 2
- c) 3
- d) 4

Answer: b

Explanation: If Clock Mode (CM) input pin is held high, then the CLK input is directly used for deriving the internal timings. Else, it is divided by 2.

10. Which of the following pin is not involved in the interface of 80287 with 80286?

- a) PEREQ
- b) ERROR#
- c) RESET
- d) CMD0 and CMD1

Answer: c

Explanation: The 10 pins, PEREQ, PEACK#, BUSY#, ERROR#, NPRD(active low)#, NPWR(active low)#, NPS1(active low)#, NPS2#, CMD0 and CMD1.

11. The PEACK (active low) when activated, the pin that goes into deactivation is

- a) PEREQ
- b) ERROR#
- c) RESET
- d) CMD0 and CMD1

Answer: a

Explanation: When the data transfer is over, the CPU activates PEACK (active low)# pin, which results in deactivating the PEREQ pin by 80287.

To practice MCQs on all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "80287 Math Coprocessor -1".

1. Which of the following is not a block of an architecture of 80287?

- a) bus control logic
- b) data interface and control unit

- c) floating point unit
- d) none of the mentioned

Answer: d

Explanation: The three blocks of an internal architecture of 80287 are:

1. bus control logic
2. data interface and control unit
3. floating point unit.

2. The unit that provides and controls the interface, between the internal 80287 bus and 80286 bus via data buffer is

- a) bus control logic
- b) data interface and control unit
- c) floating point unit
- d) none of the mentioned

Answer: a

Explanation: The bus control logic provides and controls the interface, between the internal 80287 bus and 80286 bus via data buffer.

3. The data interface and control unit consists of

- a) status and control words
- b) tag words and error pointers
- c) instruction decoders
- d) all of the mentioned

Answer: d

Explanation: The data interface and control unit contains status and controls words, TAG words and error pointers.

4. The word that optimizes the NDP performance, by maintaining a record of empty and non-empty register locations is

- a) Status and control words
- b) TAG words
- c) Error pointers
- d) All of the mentioned

Answer: b

Explanation: The TAG word optimizes the NDP performance by maintaining a record of empty and non-empty register locations. It helps the exception handler to identify special values in the contents of the stack locations.

5. The part of the data interface and control unit, that points to the source of exception generated is

- a) Status and control words
- b) TAG words
- c) Error pointers
- d) None of the mentioned

Answer: c

Explanation: The error pointers point to the source of exception (address of the instruction that generated the exception) generated.

6. The data bus in a floating point unit is of

- a) 16 bits
- b) 32 bits
- c) 64 bits
- d) 84 bits

Answer: d

Explanation: The data bus in a floating point unit is of 84-bits. Out of this 84-bits, the lower 68 bits are significant (mantissa) data bit, the next 16 bits are used for the exponent.

7. The arrangement of data that is to be shifted successively, whenever required for the execution, is done by

- a) error pointer
- b) data buffer
- c) barrel shifter
- d) none of the mentioned

Answer: c

Explanation: The barrel shifter arranges and presents the data to be shifted successively, whenever required for the execution.

8. The word that is used to select one of the processing options, among the provided ones is
- a) status word
 - b) control word
 - c) status and control words
 - d) none of the mentioned

Answer: b

Explanation: The control word is used to select one of the processing options, among the ones provided by 80287.

9. After reset of 80287, the control bit that is initialized to zero is
- a) masking bits
 - b) precision control bits
 - c) rounding control bits
 - d) infinity control bits

Answer: d

Explanation: The infinity control bit is initialized to zero after reset.

10. The bits that are modified depending upon the result of the execution of arithmetic instructions are
- a) masking bits
 - b) rounding control bits
 - c) condition code bits
 - d) error summary bits

Answer: c

Explanation: The condition code bits are similar to the flags of a CPU. These are modified depending upon the result of the execution of arithmetic instructions.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Architecture and Signal Descriptions of 80386".

1. Which of the units is not a part of the internal architecture of 80386?
- a) central processing unit
 - b) memory management unit
 - c) bus interface unit
 - d) none of the mentioned

Answer: d

Explanation: The internal architecture of 80386 is divided into three sections namely, central processing unit, memory management unit and bus interface unit.

2. The central processing unit has a sub-division of
- a) memory unit and control unit
 - b) memory unit and ALU
 - c) execution unit and instruction unit
 - d) execution unit and memory unit

Answer: c

Explanation: The central processing unit is further divided into the execution unit and instruction unit.

3. The unit that is used for handling data, and calculates offset address is
- a) memory management unit

- b) execution unit
- c) instruction unit
- d) bus interface unit

Answer: b

Explanation: The execution unit has eight general purpose and eight special purpose registers, which are either used for handling the data or calculating the offset addresses.

4. The unit that decodes the opcode bytes, received from the 16-byte instruction code queue is
- a) memory management unit
 - b) execution unit
 - c) instruction unit
 - d) barrel shifter

Answer: c

Explanation: The instruction unit decodes the opcode bytes, received from the 16-byte instruction code queue, after decoding them so as to pass it to the control section, for deriving the necessary control signals.

5. The unit that increases the speed of all shift and rotate operations is
- a) memory management unit
 - b) execution unit
 - c) instruction unit
 - d) barrel shifter

Answer: d

Explanation: The barrel shifter speeds up all shift and rotate operations.

6. The memory management unit consists of
- a) segmentation unit
 - b) paging unit
 - c) segmentation and paging units
 - d) none of the mentioned

Answer: c

Explanation: The memory management unit consists of a segmentation unit and a paging unit.

7. The segmentation unit allows
- a) maximum size of 4GB segments
 - b) use of segment address components
 - c) use of offset address components
 - d) all of the mentioned

Answer: d

Explanation: The segmentation unit allows the use of two address components. They are: segment and offset for relocation and sharing of code and data.

8. The unit that organizes the physical memory, in terms of pages of 4KB size each is
- a) segmentation unit
 - b) execution unit
 - c) paging unit
 - d) instruction unit

Answer: c

Explanation: The paging unit organizes the physical memory, in terms of pages of 4KB size each.

9. The paging unit works under the control of
- a) memory management unit
 - b) segmentation unit
 - c) execution unit
 - d) instruction unit

Answer: b

Explanation: The paging unit works under the control of the segmentation unit; i.e. each segment is further divided into pages.

10. The unit that provides a four level protection mechanism, for system's code and data against application program is

- a) central processing unit
- b) segmentation unit
- c) bus interface unit
- d) none of the mentioned

Answer: b

Explanation: The segmentation unit provides a four level protection mechanism, for protecting and isolating the system's code and data, from those of the application program.

11. The unit that has a prioritizer to resolve the priority of the various bus requests is

- a) bus sizing unit
- b) data buffer
- c) bus control unit
- d) execution unit

Answer: c

Explanation: The bus control unit has a prioritizer to resolve the priority of the various bus requests.

12. The unit that interfaces the internal data bus with the system bus is

- a) bus sizing unit
- b) data buffer
- c) bus control unit
- d) execution unit

Answer: b

Explanation: The data buffer interfaces the internal data bus with the system bus.

13. The unit that drives the bus enable and address signals A0-A31 is

- a) bus sizing unit
- b) bus driving unit
- c) address driver
- d) bus driver

Answer: c

Explanation: The address driver drives the bus enable and address signals A0-A31.

14. Which of the following pin when activated, allows address pipelining?

- a) ADS
- b) NA
- c) AP
- d) None of the mentioned

Answer: b

Explanation: The Next Address (NA) input pin, if activated, allows address pipelining, during 80386 bus cycles.

15. The signal that is used to insert WAIT states in a bus cycle in 80386 is

- a) HOLD
- b) HLDA
- c) READY
- d) PEREQ

Answer: c

Explanation: READY signal is used to insert WAIT states in a bus cycle, and is useful for interfacing of slow devices with the CPU.

16. The signal which indicates to the CPU, to fetch a data word for the coprocessor is

- a) READY
- b) NMI
- c) HLDA
- d) PEREQ

Answer: d

Explanation: The Processor Extension Request (PEREQ) output signal indicates to the CPU to fetch a data word for the coprocessor.

17. The pipeline and dynamic bus sizing units handle

- a) data signals
- b) address signals
- c) control signals
- d) all of the mentioned

Answer: c

Explanation: The pipeline and dynamic bus sizing units handle the related control signals.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on “Salient Features of 80386DX”.

1. The 80386DX is a processor that supports

- a) 8-bit data operand
- b) 16-bit data operand
- c) 32-bit data operand
- d) all of the mentioned

Answer: d

Explanation: The 80386DX is a 32-bit processor that supports, 8-bit/16-bit/32-bit data operands.

2. The 80386DX has an address bus of

- a) 8 address lines
- b) 16 address lines
- c) 32 address lines
- d) 64 address lines

Answer: c

Explanation: The 80386, with its 32-bit address bus, can address up to 4 GB of physical memory.

3. The number of debug registers that are available in 80386, for hardware debugging and control is

- a) 2
- b) 4
- c) 8
- d) 16

Answer: c

Explanation: The 80386 offers a set of total eight debug registers DR0-DR7, for hardware debugging and control.

4. The memory management of 80386 supports

- a) virtual memory
- b) paging
- c) four levels of protection
- d) all of the mentioned

Answer: d

Explanation: The memory management section of 80386 supports the virtual memory, paging and four levels of protection, maintaining full compatibility with 80286.

5. The 80386 enables itself to organize the available physical memory into pages, which is known as

- a) segmentation
- b) paging
- c) memory division
- d) none of the mentioned

Answer: b

Explanation: The concept of paging which is introduced in 80386, enables it to organize the available physical memory into pages of size 4 KB each, under the segmented memory.

6. The 80386 consists of

- a) on-chip address translation cache
- b) instruction set of predecessors with upward compatibility
- c) virtual memory space of 64TB
- d) all of the mentioned

Answer: d

Explanation: The 80386 has on-chip address translation cache, and the instruction set is upward compatible with all its predecessors.

7. 80386DX is available in a grid array package of

- a) 64 pin
- b) 128 pin
- c) 132 pin
- d) 142 pin

Answer: c

Explanation: The 80386DX is available in a 132-pin grid array package.

8. The operating frequency of 80386DX is

- a) 12 MHz and 20 MHz
- b) 20 MHz and 33 MHz
- c) 32 MHz and 12 MHz
- d) all of the mentioned

Answer: b

Explanation: The operating frequency of 80386DX is 20MHz and 33 MHz.

9. The 80386 in its protected mode, in its virtual mode of operation, can run the applications of

- a) 8086
- b) 80286
- c) 80287
- d) 80387

Answer: a

Explanation: The 80386 can run the applications under protected mode, in its virtual 8086 mode of operation.

10. The 80386 in protected mode, supports all software written for

- a) 8086 and 80287
- b) 80286 and 80287
- c) 80287 and 80387
- d) 80286 and 8086

Answer: d

Explanation: The 80386 in protected mode, supports all software written for 8086 and 80286 (to be executed under the control of memory management and protection abilities of 80386). To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Register Organisation of 80386 -1".

1. The 16-bit registers are available with their extended size of 32 bits, by adding the registers with a prefix of

- a) X
- b) E
- c) 32
- d) XX

Answer: b

Explanation: A 32 bit register, known as an extended register, is represented by the register name with a prefix of E.

2. In a 32-bit register, ESP, the lower 16-bits of the register can be represented by

- a) LSP
- b) FSP
- c) SP
- d) None of the mentioned

Answer: c

Explanation: Though the extended size of 32 bits are named as EBP, ESP, ESI and EDI, the names BP, SP, SI and DI represent the lower 16-bits.

3. Which of the following is a data segment register of 80386?

- a) ES
- b) FS
- c) GS
- d) All of the mentioned

Answer: d

Explanation: The six segment registers available in 80386 are CS, SS, DS, ES, FS and GS, out of which DS, ES, FS and GS are the four data segment registers.

4. The register width used by the 32-bit addressing modes is

- a) 8 bits
- b) 16 bits
- c) 32 bits
- d) all of the mentioned

Answer: d

Explanation: The 32-bit addressing modes may use all the register widths, i.e. 8, 16 or 32 bits.

5. The flag that is additional in flag register of 80386, compared to that of 80286 is

- a) VM flag
- b) RF flag
- c) VM and RF flag
- d) None of the mentioned

Answer: c

Explanation: The VM and RF flags are added to the 80286 flag register, to derive the flag register of 80386.

6. The VM (virtual mode) flag is to be set, only when 80386 is in

- a) virtual mode
- b) protected mode
- c) either virtual or protected mode
- d) all of the mentioned

Answer: b

Explanation: If VM flag is set, the 80386 enters the virtual 8086 mode within the protected mode. This is to be set only when the 80386 is in protected mode.

7. In protected mode of 80386, the VM flag is set by using

- a) IRET instruction
- b) Task switch operation
- c) IRET instruction or task switch operation
- d) None of the mentioned

Answer: c

Explanation: The VM flag can be set using the IRET instruction or any task switch operation, only in the protected mode.

8. During the instruction cycle of 80386, any debug fault can be ignored if

- a) VM flag is set
- b) VM flag is cleared

- c) RF is cleared
- d) RF is set

Answer: d

Explanation: If RF (resume flag) is set, any debug fault is ignored during the instruction cycle.

9. The RF is not automatically reset after the execution of

- a) IRET
- b) POPA
- c) IRET and POPF
- d) IRET and PUSHF

Answer: c

Explanation: The RF is automatically reset after the execution of every instruction, except for the IRET and POPF instructions. Also, it is not cleared automatically after the successful execution of JMP, CALL and INT instructions causing a task switch.

10. The segment descriptor register is used to store

- a) attributes
- b) limit address of segments
- c) base address of segments
- d) all of the mentioned

Answer: d

Explanation: The segment descriptor register is used to store the descriptor information like attributes, limit and base addresses of segments.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Addressing Modes of 80386, Data Types of 80386".

1. Which of the following is not a scale factor of addressing modes of 80386?

- a) 2
- b) 4
- c) 6
- d) 8

Answer: c

Explanation: In case of the scaled the modes, any of the index register values can be multiplied by a valid scale factor to obtain the displacement. The valid scale factors are 1, 2, 4 and 8.

2. Contents of an index register are multiplied by a scale factor that may be added further to get the operand offset in

- a) base scaled indexed mode
- b) scaled indexed mode
- c) indexed mode
- d) none of the mentioned

Answer: b

Explanation: In scaled indexed mode, contents of an index register are multiplied by a scale factor that may be added further to get the operand offset.

3. Contents of an index register are multiplied by a scale factor and then added to base register to get the operand offset in

- a) base scaled indexed mode
- b) scaled indexed mode
- c) indexed mode
- d) none of the mentioned

Answer: a

Explanation: In base scaled indexed mode, contents of an index register are multiplied by a scale factor and then added to base register to get the operand offset.

4. In the based scaled indexed mode with displacement mode, the contents of an index register are multiplied by a scale factor and are added to

- a) base register
- b) displacement
- c) base register and displacement
- d) none of the mentioned

Answer: c

Explanation: Contents of an index register are multiplied by a scale factor and the result is added to a base register and a displacement to get the offset of an operand.

5. The following statement of ALP is an example of
MOV EBX, [EDX*4] [ECX].

- a) base scaled indexed mode
- b) scaled indexed mode
- c) indexed mode
- d) based scaled indexed mode with displacement mode

Answer: a

Explanation: Since in base scaled indexed mode, contents of an index register are multiplied by a scale factor and then added to base register to get the operand offset.

6. The following statement is an example of
MOV EBX, LIST [ESI*2].
MUL ECX, LIST [EBP*4].

- a) base scaled indexed mode
- b) scaled indexed mode
- c) indexed mode
- d) based scaled indexed mode with displacement mode

Answer: b

Explanation: Since in scaled indexed mode, contents of an index register are multiplied by a scale factor that may be added further to get the operand offset.

7. Bit field can be defined as a group of

- a) 8 bits
- b) 16 bits
- c) 32 bits
- d) 64 bits

Answer: c

Explanation: A group of at the most 32 bits(4 bytes) is defined as a bit field.

8. The maximum length of the string in a bit string of contiguous bits is

- a) 2 MB
- b) 4 MB
- c) 2 GB
- d) 4 GB

Answer: d

Explanation: Bit string is a string of contiguous bits of maximum 4Gbytes in length.

9. The integer word is defined as

- a) signed 8-bit data
- b) unsigned 16-bit data
- c) signed 16-bit data
- d) signed 32-bit data

Answer: c

Explanation: The integer word is the signed 16-bit data.

10. A 16-bit displacement that references a memory location using any of the addressing modes is

- a) Pointer
- b) Character
- c) BCD
- d) Offset

Answer: d

Explanation: Offset is a 16-bit or 32-bit displacement that references a memory location using any of the addressing modes.

11. A decimal digit can be represented by

- a) unsigned integer
- b) signed integer
- c) unpacked BCD
- d) packed BCD

Answer: c

Explanation: Decimal digits from 0-9 are represented by unpacked bytes.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessors Multiple Choice Questions & Answers focuses on "Register Organisation of 80386 -2".

1. The 32-bit control register, that is used to hold global machine status, independent of the executed task is

- a) CR0
- b) CR2
- c) CR3
- d) All of the mentioned

Answer: d

Explanation: The 80386 has three 32-bit control registers CR0, CR2 and CR3, to hold global machine status, independent of the executed task.

2. The descriptor table that the 80386 supports is

- a) GDT (Global descriptor table)
- b) IDT (Interrupt descriptor table)
- c) LDT (Local descriptor table)
- d) All of the mentioned

Answer: d

Explanation: The 80386 supports four types of descriptor tables. They are, GDT, IDT, LDT and TSS.

3. The registers that are together, known as system address registers are

- a) GDTR and IDTR
- b) IDTR and LDTR
- c) TR and GDTR
- d) LDTR and TR

Answer: a

Explanation: The GDTR and IDTR are known as system address registers.

4. Which of the following is a system segment register?

- a) GDTR
- b) LDTR
- c) IDTR
- d) None of the mentioned

Answer: b

Explanation: The LDTR and TR are known as system segment registers.

5. The test register(s) that is provided by 80386 for page caching is

- a) test control registers
- b) page cache registers
- c) test control and test status registers
- d) test control and page cache registers

Answer: c

Explanation: Two test registers are provided by 80386 for page caching, namely test control and test status registers.

6. Among eight debug registers, DR0-DR7, the registers that are reserved by Intel are
- a) DR0, DR1, DR2
 - b) DR4, DR5
 - c) DR1, DR4
 - d) DR5, DR6, DR7

Answer: b

Explanation: Out of the eight debug registers, the two registers DR4 and DR5 are Intel reserved.

7. The registers that are used to store four program controllable break point addresses are
- a) DR5-DR7
 - b) DR0-DR1
 - c) DR6-DR7
 - d) DR0-DR3

Answer: d

Explanation: The initial four registers, DR0-DR3 store four program controllable break point addresses.

8. The register DR6 hold
- a) break point status
 - b) break point control information
 - c) break point status and break point control information
 - d) none of the mentioned

Answer: a

Explanation: The registers DR6 and DR7 respectively hold break point status and break point control information.

9. The flag bits that indicate the privilege level of current IO operations are
- a) Virtual mode flag bits
 - b) IOPL flag bits
 - c) Resume flag bits
 - d) None of the mentioned

Answer: b

Explanation: The IOPL flag bits indicate the privilege level of current IO operations.

10. The registers that are not available for programmers are
- a) data and address registers
 - b) instruction pointers
 - c) segment descriptor registers
 - d) flag registers

Answer: c

Explanation: The segment descriptor registers of 80386 are not available for programmers, rather, they are internally used to store the descriptor information.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on “Real Address Mode of 80386, Protected Mode of 80386”.

1. The instructions available in the 80386 that are not available in its real address mode is
- a) addressing techniques
 - b) instructions for protected address mode
 - c) instructions for interrupt handling
 - d) all of the mentioned

Answer: b

Explanation: All the instructions of 80386 are available in this mode except for those designed to work with or for protected address mode.

2. The unit that is disabled in real address mode is
- a) central processing unit

- b) memory management unit
- c) paging unit
- d) bus control unit

Answer: c

Explanation: The paging unit is disabled in real address mode.

3. To form a physical memory address, appropriate segment register contents are
- a) shifted by left by 4 positions
 - b) added to 16-bit offset address
 - c) operated using one of addressing modes
 - d) all of the mentioned

Answer: d

Explanation: To form a physical memory address, appropriate segment register contents are shifted by left by 4 positions and then added to 16-bit offset address formed using one of addressing modes, in same way as in the 80386 real address mode.

4. The segments in 80386 real mode are
- a) overlapped
 - b) non-overlapped
 - c) either overlapped or non-overlapped
 - d) none of the mentioned

Answer: c

Explanation: The segments in 80386 real mode are may be overlapped or non-overlapped.

5. The operation that can be performed on segments in 80386 real mode is
- a) read
 - b) write
 - c) execute
 - d) all of the mentioned

Answer: d

Explanation: The segments in 80386 real mode can be read, written or executed, i.e. no protection is available.

6. The selectors contain the segment's
- a) segment limit
 - b) base address
 - c) access rights byte
 - d) all of the mentioned

Answer: d

Explanation: In protected mode, the contents of segment registers are used as selectors to address descriptors which contain the segment limit, base address and access rights byte of the segment.

7. The linear address is calculated by
- a) effective address + segment base address
 - b) effective address - segment base address
 - c) effective address + physical address
 - d) effective address - physical address

Answer: a

Explanation: The effective address(offset) is added with segment base address to calculate linear address.

8. If the paging unit is enabled, then it converts a linear address into
- a) effective address
 - b) physical address
 - c) segment base address
 - d) none of the mentioned

Answer: b

Explanation: The paging unit when enabled, it converts a linear address into physical address.

9. If the paging unit is disabled, then the linear address is used as
- a) effective address
 - b) physical address
 - c) segment base address
 - d) none of the mentioned

Answer: b

Explanation: The linear address is used as a physical address if the paging unit is disabled.

10. The paging unit is enabled only in
- a) virtual mode
 - b) addressing mode
 - c) protected mode
 - d) none of the mentioned

Answer: c

Explanation: The paging unit is enabled only in protected mode.

11. For a single task in protected mode, the 80386 can address the virtual memory of
- a) 32 GB
 - b) 64 MB
 - c) 32 TB
 - d) 64 TB

Answer: d

Explanation: In protected mode, the 80386 can address 4 GB of physical memory and 64 TB of virtual memory per task.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Segmentation".

1. The bit that indicates whether the segment has been accessed by the CPU or not is
- a) base address
 - b) attribute bit
 - c) present bit
 - d) granular bit

Answer: b

Explanation: The accessed bit or attribute bit (A) indicates whether the segment has been accessed by the CPU or not.

2. The TYPE field of a descriptor is used to find the
- a) descriptor type
 - b) segment type
 - c) descriptor and segment type
 - d) none

Answer: c

Explanation: The type field decides the descriptor type and hence the segment type.

3. If the segment descriptor bit, S=0, then the descriptor is
- a) data segment descriptor
 - b) code segment descriptor
 - c) system descriptor
 - d) all of the mentioned

Answer: c

Explanation: If S=0, then system descriptor. If S=1, then code or data segment descriptor.

4. The bit that indicates whether the segment is page addressable is
- a) base address
 - b) attribute bit
 - c) present bit
 - d) granularity bit

Answer: d

Explanation: The granularity bit indicates whether the segment is page addressable.

5. If the Default operation size bit, D=1, the code segment operation size selected is

- a) 8-bit
- b) 16-bit
- c) 32-bit
- d) 64-bit

Answer: c

Explanation: If D=1, the segment selected is 32-bit operand segment, else, it is a 16-bit operand segment.

6. The segment descriptor contains

- a) access rights
- b) limit
- c) base address
- d) all of the mentioned

Answer: d

Explanation: The segment descriptors are 8-byte quantities containing access right or attribute bits along with the base and limit of the segments.

7. Which of the following is not a type of segment descriptor?

- a) system descriptors
- b) local descriptors
- c) gate descriptors
- d) none

Answer: d

Explanation: The five types of segment descriptors of 80386 are:

- 1. Code or data segment descriptors
- 2. System descriptors
- 3. Local descriptors
- 4. TSS(task state segment) descriptors
- 5. Gate descriptors.

8. The limit field of the descriptor is of

- a) 10 bits
- b) 8 bits
- c) 16 bits
- d) 20 bits

Answer: d

Explanation: The limit field of the descriptor is of 20 bits.

9. The starting address of the segment in physical memory is decided by

- a) physical memory
- b) segment descriptors
- c) operating system
- d) base address

Answer: c

Explanation: The base address that marks the starting address of the segment in physical memory is decided by the operating system and is of 32 bits.

10. The total descriptors that the 80386 can handle is

- a) 2K
- b) 8K
- c) 4K
- d) 16K

Answer: d

Explanation: 80386 can handle total 16K descriptors and hence segments.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Paging".

1. The advantage of pages in paging is
- a) no logical relation with program
 - b) no need of entire segment of task in physical memory
 - c) reduction of memory requirement for task
 - d) all of the mentioned

Answer: d

Explanation: The advantage of paging scheme is that the complete segment of a task need not be in the physical memory at any time. Only a few pages of the segments, which are required currently for the execution, need to be available in the physical memory.

2. The size of the pages in the paging scheme is
- a) variable
 - b) fixed
 - c) both variable and fixed
 - d) none

Answer: b

Explanation: The paging divides the memory into fixed size pages.

3. To convert linear addresses into physical addresses, the mechanism that the paging unit uses is
- a) linear conversion mechanism
 - b) one level table mechanism
 - c) physical conversion mechanism
 - d) two level table mechanism

Answer: d

Explanation: The paging unit of 80386 uses a two level table mechanism, to convert the linear addresses provided by the segmentation unit, into physical addresses.

4. The control register that stores the 32-bit linear address, at which the previous page fault is detected is
- a) CR0
 - b) CR1
 - c) CR2
 - d) CR3

Answer: c

Explanation: The control register, CR2, is used to store the 32-bit linear address, at which the previous page fault is detected.

5. Which of the following is not a component of paging unit?
- a) page directory
 - b) page descriptor base register
 - c) page table
 - d) page

Answer: b

Explanation: The paging unit handles every task in terms of three components namely page directory, page table and the page itself.

6. The control register that is used as page directory physical base address register is
- a) CR0
 - b) CR1
 - c) CR2
 - d) CR3

Answer: d

Explanation: The control register, CR3, is used as page directory physical base address register, to store the physical starting address of the page directory.

7. The bits of CR3, that are always zero are

- a) higher 4 bits
- b) lower 8 bits
- c) higher 10 bits
- d) lower 12 bits

Answer: d

Explanation: The lower 12 bits of CR3 are always zero to ensure the page size aligned with the directory.

8. Each directory entry in page directory is maximum of

- a) 2 bytes
- b) 4 bytes
- c) 8 bytes
- d) 16 bytes

Answer: b

Explanation: Each directory entry is of 4 bytes, thus a total of 1024 entries are allowed in a directory.

9. The size of each page table is of

- a) 2 Kbytes
- b) 2 bytes
- c) 4 Kbytes
- d) 4 bytes

Answer: c

Explanation: Each page table is of 4 Kbytes in size, and may contain a maximum of 1024 entries.

10. The dirty bit(D) is set, before which operation is carried out

- a) write
- b) read
- c) initialization
- d) none of the mentioned

Answer: a

Explanation: The dirty bit (D) is set before a write operation to the page is carried out.

11. The bit that is undefined for page directory entries is

- a) P-bit
- b) A-bit
- c) D-bit
- d) All of the mentioned

Answer: c

Explanation: The D-bit is undefined for page directory entries.

12. The bit that is used for providing protection is

- a) User/Supervisor bit
- b) Read bit
- c) Write bit
- d) all of the mentioned

Answer: d

Explanation: The User/Supervisor (U/S) bit and Read/Write (R/W) bit are used to provide protection.

13. The storage of 32 recently accessed page table entries to optimize the time, is known as

- a) page table
- b) page descriptor base register
- c) page table cache
- d) none of the mentioned

Answer: c

Explanation: To optimize the considerable time taken for conversion, a page table cache is provided, which stores the 32 recently accessed page table entries.

14. The page table cache is also known as

- a) page table storage
- b) storage buffer
- c) translation look aside buffer
- d) all of the mentioned

Answer: c

Explanation: The page table cache is also known as translation look aside buffer.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Virtual 8086 Mode, the Coprocessor 80387".

1. If the 80386 enters the protected mode from the real address mode, then it returns back to the real mode, by performing the operation of

- a) read
- b) write
- c) terminate
- d) reset

Answer: d

Explanation: If the 80386 enters the protected mode from the real address mode, then it cannot return back to the real mode without a reset operation.

2. The unit that is needed for virtual mode 80386, only to run the 8086 programs, which require more than 1 Mbyte of memory for memory management functions, is

- a) execution unit
- b) central processing unit
- c) paging unit
- d) segmentation unit

Answer: c

Explanation: Paging unit is not necessarily enabled in the virtual mode, but may be needed to run the 8086 programs, which require more than 1 Mbyte of memory, for memory management functions.

3. The number of pages that the paging unit allows, in the virtual mode of 80386 is

- a) 64
- b) 128
- c) 256
- d) 512

Answer: c

Explanation: In virtual mode, the paging unit allows only 256 pages, each of 4Kbytes size. Each of the pages may be located anywhere within the maximum 4Gbytes physical memory.

4. The privilege level at which the real mode programs are executed is

- a) level 0
- b) level 1
- c) level 2
- d) level 3

Answer: a

Explanation: The real mode programs are executed at the highest privilege level i.e. level 0.

5. The instructions to prepare the processor for protected mode can only be executed at the privilege level

- a) level 0
- b) level 1
- c) level 2

d) level 3

Answer: a

Explanation: The instructions to prepare the processor for protected mode can only be executed at the level 0.

6. The instruction that is unable to set or read the VM (Virtual Mode) bit is

- a) PUSHF
- b) IRET
- c) POPF
- d) PUSHF and POPF

Answer: d

Explanation: The PUSHF and POPF instructions are unable to set or read the VM (Virtual Mode) bit, as they do not access it. The virtual mode can be entered by using IRET instruction.

7. If the CKM pin of 80387 is high, then 80387 is operated in

- a) real address mode
- b) protected mode
- c) synchronous mode
- d) asynchronous mode

Answer: c

Explanation: If the CKM pin of 80387 is high, then 80387 is operated in synchronous mode. If it is low, then 80387 is operated in asynchronous mode.

8. The unit that handles the data and directs it to either FIFO or instruction decoder depending on the bus control logic directive is

- a) paging unit
- b) central processing unit
- c) segmentation unit
- d) data interface and control unit

Answer: d

Explanation: The data interface and control unit handles the data, and direct it to either FIFO or instruction decoder, depending on the bus control logic directive.

9. The unit that is responsible for carrying out all the floating point calculations, allotted to the coprocessor by 80386, is

- a) Central processing unit
- b) ALU
- c) FPU
- d) None of the mentioned

Answer: c

Explanation: The FPU (floating point unit) is responsible for carrying out all the floating point calculations, allotted to the coprocessor by 80386.

10. The sizes of instruction and data pointer registers of 80387 respectively are

- a) 32-bit, 32-bit
- b) 48-bit, 32-bit
- c) 32-bit, 48-bit
- d) 48-bit, 48-bit

Answer: d

Explanation: 80387 consists of two 48-bit registers, known as instruction and data pointer registers.

11. To inform 80387 that the CPU wants to communicate with NPS1, the NPS1 line is directly connected to

- a) A31
- b) A30
- c) M/IO
- d) D31

Answer: c

Explanation: The NPS1 and NPS2 lines are directly connected with M/IO and A31 respectively, to inform 80387 that the CPU wants to communicate with it (NPS1), and it is using one of the reserved I/O addresses for 80387 (NPS2).

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Enhanced Instruction Set of 80386".

1. Which of the following is not a newly added instruction of 80386, that are not present in 80286?

- a) bit scan instructions
- b) bit test instructions
- c) shift double instructions
- d) none of the mentioned

Answer: d

Explanation: The newly added instructions of 80386 are categorized into

- 1. bit scan instructions
- 2. bit test instructions
- 3. conditional set byte instructions
- 4. shift double instructions
- 5. control transfer via gates instructions.

2. The BSF (bit scan forward) instruction scans the operand in the order

- a) from left to right
- b) from right to left
- c) from upper nibble
- d) none of the mentioned

Answer: b

Explanation: The BSF (bit scan forward) instruction scans the operand from right to left.

3. The BSR (bit scan reverse) instruction scans the operand in the order

- a) from left to right
- b) from right to left
- c) from upper nibble
- d) none of the mentioned

Answer: a

Explanation: The BSR (bit scan reverse) instruction scans the operand from left to right.

4. If a '1' is encountered when an operand is scanned by BSF, then

- a) zero flag is reset
- b) zero flag is set
- c) VM flag is set
- d) RF flag is reset

Answer: b

Explanation: The BSF instruction scans the operand from right to left. If a '1' is encountered during the scan, zero flag is set, and the bit position of '1' is stored into the destination operand.

5. If a '1' is not encountered when an operand is scanned by BSR, then

- a) zero flag is reset
- b) zero flag is set
- c) VM flag is reset
- d) RF flag is set

Answer: a

Explanation: The BSR instruction scans the operand from left to right. If a '1' is not encountered during the scan, zero flag is reset whether the scan is BSF or BSR.

6. Which of the following is not a bit test instruction?

- a) BTC
- b) BTS
- c) BSF
- d) BTR

Answer: c

Explanation: The instruction, BSF, is a bit scan instruction. The four bit test instructions are: BT (Test a Bit), BTC (Test a Bit and Complement), BTR (Test and Reset a Bit) and BTS (Test and Set a bit).

7. In case of BT instruction, if the bit position in the destination operand specified by the source operand, is '1', then

- a) zero flag is reset
- b) carry flag is set
- c) VM flag is set
- d) RF flag is reset

Answer: b

Explanation: In case of BT instruction, if the bit position in the destination operand specified by the source operand, is '1', the carry flag is set, otherwise it is cleared.

8. Which of the following is not a conditional set byte instruction?

- a) SETNP
- b) SETO
- c) SETNAE
- d) SHRD

Answer: d

Explanation: The SHRD (Shift Right Double) is a shift double instruction.

9. The instruction that shifts the specified number of bits in the instruction, from the upper side of the source operand into the lower side of the destination operand is

- a) SHRD
- b) SHLD
- c) SETNS
- d) None of the mentioned

Answer: b

Explanation: The SHLD instruction shifts the specified number of bits in the instruction, from the upper side (i.e. MSB) of the source operand into the lower side (i.e. LSB) of the destination operand.

10. The instruction that shifts 8 LSB bits of ECX into the MSB positions of EAX, one by one starting from LSB of ECX is

- a) SHLD ECX,EAX,8
- b) SHLD EAX,ECX,8
- c) SHRD ECX,EAX,8
- d) SHRD EAX,ECX,8

Answer: d

Explanation: The SHRD instruction shifts the specified number of bits in the instruction, from the lower side (i.e. LSB) of the source operand into the upper side (i.e. MSB) of the destination operand.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessors online test focuses on "Features of 80586 (Pentium), Concepts of Computer Architecture, Branch Prediction".

1. The salient feature of Pentium is

- a) superscalar architecture
- b) superpipelined architecture
- c) superscalar and superpipelined architecture
- d) none of the mentioned

Answer: c

Explanation: The salient feature of Pentium is its superscalar, superpipelined architecture.

2. The number of stages of the integer pipeline, U, of Pentium is

- a) 2
- b) 4
- c) 3
- d) 6

Answer: b

Explanation: The Pentium has two integer pipelines, U and V, where each one is a 4-stage pipeline.

3. Which of the following is a cache of Pentium?

- a) data cache
- b) data cache and instruction cache
- c) instruction cache
- d) none of the mentioned

Answer: b

Explanation: The Pentium has two separate caches. They are data cache and instruction cache.

4. The speed of integer arithmetic of Pentium is increased to a large extent by

- a) on-chip floating point unit
- b) superscalar architecture
- c) 4-stage pipelines
- d) all of the mentioned

Answer: c

Explanation: The Pentium has two integer pipelines, U and V, where each one is a 4-stage pipeline. This enhances the speed of integer arithmetic of Pentium to a large extent.

5. For enhancement of processor performance, beyond one instruction per cycle, the computer architects employ the technique of

- a) super pipelined technique
- b) multiple instruction issue
- c) super pipelined technique and multiple instruction issue
- d) none of the mentioned

Answer: b

Explanation: For enhancement of processor performance, beyond one instruction per cycle, the computer architects employ the technique of multiple instruction issue.

6. Which of the following is a class of architecture of MII (multiple instruction issue)?

- a) super pipelined architecture
- b) multiple instruction issue
- c) very small instruction word architecture
- d) super scalar architecture

Answer: d

Explanation: The MII architecture may again be classified into two categories:

- 1. Very long instruction word architecture
- 2. Superscalar architecture.

7. The compiler reorders the sequential stream of code that is coming from memory into a fixed size instruction group in

- a) super pipelined architecture
- b) multiple instruction issue
- c) very long instruction word architecture
- d) super scalar architecture

Answer: c

Explanation: In VLIW processors, the compiler reorders the sequential stream of code that is coming from memory into a fixed size instruction group, and issues them in parallel for execution.

8. The architecture in which the hardware decides which instructions are to be issued concurrently at run time is
- a) super pipelined architecture
 - b) multiple instruction issue
 - c) very long instruction word architecture
 - d) superscalar architecture

Answer: d

Explanation: In the superscalar architecture, the hardware decides which instructions are to be issued concurrently at run time.

9. The CPU has to wait until the execution stage to determine whether the condition is met in
- a) unconditional branch
 - b) conditional branch
 - c) pipelined execution branch
 - d) none of the mentioned

Answer: b

Explanation: In conditional branch, the CPU has to wait until the execution stage to determine whether the condition is met or not. When the condition satisfies, a branch is to be taken.

10. The memory device that holds branch target addresses for previously executed branches is
- a) Tristate buffer
 - b) RAM
 - c) ROM
 - d) Branch target buffer

Answer: d

Explanation: The branch target buffer in Pentium CPU holds branch target addresses for previously executed branches.

11. The branch target buffer is
- a) four-way set-associative memory
 - b) has branch instruction address
 - c) has destination address
 - d) all of the mentioned

Answer: d

Explanation: The branch target buffer is a four-way set-associative memory. Whenever a branch is taken, the CPU enters the branch instruction address, and also the destination address in the branch target buffer.

To practice all areas of Microprocessors for online tests, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "System Architecture".

1. The stage in which the CPU fetches the instructions from the instruction cache in superscalar organization is
- a) Prefetch stage
 - b) D1 (first decode) stage
 - c) D2 (second decode) stage
 - d) Final stage

Answer: a

Explanation: In the prefetch stage of pipeline, the CPU fetches the instructions from the instruction cache, which stores the instructions to be executed. In this stage, CPU also aligns the codes appropriately.

2. The CPU decodes the instructions and generates control words in
- a) Prefetch stage
 - b) D1 (first decode) stage
 - c) D2 (second decode) stage
 - d) Final stage

Answer: b

Explanation: In D1 stage, the CPU decodes the instructions and generates control words. For simple RISC instructions, only single control word is enough for starting the execution.

3. The fifth stage of pipeline is also known as

- a) read back stage
- b) read forward stage
- c) write back stage
- d) none of the mentioned

Answer: c

Explanation: The fifth stage or final stage of pipeline is also known as "Write back (WB) stage".

4. In the execution stage the function performed is

- a) CPU accesses data cache
- b) executes arithmetic/logic computations
- c) executes floating point operations in execution unit
- d) all of the mentioned

Answer: d

Explanation: In the execution stage, known as E-stage, the CPU accesses data cache, executes arithmetic/logic computations, and floating point operations in execution unit.

5. The stage in which the CPU generates an address for data memory references in this stage is

- a) prefetch stage
- b) D1 (first decode) stage
- c) D2 (second decode) stage
- d) execution stage

Answer: c

Explanation: In the D2 (second decode) stage, CPU generates an address for data memory references in this stage. This stage is required where the control word from D1 stage is again decoded for final execution.

6. The feature of separated caches is

- a) supports the superscalar organization
- b) high bandwidth
- c) low hit ratio
- d) all of the mentioned

Answer: d

Explanation: The separated caches have low hit ratio compared to a unified cache, but have the advantage of supporting the superscalar organization and high bandwidth.

7. In the operand fetch stage, the FPU (Floating Point Unit) fetches the operands from

- a) floating point unit
- b) instruction cache
- c) floating point register file or data cache
- d) floating point register file or instruction cache

Answer: c

Explanation: In the operand fetch stage, the FPU (Floating Point Unit) fetches the operands from either floating point register file or data cache.

8. The FPU (Floating Point Unit) writes the results to the floating point register file in

- a) X1 execution state
- b) X2 execution state
- c) write back stage
- d) none of the mentioned

Answer: c

Explanation: In the two execution stages of X1 and X2, the floating point unit reads the data from the data cache and executes the floating point computation. In the "write back stage" of pipeline, the FPU (Floating Point Unit) writes the results to the floating point register file.

9. The floating point multiplier segment performs floating point multiplication in
- a) single precision
 - b) double precision
 - c) extended precision
 - d) all of the mentioned

Answer: d

Explanation: The floating point multiplier segment performs floating point multiplication in single precision, double precision and extended precision.

10. The instruction or segment that executes the floating point square root instructions is
- a) floating point square root segment
 - b) floating point division and square root segment
 - c) floating point divider segment
 - d) none of the mentioned

Answer: c

Explanation: The floating point divider segment executes the floating point division and square root instructions.

11. The floating point rounder segment performs rounding off operation at
- a) after write back stage
 - b) before write back stage
 - c) before arithmetic operations
 - d) none of the mentioned

Answer: b

Explanation: The results of floating point addition or division process may be required to be rounded off, before write back stage to the floating point registers.

12. Which of the following is a floating point exception that is generated in case of integer arithmetic?
- a) divide by zero
 - b) overflow
 - c) denormal operand
 - d) all of the mentioned

Answer: d

Explanation: In the case of integer arithmetic, the possible floating point exceptions in Pentium are:

- 1. divide by zero
- 2. overflow
- 3. denormal operand
- 4. underflow
- 5. invalid operation.

13. The mechanism that determines whether a floating point operation will be executed without creating any exception is
- a) Multiple Instruction Issue
 - b) Multiple Exception Issue
 - c) Safe Instruction Recognition
 - d) Safe Exception Recognition

Answer: c

Explanation: A mechanism known as Safe Exception Recognition (SER) had been employed in Pentium which determines whether a floating point operation will be executed without creating any exception.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Numeric Coprocessor - 80486DX".

1. The first processor with an inbuilt floating point unit is
- a) 80386

- b) 80486
- c) 80286
- d) 8086

Answer: b

Explanation: The 32-bit CPU 80486 from Intel is the first processor with an inbuilt floating point unit. 80486DX is the first CPU with an on chip floating point unit.

2. Which of the following signal is handled by bus control and request sequencer?

- a) ADS#
- b) PWT
- c) RDY#
- d) All of the mentioned

Answer: d

Explanation: The bus control and request sequencer handle the signals like ADS#, PWT, RDY#, W/R#, INTR, NMI, LOCK#, HOLD, HLDA, RESET and M/IO# which basically controls the bus access and operations.

3. The unit that subjects the processor operation to boundary scan tests is

- a) parity generation and control unit
- b) prefetcher unit
- c) boundary scan and control unit
- d) segmentation unit

Answer: c

Explanation: The boundary scan and control unit subjects the processor operation to boundary scan tests to ensure the correct operation of various components of the mother board.

4. The management of the virtual memory of the system and adequate protection to data or codes in the physical memory is provided by

- a) segmentation unit
- b) paging unit
- c) attribute PLA
- d) all of the mentioned

Answer: d

Explanation: The segmentation unit, paging unit, attribute PLA, descriptor registers, translation look aside buffer and limit work together to manage the virtual memory of the system and provide the adequate protection to the codes or data in the physical memory.

5. The flag that is added to 80486 in additional to the flags similar to 80386 is

- a) alignment check flag
- b) parity check flag
- c) conditional flag
- d) all of the mentioned

Answer: a

Explanation: The register set of 80486 is similar to that of the 80386 but only a flag called as alignment check flag is added to the flag register of 80386 to obtain the flag register of 80486.

6. The major limitation of 80386-387 system is

- a) low speed
- b) 80386 sends data using an I/O handshake technique
- c) 80386 returns to real mode by reset operation
- d) none of the mentioned

Answer: b

Explanation: The major limitation of 80386-387 system is that the 80386 sends instruction or data to 80387 using an I/O handshake technique. To perform this handshaking and to carry additional house keeping tasks, 80386 requires 15 clock cycles or more.

7. The datatype that the 80486 doesnot support is

- a) Signed and unsigned
- b) ASCII

- c) Floating point
- d) None

Answer: d

Explanation: The datatypes that 80486 supports are

- 1. Signed
- 2. Unsigned
- 3. Floating point
- 4. BCD
- 5. String
- 6. ASCII.

8. In Little Endian data format, the data is stored as

- a) MSB is stored at lower memory address and LSB at higher memory address
- b) LSB is stored at lower memory address and MSB at higher memory address
- c) MSB is stored at general purpose registers
- d) LSB is stored at general purpose registers

Answer: b

Explanation: In Little Endian data format, for a data of size bigger than 1 byte, the LSB is stored at lower memory address and MSB at higher memory address.

9. The on-chip cache is used for storing

- a) addresses of data
- b) opcodes and data
- c) data and their addresses
- d) opcodes and their addresses

Answer: b

Explanation: The unique feature of 80486 that is not available in 80386 is that the on-chip is used for storing opcodes and data.

10. The on-chip cache is controlled by

- a) Cache disable(CD)
- b) No write through(NW)
- c) Cache disable and No write through
- d) None of the mentioned

Answer: c

Explanation: Cache disable(CD) and No write through(NW) bits of control register CR0. To completely disable cache, the CD and NW bits must be 11.

11. The on-chip cache can be flushed using external hardware using

- a) FLUSH pin
- b) TERMINATE pin
- c) FLOW pin
- d) Pin FLUSH# or using software

Answer: d

Explanation: The on-chip cache can be flushed using external hardware using pin FLUSH# or using the software. The flushing operation clears all the valid bits for all the cache lines.

To practice all areas of Microprocessors and Micro-controllers, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessors online quiz focuses on "MMX Data Types, Wrap-around and Saturation Arithmetic, Multimedia Application Programming, Pentium III (P-III) CPU".

1. In the data type, packed byte, the number of bytes that can be packed into one 64-bit quantity is

- a) 2
- b) 4
- c) 8
- d) 16

Answer: c

Explanation: In packed byte data type, eight bytes can be packed into one 64-bit quantity.

2. Four words can be packed into 64-bit by using the data type,

- a) unpacked word
- b) packed word
- c) packed doubled word
- d) one quad word

Answer: b

Explanation: By using the packed word data type, four words can be packed into 64-bits.

3. The number of double words that can be packed into 64-bit register using packed double word is

- a) 2
- b) 4
- c) 6
- d) 8

Answer: a

Explanation: Using packed double word, two double words can be packed into 64-bit.

4. The data type, "one quad word" packs _____ into 64-bit.

- a) two 32-bit quantities
- b) four 16-bit words
- c) one 32-bit and two 16-bit quantities
- d) one single 64-bit quantity

Answer: d

Explanation: The data type, "one quad word" packs one single 64-bit quantity into 64-bit register.

5. If the result of an operation is overflowed(exceeded than 16 bits) or underflowed then, only the lower 16-bits of the result are stored in the register and this effect is known as

- a) overflow/underflow effect
- b) wrap-around effect
- c) exceeding memory effect
- d) none

Answer: b

Explanation: If the result of an operation is overflowed (exceeded than 16 bits) or underflowed then, only the lower 16-bits of the result are stored in the register, and this effect is known as wrap-around effect.

6. In a multitasking operating system environment, each task should return to its own processor state which is

- a) contents of integer registers
- b) contents of floating point registers
- c) contents of MMX registers
- d) all of the mentioned

Answer: d

Explanation: In a multitasking operating system environment, each task should return to its own processor state, which should be saved when the task switching occurs. The processor state here means the contents of the registers, both integer and floating point or MMX register.

7. Which of the following exception generated by MMX is the same type of memory access exception as the X86 instructions?

- a) page fault
- b) segment not present
- c) limit violation
- d) all of the mentioned

Answer: d

Explanation: The MMX instruction set generates the same type of memory access exception as the X86 instructions namely; page fault, segment does not present and limit violation.

8. When an MMX instruction is getting executed, the floating-point tag word is marked

- a) 11
- b) 10
- c) 00
- d) 01

Answer: c

Explanation: When an MMX instruction is getting executed, the floating-point tag word is marked valid i.e. 00.

9. In a preemptive multitasking O.S., the saving and restoring of FP and MMX states are performed by

- a) Control unit
- b) O.S.
- c) MMX instructions
- d) MMX registers

Answer: b

Explanation: In a preemptive multitasking O.S., the application does not know when it is preempted. It is the job of the O.S. to save and restore the FP and MMX states, when performing a context switch. Thus the user need not save or restore the state.

10. The instruction of MMX that is essential when a floating-point routine calls an MMX routine or viceversa is

- a) MOV
- b) PADD
- c) EMMS
- d) None of the mentioned

Answer: c

Explanation: The EMMS instruction is imperative when a floating point routine calls an MMX routine or vice-versa. If we do not use EMMS at the end of MMX routine, subsequent floating-point instructions will produce erratic results.

11. Pentium III is used in computers which run on the operating system of

- a) windows NT
- b) windows 98
- c) unix
- d) all of the mentioned

Answer: d

Explanation: Pentium III is the best option to use in computers from high performance desktop to workstations and servers, running on operating systems like Windows NT, Windows 98 and UNIX.

12. The architecture of CPU of Pentium III is suitable for

- a) multimedia
- b) image processing
- c) speech processing
- d) all of the mentioned

Answer: d

Explanation: The architecture of CPU of Pentium III is suitable for applications like imaging, image processing, speech processing, multimedia and internet applications.

13. The Pentium III has the operating frequencies as

- a) 300MHz,350MHz,400MHz
- b) 400MHz,450MHz,500MHz
- c) 350MHz,400MHz,450MHz
- d) 450MHz,500MHz,550MHz

Answer: d

Explanation: The Pentium III has three versions operating at frequencies, 450MHz, 500MHz and 550MHz, which are all commercially available.

14. The Pentium III consists of

- a) dual independent bus architecture
- b) 512 Kbyte cache
- c) eight 64-wide Intel MMX registers
- d) all of the mentioned

Answer: d

Explanation: The Pentium III has dual independent bus architecture that increases the bandwidth. It has a 512 Kbyte unified, non-blocking level2 cache and eight 64-wide Intel MMX registers.

To practice all areas of Microprocessors for online Quizzes, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Tricky Microprocessors Questions and Answers focuses on “Enhanced Instruction Set of Pentium, Intel MMX Architecture”.

1. Which of the following is not a transcendental instruction?

- a) FSIN
- b) FCOS
- c) FMUL
- d) FPTAN

Answer: c

Explanation: The FMUL instruction is a float point multiplication, which is not a transcendental instruction.

2. The transcendental instruction that supports computation of sine and cosine is

- a) FCOSIN
- b) FSNE
- c) FSINFCOS
- d) FSINCOS

Answer: d

Explanation: The instruction, FSINCOS, supports to compute sine and cosine.

3. The instruction that computes $\tan(x)$ is

- a) FTAN
- b) FTNGNT
- c) FPTAN
- d) FXTAN

Answer: c

Explanation: The instruction, FPTAN, computes $\tan(x)$.

4. The instruction that computes $\arctan(x)$ is

- a) FTAN
- b) FACTN
- c) FARCTAN
- d) FPATAN

Answer: d

Explanation: The instruction, FPATAN, computes $\arctan(x)$ which is arc tangent of x.

5. The instruction, F2XMI, is used to compute

- a) $2X$
- b) $2X-1$
- c) $2X+1$
- d) $2X+2$

Answer: b

Explanation: The instruction, F2XMI, is used to compute $2X-1$.

6. The instruction, FYL2XP, supports to compute the expression

- a) $Y \cdot \log X$
- b) $Y \cdot \log 2X$
- c) $Y \cdot \log(2X+1)$
- d) $Y \cdot \log 2(X+1)$

Answer: d

Explanation: The instruction, FYL2XP, supports to compute the expression $Y \cdot \log 2(X+1)$.

7. The size of a general purpose floating point register of floating point unit is

- a) 4 bytes
- b) 40 bytes
- c) 8 bytes
- d) 80 bits

Answer: d

Explanation: There are eight general purpose floating point registers in the floating point unit. Each of these eight registers are of 80-bits width.

8. For floating point operations, the bits used by mantissa in a floating point register is

- a) 32
- b) 64
- c) 72
- d) 79

Answer: b

Explanation: For floating point operations, 64 bits are used for the mantissa, and the rest 16 bits for exponent.

9. The multimedia applications mainly require the architecture of

- a) single instruction stream single data stream
- b) multiple instruction stream single data stream
- c) single instruction stream multiple data stream
- d) multiple instruction stream multiple data stream

Answer: c

Explanation: Most of the multimedia applications mainly require the architecture of single instruction stream multiple data stream.

10. The size of each MMX (Multimedia Extension) register is

- a) 32 bits
- b) 64 bits
- c) 128 bits
- d) 256 bits

Answer: b

Explanation: The MMX registers use only the 64-bit mantissa portion of the general purpose floating point registers, to store MMX operands. Thus, the MMX programmers virtually get eight new MMX registers, each of 64 bits.

11. After a sequence of MMX instructions is executed, the MMX registers should be cleared by an instruction,

- a) CLEAR
- b) RESET
- c) EMM
- d) EMMS

Answer: d

Explanation: After a sequence of MMX instructions is executed, the MMX registers should be cleared by an instruction, EMMS, which implies Empty the MMX Stack.

12. The number of pixels that can be manipulated in a single register by the CPU using MMX architecture is

- a) 4
- b) 6

- c) 8
- d) 10

Answer: c

Explanation: Any CPU can manipulate only one pixel at a time. But by using MMX architecture, we can manipulate eight such pixels, packed in a single 64-bit register.

13. After executing the floating point instructions, the floating point registers should be cleared by an instruction,

- a) CLEAR
- b) EFPR
- c) EMMF
- d) EMMS

Answer: d

Explanation: After executing the floating point instructions, the floating point registers should be cleared by an instruction, EMMS.

To practice tricky questions and answers on all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on “Pentium – Pro and Pentium-II -1”.

1. The instructions that pass through the fetch, decode and execution stages sequentially is known as

- a) sequential instruction
- b) sequence of fetch, decode and execution
- c) linear instruction sequencing
- d) non-linear instruction sequencing

Answer: c

Explanation: The linear instruction sequencing is the one in which the instructions that pass through the fetch, decode and execution stages sequentially.

2. During the execution of instructions, if an instruction is executed, then next instruction is executed only when the data is read by

- a) control unit
- b) bus interface unit
- c) execution unit
- d) cpu

Answer: b

Explanation: During the execution of instructions, only after the bus interface unit of CPU reads the data from the main memory and returns it to the register, the next instruction execution will commence.

3. Because of Pentium’s superscalar architecture, the number of instructions that are executed per clock cycle is

- a) 1
- b) 2
- c) 3
- d) 4

Answer: b

Explanation: Pentium’s superscalar architecture employs five stage pipeline with U and V pipes. Thus it can execute two instructions per clock.

4. The type of execution which means that the CPU should speculate which of the next instructions can be executed earlier is

- a) speculative execution
- b) out of turn execution
- c) dual independent bus
- d) multiple branch prediction

Answer: a

Explanation: The speculative execution is an execution which means that the CPU should speculate which of the next instructions can be executed earlier.

5. The execution in which the consecutive instruction execution in a sequential flow is hampered is

- a) speculative execution
- b) out of turn execution
- c) dual independent bus
- d) multiple branch prediction

Answer: b

Explanation: In the out of turn execution, the consecutive instruction execution in a sequential flow is hampered and the CPU should be able to execute out of turn instructions.

6. A dual independent bus has

- a) Enhanced system bandwidth
- b) CPU that can access both cache and memory simultaneously
- c) High throughput
- d) All of the mentioned

Answer: d

Explanation: A dual independent bus architecture is incorporated by Pentium-Pro to get an enhanced system bandwidth and it also yields high throughput. It has the CPU which can access both main memory and the cache simultaneously.

7. The unit that is used to implement the multiple branch prediction in Pentium-Pro is

- a) control unit
- b) bus interface unit
- c) branch target buffer
- d) branch instruction register

Answer: c

Explanation: The processor uses an associative memory called branch target buffer for implementing the algorithm, multiple branch prediction.

8. Which of the following is not an independent engine of Pentium-Pro?

- a) fetch-decode unit
- b) dispatch-execute unit
- c) control-execute unit
- d) retire unit

Answer: c

Explanation: Pentium-Pro incorporates three independent engines, 1. Fetch-decode unit 2. Dispatch-execute unit 3. Retire unit.

9. The unit that accepts the sequence of instructions from the instruction cache as input is

- a) fetch-decode unit
- b) dispatch-execute unit
- c) retire unit
- d) none

Answer: a

Explanation: The fetch-decode unit accepts the sequence of instructions from the instruction cache as input and then decodes them.

10. In fetch-decode unit, the number of parallel decoders that accept the stream of fetched instructions and decode them is

- a) 1
- b) 2
- c) 3
- d) 4

Answer: c

Explanation: A set of three parallel decoders accepts the stream of fetched instructions and decode them.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on “MMX Instruction Set”.

1. The additional instructions that are designed especially for performing multimedia tasks are known as

- a) additional MMX instructions
- b) multimedia MMX instructions
- c) enhanced MMX instructions
- d) none of the mentioned

Answer: c

Explanation: The MMX technology adds 57 new instructions to the instruction set of processors. These instructions are known as enhanced MMX instructions and are designed specifically for performing multimedia tasks.

2. The MMX instruction, EMMS consists of _____ on which it operates.

- a) source operand
- b) destination operand
- c) source and destination operand
- d) none of the mentioned

Answer: d

Explanation: The instruction, EMMS, does not have any operand.

3. In all the MMX instructions, the destination operand resides in

- a) Memory
- b) RAM
- c) Either in an MMX register or in memory
- d) MMX register

Answer: d

Explanation: In all the MMX instructions, the source operand is found either in an MMX register or in memory, and the destination operand resides in MMX register.

4. For the MMX instructions, the prefix, P, is used to represent the mode of

- a) real addressing mode
- b) virtual mode
- c) packed mode
- d) programmable mode

Answer: c

Explanation: In the MMX instructions, if the operands are in the packed mode, the prefix, P, is used to indicate packed data.

5. For the MMX instructions, the suffix, S, is used to represent

- a) status
- b) saturation
- c) signed saturation
- d) unsigned saturation

Answer: c

Explanation: For the MMX instructions, the suffix “S” indicates signed saturation, and “US” indicates unsigned saturation, while executing arithmetic computation in saturation mode.

6. The instruction that is used for quadword is

- a) PADD
- b) PCMPEQ
- c) PAND
- d) None of the mentioned

Answer: d

Explanation: The instructions, PADD, PCMPEQ and PAND are used for packed byte, word and double word.

7. The instruction, PSUBB, performs subtraction in

- a) packed word
- b) packed byte
- c) packed double word
- d) unpacked word

Answer: b

Explanation: The instruction, PSUBB, performs subtraction in a packed byte.

8. The instruction, PCMPGT, is used to compare two data types and check

- a) equal to condition
- b) less than condition
- c) greater than condition
- d) equal to and greater than condition

Answer: c

Explanation: The instruction, PCMPGT, compares to check the greater than condition in packed bytes, packed words and packed double words.

9. The instruction that is not operated on quad word is

- a) MOV
- b) PSLL
- c) PSRA
- d) All of the mentioned

Answer: c

Explanation: The instruction, PSRA, performs arithmetic shift, right in a single cycle. It supports only the shifting of packed word and double word data types.

10. When the instruction, PMULLW, is performed, then the lower order 16-bits of the 32 bit products are stored in

- a) source operand
- b) destination operand
- c) no storage of lower order
- d) either source or destination

Answer: b

Explanation: In the instruction, PMULLW, four 16 X 16 multiplications are performed, and the lower order 16 bits of the 32-bit products are stored in destination.

11. When the instruction, PMULHW, is performed, then the higher order 16-bits of the 32 bit products are stored in

- a) source operand
- b) destination operand
- c) no storage of lower order
- d) either source or destination

Answer: b

Explanation: In the instruction, PMULHW, four 16 X 16 multiplications are performed, and the higher order 16 bits of the 32-bit products are stored in destination.

12. The instruction in which both multiplication and addition are performed is

- a) PAND
- b) PMULHW
- c) PADD
- d) PMADDWD

Answer: d

Explanation: PMADDWD is an important multimedia instruction, which multiplies the four signed words of the destination operand, with four signed words of source operand. This

results in 32-bit double words which are added, and the result is stored in the higher double word of the destination operand.

13. If the result of PCMPEQ, which is a comparison of two packed data types, is a success, then the mask generated is

- a) mask 0s
- b) mask 1s
- c) mask 2s
- d) mask 3s

Answer: b

Explanation: If the result of PCMPEQ, which is a comparison of two packed data types is a success, then the mask 1s is generated, otherwise a mask of 0s is generated, in the destination operand.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessors Question Bank focuses on “Pro and Pentium-II -2”.

1. The decoder unit in fetch-decode unit converts the instructions into

- a) executable statements
- b) machine language statements
- c) MMX instructions
- d) micro operations

Answer: d

Explanation: The decoder unit converts the fetched instructions into micro operations.

2. The logical source(s) and logical destination(s) that the micro operation has respectively are

- a) 2,2
- b) 1,3
- c) 3,1
- d) 3,2

Answer: c

Explanation: Each microoperation contains two logical sources and one logical destination.

3. The microoperations that are converted by decoder are directly transferred to

- a) decoder register
- b) dispatch-execute unit
- c) retire unit
- d) register alias table

Answer: d

Explanation: The microoperations are sent to the register alias table(RAT). The RAT translates the logical register references to the physical register set actually available in the CPU.

4. The pool of instructions that are fetched is stored in an addressable memory called

- a) tristate buffer
- b) branch target buffer
- c) reorder buffer
- d) order buffer

Answer: c

Explanation: The pool of instructions that are fetched is stored in an array of content addressable memory called reorder buffer.

5. The unit that performs scheduling of instructions by determining the data dependencies is

- a) fetch-decode unit
- b) dispatch-execute unit
- c) retire unit
- d) none

Answer: b

Explanation: The dispatch-execute unit performs scheduling of instructions by determining the

data dependencies after which the microoperations of the scheduled instructions are executed in the execution unit.

6. The unit that reads the instruction pool and removes the microoperations which have been executed instruction pool is

- a) fetch-decode unit
- b) dispatch-execute unit
- c) retire unit
- d) decoding unit

Answer: c

Explanation: The retire unit reads the instruction pool containing the instructions and removes the microoperations which have been executed instruction pool.

7. The speed of Pentium-Pro when compared to that of Pentium is

- a) equal
- b) twice
- c) thrice
- d) two-third

Answer: b

Explanation: The features incorporated in Pentium-Pro enhances the speed of Pentium-Pro and is twice as that of Pentium.

8. Which of the following is not supported by Pentium-Pro?

- a) multiple branch prediction
- b) mmx instruction set
- c) speculative execution
- d) none

Answer: b

Explanation: The Pentium-Pro does not support the MMX instruction set.

9. The feature of Pentium II is

- a) high cache
- b) operates at 2.8 volts
- c) supports intel's MMX instructions
- d) all of the mentioned

Answer: d

Explanation: The Pentium II has a higher cache and it can operate at 2.8 volts, thereby reducing power consumption. The most important change of Pentium II is that it can support Intel's MMX instructions.

10. The results of speculative instruction execution is stored in

- a) visible CPU registers
- b) permanent memory
- c) temporary memory
- d) none

Answer: c

Explanation: The results of speculative instruction execution should not be stored in CPU registers and are temporarily stored, since they may have to be discarded, in case if there is a branch instruction before these speculative instruction executions.

To practice Microprocessors Question Bank, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Features of Pentium 4, Netburst Microarchitecture For Pentium4 - 1".

1. The feature of Pentium 4 is

- a) works based on NetBurst microarchitecture
- b) clock speed ranges from 1.4GHz to 1.7GHz
- c) has hyper-pipelined technology
- d) all of the mentioned

Answer: d

Explanation: Pentium 4 is based on NetBurst microarchitecture. Clock speed varies from 1.4GHz to 1.7GHz. It has hyper-pipelined technology.

2. Which of the following is not a module of Pentium 4 architecture?

- a) front end module
- b) execution module
- c) control module
- d) none

Answer: c

Explanation: Pentium 4 architecture may be viewed having four basic modules.

- 1. Front end module
- 2. Out of order execution engine
- 3. Execution module
- 4. Memory subsystem module.

3. The front module of Pentium 4 consists of

- a) trace cache
- b) microcode ROM
- c) front end branch predictor
- d) all of the mentioned

Answer: d

Explanation: The front module of Pentium 4 contains

- 1. IA 32 Instruction decoder
- 2. Trace cache
- 3. Microcode ROM
- 4. Front end branch predictor.

4. The unit that decodes the instructions concurrently and translate them into micro-operations is

- a) trace cache
- b) instruction decoder
- c) execution module
- d) front end branch predictor

Answer: b

Explanation: The role of instruction decoder is to decode the instructions concurrently and translate them into micro-operations known as micro-ops.

5. In complex instructions, when the instruction needs to be translated into more than 4 micro-operations, then the decoder transfers the task to

- a) trace cache
- b) front end branch predictor
- c) microcode ROM
- d) none

Answer: c

Explanation: In case of complex instructions, when the instruction needs to be translated into more than 4 micro-operations, then the decoder transfers the task to microcode ROM.

6. The unit that does not store the instructions, but the decoded stream of instructions is

- a) trace cache
- b) front end branch predictor
- c) microcode ROM
- d) none

Answer: a

Explanation: The trace cache is a special instruction cache because it does not store the instructions, but the decoded stream of instructions.

7. Trace cache can store the micro-ops upto a range of

- a) 6 K decoded micro-ops
- b) 8 K decoded micro-ops

- c) 10 K decoded micro-ops
- d) 12 K decoded micro-ops

Answer: d

Explanation: Trace cache can store upto 12K micro-ops. The cache assembles the decoded micro-ops into ordered sequence of micro-ops called traces.

8. The unit that predicts the locations from where the next instruction bytes are fetched is
- a) trace cache
 - b) front end branch predictor
 - c) execution module
 - d) instruction decoder

Answer: b

Explanation: The front end branch predictor predicts the locations from where the next instruction bytes are fetched.

9. If complex instructions like interrupt handling, string manipulation appear, then the control from trace cache transfers to
- a) microcode ROM
 - b) front end branch predictor
 - c) execution module
 - d) instruction decoder

Answer: a

Explanation: When some complex instructions like interrupt handling, string manipulation appear, then the control from trace cache transfers to microcode ROM.

10. After the micro-ops are issued by the microcode ROM, the control goes to
- a) trace cache
 - b) front end branch predictor
 - c) execution module
 - d) instruction decoder

Answer: a

Explanation: After the micro-ops are issued by the microcode ROM, the control goes to Trace cache once again. The micro-ops delivered by the trace cache and the microcode ROM are buffered in a queue in an orderly fashion.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessors Questions and Answers for Entrance exams focuses on “Netburst Microarchitecture For Pentium4 -2, Instruction Translation Lookaside Buffer (ITLB) and Branch Prediction”.

1. If the logical processors want to execute complex IA-32 instructions simultaneously then the number of microcode instruction pointers required is
- a) 1
 - b) 2
 - c) 3
 - d) 4

Answer: b

Explanation: If both the logical processors want to execute complex IA-32 instructions simultaneously then two microcode instruction pointers are required, which will access the microcode ROM.

2. Which of the following is a type of branch prediction?
- a) static prediction
 - b) dynamic prediction
 - c) static and dynamic prediction
 - d) none

Answer: c

Explanation: There are two types of branch prediction namely static prediction and dynamic prediction.

3. The prediction that is based on a statistical assumption that the majority of backward branches occur in repetitive loops is

- a) static prediction
- b) dynamic prediction
- c) branch prediction
- d) none

Answer: a

Explanation: The static prediction is based on a statistical assumption that the majority of backward branches occur in the context of repetitive loops.

4. The advantage of static prediction is

- a) simple and fast
- b) does not require table lookups or calculations
- c) performs without much degradation
- d) all of the mentioned

Answer: d

Explanation: The static prediction is simple and fast. It does not require table lookups or calculations. In case if a program contains a number of loops, static prediction performs without much degradation.

5. The dynamic branch prediction algorithms use

- a) Branch History Table (BHT)
- b) Branch Target Buffer (BTB)
- c) Branch History Table and Branch Target Buffer
- d) None

Answer: c

Explanation: The dynamic branch prediction algorithms use two types of tables, namely Branch History Table (BHT) and Branch Target Buffer (BTB).

6. The unit that preserves the history of each conditional branch is

- a) Branch Target Buffer (BTB)
- b) Branch History Table (BHT)
- c) Static prediction
- d) Dynamic prediction

Answer: b

Explanation: The Branch History Table (BHT) preserves the history of each conditional branch that the speculative branch prediction unit encounters during the last several cycles.

7. The BHT keeps a record that indicates the likelihood of the branches grouped as

- a) strongly taken
- b) taken
- c) not taken
- d) all of the mentioned

Answer: d

Explanation: The BHT keeps a record that indicates the likelihood that the branch will be taken based on its past history. The branches may be grouped as 'strongly taken', 'taken', 'not taken' and 'strongly not taken'.

8. Each logical processor has

- a) one 64-byte streaming buffer
- b) one 32-byte streaming buffer
- c) two 64-byte streaming buffers
- d) two 32-byte streaming buffers

Answer: c

Explanation: Each logic processor has its own set of two 64-byte streaming buffers, which store the instruction bytes and subsequently they are dispatched to the instruction decode stage.

9. If there is a trace cache miss, then the instruction bytes are required to be fetched from the
- a) instruction decoder
 - b) Level2 cache
 - c) execution module
 - d) none of the mentioned

Answer: b

Explanation: If there is a trace cache miss, then the instruction bytes are required to be fetched from the Level2 cache.

10. The Instruction Translation Lookaside Buffer(ITLB) is present in
- a) trace cache
 - b) instruction decoder
 - c) logical processors
 - d) all of the mentioned

Answer: c

Explanation: Since there are two logical processors, there are two ITLBs. Thus each logical processor has its own ITLB and its own instruction pointer to track the progress of instruction fetch for each of them.

To practice all areas of Microprocessors for Entrance exams, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Tough Microprocessors Questions and Answers focuses on “Rapid Execution Module, Memory Subsystem, Hyperthreading Technology”.

1. The units that are primarily used to resolve indirect mode of memory addressing is called
- a) ALU
 - b) AGU
 - c) ALU and AGU
 - d) NONE

Answer: b

Explanation: The AGUs(Address Generation Units) are primarily used to resolve indirect mode of memory addressing.

2. The AGUs work at a speed of
- a) equal to that of processor
 - b) twice the processor
 - c) thrice the processor
 - d) none

Answer: b

Explanation: The AGUs run at twice the processor speed.

3. Pentium 4 consists of
- a) 4 ALUs
 - b) 4 AGUs
 - c) 2 ALUs and 2 AGUs
 - d) 4 ALUs and 4 AGUs

Answer: c

Explanation: Pentium 4 consists of 2 ALUs and 2 AGUs.

4. The number of instructions that can be executed per clock cycle by the ALU or AGU is
- a) 1
 - b) 2
 - c) 3
 - d) 4

Answer: b

Explanation: As the speed of the units, ALU and AGU are doubled, which means that twice the number of instructions being executed per clock cycle.

5. The paging mechanism of IA-32 architecture has an extension as

- a) page memory extension
- b) page size extension
- c) page address extension and page size extension
- d) page memory extension and page size extension

Answer: c

Explanation: IA-32 architecture's paging mechanism includes an extension that support

1. Page address extension to address space greater than 4GB.
2. Page size extension to map linear address to physical address in 4MB.

6. The linear address space is mapped into the processors physical address space either directly or through paging by

- a) flat memory model
- b) segmented memory model
- c) flat or segmented memory model
- d) none

Answer: c

Explanation: With the flat or segmented memory model, linear address space is mapped into the processors physical address space either directly or through paging.

7. The features of thread in threading process is

- a) threads can be bunched together
- b) threads are simple and light weight
- c) threads are independent
- d) all of the mentioned

Answer: d

Explanation: Threads may be bunched together in a process. Threads are independent, simple in structure and are lightweight in the sense that they may enhance the speed of operation of an overall process.

8. The process in which multiple threads correspond to the tracking of each individual object is known as

- a) multiple thread system
- b) multi thread parallelism
- c) thread level parallelism
- d) multi level parallelism

Answer: c

Explanation: The mutiple threads correspond to the tracking of each individual object. This kind of parallelism is known as thread level parallelism(TLP).

9. Which of the following is not a type of context switching?

- a) time-slice multithreading
- b) on chip multiprocessing
- c) hyperthreading
- d) none

Answer: d

Explanation: A single processor can execute multiple threads by switching between them. The scheme of context switching may be several types. They are

1. Time-slice multithreading
2. On chip multiprocessing
3. Hyperthreading.

10. The thread level parallelism is a process of

- a) saving the context of currently executing process
- b) flushing the CPU of the same process
- c) loading the context of new next process

d) all of the mentioned

Answer: d

Explanation: The thread level parallelism is a process of

1. Saving the context of currently executing process.
2. Flushing the CPU of the same process.
3. Loading the context of new next process is called a context switch.

To practice tough questions and answers on all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Hyperthreading In Pentium".

1. Which of the following is a resource sharing strategy that had been investigated by the developers?

- a) partitioned resources
- b) threshold sharing
- c) full sharing
- d) all of the mentioned

Answer: d

Explanation: Several resource sharing strategies have been investigated by the developers.

Some of these are

1. Partitioned resources
 2. Threshold sharing
 3. Full sharing.
2. The feature of hyperthreading is
- a) simultaneous multithreading
 - b) switching is not required
 - c) effective use of processor resources
 - d) all of the mentioned

Answer: d

Explanation: Hyperthreading used the concept of simultaneous multithreading, where multiple threads can be executed on a single processor without switching.

3. Each logical processor maintains a set of architecture state which consists of

- a) general purpose registers
- b) machine state register
- c) advanced programmed interrupt controller
- d) all of the mentioned

Answer: d

Explanation: Each logical processor maintains a set of architecture state which consists of

1. Registers including the general purpose registers
2. The control register
3. Advanced programmed interrupt controller
4. Machine state register.

4. A logical processor may be temporarily stalled for

- a) including servicing cache misses
- b) handling branch mispredictions
- c) waiting for results of previous instructions
- d) all of the mentioned

Answer: d

Explanation: A logical processor may be temporarily stalled for a variety of reasons like including servicing cache misses, handling branch mispredictions and waiting for results of previous instructions.

5. The hyperthreading technology automatically involves the

- a) decrease of die area
- b) increase of die area
- c) decrease of die area to half

d) none

Answer: b

Explanation: The hyperthreading technology automatically involves the increase of die area.

6. The instruction that is used when either of the logical processors is idle is

- a) HOLD
- b) HLDA
- c) HALT
- d) NONE

Answer: c

Explanation: An optimization may require the use of HALT instruction, when either of the two logical processors is idle.

7. The mode that is available when there is only one software thread to execute is

- a) single task mode
- b) multi task mode
- c) single task and multi task mode
- d) dual task mode

Answer: c

Explanation: When there is only one software thread to execute, there are two modes namely single task mode and multi task mode.

8. The HALT instruction is a privileged instruction that can be only used by

- a) execution unit
- b) operating system
- c) control unit
- d) memory unit

Answer: b

Explanation: The HALT instruction is a privileged instruction that can be only used by operating system.

9. When the operating system uses HALT instruction on a processor which supports multithreading, the operation moves from

- a) Single task to multi task mode
- b) ST1 to ST0
- c) Multi task to single task mode
- d) None

Answer: c

Explanation: When the operating system uses HALT instruction on a processor which supports multithreading, the operation moves from multi tasking mode to single tasking mode.

10. The Xeon TM processor on which hyperthreading technology was first implemented consists of

- a) one logical processor per physical processor
- b) two logical processor per physical processor
- c) three logical processor per physical processor
- d) zero logical processor per physical processor

Answer: b

Explanation: The Xeon TM processor on which hyperthreading technology was first implemented consists of two logical processor per physical processor.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers.](#)

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Hybrid Architecture -RISC and CISC Convergence, Advantages of RISC, Design Issues of RISC Processors -1".

1. The disadvantage of CISC design processors is

- a) low burden on compiler developers
- b) wide availability of existing software

- c) complex in nature
- d) none

Answer: c

Explanation: Some computers are used in preference to CISC design due to its low burden on compiler developers and wide availability of existing software. But they are complex in nature.

2. The RISC architecture is preferred to CISC because RISC architecture has
- a) simplicity
 - b) efficiency
 - c) high speed
 - d) all of the mentioned

Answer: d

Explanation: The RISC architecture is preferred to CISC because RISC architecture is simple, highly efficient and the processors using RISC architecture have high speed.

3. The feature of RISC that is not present in CISC is
- a) branch prediction
 - b) pipelining
 - c) branch prediction and pipelining
 - d) none

Answer: c

Explanation: A RISC core allows performance enhancing features, such as branch prediction and pipelining. Traditionally, these have only been possible in RISC designs.

4. The feature of hybrid CISC-RISC architecture is
- a) consume a lot of power
 - b) not applicable to mobile applications
 - c) processed by RISC core
 - d) all of the mentioned

Answer: d

Explanation: The CISC-RISC hybrids continue to consume a lot of power and are not best candidates for mobile and embedded applications.

5. Which of the following is an application of RISC architecture by adding more instructions?
- a) multimedia applications
 - b) telecommunication encoding
 - c) image conversion
 - d) all of the mentioned

Answer: d

Explanation: By adding more instructions to the RISC architecture, some applications can be run much faster like multimedia applications, telecommunication encoding/decoding, image conversion and video processing.

6. Which of the following processor belongs to hybrid RISC-CISC architecture?
- a) Intel Pentium III
 - b) Intel Itanium 64
 - c) AMD's X86-64
 - d) All of the mentioned

Answer: d

Explanation: The processors, Intel Pentium III, Intel Itanium 64 and AMD's X86-64 consists of hybrid RISC-CISC architecture.

7. In order to implement complex instructions, CISC architectures use
- a) macroprogramming
 - b) hardwire
 - c) microprogramming
 - d) none

Answer: c

Explanation: In order to implement complex instructions, CISC architectures use microprogramming.

8. The advantage of RISC processors is

- a) can operate at high clock frequency
- b) shorter design cycle
- c) simple and fast
- d) all of the mentioned

Answer: d

Explanation: The advantages of RISC processors are that they can work at high clock frequency, can be designed, developed and tested more quickly with a high speed.

9. The additional functionality that can be placed on the same chip of RISC is

- a) Memory management units
- b) Floating point units
- c) Memory management and floating point arithmetic units
- d) RAM, ROM

Answer: c

Explanation: Several extra functionalities, such as memory management units or floating point arithmetic units, can also be placed on the same chip of RISC.

10. The number of clockcycles that take to wait until the length of the instruction is known in order to start decoding is

- a) 0
- b) 1
- c) 2
- d) 3

Answer: a

Explanation: The loading and decoding the instructions in a RISC processor is simple and fast. It is not needed to wait until the length of the instruction is known in order to start the decoding.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Basic Microprocessors Questions and Answers focuses on “Extended Instruction Set In Advanced Pentium Processors, Formal Verification”.

1. The MMX instructions support only

- a) character data type
- b) float data type
- c) integer data type
- d) string data type

Answer: c

Explanation: The MMX instructions support only integer data type.

2. For single precision floating point numbers, the SSE instructions are

- a) MMX instructions
- b) SIMD instructions
- c) Floating point executions
- d) None

Answer: b

Explanation: The SSE instructions are SIMD(Single Instruction Multiple Data Stream) instructions for single precision floating point numbers.

3. The feature of SSE among the following is

- a) operate on four 32-bit floating points
- b) register size is of 128 bits
- c) no switching from one mode to other
- d) all of the mentioned

Answer: d

Explanation: The features of SSE(Streaming SIMD extensions) are

1. SSE instructions are SIMD instructions for single precision floating point numbers.
2. They operate on four 32-bit floating points.
3. The register size is of 128 bits
4. No necessity to switch from one mode to other.

4. The new instructions that are added in SSE for floating point operations are of

- a) 72
- b) 50
- c) 25
- d) 8

Answer: b

Explanation: The new instructions that are added in SSE for floating point operations are 50.

5. The SSE instructions can operate on

- a) packed data
- b) unpacked data
- c) dynamic data
- d) all of the mentioned

Answer: a

Explanation: The SSE instructions can operate on packed data or scalar data.

6. Which of the following group is not of SSE instructions?

- a) jump or branch group of instruction
- b) logic and comparison group of instruction
- c) shuffle instructions
- d) all of the mentioned

Answer: d

Explanation: The SSE instructions can be grouped to many types. Some of them are

1. Data transfer instructions
2. Arithmetic, logic and comparison group of instruction
3. shuffle instructions
4. Cacheability instructions.

7. Which of the following is true about SSE2 instructions in Pentium III and Pentium 4?

- a) SSE increases the accuracy of double precision floating point operations
- b) SSE supports new formats of packed data
- c) SSE increases the speed of manipulation of SIMD integer operations
- d) All of the mentioned

Answer: d

Explanation: The SSE new instruction set increases the accuracy of double precision floating point operations, supports new formats of packed data.

8. The data type that the SSE2 instructions doesn't support is

- a) single precision floating points
- b) double precision floating points
- c) single and double precision floating points
- d) none of the mentioned

Answer: d

Explanation: The SSE2 instructions support new data types such as double precision floating points along with single precision floating points.

9. The additional instructions of SSE3 over SSE2 contains

- a) video encoding
- b) complex arithmetic operation
- c) thread synchronization
- d) all of the mentioned

Answer: d

Explanation: The SSE3 contains 13 additional SIMD instructions over SSE2. These instructions comprise five types.

- i. floating point to integer conversion
- ii. complex arithmetic operation
- iii. video encoding
- iv. SIMD floating point operations using array of structures format
- v. thread synchronization.

10. The unit that may acts as an interface between the Front end and the Out of order execution engine in the pipeline flow is

- a) micro-op queue
- b) micro-op stack
- c) micro-ops
- d) none

Answer: a

Explanation: The micro-op queue acts as an interface between the Front end and the Out of order execution engine in the pipeline flow.

11. The verification of the logic using formal mathematical tools is called

- a) arithmetic verification
- b) formal verification
- c) mathematical verification
- d) logical verification

Answer: b

Explanation: The verification of the logic using formal mathematical tools is called formal verification.

12. The formal verification is important for

- a) developing the tools
- b) developing the methodologies
- c) to detect the bugs in design
- d) all of the mentioned

Answer: d

Explanation: The formal verification is important to develop the tools and methodologies to handle a large number of proofs using which it will be possible to detect the bugs in the design.

13. By using the techniques of formal verification, one can detect the logical bugs of

- a) more than 50
- b) less than 50
- c) more than 100
- d) less than 100

Answer: c

Explanation: By using the techniques of formal verification, one can detect more than 100 logical bugs.

14. The modern processors are designed to achieve

- a) high speed
- b) operate at low operating voltage
- c) uses cooling technology
- d) all of the mentioned

Answer: d

Explanation: The modern processors are designed to operate at a very high speed and even with the lower operating voltages, the power consumption is high enough to require expensive cooling technology.

To practice basic questions and answers on all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessors Problems focuses on "Hybrid Architecture -RISC and CISC Convergence, Advantages of RISC, Design Issues of RISC Processors -2".

1. The number of CPIs(Clock Per Instruction) for an instruction of RISC processors is
- a) 0
 - b) 1
 - c) 2
 - d) 3

Answer: b

Explanation: RISC processors have unity CPI(Clock Per Instruction), which is due to the optimization of each instruction on the CPU and massive pipelining embedded in a RISC processor.

2. Which of the following is not true about RISC processors?
- a) addressing modes are less
 - b) pipelining is key for high speed
 - c) microcoding is required
 - d) single machine cycle instructions

Answer: c

Explanation: Unlike the CISC, in RISC architecture, instruction microcoding is not required.

3. The RISC processors that support variable length instructions are from
- a) Intel
 - b) Motorola
 - c) AMD
 - d) Intel and Motorola

Answer: d

Explanation: In RISC, each instruction is of the same length, so that it may be fetched in a single operation. The traditional microprocessors from Intel or Motorola support variable length instructions.

4. Which of the following is true about register windowing?
- a) chips expose 32 registers to programmer
 - b) puts demands on multiplexers
 - c) puts enormous demands on register ports
 - d) all of the mentioned

Answer: d

Explanation: The register windowing involves a mechanism where the chips expose 32 registers to the programmer at any one time. It puts enormous demands on multiplexers and register ports to make any physical register appear to be any logical register.

5. The disadvantage of register windowing is
- a) high speed
 - b) puts demands on multiplexers/register ports
 - c) consumes less cycles
 - d) doesn't handle overflow/underflow

Answer: d

Explanation: It is impossible to predict when the register file will overflow or underflow, so performance is unpredictable. It generates a software fault, which the operating system has to handle, consuming more cycles.

6. The register window is used to point the number of physical registers is
- a) infinite
 - b) that are currently used
 - c) finite
 - d) that are unused

Answer: c

Explanation: The register window only helps us to point the number of physical registers is finite.

7. Which of the following is not a stage of pipeline of a RISC processor?
- a) read registers and decode the instructions

- b) fetch instructions from registers
- c) write result into a register
- d) access an operand in data memory

Answer: b

Explanation: There are 5 stages in pipelining. They are

1. Fetch instructions from memory
2. Read registers and decode the instructions
3. Execute the instructions or calculate an address
4. Access an operand in data memory
5. Write result into a register.

8. When an instruction depends on the results of the previous instructions then

- a) error occurs
- b) software fault occurs
- c) data dependency occurs
- d) hardware fault occurs

Answer: c

Explanation: A data dependency occurs when an instruction depends on the results of the previous instructions.

9. The instructions that instruct the processor to make a decision about the next instruction to be executed are

- a) data dependency instructions
- b) branch instructions
- c) control transfer instructions
- d) none

Answer: b

Explanation: The branch instructions are those which instruct the processor to make a decision about the next instruction to be executed, depending upon whether the condition is satisfied or not.

10. The reason for which the RISC processor goes to idle state(or stall) is

- a) delay in reading information from memory
- b) poor instruction set design
- c) dependencies between instructions
- d) all of the mentioned

Answer: d

Explanation: There are a variety of reasons, including delays in reading information from memory, poor instruction set design, or dependencies between instructions for the RISC processor to remain idle.

To practice all areas of Microprocessors Problems, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Architecture of 8051".

1. The register that may be used as an operand register is

- a) Accumulator
- b) B register
- c) Data register
- d) Accumulator and B register

Answer: d

Explanation: In some instructions, the Accumulator and B register are used to store the operands.

2. The register that can be used as a scratch pad is

- a) Accumulator
- b) B register
- c) Data register
- d) Accumulator and B register

Answer: b

Explanation: B register is used to store one of the operands for multiply and divide instructions. In other instructions, it may just be used as a scratch pad.

3. The registers that contain the status information is

- a) control registers
- b) instruction registers
- c) program status word
- d) all of the mentioned

Answer: c

Explanation: The set of flags of program status word contains the status information and is considered as one of the special function registers.

4. Which of the processor's stack does not contain the top-down data structure?

- a) 8086
- b) 80286
- c) 8051
- d) 80386

Answer: c

Explanation: The 8051 stack is not a top-down data structure, like other Intel processors.

5. The architecture of 8051 consists of

- a) 4 latches
- b) 2 timer registers
- c) 4 on-chip I/O ports
- d) all of the mentioned

Answer: d

Explanation: The architecture of 8051 consists of 4 latches and driver pairs are allotted to each of the four on-chip I/O ports. It contains two 16-bit timer registers.

6. The transmit buffer of serial data buffer is a

- a) serial-in parallel-out register
- b) parallel-in serial-out register
- c) serial-in serial-out register
- d) parallel-in parallel-out register

Answer: b

Explanation: The transmit buffer of serial data buffer is a parallel-in serial-out register.

7. The receive buffer of serial data buffer is a

- a) serial-in parallel-out register
- b) parallel-in serial-out register
- c) serial-in serial-out register
- d) parallel-in parallel-out register

Answer: a

Explanation: The serial data register has two buffers. The transmit buffer is a parallel-in serial-out register and receive buffer is a parallel-in serial-out register.

8. The register that provides control and status information about counters is

- a) IP
- b) TMOD
- c) TCON
- d) PCON

Answer: b

Explanation: The registers, TMOD and TCON contain control and status information about timers/counters.

9. The register that provides control and status information about serial port is

- a) IP
- b) IE
- c) TCON

d) PCON and SCON

Answer: d

Explanation: The registers, PCON and SCON contain control and status information about serial port.

10. The device that generates the basic timing clock signal for the operation of the circuit using crystal oscillator is

- a) timing unit
- b) timing and control unit
- c) oscillator
- d) clock generator

Answer: c

Explanation: The oscillator circuit generates the basic timing clock signal for the operation of the circuit using crystal oscillator.

11. The registers that are not accessible by the user are

- a) Accumulator and B register
- b) IP and IE
- c) Instruction registers
- d) TMP1 and TMP2

Answer: d

Explanation: The arithmetic operations are performed over the operands held by the temporary registers, TMP1 and TMP2. Users cannot access these temporary registers.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Register Set of 8051".

1. Which of the following is an 8-bit register?

- a) PSW(Program Status Word)
- b) TCON(Timer Control Register)
- c) Accumulator
- d) All of the mentioned

Answer: d

Explanation: The registers, PSW, TCON and Accumulator are 8-bit registers.

2. Which of the following register can be addressed as a byte?

- a) P1
- b) SCON
- c) TMOD
- d) TCON

Answer: c

Explanation: The registers, TMOD, SP, TH0, TH1, TL0, TL1 are to be addressed as bytes.

3. Which of the following is bit-addressable register?

- a) SBUF
- b) PCON
- c) TMOD
- d) SCON

Answer: d

Explanation: The registers, accumulator, PSW, B, P0, P1, P2, P3, IP, IE, TCON and SCON are all bit-addressable registers.

4. The higher and lower bytes of a 16-bit register DPTR are represented respectively as

- a) LDPTTR and HDPTR
- b) DPTRL and DPTRH
- c) DPH and DPL
- d) HDP and LDP

Answer: c

Explanation: The registers, DPH and DPL are the higher and lower bytes of a 16-bit register DPTR.

5. The register that is used for accessing external data memory is

- a) DPH
- b) DPL
- c) DPTR
- d) NONE

Answer: c

Explanation: The Data Pointer(DPTR) is used for accessing external data memory which means that it includes both DPH and DPL.

6. Among the four groups of register banks, the number of groups that can be accessed at a time is

- a) 1
- b) 2
- c) 3
- d) all the four

Answer: a

Explanation: At a time, only one of the four register banks can be accessed.

7. The number of 8-bit registers that a register bank contain is

- a) 2
- b) 4
- c) 6
- d) 8

Answer: d

Explanation: The 32, 8-bit registers are divided into four groups of 8 registers each, called register banks.

8. If $RS1=1$, $RS0=0$, then the register bank selected is

- a) register bank 0
- b) register bank 1
- c) register bank 2
- d) register bank 3

Answer: c

Explanation: If $RS1=1$, $RS0=0$, then the register bank selected is register bank 2.

9. If $RS1=1$, $RS0=1$, then the register bank selected is

- a) register bank 0
- b) register bank 1
- c) register bank 2
- d) register bank 3

Answer: d

Explanation: If $RS1=1$, $RS0=1$, then the register bank selected is register bank 3. If $RS1=0$, $RS0=0$, then selected bank is register bank 0.

10. The PCON register consists of

- a) power mode bit
- b) power idle bit
- c) power ideal bit
- d) power down bit and idle bit

Answer: d

Explanation: The power control register, PCON consists of power down bit and idle bit which activate the power down mode and idle mode in 80C51BH.

11. The on-chip oscillator is stopped in

- a) power mode
- b) power down mode

- c) idle mode
- d) ideal mode

Answer: b

Explanation: In power down mode, the on-chip oscillator is stopped.

12. In idle mode, the device that is disabled is

- a) serial port
- b) timer block
- c) clock to CPU
- d) all of the mentioned

Answer: c

Explanation: In idle mode, the oscillator continues to run and the interrupt, serial port and timer blocks are active but the clock to the CPU is disabled.

13. The only way to terminate the power down mode is to

- a) CLEAR
- b) RESET
- c) HOLD
- d) HLT

Answer: b

Explanation: The only way to terminate the power down mode is hardware reset. The reset redefines all the SFRs but the RAM contents are left unchanged.

14. The idle mode can be terminated by

- a) PRESET
- b) CLEAR
- c) Interrupt
- d) Interrupt or reset

Answer: d

Explanation: The idle mode can be terminated with a hardware interrupt or hardware reset signal.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessors Assessment Questions and Answers focuses on "Interrupt and Stack of 8051 - 2".

1. The timer generates an interrupt, if the count value reaches to

- a) 00FFH
- b) FF00H
- c) 0FFFH
- d) FFFFH

Answer: d

Explanation: The timer is an up-counter and generates an interrupt when the count has reached FFFFH.

2. The external interrupt that has the lowest priority among the following is

- a) TF0
- b) TF1
- c) IE1
- d) NONE

Answer: c

Explanation: The order of given interrupts from high to low priority is TF0, IE1 and TF1.

3. Among the five interrupts generated by 8051, the lowest priority is given to the interrupt

- a) IE0
- b) TF1
- c) TF0
- d) RI

Answer: d

Explanation: The interrupt, RI=TI (serial port) is given the lowest priority among all the interrupts.

4. Among the five interrupts generated by 8051, the highest priority is given to the interrupt

- a) IE0
- b) TF1
- c) TF0
- d) IE1

Answer: a

Explanation: The interrupt, IE0(External INT0) is given the highest priority among all the interrupts.

5. All the interrupts are enabled using a special function register called

- a) interrupt priority register
- b) interrupt register
- c) interrupt function register
- d) interrupt enable register

Answer: d

Explanation: All the interrupts are enabled using a special function register called interrupt enable register (IE) and their priorities are programmed using another special function register called interrupt priority register(IP).

6. The number of bytes stored on the stack during one operation of PUSH or POP is

- a) 1
- b) 2
- c) 3
- d) 4

Answer: a

Explanation: As 8051 stack operations are 8-bit wide i.e. in an operation using PUSH or POP instruction, one byte of data is stored on a stack or retrieved from the stack. For implementing 16-bit operations, two 8-bit operations are cascaded.

7. The step involved in PUSH operation is

- a) increment stack by 2 and store 8-bit content to address pointed to by SP
- b) decrement stack by 1 and store 16-bit content to address pointed to by SP
- c) increment stack by 1 and store 8-bit content to address pointed to by SP
- d) store 8-bit content to address pointed to by SP and then increment stack by 1

Answer: c

Explanation: The PUSH instruction follows two steps.

1. Increment stack by 1
2. Store 8-bit content of the 8-bit address specified in the instruction to the address pointed to by SP.

8. The step involved in POP operation is

- a) decrement stack by 2 and store 8-bit content to address pointed to by SP
- b) store 16-bit content to address pointed to by SP and decrement stack by 1
- c) decrement stack by 1 and store content of top of stack to address pointed to by SP
- d) store content of top of stack to address pointed to by SP and then decrement stack by 1

Answer: d

Explanation: The POP instruction follows two steps.

1. Store the contents of top of stack pointed to by SP register to the 8-bit memory specified in the instruction.
2. Decrement stack by 1.

9. The 8051 stack is

- a) auto-decrement during PUSH operations
- b) auto-increment during POP operations
- c) auto-decrement during POP operations
- d) auto-increment during PUSH operations

Answer: d

Explanation: The 8051 stack is opposite to that in 8085 or 8086 i.e. in 8085 it is auto-decrement while in 8051 it is auto-increment during PUSH operations.

10. After reset, the stack pointer(SP) is initialized to the address of

- a) internal ROM
- b) internal RAM
- c) external ROM
- d) external RAM

Answer: b

Explanation: The stack pointer(SP) is an 8-bit register and is initialized to internal RAM address 07H after reset.

To practice all areas of Microprocessors Assessment Questions, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Interrupt and Stack of 8051 -1".

1. Which of the following is an external interrupt?

- a) INT0(active low)
- b) INT2(active low)
- c) Timer0 interrupt
- d) Timer1 interrupt

Answer: a

Explanation: INT0(active low) and INT1(active low) are two external interrupt inputs provided by 8051.

2. The interrupts, INT0(active low) and INT1(active low) are processed internally by flags

- a) IE0 and IE1
- b) IE0 and IF1
- c) IF0 and IE1
- d) IF0 and IF1

Answer: a

Explanation: The interrupts, INT0(active low) and INT1(active low) are processed internally by the flags IE0 and IE1.

3. The flags IE0 and IE1, are automatically cleared after the control is transferred to respective vector if the interrupt is

- a) level-sensitive
- b) edge-sensitive
- c) in serial port
- d) in parallel port

Answer: b

Explanation: If the interrupts are programmed as edge sensitive, the flags IE0 and IE1 are automatically cleared after the control is transferred to respective vector.

4. If the external interrupt sources control the flags IE0 and IE1, then the interrupt programmed is

- a) level-sensitive
- b) edge-sensitive
- c) in serial port
- d) in parallel port

Answer: a

Explanation: If the interrupts are programmed as level sensitive, then the flags IE0 and IE1 are controlled by external interrupt sources themselves.

5. The pulses at T0 or T1 pin are counted in

- a) timer mode
- b) counter mode
- c) idle mode

d) power down mode

Answer: b

Explanation: In counter mode, the pulses are counted at T0 or T1 pin.

6. In timer mode, the oscillator clock is divided by a prescaler

- a) (1/8)
- b) (1/4)
- c) (1/16)
- d) (1/32)

Answer: d

Explanation: In timer mode, the oscillator clock is divided by a prescaler (1/32) and then given to the timer.

7. The serial port interrupt is generated if

- a) RI is set
- b) RI and TI are set
- c) Either RI or TI is set
- d) RI and TI are reset

Answer: c

Explanation: The serial port interrupt is generated if atleast one of the two bits, RI and TI is set.

8. In serial port interrupt, after the control is transferred to the interrupt service routine, the flag that is cleared is

- a) RI
- b) TI
- c) RI and TI
- d) None

Answer: d

Explanation: In serial port interrupt, after the control is transferred to the interrupt service routine, neither of the flags are cleared.

9. The atleast number of machine cycles for which the external interrupts that are programmed level-sensitive should remain high is

- a) 1
- b) 2
- c) 3
- d) 0

Answer: b

Explanation: The external interrupts, programmed level-sensitive should remain high for atleast 2 machine cycles.

10. If the external interrupts are programmed edge sensitive, then they should remain high for atleast

- a) 0 machine cycle
- b) 2 machine cycles
- c) 1 machine cycle
- d) 3 machine cycles

Answer: c

Explanation: If the external interrupts are programmed edge sensitive, then they should remain high for atleast one machine cycle and low for atleast one machine cycle, for being sensed.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Addressing Modes of 8051".

1. Which of the following is not an addressing mode of 8051?

- a) register instructions
- b) register specific instructions

- c) indexed addressing
- d) none

Answer: d

Explanation: The six addressing modes of 8051 are

1. Direct addressing
2. Indirect addressing
3. Register instructions
4. Register specific(Register Implicit) instructions
5. Immediate mode
6. Indexed addressing.

2. The symbol, 'addr 16' represents the 16-bit address which is used by the instructions to specify the

- a) destination address of CALL
- b) source address of JUMP
- c) destination address of call or jump
- d) source address of call or jump

Answer: c

Explanation: The symbol, 'addr 16' represents the 16-bit destination address which is used by the LCALL or LJMP instruction to specify the call or jump destination address, within 64 Kbytes program memory.

3. The storage of addresses that can be directly accessed is

- a) external data RAM
- b) internal data ROM
- c) internal data RAM and SFRS
- d) external data ROM and SFRS

Answer: c

Explanation: Only internal data RAM and SFRS can be directly addressed in direct addressing mode.

4. The address register for storing the 16-bit addresses can only be

- a) stack pointer
- b) data pointer
- c) instruction register
- d) accumulator

Answer: b

Explanation: The address register for storing the 16-bit addresses can only be data pointer.

5. The address register for storing the 8-bit addresses can be

- a) R0 of the selected bank of register
- b) R1 of the selected bank of register
- c) Stack pointer
- d) All of the mentioned

Answer: d

Explanation: The registers R0 and R1 of the selected bank of registers or stack pointer can be used as address registers for storing the 8-bit addresses.

6. The instruction, ADD A, R7 is an example of

- a) register instructions
- b) register specific instructions
- c) indexed addressing
- d) none

Answer: a

Explanation: In register instructions addressing mode, operands are stored in the registers R0-R7 of the selected register bank. One of these registers is specified in the instruction.

7. The addressing mode, in which the instructions has no source and destination operands is

- a) register instructions

- b) register specific instructions
- c) direct addressing
- d) indirect addressing

Answer: b

Explanation: In register specific instructions addressing mode, the instructions don't have source and destination operands. Some of the instructions always operate only on a specific register.

8. The instruction, RLA performs
- a) rotation of address register to left
 - b) rotation of accumulator to left
 - c) rotation of address register to right
 - d) rotation of accumulator to right

Answer: b

Explanation: The instruction, RLA rotates accumulator left.

9. The instruction, ADD A, #100 performs
- a) 100(decimal) is added to contents of address register
 - b) 100(decimal) is subtracted from the accumulator
 - c) 100(decimal) is added to contents of an accumulator
 - d) none

Answer: c

Explanation: Immediate data 100(decimal) is added to the contents of the accumulator.

10. In which of these addressing modes, a constant is specified in the instruction, after the opcode byte?
- a) register instructions
 - b) register specific instructions
 - c) direct addressing
 - d) immediate mode

Answer: d

Explanation: In immediate mode, an immediate data, i.e. a constant is specified in the instruction, after the opcode byte.

11. The only memory which can be accessed using indexed addressing mode is
- a) RAM
 - b) ROM
 - c) Main memory
 - d) Program memory

Answer: d

Explanation: Only program memory can be accessed using the indexed addressing mode.

12. The data address of look-up table is found by adding the contents of
- a) accumulator with that of program counter
 - b) accumulator with that of program counter or data pointer
 - c) data register with that of program counter or accumulator
 - d) data register with that of program counter or data pointer

Answer: b

Explanation: The look-up table data address is found out by adding the contents of register accumulator with that of the program counter or data pointer.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "8051 Instruction Set -1".

1. Which of the following is not an instruction of 8051 instructions?
- a) arithmetic instructions
 - b) boolean instructions
 - c) logical instructions

d) none

Answer: d

Explanation: The 8051 instructions are categorized as

1. Data transfer instructions
2. Arithmetic instructions
3. Logical instructions
4. Boolean instructions
5. Control transfer instructions.

2. The operations performed by data transfer instructions are on

- a) bit data
- b) byte data
- c) 16-bit data
- d) all of the mentioned

Answer: d

Explanation: The data transfer instructions implement a bit, byte, 16-bit data transfer operations between the SRC(source) and DST(destination) operands.

3. Which of the following is true while executing data transfer instructions?

- a) program counter is not accessible
- b) restricted bit-transfer operations are allowed
- c) both operands can be direct/indirect register operands
- d) all of the mentioned

Answer: c

Explanation: In data transfer instructions,

1. Program counter is not accessible.
2. Restricted bit-transfer operations are allowed.
3. Both operands can be direct/indirect register operands.
4. BOTH operands can be internal direct data memory operands.

4. The logical instruction that affects the carry flag during its execution is

- a) XRL A;
- b) ANL A;
- c) ORL A;
- d) RLC A;

Answer: d

Explanation: The logical instructions that doesn't affect the carry flag are, ANL, ORL and XRL. The logical instructions that affect the carry flag during its execution are RL, RLC, RRC and RR.

5. The instruction that is used to complement or invert the bit of a bit addressable SFR is

- a) CLR C
- b) CPL C
- c) CPL Bit
- d) ANL Bit

Answer: c

Explanation: The instruction, CPL Bit is used to complement or invert the bit of a bit addressable SFR or RAM.

6. The instructions that change the sequence of execution are

- a) conditional instructions
- b) logical instructions
- c) control transfer instructions
- d) data transfer instructions

Answer: c

Explanation: The control transfer instructions transfer the control of execution or change the sequence of execution conditionally or unconditionally.

7. The control transfer instructions are divided into
- a) explicit and implicit control transfer instructions
 - b) conditional and unconditional control transfer instructions
 - c) auto control and self control transfer instructions
 - d) all of the mentioned

Answer: b

Explanation: The control transfer instructions are divided into conditional and unconditional control transfer instructions.

8. The conditional control transfer instructions check a bit condition which includes any bit of
- a) bit addressable RAM
 - b) bit addressable SFRs
 - c) content of accumulator
 - d) all of the mentioned

Answer: d

Explanation: The conditional control transfer instructions check a bit condition which includes any bit of bit addressable RAM or bit addressable SFRs or content of accumulator for transferring the control to the specified jump location.

9. All conditional jumps are
- a) absolute jumps
 - b) long jumps
 - c) short jumps
 - d) none

Answer: c

Explanation: All conditional jumps are short jumps.

10. The first byte of a short jump instruction represents
- a) opcode byte
 - b) relative address
 - c) opcode field
 - d) none

Answer: a

Explanation: The short jump instruction has two byte instruction. The first byte represents opcode byte and second byte represents an 8-bit relative address.

11. In logical instructions, the immediate data can be an operand for
- a) increment operation
 - b) decrement operation
 - c) single operand instruction
 - d) none

Answer: d

Explanation: In logical instructions, the immediate data can't be an operand for increment/decrement or any other single operand instruction.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessors Questions and Answers for Aptitude test focuses on "8051 Instruction Set -2".

1. If the most significant bit of relative address byte is 1, then the short jump instruction is
- a) forward jump
 - b) back jump
 - c) either forward or back jump
 - d) none

Answer: b

Explanation: If the most significant bit of relative address byte is 1, then the short jump instruction is back jump, else it is considered as forward jump.

2. The first byte of an absolute jump instruction consists of
- a) 3 LSBs of opcode and 5 MSBs of 11-bit address
 - b) 5 MSBs of opcode and 3 LSBs of 11-bit address
 - c) 6 MSBs of opcode and 1 LSB of 11-bit address
 - d) 5 LSBs of opcode and 3 MSBs of 11-bit address

Answer: d

Explanation: The first byte of an absolute jump instruction consists of 5 LSBs of opcode and 3 MSBs of 11-bit address. The next byte carries the least significant 8 bits of the 11-bit address.

3. The third byte of the long jump instruction is
- a) opcode
 - b) 5 LSBs of opcode
 - c) higher byte of jump location or subroutine
 - d) lower byte of jump location or subroutine

Answer: c

Explanation: The third byte of the long jump instruction is a higher byte of jump location or subroutine.

4. The absolute jump instruction is intended mainly for a jump within a memory space of
- a) 2 bytes
 - b) 2 Kbytes
 - c) 2 Mbytes
 - d) none

Answer: b

Explanation: The absolute jump instruction is intended mainly for a jump within a memory space of 2 Kbytes.

5. The LJMP instruction is very useful in programming in the external code memory space of
- a) 32 MB
 - b) 64 MB
 - c) 32 KB
 - d) 64 KB

Answer: d

Explanation: The LJMP instruction is very useful in programming in the external code memory space of 64 KB.

6. Which of the following is not an unconditional control transfer instruction?
- a) JMP
 - b) RET
 - c) JNC
 - d) CALL

Answer: c

Explanation: The instructions, JMP, RET, RETI, CALL are the unconditional control transfer instructions.

7. The conditional control transfer instructions use
- a) status flags
 - b) bits of bit addressable RAM
 - c) SFRs termed bit
 - d) all of the mentioned

Answer: d

Explanation: The conditional control transfer instructions use status flags or bits of bit addressable RAM or SFRs termed bit.

8. Which of the following is not a conditional control transfer instruction?
- a) JC
 - b) JBC
 - c) JNC
 - d) NONE

Answer: d

Explanation: The instructions, JC, JBC, JNC, JB and JNB are the conditional control transfer instructions.

9. The mnemonic used to perform a subtraction of source with an 8-bit data and jumps to specified relative address if subtraction is non-zero is

- a) DJNZ
- b) CJNE
- c) JZ
- d) JNC

Answer: b

Explanation: The CJNE instruction perform a subtraction of source with an 8-bit data and jumps to specified relative address only if the result of the subtraction is non-zero, else continues to the next instruction.

10. The mnemonic, JNB is used to jump to the specified relative address only if

- a) specified bit=1
- b) specified bit=0
- c) specified bit is non-recursive
- d) none

Answer: a

Explanation: The mnemonic, JNB is used to jump to the specified relative address only if specified bit=1, else continues to the next instruction.

11. The type of operand that is not allowed to use in boolean instructions of 8051 is

- a) direct register operands
- b) indirect register operands
- c) immediate bit
- d) none

Answer: c

Explanation: In boolean instructions, the immediate bit is not allowed as an operand.

12. In boolean instructions, the flag that is the only allowed destination operand for two operand instructions is

- a) overflow flag
- b) underflow flag
- c) auxiliary flag
- d) carry flag

Answer: d

Explanation: Carry flag(C) is the only allowed destination operand for two operand instructions in boolean instructions.

To practice all areas of Microprocessors for Aptitude test, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Interfacing With 8051 Ports -1".

1. Which of the following is not one of the SFR addresses of the ports of 8051?

- a) 80H
- b) 90H
- c) A0H
- d) NONE

Answer: d

Explanation: The SFR addresses of the ports P0, P1, P2 and P3 are 80H, 90H, A0H and B0H respectively.

2. Each port line of a port can individually source a current of upto

- a) 0.2 mA
- b) 0.25 mA
- c) 0.5 mA

d) 0.75 mA

Answer: c

Explanation: Each port line of a port can individually source a current of upto 0.5 mA.

3. Each port line of a port can individually sink a current of upto

- a) 2 mA
- b) 8 mA
- c) 5 mA
- d) 1 mA

Answer: b

Explanation: Each port line of a port can individually sink a current of upto 8 mA.

4. The number of TTL inputs that can be sinked by the port 0 when a logic 0 is sent to a port line as an output port is

- a) 2
- b) 4
- c) 6
- d) 8

Answer: d

Explanation: When a logic 0 is sent to a port line as an output port, it can sink 8 LS TTL inputs. Port 0 is used as data bus during external interfacing whenever required.

5. The open drain bidirectional (input or output) port with internal pullups is

- a) Port 0
- b) Port 1
- c) Port 2
- d) Port 3

Answer: a

Explanation: Port 0 is an open drain bidirectional (input or output) port with internal pullups. Port 1, Port 2, Port 3 are 8-bit bidirectional ports.

6. The port that can source or sink 4 LS TTL inputs when being used as an output port on each of its line is

- a) Port 1
- b) Port 2
- c) Port 3
- d) all of the mentioned

Answer: d

Explanation: The ports P1, P2 and P3 can source or sink 4 LS TTL inputs when being used as an output port on each of its line.

7. The port that will source a current of 500 micro amperes when being used as input ports is

- a) 0.5 mA
- b) 0.25 mA
- c) 250 micro amperes
- d) 500 micro amperes

Answer: d

Explanation: Port 3 pins which are externally pulled low when being used as input pins will source current of 500 micro amperes.

8. If the EA(active low) signal is grounded then the execution

- a) directly start from main memory
- b) directly start from 16 bit address in main memory
- c) directly start from 16 bit address in program memory
- d) directly start from RAM

Answer: c

Explanation: For interfacing external program memory, EA(active low) pin must be grounded. If the EA(active low) signal is grounded then the execution will start directly from the 16-bit address 0000H in external program memory.

9. When the port lines of a port are to be used as input lines then the value that must be written to the port address is

- a) F0H
- b) 0FH
- c) FFH
- d) 00H

Answer: c

Explanation: When the port lines of a port are to be used as input lines then 'FF'H must be written to the port address.

10. Port 1 lines are used during programming of

- a) external EPROM and EEPROM
- b) external ROM and RAM
- c) internal ROM and RAM
- d) internal EPROM and EEPROM

Answer: d

Explanation: Port 1 lines are used as lower byte of 16-bit address bus during programming of internal EPROM or EEPROM.

11. The configuration in which each LED receives operating current of 8 mA from power supply while the port lines sink the current on each port line is

- a) common port configuration
- b) common anode configuration
- c) common cathode configuration
- d) none of the mentioned

Answer: b

Explanation: The common anode configuration is preferred to that of other configurations as in common anode configuration, each LED receives operating current of 8 mA from power supply while the port lines sink the current on each port line.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessors Questions and Answers for Campus interviews focuses on "Interfacing With 8051 Ports -2".

1. If EA(active low) signal =1, then the execution starts from

- a) internal EPROM
- b) flash RAM
- c) internal EPROM or flash RAM
- d) none

Answer: c

Explanation: If EA(active low) signal =1, then the execution starts from an internal EPROM or flash RAM address 000H, can continue upto FFFH address and then for higher addresses it will go into external memory.

2. The pin that is grounded for interfacing external EPROM is

- a) EA(active low)
- b) PSEN(active low)
- c) OE(active low)
- d) All of the mentioned

Answer: a

Explanation: The EA(active low) pin is grounded for interfacing external EPROM. The PSEN(active low) is used for interfacing EPROM i.e. it acts as an OE(active low) input to EPROM.

3. The step that is involved in the procedure of memory interfacing with 8051 is

- a) data bus is connected to data lines of memory chips
- b) PSEN(active low) is connected to OE(active low) of EPROM chips
- c) writing address map of memory chip in bit form
- d) all of the mentioned

Answer: d

Explanation: The procedure of memory interfacing with 8051 includes, data bus connection to data lines of memory chips, PSEN(active low) connected to OE(active low) of EPROM chips and writing address map of memory chip in bit form.

4. The device that is used for deriving chip select signals is

- a) Logic gates
- b) Multiplexers
- c) PLAs and EPROMs
- d) All of the mentioned

Answer: d

Explanation: The logic gates and multiplexers are most commonly used for deriving chip select signals. The advanced circuits like PLAs and EPROMs are also used for deriving chip select signals.

5. For deriving chip selects of isolated memory or IO devices, the gates that are traditionally used are

- a) NOR and NAND
- b) NAND and NOT
- c) NOT and NOR
- d) AND, OR and NOT

Answer: b

Explanation: For deriving chip selects of isolated memory or IO devices, the NAND and NOT gates are traditionally used.

6. The current that is required for a LED for an appropriate glow is

- a) 6-8 mA
- b) 4-6 mA
- c) 8-10 mA
- d) 10-12 mA

Answer: c

Explanation: For appropriate glow, a LED typically requires 8-10 mA with around 1.6 Volts.

7. The maximum current that can be sunked totally by all the ports of 8051 is

- a) 61 mA
- b) 81 mA
- c) 91 mA
- d) 71 mA

Answer: d

Explanation: All the ports together (4 ports) should not be made to sink more than 71 mA.

8. The number of LEDs that can be connected to a port of 8051, if all are expected to glow simultaneously is

- a) 6
- b) 8
- c) 10
- d) 12

Answer: b

Explanation: If 8 LEDs are connected to a port of 8051, and if all are expected to glow simultaneously, the total current sunked by the 8051 port will be $8 \times 8 = 64$ mA (since min voltage for an LED to glow = 8 mA) which is less than the maximum 71 mA.

9. Which is true in interfacing 7 segment code display?

- a) transmitted by second port
- b) display is selected by third port
- c) display is selected by second port
- d) none of the mentioned

Answer: c

Explanation: The 7-segment code of a digit is transmitted by the first port and the display is

selected by second port. As soon as the display is selected by the second port, the digit starts glowing on that display position.

10. After the display is selected by second port, then the digit (LED) glows for a duration of
- a) 5 msec
 - b) 10 msec
 - c) 2 msec
 - d) 6 msec

Answer: a

Explanation: The unit(LED) glows for a duration of 5 msec.

11. The number of scans of the complete 8-digit display that can be carried out in one second is

- a) 15
- b) 25
- c) 35
- d) 55

Answer: b

Explanation: Starting from either right most or left most digit, every digit glows for 5 msec one by one. Thus one scan of the 8 digit display requires 40 msec. Thus in one second, 25 scans of the complete 8-digit display can be carried out.

12. To convert its current output into a voltage, the DAC 0808 is connected with

- a) Transistor(BJT) externally
- b) FET externally
- c) OPAMP externally
- d) OPAMP internally

Answer: c

Explanation: the DAC 0808 is connected with OPAMP externally, to convert its current output into voltage.

To practice all areas of Microprocessors for Campus Interviews, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Interrupt Structure of 8051".

1. The external interrupts of 8051 can be enabled by

- a) 4 LSBs of TCON register
- b) Interrupt enable
- c) priority register
- d) all of the mentioned

Answer: d

Explanation: The external interrupts namely INT0(active low) and INT1(active low) can be enabled and programmed using the least significant four bits of TCON register and the Interrupt enable and priority registers.

2. The bits that control the external interrupts are

- a) ET0 and ET1
- b) ET1 and ET2
- c) EX0 and EX1
- d) EX1 and EX2

Answer: c

Explanation: The bits, EX0 and EX1 individually control the external interrupts, INT0(active low) and INT1(active low). If INT0(active low) and INT1(active low) interrupts are to be enabled then the bits EX0 and EX1 must be set respectively.

3. EA bit is used to

- a) enable or disable external interrupts
- b) enable or disable internal interrupts
- c) enable or disable all the interrupts

d) none of the mentioned

Answer: c

Explanation: Using EA bit, all the interrupts can be enabled or disabled. Using the individual respective bit, the respective interrupt can be enabled or disabled.

4. The number of priority levels that each interrupt of 8051 have is

- a) 1
- b) 2
- c) 3
- d) 4

Answer: b

Explanation: Each interrupts level of 8051 can have two levels of priority namely level 0 and level 1. Level 1 is considered as a higher priority level compared to level 0.

5. The priority level of an interrupt of 8051 for which SI(serial interrupt) interrupt is programmed is

- a) level 0
- b) level 1
- c) level 0 or level 1
- d) none

Answer: b

Explanation: SI interrupt is programmed for level 1 priority.

6. The interrupt bit that when set works at level 1, and otherwise at level 0 is

- a) PT1
- b) PT0
- c) PX1
- d) All of the mentioned

Answer: d

Explanation: The bits, PT1, PT0, PX0 and PX1 when set, work at level 1, otherwise at level 0.

7. All the interrupts at level 1 are polled in the second clock cycle of the

- a) forth T state
- b) fifth T state
- c) third T state
- d) none

Answer: b

Explanation: All the interrupts at level 1 are polled or sensed in the second clock cycle of the fifth T state or 9th clock cycle out of 12 clock cycles. Then all the interrupts at level 0 are also polled in the same cycle.

8. The minimum duration of the active low interrupt pulse for being sensed without being lost must be

- a) greater than one machine cycle
- b) equal to one machine cycle
- c) greater than 2 machine cycles
- d) equal to 2 machine cycles

Answer: b

Explanation: The minimum duration of the active low interrupt pulse should be equal to the duration of one machine cycle for being sensed, else it will be lost.

9. If two interrupts, of higher priority and lower priority occur simultaneously, then the service provided is for

- a) interrupt of lower priority
- b) interrupt of higher priority
- c) lower & higher priority interrupts
- d) none of the mentioned

Answer: b

Explanation: If two interrupts, occur simultaneously, then the one with higher priority level and

early polling sequence will receive service. The other one with lower priority may get lost there, as there is no mechanism for storing the interrupt requests.

10. For an interrupt to be guaranteed served it should have duration of

- a) one machine cycle
- b) three machine cycles
- c) two machine cycles
- d) four machine cycles

Answer: c

Explanation: For an interrupt to be guaranteed served it should have duration of two machine cycles.

11. The service to an interrupt will be delayed if it appears during the execution of

- a) RETI instruction
- b) Instruction that writes to IE register
- c) Instruction that writes to IP register
- d) All of the mentioned

Answer: d

Explanation: The service to an interrupt will be delayed if it appears during the execution of RETI instruction or the instruction that writes to IE/IP registers.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Power Control Register".

1. The power control register is

- a) used for power saving during idle state
- b) used for eventual power off to 8051 chip
- c) non-bit addressable register
- d) all of the mentioned

Answer: d

Explanation: The power control register is used for power saving during idle state of the microcontroller and eventual power off to the microcontroller chip. It has SMOD bit which is used to double the baud rate.

2. The state of signals in idle mode is

- a) ALE is high
- b) PSEN is high
- c) PSEN(active low) is high
- d) ALE and PSEN(active low) are high

Answer: d

Explanation: ALE and PSEN(active low) remain high in Idle mode.

3. To come out of idle mode, the external interrupt that is enabled is

- a) SI(serial)
- b) INT0
- c) INT1
- d) All of the mentioned

Answer: d

Explanation: To come out of idle mode, any external interrupt that is enabled like SI(Serial), INT0 and INT1.

4. The microcontroller enters into power down mode when

- a) SMOD bit of PCON is set
- b) GF1 bit of PCON is set
- c) PD bit of PCON is set
- d) GF2 bit of PCON is set

Answer: c

Explanation: If the PD bit of PCON register is set, it enters power down mode.

5. The clock signal is disabled to all parts of 8051 in
- a) normal mode
 - b) idle mode
 - c) power down mode
 - d) addressing mode

Answer: c

Explanation: In power down mode, the clock signal to all parts of 8051 chip is disabled.

6. During power down to save battery, the supply voltage can be reduced to a value of
- a) 4 volts
 - b) 2 volts
 - c) 8 volts
 - d) 1 volt

Answer: b

Explanation: The supply voltage can be reduced to a value of around 2 volts, during power down to save battery.

7. The signal that only pulls the microcontroller(8051) out of the power down mode is
- a) CLEAR
 - b) LEAVE
 - c) RESET
 - d) EXIT

Answer: c

Explanation: Only Reset signal can pull 8051 out of the power down mode.

8. The state of signals in power down mode is
- a) ALE is high
 - b) PSEN is low
 - c) ALE and PSEN(active low) are high
 - d) ALE and PSEN(active low) are low

Answer: d

Explanation: ALE and PSEN(active low) remain low in power down mode of 8051.

9. In power down mode,
- a) Port pins maintain their logic levels
 - b) SFRs maintain their logic levels
 - c) Clock signal is disabled
 - d) All of the mentioned

Answer: d

Explanation: In power down mode, the clock signal is disabled and all the port pins and respective SFRs maintain their logic levels.

10. The SMOD bit is used to
- a) decrease the baud rate by 2
 - b) increase the baud rate by 4
 - c) increase the baud rate by 2
 - d) triple the baud rate

Answer: c

Explanation: The SMOD bit is used to double the baud rate.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on "Serial Communication Unit".

1. The serial communication is
- a) cheaper communication
 - b) requires less number of conductors
 - c) slow process of communication
 - d) all of the mentioned

Answer: d

Explanation: The serial communication requires less number of conductors and thus it is cheaper. It is slow as the bits are transmitted one by one along with start, stop and parity bits.

2. The serial communication is used for

- a) short distance communication
- b) long distance communication
- c) short and long distance communication
- d) communication for a certain range of distance

Answer: b

Explanation: Serial communication is more popular for communication over longer distances as it requires less number of conductors.

3. The mcs 51 architecture supports

- a) serial transmission and reception
- b) simultaneous transmission and reception
- c) transmission and reception of data using serial communication interface
- d) all of the mentioned

Answer: d

Explanation: The mcs 51 architecture supports simultaneous transmission and reception of binary data byte by byte i.e. full duplex mode of communication. It supports serial transmission and reception of data using standard serial communication interface and baud rates.

4. The number of bits transmitted or received per second is defined as

- a) transmission rate
- b) reception rate
- c) transceiver rate
- d) baud rate

Answer: d

Explanation: Here, baud rate can be defined as the number of bits transmitted or received per second.

5. The task of converting the byte into serial form and transmitting it bit by bit along with start, stop and parity bits is carried out by

- a) reception unit
- b) serial communication unit
- c) transmission unit
- d) all of the mentioned

Answer: c

Explanation: the serial communication unit consists of transmission unit and reception unit. The task of converting the byte into serial form and transmitting it bit by bit along with start, stop and parity bits is carried out by transmission unit.

6. The transmission unit does not require assistance from processor if once a byte for transmission is written to

- a) SCON register
- b) SBUF register
- c) SFR address
- d) Any of the mentioned

Answer: b

Explanation: once a byte for transmission is written to the serial buffer(SBUF) register, the transmission unit does not require assistance from a processor.

7. The common unit shared by the receiver unit and transmission unit of serial communication unit is

- a) SCON(Serial Port Control) Register
- b) SBUF(Serial Buffer) register
- c) 8-bit serial data interface
- d) All of the mentioned

Answer: d

Explanation: The transmission unit and receiver unit both are controlled by using a common SCON(Serial Port Control) Register. Also both units share a common serial buffer(SBUF) register which is a common 8-bit serial data interface.

8. During serial reception, the buffer that receives serial bits and converts to a byte is

- a) receive buffer 0
- b) receive buffer 1
- c) receive buffer 2
- d) none

Answer: b

Explanation: During serial reception, the receive buffer 1 receives serial bits and converts to a byte, it then transfers the received parallel byte in receive buffer 2.

9. If SM0=1, SM1=0, then the transceiver selected is

- a) 8-bit synchronous
- b) 9-bit synchronous
- c) 8-bit asynchronous
- d) 9-bit asynchronous

Answer: d

Explanation: If SM0=1, SM1=0, then the 9-bit asynchronous transceiver is selected.

10. If the microcontroller is expected to communicate in a multiprocessor system, then the required condition is

- a) SM0 is set
- b) SM1 is set
- c) SM2 is set
- d) REN is set

Answer: c

Explanation: The bit, SM2 is set if the microcontroller is expected to communicate in a multiprocessor system.

11. In mode 2, the baud rate depends only on

- a) SMOD bit
- b) SCON bit
- c) Oscillator clock frequency
- d) SMOD bit and oscillator clock frequency

Answer: d

Explanation: In mode 2, the baud rate depends only on SMOD bit and oscillator clock frequency.

12. The mode that offers the most secured parity enabled data communication at lower baud rates is

- a) mode 2
- b) mode 1
- c) mode 0
- d) all of the mentioned

Answer: a

Explanation: The mode 3 offers the most secured parity enabled data communication at lower baud rates of mode 1.

To practice all areas of Microprocessors, [here is complete set of 1000+ Multiple Choice Questions and Answers](#).