Realtek Ameba1 DEV01 User Manual

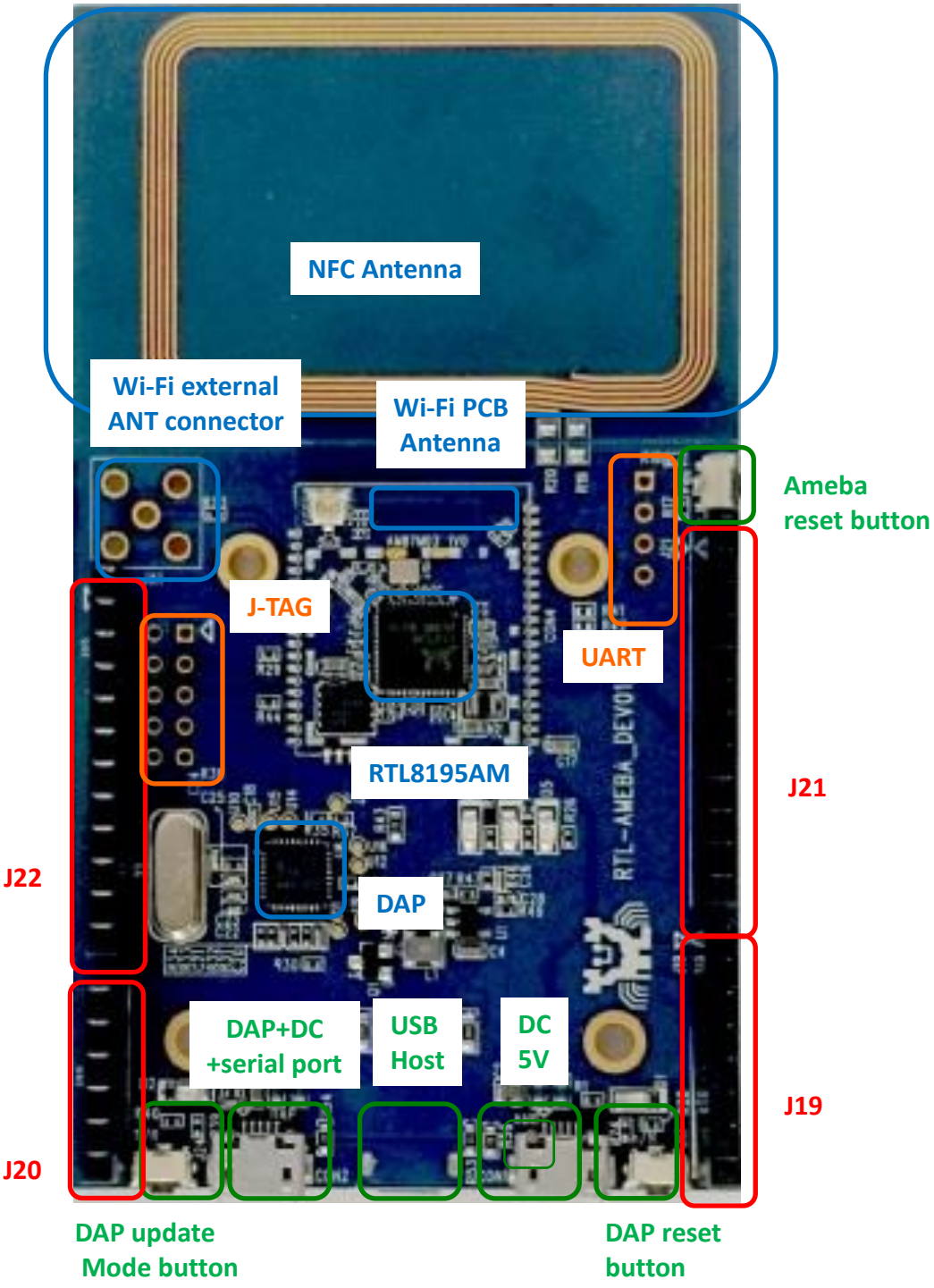
This document define pin out of Ameba DEV.

Version 1.3

Table of Contents

1 Hardware block diagram

- IC: RTL8195AM
- DEV: RTL-AMEBA_DEV01



2 System requirements

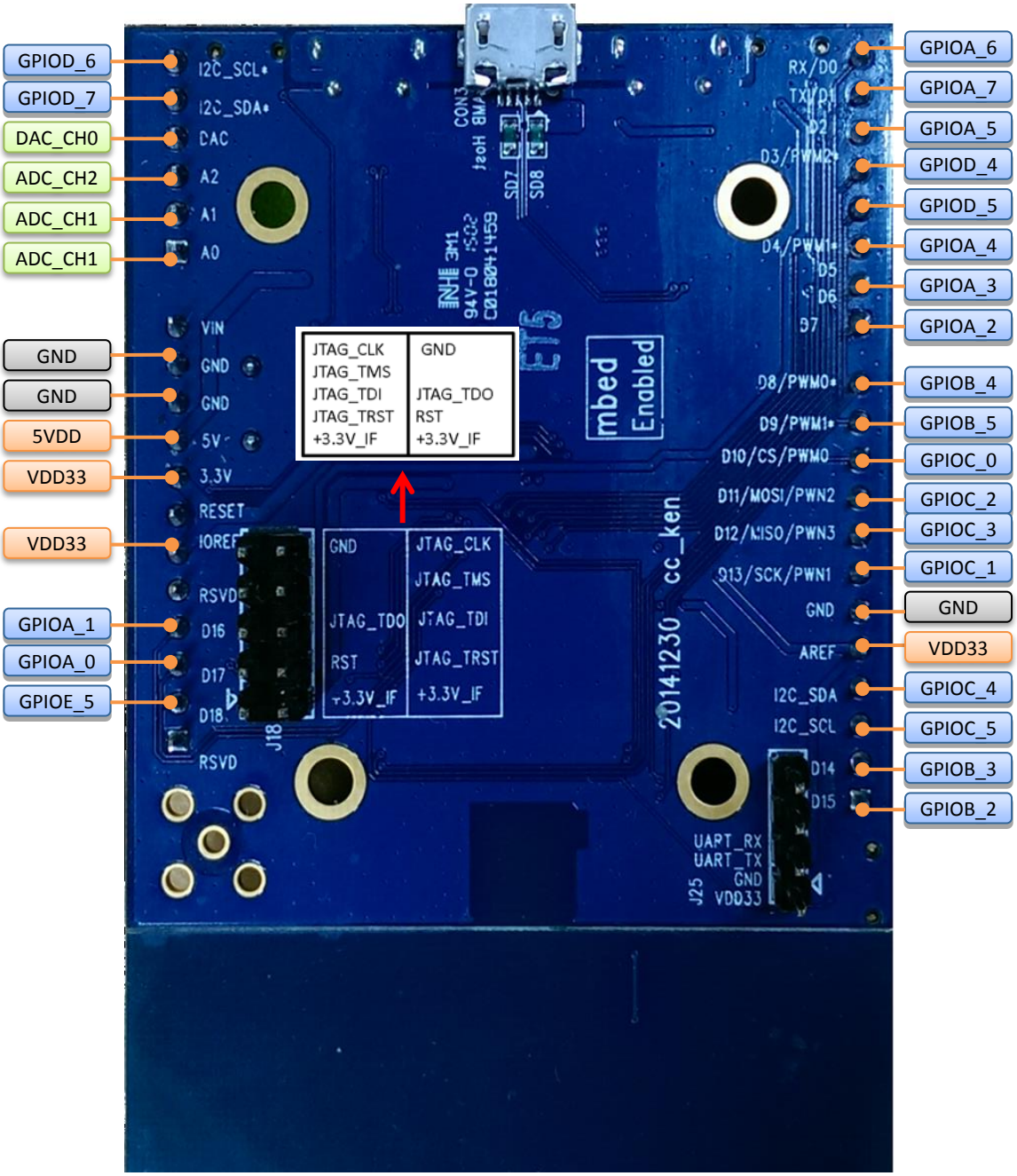
- Windows PC (XP, Vista, 7)
- USB type A to Micro-B USB cable x 1
- RS-232 to UART board(debug) x 1, JTAG cable x1 (option)

3 Pin out reference

3.1 Pin out table

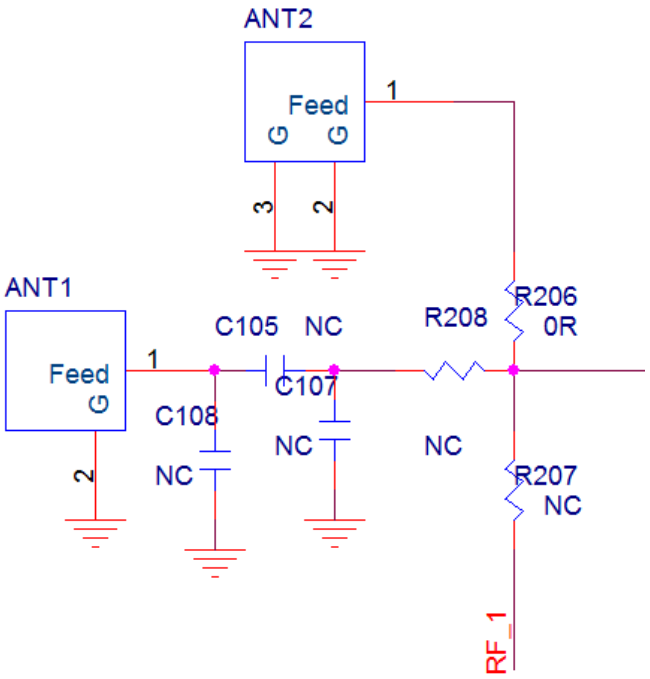
Con	DEV name	Pin	Net name	Con	DEV name	Pin	Net name
J20	I2C_SCL*	6	GPIOD_6	J19	RX/D0	8	GPIOA_6
	I2C_SDA*	5	GPIOD_7		TX/D1	7	GPIOA_7
	DAC	4	DAC_CH0		D2	6	GPIOA_5
	A2	3	ADC_CH2		D3/PWM2*	5	GPIOD_4
	A1	2	ADC_CH1		D4/PWM1*	4	GPIOD_5
	A0	1	ADC_CH1		D5	3	GPIOA_4
					D6	2	GPIOA_3
					D7	1	GPIOA_2
Con	**DEV name**	**Pin**	**Net name**	**Con**	**DEV name**	**Pin**	**Net name**
sJ22	VIN	12	NC	J21	D8/PWM0*	12	GPIOB_4
	GND	11	GROUND		D9/PWM1*	11	GPIOB_5
	GND	10	GROUND		D10/CS/PWM0	10	GPIOC_0
	5V	9	5VDD		D11/MOSI/PWM2	9	GPIOC_2
	3.3V	8	VDD33		D12/MISO/PWM3	8	GPIOC_3
	RESET	7	NC		D13/SCK/PWM1	7	GPIOC_1
	IOREF	6	VDD33		GND	6	GND
	RSVD	5	NC		AREF	5	VDD33
	D16	4	GPIOA_1		I2C_SDA	4	GPIOC_4
	D17	3	GPIOA_0		I2C_SCL	3	GPIOC_5
	D18	2	GPIOE_5		D14	2	GPIOB_3
	RSVD	1	NC		D15	1	GPIOB_2

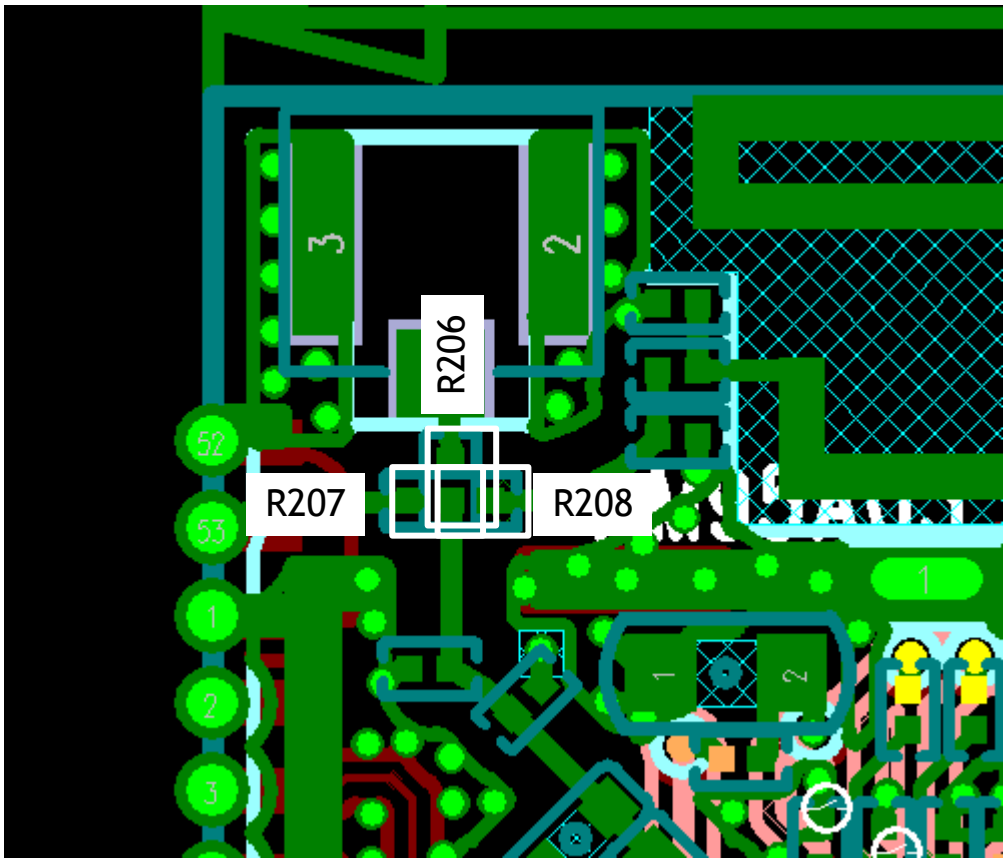
3.2 Pin out reference



4 Antenna hardware setup

- I-PEX/U.FL connector: R206
- External antenna: R207
- PCB antenna: R208





5 Peripherals support

- Debug UART: GPIOB_[0..1]
- JTAG: GPIOE_[0..4]
- UART
- I2C / I2S/SPI
- PWM/PCM

5.1 Reference setup

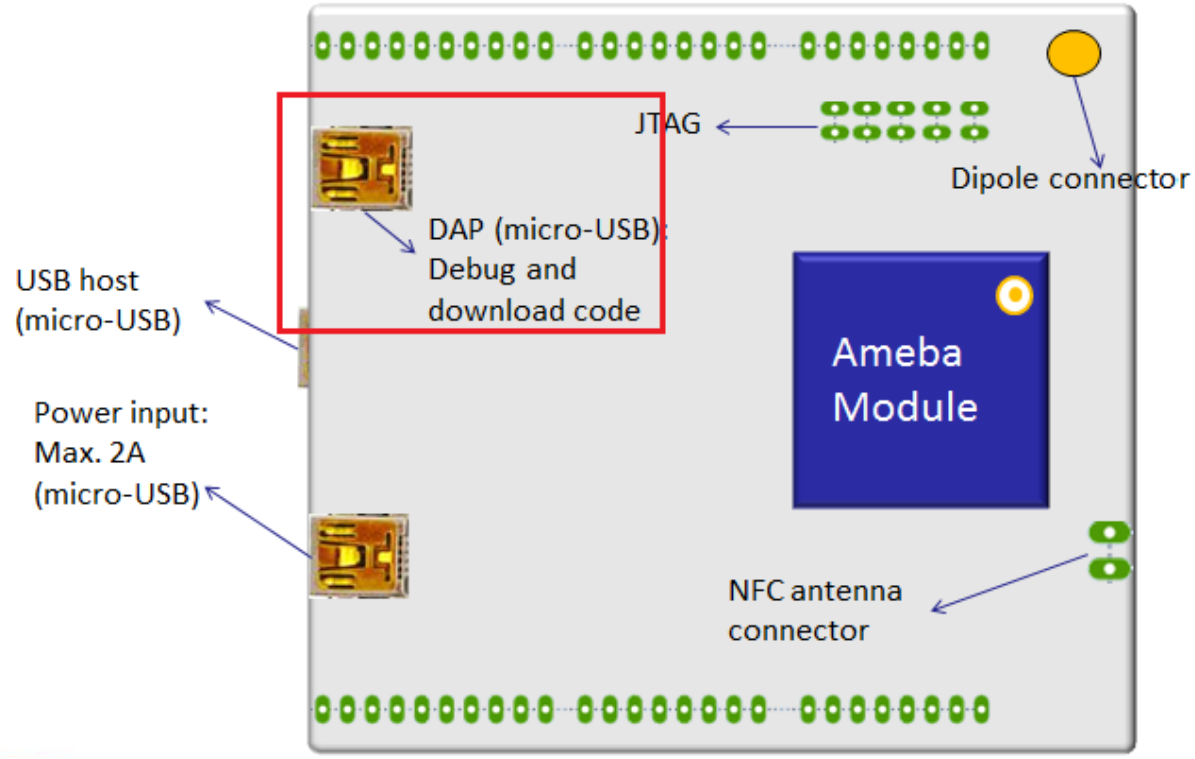
PIN name	JTAG	UART Funtion	I2C Group	SPI Group	I2S GROUP	PCM Group	WL_LED0	PWM	WKDT	GPIO_INT
GPIOA_0		UART2_IN		SPI1_MISO						GPIO_INT
GPIOA_1		UART2_CTS		SPI1_MOSI						GPIO_INT
GPIOA_2		UART2_RTS		SPI1_CLK						
GPIOA_3		UART0_RTS			SPI					
GPIOA_4		UART2_OUT		SPI1_CS						
GPIOA_5		UART0_CTS							WKDT0	
GPIOA_6		UART0_IN								
GPIOA_7		UART0_OUT								
GPIOB_0		UART_LOG_OUT								
GPIOB_1		UART_LOG_IN					WL_LED0			
GPIOB_2			I2C3_SCL							
GPIOB_3	Debug console		I2C3_SDA							GPIO_INT
GPIOB_4							WL_LED0	PWM0		GPIO_INT
GPIOB_5			I2C				WL_LED0	PWM1		
GPIOC_0		UART0_IN		SPI0_CS0	I2S1_WS	PCM1_SYNC		PWM0		
GPIOC_1		UART0_CTS		SPI0_CLK	I2S1_CLK	PCM1_CLK		PWM1		GPIO_INT
GPIOC_2		UART0_RTS		SPI0_MOSI	I2S1_SD_TX	PCM1_OUT		PWM2	PWM	
GPIOC_3		UART0_OUT		SPI0_MISO	I2S1_MCK	PCM1_IN		PWM3		GPIO_INT
GPIOC_4			I2C1_SDA	SPI0_CS1	I2S1_SD_RX					GPIO_INT
GPIOC_5			I2C1_SCL	SPI0_CS2		I2S				GPIO_INT
GPIOD_4		UART2_IN	I2C0_SDA	SPI1_CS		PCM1_SYNC		PWM0		GPIO_INT
GPIOD_5	JTAG	UART2_CTS	I2C0_SCL	SPI1_CLK		PCM1_CLK		PWM1	WKDT2	GPIO_INT
GPIOD_6		UART2_RTS	I2C1_SCL	SPI1_MOSI	I2S0_SD_RX	PCM1_OUT		PWM2		GPIO_INT
GPIOD_7		UART2_OUT	I2C1_SDA	SPI0_MISO		PCM1_IN		PWM3		GPIO_INT
GPIOE_0	JTAG_TRST	UART0_OUT	I2C2_SCL	SPI0_CS0	I2S0_WS	PCM0_SYNC		PWM0		
GPIOE_1	JTAG_TDI	UART0_RTS	I2C2_SDA	SPI0_CLK	I2S0_CLK	PCM0_CLK		PWM1		GPIO_INT
GPIOE_2	JTAG_TDO	UART0_CTS	I2C3_SCL	SPI0_MOSI	I2S0_SD_TX	PCM0_OUT		PWM2		GPIO_INT
GPIOE_3	JTAG_TMS	UART0_IN	I2C3_SDA	SPI0_MISO	I2S0_MCK	PCM0_IN		PWM3	WKDT3	GPIO_INT
GPIOE_4	JTAG_CLK		I2C3_SCL	SPI0_CS1						
GPIOE_5			I2C3_SDA	SPI0_CS2						GPIO_INT

6 Hardware configuration

6.1 CMSIS-DAP

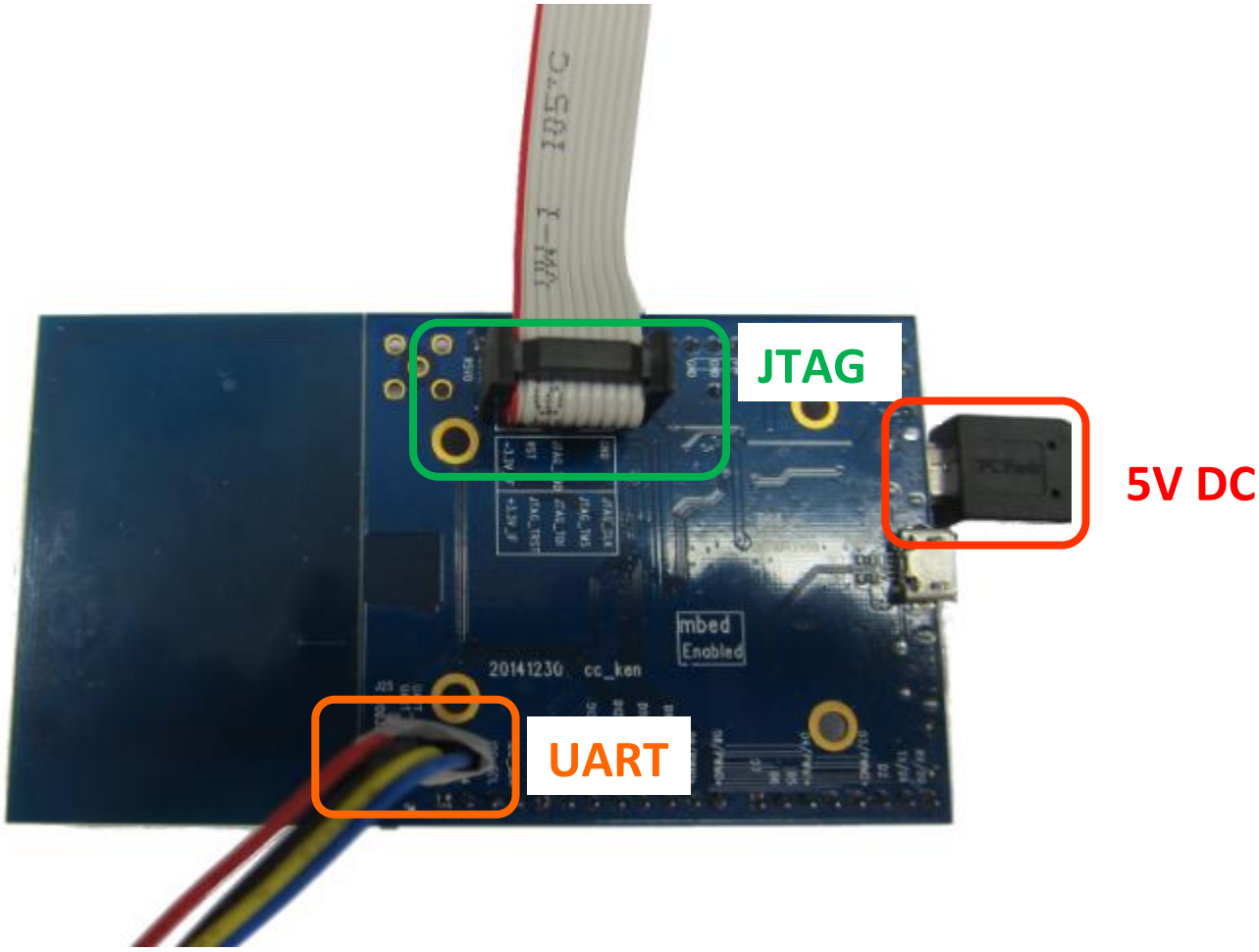
RTL-AMEBA_DEV01 supports CMSIS-DAP debugger. It requires installing “serial to USB driver”at first. Serial to USB driver can be found in tools\serial_to_usb\mbedWinSerial_16466.

Connect board to the PC with micro-USB cable.



6.2 J-Link/JTAG

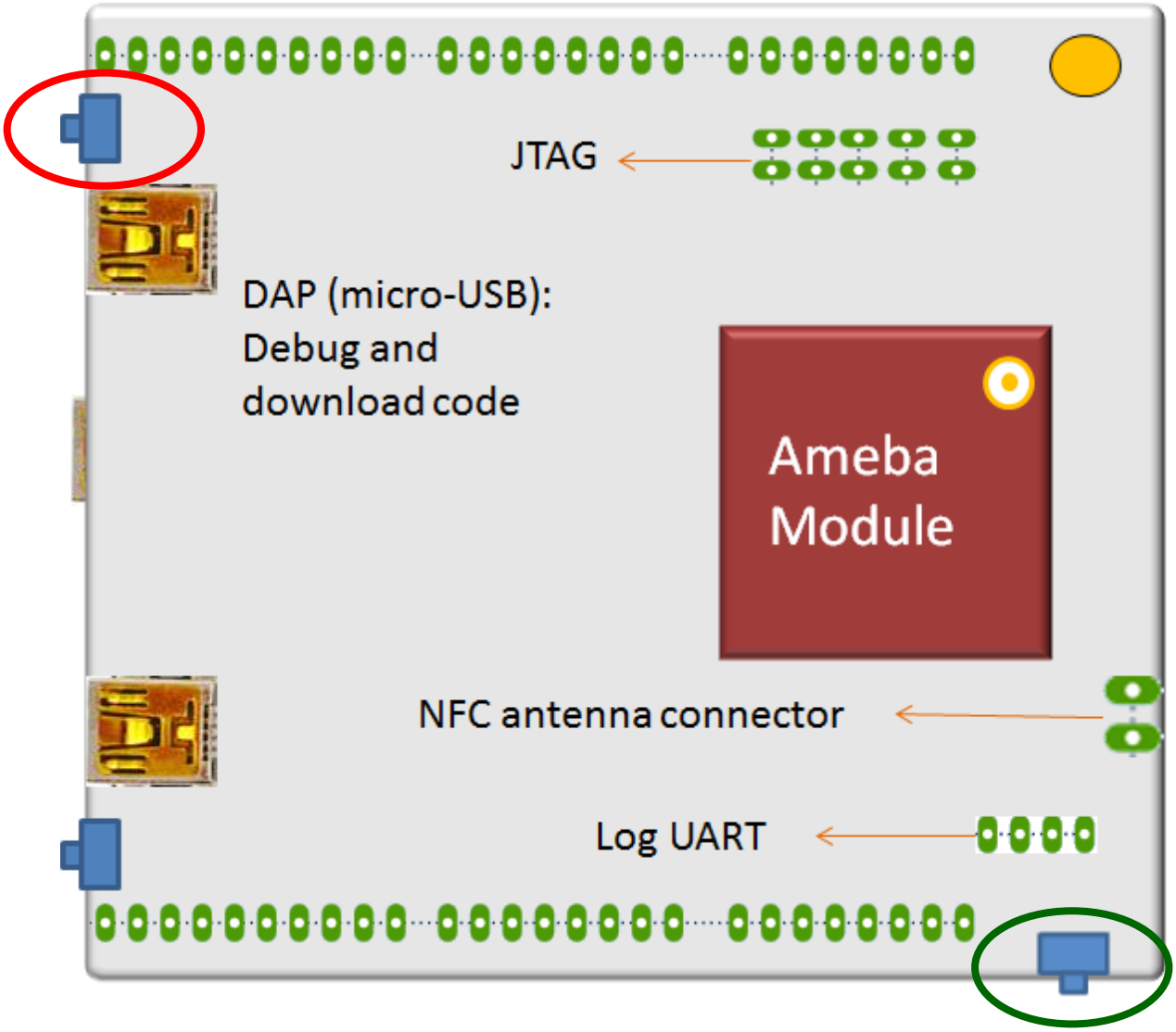
Weld JTAG and log UART connectors to HDK board and connect with pitch 2.54mm 2x5pins connector. It is recommended to weld the connector on the bottom side. Users can connect extension boards from top side.



Dupont Line or 2.54mm 2x5 pins connector.

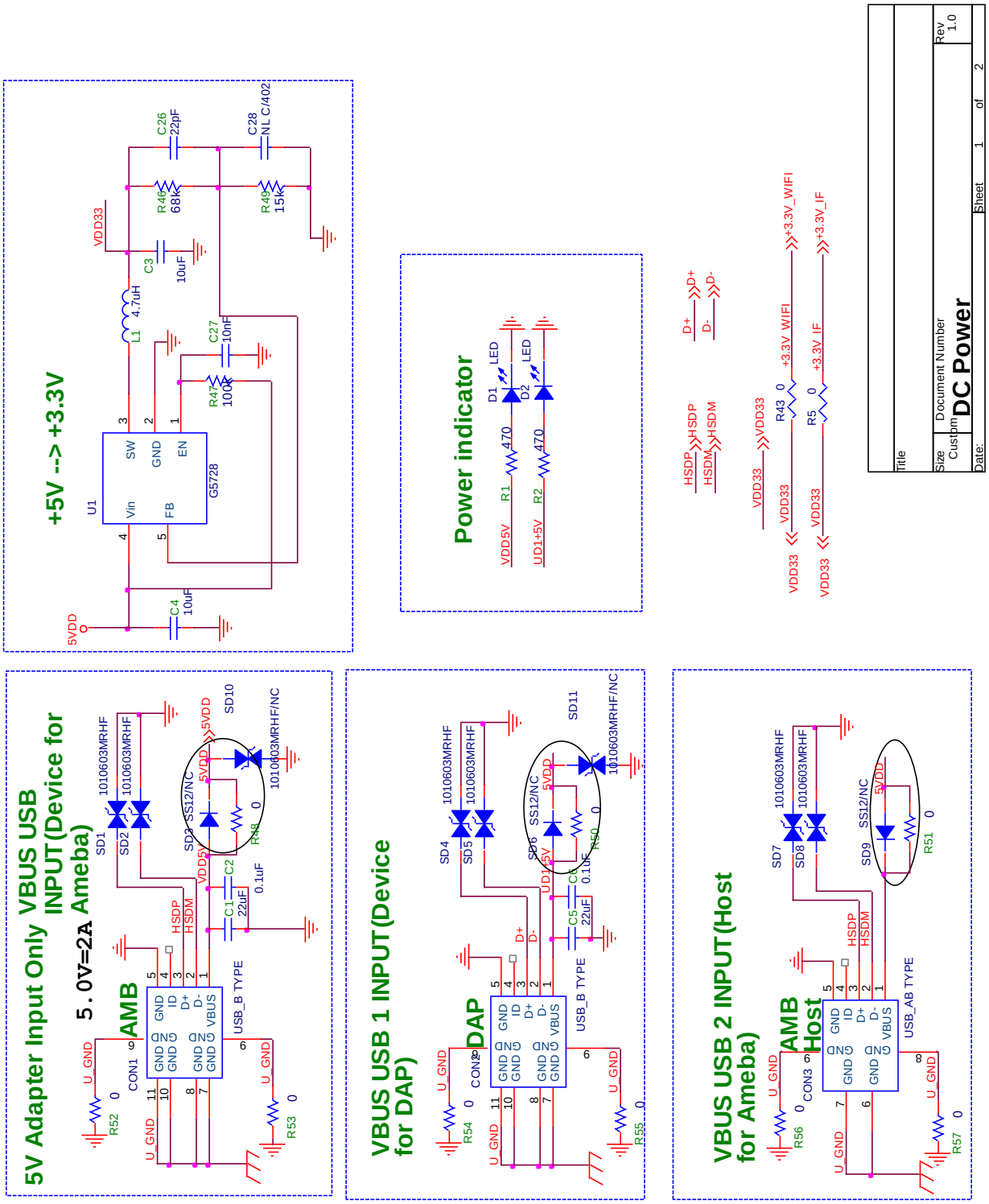
Power On

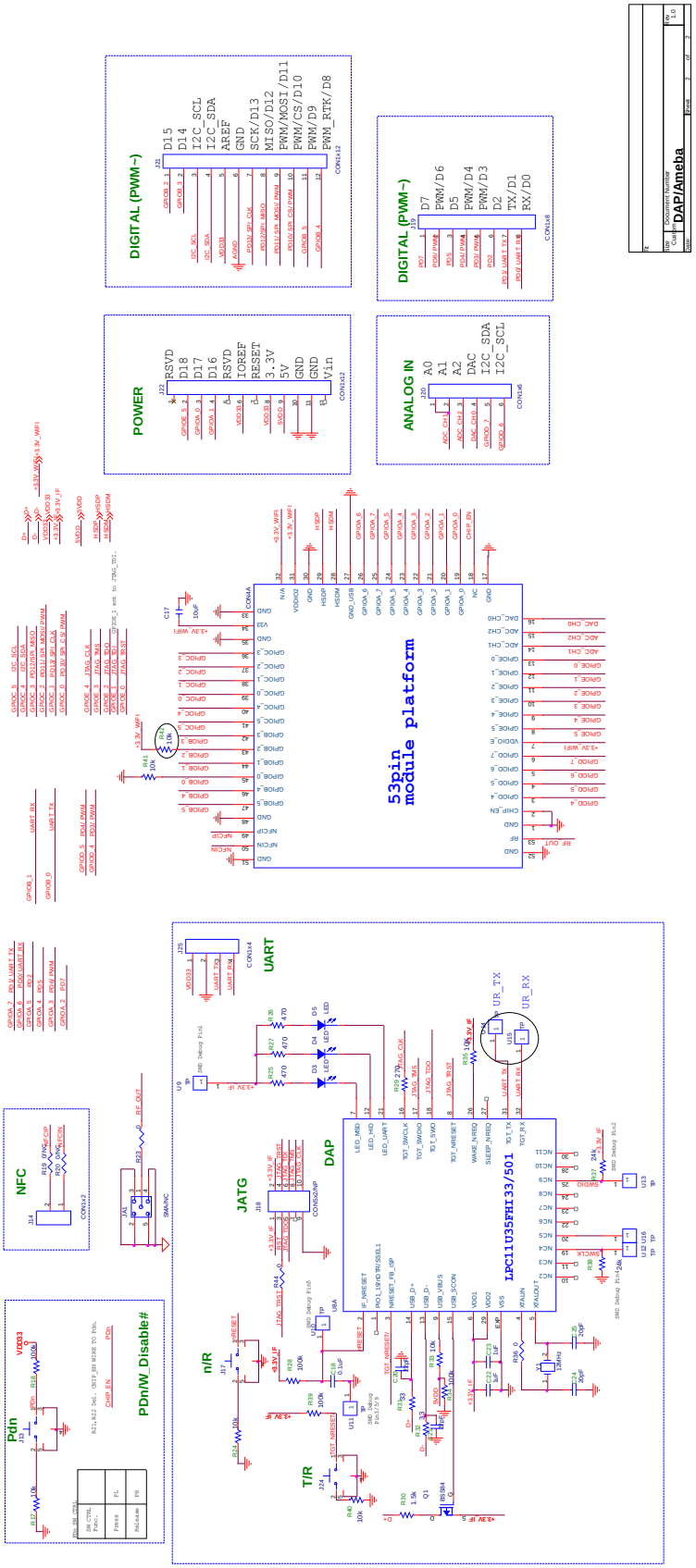
Holding button (red-circled) then plugging power to disable CMSIS-DAP function. Release the button after power on.



Note: To reset main chip, it is recommended to press Reset button (green-circled) instead of re-plugged in the power cable.

7 Reference electrical schematics




DIGITAL (PWM~)
D15
D14
I2C_SCL
I2C_SDA
AREF
GND
SCK/D13
MISO/D12
PWM/MOSI/D11
PWM/CS/D10
PWM/D9
PWM_RTK/D8
DIGITAL (PWM~)
D7
PWM/D6
D5
PWM/D4
PWM/D3
D2
TX/D1
RX/D0
POWER
RSVD
D18
D17
D16
RSVD
IOREF
RESET
3.3V
5V
GND
GND
Vin
ANALOG IN
A0
A1
A2
DAC
I2C_SDA
I2C_SCL
53pin module platform
NFC
UART
JATG
DAP
n/R
T/R
Pdn
PDn/W_Disable#
LPC11U35FHI33/501
DAP/Ameba

8 Ameba1 DEV01 pin out