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Project 4 || System & Networks I

Due By: 11/5/2016

Page-Fault Analysis

As we accessed the memory in order there should be 20480 page faults when accessing by the row and the column will be 20480*4096. This is due to the page size of 4096. Each row holds one page but skipping down by column jumps a page. Not fully sure what is wanted for the diagram, so below I showed an example of the memory in LRU style being accessed for memory of 0-9 in a smaller example of what is happening in our code. These are small examples condensed down. The first example is each sample is a row (0-9) so it's jumping rows. The second example is when it is staying in a row for multiple write/read. You can see the difference in faults will be each time the row is jumped.

0 1 2 3 4 5 6 7 8 9 (each is a row)										
	1	2	3	4	5	6	6	7	8	9
1	0	1	2	3	4	5	6	7	8	9
2		0	1	2	3	4	5	6	7	8
3			0	1	2	3	4	5	6	7
4				0	1	2	3	4	5	6
5					0	1	2	3	4	5
6						0	1	2	3	4
	New	LRU								

0 0 1 1 2 2 3 3 4 4 5 5 (each is a row)												
	1	2	3	4	5	6	7	8	9	10	11	12
1	0	0	1	1	2	2	3	3	4	4	5	5
2			0	0	1	1	2	2	3	3	4	4
3					0	0	1	1	2	2	3	3
4							0	0	1	1	2	2
5									0	0	1	1
	New	LRU										