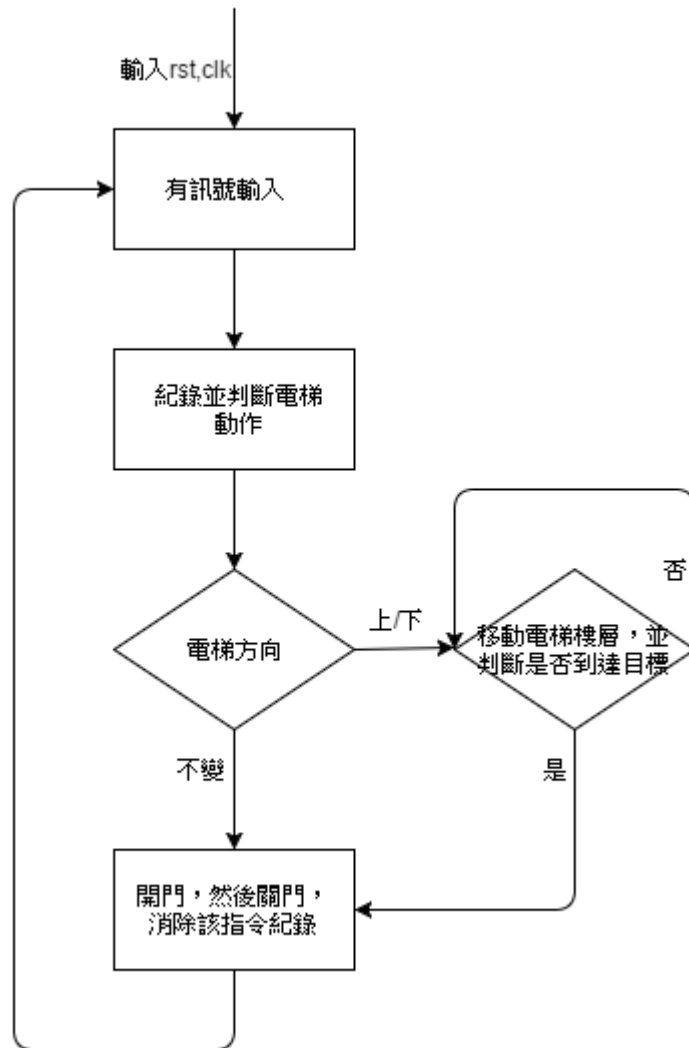


HW Final

設計概念：

對於所有的輸入(各樓層上下按鈕、前往指定樓層)，紀錄並做出相對應的動作，直到沒有新的輸入為止。

架構細節及方塊圖：

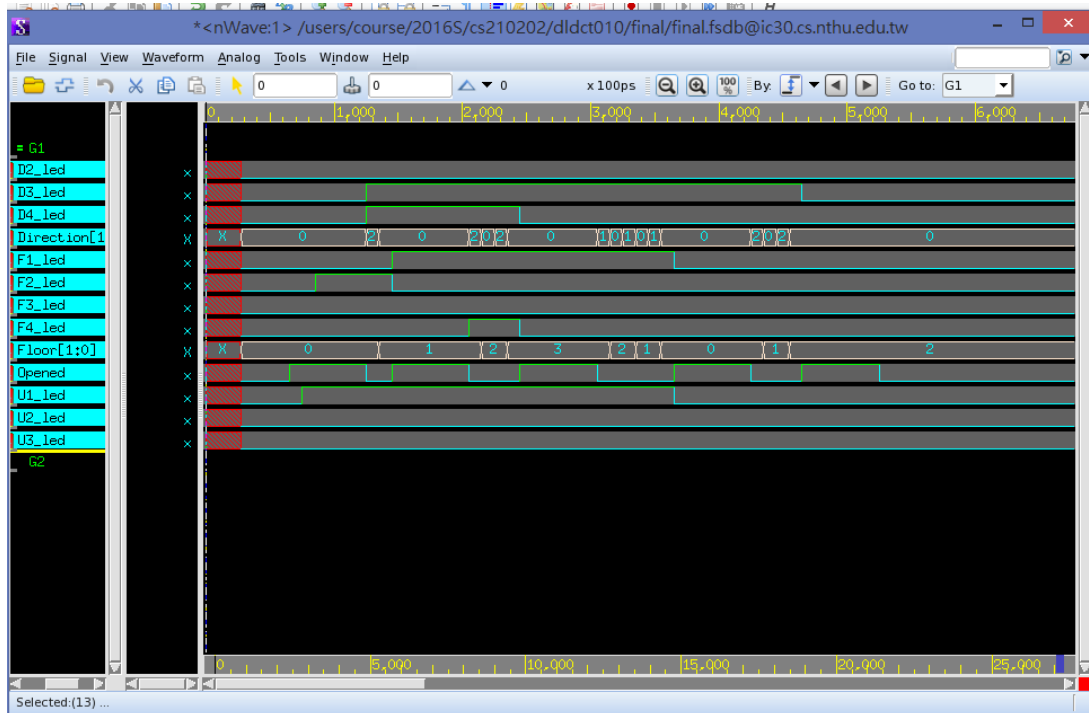


實作完成度說明：

完成 SPEC 上所要求的基本功能。

```
[dldct010@ic30 ~/final]$ make
ncverilog final_test.v final.v +access+r
ncverilog: 14.10-s005: (c) Copyright 1995-2014 Cadence Design Systems, Inc.
Recompiling... reason: file './final.v' is newer than expected.
expected: Sun Jun 19 23:49:42 2016
actual: Sun Jun 19 23:50:13 2016
file: final.v
module worklib.elevator:v
  errors: 0, warnings: 0
  Caching library 'worklib' ..... Done
Elaborating the design hierarchy:
Building instance overlay tables: ..... Done
Generating native compiled code:
  worklib.elevator:v <0x561e4736>
  streams: 5, words: 10723
Building instance specific data structures.
Loading native compiled code: ..... Done
Design hierarchy summary:
      Instances  Unique
Modules:         2         2
Registers:       41        41
Scalar wires:    24         -
Vectored wires:  2         -
Always blocks:   8          8
Initial blocks:  2          2
Pseudo assignments: 1          1
Simulation timescale: 100ps
Writing initial simulation snapshot: worklib.stimulus:v
Loading snapshot worklib.stimulus:v ..... Done
*Verdi3* Loading libsscore_ius141.so
*Verdi3* : Enable Parallel Dumping.
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
FSDb Dumper for IUS, Release Verdi3_J-2014.12-SP3, Linux, 07/05/2015
(C) 1996 - 2015 by Synopsys, Inc.
*Verdi3* FSDb WARNING: The FSDb file already exists. Overwriting the FSDb file may crash the programs that are using this file.
*Verdi3* : Create FSDb file 'final.fsd'

```



測試完整度：

按各層樓按鍵，以及上下鍵，測試電梯運行。

困難與解決方法：

遇到各式各樣困難的、不會寫的、出錯的東西

<sol>問助教、上網查。

心得：難翻了。