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1. The _____ format is usually used to store data.
   a) BCD
   b) Decimal
   c) Hexadecimal
   d) Octal
2. The ALU makes use of _____ to store the intermediate results.
   a) Accumulators
   b) Registers
   c) Heap
   d) Stack

3. _____ are numbers and encoded characters, generally used as operands.
   a) Input
   b) Data
   c) Information
   d) Stored Values
4. _____ is generally used to increase the apparent size of physical memory.
   a) Secondary memory
   b) Virtual memory
   c) Hard-disk
   d) Disks
5. The time delay between two successive initiations of memory operation _____
   a) Memory access time
   b) Memory search time
   c) Memory cycle time
   d) Instruction delay
6. The decoded instruction is stored in _____
   a) IR

b) PC
c) Registers
d) MDR

7. Which registers can interact with the secondary storage?
a) MAR
b) PC
c) IR
d) R0

8. During the execution of a program which gets initialized first?
a) MDR
b) IR
c) PC
d) MAR

9. Which of the register/s of the processor is/are connected to Memory Bus?
a) PC
b) MAR
c) IR
d) Both PC and MAR

10. The internal components of the processor are connected by _____
a) Processor intra-connectivity circuitry
b) Processor bus
c) Memory bus
d) Rambus

11. The registers, ALU and the interconnection between them are collectively called as _____
a) process route
b) information trail
c) information path
d) data path

12. In memory-mapped I/O _____
a) The I/O devices and the memory share the same address space
b) The I/O devices have a separate address space
c) The memory and I/O devices have an associated address space
d) A part of the memory is specifically set aside for the I/O operation

13. The usual BUS structure used to connect the I/O devices is _____
a) Star BUS structure -
b) Multiple BUS structure
c) Single BUS structure
d) Node to Node BUS structure

14. The advantage of I/O mapped devices to memory mapped is _____
a) The former offers faster transfer of data
b) The devices connected using I/O mapping have a bigger buffer space
c) The devices have to deal with fewer address lines
d) No advantage as such

15. The system is notified of a read or write operation by _____
a) Appending an extra bit of the address
b) Enabling the read or write bits of the devices
c) Raising an appropriate interrupt signal
d) Sending a special signal along the BUS

16. The method of accessing the I/O devices by repeatedly checking the status flags is _____
a) Program-controlled I/O
b) Memory-mapped I/O
c) I/O mapped
d) None of the mentioned

17. The method of synchronising the processor with the I/O device in which the device sends a signal when it is ready is?
a) Exceptions
b) Signal handling
c) Interrupts

d) DMA

18. To get the physical address from the logical address generated by CPU we use _____
a) MAR
b) MMU
c) Overlays
d) TLB

19. _____ method is used to map logical addresses of variable length onto physical memory.
a) Paging
b) Overlays
c) Segmentation
d) Paging with segmentation

20. During the transfer of data between the processor and memory we use _____
a) Cache
b) TLB
c) Buffers
d) Registers

21. Physical memory is divided into sets of finite size called as _____
a) Frames
b) Pages
c) Blocks
d) Vectors

22. If we want to perform memory or arithmetic operations on data in Hexa-decimal mode then we use _____ symbol before the operand.
a) ~
b) !
c) $

d) *

23. Which of the following attribute(s) do/does not belong to computer architecture?

A. Number of bits used to represent data types
B. The instruction set
C. Interface between the computer and peripherals
D. Techniques for addressing memory
E. The memory technology used

24. What are the major structual components of Central Processing Unit (CPU)?

A. Registers

B. CPU interconnection

C. Arithmetic and Logic Unit (ALU)

D. I/O Modules

E. Main memory

F. Control Unit (CU)

25. Which of the following statement(s) do/does not belong to the content of Von Newmann's principle?

xA. The computer's memory is addressable

B. Program represented in a form suitable for storing in memory alongside the data

xC. The computer uses a counter program to indicate the next instruction

xD. Each instruction must have a memory area that contains the next address instruction

E. The computer can control all operations with a single program

26. With the challenge of balancing processor performance with that of main memory and other computer components, the improvements in Chip Organization and Architecture could be:

A. Change processor organization and architecture such as parallelism,…

B. Increase hardware speed of processor

C. Increase size and speed of caches

D. All of the above

27. A benchmark program is run on a 40 MHz processor. The executed program have following parameters as follow:

Instruction Type	Frequency	Cycles per Instruction
Integer arithmetic	**45%**	**1**
Data transfer	**32%**	**2**
Floating point	**15%**	**2**
Control transfer	**8%**	**2**

Which of the following is true about the average CPI of the above table?

A. Integer arithmetic takes ~33% of total cycles

B. Data transfer takes ~ 41.3% of total cycles

C. Floating point takes ~ 19.35% of total cycles

D. Control transfer takes ~ 20.2% of total cycles

28. A processor has 150 different instructions and 50 general purpose registers. A 24-bit instruction word has an opcode, two register operands and an immediate operand. The number of bits available for the immediate operand field is ____

A. 3 bits

B. 4 bits

C. 5 bits

D. 6 bits

29. The two phases of executing an instruction are _____

a) Instruction decoding and storage

b) Instruction fetch and instruction execution

c) Instruction execution and storage

d) Instruction fetch and Instruction processing

30. The Instruction fetch phase ends with _____

a) Placing the data from the address in MAR into MDR

b) Placing the address of the data into MAR

c) Completing the execution of the data and placing its storage address into MAR

d) Decoding the data in MDR and placing it in IR

31. When using Branching, the usual sequencing of the PC is altered. A new instruction is loaded which is called as _____

a) Branch target

b) Loop target

c) Forward target

d) Jump instruction

32. The instructions like MOV or ADD are called as _____

a) OP-Code

b) Operators

c) Commands

d) None of the mentioned

33. _____

a) Replaces the target with its address

b) Does not replace until the test condition is satisfied

c) Finds the Branch offset and replaces the Branch target with it

d) Replaces the target with the value specified by the DATAWORD directive

34. The utility program used to bring the object code into memory for execution is _____

a) Loader

b) Fetcher

c) Extractor

d) Linker

35. The most efficient way of handling parameter passing is by using _____

a) General purpose registers

b) Stacks

c) Memory locations

d) None of the mentioned

36. The logical addresses generated by the cpu are mapped onto physical memory by _____

a) Relocation register

b) TLB

c) MMU

d) None of the mentioned

37. VLSI stands for _____

a) Very Large Scale Integration

b) Very Large Stand-alone Integration

c) Volatile Layer System Interface

d) None of the mentioned

38. A 16 X 8 Organisation of memory cells, can store upto _____

a) 256 bits

b) 1024 bits

c) 512 bits

d) 128 bits

39. Circuits that can hold their state as long as power is applied is _____

a) Dynamic memory

b) Static memory

c) Register
d) Cache

40. In a 4K-bit chip organisation has a total of 19 external connections including 2 pins of sense/write and CS signals, then it has _____ address if 8 data lines are there.
a) 10
b) 8
c) 9
d) 12