BLDC & PMSM Motor Control 硬件原理图分析

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STM32G0 + STSPIN830
STM32G4 + STDrive101

May4th,2022
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STM32生态产品

Arm® Cortex® 32-bit MCU & MPU 的领导者

LONGEVITY 10 YEARS COMMITMENT

2007	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
全球第一款 Cortex-M MCU	**全球第一款** Cortex-M 超低功耗	第一款高性能 120 MHz, 90nm	第一款高性能 Cortex-M4 168 MHz	第一款混合信号 DSP + Analog STM32F3 Cortex-M4	入门级 超低功耗	**全球第一款** Cortex-M7	领先的超低功耗 Cortex-M4 #1 ULP 447 ULPBench™	**性能第一** 3224 CoreMark	主流 Cortex-M0+ MCUs 功耗与性价比最优的入门级!	Cortex-M33 兼顾超低功耗和信息安全	**世界上最强大的 MCU** 最新一代混合信号 Cortex-M4 MCUs	**全球第一款** LoRa®-enabled System-on-Chip
STM32**F1**	STM32**L1**	STM32**F2**	STM32**F4**	STM32**F3** STM32**F0**	STM32**L0**	STM32**F7**	STM32**L4**	STM32**H7** 超低功耗 性能优异 STM32**L4+**	STM32**G0**	STM32**L5** 双核, 多协议和开放射频 STM32**WB**	STM32**H7** 第一款双核微处理器 STM32**G4** STM32**MP1**	STM32**WL**

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STM32主流型MCU演变

STM32F1
- 72MHz (Cortex-M3)
- 通用应用

STM32F0
- 48MHz (Cortex-M0)
- 通用应用

STM32G0
- **64MHz (Cortex-M0+)**
- 通用应用/USB-C PD
- 更高性价比

STM32F3
- 72MHz (Cortex-M4)
- 电机和电源

STM32G4
- 170MHz (Cortex-M4)
- 数学运算加速器
- 电机、电源和通用兼顾

申请STMCU样片流程.pdf

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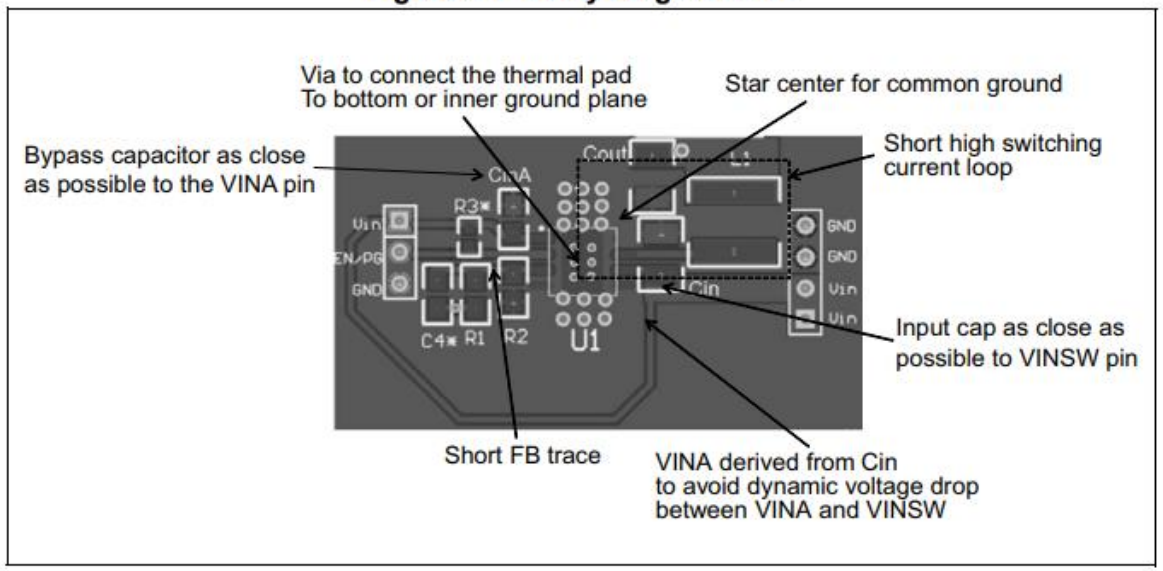
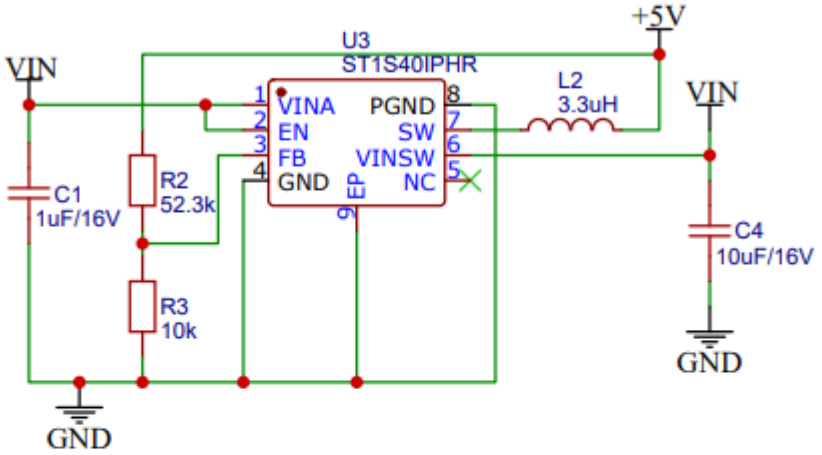
电源部分原理图设计

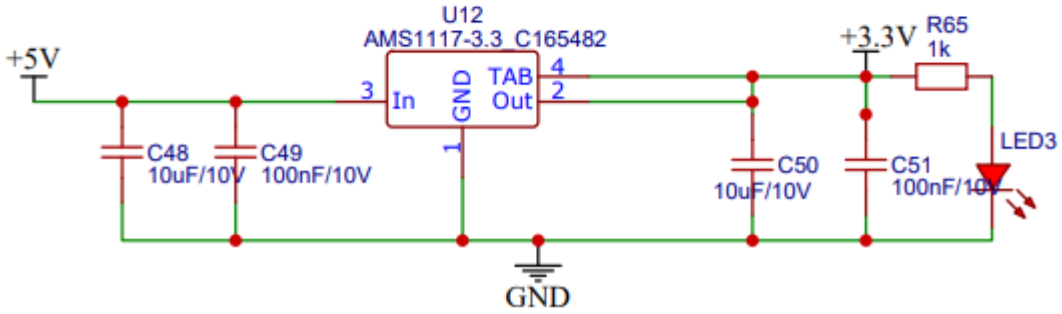
Table 1. Pin description

N°		Type	Description
VFQFPN and HSOP-8	S08-BW		
1	3	V_{INA}	Unregulated DC input voltage
2	4	EN	Enable input. With EN higher than 1.2 V the device in ON and with EN lower than 0.4 V the device is OFF (ST1S40Ixx).
3	5	FB	Feedback input. Connecting the output voltage directly to this pin the output voltage is regulated at 0.8 V. To have higher regulated voltages an external resistor divider is required from Vout to the FB pin.
4	6	AGND	Ground
5	-	NC	It can be connected to ground
6	8	VINSW	Power input voltage
7	1	SW	Regulator output switching pin
8	2	PGND	Power ground
-	7		Ground
9	-	ePad	Exposed pad mandatory connected to ground

Figure 8. PCB layout guidelines







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STM32G0原理图设计

System

- Power supply POR/PDR
- Xtal oscillator 32 kHz + 4 to 48 MHz
- Internal RC oscillators 32 kHz + 16 MHz
- PLL + Prescaler
- Clock control
- RTC/AWU
- Systick timer
- 2x watchdogs (independent and window)
- 60 I/Os on 64 pins
- Cyclic redundancy check (CRC)

Arm® Cortex®-M0+ CPU Up to 64 MHz

- Nested vector interrupt Controller (NVIC)
- SW debug
- Memory Protection Unit
- AHB-Lite bus matrix
- APB bus
- Up to 128-Kbyte Flash memory
- Up to 36-Kbyte SRAM
- 20-byte backup registers
- Boot ROM
- 7-channel DMA

Analog

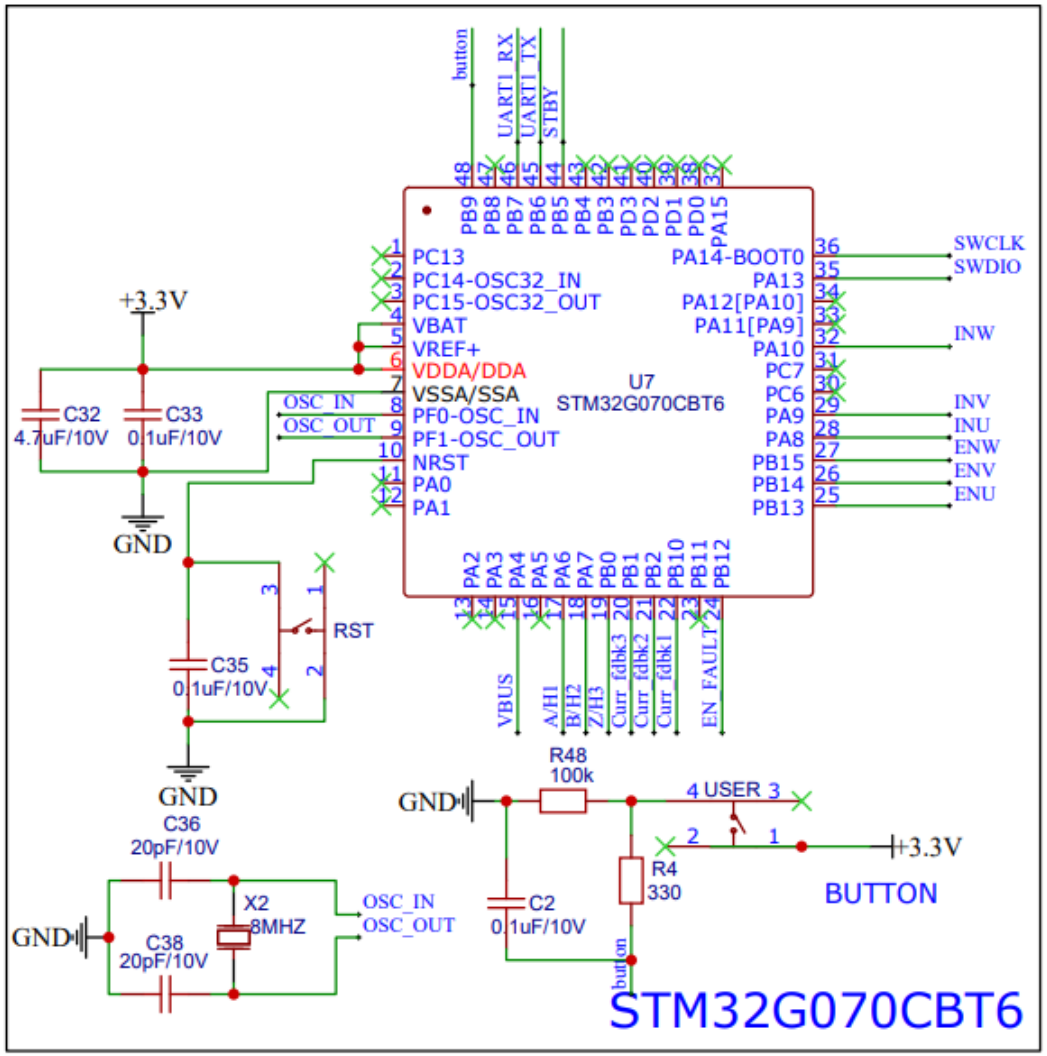
- Temp. sensor
- 1x 12-bit ADC SAR 16-channels / 2.5 MSPS

Connectivity

- 2x SPI (I²S)
- 4x USART (2x with LIN, smartcard, IrDA, modem control)
- 2x I²C (SMBus, PMBus, Fast Mode Plus)

Control

- 1x 16-bit Motor C. timer 4 PWM + 3 compl.
- 5x 16-bit timers 2 PWM each



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STSPIN830原理图设计

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Features

- Operating voltage from 7 to 45 V
- Maximum output current 1.5 A_{rms}

Table 6. Pin description

N.	Name	Type	Function
1	REF	Analog input	Reference voltage for the PWM current control circuitry
2	TOFF	Analog input	Internal oscillator frequency adjustment
3, 6, 15	GND	Ground	Device ground
4	SNS	Analog input	Current limiter sense input
5	SENSEU	Power output	Sense output of the bridge U
7	OUTU	Power output	Power bridge output U
9	VS	Supply	Device supply voltage
10	VS	Supply	Device supply voltage
11	OUTV	Power output	Power bridge output V
12	OUTW	Power output	Power bridge output W
13	SENSEV	Power output	Sense output of the bridge V
14	SENSEW	Power output	Sense output of the bridge W
16	STBY\RESET	Logic input	Standby\Reset input When forced low the device enters in low consumption mode
17	EN\FAULT	Logic input\ Open drain output	Logic input 5 V compliant with open drain output. This is the power stage input enable (when low, the power stage is turned off) and is forced low through the integrated open-drain MOSFET when a failure occurs
18	MODE	Logic input	Inputs driving method selection. When low the ENx\INx option is selected, when high the INxH\INxL option is enabled
19	INU\INUH	Logic input	Output U high-side driving input (1)
20	ENU\INUL	Logic input	Output U low-side driving input (1)
21	INV\INVH	Logic input	Output V high-side driving input (1)
22	ENV\INVL	Logic input	Output V low-side driving input (1)
23	INW\INWH	Logic input	Output W high-side driving input (1)
24	ENW\INWL	Logic input	Output W low-side driving input (1)
8	NC	NC	Not connected.

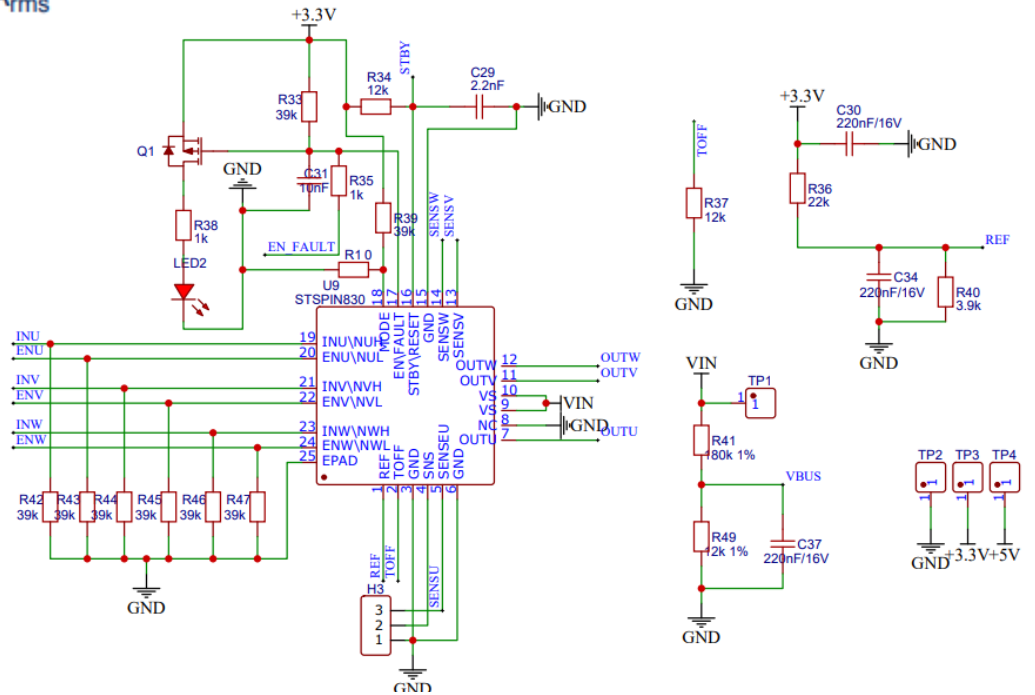
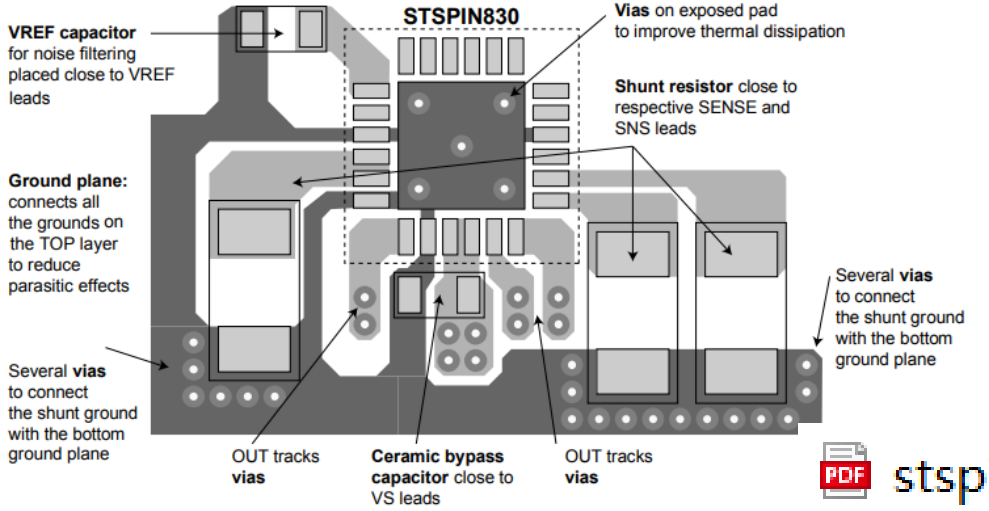


Figure 14. **PCB layout example with triple shunt (top layer)**



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STSPIN830过流保护

Figure 4. **PWM current limit sequence example**

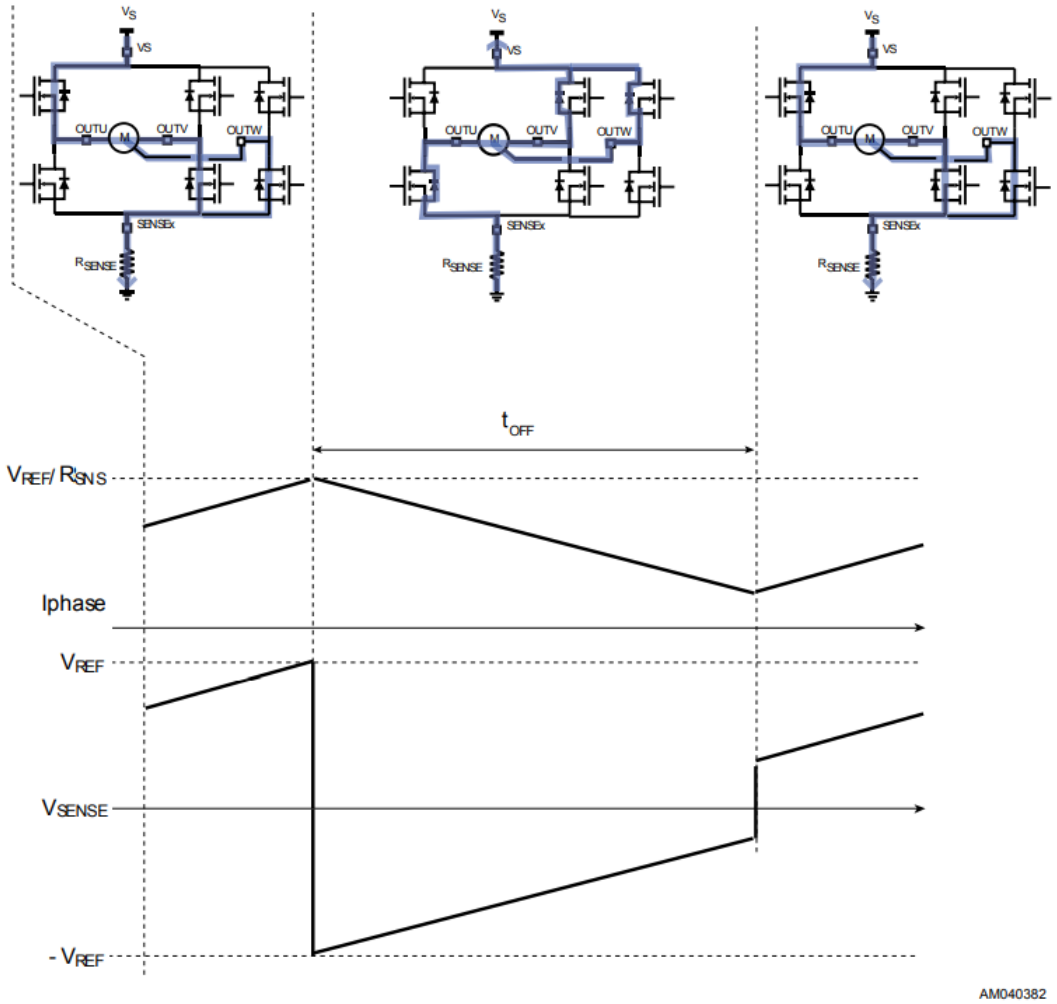


Figure 3. **Current in the power stage during on-time and off-time**

TON:
the current is charged in the load turning on one HS MOSFET and an LS MOSFET

TOFF:
the current is discharged in the load turning on both LS MOSFETs

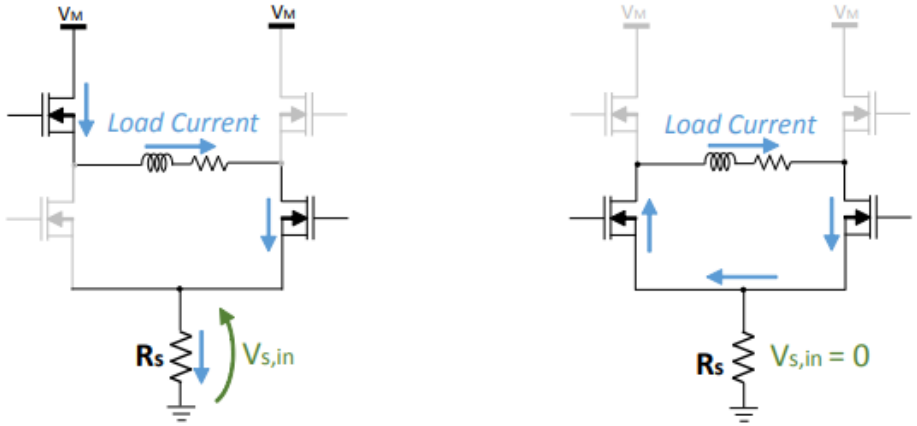
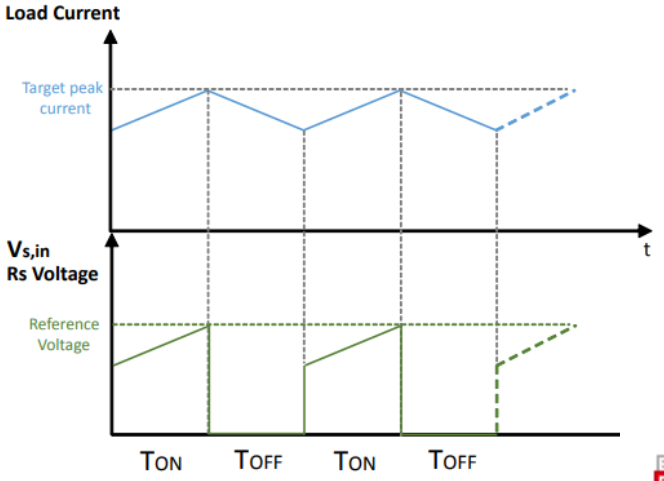


Figure 4. **PWM current control based on the current peak**



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an5397-current-sensing-

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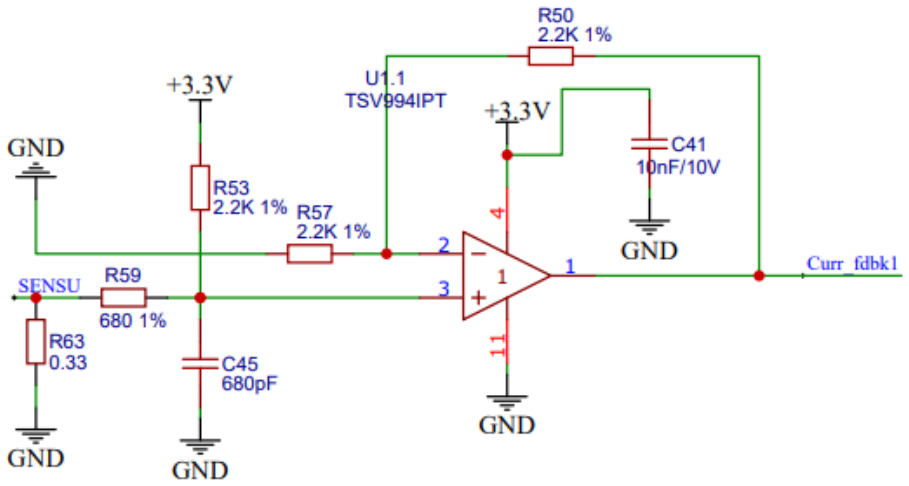
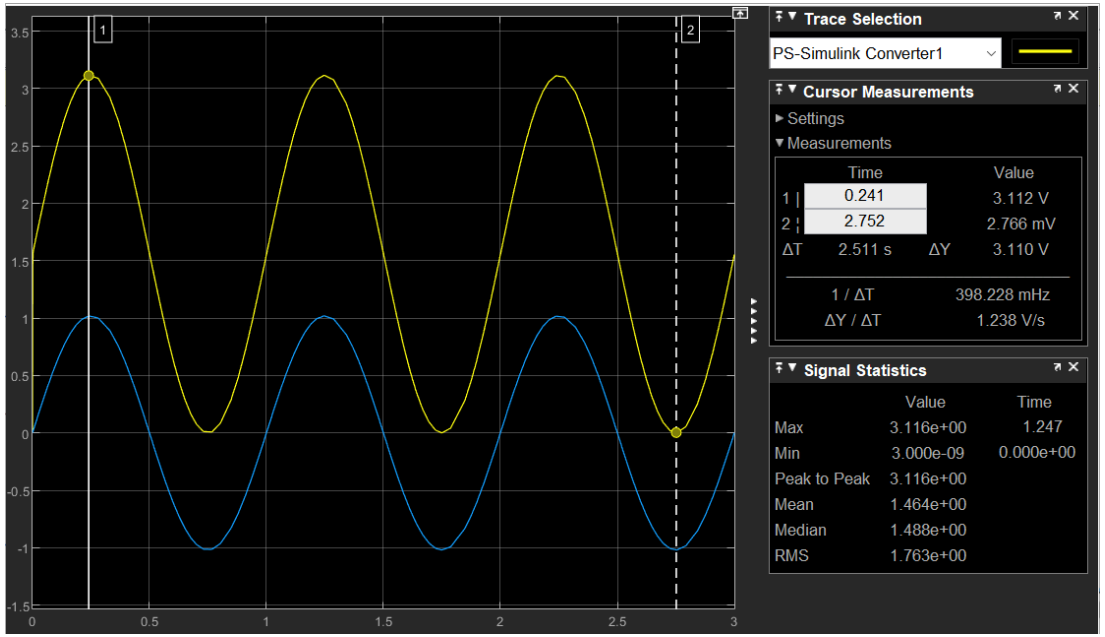
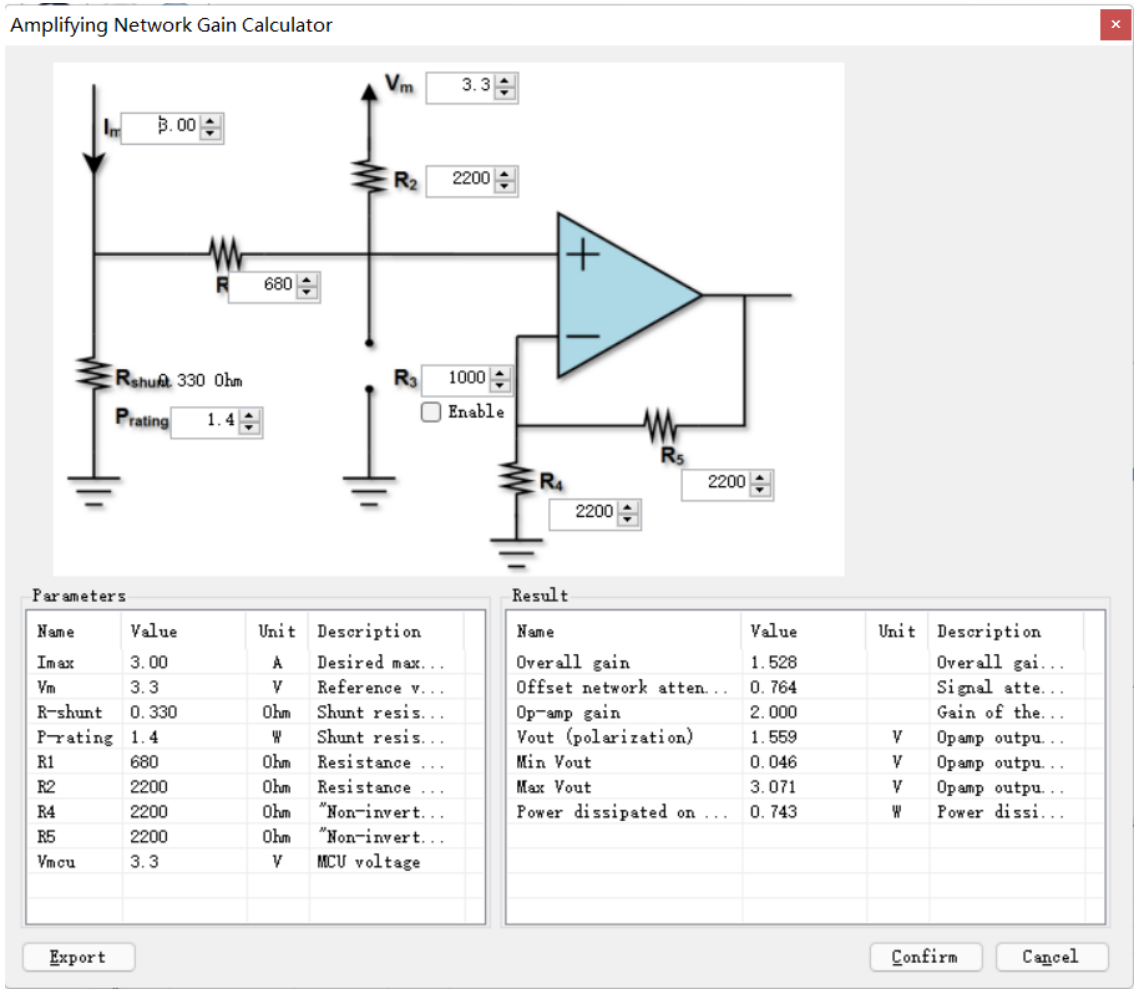
TSV994原理图设计







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