Abstract

Due to the rapid evolution of CMOS technologies, digital processing of signals has become an attractive option in mixed-signal systems, such as digital communication and medical instrumentation. In such a system, the analog-to-digital converter (ADC) plays a key role by digitizing the analog input signal. Time-interleaving of ADCs is an attractive way to increase the overall conversion rate in a given technology while keeping the high resolution.

Time-interleaving is a technique involving multiple parallel ADC channels clocked out of phases and operating together to increase the overall sample rate. However, mismatches among the time-interleaved ADCs generate undesired spectral components and can significantly degrade the signal-to-noise-and-distortion ratio of the system. Mismatches that have been considered in the past are gain mismatches and timing mismatches. Gain mismatches cause amplitude modulation of the input samples by the sequence of channel gains. Timing mismatch cause phase modulation of the input samples. Without any calibration, careful layout techniques have shown a limitation to about 7 to 8 bits of accuracy because of these mismatches.

These mismatches have to be corrected in order to get sufficient performances from the converter. This paper presents the classical calibration methods and focuses on the blind ones. Among those, both mixed analog-digital methods and fully digital methods are overviewed. By considering the state-of-the-art of published chips, a comparison between those methods is provided.

Time Interleaved ADCs (TIADC) are an increasingly used solution to implement high sampling rate ADCs at a moderate hardware cost. They are comprised of M single converters operating in parallel at a frequency Fs/M, where Fs is the sampling frequency of the overall TIADC. However, due to the manufacturing process, the sub-converters have slightly different characteristics causing mismatches. Offset mismatch occurs when the sub-ADCs have different offset values whereas gain mismatch happens when the sub-ADCs have different gain values. Timing skew mismatch is due to the fact that the sub-ADCs sample the signal with a small timing offset with respect to their ideal sampling time. Finally, bandwidth mismatch happens when the sub-ADC sampling front-ends have different frequency responses, for example different cut-off frequencies.

The mismatches deteriorate the TIADC output signal by creating mismatch noise, a sum of spurious tones and aliased versions of the input signal. They consequently become a limiting factor in the design of high-speed TIADCs as they reduce the SNDR and the SFDR of the converter. For that reason, it has long been a challenge to correct these mismatches and several approaches have been proposed. They can be classified into different categories.

Previous monolithic time-interleaved ADC arrays used foreground calibrations, digital filters, or trimming to minimize the effects of these mismatches. A disadvantage of trimming is that it lacks the ability to track variations over time and temperature. They require a known signal, for example a sine-wave, at the input of the TIADC during an offline phase. Foreground calibration interrupts the conversion of the input while the calibration occurs, which is undesirable in many applications. Also, foreground calibration circuitry does not track changes over time in calibrated parameters. They are not suitable for applications where the converter is always 'on', for example communications systems. Indeed, temperature variations and aging may require the calibration to be done frequently or even continuously. These techniques can however find their application in high-end measurement systems where the equipment can often be sent to calibration.

To overcome the limitations of foreground calibration, calibration can be done in the background. Background calibration has the advantage of being transparent to the user and can be performed without interrupting normal ADC operation. Much work has been done on calibration methods to correct for gain mismatches and some work has been done on correcting timing mismatches. However, when the conversion rate increases, this requirement becomes more difficult to satisfy. Background calibration techniques can be subdivided into blind and non-blind techniques.

Non-blind background calibration techniques require to slightly modify the input signal in the analog domain in order to calibrate for the mismatches. For example offset and gain mismatch calibration can be performed by generating a random signal that can either be added to the analog input signal or, multiplied with it. The technique published in performs bandwidth mismatch estimation by adding a known sine-wave to the TIADC input signal.

In this special session, we focus on blind background calibration for offset, gain and timing skew mismatches. Blind background calibration techniques are probably the most challenging ones because they need to work with the actual input signal only. In most, if not all blind techniques, the calibration of the mismatches is controlled in the digital domain. When the calibration is done with the help of a feedback to the analog front-end, we talk about mixed signal calibration or mixed calibration. If the calibration entirely takes place in the digital domain, we speak about fully digital calibration, and it can be an alternative and can be used in place of analog trimming. To apply ADCs to a Digital communication system that requires high-speed signal processing and high dynamic input range as well, digital background calibration is mostly used. Offset mismatch can be corrected by subtracting the estimated offset from each sub-ADC digital samples, which only requires an adder per sub-ADC. Similarly, gain mismatch can be corrected by multiplying the output of each sub-ADC by the inverse of its estimated gain, which only requires one multiplier per sub-ADC

Digital skew mismatch correction requires more filtering in order to recover the samples with the correct sampling times. The skew mismatch correction technique implemented in is inspired from the technique presented in. It uses the fact that the

timing offset of each ADC is small as compared to the sampling period. In this particular case, the samples can be recovered by doing a first-order Taylor approximation of the skew mismatch error. This requires the use of the signal derivative, obtained by passing the TIADC samples through a digital differentiating FIR filter.

Another possibility is to reconstruct the signal with the help of fractional delay filters as explained in . However, similarly to the derivative-based technique, this method requires a significant amount of digital filtering.

The researches on mismatch calibration methods for TIADC have been processed for a great many years at home and abroad and massive achievements have been gained. Among these, the most anonymous are University of Graz, UC Davis and Santa Barbara. They all published an extremely great many of papers on this region.