Batteries & Supercaps

Research Article
doi.org/10.1002/batt.202400364

Chemistry Europe
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Sputtered Zero-Excess Electrodes with Metallic Seed Layers for Solid-State Sodium Batteries

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Zero-excess sodium metal solid-state batteries offer improved safety, lower cost, higher energy density, and reduced resource dependency compared to today's lithium-ion technology. This study demonstrates the fabrication of zero-excess electrodes with unprecedented stability during plating/stripping cycles. The fabrication process involves the sputter deposition of 20 nm metallic seed layers – zinc, silver, indium, or tin – onto NASICON ($Na_{3.4}Zr_2Si_{2.4}P_{0.6}O_{12}$) ceramic separators, followed by the sputter deposition of a 30 μm copper current collector. The favorable influence of these seed layers on the in-situ formation of the sodium | NASICON interface is examined through nucleation and cycling experiments, with a sodium metal reservoir serving as the non-limiting counter electrode. Due to alloy formation the seed layers – particularly tin – stabilize sodium nucleation and cycling substantially and reduce dendrite formation compared to reference cells with bare copper current collectors. Sodium loss during cycling is primarily attributed to local cracking of the current collector and its partial delamination from the NASICON. Compared to polished NASICON, a roughened surface reduces the resistance e.g. of the counter electrode 200-fold to approx. 1 Ωcm^2 at 3 MPa and suppresses delamination further.

1. Introduction

With rapidly increasing demand for energy storage, sodium-based batteries are gaining interest as a low-cost alternative to the established lithium-based technology. The prevalent approach in this field substitutes lithium with sodium in conventional liquid electrolyte ion batteries.[1] While a plain substitution may lead to a cost reduction due to the lower price of sodium, it inevitably leads to a decrease in energy and power density, due to sodium's less negative standard potential and higher molar mass compared to lithium (Na: −2.71 V; 22.99 g/mol and Li: −3.04 V; 6.94 g/mol).

To address these challenges, a promising upcoming technology replaces the liquid electrolyte infiltrated separators commonly used in current batteries with sodium-ion conducting oxide ceramics like NASICON (Na-Super-Ionic-CONductor; $Na_{3.4}Zr_2Si_{2.4}P_{0.6}O_{12}$)[2,3] as solid-state electrolytes (SSE). These rigid SSEs might reduce sodium dendrite formation during cycling and therefore might allow the use of pure metallic sodium anodes.[4,5] This has the potential to increase energy and power densities substantially, as the anode capacity is then limited only by the mechanical constraints of the battery to accommodate enough metallic sodium. In contrast, liquid electrolyte sodium batteries commonly use intercalation-based hard carbon anodes. Their capacity naturally is limited by the diffusion of the sodium cations into the hard carbon, the amount of hard carbon used, and the maximum sodium metal content of the hard carbon, which to date reaches only one-third by weight.[6]

However, due to sodium metal's reactivity in air, a dry argon or nitrogen atmosphere would be required for its safe and inert handling,[7] rendering the fabrication of batteries with metallic sodium electrodes procedurally challenging. One proposed solution to this is the concept of zero-excess sodium metal SSBs, also referred to as "reservoir-free" (or colloquially as "anode-free") sodium metal SSBs.[8–10] As depicted in Figure 1, in this approach, the cell is initially assembled without a sodium metal anode, but with sodium cations at the cathode only. Metallic sodium is subsequently deposited in-situ between the SSE separator and an anodic current collector during the first charging cycle of this initially uncharged battery. Consequently, the metal electrode contains only the sodium which is cycled, and no metallic sodium is needed during battery assembly. Thus, production costs are decreased, and safety is increased. For NASICON based batteries, this approach holds arguably more promise than for lithium-SSBs, as NASICON is claimed to be stable even in humid air.[11,12] Therefore, assuming a suitable cathode, battery manufacture could be done even outside a glovebox, should this approach be successfully realized.

However, challenges to this approach have so far prevented large-scale application of sodium metal SSBs in general and zero-excess sodium metal SSBs in particular. One major challenge is the interface between the electrodes and the SSE. The absence of liquid electrolyte can result in insufficient contact between the solid components, as pores and gaps due

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Supporting information for this article is available on the WWW under https://doi.org/10.1002/batt.202400364

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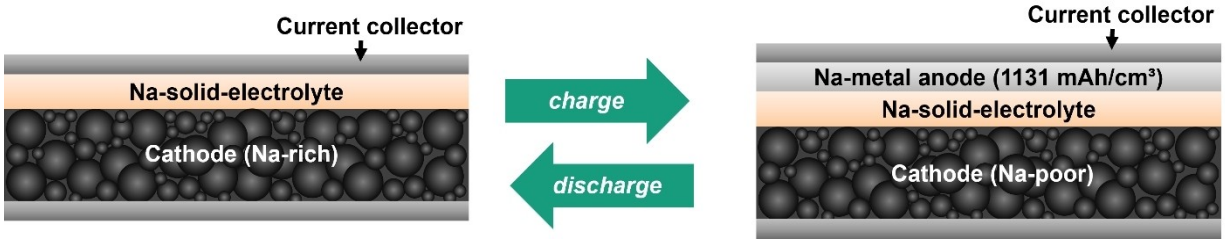

Figure 1. Schematics of a zero-excess sodium metal SSB. Plating (left to right, during charge) and stripping (right to left, during discharge) of a sodium metal electrode in zero-excess sodium SSBs.

to delamination of the components are not automatically filled with an ion-conducting liquid. This leads to high interfacial resistances,[13] and to the formation of dendrites[5,14–17] and voids[14,18] during sodium-plating and stripping at the sodium | SSE-interface at medium and high current densities.

When not applying the sodium as sodium metal to the NASICON separator during cell assembly, but instead only a current collector to enable zero-excess sodium electrodes, these challenges become more severe. As shown in Figure 1, now a good initial contact between the ceramic and a current collector made from a metal not as soft and ductile as sodium – e.g. from aluminum or copper – must be realized, as for instance observed by Ortmann et al.[19] They prepared a copper | NASICON interface by depositing copper on a polished NASICON surface by thermal evaporation and observed that larger gaps resulted from the initially incomplete physical contact between the copper electrode and the SSE during the subsequent electrochemical deposition of sodium. Larger gaps have also been observed when the current collector is pressed only on a lithium SSE, as in the case of copper | Li_6PS_5Cl.[20]

To strengthen the physical contact between the current collector and the SSE, this study pursues three approaches in parallel:

a. Sputter deposition of the copper current collector instead of current collector foils, commonly used in today's battery technology. Sputter deposition allows the seed layer and thereafter the current collector to be deposited onto the solid electrolyte without gaps at room temperature. To the knowledge of the authors, only vapor deposition of copper in combination with plating of sodium has been used so far.[19] A few studies which demonstrate cycling of substantial (1 mAh/cm^2 order of magnitude) area specific charges, were done for lithium metal zero-excess solid state batteries. However, here the current collector was applied by pressing copper foils at high pressures and temperatures onto ceramic lithium-ion conductors.[20,21]
b. Roughening the surface of the NASICON separator by surface sanding with P120 grits sanding paper in argon atmosphere. This roughening increases the surface area and facilitates adhesion between both the current collector and the subsequently electroplated sodium layer with the ceramic – compared to polishing as suggested in literature[19] so far. Roughening on both sides of the separator lowers the ohmic resistance of both interfaces.
c. A metallic seed layer of lower melting point metals – such as tin or indium – between the copper current collector and the SSE. A seed metal that is softer and more sodiophilic than copper could reduce mechanical stress and improve bonding at the copper | NASICON interface, as well as promote a homogeneous electrochemical sodium deposition.

Modifications of current collectors with metallic seed layers and altered surface morphologies to enhance homogeneous and reversible alkali-metal deposition have been already tested before in liquid electrolyte batteries,[22] but there the underlying mechanism is different.

The approach of zero-excess anodes with sputter deposited current collectors and oxide-ceramic electrolytes is novel and has not been extensively studied in plating and stripping experiments at significant electrode loadings up to date, thus, little is known about the loss of electrochemically active metal during the cycling. Such losses are known from liquid electrolyte batteries[8,10,22] with alkaline metal anodes, where they are commonly traced to side reactions with the liquid electrolyte. The losses of electrochemically active metal can be quantified by the Coulombic efficiency *CE*, i.e., the ratio of the transported electric charges $Q_{discharge}$ and Q_{charge} in a subsequent charging and discharging cycle of the battery:

$$CE = \frac{Q_{discharge}}{Q_{charge}} \quad (1)$$

This work aims to examine the approach of zero-excess sodium SSBs with sputter deposited current collectors and optional metallic seed layers, especially the plating and stripping of sodium electrodes with areal capacities of up to 1 mAh/cm^2 in Section 2.4. It analyzes the underlying mechanistical differences among different seed layer metals by electrochemical nucleation experiments in Section 2.5. and by contact angle measurements with molten sodium in Section 2.6.

2. Results and Discussion

2.1. Preparation of the Model Cells

Model cells are assembled as illustrated in Figure 2a to characterize the behavior of zero-excess electrodes. A NASICON ($Na_{3.4}Zr_2Si_{2.4}P_{0.6}O_{12}$) separator[5] sanded at grits of P120 (for a

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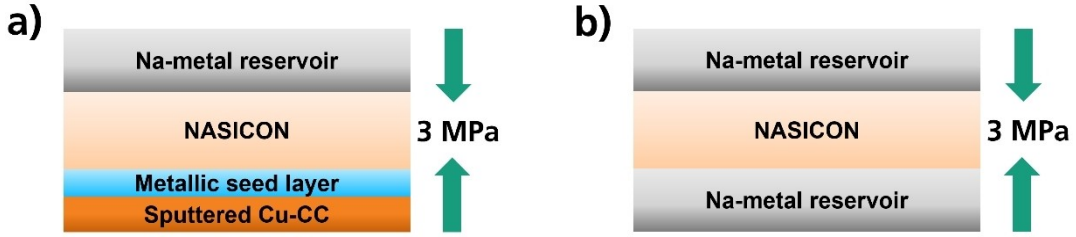

Figure 2. a): Schematic illustration of model cells before initial charging with a sodium metal reservoir as counter electrode, with a 1.4 mm thick NASICON-separator, a zero-excess electrode with a 20 nm thick sputter deposited metallic seed layer (of zinc, silver, indium or tin), and a sputter deposited copper current collector. b): Symmetrical test cells to evaluate the performance of the counter electrode.

roughened surface) or up to P4000 (polished surface) is sandwiched between the zero-excess anode – which consists of an optional sputter deposited metallic seed layer of zinc, silver, indium or tin and a copper coating, deposited by sputter deposition or thermal evaporation – and a sodium metal counter electrode.

Since the focus of this work is towards realizing the zero-excess anode, limitations caused by the counter electrode must be avoided. Therefore, instead of using an unoptimized high potential cathode, which may contribute significantly to the overall resistance of the cell due to high interfacial losses or diffusion limitations, excess sodium metal is chosen as the counter electrode material. The resulting model cells are not energy storage devices as they are electrochemically symmetrical. However, this does not change the electrochemistry of the interface at the zero-excess electrode.

In addition to the cells shown in Figure 2a, symmetrical model cells displayed in Figure 2b each with two excess sodium metal electrodes (sodium | NASICON | sodium) were assembled. This combination of two sodium metal counter electrodes allows to assess their limitations.

2.2. Electrochemical Characterization of the Sodium Counter Electrode

For the cells shown in Figure 2a sodium metal foils thick enough to provide excess sodium were pressed onto NASICON separators. Here, they serve as counter electrodes, i.e. as reservoirs for the in-situ deposition of sodium at the zero-excess electrode. Moreover, the performance of these sodium counter electrodes can be compared with the more advanced in-situ deposited sodium metal electrodes of the zero-excess electrode concept.

Before analyzing the asymmetrical cells shown in Figure 2a in Section 2.4., the electrochemical performance of the excess sodium counter electrodes is characterized in symmetrical model cells as depicted in Figure 2b. Three symmetrical cells with a NASICON separator polished on both sides and four cells with a NASICON separator roughened on both sides are assembled as described in the Experimental Section 4.1. Electrochemical impedance spectra (EIS) were recorded at incrementally increasing stack pressures, ranging from 0.06 MPa to 19.8 MPa.

Focusing first on the three cells with polished separators, Figure 3a illustrates the spectrum of the cell exhibiting the lowest resistance, measured at 19.8 MPa. The interfacial contribution in Figure 3a were extracted from the impedance data between 200 kHz and 0.5 kHz using the depicted equivalent circuit as described in the Experimental Section 4.5. Figure 3b shows the interfacial resistance contribution at increasing pressure, averaged across the three symmetrical cells. Interfacial resistance values were extracted analogous to Figure 3a. They decrease with increasing pressure. Most experiments in this study are conducted at a pressure of 3 MPa. Here the average interfacial resistance is $(206 \pm 74)\ \Omega cm^2$. At 19.8 MPa a minimum of $(36 \pm 12)\ \Omega cm^2$ is reached – one individual cell even attained $22\ \Omega cm^2$. Stack pressures above 20 MPa are not possible with the experimental setup used in this study and are unlikely to be suitable for future technical applications anyway. The data indicate however, that even higher pressures would be required for polished separators to achieve low interfacial resistances in the order of $1\ \Omega cm^2$, as reported by Ortmann et al.[14]

Shifting focus to the four cells with symmetrically roughened NASICON separators, Figure 3c shows an example electrochemical impedance spectrum at 3 MPa of stack pressure. The interfacial impedance contribution is attributed to measurements between 20 kHz and 1 kHz. Impedance spectroscopy of all four symmetrical cells yields the average interfacial resistance of one electrode as $(0.98 \pm 0.23)\ \Omega cm^2$ at 3 MPa. Increasing the stack pressure to 19.8 MPa did not reduce this value significantly.

It should be noted that the actual interfacial resistance between sodium and NASICON is known to be very small. It can be described accurately in a one dimensional model.[14] However, the resistive contribution related to current constriction inside the solid electrolyte in the vicinity of the metal electrode due to an incomplete contact of both solid components can become very large and is a three dimensional problem. This effect needs numerical modeling to be evaluated in detail. However, for the thick NASICON separators (1.4 mm) used in this study, the one-dimensional model (see Figure 3a and c) which effectively reduces current constriction to a purely interfacial property is a good enough approximation. This is indicated by the observation, that the resistive contribution attributed to the bulk NASICON is similar across all symmetrical cells at frequencies above 20 kHz with a contribution of $(39 \pm 5)\ \Omega cm^2$. While the electrochemical properties of the polished

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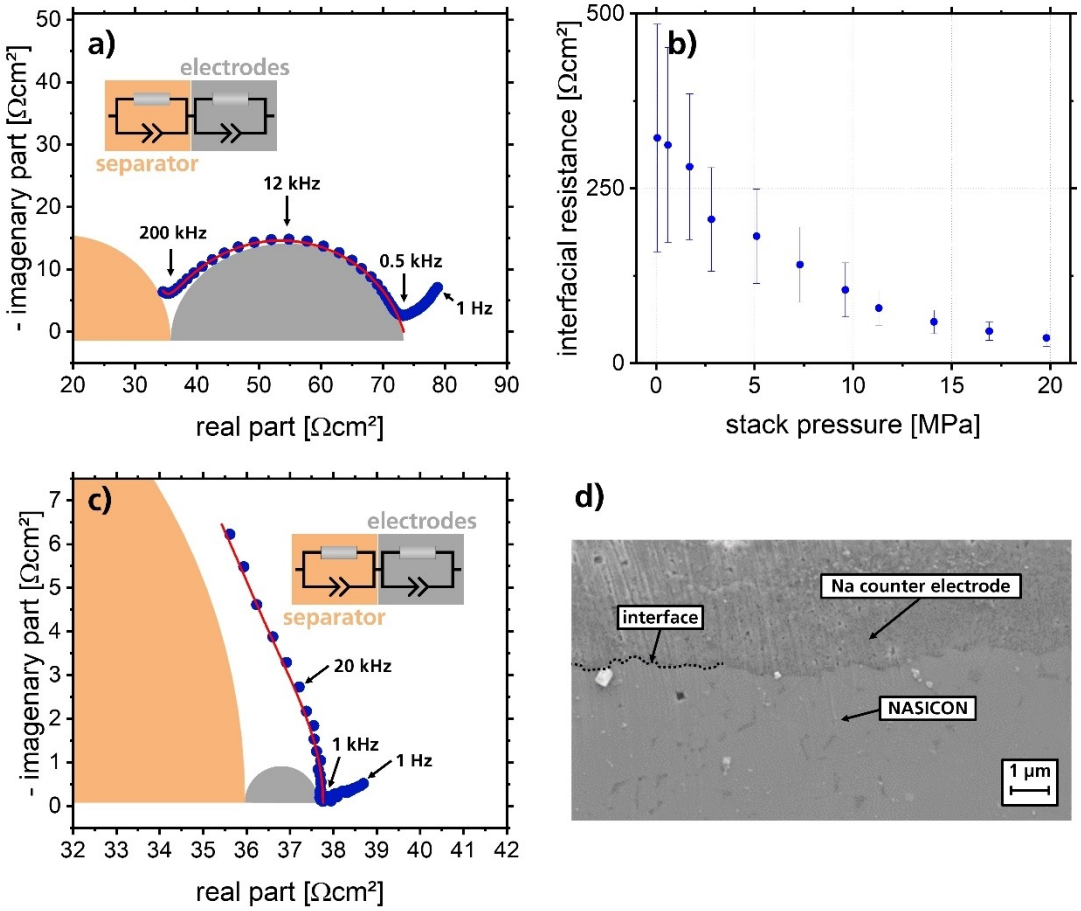

Figure 3. a): Impedance spectrum of a cell with a NASICON separator polished on both sides and symmetrical sodium electrodes between 1 MHz and 1 Hz at 30 °C and 19.8 MPa. b): Interfacial resistance between polished NASICON and a sodium electrode at increasing pressure. c) Impedance spectrum of a cell with a NASICON separator roughened on both sides and symmetrical sodium electrodes between 1 MHz and 1 Hz at 30 °C and 3 MPa. d): FESEM-image of the sodium | roughened NASICON interface at the sodium electrode. No significant porosity or delamination is visible at the interface.

interface (Figure 3b) are dominated by this current constriction, as indicated by the strong pressure dependence, the situation is less clear for the roughened interface. To investigate this, cross sections of this interface were prepared and resolved in the Field Emission Scanning Electron Microscope (FESEM), as depicted in Figure 3d. A predominantly complete wetting of the NASICON with the sodium electrode is found. No significant porosity, delamination or contamination is visible at the interface. Therefore, current constriction due to low interfacial contact – as a source of interfacial resistance between NASICON and sodium[14] – should be minimal.

Compared to the NASICON bulk resistance of (39 ± 5) Ωcm², the roughened sodium | NASICON interface contribution of (0.98 ± 0.23) Ωcm² does not significantly limit cell resistivity. To evaluate potential limitations during cycling, the four symmetrical cells with roughened NASICON are tested at a ten times higher current density than used for the zero-excess model cells in DC-stripping/plating experiments of Section 2.4. A constant current density of 1 mA/cm² was applied at a cell-stack pressure of 3 MPa and 30 °C. During this sodium transport from one electrode to the other, the current driving voltage was monitored. Impedance spectra show no significant change of the interfacial resistance before and after transporting sodium. During the 10 hours of sodium transport at 1 mA/cm², voltage fluctuations do not exceed 10 %. The influence of the counter-electrode with roughened NASICON separator can therefore be neglected on a scale above 1 Ωcm², when applying current densities of 0.1 mA/cm² in cells with zero-excess electrodes at 3 MPa. The approach of roughening the NASICON was therefore chosen for all the zero-excess cells (Figure 2a) presented in this study.

2.3. Characterization of the Sputter Deposited Copper Current Collector

The influence of deposition method and thickness of the zero-excess electrode's copper current collector was investigated. A 5 µm copper layer thermally vapor deposited on polished (P4000) or roughened (P120) NASICON substrate was found to provide sufficient contact to the NASICON for allowing sodium plating onto the current collector. However, when 1 mAh/cm² of sodium was plated, the thin copper layer was consistently penetrated by the deposited sodium (see Figure S1 in Support-

ing Information). This observation contrasts the absence of penetration of a similar copper layer, thermally vapor deposited on a polished NASICON surface at a higher current density observed by Ortmann et al.[19] To avoid penetration, the thickness of the current collector was increased. The copper layer was DC sputter deposited instead of thermally vapor deposited to increase the deposition rate in the available experimental setup.

With a now sputter deposited copper current collector of 10 μm thickness, again significant current collector sodium penetration was observed when plating 1 mAh/cm^2 of charge, both for the polished (P4000) and the roughened (P120) NASICON surfaces. At a copper layer thickness of 30 μm and above on a roughened NASICON surface, no penetration of the current collector could be observed visually when 1 mAh/cm^2 of sodium had been transported. However, attempts to sputter deposit a current collector of this thickness on polished NASICON substrates were not successful. Notably, a complete delamination of the 30 μm copper layer from the NASICON is consistently observed for polished NASICON-substrates. This is certainly a result of a built up in layer tension, as DC sputter deposition is commonly used to deposit metallic films at thicknesses below 10 μm only. With increasing film thickness, the mechanical stress in sputter deposited copper layers rises.[23] Alternative deposition methods, such as thermal vapor deposition – used in Section 2.5. for 5 μm copper layers without delamination – or electrochemical copper deposition, may improve adhesion to polished substrates. The increased grip provided by a roughened NASICON surface proved to be essential to avoid delamination of the sputter deposited current collector during cell preparation in this study at current collector thicknesses of 30 μm.

The contact of the 30 μm thick current collector to the roughened NASICON was investigated via FESEM-imaging of cross sections of this interface. As depicted in Figure 4, small gaps were found between the copper current collector and the NASICON separator. The layer stress at a copper film thickness of 30 μm may be sufficient to cause partial delamination of the deposited layer, even from the roughened NASICON substrate, explaining the partial delamination found in Figure 4.

In the cycling experiments presented in the following Section 2.4., 30 μm of copper were sputter deposited on roughened NASICON to minimize current collector penetration during sodium plating. However, in the nucleation experiments discussed in Section 2.5., 5 μm thick current collectors were thermally vapor deposited on polished NASICON surfaces. Here, sodium penetration of the current collector does not impose a challenge, since only small amounts of sodium are plated at the zero-excess electrode and are not dissolved later.

2.4. Cycling of the Zero-Excess Electrode

Sodium model cells were assembled with zero-excess electrodes as depicted in Figure 2a. As discussed above, polished NASICON separators exhibit high interfacial resistance at the counter electrode and are prone to delamination of sufficiently thick sputter deposited current collectors. Thus, both sides of the NASICON separators were roughened (P120) during cell assembly. 17 model cells were characterized: five without seed layer and three each for zinc, silver, indium and tin, see Figure S2–Figure S6 in Supporting Information. Each seed layer was sputter deposited at a thickness of 20 nm.

In the following, the sodium plating at the zero-excess electrode is referred to as negative current, while the sodium stripping of the zero-excess electrode will be referred to as positive. A charge of 1 mAh/cm^2 was deposited at −0.1 mA/cm^2 and thereafter stripped again at 0.1 mA/cm^2. This process was repeated for a total of 10 cycles for each cell. During cycling, the cell voltage was recorded. While the plating current was applied for 10 hours, the stripping current was applied until the voltage across the cell reached 3.0 V. After each plating step, the open circuit voltage was measured for 15 minutes, and an impedance spectrum was recorded. In combination with the characterization of the counter electrode in symmetrical test cells (Figure 2b), these spectra are used to evaluate the properties of the interface between the ceramic separator and the electroplated sodium electrode.

Three types of voltage profiles are found as summarized in Figure 5. All cells have vanishing galvanic voltages when there is sodium accessible at the zero-excess electrode due to their sodium counter electrode. Therefore, the voltage during cycling is of purely resistive nature.

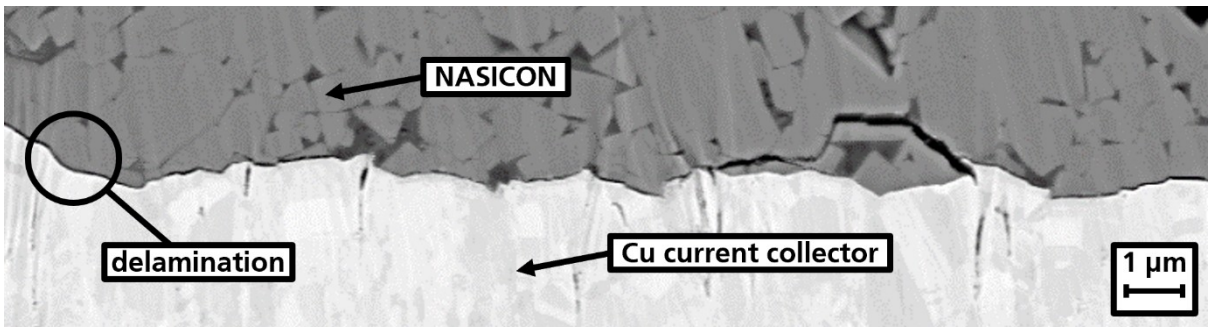

Figure 4. FESEM-Image of the current collector | NASICON interface. Partial delamination of the copper current collector from the NASICON substrate is observed.

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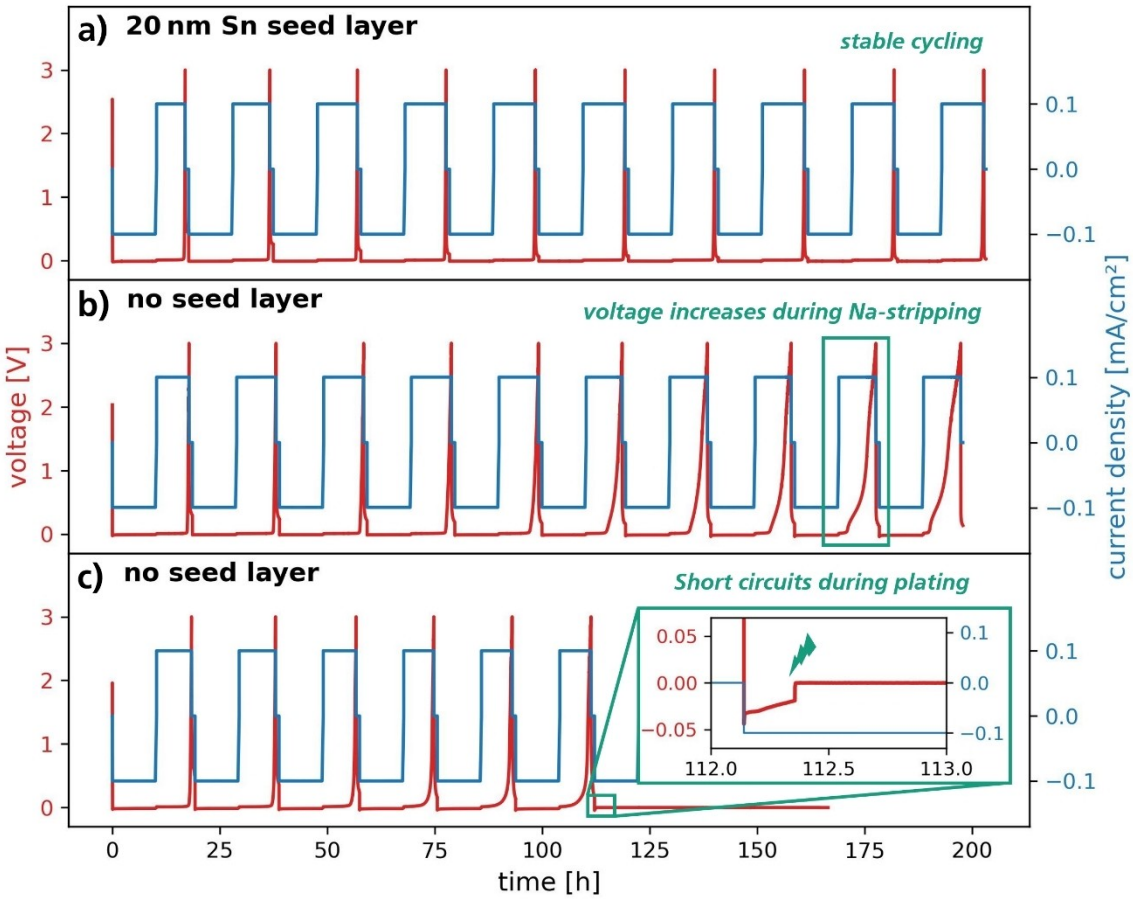

Figure 5. Depiction of the three characteristic voltage profiles (vs. sodium) found in model cells during cycling of 1 mAh/cm^2 at 0.1 mA/cm^2 for 10 cycles. a): Cell with seed layer (20 nm tin), showing stable cycling. b): Cell without seed layer showing voltage increases during sodium stripping. c): Cell without seed layer showing a short circuit during the 7th plating step due to dendrite formation (magnified).

2.4.1. Sodium Plating

During sodium plating at −0.1 mA/cm^2 an approximately constant voltage – and therefore approximately constant interfacial resistance – is observed in cells exhibiting a behavior akin to Figure 5. The only major change in voltage – and therefore in cell resistance – during sodium plating are sudden short circuits as indicated in Figure 5c. Upon removal of the current collector and any plated sodium at the zero-excess electrode, dendritic growth was visually identified as the root cause of the short circuits. The dendrites are visible in the white NASICON as veins of metallic grey, as depicted in Figure 6a. Upon application of mechanical stress, the NASICON pellet will consistently break at these weak spots, revealing the sodium plated inside the crack, as depicted in Figure 6b and c.

Although dendritic short circuits were also observed in cells with metallic seed layers (specifically, in two cells with indium and one with a zinc seed layer, out of a total of 12 cells with seed layers), they were significantly more prominent in cells lacking any seed layer. Of five cells assembled without seed

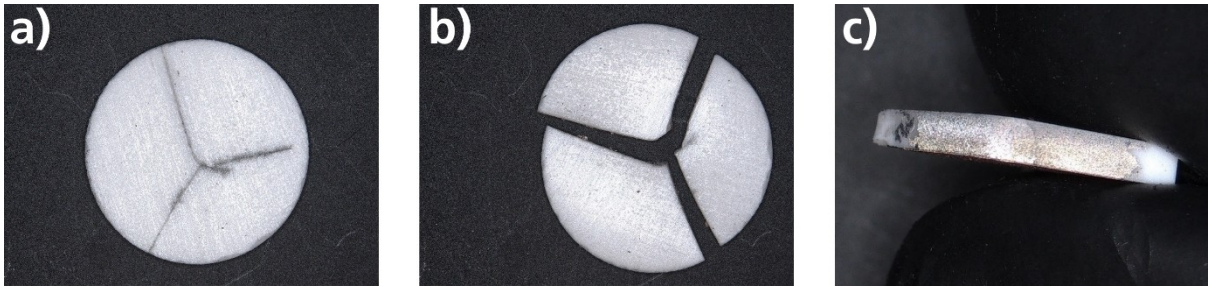

Figure 6. NASICON separator after short circuit during cycling of 1 mAh/cm^2 at 0.1 mA/cm^2. The copper current collector and any remaining sodium of the zero-excess electrode had been removed before. Dendritic sodium deposits are visible as grey veins in the white ceramic.

layer, only one could be cycled ten times at the discussed parameters without short circuit. Two of these cells without seed layer even exhibited the short circuit during the initial plating step, a behavior which was not observed in cells with seed layer. Therefore, this study suggests a dendrite suppressing effect of metallic seed layers. While conclusive statistical statements about variances among seed layer metals cannot be made due to the limited number of characterized cells, the data suggests that silver and tin seed layers exhibit the highest potential for dendrite suppression.

2.4.2. Sodium Stripping

An approximately constant voltage during sodium stripping at 0.1 mA/cm^2, followed by an abrupt rise in voltage to the limit of 3.0 V – as fixed in the measuring protocol – is observed in cells exhibiting a behavior akin to Figure 5a. This indicates a constant effective contact area between separator and plated sodium, and therefore a constant interfacial resistance, up until the voltage increase. The voltage increase is indicative of a rapid increase in interfacial resistance, once no more electrochemically active sodium is available at the zero-excess electrode. It is noteworthy that in cells exhibiting behavior analogous to that depicted in Figure 5a, the voltage prior to the final voltage increase during sodium stripping is approximately the same in absolute value as during sodium plating. This suggests a symmetrical behavior of the sodium | NASICON-interface at the zero-excess electrode with respect to current direction.

In contrast, the voltage profiles shown in Figure 5b or Figure 5c indicate interfacial degradation during cycling. Here, with increasing cycle number the voltage increases with each cycle at an earlier point within the stripping period at 0.1 mA/cm^2. Further, the slope of the rising voltage at the end of the cycle decreases. To investigate this phenomenon, the cell depicted in Figure 5b was subjected to an 11th plating/stripping-cycle. However, the stripping current was paused for 15 minutes during stripping at increased voltage. The resulting voltage profile is depicted in Figure 7a. Before the pause, the voltage increases above 2 V during sodium stripping. Once the stripping current is paused, the voltage drops to values below 0.1 V. Notably this voltage is of purely galvanic origin, as no current is flowing. Upon resumption of the stripping process after the pause, the current of 0.1 mA/cm^2 initially resumes at the same elevated voltage level, as before the pause. This proves, that indeed high interfacial resistances and not galvanic voltages are responsible for the stripping at increased voltages, as observed in cells corresponding to Figure 5b and c. Furthermore, any increase in interfacial resistance during sodium stripping prior to the pause was not alleviated by continued compressing of the cell stack at its constant stack pressure of 3 MPa during the pause of 15 minutes. Therefore, a delamination of the plated sodium electrode from the NASICON separator due to the formation of nanoscopic voids during the stripping process as observed Ortmann et al.[14] or by Barai et al.[18] is not a likely mechanism for the increasing interfacial resistance. The more likely explanation is a partial delamination of current collector and parts of the deposited sodium layer from the NASICON separator, due to insufficient adhesion.

All three of the five cells without seed interlayer, that did not short circuit during the initial plating step, exhibited a stripping behavior akin to Figure 5b or Figure 5c. In contrast, the homogeneous sodium stripping behavior shown in Figure 5a could be observed in cells with metallic seed layers of zinc, silver, indium, or tin. In Figure 7b, the last hour of each stripping step during the 10 cycles is depicted for an exemplary cell with a 20 nm thick silver seed layer. The curve does not change significantly with each cycle. Thus, Figure 7b demonstrates the possibility of realizing a stable zero-excess sodium metal electrode by sputter depositing current collectors on NASICON separators. In the case of a cell with an indium seed layer, the increase even becomes steeper with each cycle (Figure S7 in Supporting Information). However, the reproducible preparation of cells with such a stable performance shown in Figure 5a remains challenging. The deteriorating stripping behavior of Figure 5b or c was also observed in individual cells of all seed layer metals except for tin. From the limited statistic of three cells per seed layer metal, therefore no significant

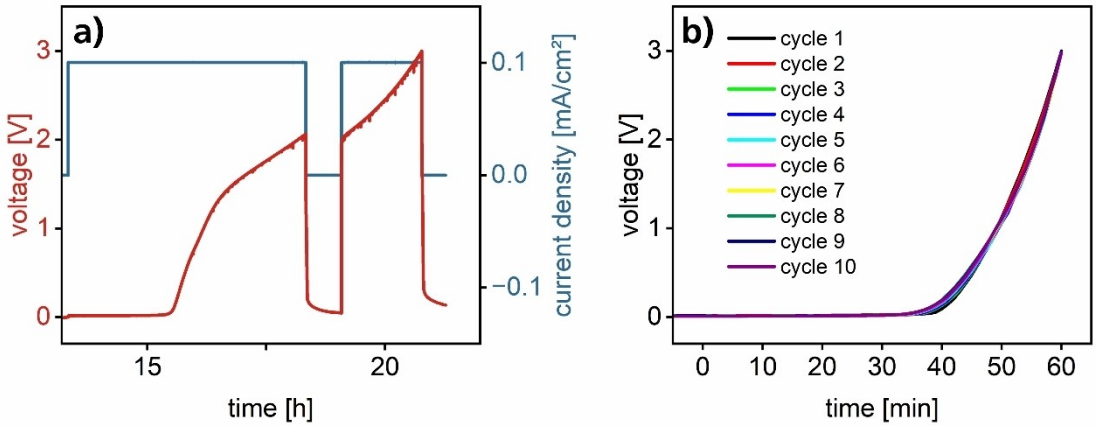

Figure 7. a): Additional 11th cycle of 1 mAh/cm^2 at 0.1 mA/cm^2 with pause after 5 hours stripping for 15 minutes of cell without seed layer (previous 10 cycles depicted in Figure 5b). No lowering of interfacial resistance while pausing during sodium stripping is observed. b): final hour of stripping until voltage limit of 3 V is reached for a cell with silver seed layer over 10 cycles (Ag cell 3).

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conclusions to the performance differences between zinc, silver, indium, and tin becomes apparent. However, a stabilizing effect on sodium stripping of a seed layer in comparison to uncoated substrates is suggested.

2.4.3. Reversibility and Sodium Loss

To quantify reversibility, the coulombic efficiency (*CE*) is calculated according to Equation (1). 15 out of the 17 cells cycled for 1 mAh/cm^2 at 0.1 mA/cm^2 were analyzed, i.e. excluding the two cells without seed layer, that exhibited cell failure due to dendritic shorts right at the start of the initial plating step. The average coulombic efficiency $<CE>$ for each of the five cell species (no interlayer, zinc, silver, indium, tin seed layer) is calculated by averaging *CE* over all cycles of the respective cell species, with cycles after a short circuit being omitted. The *CE* of each cycle ($<CE>$) and the maximum *CE* (CE_{max}) per seed layer modification observed in a single cycle are summarized in Figure 8. Cells with silver or tin seed layers showed the highest degree of reversibility with a $<CE>$ of 89% and 90%, respectively and CE_{max} values of 98%.

Most of the 15 cells show a tendency of *CE* increasing with increasing cycle number. E.g. for a cell with 20 nm tin interlayer, *CE* starts below 80% and increases to a maximum of 98%. A likely explanation for this is found by FESEM imaging of cross sections of the zero-excess electrode in cells at different stages of cycling. As depicted in Figure 9a, after one sodium plating step at −0.1 mA/cm^2 for 10 hours, the sputter deposited copper current collector shows sodium filled cracks, as confirmed by Energy-Dispersive X-ray spectroscopy (EDX). FESEM-preparation of cells after the 10 cycles at 0.1 mA/cm^2 in the stripped state, reveal that similar sodium filled cracks are left in the current collector, as depicted in Figure 9b. Therefore, a likely mecha-

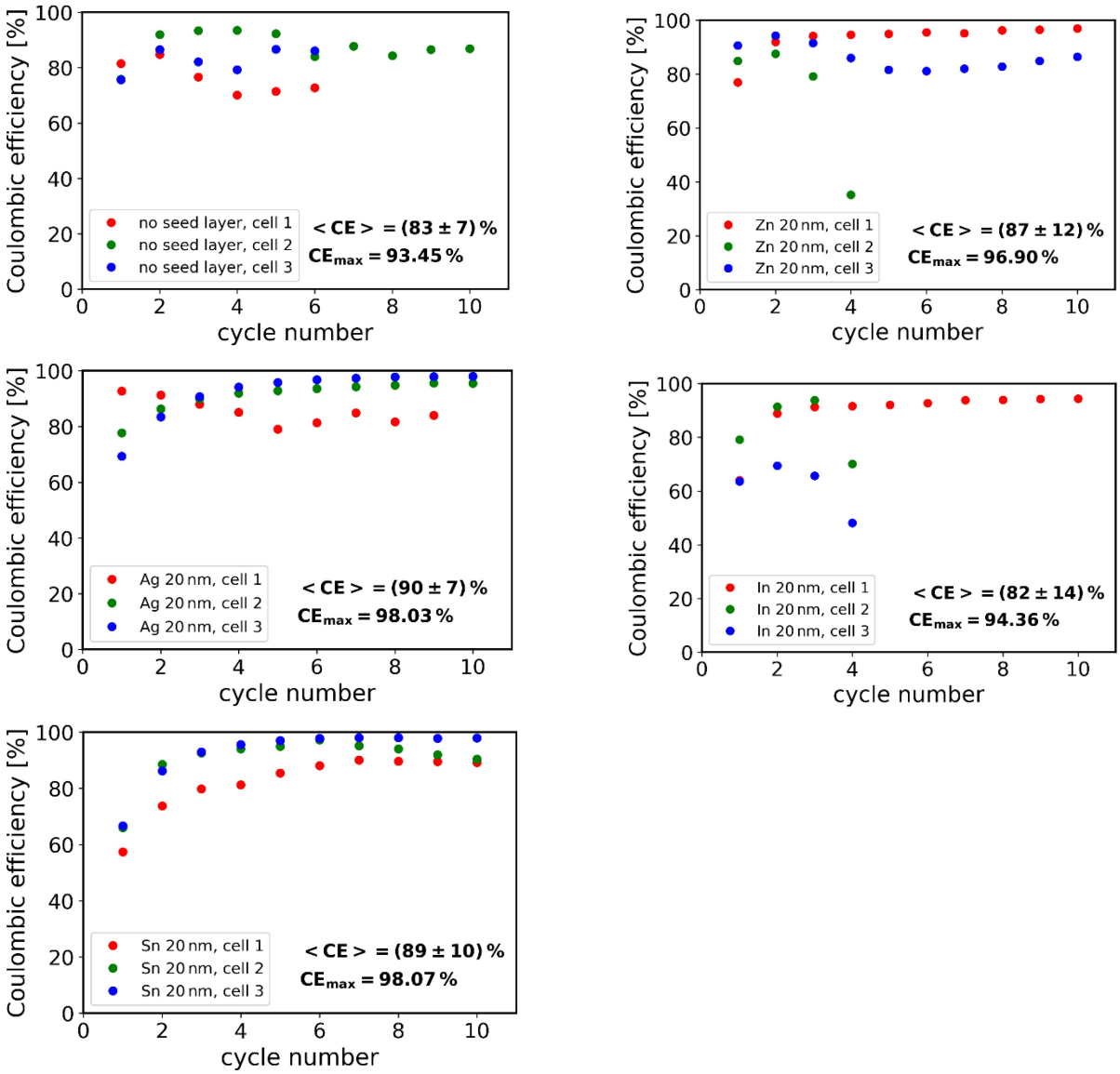

Figure 8. Coulombic efficiency (CE) of model cells during cycling of 1 mAh/cm^2 at 0.1 mA/cm^2. The highest CE per cell species (CE_{max}) and the average $<CE>$ over all dendrite-free cycles is depicted per cell species.

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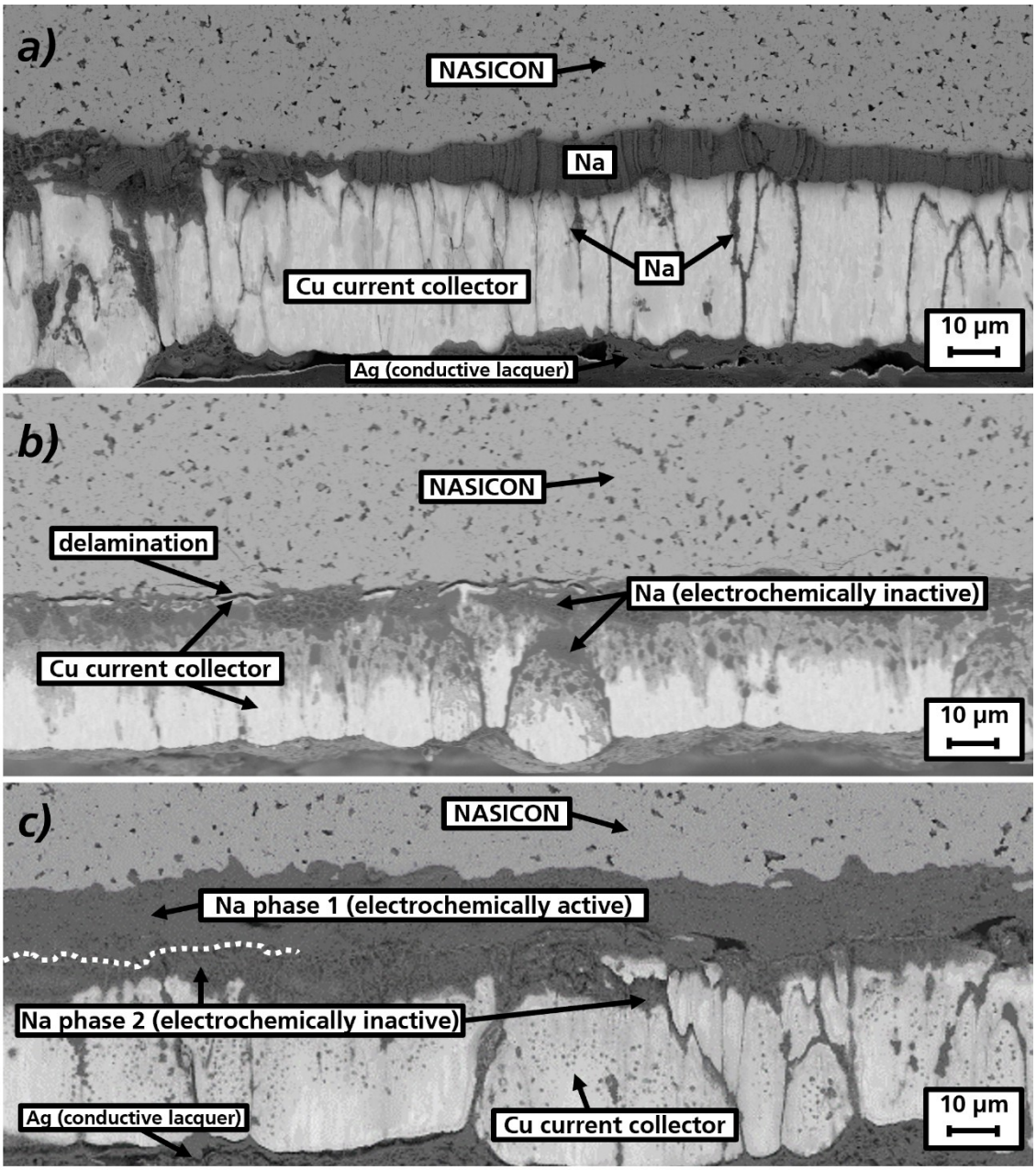

Figure 9. FESEM-imaging of cross sections at the zero-excess electrode in different stages of sodium cycling of 1 mAh/cm^2 at 0.1 mA/cm^2. The "Ag (conductive lacquer)" was applied for FESEM preparation after the experiment. a): Cross section prepared after one plating step. b): Cross section prepared after 10 cycles in the stripped state. c): Cross section prepared after 10 cycles and an 11th plating step.

nism for the initially low *CE*s of most cells is the irreversible filling of cracks and voids in the copper current collector with sodium during the first plating cycle.

In the subsequent cycles, additional electrochemically inactive sodium is formed in these cracks and voids at the current collector. This is visible in Figure 9b, a cross section of a cell in the stripped state after 10 cycles. Here, a sodium layer with a thickness of approximately 6.3 µm is observed. This thickness is in the same order of magnitude as the expected thickness of 8.8 µm, calculated from the total amount of sodium lost during cycling prior to sample preparation ($\sum(1 - CE) \cdot 1$ mA/cm^2 = 0.72 mAh/cm^2 and assuming a sodium density of 0.971 g/cm^3). This sodium layer is partially delaminated from the NASICON, but not from the current collector. This indicates high work of adhesion to the current collector and low work of adhesion to the NASICON-separator. Such low adhesion at the electrochemically active interface might lead to high interfacial resistances between this sodium layer and the NASICON due to current constriction.[14] Consequently, voltages below 3 V are insufficient to dissolve this inactive sodium layer during stripping.

The layer of electrochemically inactive sodium at the copper current collector is also visible in cross sections of cells in the plated state at later stages of cycling, as exemplified in

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Figure 9c. The cross section was prepared after sodium cycling of 1 mAh/cm^2 at 0.1 mA/cm^2 for ten complete cycles plus an eleventh plating step with the same parameters. Two distinct regions of plated sodium can be identified. One region closer to the NASICON interface and one region at the current collector interface, separated by a distinct phase boundary. A likely explanation is, that the first region at the NASICON-interface was deposited in the eleventh plating step, while the second region at the current collector is an agglomeration of sodium which was not stripped in the stripping step precursing the final eleventh plating. This hypothesis is again supported by an estimation of layer thicknesses: 1 mAh/cm^2 corresponding to 8.8 μm sodium that was plated in the eleventh plating step. For the ten complete cycles a charge of $\sum(1-CE)\cdot 1\ \text{mAh/cm}^2 =$ 1.03 mAh/cm^2 irreversible loss was calculated, corresponding to 9.1 μm electrochemically inactive sodium. The two calculated sodium thicknesses align with the observed sodium thicknesses of Figure 9c, although there are significant uncertainties in the sodium density due to porosity.

While the loss of electrochemically inactive sodium can be visually traced to the sputter deposited copper current collector, no significant sodium loss is observed at the NASICON separator. This phenomenon is mechanistically distinct from that observed in zero-excess batteries with liquid electrolytes, where the loss mechanism was found to be dominated by reactions with the liquid electrolyte.[24–26]

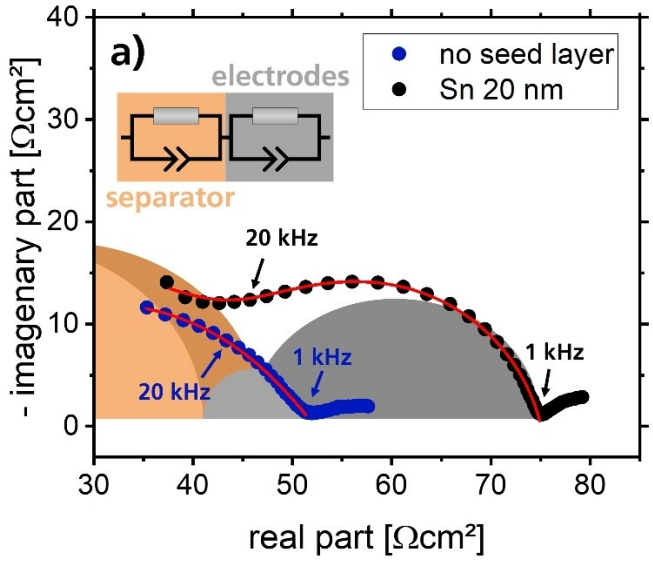
2.4.4. Interfacial Resistance at the Zero-Excess Electrode

The contact between the sodium layer which is plated in the zero-excess electrode and the NASICON separator can be quantified by the impedance spectra, measured after each plating step. The extraction of the interfacial resistance is illustrated in Figure 10a for the impedance of the most stable cells with no seed layer and with a 20 nm tin seed layer, respectively (see Figure 5a and b), in both cases after the initial plating step.

As graphically indicated in Figure 10a, the low frequency circuit, attributed to the interfacial resistance of the electrode corresponds to frequencies between approximately 1 kHz and 20 kHz. Out of the two cells in Figure 10a, the cell without a seed layer has the lower interfacial resistance at $(10\pm4)\ \Omega\text{cm}^2$ after the first plating step. This is also the lowest interfacial resistance of all the 17 cells which were characterized. The interfacial resistance of the 20 nm tin cell in Figure 10a is estimated as $(33\pm1)\ \Omega\text{cm}^2$.

The lowest individually measured interfacial resistance $R_{\text{interface, minimal}}$ for each cell type is summarized in Figure 10b. However, the interfacial resistance varies substantially across cells of identical assembly. As previously stated, the probable reason for this high variance in interfacial resistance, is the variance in the partial delamination of the sputter deposited current collector from the NASICON (see Figure 4). This results in a high variance of the effective contact area and therefore current constriction in the NASICON at the zero-excess electrode interface. While the lowest interfacial resistance of $(10\pm4)\ \Omega\text{cm}^2$ in these cells with a roughened NASICON surface at the zero-excess electrode is significantly higher than the $(0.98\pm0.23)\ \Omega\text{cm}^2$ found during the evaluation of the counter electrode for the interface between bulk sodium and the roughened NASICON, it is significantly lower than any interfacial resistance between a sodium and polished (P4000) NASICON which was achieved in this study (for electrodes with and without excess).

No clear connection between the initial interfacial resistance of a cell and its stability during cycling is found. E.g., although the most stable cell with no seed layer is initially lower in



b)

	$R_{\text{interface, minimal}}$
No seed layer	10 ± 4
20 nm Zn	11 ± 5
20 nm Ag	19 ± 4
20 nm In	32 ± 3
20 nm Sn	26 ± 2

Figure 10. a): Impedance spectra (1 MHz - 1 Hz, 30 °C) of the lowest resistance cell without interlayer and with interlayer (20 nm of Sn) after plating of 1 mAh/cm^2 at 0.1 mA/cm^2. Fitted equivalent circuit to extract the interfacial resistance at the zero-excess electrode. b): Minimal resistance and constant phase element of the sodium | NASICON-interface at the zero-excess electrode in the plated state per seed layer modification.

interfacial resistance compared to the cell with 20 nm of tin as seed layer featured in Figure 10a the voltage profiles during cycling (Figure 5a and b) indicate higher interfacial stability for the cell with the tin seed layer. This is however reflected in the evolution of the interfacial resistance during cycling. As depicted in Figure 11, the interfacial resistance after each plating step increases for the less stable cell without seed layer and decreases for the most stable cell with 20 nm of tin seed layer. Decreases in interfacial resistance during cycling are found in no cell without seed layer, but in several of the cells with metallic seed layers. A more pronounced example of a cell with 20 nm of zinc as seed layer which showed a voltage profile corresponding to Figure 5a during cycling, is added in Figure 11.

2.5. Initial Sodium Nucleation at the Zero-Excess Electrode

To investigate the influence of metallic interlayers on the initial sodium deposition, model cells where assembled, as depicted in Figure 2a. The zero-excess electrode was prepared by sputter depositing interlayers of zinc, silver, indium or tin onto the polished NASICON surface at thicknesses of 100 atomic layers each – corresponding to thicknesses between 24 and 30 nm. Subsequently, the copper current collector was applied at a thickness of 5 nm via thermal vapor deposition. The cell stack pressure was 3 MPa. As a reference, cells without any metallic seed layer were similarly assembled. A current of $j = -0.01$ mA/cm^2 was applied for a duration of 10 hours, to transport sodium from the counter electrode to the zero-excess electrode.

The characteristic voltage profile during the first 2000 s after current application is depicted in Figure 12a, for each seed layer modification. The cell voltage is the sum of the galvanic voltage and the ohmic voltage drop at the applied current density:

$$U = U_{galvanic} + U_{ohmic} = U_{galvanic} + R_{cell} \cdot j \quad (2)$$

In cells without additional seed layer, as soon as the current reaches -0.01 mA/cm^2 at time $= 0$ s, the voltage drops almost instantly from a volatile open circuit voltage above 1 V to below 0 V. This voltage drop is easily explained by the nucleation of metallic sodium at the interface of the bare copper current collector and the sodium solid electrolyte. Consequently, an electrode symmetrical setup quickly emerges with pure metallic sodium at both electrodes and $U_{galvanic}$ vanishes. In the following, the time at which this nucleation of metallic sodium becomes apparent is labeled as the nucleation pointP_N. Following from Equation (2), the measured voltage at times after P_N is equal to the pure ohmic contribution. The voltage in the vicinity around P_N is magnified in Figure 12b. After P_N U_{ohmic} increases and thus the interfacial resistance decreases as the negative current density remains constant. This observation is most likely due to an increase of the electrochemically active contact area between the plated sodium layer and the solid electrolyte as the sodium nuclei grow.

For cells with 100 atomic layers of seed metal Figure 12a shows again a voltage decrease starting from the volatile open circuit voltage above 1 V. However, for any seed layer metal the voltage decay is much slower compared to the voltage drop in case of the bare copper current collector. A likely explanation is the formation of alloys between the reduced sodium atoms and the seed layer metals at the interface. Following this hypothesis, $U_{galvanic}$ decays gradually as more sodium dissolves in the alloy. Eventually, no more sodium can be dissolved in the alloy and the electrochemical reaction switches from alloy formation to sodium nucleation. This heterogenic reaction is indicated by a discontinuity in the voltage profiles for cells with silver or indium seed layers at P_N in Figure 12a and b. For cells with zinc or tin seed layers, this behavior is significantly less pronounced, resulting in a less clear nucleation point.

None of the seed layer cells exhibits a distinct short overvoltage minimum after P_N as observed in cells with no seed layer. Following the assumption that P_N marks the switch from alloy formation to sodium metal deposition and the voltage

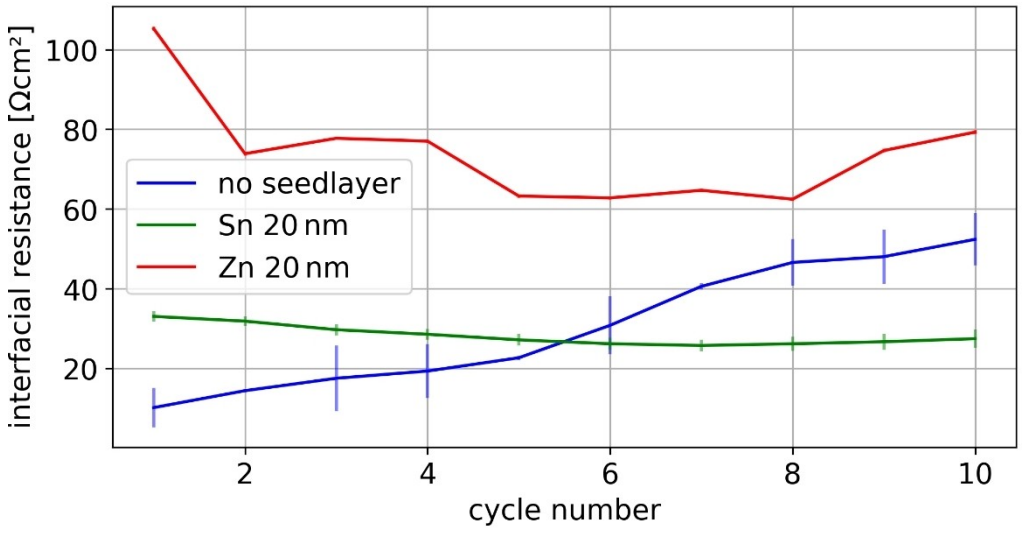


Figure 11. Evolution of the interfacial resistance at the zero-excess electrode in the plated state during 10 cycles of 1 mAh/cm^2 at 0.1 mA/cm^2.

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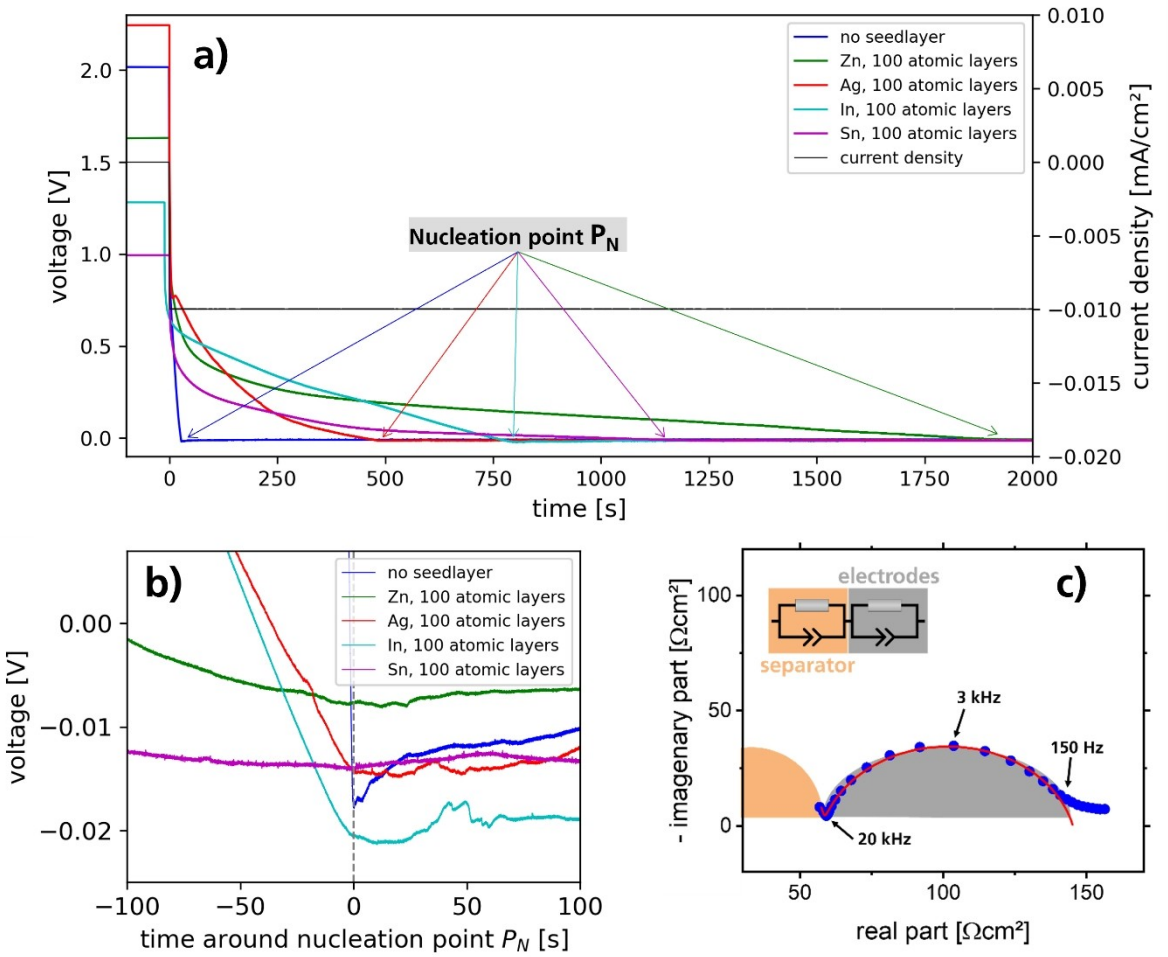

Figure 12. Sodium deposition at −0.01 mA/cm² for 10 h at zero-excess electrodes with polished NASICON surface. a): Initial 2000 seconds of the deposition, b): magnification at the individual nucleation point, c): Impedance spectrum for a cell with tin as the seed layer metal, exhibiting the lowest measured interfacial resistance after sodium deposition.

minimum under discussion is related to the growth of an electrochemically active interfacial area between sodium nuclei and the solid electrolyte, the initial sodium metal nucleation at the interface is therefore smoother in cells with any of the four seed layer metals.

The voltage after the sodium metal nucleation is almost the same for all cells, with or without seed metal, indicating an electrode symmetrical setup with vanishing $U_{galvanic}$ as discussed above. It is therefore concluded that no significant concentration of any seed layer metal atoms remains at the interface after the deposition of −0.01 mA/cm² over 2000 s. An additional influence of the seed layers which goes beyond the initial formation of the sodium|solid-electrolyte-interface is therefore unlikely.

After the sodium deposition for 10 hours, impedance spectra were recorded. Cells with tin as the seed layer metal exhibited the lowest interfacial resistance ranging as low as (85 ± 5) Ωcm² in spectrum Figure 12c. By comparison with the impedance spectrum of the symmetrical cell with roughened NASICON separator (Figure 3c), the resistive contribution of the dominant semi-circle is separated from the contribution of the separator as the desired interfacial resistance. This low frequency circuit corresponds to frequencies between approximately 150 Hz and 20 kHz. The interfacial resistance between the opposing roughened side of the NASICON separator and the sodium metal counter electrode is neglectable, as previously discussed.

Notably, by comparison with Figure 3b it is found, that this zero-excess electrode interfacial resistance of (85 ± 5) Ωcm² is smaller at a stack pressure of 3 MPa than the (206 ± 74) Ωcm² interfacial resistance between polished NASICON separators and sodium metal electrodes applied as metal foils. This demonstrates that the in-situ formation of the sodium metal electrode on polished NASICON surfaces in the zero-excess electrode setup is a viable alternative to the more conventional approach of applying sodium foil in terms of interfacial contact.

2.6. Investigation of the Interfacial Tension

Contact angles of liquid sodium with the different seed metals were measured, as they may relate to the interfacial tension at

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the zero-excess electrode's electrochemically active interface. The result is depicted in Figure 13. Following Young's equation

$$\cos\theta = \frac{\gamma_{SG} - \gamma_{SL}}{\gamma_{LG}}, \quad (3)$$

with surface tensions γ_{SG} and γ_{LG} of solid and liquid and the interfacial tension γ_{SL} a low contact angle is indicative for low interfacial tension. A significantly higher wettability is found for the silver and tin coatings, as indicated by the lower contact angles of $(82 \pm 2)^\circ$ and $(92 \pm 7)^\circ$, compared to the contact angle $(126 \pm 2)^\circ$ for the uncoated NASICON-samples and a contact angle of approx. 114° for copper sputter deposited on polished silicon.

As silver and tin showed the highest degree of reversibility (see Figure 8), their high wettability does not falsify the natural hypothesis of a decrease in interfacial tension at the sodium | NASICON-interface, and thus better adhesion as a driving mechanism for homogeneous and reversible sodium plating. However, as apparent from Figure 12a and b, while tin exhibited the smoothest sodium nucleation behavior with no clearly visible nucleation point P_N, silver did not show a particularly noticeable smothering of the nucleation curve during these nucleation experiments. Most likely, benefits of metallic interlayers during sodium nucleation are not purely explained by the modification of interfacial tension, but the kinetics of alloy formation must also be considered.

Moreover, in contrast to liquid electrolyte batteries, strong adhesion between sodium and the current collector is not necessarily an advantage, as delamination of the current collector in this case leads to delamination of sodium from the NASICON (see Figure 9b). Therefore, while minimizing the tension of the sodium | NASICON-interface with suitable interfacial modifications is most likely beneficial for electrode stability, modifications of the current collector | sodium interface to increase interfacial tension and lessen work of adhesion might be a complimentary promising approach.

3. Conclusions

This study demonstrates that sputter deposition of copper current collectors on solid electrolytes is a promising route to cycle stable zero-excess sodium metal electrodes for solid-state batteries. Model cells with a sodium metal counter electrode, acting as a sodium reservoir, and NASICON separators prove:

a. The sputter deposited copper current collector needs a thickness of at least 30 μm to prevent sodium penetration during its plating with sodium. When 1 mAh/cm² of sodium was plated onto a 5 μm copper layer thermally vapor deposited on NASICON, the thin copper layer was consistently penetrated by the deposited sodium. The same was true for a 10 μm sputter deposited copper collector, but not for 30 μm sputter deposited copper.
b. Roughening the NASICON separator surface enhances current collector adhesion and improves the electrode contact, resulting in significantly lower interfacial resistances. While DC sputter deposition achieved 30 μm at high rates, the resulting copper current collector completely delaminated from polished NASICON, rendering the current collector unusable. However, adequate adhesion was achieved when the copper was sputter deposited on P120 roughened NASICON. Further, roughening lowers the interfacial resistance e.g. of the sodium foil counter electrodes:

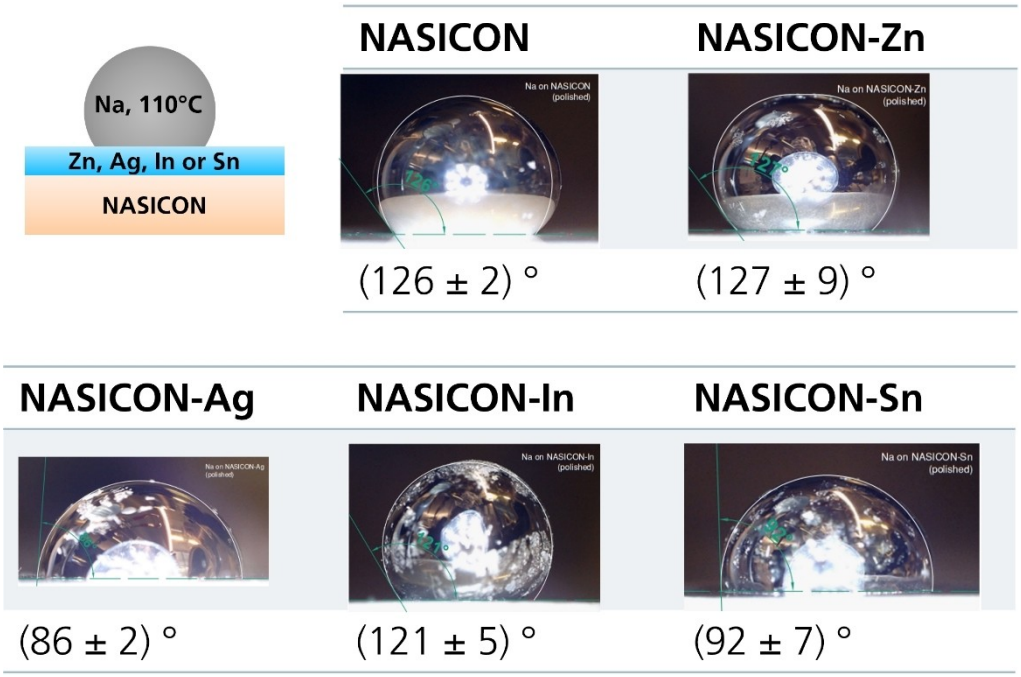

Figure 13. Qualitative comparison of interfacial tension between liquid sodium and NASICON at 110 °C via contact angle measurements for different interfacial modifications: unmodified and with 20 nm of zinc, silver, indium, and tin.

On NASICON sanded at grits of P120 (0.98 ± 0.23) Ωcm^2 at 3 MPa were measured compared to (206 ± 74) Ωcm^2 on P4000 polished NASICON at the same pressure or (36 ± 12) Ωcm^2 on polished NASICON at 19.8 MPa. Likewise, a low resistance of (10 ± 4) Ωcm^2 was measured between roughened NASICON and in-situ plated sodium. Roughing is likely to improve sodium wetting, thus reducing current constriction.

c. Seed layers of zinc, silver, indium, or tin improve cell cyclability substantially, with silver and tin showing the most stabilizing effects. The six cells with these two seed layers showed no sodium penetration through the NASICON separator in contrast to only one of the five cells without a seed layer. In the other four cells sodium dendrites formed through the NASICON during plating. This dendrite formation is probably caused by poor adhesion and thus locally high current densities. Further, the six cells showed stable voltage profiles over ten cycles, with average Coulombic efficiencies of 89% and 90%, respectively, and a maximum of 98% by the tenth cycle. They thus outperformed the cell without seed layer and without dendrite formation that showed an average Coulombic efficiency of 83% and a maximum of 93%. Cross-sectional FESEM imaging indicated that sodium loss during cycling, i.e. Coulombic efficiencies below 100%, is primarily due to copper current collector degradation, rather than sodium reactions with the solid electrolyte, contrasting with mechanisms in liquid electrolyte batteries. This favorable influence of seed layers was analyzed in nucleation experiments and contact angle measurements. As expected, no alloy formation was observed between sodium and 5 μm thick copper current collectors on polished NASICON, leading to a small overvoltage before nucleation. In contrast, layers of 100 atoms of any of the four seed metals promoted alloy formation with sodium during plating, particularly with tin. Tin made the nucleation overpotential disappear and lowered the interfacial resistance to (85 ± 5) Ωcm^2, which outperformed any other interface with polished NASICON separator and sodium metal electrode at 3 MPa (both in-situ deposited and applied as sodium foil). Contact angle measurements showed improved wettability of silver- and tin-coated NASICON surfaces, likely reducing interfacial tension and enhancing contact between sodium and NASICON, leading to more uniform and reversible sodium plating.Despite their overall advantages, the differences among different seed layer metals in cycling experiments are weak. This may partly be due to challenges with reproducible cell preparation and thus current collector delamination. All seed layers form sodium alloys thereby smoothening the initial plating and decrease electrochemical nucleation overpotential. In addition, seed layers may act as adhesive layers, improving current collector attachment and preventing high local current densities.

Experimental Section

Preparation of the Symmetrical Cells of Two Sodium Counter Electrodes

The NASICON separator was prepared by sintering uniaxially pressed $Na_{3.4}Zr_2Si_{2.4}P_{0.6}O_{12}$ powder pellets with a diameter of 20 mm at 1350 °C for 30 min. (Powder provided by M.-T. Gerhards, E. Dashjav and F. Tietz from Forschungszentrum Jülich). The sintered NASICON separators have a diameter of 15 mm and a thickness of 1.5 mm. The ceramic surface of the NASICON separator is modified in roughness and cleaned via surface sanding with medium coarse (P600 grit) silicon carbide sandpaper in dry air down to a thickness of 1.4 mm. Samples are then either roughened with P120 grit sanding paper or polished, in succession with P1200, P2500 and P4000 grit sanding paper. Residues are blown off with the compressed dry air gun.

The symmetrical cells with a NASICON separator either polished on both sides or roughened on both sides are assembled by contacting sodium foil at 97 °C and 10 MPa in argon atmosphere. The cell stacks were transferred into EL-CELL® Pat-cell-force battery housings (EL-CELL GmbH) and thermalized to 30 °C in a temperature chamber for 90 minutes without significant stack pressure. Stack pressure was then increased and monitored during the electrochemical measurement.

Preparation of Zero-Excess Cells

The NASICON separator was prepared as described in Section 4.1. above. A magnetron AC-sputter deposition source (OPTIvap Series 3G Magnetron-Sputtersource Gencoa®) is used to sputter deposit zinc, silver, indium, or tin seed layers onto the sanded NASICON surface. The deposition is carried out in argon atmosphere at 6 μbar pressure, a plasma power of 50 W and with 2-inch sputter targets of 99.99% purity (Kurt J. Lesker Company). These seed layers were applied with a thickness error of ±10%. Layer thickness was controlled via deposition time and sputter deposition rate. The latter was calibrated by depositing a thicker layer for a longer time onto three test wafers of known weight. From the weight of the deposited layer and the deposition time, the deposition rate was calculated. The results were verified by thickness measurement via an X-ray fluorescence meter (FISCHERSCOPE® X-RAY XDV®-SDD, Helmut Fischer GmbH). Onto the seed layer, the copper current collector is sputter deposited. Here, a DC-sputter deposition source (3-inch target, FHR Anlagenbau GmbH) at 250 W and 6 μbar process pressure is used, to achieve higher deposition rates at lower particle energies and therefore lower layer tensions.

To prepare the sodium metal counter electrode, the NASICON separator is first roughened with P120 grit silicon carbide sandpaper in argon atmosphere to increase the roughness and facilitate adhesion between the sodium and the ceramic. The benefit of such surface treatment for the sodium metal counter electrode was previously demonstrated by Hüttl at al. and Ortmann et al.[14,23] Polishing the surface led to a poorer interfacial contact. Subsequently, sodium foil is placed onto the ceramic. The cell package is then tempered at 97 °C and 10 MPa uniaxial pressure in argon atmosphere, to achieve a good contact to the counter electrode.

The assembled cell stacks are hermetically sealed in EL-CELL® Pat-cell-force battery housings (EL-CELL GmbH) at a uniaxial stack pressure of 3 MPa.

Preparation of Zero-Excess Cells for Nucleation Experiments

The sodium metal counter electrode was prepared on a roughened (P120) NASICON. The zero-excess electrode was prepared thereafter by polishing the other side of the NASICON substrate to a grit of P4000 (whereas NASICON roughened on both sides was used in Section 2.4. for the cycling experiments). Thereafter seed layer metals were sputter deposited onto the polished side. For all seed metals, the layer thickness was standardized to 100 atomic layers to facilitate comparisons in alloy formation: 24 nm for zinc, 26 nm for silver, 29 nm for indium, and 30 nm for tin (in contrast to the uniform 20 nm thickness used in Section 2.4.). A 5 μm thin copper layer was thermally evaporated from a crucible in a vacuum of 0.01 μbar (in contrast to 30 μm sputter deposited in Section 2.4.). Layer thickness was monitored using a quartz crystal microbalance. The cell stacks were sealed as discussed above, at a stack pressure of 3 MPa. The cells were thermalized to 30 °C. The cell voltage was monitored during the experiment. A current of $j = -0.01$ mA/cm^2 was applied for a duration of 10 hours (in contrast to -0.1 mA/cm^2 in Section 2.4.).

Electrochemical Characterization

All electrochemical characterizations presented in this study are conducted in a temperature chamber at 30.0 °C using a VMP3 potentiostat (BioLogic).

Impedance Spectra

Electrochemical impedance spectra (EIS) were recorded between 1 MHz and 1 Hz at 30 °C with a voltage amplitude of 25 mV to assess interfacial resistances. A serial circuit, consisting of two resonant circuits, each containing a resistor and a constant-phase element, was fitted to the recorded impedance data. The resistive contribution of the spectrum's low frequency semicircle is extracted as the desired interfacial resistance. Contributions at frequencies below this semicircle are due to stripping and plating of the sodium electrodes and are therefore excluded from the fit. Contributions at frequencies above the semicircle are attributed to the impedance of the NASICON separator and are also excluded from the fit. Even higher frequencies, which would have allowed a distinction between bulk and grain boundary conductivity of the solid electrolyte, were inaccessible due to the 1 MHz high frequency limit in this study.

Cross Section Imaging

To image the interfaces in the assembled model cells, cross sections of the cells were investigated using a Field Emission Scanning Electron Microscope (FESEM, Carl Zeiss Crossbeam 550 microscope). Therefore, model cells at different stages of cycling were transferred into an argon filled glovebox. The cell housing was disassembled. Subsequently, ion beam slope cutting under inert conditions (Gatan PECS II Model 682) was used to cut through the cell stack and reveal its polished profile. The sample was coated with graphite, glued to an appropriate sample holder with conductive silver lacquer and inertly transferred into the FESEM chamber.

Contact Angle Measurement

To qualitatively compare the influence of seed layers on the interfacial tension between the separator and sodium, contact angle measurements with liquid sodium were carried out. To this end, zinc, silver, indium, or tin were sputter deposited at (20 ± 2) nm thickness onto NASICON, as described above. The coated NASCION substrates were placed and heated to 110 °C on a heating plate inside of an argon filled glovebox. In the same glovebox, sodium was molten in a stainless-steel crucible at 110 °C and dripped onto the coated NASCION with a pipette, at defined drop size. The sodium drops on the ceramic surface were photographed in profile. From these photographs, the contact angle was geometrically determined.

Author Contributions

Ansgar Lowack, Henry Auer and Paula Grun designed the experiments. Rafael Anton prepared the solid electrolyte pellets. Ansgar Lowack and Paula Grun prepared all cells and performed the experiments. Ansgar Lowack wrote the manuscript. All authors discussed the results and contributed to the preparation of the manuscript.

Acknowledgements

This study was funded by the German Federal Ministry of Education and Research (BMBF) in the framework of the project HeNa (FKZ 03XP0390 A). Special thanks are extended to our project partners Marie-Theres Gerhards, Enkhtsetseg Dashjav and Frank Tietz from Forschungszentrum Jülich for providing their NASICON powder which was used as solid electrolyte for this study. Open Access funding enabled and organized by Projekt DEAL.

Conflict of Interests

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords: Sodium batteries · Solid-state · Zero-excess electrodes · Sputter deposition · Vapor deposition · Seed metals · Seed layers

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Manuscript received: September 22, 2024
Accepted manuscript online: October 25, 2024
Version of record online: November 19, 2024