

Article

Fault Characterization for AC/DC Distribution Networks Considering the Control Strategy of Photovoltaic and Energy Storage Battery

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Abstract: In order to cope with the failure of existing fault analysis schemes for AC/DC distribution networks with a high proportion of distributed generations, this paper proposes a fault characteristic analysis method for AC/DC distribution networks that considers the influence of distributed generation control strategies. Firstly, a transient model for the AC/DC distribution network connected to distributed generations is built. Then, the fault characteristics of the AC/DC distribution network in different stages, such as the capacitor discharge stage, inductive renewal stage, and steady state stage, is analyzed. Finally, detailed simulation analysis is conducted using PSCAD/EMTDC to validate the effectiveness of the developed scheme by the superior approximation performance between simulated curves and calculated curves.

Keywords: distributed generations; transient model; fault characterization; control strategies



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1. Introduction

The construction of DC distribution networks is conducive to the massive access of distributed generations [1], which can significantly improve the transmission capacity and power quality of the distribution network and has broad development prospects [2]. However, AC distribution networks are mature, and AC power sources and loads are still the main components of distribution networks. Therefore, DC distribution networks cannot completely replace AC distribution networks. Building hybrid AC/DC distribution networks is the future development trend in distribution networks [3]. An AC/DC hybrid distribution network contains a large number of distributed generations and electronic interfaces, and the fault analysis and protection schemes of traditional distribution networks may fail. Therefore, studying the fault characteristics analysis of AC/DC hybrid distribution networks with distributed generations is of great significance.

In recent years, numerous experts and scholars have conducted a series of studies on the fault analysis of AC/DC distribution networks. In [4], the oscillations in active and reactive power introduced by voltage source converters (VSCs) were discussed, which can help derive the power peaks during fault ride-through. In [5], the authors proposed fault current calculation methods in multi-terminal DC networks so as to assess the fault level. Short-circuit faults using an JFET-based solid state circuit breaker in a residential DC microgrid were addressed in [6]. In [7], the characteristics of polar faults on high-voltage DC transmission lines were discussed. The effects of different distributed generations on short-circuit fault characteristics in DC networks were compared in [8]. Starting from traditional fault characterization, different sources of short-circuit currents and their corresponding fault currents were analyzed in [9]. A fault detection index was proposed,

which demonstrated that there exists a direct correlation between the two [10]. The faults of sensors on both sides of the converters at the grid side were considered and a nonlinear estimation scheme for the presence of the faults was devised in [11,12]. Although the above-mentioned studies have addressed a large variety of topics and provided analytical insights, none of these papers propose an equation for fault current expression that determines the fault stage based on the state of the components. Additionally, the control schemes of power electronic devices in the circuit structure also will affect the analysis of fault currents [13–15]. Therefore, when designing fault diagnosis and protection for power grids [16,17], it is necessary to consider the impact of control schemes for power electronic devices. However, limited literature addressing the impact from different control schemes of distributed generation converters on fault currents currently exists.

To overcome the aforementioned problem, a new short-circuit current calculation method is developed in this paper. The topological model of the AC/DC distribution network containing a distributed generation is constructed first. On this basis, the system fault response mechanism of the AC/DC distribution network when an inter-pole short-circuit fault occurs on the DC side is analyzed. Finally, simulation verification is carried out to compare and analyze the fault characteristics under different control strategies for distributed generations such as photovoltaic (PV) and energy storage batteries (ESBs).

The rest of the paper is organized as follows: The AC/DC distribution network is presented in Section 2. In Sections 3 and 4, the proposed idea is discussed. In Section 5, a simulation and comparisons under different situations are built to demonstrate the applicability of the proposed method. Section 6 concludes the paper.

2. AC/DC Distribution Networks

In order to comprehensively observe the influence of the distributed generation control strategies on fault characteristics, the AC/DC distribution network structure is selected as a radial single-ended power supply.

Considering the advantages of the large capacity and mature technology of VSCs [18], an AC/DC distribution network based on a VSC is constructed, as shown in Figure 1. A VSC is connected to the AC/DC distribution network, and PV and ESBs are connected to the DC side as distributed generations.

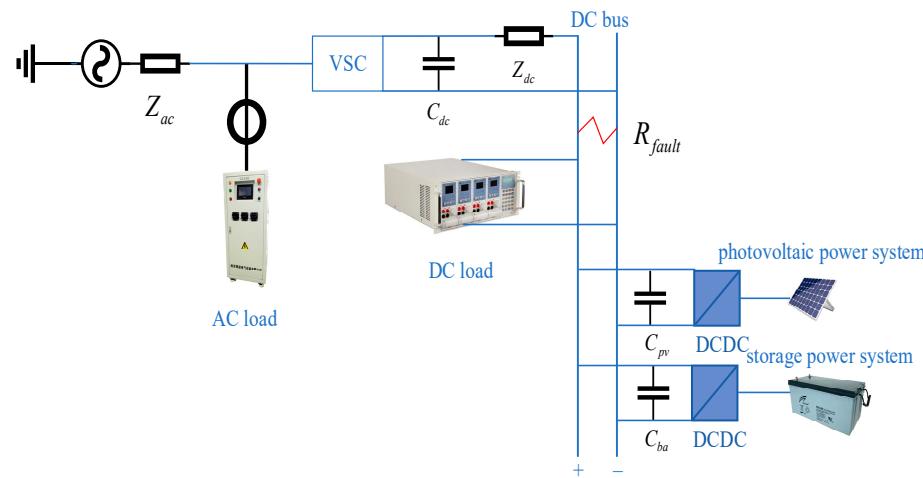


Figure 1. Structure of VSC-based AC/DC distribution networks.

In Figure 1, Z_{ac} is the AC line impedance, C_{dc} is the DC port shunt filter capacitance of the VSC and Z_{dc} is the DC line impedance. C_{pv} and C_{ba} are the DC-sideshunt filter capacitances of the PV and ESB, respectively. R_{fault} is the DC fault transition resistor.

The VSC structure is shown in Figure 2. Each phase branch consists of an upper and lower arm, the structure of a single arm consists of an IGBT and an antiparallel diode, and

the equivalent resistance and inductance on each phase are written as R_{ac} and L_{ac} [19,20]. The converter power loss is negligible compared to the load.

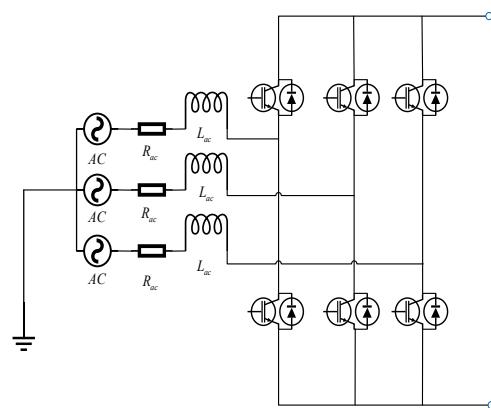


Figure 2. VSC structure.

Since AC-side fault analysis has become quite mature, this paper focuses on DC-side faults. In addition, DC line short-circuit faults between poles usually have low fault impedance characteristics, which are more hazardous to the transmission lines and are the most serious fault type [21], so the main type of fault characteristic targeted in this paper is the DC short-circuit fault between poles of the AC/DC distribution networks. The DC inter-pole fault is set on the DC bus, as shown in Figure 1.

3. Fault Analysis of Distribution Networks Containing PV

When a DC inter-pole short-circuit fault occurs, it is assumed that all IGBTs in the VSC are blocked due to self-protection. The DC port shunt capacitors in the converter will be discharged through the short-circuit fault point. When the capacitors are fully discharged, the antiparallel continuity diodes of the IGBTs in the VSC and PV converter start to conduct and provide a path for the AC grid and the PV to inject current into the fault point. The fault response process consists of the following three main stages [22]:

(1) DC Capacitors' Discharge Stage

When a DC inter-pole fault has just occurred, the IGBT gate signal is blocked for the protection of the VSC. As the DC bus voltage U_{dc} is higher than the instantaneous value of the AC-side line voltage, the converter diode cuts off in reverse, and the fault current i_f is mainly supplied by the DC-side capacitor C_{dc} and the PV-side capacitor C_{DG} . This means i_f is the sum of i_1 and i_2 , i_1 is the DC capacitor-side current, and i_2 is the PV-side current. Considering that the DC load R_{load} is much larger than the inter-pole fault transition resistance R_{fault} , the fault shunt equivalent resistance can ignore the DC load. The DC capacitor C_{dc} , line impedance Z_{dc} , and fault-parallel equivalent resistance R_k form the RLC second-order discharge circuit, shown in Figure 3. R_{dc} and L_{dc} are the equivalent resistance and equivalent inductance of the Z_{dc} composition, and R_{ac} and L_{ac} are the equivalent resistance and equivalent inductance of the Z_{ac} composition. The PV-side capacitor C_{DG} discharging circuit is shown in Figure 4, where R_{DG} and L_{DG} are the equivalent resistance and equivalent inductance of the PV side. The flowing direction of current has been demonstrated.

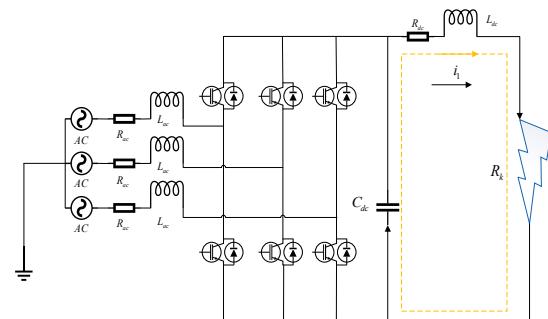


Figure 3. DC capacitor discharge stage.

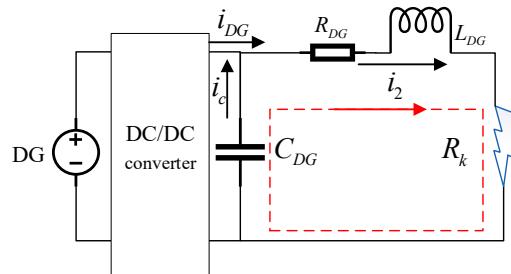


Figure 4. PV power capacitor discharge stage.

When the fault belongs to a metallic load, the transition resistance is small, leading to the fact that the fault circuit satisfies

$$R_{dc} < 2\sqrt{L_{dc}/C_{dc}} \quad (1)$$

At this point, the circuit is underdamped and the characteristic equation of the circuit with respect to the DC-side current i_1 is

$$\frac{d^2i_1}{dt^2} + \frac{R_{dc}}{L_{dc}} \frac{di_1}{dt} + \frac{i_1}{L_{dc}C_{dc}} = 0 \quad (2)$$

The expression for inductive current is

$$i_1 = K_1 \cos(\beta t) e^{-at} + K_2 \sin(\beta t) e^{-at} \quad (3)$$

In addition, $a = \frac{R_{dc}}{2L_{dc}}$, $\beta = \sqrt{1/(L_{dc}C_{dc}) - a^2}$, and K_1 and K_2 are the coefficients to be determined. Since the DC bus voltage is stable under normal operation and the DC load can be treated as a constant load, the circuit expression at steady state is

$$\begin{cases} u_1 = i_1 R_{dc} + (i_1 + i_2) R_{load} \\ u_2 = i_2 R_{DG} + (i_1 + i_2) R_{load} \end{cases} \quad (4)$$

Therefore, assuming that the initial values of the DC capacitor voltage u_1 and the PV capacitor voltage u_2 are U_{dc} , the initial value of the current i_1 can be obtained as

$$i_1(t_0) = U_{dc} R_{DG} / (R_{DG} R_{dc} + R_{DG} R_{load} + R_{dc} R_{load}) \quad (5)$$

Bringing Equation (5) to Equation (3) gives $K_1 = i_1(t_0)$, $K_2 = [(U_{dc} - R_{dc}K_1)/L_{dc} + aK_1]/\beta$. By taking the derivative of Equation (3) and making it equal to zero, we can find the expression for $t_{i1(\max)}$, which represents the time for i_1 to reach its maximum value:

$$t_{i1(\max)} = t_0 + \frac{1}{\beta} \arctan \left(\frac{K_2 \beta - K_1 a}{K_1 \beta + K_2 a} \right) \quad (6)$$

It is assumed that the PV operates in the boost mode until a short-circuit fault occurs between the DC bus poles. Then, the initial value of i_2 can be obtained as

$$i_2(t_0) = U_{dc}R_{dc}/(R_{DG}R_{dc} + R_{DG}R_{load} + R_{dc}R_{load}) \quad (7)$$

Since the short-circuit current i_2 at the PV side is mainly composed of i_{DG} and the capacitor discharging current i_c , i_2 can be expressed as

$$i_2 = i_{DG} + i_c \quad (8)$$

The circuit formed by the PV, C_{cp} , and IGBT branch works normally, as shown in Figure 5a, where the energy is stored by the inductor L_{pv} and the diode stays off during this stage, and the PV converter loses to the control. At this moment, the short-circuit current i_2 for the PV side is mainly composed of capacitor discharging current i_c . Therefore, the capacitor discharging circuit can be analyzed to obtain the following circuit characteristic equation:

$$\frac{d^2i_c}{dt^2} + \frac{R_{DG}}{L_{DG}} \frac{di_c}{dt} + \frac{i_c}{L_{DG}C_{DG}} = 0 \quad (9)$$

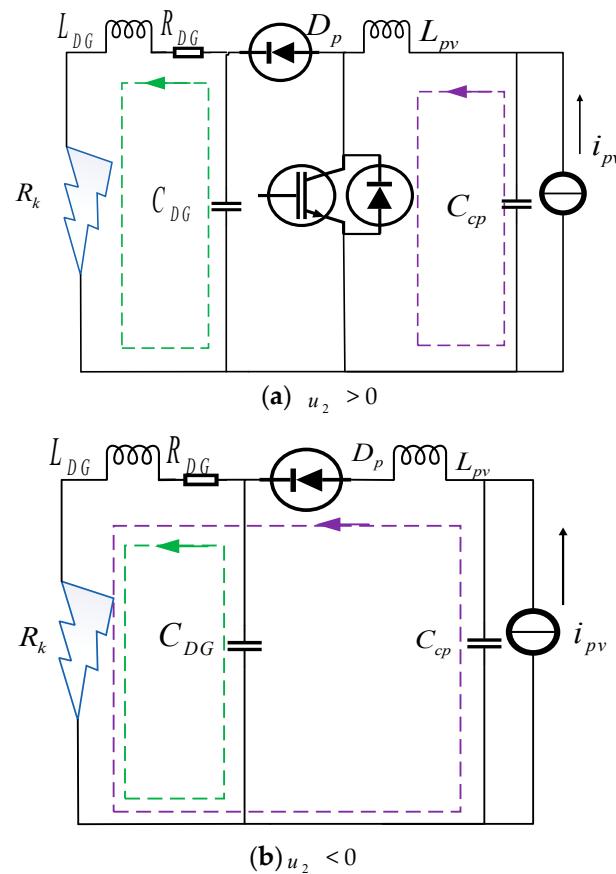


Figure 5. PV fault response circuits.

At this time, the short-circuit current i_c through the inductor is

$$i_c = K_{c1}\cos(\beta_c t)e^{-a_c t} + K_{c2}\sin(\beta_c t)e^{-a_c t} \quad (10)$$

In addition, $a_c = \frac{R_{DG}}{2L_{DG}}$, $\beta_c = \sqrt{1/(L_{DG}C_{DG}) - a_c^2}$, $K_{c2} = [(U_{DG} - R_{DG}K_{c1})/L_{DG} + a_c K_{c1}]/\beta_c$, $K_{c1} = i_c(t_0)$.

Kirchhoff's voltage law can also be applied to the capacitor discharging circuit in the PV converter. Since the PV converter is a boost converter, i_{DG} consists of the capacitive current i_{cp} and the PV array output current i_{pv} .

(2) Inductive Renewal Stage

When a fault occurs, the capacitor begins to discharge into the external circuit. When the capacitance voltage is positive and the H-bridge is within the antiparallel diode terminals plus negative voltage, orientation cannot be conducted. When the capacitance voltage crosses the zero point for the first time, the diode will meet the conduction conditions. The inductor current will flow through the antiparallel diode of the H-bridge and bypass the capacitance branch. Then, the new stage named the inductive renewal stage will be initiated. The diode renewal circuit is shown in Figure 6.

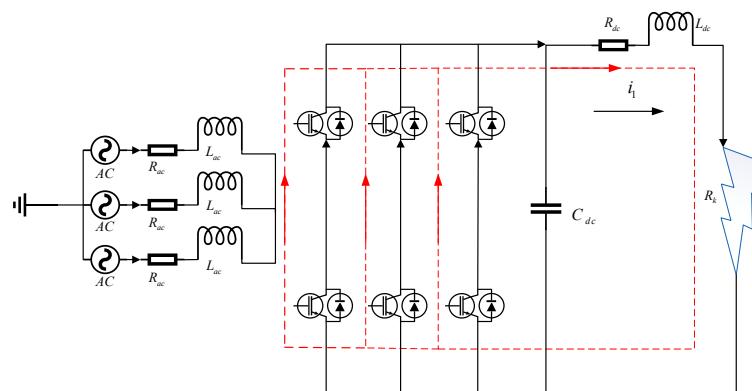


Figure 6. Diode conduction inductance renewal stage.

At this time, the current i_1 is

$$i_1 = I_{1\max} e^{-\frac{R_{dc}}{L_{dc}} t} \quad (11)$$

where $I_{1\max}$ is the value of i_1 in Equation (3) at the time $t_{i1(\max)}$.

At this stage, the PV converter is in an abnormal working state. Since the capacitance value of the filter capacitor C_{DG} is less than C_{dc} , the filter capacitor discharging time is less than the discharging time of C_{dc} . When the capacitor voltage of C_{DG} drops to zero, the IGBT reversely cuts off, the diode begins to conduct, and the PV array and capacitor C_{cp} begin to discharge towards the fault point through the diode, as shown in Figure 5b. At this moment, C_{cp} is charging C_{DG} , and i_2 is made up of i_{cp} and i_{pv} [23,24]. The i_{cp} can be expressed as

$$\frac{d^2 i_{cp}}{dt^2} + \frac{R_{DG}}{L'_{DG}} \frac{di_{cp}}{dt} + \frac{i_{cp}}{L'_{DG} C_{cp}} = \frac{i_c}{L'_{DG} C_{DG}} \quad (12)$$

Thus, the expression for the current i_{cp} can be obtained.

$$i_{cp} = \begin{cases} E \cos(\beta_1 t) e^{-\alpha_1 t} + F \sin(\beta_1 t) e^{-\alpha_1 t} \\ + G \cos(\beta_c t) e^{-\alpha_c t} + H \sin(\beta_c t) e^{-\alpha_c t} \end{cases} \quad (13)$$

where $L'_{DG} = L_{DG} + L_{pv}$, $\beta_1 = \sqrt{1/(L'_{DG} C_{cp}) - (R_{DG}/2L'_{DG})^2}$, $\alpha_1 = R_{DG}/2L'_{DG}$, $E = i_{cp}(t_0)$, $F = \beta_1 [(U_{dc} - R_{DG}E)/L'_{DG} + \alpha_1 E]$, $G = \frac{C_{cp}R_{DG}C_{DG}(a_c^2 - \beta_c^2) + C_{cp}K_{c1}}{C_{DG}L'_{DG}(a_c^2 + \beta_c^2) + R_{DG}C_{DG}a_c}$, $H = \frac{C_{cp}R_{DG}C_{DG}(\beta_c^2 - a_c^2) - C_{cp}K_{c2}}{C_{DG}L'_{DG}(a_c^2 - \beta_c^2) + R_{DG}C_{DG}\beta_c}$.

When the voltage of C_{DG} is greater than zero due to C_{cp} discharging, the discharging of C_{DG} is resumed, causing the diode to turn off and the IGBT to turn on again, and the discharging circuit is shown in Figure 5a. At this time, C_{DG} is in the state of oscillating discharge, and it is decided to conduct and turn on the IGBT of the PV converter by

the control mode, where i_{pv} is the natural discharge current of the PV array under the set conditions.

(3) Steady State Stage

When the inductive discharge is finished, the diode naturally commutates and conducts under the action of the AC grid, the DC voltage is a fixed value, and the short-circuit current is an almost-constant DC current, supplied by the AC system. At this point, the circuit is shown in Figure 7.

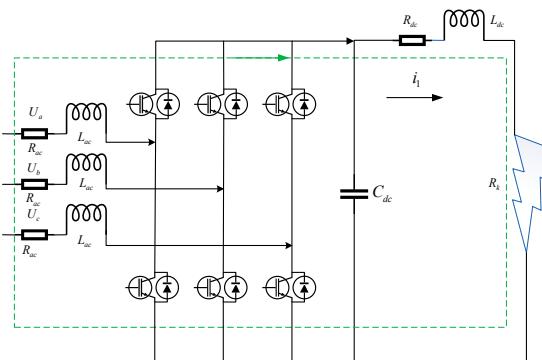


Figure 7. Steady-state discharge stage.

Taking phase A of the AC grid as an example, using the power system three-phase short-circuit fault analysis, the phase voltage can be obtained as

$$v_A = V_{ac} \sin(w_s t + \varphi_a) \quad (14)$$

where V_{ac} is the AC-side voltage amplitude before the fault, w_s is the synchronous angular frequency, and φ_a is the angle of A-phase voltage at time $t_{i1(\max)}$. Therefore, the current in phase A after the break is

$$i_A = \begin{cases} I_{ac} \sin(w_s t + \varphi_a - \theta) + \\ [I_{ac0} \sin(\varphi_a - \theta_0) - I_{ac} \sin(\varphi_a - \theta)] e^{-\frac{R_{dc}}{L_{dc} + L} t} \end{cases} \quad (15)$$

where $\theta = \arctan[w_s(L + L_{dc})/R_{dc}]$, I_{ac0} is the starting amplitude of the current, θ_0 is the starting angle of current, and L is the AC filter inductance. At this time, the AC-side current is in the stage of uncontrolled rectification, and i_{VSC} is

$$i_{VSC} = i_A (> 0) + i_B (> 0) + i_C (> 0) \quad (16)$$

Assuming that the starting angle of AC voltage is 0 and the A-phase current has the maximum current amplitude, i_1 can be expressed as

$$i_1 = \begin{cases} A_1 \sin(w_s t + \gamma) + (D_1/\beta) \sin(\beta t) e^{-at} + \\ B_1 e^{-t/\tau} + D_2 (\lambda/\beta) e^{-at} \sin(\beta t + \sigma) \end{cases} \quad (17)$$

where $\lambda = \sqrt{a^2 + \beta^2}$, $\tau = (L + L_{dc})/R_{dc}$, $B_1 = I_{ac}[\tau^2/(a^2 - R_{dc}C_{dc}\tau + L_{dc}C_{dc})]$, $\sigma = \arctan[(R_{dc}C_{dc}w_s)/(1 - w_s^2L_{dc}C_{dc})]$, $\gamma = \varphi_a - \theta - \sigma$, $D_1 = -(A_1 \sin \gamma + B_1)$, $A_1 = I_{ac}/\sqrt{[(1 - w_s^2L_{dc}C_{dc})^2 + (R_{dc}C_{dc}w_s)^2]}$, $D_2 = B_1/\tau - A_1 w_s \cos \gamma$.

It is noteworthy that i_2 still will attenuate into a steady state in the form of oscillation. When reaching the steady state, the PV converter resumes its control and the PV array provides current to the point of fault through the renewal diode of the converter. At this time, i_2 consists of i_{pv} driven by control strategies [25].

4. Fault Analysis of Distribution Networks Containing ESB

Assuming that the IGBTs in the VSC are blocked when a DC inter-pole short-circuit occurs in the AC/DC distribution network, the effect of using different control methods for the ESB converter on the fault characteristics is considered. After the short-circuit fault occurs, the DC port shunt capacitor discharges rapidly. When the capacitor voltage crosses the zero point, the inductor current starts to renew through the conduction diode, and the capacitor oscillates and discharges until the current stabilizes. The fault response process can be divided into the following three stages:

(1) DC Capacitors Discharge Stage

When a fault occurs, the capacitance discharge stage is similar to the capacitance discharge stage of PV, and the DC bus capacitor C_{dc} and ESB capacitor C_{DG} rapidly discharge to form a short-circuit current. Thus, the DC capacitor side current i_1 is

$$i_1 = K_1 \cos(\beta t) e^{-at} + K_2 \sin(\beta t) e^{-at} \quad (18)$$

In addition, $a = \frac{R_{dc}}{2L_{dc}}$, $\beta = \sqrt{1/(L_{dc}C_{dc}) - a^2}$, $K_1 = i_1(t_0)$, $K_2 = [(U_{dc} - R_{dc}K_1)/L_{dc} + aK_1]/\beta$, $i_1(t_0) = U_{dc}R_{DG}/(R_{DG}R_{dc} + R_{DG}R_{load} + R_{dc}R_{load})$, and U_{dc} is the DC steady voltage.

The ESB-side current i_2 is

$$i_2 = K_{c1} \cos(\beta_c t) e^{-a_c t} + K_{c2} \sin(\beta_c t) e^{-a_c t} \quad (19)$$

In addition, $a_c = \frac{R_{DG}}{2L_{DG}}$, $\beta_c = \sqrt{1/(L_{DG}C_{DG}) - a_c^2}$, $K_{c2} = [(U_{DG} - R_{DG}K_{c1})/L_{DG} + a_c K_{c1}]/\beta_c$, $K_{c1} = i_c(t_0)$.

(2) Inductive Renewal Stage

When the capacitor voltage crosses the zero point, the inductor current will flow through the conduction diode to renew. Since the ESB serves as the power source, i_2 at this time primarily consists of the inductor current and the discharge current from the ESB. The circuit configuration is illustrated in Figure 8.

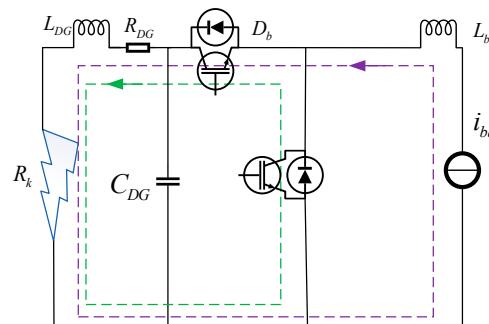


Figure 8. Fault response circuit of the ESB.

In this stage, i_1 can be expressed as

$$i_1 = I_{1\max} e^{-\frac{R_{dc}}{L_{dc}}t} \quad (20)$$

where $I_{1\max}$ represents the maximum value of i_1 when the capacitor voltage crosses the zero point.

Analogously, i_2 can be expressed as

$$i_2 = I_{c\max} e^{-\frac{R_{DG}}{L_{DG}}t} + i_{ba} \quad (21)$$

where $I_{c\max}$ represents the maximum value of i_c when the capacitor voltage crosses the zero point, and i_{ba} is the ESB discharge current.

(3) Steady-State Stage

After the end of the inductor current discharge, the steady state of the ESB is similar to the steady state of the PV, i.e., i_1 is also powered by AC, and the expression is the same as Equation (17).

When entering the steady-state stage, the fault current on the ESB converter side continues to decay in an oscillating situation and reaches a steady state. The amplitude of the fault current in this process will be much smaller than the capacitive discharge stage and inductive renewal stage. The ESB and its converter can be equivalent to a voltage source $U_0(s)$ and impedance $Z_0(s)$ in a series circuit, and i_2 is provided only by the equivalent voltage source $U_0(s)$. Thus, the relationship is denoted as follows:

$$U_0(s) = i_2(Z_0(s) + R_{DG} + L_{DG}s + R_k) \quad (22)$$

The control strategy affects the magnitude of the equivalent impedance $Z_0(s)$, leading to the variation in the magnitude of i_2 .

5. Validations

In Power Systems Computer Aided Design/Electromagnetic Transients including DC (PSCAD/EMTDC) simulation software of version 4.6.2, AC/DC distribution networks with different distributed generations are constructed separately to verify the correctness of fault characterization, and the fault characteristics are analyzed and discussed under the consideration of the influence of control strategies. The simulation parameters of the AC/DC distribution network are shown in Table 1 [8].

Table 1. Parameters of AC/DC grid.

Parameters	Value
DC bus voltage	0.4 kV
Fault transition resistance	0.001 Ω
Valve-side capacitance	0.005 F
Distributed power capacitance	0.002 F
Valve-side circuit parameters	0.12 Ω, 0.00056 H
Power-side circuit parameters	0.012 Ω, 0.000056 H
Single-phase AC line inductance	0.005 H
DC load resistance value	15 Ω

Remark 1: There are various types of software available for circuit simulation, such as PSCAD, MATLAB/Simulink, PSS/E (Power System Simulator for Engineering), and DiGILENT PowerFactory. In the context of power fault analysis, PSCAD's computational logic excels at accurately simulating real-world circuit faults, making it more precise and reliable for fault analysis compared to other software [26,27].

Figures 9 and 10 display the comparison results between the calculated values and the simulated values of fault current for an AC/DC distribution network with PV and ESB, respectively. One can find that the calculated values are close to the simulated values, which demonstrate that the proposed theoretical analysis for fault current is effective.

In order to give a detailed quantitative analysis, the mean error rate (MER) R_{mer} is used as follows:

$$R_{mer} = \frac{1}{N} \sum_{i=1}^N \left| \frac{S_i^* - S_i}{S_i^*} \right| \quad (23)$$

where S_i is the calculated value, S_i^* is the simulated value, and N is the number of total sampling points. The MERs of the AC/DC distribution network with different distributed generations are shown in Table 2. We can see that within 10 ms of the fault occurrence, the overall accuracy of the proposed fault current calculation method is about 90%, and the accuracy of i_1 can even reach close to 95%. Therefore, the proposed method can analyze the actual fault current better.

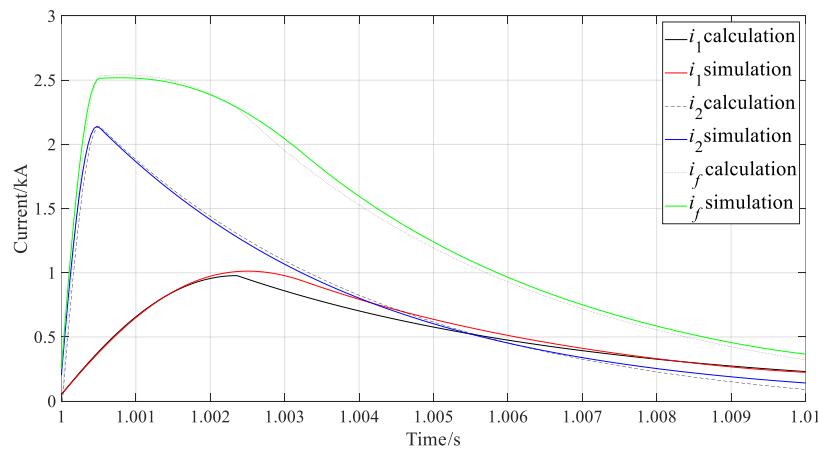


Figure 9. Comparison results for the distribution networks with PV.

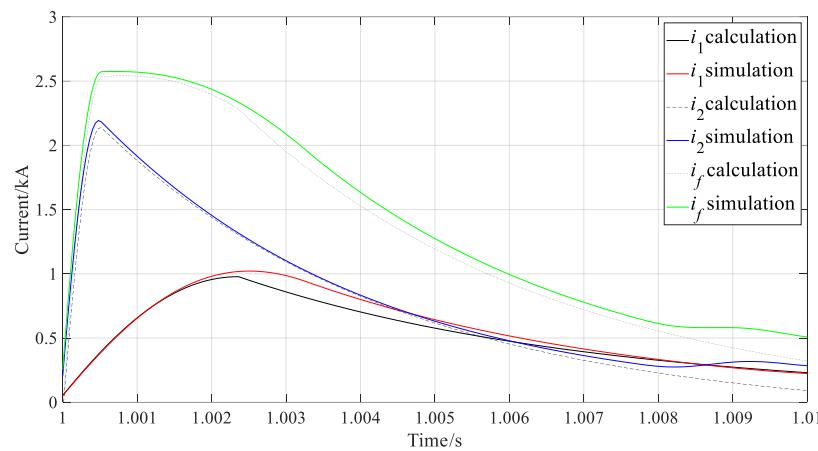


Figure 10. Comparison results for the distribution networks with ESB.

Table 2. Mean error rate of AC/DC grid with distributed generations.

Systems	i_1	i_2	i_f
PV	0.0532	0.0745	0.0497
ESB	0.0573	0.1386	0.1012

Figure 11 shows the fault current simulation results for AC/DC distribution networks with PV, where scenarios 1, 2, 3, and 4 represent maximum power point tracking (MPPT) control, constant voltage control, constant power control, and IGBT blocking for PV converter, respectively. Figure 11a shows the simulation curves of i_1 , which demonstrate that the PV converter control strategies have almost no effect on i_1 during the fault response. Figure 11b shows the simulation curves of i_2 , which demonstrate that i_2 is also unaffected by the control strategies of the PV converter in the first two stages of the fault response. In the steady-state stage, the fault current i_2 under MPPT control is larger than the other conditions, and the curves of Scenario 2 and Scenario 3 are almost coincident. Figure 11c shows the simulation curves of i_f , which demonstrate that i_f is affected by the PV converter control strategies only in the steady-state stage.

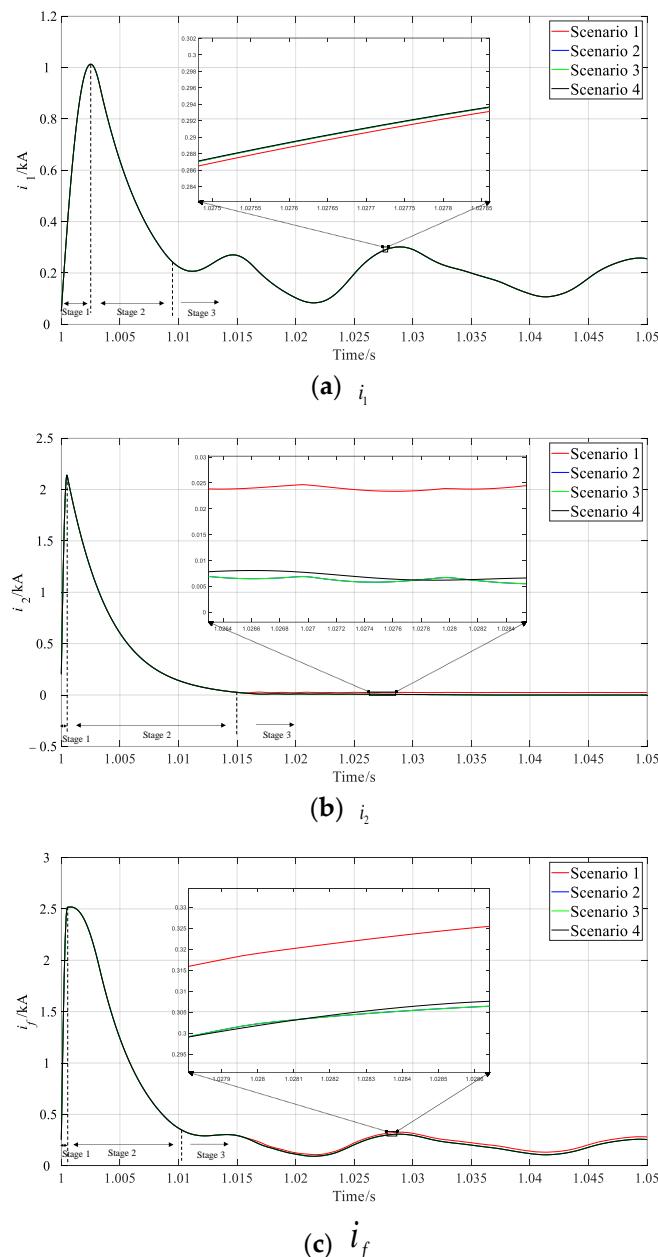


Figure 11. Simulation results for AC/DC distribution networks with PV.

As shown in Figure 12, the simulation results of fault current for AC/DC distribution networks with ESBs are compared, in which scenarios 1, 2, 3, and 4 represent constant voltage control, constant power control, voltage droop control, and IGBT blocking situations for the ESB converter. It can be seen that i_1 , i_2 , and i_f all are almost unaffected by the considered control strategies of ESB converter in the first two stages. In the steady-state stage, the constant voltage control, constant power control, and voltage droop control curves are almost completely overlapped.

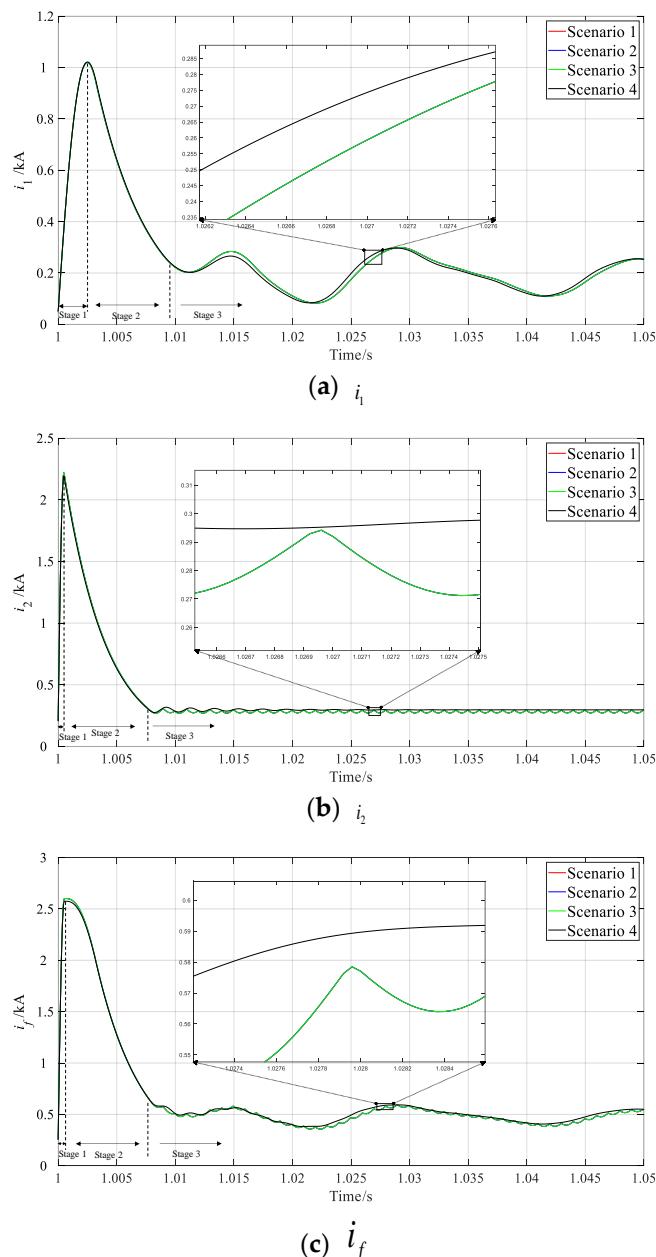


Figure 12. Simulation results for AC/DC distribution networks with ESBs.

The impact of line inductance variation on faults is shown in Figure 13. The 'sim' represents the simulated value and the 'cal' represents the calculated value. From the curves, we can see that the calculated value is close to the simulated value under the variations in inductance, which demonstrates the effectiveness of the proposed method.

Remark 2: It is worth noting that the effect of electrochemical properties such as ESB power and capacity have not been considered in this study. From the perspective of fault characteristics, this paper mainly focuses on the effect of control strategies from PV and ESBs. In the future, we will investigate the effects of the electrochemical properties on fault characteristics.

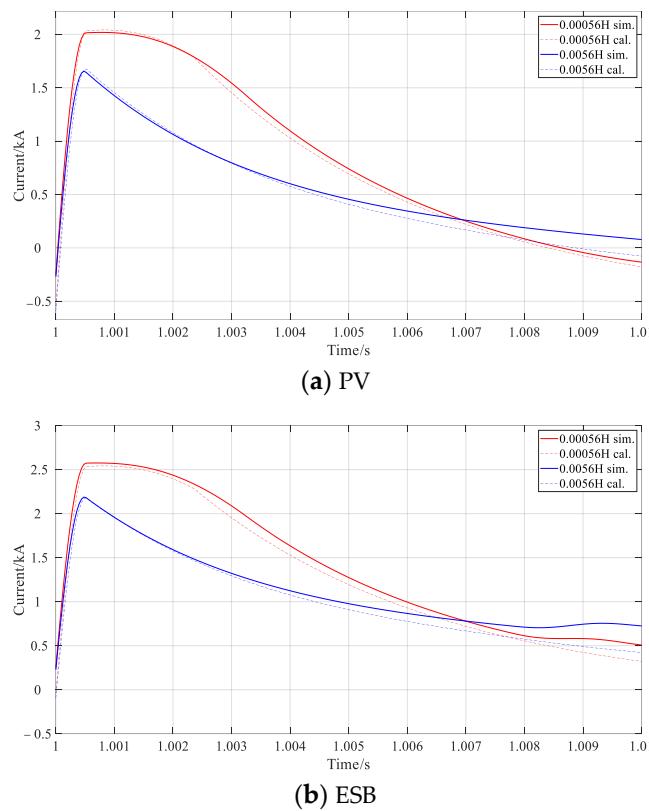


Figure 13. Fault current with line inductance variations.

6. Conclusions

With increasing high-capacity distributed generators (e.g., PV, ESBs), the fault behavior in the VSC-based AC/DC distribution network becomes more complex. In this study, a three-stage fault characteristic scheme is proposed for a VSC-based AC/DC distribution network with different distributed generators. Based on circuit analysis, the fault response process is divided into three stages including the DC capacitor discharge stage, inductive renewal stage, and steady-state stage. Then, the expression of fault current for different stages is established. In particular, the effect of control strategies for distributed generators is integrated into the fault characteristics. Simulation validation showed that the simulation curve aligned well with the presented equations, and the proposed fault analysis scheme performed with high accuracy for different conditions, where the mean error rate was less than 10%. Moreover, the comparison results considering the variations in inductance also indicated that the developed scheme had excellent performance for fault characteristics.

The main contributions of this paper can be enumerated as follows:

- (1) Compared with [13,16], this study proposes a three-stage fault analysis scheme for a VSC-based AC/DC distribution network, which provides a unified expression to analyze the fault current for different distributed generators.
- (2) Different from [8], this study verifies the impact of the control strategies of distributed generation converters on fault current, which provides valuable guidance for the design of protection techniques.

It is worth noting that this paper only discusses the effect of distributed generation converter control strategies on fault characteristics and does not consider the effect of VSC control strategies, which will be carried out in our future study.

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