

Article

# EIS Study on the Electrode-Separator Interface Lamination

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**Abstract:** This paper presents a comprehensive study of the influences of lamination at both electrode-separator interfaces of lithium-ion batteries consisting of  $\text{LiNi}_{1/3}\text{Mn}_{1/3}\text{Co}_{1/3}\text{O}_2$  cathodes and graphite anodes. Typically, electrode-separator lamination shows a reduced capacity fade at fast-charging cycles. To study this behavior in detail, the anode and cathode were laminated separately to the separator and compared to the fully laminated and non-laminated state in single-cell format. The impedance of the cells was measured at different states of charge and during the cycling test up to 1500 fast-charging cycles. Lamination on the cathode interface clearly shows an initial decrease in the surface resistance with no correlation to aging effects along cycling, while lamination on both electrode-separator interfaces reduces the growth of the surface resistance along cycling. Lamination only on the anode-separator interface shows up to be sufficient to maintain the enhanced fast-charging capability for 1500 cycles, what we prove to arise from a significant reduction in growth of the solid electrolyte interface.

**Keywords:** lithium-ion battery; lamination; electrochemical impedance spectroscopy; fast-charging capability; lifetime

## 1. Introduction

Lithium-ion battery (LIB) technology has grown to a market leader in the field of rechargeable batteries in the last decades. LIBs are used as the energy source for portable devices and electric vehicles (EVs), as well as for stationary energy storage systems to ensure grid stability upon fluctuations from renewable energy sources. To improve the fast-charging capability as well as the travelling distance of the EVs, ongoing research mainly addresses the basic cell components like active materials [1,2], electrolyte [3], separator [4–7], and manufacturing steps. Different manufacturing techniques, such as ultra-thick electrodes [8–11], calendering process [12], controlled stack pressure [13,14], laser structuring [15–20] and lamination [21], have been applied to increase the power density, energy density, lifetime and for cost reduction of LIBs. Typically, the calendering process improves the contact situation between the active material particles [14], which leads to an increase of the rate capability as well. On the other hand, extensive calendering can break the active material particles and block the lithium-ions at the electrode-electrolyte interface which makes the fast-charging capability problematic [12,22].

The electrode-separator lamination technique is known for the simplification of the stacking process upon reducing the probability of stack component slipping in the anode-separator-cathode compound [23], as well as accelerating the manufacturing speed. Besides, it can also improve the fast-charging capability and reduce the capacity fade at high C-rates [21]. This leads to the assumption

that the detailed mechanisms that drive the fast-charging capability upon electrode-separator lamination are not completely understood so far, which inspired this study.

A recent study of lithium metal anodes showed that surface treatments for smooth lithium surfaces can significantly suppress lithium dendrite growth by modifying the surface topography and local surface chemistry, therefore lowering the solid electrolyte interface (SEI) growth losses during cycling [24]. Similarly, it was shown that electrochemical polishing on alkali metal anodes, which yield ultra-smooth surfaces, provide ultra-thin SEI layers which possibly suppress dendrite growth along cycling [25].

In our previous study, cross-section images gained by scanning-electron-microscopy (SEM) clearly showed pore size reduction at both electrode-separator interfaces upon lamination [21]. Hence, the lithium-ion diffusion paths can be expected to be shortened and homogenized at both electrode-separator interfaces. As a result, the ion current density distribution along the active area of the full cell gets equalized according to the ion path length homogenization on the electrode-separator interfaces. Equalizing the current density distribution reduces the possibility to locally reach exceptional high ohmic overpotentials, high enough to undergo the lithium deposition potential and cause local lithium dendrite formation, especially at high charging rates. Similar effects were found by Müller, S. et al., who recently reported a clear correlation for graphite anode inhomogeneities at different scale lengths to possibly cause local overpotentials high enough to undergo the lithium deposition potential [26].

To overcome some of the mentioned problems, the electrode-separator lamination technique provides proper contacts of separator and electrode at micro level. Suppression of ridges and wrinkles as well as reducing the probability to form cracks during cycling, analogously holds the potential to prevent dendrite formation and SEI growth. Validity of this assumption can be reasonably studied using electrochemical impedance spectroscopy (EIS).

To appropriately study the contribution of each electrode within a full cell using EIS, typically three electrode geometries are designed and used, which unfortunately requires special modifications to any kind of full cell design [27,28]. In case of two-electrode impedance spectroscopy, the distinction of each electrode contribution is challenging, but possible [27]. The EIS signal responses for  $\text{LiNi}_{1/3}\text{Mn}_{1/3}\text{Co}_{1/3}\text{O}_2$  (NMC) cathodes [22] or related structures [29] and graphite anodes [30,31] have yet been studied in detail. Using this information, the EIS signal of a graphite/NMC full cell could be considered well understood so far. Nevertheless, in literature the interpretation of the surface resistance semicircle reflects several further aspects. While the signal is often assigned to mainly depend on the SEI [32,33], there are also studies that show separate influences arising from the electrode-current collector contact situation [34]. Therefore, reliable studies of SEI effects emerging from the surface resistance signal have to deal with a proper separation of the signal contributions.

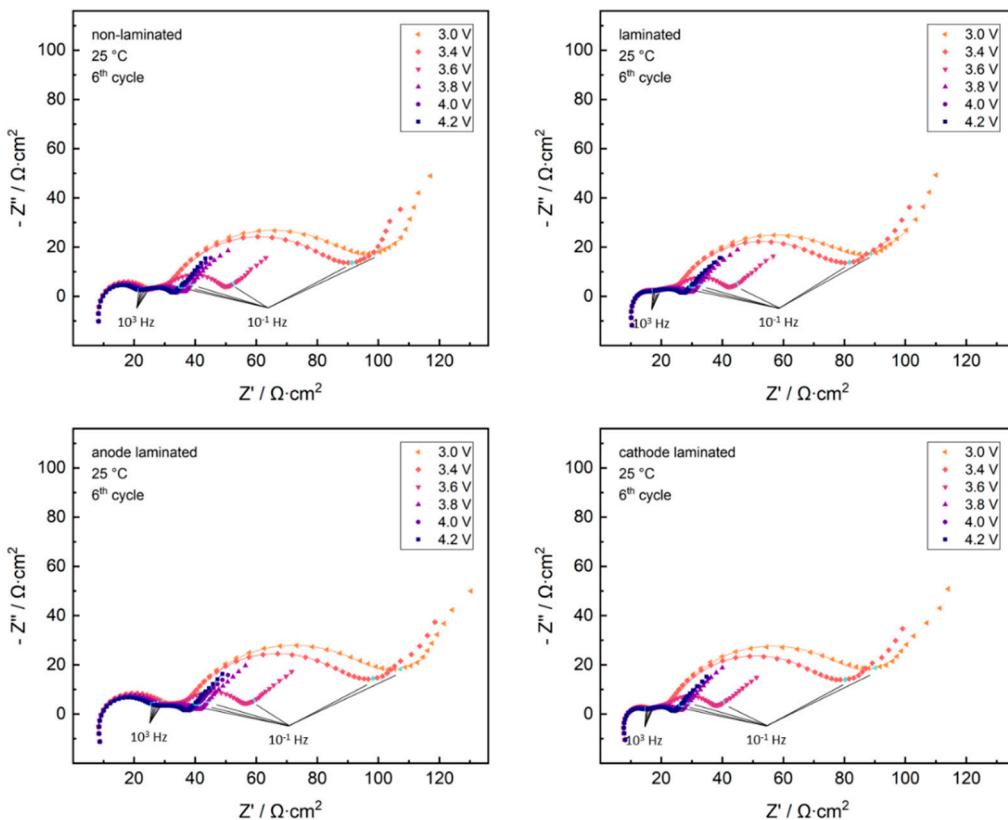
To overcome this difficulty, EIS measurements are either driven at exceptional low temperatures [32], which is problematic when aiming for aging studies purely based on cycling effects, or by introducing reference electrodes into the cell geometry [27,28].

In this study, we will show the ability of the lamination technique to provide this signal separation even in a two-electrode geometry, and use the correlation to prove the enhanced fast-charging capability of laminated cells to arise from a reduction in SEI growth.

## 2. Results and Discussion

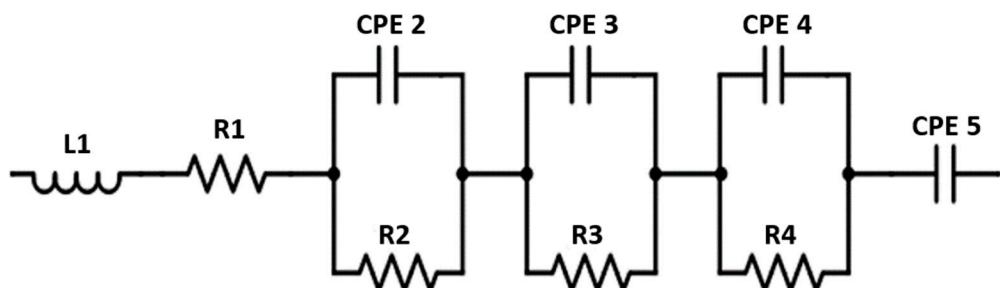
### 2.1. Cathode-Separator Lamination Effects

Single cells consisting of a NMC cathode, separator and graphite anode were studied via EIS in non-laminated/partially laminated/fully laminated state along varied state of charge (SOC) after three formation cycles (C/10 rate) and two initial cycles at 1C rate. Figure 1 shows the impedance spectra gathered upon different lamination modes.



**Figure 1.** Impedance measurements of laminated/partially laminated/non-laminated cells: EIS (100 kHz–10 mHz) along charging step, 6th cycle; fitting curves indicated as solid lines; data points at  $10^3$  Hz and  $10^{-1}$  Hz highlighted in pale blue.

The Nyquist plots uniquely show inductive behavior at the high-frequency regime, followed by three semicircles and the typical Warburg behavior at the lowest frequencies. For further studies, we characterize the three semicircles and the Warburg regime using the equivalent circuit model shown in Figure 2.



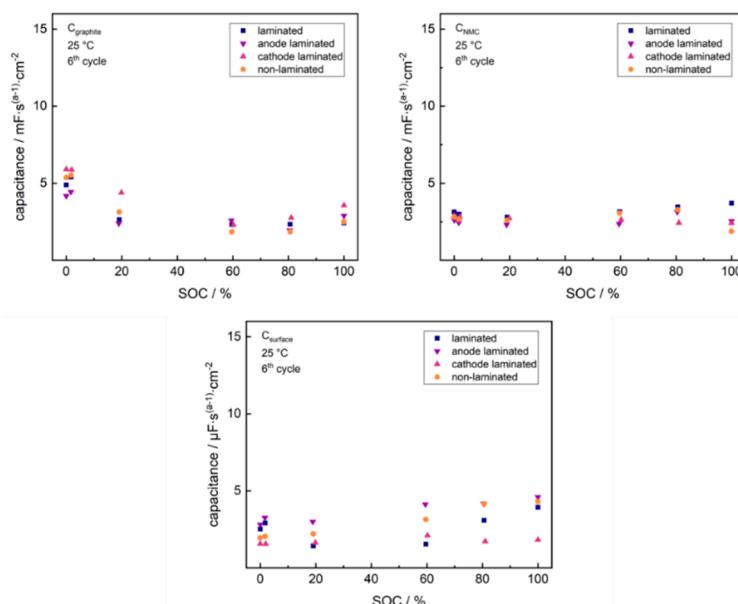
**Figure 2.** Equivalent circuit model used for EIS fit analysis.

This common equivalent circuit model is frequently used in literature [32] to describe NMC/graphite full cells. In the highest frequency regime, the signal is dominated by inductive phenomena arising from the impedance measurement environment. Both inductance element L1 and the electronic resistance R1, considered to mainly arise from the electrolyte resistance, contain side influences from the setup, such as cell tabs, welding points, impedance channel contacts and cables. The first semicircle represents the surface resistance phenomena. The second and third semicircle are driven by the charge-transfer reactions of graphite anode and NMC cathode, respectively. Low frequency phenomena arise from solid state diffusion characteristics, that can be split into closed and open Warburg regime [35], and therefore sometimes occurring as a consecutive series of

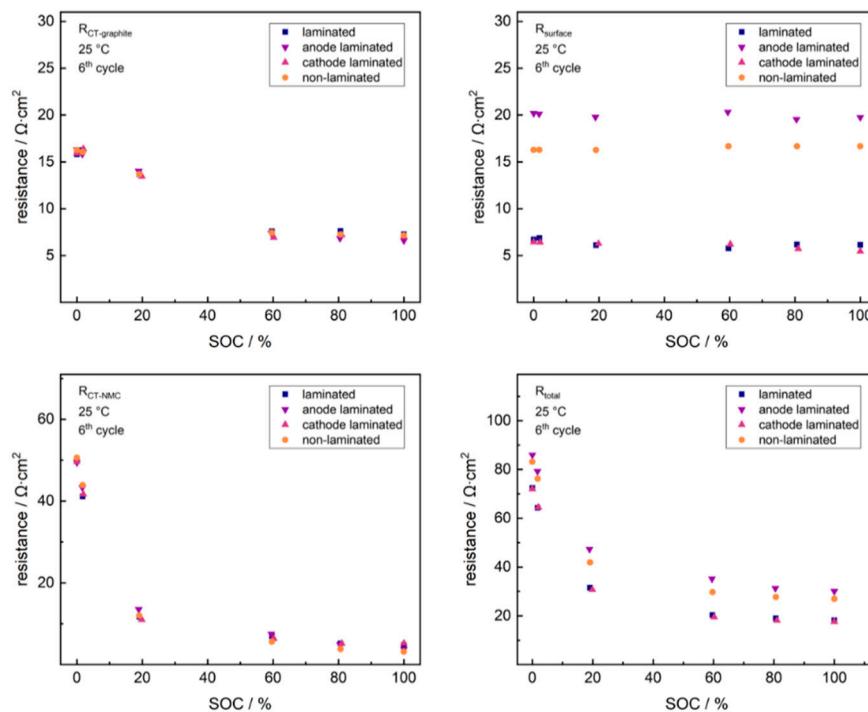
varying slopes in the Nyquist presentation of the lowest frequency responses. As described above, signals from both charge-transfer reactions tend to overlap in this reference system as arising from the sum of the graphite anode and NMC cathode charge-transfer contributions [29–31,36]. For proper signal separation of these charge-transfer contributions, typically three-electrode cell designs are used involving reference electrodes. But in the case of NMC/graphite full cells, given knowledge on the separate EIS signal trends along SOC for the NMC cathode [37] or related composite materials [29], and graphite anode [30,31] can be used to identify the individual full cell signal contributions to the charge-transfer resistance. It is well accepted that in case of LIB full cells the sum of the signal contributions of the separate electrodes define the EIS response in a two-electrode geometry [36,38]. Jimenez Gordon et al. described the signal contribution of graphite anodes in LIBs [30,31]. While the surface resistance contribution, arising from porosity aspects and SEI characteristics, stays independent from the SOC of the cell [30], the charge-transfer signal of graphite decreases with increasing SOC, following a characteristic trend [31]. Liu et al. clarified the EIS trends of composite cathodes with respect to the amount and ratio of the conductive additive and PVDF binder, identifying separate mechanisms to drive the raise in impedance depending both on the ratio and on the total content of binder and conductive additive [29]. In the case of a ratio of 0.8:1 for acetylene black: PVDF, both for the total contents of 3.6% and 9%, they found a characteristic increase of the charge-transfer resistance with increasing depth of discharge (DOD). A drastic increase of the slope was found approaching 100% DOD [29].

The highlighted data point set at  $10^3$  Hz in Figure 1 lies close to the minimum between the first and second semicircle for all shown Nyquist datasets. As its relative position does not change with SOC for any cell, the surface resistance, that characterizes the first semicircle, can be considered independent from SOC. The second highlighted data point series at  $10^{-1}$  Hz lies within the Warburg regime at high SOC for all cells, shifting closer to the minimum between the third semicircle and Warburg regime with decreasing SOC. This behavior indicates a shift to lower time constants of the cathode charge-transfer process with decreasing SOC, which is a known effect on the charge-transfer resistance of NMC based full cells [37].

Using the described correlations of the EIS signal response, the equivalent circuit analysis of the signals shown in Figure 1 is unambiguous. As for the structure of the chosen equivalent circuit, the open Warburg behavior was excluded from the data fit. Results are presented in Figures 3 and 4.



**Figure 3.** EIS capacitance fit parameters of laminated/partially laminated/non-laminated cells along charging step, sixth cycle; data normalized to geometric electrode area.



**Figure 4.** EIS resistance fit parameters of laminated/partially laminated/non-laminated cells along charging step, sixth cycle; data normalized to geometric electrode area.

As shown in Figure 3, the capacitance fit parameters for the graphite anode and NMC cathode lie around  $3\text{--}4 \text{ mF}\cdot\text{s}^{(\text{a}-1)}\cdot\text{cm}^{-2}$  with negligible dependence on SOC, which is in the range of typically reported values for EIS capacitance fit parameters, normalized to the geometric electrode area, of graphite anodes and composite cathodes in non-aqueous electrolytes [39–41]. The capacitance fit parameters of the surface resistance semicircle show no significant correlation to the SOC and lie around  $3\text{--}5 \mu\text{F}\cdot\text{s}^{(\text{a}-1)}\cdot\text{cm}^{-2}$  for all cells, which is in the range of double layer capacitances of non-aqueous electrolytes [39]. Further information can be extracted from the resistance fit parameters, shown in Figure 4.

For all cells, the charge-transfer resistance signal for the graphite anode decreases initially down to  $\sim 14 \Omega\cdot\text{cm}^2$  at 20% SOC. For SOC higher than 60%, the charge-transfer signals lie at a constant lower plateau at around  $7 \Omega\cdot\text{cm}^2$ . This trend of the graphite anode charge-transfer resistance was well-described by Jiménez Gordon, I. et al. [30,31]. As it can be seen, there is no significant difference between different lamination modes.

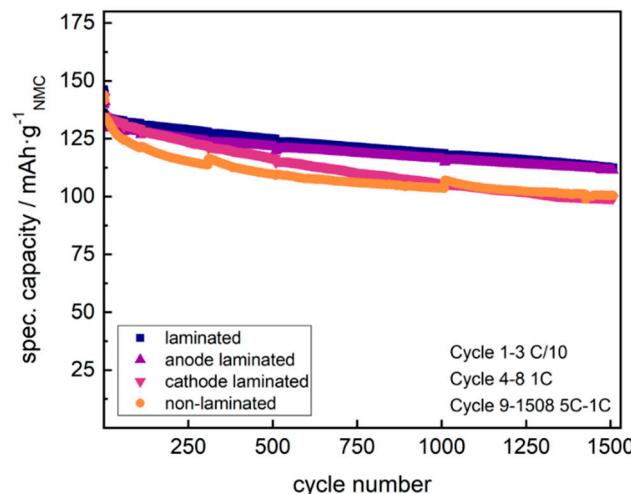
Analogously, a logarithmic drop of the NMC charge-transfer resistance along increasing SOC is found for all cells, with no correlation to any lamination mode. This logarithmic trend of the NMC charge-transfer signal is well-known [29,42].

The first significant difference between the lamination modes can be found in the trends of the surface resistance. Both non-laminated cell ( $\sim 16 \Omega\cdot\text{cm}^2$ ) and anode-laminated cell ( $\sim 20 \Omega\cdot\text{cm}^2$ ) show relatively high surface resistance signals, whereas cathode-laminated and fully laminated cells both drop to a surface resistance signal around  $6 \Omega\cdot\text{cm}^2$ , especially at higher SOC. Zheng, H. et al. found a similar drop of the surface resistance purely upon calendering NMC-cathodes to different porosities, where also lowest resistances at around  $5 \Omega\cdot\text{cm}^2$  are reached [22]. This recognizable drop arises from porosity changes and contact optimization at the cathode side. As both lamination and calendering technique are applied previous to final cell assembly, this surface resistance drop can act as a normalization for the starting conditions of the full cell surface resistance. After minimizing all well-known NMC cathode influences on the surface resistance as in the cathode-laminated and fully

laminated state previous to cycling studies, any further changes on the surface resistance upon cycling uniquely arise from changes in the SEI.

## 2.2. Anode-Separator Lamination Effects

Figure 5 presents the results of non-laminated/partially laminated/fully laminated cells in the cycling test, when charging at 5C (CCCV mode) and discharging at 1C (CC mode). Recent studies on electrode-separator lamination showed a recognizable reduction in capacity fading upon fast-charging cycles at fully laminated state [21].



**Figure 5.** Discharge capacity data of laminated/partially laminated/non-laminated cells in fast-charging cycle test; charge at 5 C CCCV mode, discharge at 1 C CC mode.

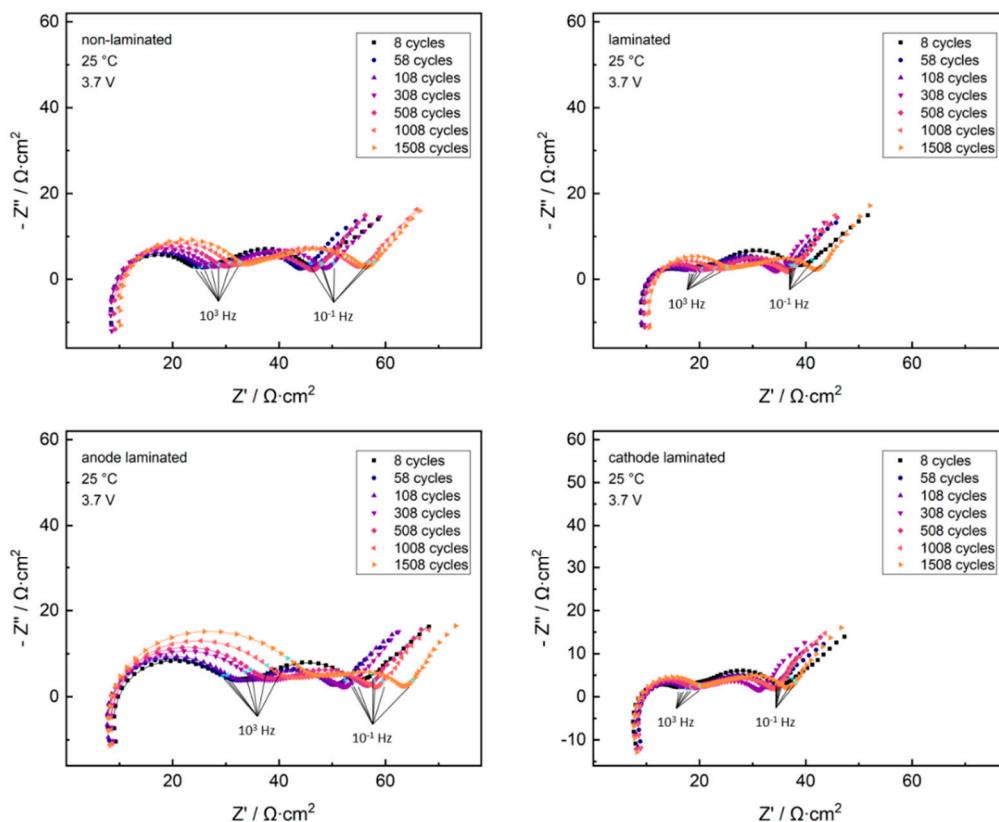
Both the non-laminated cell and cathode-laminated cell reveal severe capacity fading, decreasing from  $133.0 \text{ mAh}\cdot\text{g}^{-1}$  (100%) and  $133.4 \text{ mAh}\cdot\text{g}^{-1}$  (100%) at the 9th cycle, down to  $100.4 \text{ mAh}\cdot\text{g}^{-1}$  (75.5%) and  $99.3 \text{ mAh}\cdot\text{g}^{-1}$  (74.6%) at the 1508th cycle, respectively. Additionally, both laminated and anode-laminated cells show a reduced capacity fading, decreasing from  $133.2 \text{ mAh}\cdot\text{g}^{-1}$  (100%) and  $129.6 \text{ mAh}\cdot\text{g}^{-1}$  (100%) at the 9th cycle, down to  $112.5 \text{ mAh}\cdot\text{g}^{-1}$  (84.6%) and  $111.4 \text{ mAh}\cdot\text{g}^{-1}$  (83.7%) at the 1508th cycle, respectively. Capacity fade trends are summarized in Table 1.

**Table 1.** Capacity fade of laminated/partially laminated/non-laminated cells in the fast-charging cycle test.

Cycle Number	Laminated	Anode-Laminated	Cathode-Laminated	Non-Laminated
9	133.2 $\text{mAh}\cdot\text{g}^{-1}$	129.6 $\text{mAh}\cdot\text{g}^{-1}$	133.4 $\text{mAh}\cdot\text{g}^{-1}$	133.0 $\text{mAh}\cdot\text{g}^{-1}$
1508	112.5 $\text{mAh}\cdot\text{g}^{-1}$	111.4 $\text{mAh}\cdot\text{g}^{-1}$	99.3 $\text{mAh}\cdot\text{g}^{-1}$	100.4 $\text{mAh}\cdot\text{g}^{-1}$

From the cycling test results, there arise two unique conclusions. First, minimization of the surface resistance via cathode lamination cannot ensure a permanent reduction in capacity fading upon fast-charging cycles, as is shown from the cathode-laminated cell. Second, yet the partial lamination on the anode interface is sufficient to generate the well-known reduction of capacity fade during fast-charging cycles, as shown from the discharge capacity trend of the anode-laminated cell in Figure 5. The data therefore show clearly that the fast-charging capability arises only from lamination at the anode interface, while the cathode interface does not affect the fast-charging aging mechanisms.

The cells studied at the fast-charging cycle test were also characterized with EIS along the cycling. Figure 6 shows the trends of the respective datasets in the Nyquist plots.



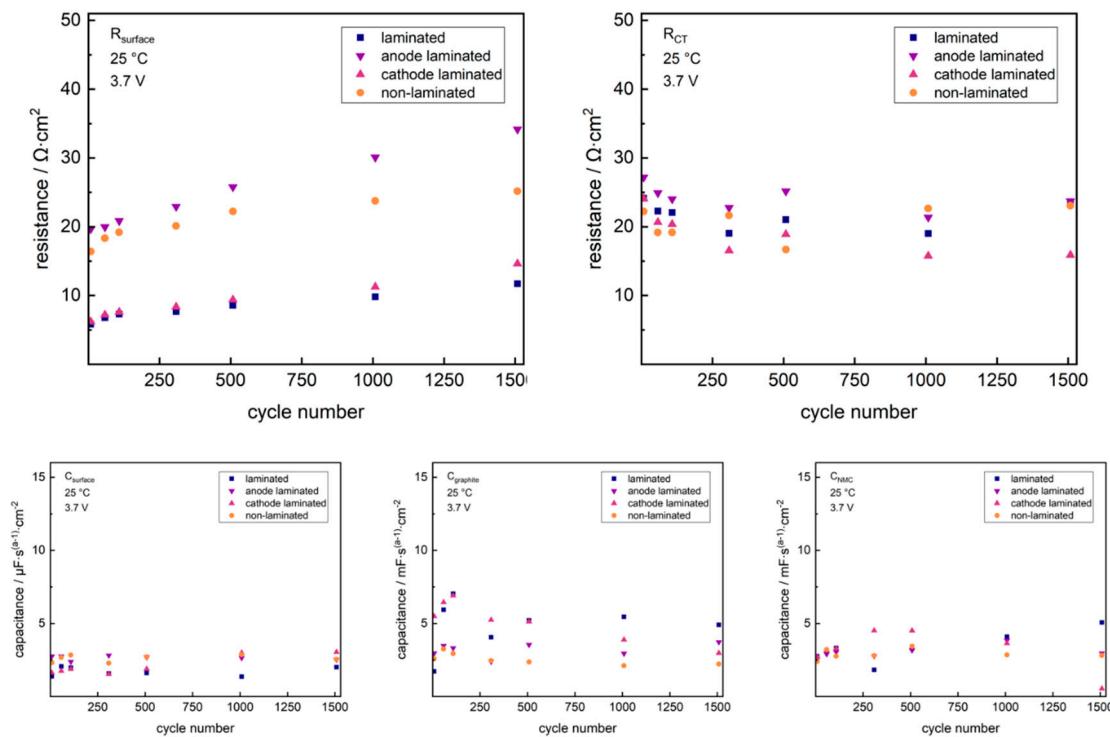
**Figure 6.** Impedance measurements of laminated/partially laminated/non-laminated cells: EIS (100 kHz–10 mHz) along fast-charging cycles; fitting curves indicated as solid lines; data points at  $10^3 \text{ Hz}$  and  $10^{-1} \text{ Hz}$  highlighted in pale blue.

Similar to Figure 1, the highlighted data point set at  $10^3 \text{ Hz}$  in Figure 6 lies close to the minimum between the first and second semicircle for all datasets, while the second highlighted dataset series at  $10^{-1} \text{ Hz}$  lies close to the minimum between the third semicircle and Warburg regime. Both benchmark frequency datasets do not change in relative position within the Nyquist datasets along cycling, indicating a negligible change of the time constant with cell aging at the chosen conditions. This correlates well to findings by Waag, W. et al. on NMC based full cells at moderate SOC [37].

To exclude side influences from cathode interface phenomena to the surface resistance signal, EIS aging studies focused on SEI effects require a minimization of the surface resistance starting condition. As discussed above, lamination at the cathode-separator interface minimizes the surface resistance previous to cycling influences. Initially, both the cathode-laminated and fully laminated cell have smaller surface resistance semicircles, while anode-laminated and non-laminated cell reveal enlarged surface resistance semicircles. All cells reveal, that the surface resistance semicircle increases with rising cycle number, while no clear trend for the charge-transfer semicircles arises along cycling for any cell. Further insights can be extracted by studying the semicircles in the equivalent circuit fit. Again, due to the structure of the chosen equivalent circuit, the open Warburg regime was excluded from the data fit. Figure 7 shows the trends of the resistances and capacitances calculated upon the fitting.

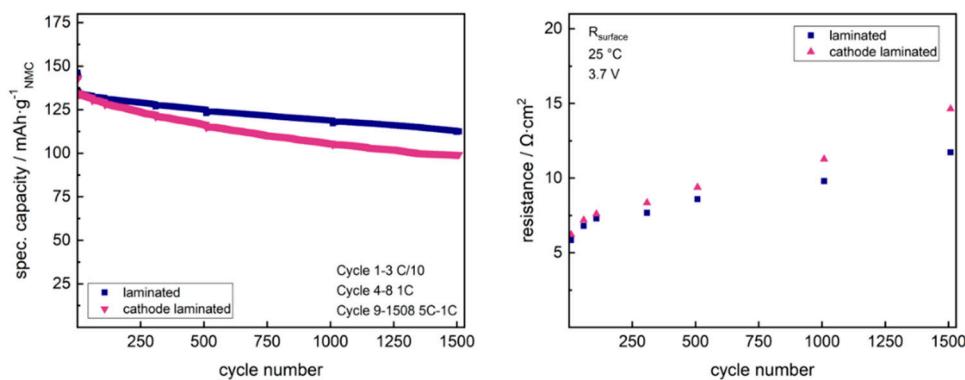
As both charge-transfer signals have drastic overlap, only the sum of the fitted charge-transfer resistances can be studied. No clear trend on the charge-transfer resistance signal along cycling is found for any lamination mode. Although all surface resistance signals differ in starting values, as indicated in the Nyquist plots, they all increase upon cycling. Both the capacitance fit parameters for the graphite anode and NMC cathode ( $3\text{--}4 \text{ mF}\cdot\text{s}^{(a-1)}\cdot\text{cm}^{-2}$ ) and the capacitance signals of the surface resistance semicircles ( $\sim 3 \mu\text{F}\cdot\text{s}^{(a-1)}\cdot\text{cm}^{-2}$ ) reveal no significant trend along cycling.

As discussed above, focusing on the SEI trends arising from the lamination modes requires minimization of the cathode influences on the surface resistance. Therefore, only the surface resistance signals of the cathode-laminated and fully laminated cell deliver unpersuaded information on the SEI changes.



**Figure 7.** EIS resistance fit parameters of laminated and non-laminated single cells along fast-charging cycles; data normalized to geometric electrode area.

As shown in Figure 8, both cathode-laminated and fully laminated cells have a minimized surface resistance of  $6.2 \Omega \cdot \text{cm}^2$  and  $5.8 \Omega \cdot \text{cm}^2$  at the eighth cycle. The cathode-laminated cell increases in surface resistance up to  $14.6 \Omega \cdot \text{cm}^2$  after 1508 cycles, while the laminated cell dampens the surface resistance growth to  $11.7 \Omega \cdot \text{cm}^2$  after 1508 cycles. This trend in surface resistance clearly proves a reduction in SEI growth, which is specifically due to the lamination at the anode-separator interface.



**Figure 8.** Decrease of discharge capacity vs. increase of surface resistance of laminated and cathode-laminated single cells along fast-charging cycles.

### 3. Materials and Methods

#### 3.1. Electrode Preparation

For preparation of anode slurries, MAGE3 graphite (HITACHI CHEMICAL, Sakuragawa, Japan), Solef® 5130 polyvinylidene difluoride (PVDF, SOLVAY, Milan, Italy), Super C65 carbon (IMERYS, Bodio, Switzerland) and SFG6L graphite (IMERYS) were mixed in a ratio of 90/7/2/1 with N-methyl-pyrrolidone (NMP, Overlack, Mönchengladbach, Germany) in a planetary mixer (TX 2, INOUE, Isehara, Japan), while for cathodes, LiNi<sub>1/3</sub>Mn<sub>1/3</sub>Co<sub>1/3</sub>O<sub>2</sub> (NMC, NM-3102 h, BASF TODA America, Battle Creek, USA), PVDF (SOLVAY), Super C65 carbon (IMERYS) and KS6L graphite (IMERYS) were mixed in a ratio of 93/3/3/1 with NMP. Anode and cathode slurries were coated on copper foil (15 µm, GELON LIB, Hong Kong, China) and aluminum foil (20 µm, GELON LIB), respectively, by single-side coating on a doctor-blade coater in a roll-to-roll process coating machine, including in-line drying in a two-step drying tunnel at the temperature range of 135–150 °C. The averaged active mass loadings of cathode and anode electrodes were ~8.4 mg·cm<sup>-2</sup> (1.30 mAh·cm<sup>-2</sup>) and ~4.2 mg·cm<sup>-2</sup> (1.51 mAh·cm<sup>-2</sup>), respectively. Cathodes and anodes were matched to have a capacity balancing factor of ~1:1.16 in all full cells.

#### 3.2. Pouch Cell Preparation

Within the pouch cell, punched cathode, anode and separator (inorganic filled separator, 67% Al<sub>2</sub>O<sub>3</sub> and 33% PVDF/HFP copolymer) sheets with the dimensions 5 × 8 cm<sup>2</sup>, 5.4 × 8.4 cm<sup>2</sup> and 5.8 × 8.8 cm<sup>2</sup> were assembled. For the fully laminated state, stacks of cathode-separator-anode were laminated to form a single stack by using a lamination machine (BLE 282 D, MANZ Italy, former Arcotronics Italia, Bologna, Italy) at the roll speed of 1.4 m·min<sup>-1</sup>, using a line force of 157 N·cm<sup>-1</sup> in the temperature range of 100–120 °C. For separate electrode-separator lamination, stacks of cathode-separator-PE (polyethylene) carrier and anode-separator-PE carrier were laminated at identical parameters. Pre-assembled pouch cell stacks were dried under vacuum at 110 °C for 12 h. 1 M LiPF<sub>6</sub> in ethylene carbonate (EC): ethylmethylcarbonate (EMC) 3:7 w/w (Selectlyte LP57, BASF, Florham Park, USA) and vinylene carbonate (VC, Vinylene Carbonate E, BASF, Florham Park, USA), mixed in a ratio of 98/2, was used as electrolyte. The pre-assembled stacks were filled with 1000 µL electrolyte within an argon filled glovebox (MB20, H<sub>2</sub>O and O<sub>2</sub> content <0.1 ppm, MBraun, Garching, Germany) and sealed under vacuum. Before starting the electrochemical characterization, wetting of all pores was ensured by keeping the cells at room temperature for 24 h previous to starting the formation cycles.

#### 3.3. Electrochemical Characterization

Electrochemical characterization was done with a battery tester (CTS-LAB, BaSyTec, Asselfingen, Germany) and a potentiostat (PGSTAT204, METROHM, Filderstadt, Germany). Cells were cycled between 3.0 V and 4.2 V, using a CCCV protocol for charging (constant current protocol followed by constant voltage protocol) with a CV termination below 0.05C rate, and CC protocol for discharging. Formation was done by applying three cycles at 0.1C, using the nominal capacity of the NMC in each cell, calculated from the specific NMC capacity of 155 mAh·g<sup>-1</sup>, given by the supplier. After formation, the discharge capacity of the third formation cycle was taken as the nominal capacity for C-rate calculation of all following steps.

For EIS analysis along SOC, cells were first discharged to 3.0 V at 0.2C rate after the fifth cycle, to then charge the cell up to each point of investigation at 0.2C rate. For EIS analysis along cycling, cells were charged to 3.7 V at 1C rate previous to EIS measurements at each specific cycle. Comparable temperature (25 °C) in EIS measurements was ensured by measuring in a cooled incubator (INCULine® IL 68 R, VWR, Ismaning, Germany). Cells rested for 2 h at OCV prior to each EIS measurement. EIS measurements were carried out in the frequency range of 100 kHz–10 mHz (potentiostatic mode) using an amplitude of 10 mV<sub>rms</sub>. For EIS data fitting the Z-fit protocol, included in the BT-Lab software, was used (BT-Lab V1.55, BioLogic SAS via GAMEC, Illingen, Germany).

To ensure reproducibility of the study, for each cell assembly mode at least three cells were prepared and studied thoroughly. At each path, the performance of the respective cell with lowest initial impedance contributions and lowest capacity fade along 1500 fast-charging cycles is shown and discussed.

#### 4. Conclusions

NMC/graphite full cells were studied in several lamination modes upon significant interface lamination effects revealed by EIS. Along variation of the SOC, both NMC cathode and graphite anode charge-transfer signals were found to stay independent from any lamination mode. The initial surface resistance gets minimized upon lamination at the cathode-separator interface previous to cycling influences.

Fast-charging cycling studies revealed a clear correlation of the reduction in capacity fade, to arise from lamination at the anode-separator interface. The surface resistance minimization via cathode-separator lamination was furthermore used to exclude cathode influences on the surface resistance signal evolution in cycling tests. Using this correlation, the cycling studies prove the fast-charging capability to arise from a reduction in SEI growth specifically arising from lamination at the anode-separator interface.

So, lamination at the cathode-separator interface is found to decrease the internal cell resistances, while lamination at the anode-separator interface reduces long term aging phenomena during fast-charging cycles.

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