

Article

Incremental Capacity-Based Variable Capacitor Battery Model for Effective Description of Charge and Discharge Behavior [†]

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Abstract

Determining charge and discharge behavior is essential for optimizing charging strategies and evaluating balancing algorithms in battery energy storage systems and electric vehicles. Conventionally, a sequence of circuit simulations or tedious hardware tests is required to evaluate the performance of the balancing algorithm. To mitigate these problems, this paper proposes a variable capacitor model that can be easily built from the incremental capacity curve. This model provides a direct and insightful R-C time constant method for the charge/discharge time calculation. After validating the model accuracy by experimental results based on the cylindrical lithium-ion cell test, a switched-capacitor active balancing and a passive cell balancing circuit are implemented to further verify the effectiveness of the proposed model in calculating the cell balancing time within 2% error.

Keywords: battery modeling; charge and discharge time; incremental capacity (IC); variable capacitor



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1. Introduction

Due to the rapid evolution of battery energy storage systems (BESS) and electric vehicles (EVs), the demand for high-capacity batteries has significantly increased. Depending on application requirements, multiple cells are connected in series and/or parallel to meet power and energy requirements [1–3]. However, their utilization comes with a set of challenges in ensuring the longevity and safety of these systems [4–6], and thus battery management systems (BMS) must implement effective charging strategies and cell balancing algorithms [7–9].

One of the most critical factors in both the charging control and balancing operation of batteries is accurate calculation of the charge/discharge time (CDT) [10–12]. In conventional practice, evaluating the performance of cell-balancing algorithms has been a challenging task. Typically, this process involves a sequence of circuit simulations or hardware tests [13–15]. While effective, these approaches are often time-consuming, resource-intensive, and not well suited for systems with large battery capacities. The scale and complexity of these systems necessitate an alternative approach that can provide direct and accurate calculations of the balancing time. Likewise, in multi-stage constant current charging algorithms [16,17], CDT approximation allows determining the stage duration for

various constant currents, energy distributions, and thermal behaviors. However, determining CDT is particularly challenging due to the non-linear and time-varying nature of battery behavior, especially under aging conditions.

Accurate modeling of battery behavior is essential for addressing these issues. Among the various modeling techniques available [18,19], equivalent circuit models (ECMs) have gained prominence in real-time applications due to their low computational complexity and straightforward model parameter extraction [20,21]. Conventional ECMs, such as the Randles model consisting of a variable voltage source and a resistor-capacitor (RC) network, are widely adopted (Figure 1). However, a drawback of the voltage source-based model is that the voltage source does not dynamically interact with the circuit without an external feedback mechanism, such as the state of charge (SOC) calculation (Figure 2a). Therefore, these models are often insufficient for predicting dynamic behaviors like CDT or balancing time without detailed time-domain simulations.

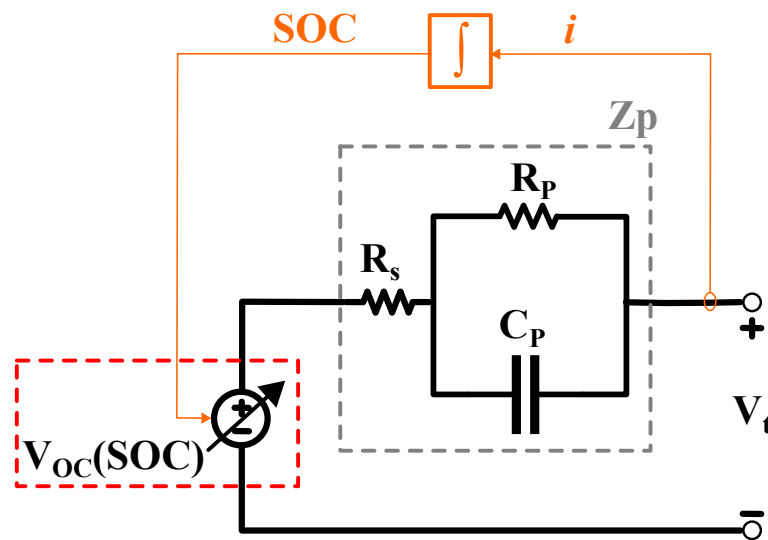


Figure 1. Variable voltage source battery model.

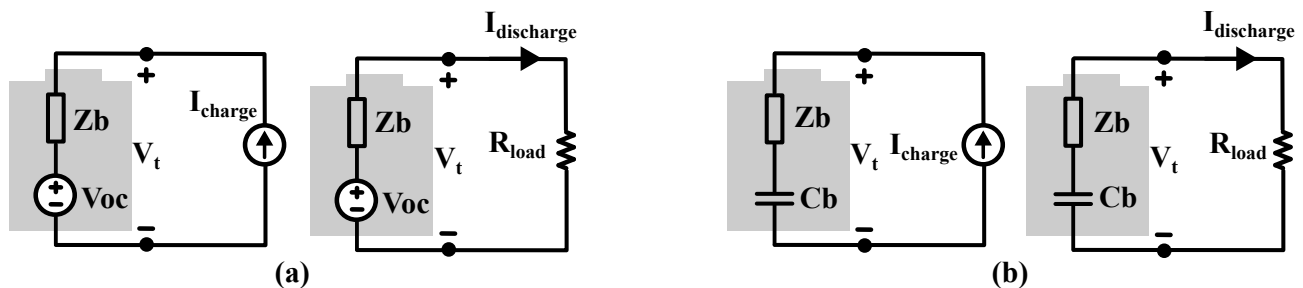


Figure 2. Battery model to describe the charge–discharge behavior. (a) Voltage source-based model; (b) Capacitor-based model.

In contrast, the capacitor-based battery model [22], as Figure 2b, is more circuit-friendly. Because capacitors naturally respond to changes in voltage, they provide a dynamic interaction with the circuit during charge and discharge processes, even without external SOC feedback. This characteristic enables analytical and effective CDT determination based on circuit parameters and voltage conditions. Figure 3 illustrates the existing capacitor-based battery models. Figure 3a presents a simple RC model that assumes constant capacitance C_b and resistance R_b [23]. While this approach offers ease of implementation for charging time calculation, it does not provide details for an accurate description of non-linear behaviors. In [24], the author introduced a more detailed resistance–capacitance battery model based on SOC and temperature as Figure 3b. While this model enhances the model

accuracy, it increases system complexity. Likewise, a non-linear double-capacitor model (Figure 3c) is proposed in [25]. The capacitor C_s integrates the current to set the SOC information to adjust the voltage source, allowing the battery dynamics to be captured, but it introduces additional complexity that limits its practical use in control algorithms and embedded systems.

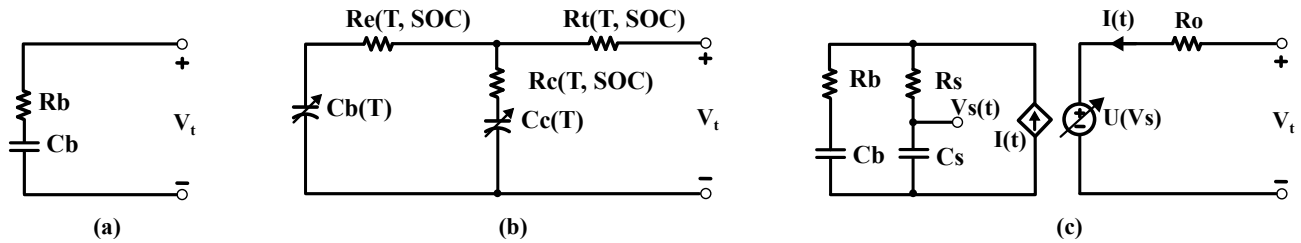


Figure 3. Conventional capacitor-based battery model (a) Simple RC model [23]; (b) RC model [24]; (c) Non-linear double-capacitor model [25].

To ensure the simplicity of the model and describe the battery non-linearity, this paper introduces an effective modeling approach that replaces the voltage-source structure with a variable capacitance model. This model is inspired by incremental capacity (IC) analysis [26–29], a technique that reveals the capacity fading and impedance increment of lithium-ion batteries by differentiating capacity with respect to voltage (dQ/dV). The IC profile directly reflects how the battery charge storage capacity varies with voltage, providing physically meaningful and electrochemically relevant information for modeling. Moreover, the IC curve is highly sensitive to aging phenomena, allowing the model to be easily updated with new IC data to reflect battery degradation. By leveraging the IC curve, the proposed model allows direct calculation of CDT using the R-C time constant method that is well established in circuit theory, offering a practical and computationally efficient method for predicting CDT. The contributions of this work are summarized as follows:

- A voltage-dependent capacitor battery model is proposed, which is directly obtained from the IC curve.
- Equivalent capacitance is introduced to approximately calculate the balancing time process, together with the circuit equivalent resistance.
- A balancing time calculation process is formulated for active balancing topologies as well as a passive balancing circuit.

The rest of the paper is organized as follows: Section 2 presents the derivation and formulation of the variable capacitor model. Section 3 discusses its application in balancing time calculation and integration with the balancing scheme. Finally, the conclusions are presented in Section 4.

2. IC-Based Variable Capacitor Battery Model

2.1. Model Formulation

The proposed model utilizes the relationship between the stored charge and the open circuit voltage (OCV) of the battery to determine the incremental capacitance. It adopts a simple structure consisting of a variable capacitor in series with the RC, as shown in Figure 4, where the capacitance changes depending on the OCV. The key idea is to replace the conventional variable voltage source in the Randles model with a variable capacitor. This variable capacitor can be combined with various battery models, depending on the specific application requirements.

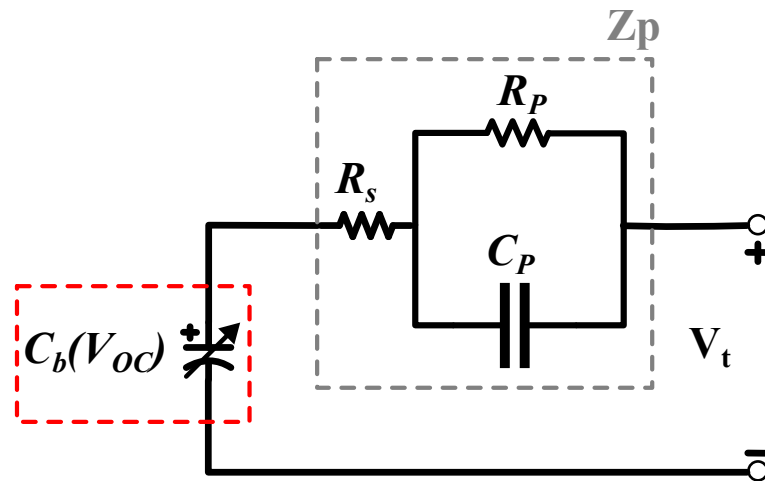


Figure 4. Proposed variable capacitor battery model.

To construct the proposed model, the capacitance at each OCV point is obtained by calculating the tangential slope of the capacity vs. the OCV ($Q - V_{OC}$) curve, as illustrated in Figure 5a. As a result, the capacitance function is defined by

$$C_b(V_{OC}) = \frac{dQ(V_{OC})}{dV_{OC}} \quad (1)$$

This derivative corresponds to IC, a diagnostic profile for assessing lithium-ion battery aging and internal characteristics, as shown in Figure 5b. Therefore, the IC curve can be directly utilized as the capacitance function in the proposed model.

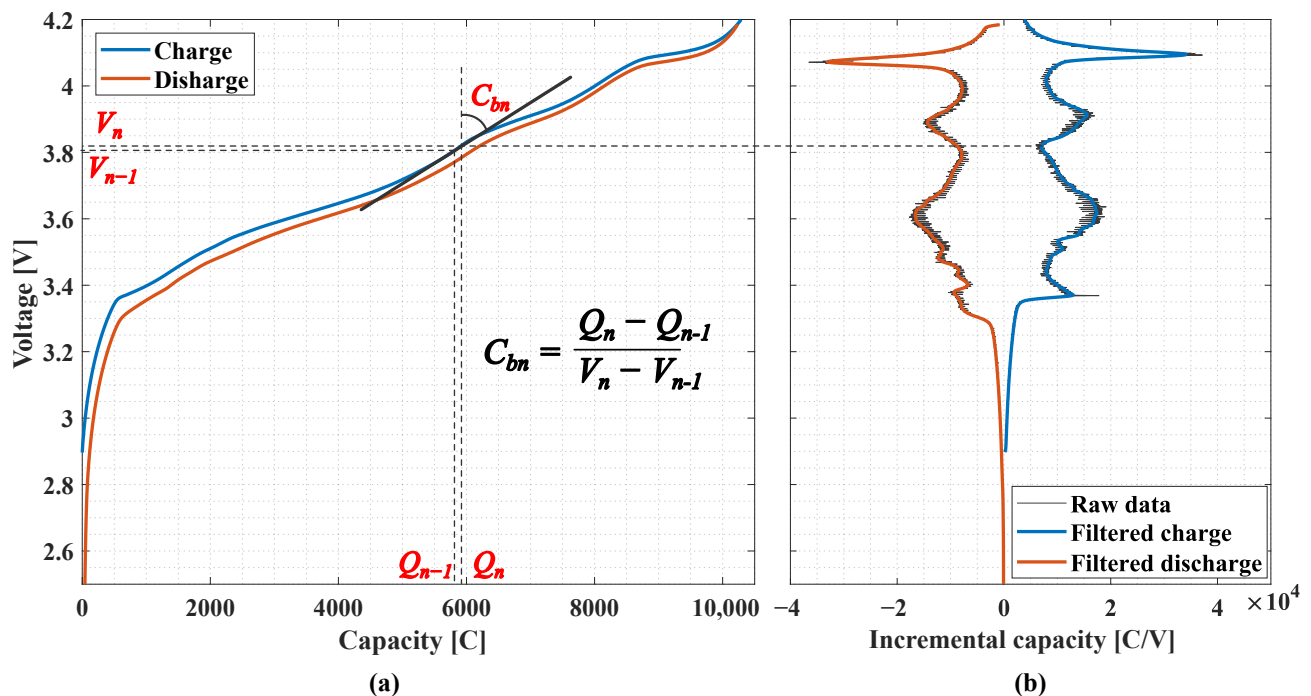


Figure 5. Battery charge–discharge profile according to the open circuit voltage. (a) Capacity; (b) Incremental capacity curve.

In this work, the IC curve is extracted from experimental data by conducting a constant current (CC) charge and discharge test at low current, typically $C/20$, to ensure that the terminal voltage closely approximates the true OCV. During this process, the battery voltage and corresponding cumulative capacity are recorded. The data are then uniformly

resampled with a fixed voltage interval, commonly set to 1 mV, to compute the derivative dQ/dV . To minimize the effects of measurement noise and enhance the smoothness of the resulting curve, a low-pass filter is applied during data processing.

To simplify the hysteresis between charge and discharge processes, the average absolute of the charge and discharge IC curves, as illustrated in Figure 6, is used in constructing the model and to ensure a consistent and representative capacitance profile across the entire voltage range.

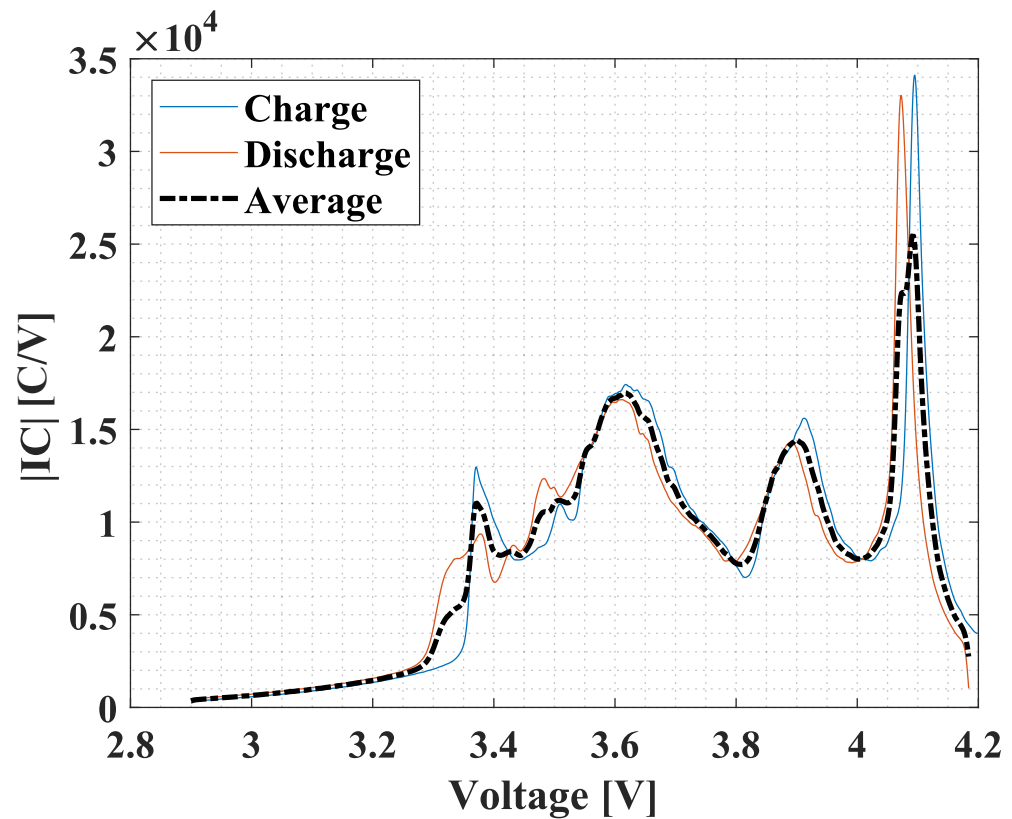


Figure 6. Absolute averaging process for the charge and discharge IC curve.

2.2. Model Validation

To validate the accuracy of the proposed model, a simulation schematic is implemented using the circuit simulation software, PLECS [30]. Experimental reference data are obtained from a cylindrical Li-ion cell (SDI, INR18650-29E, 3.6 V/2.85 Ah) under controlled laboratory conditions at 25 degrees Celsius. The cell is fully charged using CC at a 0.5 C-rate, followed by a constant voltage (CV) phase at 4.2 V with a cutoff current of 55 mA. Subsequently, the cell is discharged at multiple constant current levels—0.5 C, 1 C, 1.5 C, 2 C, and 3 C—until reaching a cutoff voltage of 2.5 V, also at 25 degrees Celsius ambient temperature.

The comparison results in Figure 7 illustrate that the terminal voltage profiles of the proposed model closely match the experimental data during both charging and discharging stages. At the end of discharge, the voltage deviation between the model and measured values is negligible. The mean absolute percentage error (MAPE), summarized in Table 1, indicates high accuracy, with a MAPE of 0.031% during the CC charging stage and 0.124% at the maximum 2 C-rate discharge. These results confirm that the variable capacitor model effectively captures battery behavior in both charge and discharge conditions.

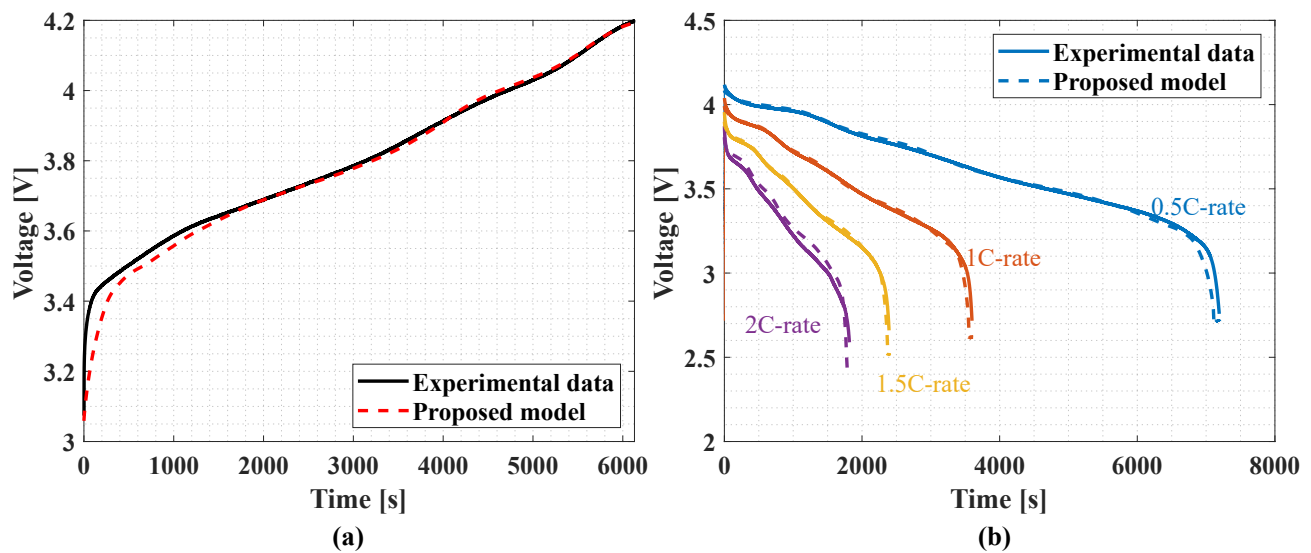


Figure 7. Terminal voltage comparison of the experimental data and the proposed model simulation (a) 0.5 C-rate CC charging; (b) CC discharging in various C rates.

Table 1. Terminal voltage error for the test in Figure 7.

Stage	Current	MAPE [%]
Charge	0.5 C-rate	0.031
Discharge	0.5 C-rate	0.040
	1 C-rate	0.046
	1.5 C-rate	0.033
	2 C-rate	0.124

3. CDT Calculation for Cell Balancing

One of the key advantages of the proposed variable capacitor model is its ability to provide direct and accurate calculations of the cell balancing time. In this study, the balancing time is selected as a representative use case to validate the CDT calculation procedure, as it inherently includes charge and discharge behavior during the balancing operation. In both active and passive balancing schemes, determining the charge transfer duration is essential for control design and efficiency evaluation. The model allows direct computation of the balancing time based on the capacitance and initial cell voltage conditions, without requiring simulations or hardware tests.

The equivalent capacitance, C_{eq} , is defined based on the IC-to-voltage relationship of the battery cell, capturing its dynamic behavior during the balancing process. In practical balancing circuits, this capacitance works together with the circuit equivalent resistance, R_{eq} , to determine the time constant. While C_{eq} is determined by the battery characteristics, R_{eq} depends on the specific balancing topology and hardware implementation. Detailed considerations of R_{eq} for various methods are discussed in later sections.

3.1. Active Cell Balancing

In active balancing systems, intermediate energy transfer circuits such as switching capacitors, switching inductors, or converters are used to transfer charge from higher voltage cells to lower ones [31]. Among these structures, switched-capacitors (SC) [32] are known to be attractive due to their high efficiency, modularity, and cost-effectiveness. In this work, a single switched-capacitor (SSC) balancing configuration [13] is adopted for the practical application of the proposed variable capacitor model. The SSC equalizer facilitates energy transfer between cells in a battery string through the operation of a

balancing capacitor, $C_{balancing}$, as shown in Figure 8a. During operation, the balancing capacitor, $C_{balancing}$, connects to cells through switches, allowing charge to flow from the higher voltage cell to the lower voltage cell.

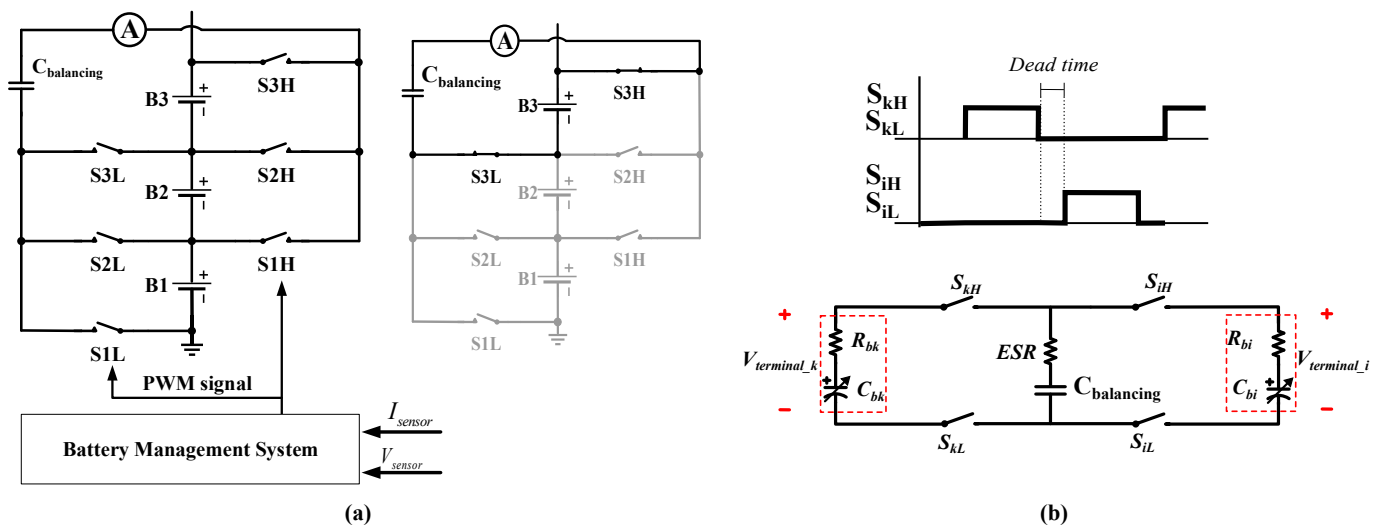


Figure 8. Single switched-capacitor equalizer. (a) Topology structure and operation; (b) Its equivalent circuit.

The proposed model is applied to this topology to enable simple and accurate calculation of the balancing time. In this case, the battery is modeled using a variable capacitor in series with an internal resistor to keep the structure simple and computationally efficient, as in Figure 8b. By doing this, CDT in the transfer process can be directly calculated using the R-C time constant.

To determine the charge-equivalent capacitance C_{eq} of a cell, the model utilizes the IC profile. In this context, the IC is considered as the cell instantaneous capacitance, C_b . As shown in Figure 9, C_{eq} reflects the charge-equivalent capacitance of the cell across a specified voltage range of interest.

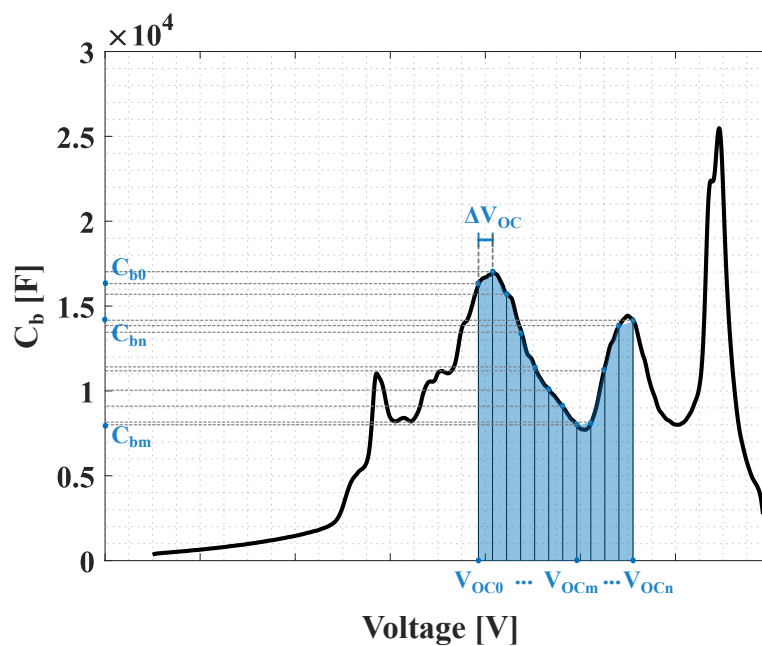


Figure 9. The charge-equivalent capacitance over a voltage range using the trapezoidal method.

The trapezoidal integration method is employed to calculate C_{eq} , offering a trade-off between numerical accuracy and computational simplicity [33]. This method is well suited when working with a discrete or experimentally obtained IC curve. The final expression for C_{eq} is derived in

$$C_{eq}(V_{OC}) = \frac{\Delta V_{OC} [\frac{C_{bn} + C_{b0}}{2} + \sum_{m=1}^{n-1} C_{bm}]}{V_{OCn} - V_{OC0}}, \quad (2)$$

where C_{bm} refers to the slope of the $Q - V_{OC}$ curve at the m -th voltage step, representing how much charge is stored per unit voltage. C_{b0} and C_{bn} are the slope values at the start (V_{b0}) and the end (V_{bn}) of the voltage range, respectively. ΔV_{OC} denotes the constant voltage interval between data points used for numerical integration.

On the other hand, the equivalent resistance [13] of the SSC balancing circuit in Figure 8 is found by

$$R_{eq} = \frac{1}{f_s C_{balancing}} \frac{1 + e^{-D/(f_s \tau)}}{1 - e^{-D/(f_s \tau)}}, \quad (3)$$

$$\tau = C_{balancing}(ESR + R_b), \quad (4)$$

where f_s is the switching frequency of the balancing circuit, D is the duty ratio, and τ is the circuit time constant that can be calculated as the product of the balancing capacitor, $C_{balancing}$, and the total resistance, which is the sum of the equivalent series resistance (ESR) of the balancing capacitor and the internal resistance of the cell, R_b .

Based on the equivalent charge transfer analysis, the voltage after completing the balancing process is identified by

$$V_b(t) = V_{0,i} + \frac{C_{eq,k}(V_{0,k} - V_{0,i})}{C_{eq,i} + C_{eq,k}} (1 - e^{-\frac{t}{\tau_b}}), \quad (5)$$

$$\tau_b = \frac{R_{eq} C_{eq,i} C_{eq,k}}{C_{eq,i} + C_{eq,k}}, \quad (6)$$

where τ_b is the balancing time constant, the subscripts i and k denote the lower and higher voltage cell, $V_{0,i}$ and $V_{0,k}$ denote the battery initial voltages, $C_{eq,i}$ and $C_{eq,k}$ represent the charge equivalent capacitance, and R_{eq} is the equivalent resistance of the equalizer circuit given in Equation (3).

For a given target voltage difference between the two cells, ΔV_b , defined by Equation (7), the total balancing time to achieve that balancing state can be calculated by Equation (8).

$$\Delta V_b = V_{b,k} - V_{b,i} = (V_{0,k} - V_{0,i}) e^{-\frac{t_b}{\tau_b}} \quad (7)$$

$$t_b = \tau_b \ln\left(\frac{V_{0,k} - V_{0,i}}{\Delta V_b}\right) \quad (8)$$

To validate the proposed calculation method, a PLECS simulation is conducted using two Li-ion batteries with initial SOC levels of 80% and 60%, connected in series and interfaced with an SSC balancing circuit. The battery model is equipped with cylindrical cell (SDI, INR18650-29E, 3.6 V/2.85 Ah) characteristics. The initial voltages of the cells are set to 4.0089 V and 3.7970 V, respectively.

The simulation parameters are configured as follows: the balancing capacitor is 2200 μ F, the switching frequency is chosen as 20 kHz with a PWM duty of 0.45, the balancing capacitor ESR is 0.15 Ω , and the internal resistance of the cell is 0.035 Ω .

Figure 10 shows the gradual convergence of the two cell voltages, eventually reaching a balanced state. The equivalent resistance, R_{eq} , of the SSC circuit is calculated as 0.8224Ω by Equation (3). Using Equation (2), the charge-equivalent capacitance, C_{eq} , for each cell is determined, which allows access to the balancing time through Equations (5) to (8). The computed balancing time is compared with the simulation results at several time instants, as summarized in Table 2. At each time instant, the OCV of the k -th and i -th cells are recorded, and the corresponding C_{eq} values are calculated based on those voltages. The comparison shows that the calculated balancing time deviates from the simulated results by within 2.04%.

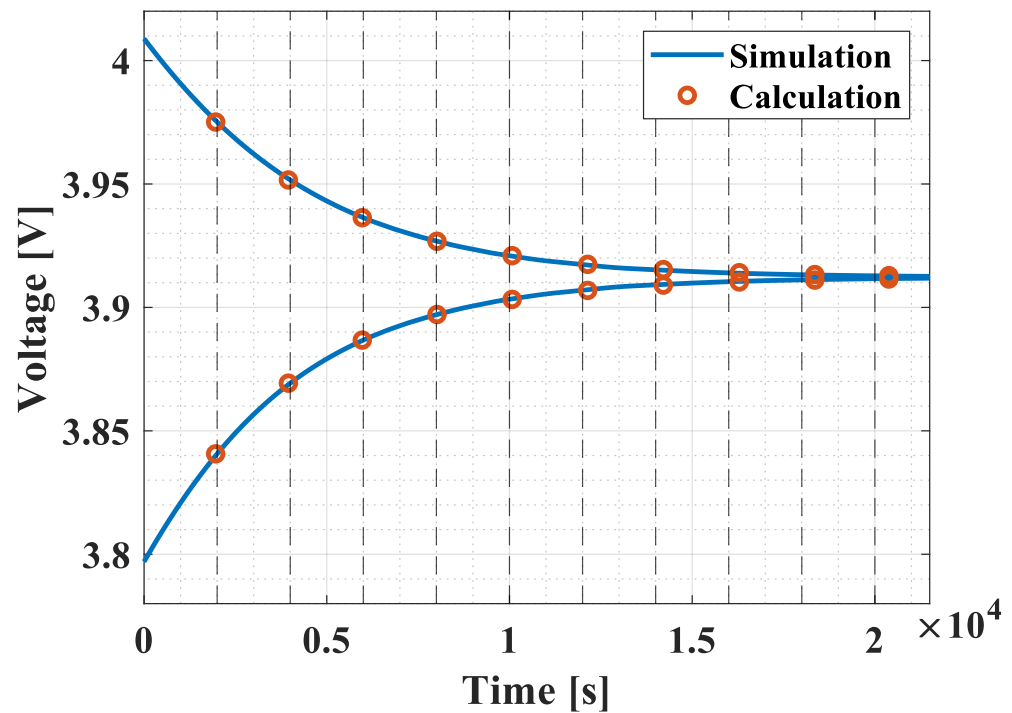


Figure 10. Voltage waveform of the balancing process.

Table 2. Comparative result for the active balancing time.

Time [s]	$V_{b,k}$ [V]	$V_{b,i}$ [V]	$C_{eq,k}$ [F]	$C_{eq,i}$ [F]	ΔV_b [mV]	t_{sim} [s]	t_b [s]	t_{error} [%]
2000	3.975	3.841	12,002.63	9283.09	134.43	2000	1959.11	2.04
4000	3.952	3.869	11,490.82	9100.40	82.32	4000	3949.03	1.27
6000	3.936	3.887	11,183.37	9039.34	49.58	6000	5971.65	0.47
8000	3.927	3.897	11,004.61	9022.76	29.67	8000	8016.20	−0.20
10,000	3.921	3.903	10,900.80	9020.14	17.72	10,000	10,073.07	−0.73
12,000	3.917	3.907	10,840.22	9021.14	10.57	12,000	12,140.47	−1.17
14,000	3.915	3.909	10,804.68	9022.64	6.31	14,000	14,209.55	−1.50
16,000	3.914	3.910	10,783.58	9023.85	3.76	16,000	16,289.74	−1.81
18,000	3.913	3.911	10,771.21	9024.68	2.25	18,000	18,355.77	−1.98
20,000	3.913	3.912	10,763.67	9025.19	1.36	20,000	20,383.05	−1.92

The calculated balancing time, t_b , closely matches the simulation result, t_{sim} . This confirms the effectiveness of the proposed variable capacitor model for predicting the balancing behavior in active balancing systems.

3.2. Passive Cell Balancing

Although active balancing offers higher efficiency, passive balancing remains widely used in industry due to its simplicity and cost-effectiveness [34]. Figure 11a illustrates a typical passive cell balancing configuration. The balancing resistors discharge the cell with the highest voltage, reducing its voltage until it matches with the other cell voltages in the pack. This process continues until all the cells are balanced. In this scheme, the equivalent circuit incorporated with the proposed variable capacitor model in Figure 11b consists of a capacitor and resistors. It means that the balancing time can be directly determined simply by the R-C time constant. In this model, the charge equivalent capacitance is derived by Equation (2), while the equivalent resistance of this circuit is the sum of the discharging resistance, R_i , and the internal resistance of a battery, R_{bi} , for each cell.

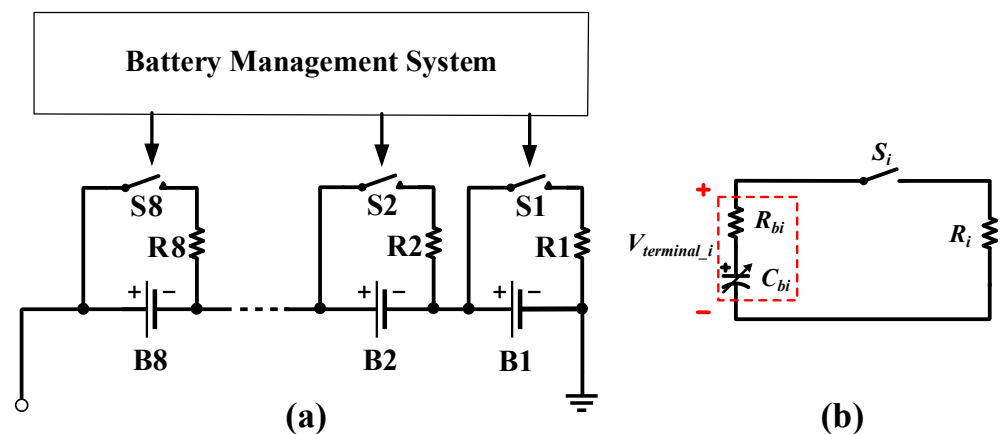


Figure 11. Passive cell balancing circuit. (a) Topology structure; (b) Equivalent circuit.

In order to validate this approach, an experiment on the passive balancing process is implemented at room temperature as illustrated in Figure 12. Eight cylindrical Li-ion cells (SDI, INR18650-29E, 3.6 V/2.85 Ah) with different initial SOC levels are controlled by a passive balancing chip (Analog Device, LTC6804) with a 27 Ω balancing resistor. Cell voltage data during operation are recorded using a data logger (HIOKI, LR8420). For the battery model, the internal resistance of a cell is measured as 35 m Ω by an impedance analyzer (ZIVE, SP10). By summing the series resistances, the equivalent resistance (R_{eq}) is obtained as 27.355 Ω , including 0.32 Ω for a switch on-resistance and a small wiring resistance. The summary of the test setup is shown in Table 3.

Table 3. Summary of experimental equipment and test conditions of passive balancing.

Experimental Item	Specification
Battery cell	SDI, INR18650-29E, 3.6 V/2.85 Ah
Temperature	Room temperature
Passive balancing chip	Analog device, LTC6804
Data logger	HIOKI, LR8420
Impedance analyzer	Zive SP10

The cell voltage profiles observed throughout the balancing process are illustrated in Figure 13. Since cells #7 and #8 have the lowest initial voltages, they are not connected to discharge resistors. The remaining cells, with voltages exceeding those of cells #7 and #8, are connected to the discharging resistor until ΔV becomes less than 13 mV.

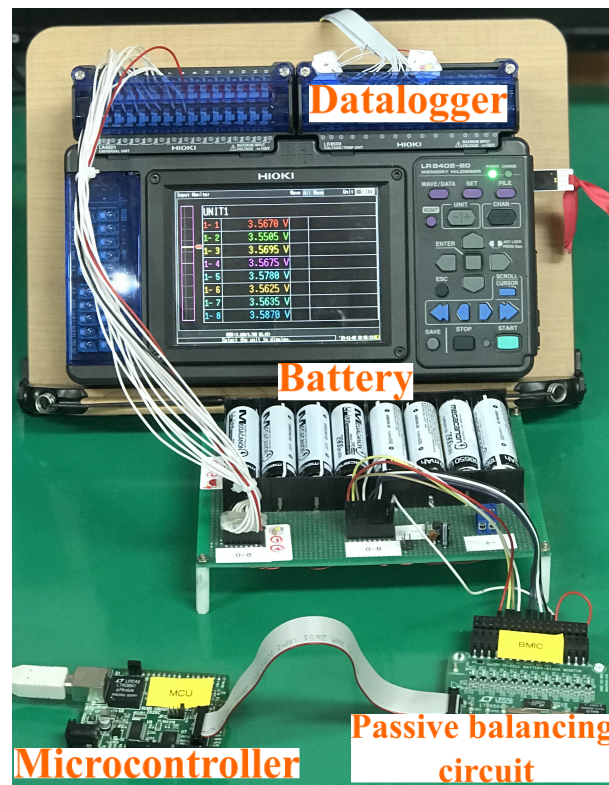


Figure 12. Experimental setup of the passive cell balancing test.

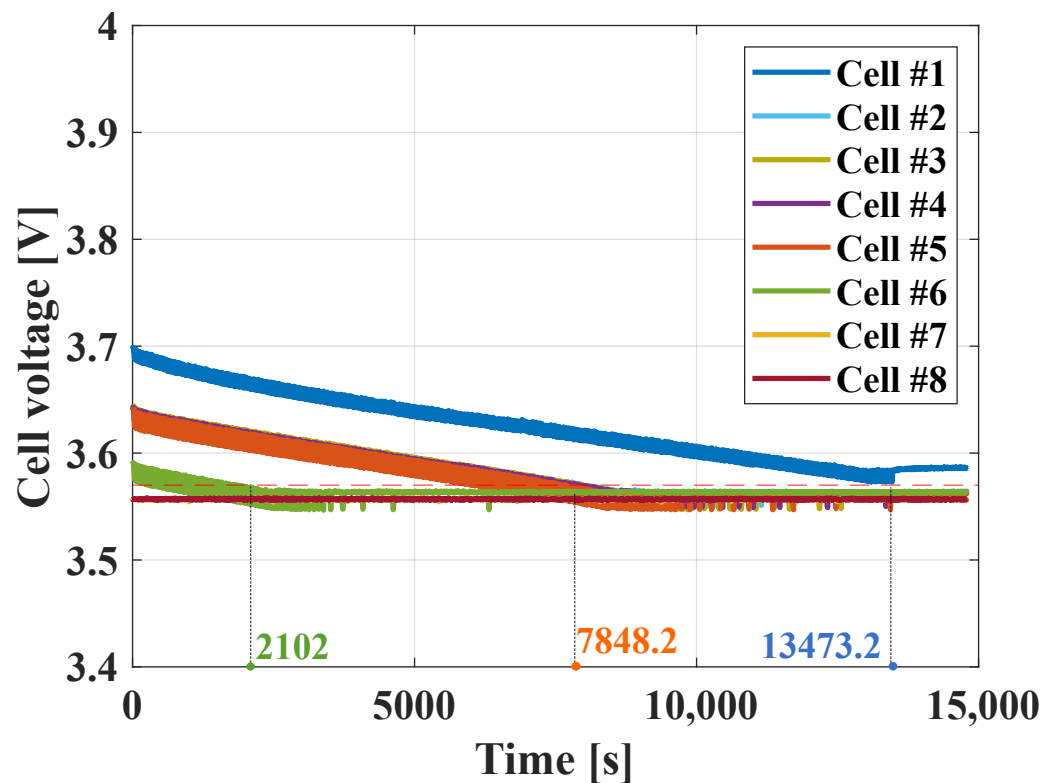


Figure 13. Cell voltages of the passive balancing experiments.

Table 4 presents a comparative analysis of the results obtained from the balancing time measurements and the proposed calculations, denoting t_{exp} and t_{cal} as the balancing times in the experiment and the calculation, respectively. The results substantiate that the calculation of the passive balancing time closely aligns with the actual results, with an error of 2.011%.

Table 4. Comparative results for the passive balancing time.

Cell	SOC_{init}	SOC_{target}	V_{init} [V]	V_{target} [V]	C_{eq} [F]	R_{eq} [Ω]	t_{cal} [s]	t_{exp} [s]	t_{error} [%]
#1	0.49	0.32	3.698	3.57	13,731.574	27.355	13,232.046	13,473.2	1.790
#2, #3, #4	0.42	0.32	3.643	3.57	14,029.867	27.355	7768.587	7848.2	1.014
#5	0.34	0.32	3.59	3.57	14,031.207	27.355	2144.272	2102	−2.011
#6, #7	0.30	-	3.557	-	-	-	-	-	-

3.3. Discussion

Overall, the results from both active and passive balancing case studies confirm the effectiveness of the proposed variable capacitor model in providing effective and accurate calculation of the balancing time. The validated results demonstrate that the CDT can be determined by using the proposed calculation process with calculation errors of 2.04% and 2.01% for active and passive cell balancing, respectively. Besides its apparent simplicity, the proposed model proves to be a valuable tool in evaluating the performance of balancing circuits. It is not only suitable for circuit design tasks such as evaluating balancing algorithms or designing charging strategies, but also shows potential for practical deployment. By integrating with charging control schemes, the model enables real-time estimation of charge and balancing durations in the BMS. Its compatibility with both active and passive balancing architectures affirms its flexibility and applicability for diverse system designs.

The calculation process for determining the balancing time is summarized in Figure 14. First, the initial voltage, V_{b0} , and target voltage, V_{bn} , are defined. Using the IC curve of the cells, the charge-equivalent capacitance, C_{eq} , is calculated via Equation (2). And then the equivalent resistance, R_{eq} , is obtained based on the circuit type, using Equation (3) for the SSC, or as the total series resistance in the passive circuit. For various active balancing circuits, the equivalent circuit resistance is summarized in Table 5, with their circuit configurations shown in Figure 15. Finally, the balancing time, t_b , is calculated by Equation (8).

The charge-equivalent capacitance, C_{eq} , is formulated to capture the voltage-dependent dynamic behavior of lithium-ion cells during the balancing process in Section 3.1. While previous analyses focused on the SSC and passive balancing scheme, the concept of R_{eq} can be extended to other active balancing architectures as well. For example, in a switched-inductor equalizer [35], R_{eq} includes the inductor resistance (R_L), the internal resistance of the battery cells (R_{bi} and R_{bi-1}), and the duty cycle (D). For capacitor-based balancing topology [36], R_{eq} is a function of the angular resonant frequency (ω_r), the inductance (L), the capacitance (C), and the total parasitic resistance of each resonant loop (R), and depends on the switching frequency (f_s). In transformer-based circuits [37], R_{eq} is modeled using the duty cycle (D), battery internal resistance (R_{bi}), and ESR of the output filter (R_{Lfi} and R_{Cfi}), as well as the on-resistance of MOSFET (R_{oni}), and the parasitic resistance in the resonant path (R_i). By incorporating these topology-specific resistances, R_{eq} , into the proposed battery model, the balancing time can be directly determined.

As batteries degrade, both the $Q - V_{OC}$ relationship and the internal impedance require periodic updates to the model to maintain accuracy. By leveraging the IC curve [26–29,38], these aging-related changes can be easily incorporated, allowing the model to adapt over time. This adaptability is essential for ensuring the long-term reliability and relevance of the battery model across the entire operational lifespan.

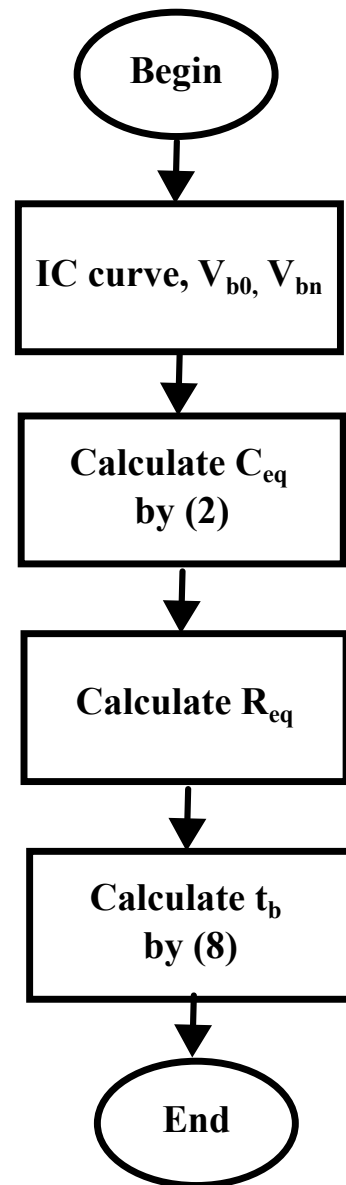


Figure 14. Balancing time calculation process.

Moreover, the proposed model structure, if combined with a lookup table (LUT) approach for implementing the variable capacitance $C_b(V_{OC})$, offers a natural extension for including temperature effects. Multiple IC profiles can be experimentally obtained and stored in a LUT by temperature. During operation, $C_b(V_{OC}, T)$ can be interpolated in real-time based on the measured cell temperature, T . Similarly, temperature-dependent models of internal resistance $R_b(T)$ allow the model to reflect realistic thermal behavior. As a result, the proposed model enables improved accuracy under varying thermal conditions.

Table 5. Equivalent resistance, R_{eq} , expressions for different active balancing topologies.

Active Balancing Topology	Switched-Inductor [35]	Switched-Capacitor [36]	Multiwinding Transformer [37]
R_{eq}	$R_L + (1 - D)R_{bi-1} + DR_{bi}$	$\frac{1+e^{-\beta\pi/\omega_T}}{Cf_s(1-e^{-\beta\pi/\omega_T})}$ where $\beta = R/(2L)$	$R_{BLi} + \frac{1-D}{D}R_{Cfi} + \frac{1}{D}(R_i + R_{oni})$ where $R_{BLi} = R_{bi} + R_{Lfi}$

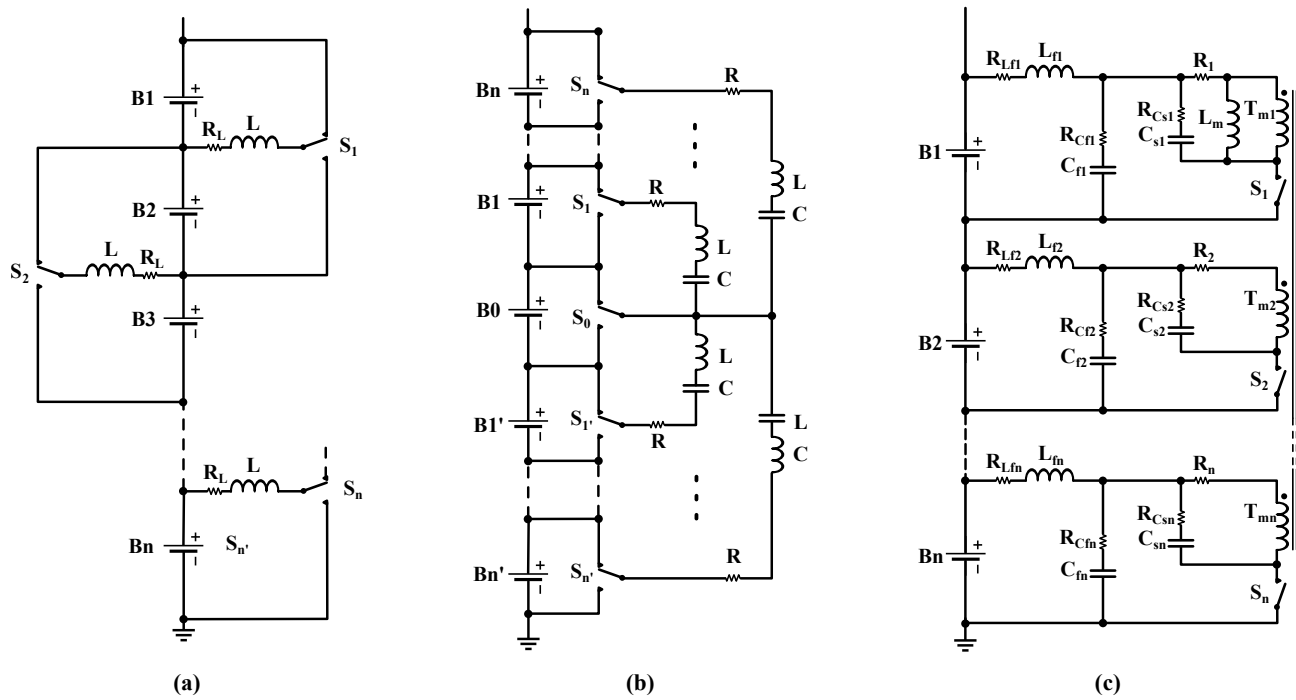


Figure 15. Various active balancing circuits. (a) Switched-inductor [35]; (b) Switched-capacitor [36]; (c) Multiwinding transformer [37].

4. Conclusions

This paper presents a battery modeling approach based on a variable capacitor that can be built from the IC curve. The proposed model enables direct determination of the balancing time through the R-C time constant, applicable to both active and passive balancing circuits. Simulation and experimental results demonstrate the model's practicality and accuracy, validating its effectiveness for balancing time prediction. Owing to its simple structure, the model is well suited for real-time BMS applications. Furthermore, utilization of the IC curve facilitates easy adaptation to battery aging, as evolving IC curves allow periodic updates. This makes the proposed model a scalable and flexible solution for long-term battery monitoring and control. Future work should focus on a more in-depth analysis of how temperature and aging effects influence charge-equivalent capacitance and CDT calculation accuracy. In addition, the influence of hysteresis effects on the IC-derived capacitance profile warrants further study to enhance model performance.

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