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Inductor-Based Active Balancing Topology with Wide Voltage Range Capability

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Abstract: With the increasing number of batteries integrated into the grid, the electrification of transportation, and the importance of reusing secondary batteries to preserve natural resources, active balancing techniques are becoming critical for optimizing battery performance, ensuring safety, and extending their lifespan. There is a demand for battery management solutions that can efficiently manage the balancing of battery cells across a wide range of voltage levels. This paper proposes a new inductor-based active balancing topology that achieves balancing by transferring energy from battery cells to the battery pack. One of its main advantages over existing designs is that it can operate over a wide battery cell voltage range. Moreover, multicell balancing with a balancing current independent of the imbalance level can be achieved by adjusting the width and interval of pulses. The proposed topology can be implemented using traditional low-side gate driving integrated circuits, avoiding the need for expensive isolated power modules and high-side gate drivers. Sample balancer designs for low-voltage battery cells as well as higher-voltage cells are provided. The presented experimental results verify the operation of the proposed balancer on a lithium-ion battery pack.

Keywords: battery; energy storage; active balancing; driver circuits; battery management systems



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1. Introduction

Energy storage systems, such as batteries and supercapacitors, are used in various commercial and consumer applications, such as electric vehicles (EVs), uninterruptible power supplies (UPS), and distribution systems. To meet the required power demand, individual cells are interconnected in both series and parallel configurations to achieve the necessary voltage and power ratings [1].

The automotive industry experienced a significant increase in the demand for lithium-ion (Li-ion) batteries, rising from 330 GWh in 2021 to 550 GWh in 2022, marking a 65% increase. This uptick in demand can be attributed to the growing sales of electric passenger cars, which saw a remarkable 55% increase in new registrations in 2022 compared to 2021 [2]. Unfortunately, this surge in demand will result in the retirement of 100–200 gigawatt-hours worth of batteries by 2030 as they are no longer suitable for EV use. This will present a significant challenge, as the toxic content and reactive properties of the batteries are hazardous.

As the demand for batteries escalates with the rise of renewable energy systems and electric vehicles, there is a growing interest in repurposing retired battery packs. Although no longer useful for their primary applications, retired batteries still contain a significant capacity and energy storage capability, which can be utilized in secondary applications such

as stationary energy storage systems, off-grid solutions, and household PV units [3,4]. As a result, there has been an increasing interest in repurposing these batteries for secondary applications to extract more value from these assets and contribute to a more sustainable and circular economy.

Energy storage systems utilize a variety of different types of cells. For example, lithium-titanate batteries and supercapacitors are ideal for high C-rate applications in heavy vehicles and locomotives. Redox flow batteries are a safe alternative for energy storage facilities. However, their different electrochemical characteristics result in varying voltage levels of the cells, which makes them incompatible with current commercial battery management integrated circuits (ICs) designed for lithium-ion cells.

The battery cells capacity inconsistency is one of the main contributing factors to the imbalance. It also significantly impacts the overall battery pack capacity, with the smallest capacity cell being the limiting factor [5]. Additionally, as the number of charging and discharging cycles increases, the capacity disparity can further exacerbate the system's performance.

Therefore, developing a practical active balancer that can operate over a wide cell voltage range and, hence, be compatible with different electrochemistry cell types is of significant interest.

Research on active balancing methods can be categorized into three major categories: capacitor-based, inductor-based, and transformer-based [6,7]. The optimal switching capacitor-based balancer in [8,9] significantly reduced the number of switches required per cell, improved the balancing speed, and achieved multicell balancing compared to traditional adjacent cells balancing topology in [10]. This type of balancer has been applied to some commercial products as it has a simple driving circuit and no control is required, which simplifies implementation. However, the capacitor-based balancer exhibits three inherent limitations. Firstly, its balancing speed is contingent on capacitance value, and uncontrolled balancing currents render it incapable of eliminating inrush currents. Secondly, the necessity of employing large capacitors with adequate voltage ratings increases production cost. Lastly, when cell voltage variations are negligible, the balancing current diminishes to very low levels, which significantly elevates the energy consumption of its driving circuit in comparison to the actual balancing power utilized.

Transformer-based balancing methods can be classified into two categories: isolated DC-DC converters and multi-winding transformer-based. Current commercial solutions offered by companies such as Texas Instruments and Analog Devices typically employ flyback converters to facilitate energy transfer from individual cells to the battery pack. These solutions often rely on complex switching matrices utilizing MOSFETs and specialized integrated circuits, or alternatively, they utilize standalone converters for each cell. However, these approaches are associated with high costs and are heavily dependent on specific integrated circuit manufacturers, limiting their scalability and adaptability to different battery management systems [11,12].

Research advancements have improved balancers utilizing multi-winding transformers, making multicell balancing feasible [13–17]. The iterative refinement of driving and control methods has simplified their implementation. However, challenges persist in terms of efficiency, transformer size, automated assembly complexity during manufacturing, and transformer customization, all of which have significant drawbacks for industrial applications.

Inductor-based balancers [18–23] and L-C balancers [23] present several challenges. Early-stage designs exhibited low efficiency due to diodes being used in the current path to a cell and being used in lower voltage applications [18,19]. Additionally, the inductor-based balancer in [20] was restricted to balancing between adjacent cells only. Other approaches required a high number of floating MOSFETs, which necessitated expensive

driving circuits, including isolated power modules and isolated gate driving ICs [21–23]. A high-speed simple topology was proposed in [24], but the cost of the required driving circuit and uneven charging of other cells while balancing remained significant drawbacks. Hence, further research and development are necessary to devise new topologies that are compatible with low-cost driving circuits and offer high operating efficiency.

This paper proposes a novel inductor-based low-cost balancing topology that is compatible with various cell voltage ranges, has multicell simultaneous balancing capability, controllable balancing current, a simple control strategy, and does not require specific integrated circuits or a controller. Table 1 summarizes the comparison of the proposed balancer with the existing balancing topologies, which meet more than one out of three criteria in the left column.

Table 1. Comparison of the proposed balancer with the existing balancing topologies.

	References: [11–17,19] #, [21,23] *	References: [1,8–10,18,20,22] **	References: [24] ***	Proposed
Maintaining a consistent balancing speed regardless of imbalance levels	✓		✓	✓
Eliminating isolated power modules and gate drivers		✓		✓
Avoiding complex control systems or specific controller ICs		✓	✓	✓

* Quiescent current loss, not suitable for cell level balancing, customised magnetic components. ** Slow one-by-one balancing speed or increased power losses when balancing adjacent cells. *** Bulky power modules, quiescent current loss. # Although this topology uses only one inductor, the overall cost is high as it requires isolated power modules and isolated gate drivers.

2. Proposed Balancing Topology Description

The proposed active balancing topology for an n -cell series-connected battery pack is illustrated in Figure 1. It requires n pairs of switches, n inductors, n pairs of Schottky diodes, and n dual-output low-side driving ICs.

The operation of the circuit is controlled by a pulse signal, which synchronously turns on and off the switch-pairs during the balancing process. The operational principle involves two sequential steps: initially, both switches are closed, facilitating energy transfer from the cell to the inductor (as indicated by the red arrow in Figure 1a). Subsequently, with the switches open, the inductor maintains a consistent current flow direction, and the discharge path of the inductor is redirected by the pair of diodes to the terminals of the battery pack (as indicated by the green arrow in Figure 1b). Consequently, energy is transferred from an individual cell to the entire battery pack. Notably, this balancing procedure operates independently for each cell, enabling the simultaneous discharge of multiple cells. This topology operates independently of the cell voltage level. As long as a cell can charge the inductor and the cell's voltage does not fall below its minimum operating voltage, the balancing current can be maintained at a desired RMS value.

In low-voltage battery packs, the pair of switches can be implemented by N -channel MOSFETs and a low forward-voltage Schottky diode to maximize efficiency. A schematic of the implementation is shown in Figure 2. In a typical low-voltage battery pack, such as a series-connected 10-cell NiMH battery pack (12 V) or a three- to four-cell series-connected lithium battery pack (typically 12.6 V to 14.8 V), a low-side driver with a maximum output voltage range of 20 V to 25 V can activate the high-side switch. This configuration provides a gate-source voltage between 5 to 10 volts, which is sufficient for MOSFETs that operate at

a 4.5 V gate-source voltage. The switches are open when the driver output voltage (gate-ground voltage) is changed to zero. Consequently, both the gate-source and drain-source voltages for the lower MOSFET will not drop below the negative pack voltage, which remains significantly lower than the maximum rating. Simultaneously, the source voltage of the upper MOSFET falls to around -0.5 V due to the discharge current path through the Schottky diodes. With a gate voltage of approximately 0.5 V, the MOSFET remains inactive.

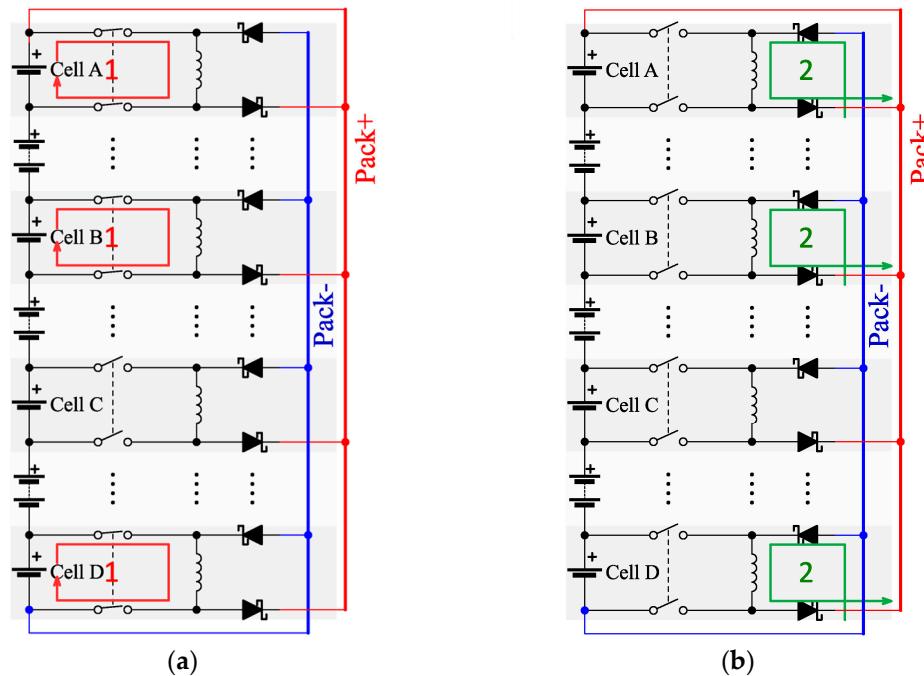


Figure 1. Proposed active balancing topology. Cells *A*, *B* and *D* are being balanced, while Cell *C* is within the balancing threshold and is not being balanced. *Pack+* represents the positive terminal of the pack. *Pack-* represents the negative terminal of the pack. (a) *Path 1* represents the cells charging the inductors. (b) *Path 2* represents the inductors releasing energy to the battery pack.

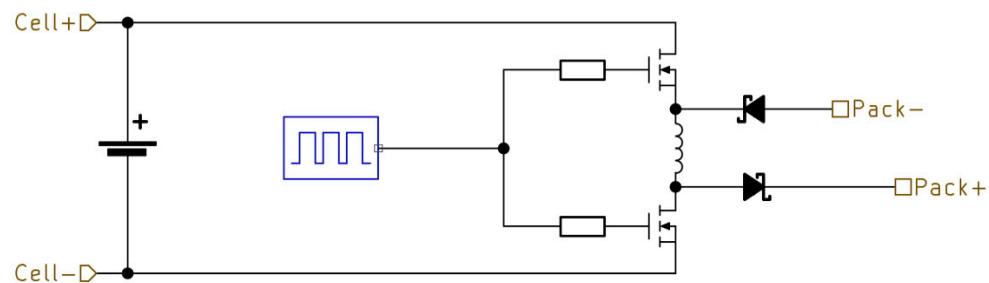


Figure 2. Implementation for low voltage cells.

Figure 3 illustrates the necessary modifications to adapt the topology for higher-voltage battery packs. Typically, commercial BMS front ends support 6–16 series-connected lithium cells with voltages ranging from 25.2 V to 67.2 V. This results in pack voltages that exceed the typical maximum operating range of low-side gate drivers, causing multiple cells to have voltage levels higher than the gate drivers' power supply.

In Figure 2, the upper switch's high side and the bottom switch's low side are connected to the positive and negative terminals of the corresponding cell, thereby providing a relatively steady voltage level reference to the negative terminal of the pack. To eliminate the floating source of the MOSFET, *P*-channel MOSFETs, and *N*-channel MOSFETs are used as replacements for the switches in Figure 3. A dual-channel low-side driver drives the complementary pair of MOSFETs with one inverting output through a bootstrap circuit.

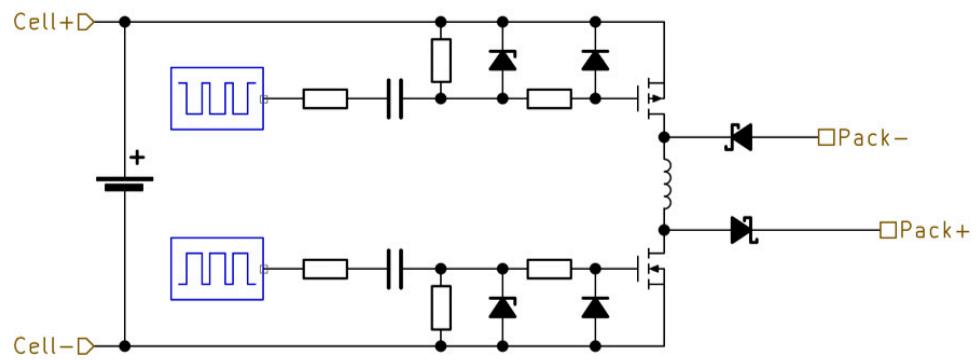


Figure 3. Implementation for higher voltage cells.

This configuration guarantees synchronous switching on and off simultaneously. Gate resistors R_g are placed in series on both sides of the bootstrap capacitor to limit peak current in the driving circuit and inrush current via the bootstrap diode during transient states when connecting the balancer to the cells. Additionally, optional Zener or TVS diodes with operating voltage between gate-driving and maximum gate-source voltage provide extra protection by capping the gate-source voltage within the maximum rating. The gate-source resistor pulls the gate-source voltage to zero when the driver IC with a push-pull output shuts down, enhancing safety and robustness in a noisy environment.

In summary, the proposed balancing topology is insensitive to the cells operating voltage range. Its performance is constrained primarily by the voltage ratings of the selected components rather than by any inherent topology limitations. In very low-voltage cells (provided the cell voltage remains above zero), the inductor can still store and transfer energy effectively. Conversely, in high-voltage cells, one can simply replace the Schottky diodes and MOSFETs with high-voltage-rated components to maintain functionality.

3. Control Signal Generation and Efficiency Analysis

This section describes the PWM control signal generation and analyses energy transfer efficiency to assist in selecting suitable operating parameters for the implementation of the proposed balancing topology. The efficiency calculation does not consider eddy current losses in the inductor and copper plane below it, MOSFET reverse recovery, diode recovery, or energy consumed by the driving circuit. All symbols are listed in Table 2.

Table 2. Nomenclature.

Symbol	Unit	Description
t_1	s	Interval when signal pulse is set to high
t_2	s	Interval when inductor is discharging
t_3	s	Deadtime
R_P	Ω	Resistance of P-channel MOSFET fully on
R_N	Ω	Resistance of N-channel MOSFET fully on
R_L	Ω	Inductor resistance
R	Ω	Sum of R_p , R_N and R_L
L	H	Inductor inductance
n	-	Number of cells
V	V	Cell voltage
V_p	V	Pack voltage
V_f	V	Diode forward voltage drop
I_L	A	Inductor current

Table 2. Cont.

Symbol	Unit	Description
I_{peak}	A	Inductor peak current
I_{Cavg}	A	Average cell current during balancing
I_{Davg}	A	Average diode current during balancing
E_L	J	Energy stored in inductor
E_{Rloss}	J	Energy loss due to series resistance
E_{Dloss}	J	Energy loss due to diode forward voltage

PWM Signal Generation

In Figure 4, t_1 represents the interval when the control signal pulse is high. During this time, the MOSFET pairs are turned on, allowing the cell to charge the inductor. t_2 represents the interval during which the MOSFETs are switched off, enabling the inductor to release energy to the pack via the pair of diodes. t_3 represents the dead time before the next cycle, allowing for diode reverse recovery and extra time to prevent continuous current flow through the inductor due to electromagnetic interference or propagation delay on gate drivers.

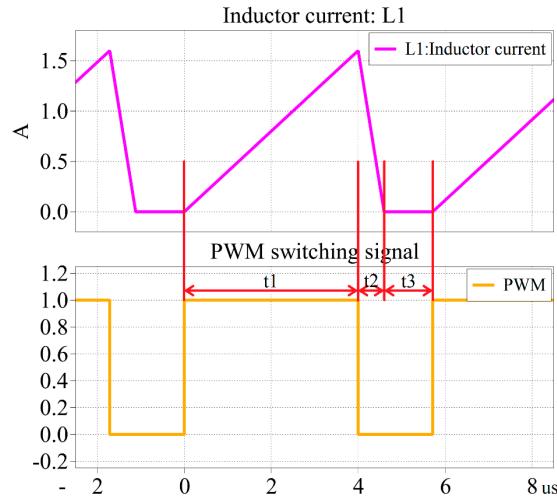


Figure 4. Simulated inductor current (A) and PWM signal vs. time (μ s).

The peak current through the inductor I_{peak} can be expressed as (1), where R is the sum of the series resistance of the P-channel MOSFET R_P , the N-channel MOSFET R_N and the inductor R_L ; V is the cell voltage, and L is the inductor inductance,

$$I_{peak} = \frac{V}{R} - \frac{V}{R} \times e^{-\frac{R}{L} \cdot t_1} \quad (1)$$

For the desired peak current through the inductor, the duration of t_1 is obtained from (1) as (2),

$$t_1 = -\frac{\ln\left(-\frac{I_{peak}R-V}{V}\right)L}{R} \quad (2)$$

Note: Since $t_1 \ll L/R$ in Figure 4, (1) and (2) could be simplified as $I_{peak} = \frac{V}{L}t_1$ and $t_1 = \frac{I_{peak}L}{V}$, respectively.

The energy stored in the inductor is given by (3),

$$E_L = \frac{1}{2} I_{peak}^2 L \quad (3)$$

and it is equal to the energy transfer during discharging, given by (4),

$$E_L = \int_0^{t_2} (V_P + V_f) \cdot \left(-\frac{I_{peak}}{t_2} \cdot t + I_{peak} \right) dt \quad (4)$$

Solving (3) and (4), the interval t_2 can be found as (5),

$$t_2 = \frac{I_{peak} L}{V_P + V_f} \quad (5)$$

The series resistance loss R_{loss} while the cell is charging the inductor during one cycle is given by (6),

$$E_{R_{loss}} = \int_0^{t_1} \left(\frac{V}{R} - \frac{V}{R} \times e^{-\frac{R}{L} \cdot t_1} \right)^2 R dt \quad (6)$$

The diode loss D_{loss} while the inductor is releasing energy to pack during one cycle is given by (7),

$$E_{D_{loss}} = \int_0^{t_2} 2V_f \cdot \left(I_{Peak} - \frac{I_{peak}}{t_2} \cdot t \right) dt \quad (7)$$

The efficiency of the cell-to-pack energy transfer can be estimated by (8), and after substituting (2) and (5), the simplified expression (9) can be obtained,

$$\begin{aligned} \text{Efficiency} &= \frac{E_L - E_{D_{loss}}}{E_{R_{loss}} + E_L} \times 100\% \\ &= \frac{\frac{1}{2} I_{peak}^2 L - \int_0^{t_2} 2V_f \cdot \left(I_{Peak} - \frac{I_{peak}}{t_2} \cdot t \right) dt}{\int_0^{t_1} \left(\frac{V}{R} - \frac{V}{R} \times e^{-\frac{R}{L} \cdot t_1} \right)^2 R dt + \frac{1}{2} I_{peak}^2 L} \times 100\% \end{aligned} \quad (8)$$

$$= \frac{I_{peak}^2 (-V_p + V_f) R^2}{2(V_p + V_f) V \left(I_{peak} R + \ln \left(\frac{-I_{peak} R + V}{V} \right) V \right)} \times 100\% \quad (9)$$

Assuming $V_p = n \cdot V$ and using parameters from the datasheets of the components in Table 3 as an example, (9) can be simplified as (10),

$$= \frac{0.0008405 (V \cdot n - 0.4) I_{peak}^2}{(0.041 I_{peak} + \ln \left(\frac{-0.041 I_{peak} + V}{V} \right) V) V (V \cdot n + 0.4)} \times 100\% \quad (10)$$

Table 3. Components parameters for efficiency estimation example.

	Condition	Typical
V_f	$I_{avg} = 3A, 25^\circ C$	0.4 V
R_P	$V_{GS} = -10 V$	<16.5 mΩ
R_N	$V_{GS} = +10 V$	<9.5 mΩ
R_L	-	15 mΩ
R	-	0.041 Ω

Figure 5 illustrates the efficiency of the balancing circuit. The vertical axis of the 3D graph represents the efficiency; the horizontal axes show the inductor's peak current and the cell's voltage. It displays six layers from bottom to top, illustrating the relationship between the pack voltage and balancing efficiency with the number of cells varying from 4 to 9.

The trend indicates that increasing the number of cells, and consequently the pack voltage, results in higher balancing efficiency.

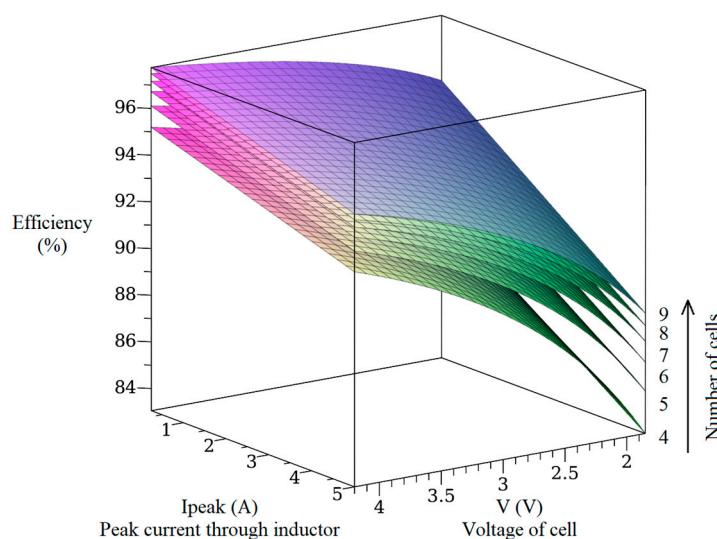


Figure 5. Efficiency analysis for various cell voltages, number of cells in a pack, and peak balancing current.

4. Experimental Setup and Test Results

4.1. Components Selection Guide and Application Note

4.1.1. MOSFET Selection

Based on the operating principle of the proposed balancer, the maximum MOSFET voltage stress occurs at the top cell's high side and the bottom cell's low side; hence, selecting MOSFETs with voltage ratings slightly higher than the maximum pack voltage suffices.

In the simplified driving circuit for low-voltage cells (Figure 2), the gate voltage rating is more critical than the pack voltage. This is because the maximum pack voltage is limited by the difference between the maximum voltage of the gate and its driver. MOSFETs typically turn on at around 4.5 V, so selecting components with voltage ratings of 12 V and 25 V establishes pack voltage limits of 7.5 V and 20.5 V, respectively.

For driving circuits designed for higher cell voltages and a wider cell voltage range (Figure 2), conventional MOSFETs with a maximum gate-source rating between $\pm 15\text{--}\pm 20$ V are sufficient for driving ICs operating at a typical voltage of 12 V.

4.1.2. Driver IC Selection

The selection of gate drivers is critical to minimize additional energy loss outside of the balancing circuitry. A dual-channel low-side driver should be considered during the design phase. Such a driver ensures consistent internal propagation delay, hysteresis, and synchronous output while drawing less current than two standalone single-channel drivers. A pulse output current capability higher than 1 A is sufficient to rapidly turn on small MOSFETs for balancing applications.

4.1.3. Inductor Selection

The selection of inductors for the proposed topology prioritizes size, balancing speed, and efficiency. Equation (10) confirms that with a fixed value of series resistance, efficiency remains independent of inductance. However, (5) and (6) reveal that for a consistent peak current through the inductor, a lower inductance leads to a shorter cycle period, resulting in a higher average cell discharging current and improved balancing speed.

Consequently, after calculating the inductance value based on the desired balancing speed, inductors with low series resistance and fully shielded designs within physical size constraints are recommended. Furthermore, when employing non-shielded inductors, it is

pertinent to note that wide copper tracks or planes beneath the surface-mounted inductor may induce eddy current loss and elevate the current through the inductor.

4.1.4. Diode Selection

Assuming $t_1 \ll L/R$, the average cell current during balancing (the average value of the inductor current) I_{Cavg} is given by (11),

$$I_{Cavg} = \frac{1}{2} \cdot I_{peak} \cdot D \quad (11)$$

The voltage rating of the Schottky should be slightly higher than the pack voltage, and the average current through the diode I_{Davg} at the PWM duty cycle D when the inductor releases energy to the pack is given by (12),

$$I_{Davg} = I_{Cavg} \cdot \frac{V}{V_p} \approx I_{Cavg} \cdot \frac{1}{n} \approx \frac{1}{2n} \cdot D \cdot I_{peak} \quad (12)$$

Since I_{Davg} is significantly lower than I_{Cavg} , the required current rating of Schottky diodes is significantly lower than I_{peak} , which is beneficial for cost reduction.

4.2. Experiment Setup

To validate the proposed balancing topology and its low-cost driving circuit, a series of experiments were conducted. The experimental setup, shown in Figure 6, consists of a five-cell series-connected battery pack, a five-cell balancer board with the gate driving circuit shown in Figure 3, and a controller board for cell voltage measurement, PWM generation, and data logging. Additionally, power supplies for the gate driving circuits and a bi-directional power supply were directly connected to the terminals of the pack for balancing tests during both charging and discharging. Table 4 lists the values of the components used for the balancer board in Figure 6.

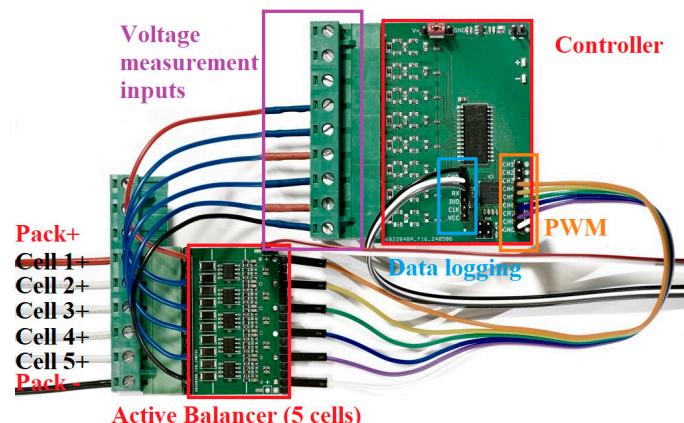


Figure 6. Balancing setup.

Table 4. Components specification and design considerations for the proposed balancer board.

	Component	Value	Number	1st Consideration	2nd Consideration
Cells	Li-ion	INR18650-25R	5	N/A	N/A
Analog front-end	Multiplexer	MUX507	1	N/A	N/A
	Op-amp	INA826	1	N/A	N/A
Controller	Microcontroller	STM32G0 series	1	ADC resolution	Cost

Table 4. Cont.

	Component	Value	Number	1st Consideration	2nd Consideration
Driving circuit	Dual-output Driver	UCC21525	1 *	Cost	N/A
	Capacitor (boot)	1 μ F, 25 V	2 *	Cost	Voltage rating
	Resistor (gate)	2.2 Ω	2 * or 4 **	Cost	Gate current
	Resistor (gate-source)	300 k Ω	2 *	Cost	N/A
	Diode	1N4148	2 *	Cost	Recovery time
	Zener Diode (Optional)	15 V	2 *	Cost	Voltage rating
Balancing circuit	Power Inductor	10 uH	1 *	Current rating	Switching time
	MOSFET Pair	AO4614B	1 *	Voltage rating	Current rating
	Schottky Diode	PMEG4030ER	2 *	Voltage rating	Current rating

* Per cell. ** R_g connected to the driver output and C_{boot} is optional.

4.3. Balancing Circuit Verification

To verify that the topology and the driving circuit are functioning as expected, the five-cell series-connected pack was charged to 20.532 V, with the top cell at 4.2062 V and its negative terminal referenced to the Pack— at 16.327V. The power supply for the gate driving circuit is 11.25 V, referenced to Pack—. In this case, both the positive and negative terminals of the top cell have higher voltages than the supply voltage of the gate drivers.

In Figure 7, Channel 4 shows the 3.3 V, 175 kHz PWM control signal with a duty ratio of 70%, which feeds to the gate driver input and is used as the trigger of the source. Channel 1 and Channel 2 display the DC-coupled gate voltages of the P-channel MOSFET and N-channel MOSFET, respectively, for the top cell referenced to the Pack-(GND). Channel 3 shows the DC-coupled current through the inductor during balancing. (Two wires are attached to the inductor and then soldered to the PCB for inductor current measurement.)

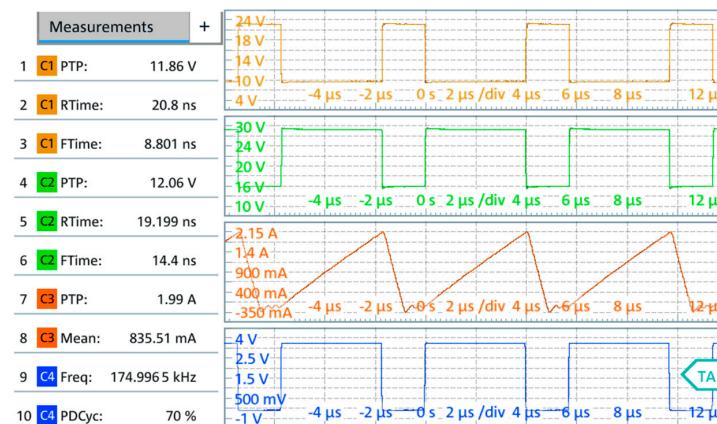


Figure 7. Experimental measurements (oscilloscope). Ch1: DC coupled gate voltage of P-channel MOSFET. Ch2: DC coupled gate voltage of N-channel MOSFET. Ch3: DC coupled inductor current Ch4: PWM control signal, trigger source.

Oscilloscope measurements show that the peak-to-peak voltage of the P-channel MOSFET is 11.86 V, with an 8.801 ns fall time and 20.8 ns rise time; the peak-to-peak voltage of the N-channel MOSFET is 12.06 V, with a 19.199 ns rise time and 14.4 ns fall time. The measured results validate that the proposed circuit can adequately drive the pair of complementary MOSFETs on the high side. The gate-source voltages of both MOSFETs are kept over 10 V for the entire on-time when using an 11.25 V (measured) non-isolated power supply. The rise and fall times of the gate voltage are short enough to avoid significant switching loss.

The current waveform in Channel 3 shows that when the control signal in Channel 4 rises to high, and the MOSFETs are turned on, the inductor is charged by the cell (between 0 to 4 μ s), then releases energy back to the pack when the control signal drops too low,

and the MOSFETs turn off (between 4 to 4.9 μ s). The current ripple between 4.9 to 5.7 μ s represents the diode reverse recovery and oscillation of parasitic components before the next cycle begins. The measured result matches the simulation result shown in Figure 4. The slight difference in peak current through the inductor is caused by the difference in cell voltage between the simulation and the actual test, as well as the tolerance of the inductor. The additional dead time (t_3) mentioned in Figure 4, inserted before the next pulse of PWM, may vary for each specific battery pack and can be finalized during this stage.

4.4. Control Algorithm

The control algorithm for the proposed active balancer is voltage-based and designed to ensure efficient and balanced energy distribution among cells in a battery pack.

As outlined in the flowchart Figure 8a, the battery cell balancing process begins with the system's initialization and calibration. Then, the system scans the voltages of all battery cells to identify any variations. If the variation does not exceed the threshold initially, the system takes no action and waits before repeating the voltage scan. If the voltage variation exceeds a pre-defined threshold, the system configures the Pulse Width Modulation (PWM) timer based on the cell voltages. This allows the balancing process to adapt to the specific conditions of the cells, whether it involves a single cell or multiple cells requiring balancing. Once configured, the balancing process starts and continues for a specified duration, during which the system waits to allow the cells with higher voltages to be discharged and transfer the energy to the pack to equalize. The balancing process could be performed cell-by-cell or on multiple cells simultaneously. After the waiting period, the balancing is stopped, and a relaxation phase follows to account for any transient effects for more accurate measurements of the next scan. This iterative process ensures that balancing is achieved efficiently across either individual or multiple cells as needed.

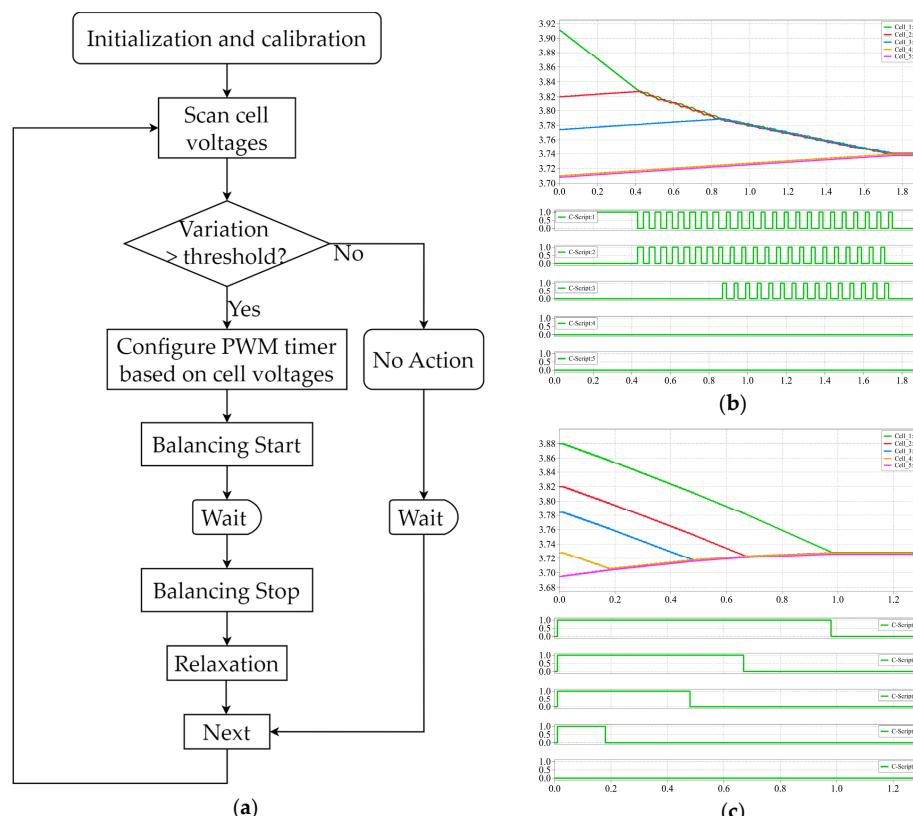


Figure 8. (a) Workflow of cell balancing algorithm; (b) cell voltages and balancing status vs. time for balancing cell-by-cell (simulation results); (c) cell voltages and balancing status vs. time for balancing multiple cells (simulation results).

Figure 8b illustrates the cell voltages (top plot) and the balancing status of each cell (bottom plot) during the simulation of balancing a single cell. As depicted in the bottom plot, only the cell with the highest voltage, which exceeds the balancing threshold, is discharged, releasing energy back to the battery pack. Figure 8c presents the cell voltages (top plot) and the balancing status of each cell (bottom plot) during the simulation of balancing multiple cells. As shown in the bottom plot, all cells whose voltages exceed the balancing threshold are discharged simultaneously, releasing energy to the battery pack.

4.5. Experimental Results

The experiment results presented in Figures 9–12 demonstrate the effectiveness of battery cell balancing under various operating conditions.

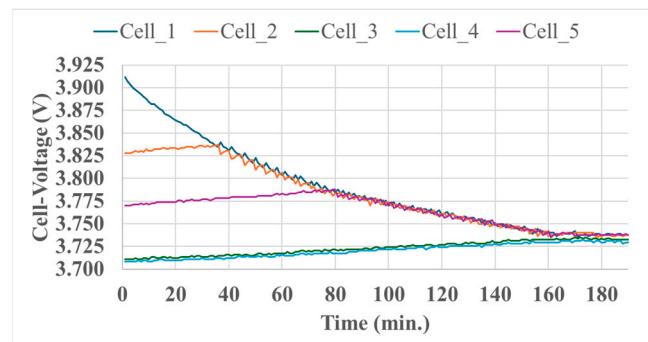


Figure 9. Experimental results illustrating cell voltages vs. time (balancing cell-by-cell, 170 min are required to reduce the cells' voltages difference to below a threshold of 10 mV).

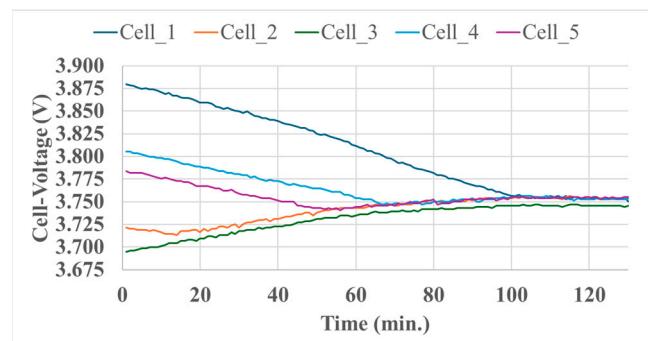


Figure 10. Experimental results illustrating cell voltages vs. time (balancing multiple cells, 100 min are required to reduce the cell voltage difference to below a threshold of 10 mV).

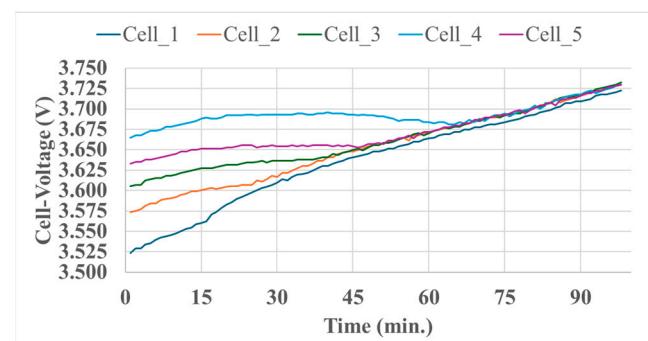


Figure 11. Experimental results illustrating cell voltage vs. time (balancing multiple cells while charging, 67 min are required to reduce the cell voltage difference to below a threshold of 10 mV).

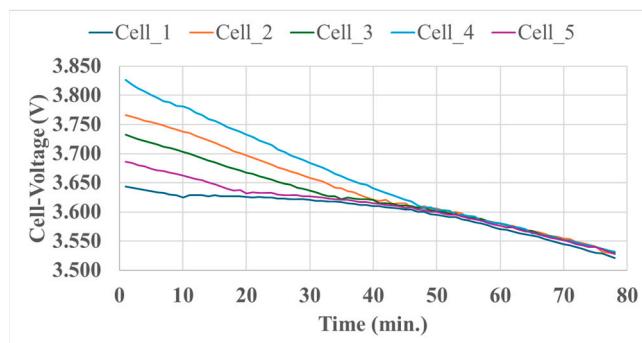


Figure 12. Experimental results illustrating cell voltage vs. time (balancing multiple cells while discharging, 47 min are required to reduce the cell voltage difference to below a threshold of 10 mV).

In Figure 9, the cell voltage variation over time during the cell-by-cell balancing is shown. In this test, only the cell with the highest cell voltage is discharged and releases the energy to the pack. Initially, cell 1 had a significantly higher voltage than the other cells. As the balancing process progresses, the voltage of cell 1 decreases steadily while the other cells are being charged until its voltage converges with the voltage of cell 2. Now, cells 1 and 2 are the cells with the highest voltage, and subsequently, they are being alternatively discharged one after the other until their voltages converge to the voltage of cell 5. By the end of the process, all cell voltages converge to the same voltage within the balancing threshold. The steady increase in cell voltages indicates that the balancing process does not discharge the cells but rather evenly charges them.

Cells 3 and 4 have the lowest voltage initially, and since their voltage variation remains within the balancing threshold, they are only being charged during the whole balancing process. This proves that the balancer does not introduce additional imbalance within the pack.

Figure 10 illustrates the result for multiple cell balancing. Except for cell 3, which has the lowest cell voltage at the beginning of the test, all other cells (1, 2, 4, and 5) are being discharged and release energy to the pack until their voltages are within the balancing threshold. By the end of the process, all cell voltages converge, indicating successful multicell balancing. This test also demonstrates the system's capability to balance multiple cells simultaneously, thereby ensuring a faster and more uniform voltage distribution throughout the battery pack.

Figure 11 shows the result of balancing multiple cells during the charging process. The imbalanced pack is charged with an external power supply during the test. Balancing is not enabled for the first 15 minutes, and significant cell voltage differences remain while charging. Once the balancing is started, the voltage increases of cells with higher voltages become slower as they are being discharged by the balancer, and the cells with lower voltages are being charged faster. In this case, the system is not only balancing the cells but also compensating for the cell voltage increases due to charging. Despite the overall rise in the cell voltage, the voltages gradually converge, demonstrating the system's ability to perform cell balancing in a dynamic charging condition.

Additionally, Figure 12 presents the balancing result while discharging. Similar to the previous experiments, the system equalizes the voltages of cells while the battery pack is connected to a discharging load. This showcases the system's robustness in maintaining balanced cell voltages under both charging and discharging scenarios.

5. Conclusions

This paper reviewed various existing solutions for active balancing and proposed a novel, inductor-based, cell-to-pack active balancing topology capable of operating across a

wide range of cell voltages. Compared to conventional balancers, this topology integrates the necessary driving circuits, thus reducing overall system costs by eliminating the need for costly isolated power modules or high-side gate drivers while maintaining a simpler control structure. The proposed system efficiently transfers energy from individual cells to the battery pack, enabling multicell balancing with a balancing current that remains unaffected by the level of imbalance. Furthermore, it employs a straightforward control algorithm, simplifying implementation. The system's effectiveness is confirmed by the experimental results, which demonstrate the convergence of cell voltage during both charging and discharging operations.

Future work will focus on adapting the circuit design for series-connected pack-level balancing. Additionally, a simple and cost-effective controller will be developed to ensure continuous conduction mode (CCM) operation in higher-voltage applications, thereby increasing average balancing power. Experimental validation will be extended to larger battery modules and real-world applications, such as PV energy storage systems, to evaluate scalability and long-term reliability.

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