Task 1

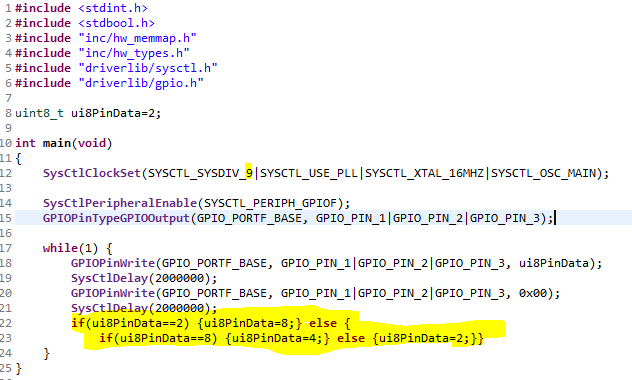
The clock is specified at 400MHz with a default division by 2, and a specified division by 5 resulting in 40MHz. Then, including the additional division of 5 specified in the code,



To change the delay to 0.425sec,

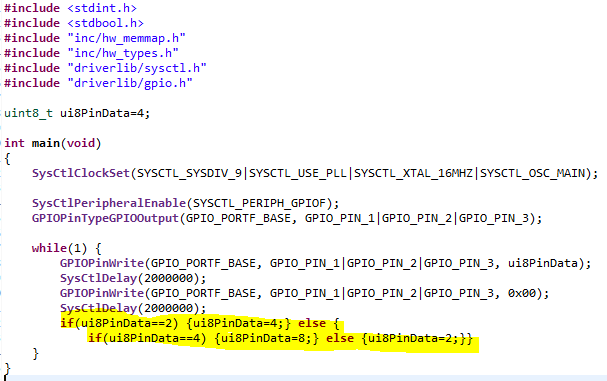


Please note that the sequence described in the lab does not match the sequence set forth by the given code, so the code was altered to match what is asked for in the lab: 2, 8, 4.



Task 2

To change the sequence from RGB to BGR, the number sequence needs to switch from 2,8,4 to 4,8,2



Then, to implement the described sequence: R, G, B, RG, RB, GB, RGB, R, G, ... requires the number sequence: 2, 8, 4, 10, 6, 12, 14, 2, ...

