Function			Stage Gate	
Project Management	☐		Open	☒
Marketing Launch	☐		Select	☐
Design & Test	☒	**AM64 BRICK**	Do	☐
Industrialization Manufacturing	☐	**Electronic design**	Implement	☐
Purchasing	☐		Produce	☐
Logistics	☐		Sell	☐
Quality	☐		Close	☐

Document status	Draft ☒	In Review ☐	Official ☐

Revision History				
00	2022-04-12	JPK	☐ xxx ☐ xxx ☐ xxx ☐ xxx	Refer to Detailed historic of the document.
01	2023-24-03	THA	☐ xxx ☐ xxx ☐ xxx ☐ xxx	Restarted for BRICK (GEX95646)
02	2023-27-03	THA/ABI	☐ xxx ☐ xxx ☐ xxx ☐ xxx	Remove old TPM history
03	2023-22-05	THA		Add informations on PCIe boot mode
04	2023-04-08	THA/ABI		Add LPDDR4 informations
05	2023-09-06	THA		Updates on supported devices
Rev.	**Date** (yyyy-mm-dd)	**Author(s)**	**Approver(s)**	**Comments**

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1 GENERALITY ABOUT THE DOCUMENT

1.1 Purpose of the document

Explain the technical choices of the brick design.
All available interfaces are not necessary fully implemented into the brick (PCIe or USB or RGMII for instance), they are implemented outside the brick, in this case the keyword “outside” the brick is used to ease its search.

1.2 Detailed historic of the document

Rev.	**Date** (yyyy-mm-dd)	**Author**	**File name**	**Section or chapter**	**Modification**
00	2022-04-12	JPK			Creation
01	2022-10-04	THA			Started new version due to New AETHENA and new brick projects
02	2023-27-03	ABI/THA		all	Upgrade/update almost all chapters
03	2023-22-05	THA			Add informations on PCIe boot mode
04	2023-04-08	THA/ABI			Add LPDDR4 informations VMON_VSYS computing formula V_3V3IO decoupling PMIC powersequence precision NAND flash update Crystal computation formula
05	2023-09-06	THA			Updates on supported devices: CPU NAND NOR LPDDR4 TPM

1.3 Diffusion list

Date (yyyy-mm-dd)	**Name**	**Function**	**Site**
201X-XX-XX			

1.4 List of reference documents

ID	**Document Reference**	**File name**	**Writer**
REF1	AM64x_243x Technical Reference Manual	spruim2f_AM64x_243x Technical Reference Manual.pdf	T.I.
REF2	AM6442 Datasheet	sprsp56e_Datasheet am6442 Sept 2022 revE.pdf	T.I.
REF3	AM64x_Power_Estimation_Tool_Worst UseCase.xlsm	AM64x_Power_Estimation_Tool_WorstUseCase.xlsm	VVE
REF4	AM64x_Power_Estimation_Tool_Typica lUseCase.xlsm	AM64x_Power_Estimation_Tool_TypicalUseCase.xls m	VVE
REF5	TPS65220xx PMIC Datasheet	slvsgy1_TPS65220_Datasheet.pdf	T.I.
REF6	Schematic Checklist	spracu5b_AM64x_AM243x Schematic Checklist.pdf	T.I.

REF7	TPS6522053 PMIC Technical Reference Manual	slvucj3_TPS6522053_TRM.pdf	T.I.
REF8	AM64x & AM24x Board Design Guidelines	spracu1a_AM64x_AM243x DDR Board Design and Layout Guidelines.pdf _AM64x_AM243x DDR Board Design and Layout Guidelines.pdf	T.I.
REF9	ST33HTPH2X32AHD8 Datasheet	ST33HTPH2X32AHD8_DS_ST33TPHF2XSPI_Rev-7.pdf	S.T.
REF10	TPS22965 Datasheet	Texas Instruments_TPS22965_data sheet_RevF_Aug2016.pdf	T.I.
REF11	PCIE Card ElectroMechanical standard rev4 Version 1.0	PCIe_CEM_SPEC_R4_V1_0_08072019_NCB.pdf	PCI SIG
REF12	High speed Layout Guidelines for USB	Ti High-Speed Layout Guidelines for Signal Conditioners and USB Husbs slla414.pdf	T.I.
REF13	USB3.1 r1.0 standard	USB_3_1_r1.0.pdf	USB.org
REF14	USB3.1 Engineering Change Notice AC Coupling capacitor	USB 3.1 ECN Rx AC Coupling Capacitor Option.pdf	USB.org
REF15	High-Speed Interface Layout Guidelines.pdf	spraar7j_High-Speed Interface Layout Guidelines.pdf	T.I.
REF16	I^2C-bus specification and user manual	UM10204 rev7_2021.pdf	NXP
REF17	Pinmux	AM64xx-usecases_functions_pinmux_v006.xlsx	=S=
REF18	PCI Express Base Specification rev4.0 Version 1.0	NCB-PCI_Express_Base_4.0r1.0_September-27-2017-c.pdf	PCI SIG
REF19	Mission Profile - AM64xx Brick.pptx	Mission Profile - AM64xx Brick.pptx	Mission Profile

1.5 Glossary

Acronym	Meaning
CSM/PDM	Schneider part database
MSPS	Mega Samples Per Second
PDN	Power Decoupling Network
POR	Power-On Reset
PU/PD	Pull Up /Pull Down
SPN	Schneider Part Number
TBC	To Be Confirmed / To Be Completed

1.6 Writing convention

Writing convention for naming signals for the BRICK is:
Always using the entire name from the provider and adding "**_N**" when it is active at the low voltage state.

This allows finding signals into schematics and datasheets using copy/paste, the more easily.
This changes sometimes or add several times the same indication, due to non-constant naming from providers

- Some providers are adding a "n" before the signal NAME: **nNAME**
- TI is sometime adding a n or sometime adding a z at the end of the signal NAME to indicate its low-level active state (**NAMEz**)

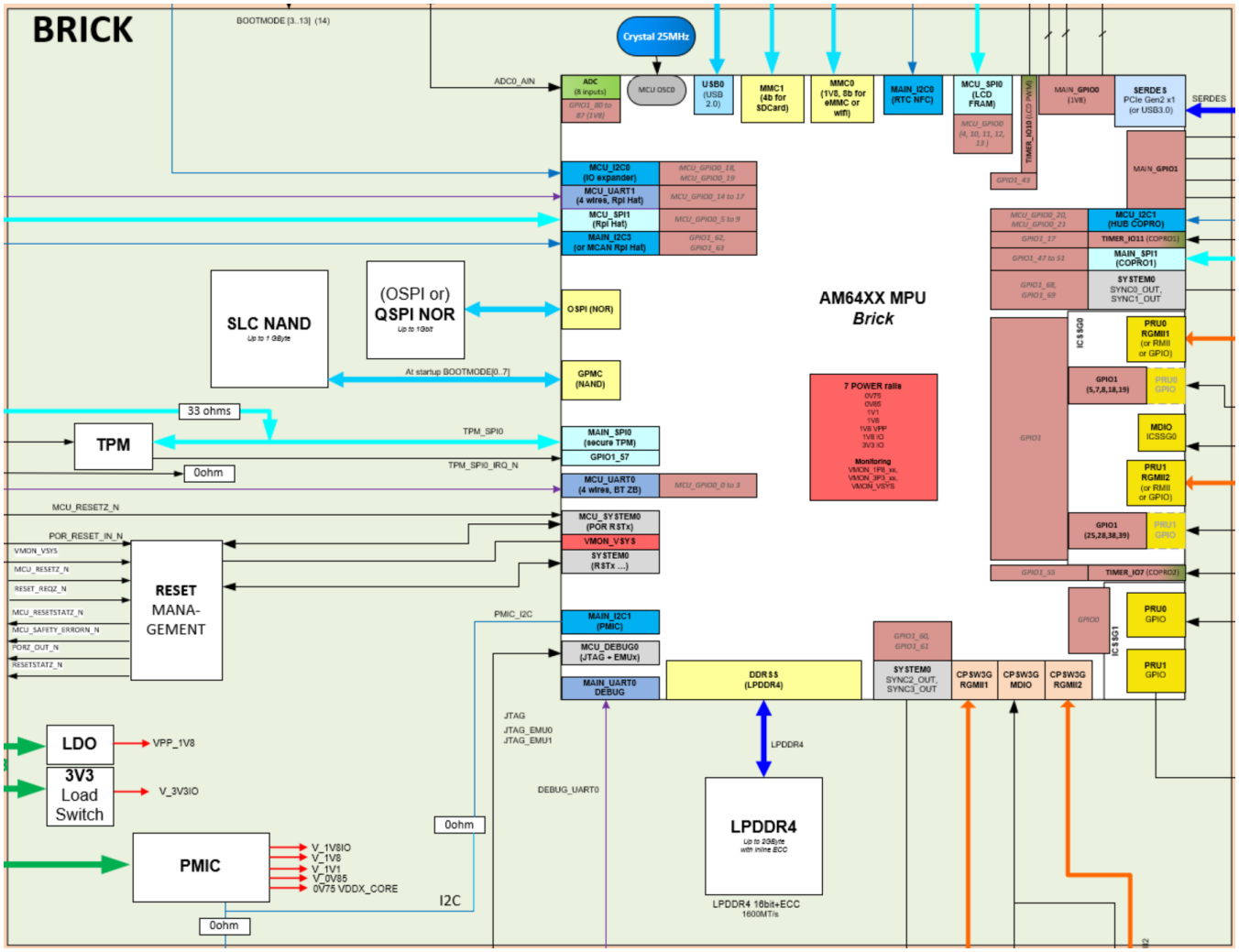
As a result, our signal on the BRICK could be finally named: **nNAMEz_N** (in the worst case).

2 ARCHITECTURE OVERVIEW

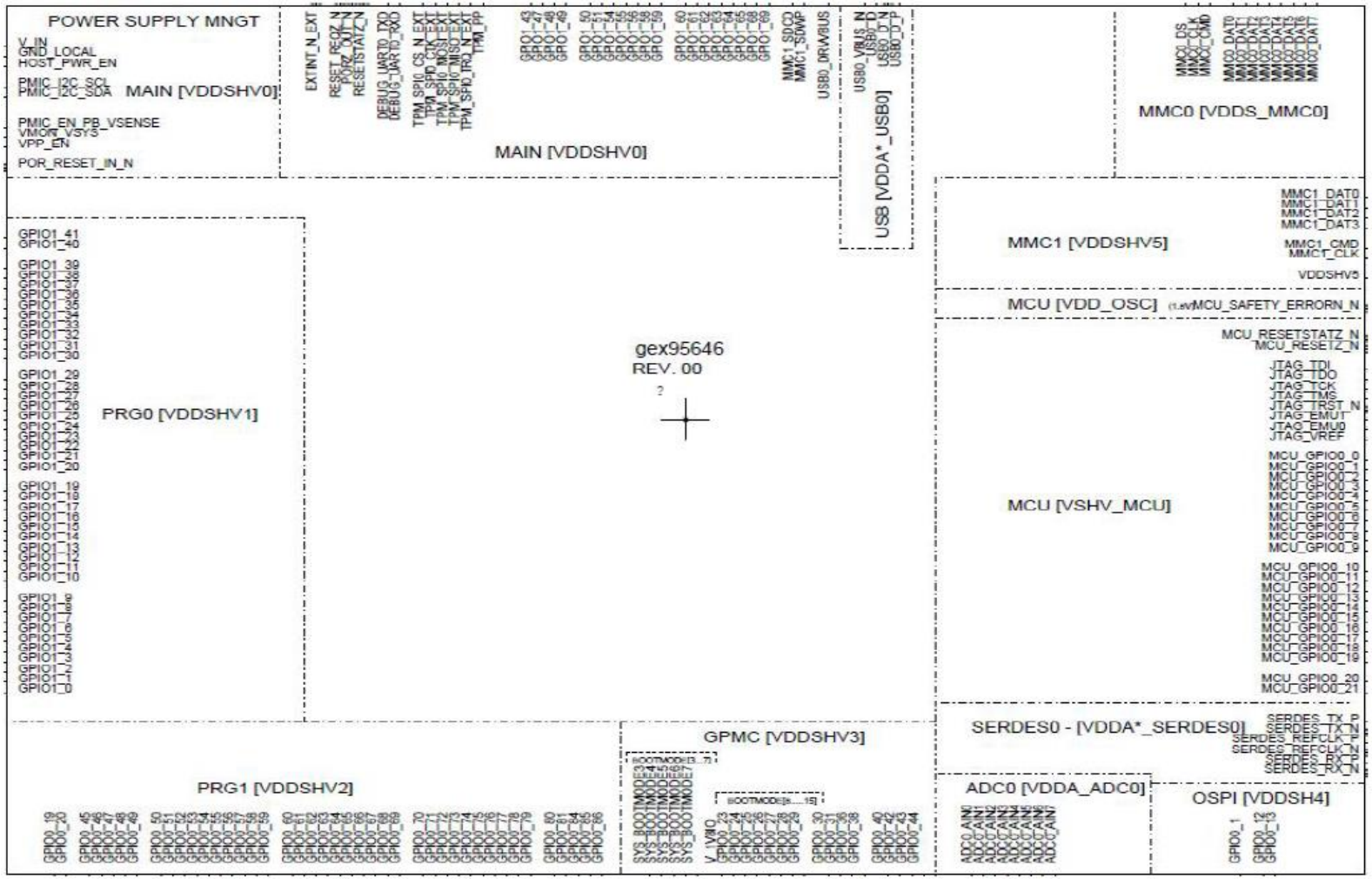
2.1 Architectural View

The AM64 macrocomponent integrate the set of common core components needed by any host project which wants to use the AM64 SoC:

- AM64
- LPDDR4 SDRAM Memory
- QSPI / OSPI NOR Flash Memory
- NAND Flash Memory
- Crystal
- Power Management (DC/DC converters, Power sequencer and voltage supervisor)
- Power Bypass capacitors

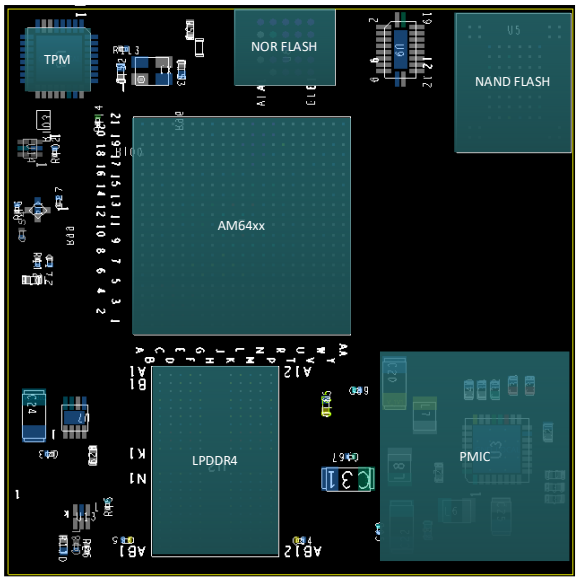


2.2 Schematic Symbol View

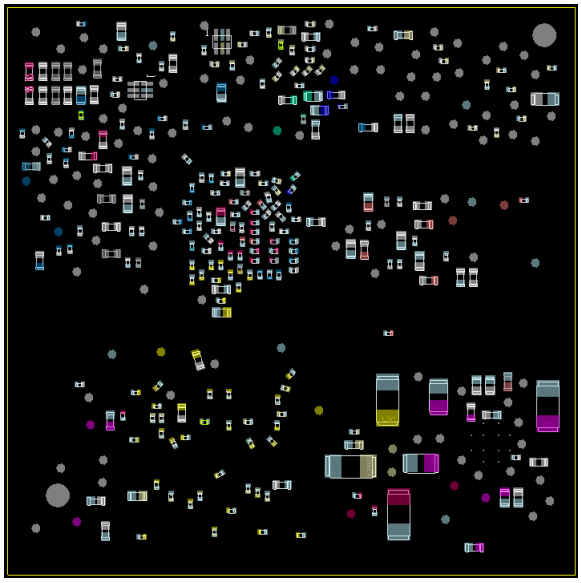


2.3 PCB View

2.3.1 Top view



2.3.2 Bottom view



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Created by Author

3 EXTERNAL SPECIFICATIONS

3.1.1 Dimensions

~45mm x 45mm
Stackup 10 layers
Min size component 0201

3.1.2 Mission profile

In short, the Brick is designed to stand -40° / +70°C ambient temperature range during some time but you will find the details in the following file: REF19

3.1.2.1 AM64 Temperature range

SUPPLY NAME	DESCRIPTION		MIN(1)	NOM	MAX(1)	UNIT
T_J	Operating junction temperature range	Extended	-40		105	°C

3.1.2.2 PMIC Temperature range

POS			MIN	NOM	MAX	UNIT
3.3.1	$T_{A_}$	Operating free-air temperature	–40		125	°C
3.3.2	$T_{J_}$	Operating junction temperature	–40		150	°C

3.1.2.3 Other components

All other component fit requirement of -40°C < T_{amb} < 105°C.

3.1.3 Power supply

According to 4.1.1.1 Power Input Voltage Vin= 3V3 ± 2% input voltage

Important Note: The internal power planes are NOT intended to be used outside the brick. Doing so, the behavior of the electronics cannot be guaranteed, and the whole simulation analysis has to be redone.

3.1.4 I/O features

Basically, the AM64 brick provide following interfaces:

- 2 x RGMII (CPSW3G)
- 2 x RGMII (ICSSG0 PRUs)
- 1 x MII (coming from?) usable for T1S
- 1 SERDES TX + 1 SERDES RX (PCIe or USB3.1)
- USB2.0 OTG
- SDCard
- EMMC support
- 1 x SPI TPM
- 8 ADC inputs
- 1 DEBUG UART
- 1 JTAG+ EMU0/1
- Many SPI / I2C / UART & GPIO LVCMOS3.3 (a few LCVMOS1.8)

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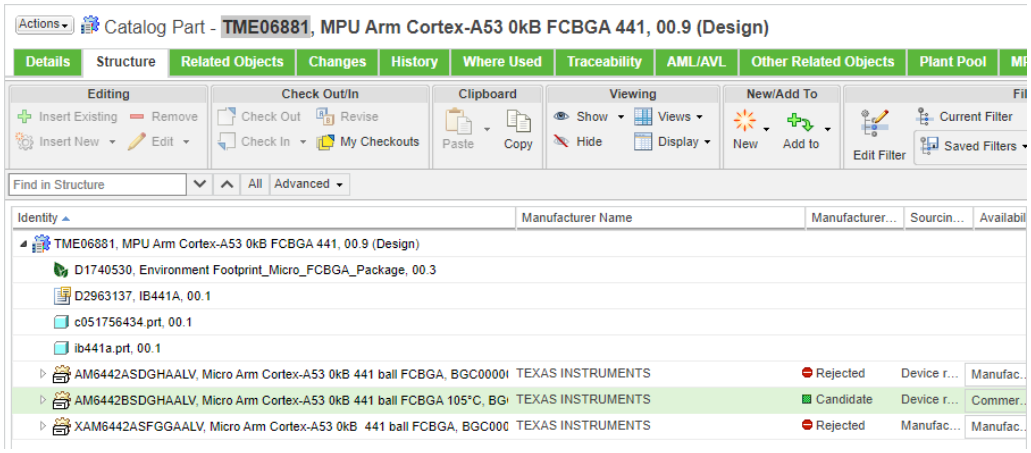
3.1.4.1 Pin usage

Please check [REF17]

3.1.4.2 AM64xx supported devices

- TME06881 version 00.9
  - AM6442BSDGHAALV



- AM6422 (*)
- AM6411 (*)

Note *: AM6441, AM6421, AM6412 could work also but were not selected, and won't be tested as a part of the low, medium or high Tier configurations.

FEATURES	REFERENCE NAME	AM6442	AM6441	AM6422	AM6421	AM6412	AM6411
CTRLMMR_WKUP_JTAG_DEVICE_ID[31:13] DEVICE_ID register bit field value[1]		D: 0x19464 E: 0x19465 F: 0x19466	D: 0x19264 E: 0x19265 F: 0x19266	D: 0x19424	D: 0x19224 E: 0x19225 F: 0x19226	C: 0x19403	C: 0x19203
PROCESSORS AND ACCELERATORS							
Speed Grades (See Table 7-1)		S	S	S	S	S, K	S, K
Arm Cortex-A53 Microprocessor Subsystem	Arm A53	Dual Core	Single Core	Dual Core	Single Core	Dual Core	Single Core
Arm Cortex-R5F	Arm R5F	2 × Dual Core	2 × Dual Core	1 × Dual Core	1 × Dual Core	Single Core	Single Core
Arm Cortex-M4F	Arm M4F	Single Core Functional Safety Optional[4]		Single Core	Single Core Functional Safety Optional[4]	Single Core	

3.1.5 Errata

All specifications of this document are not related to AM64's errata, please refer to official AM64 errata to check if there are some design limitations.

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4 DESCRIPTION OF FUNCTIONAL BLOCKS INSIDE THE BRICK

4.1 AM64 CPU

4.1.1 PMIC Power Management Integrated Circuit

4.1.1.1 Power Input Voltage

The BRICK operates with:

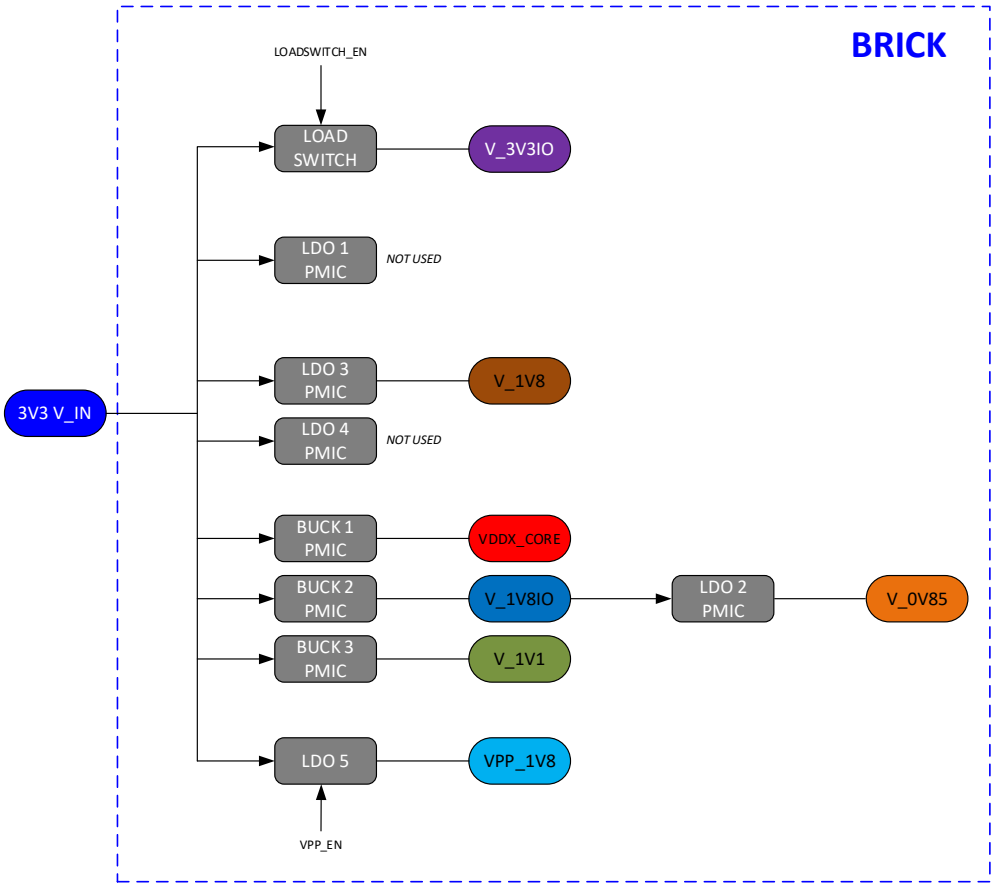
- 3V3 ± 2% input voltage. The tolerance must be confirmed, it depends on the selection of the Ethernet PHYs and the tolerance voltage of the PMIC Enable pin.

It has an external power enable logic input, which can be managed by the system or left unconnected (in this case the BRICK will be enabled with the under-voltage threshold monitoring of the PMIC).

PMIC generates, sequences and manage power fault conditions on all power rails delivered to supply the BRICK through its 3V3 input voltage system. In the case of 5V input Host design, an additional 5V to 3V3 DC/DC converter must be integrated by the Host designer.

Following architectures describe both configuration 3V3 input voltage and the 5V input Host voltage.

Here the power tree of the BRICK with 3V3 input voltage:



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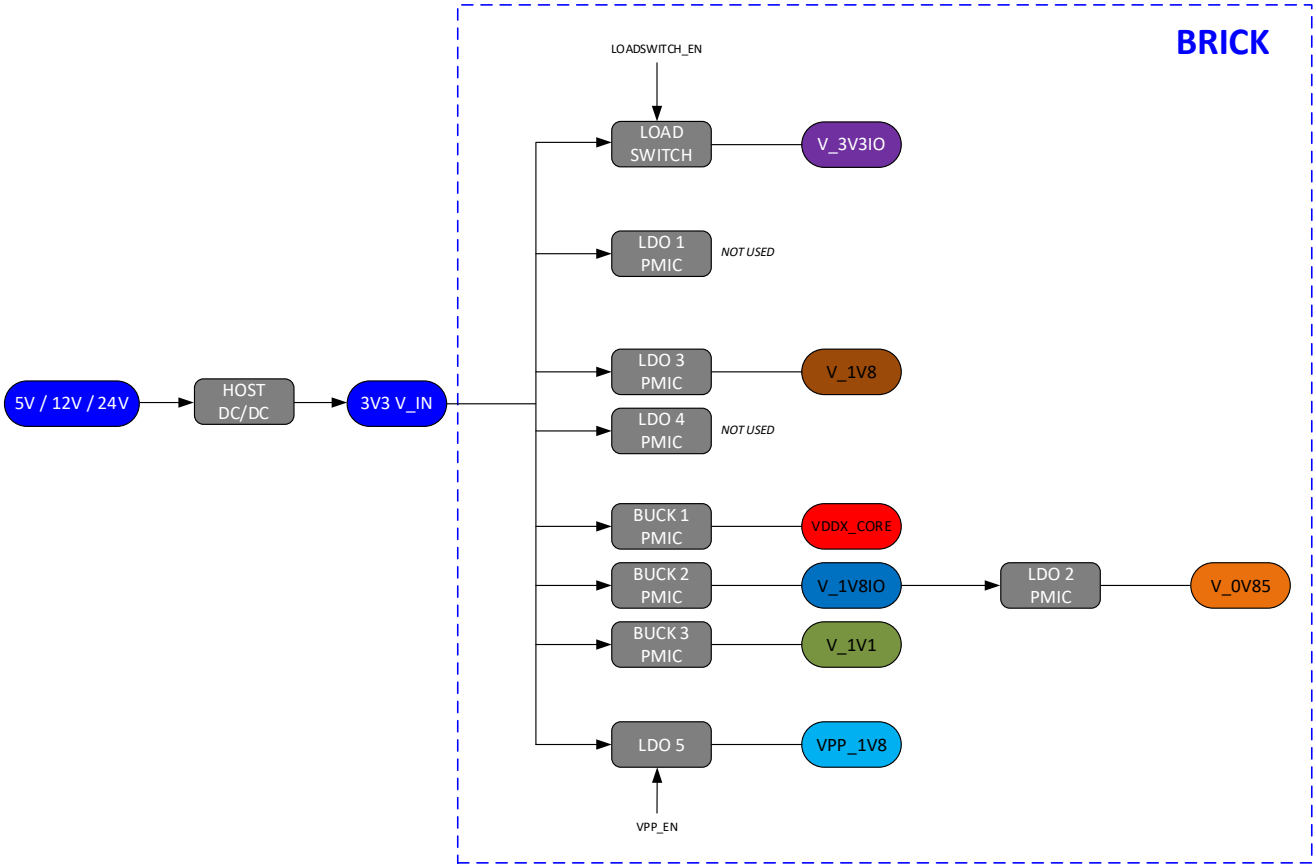
Here the power tree of the BRICK with 5V input voltage:



Note: Host will be responsible of his main power rail to 3V3 V_IN DC/DC converter.
For this additional DC/DC converter it must:

- Supply main Input Voltage of the BRICK,
- Comply with the technical specification of the Main Power Rail input 3V3 V_IN,
- Comply with the thermal constraint of the design.

4.1.1.2 Power Management

The TPS65220 provides 3 step-down converters, 4 LDOs, 3 general purpose I/Os and 3 multifunction pins. The integrated voltage supervisor monitors Buck 1 to 3, LDO 1 to 4 for undervoltage. The monitor has 2 sensitivity settings. Power good signal is provided to report the successful ramp of the seven power rails and GPOs of the PMIC. The nRSTOUT pin is pulled low until the PMIC enters in active state. The nRSTOUT pin has an open drain output.

Output voltage of each BUCK / LDO are adjustable through the I2C interface. In the BRICK design we did not consider this feature and do not manage Dynamic Voltage Scaling.

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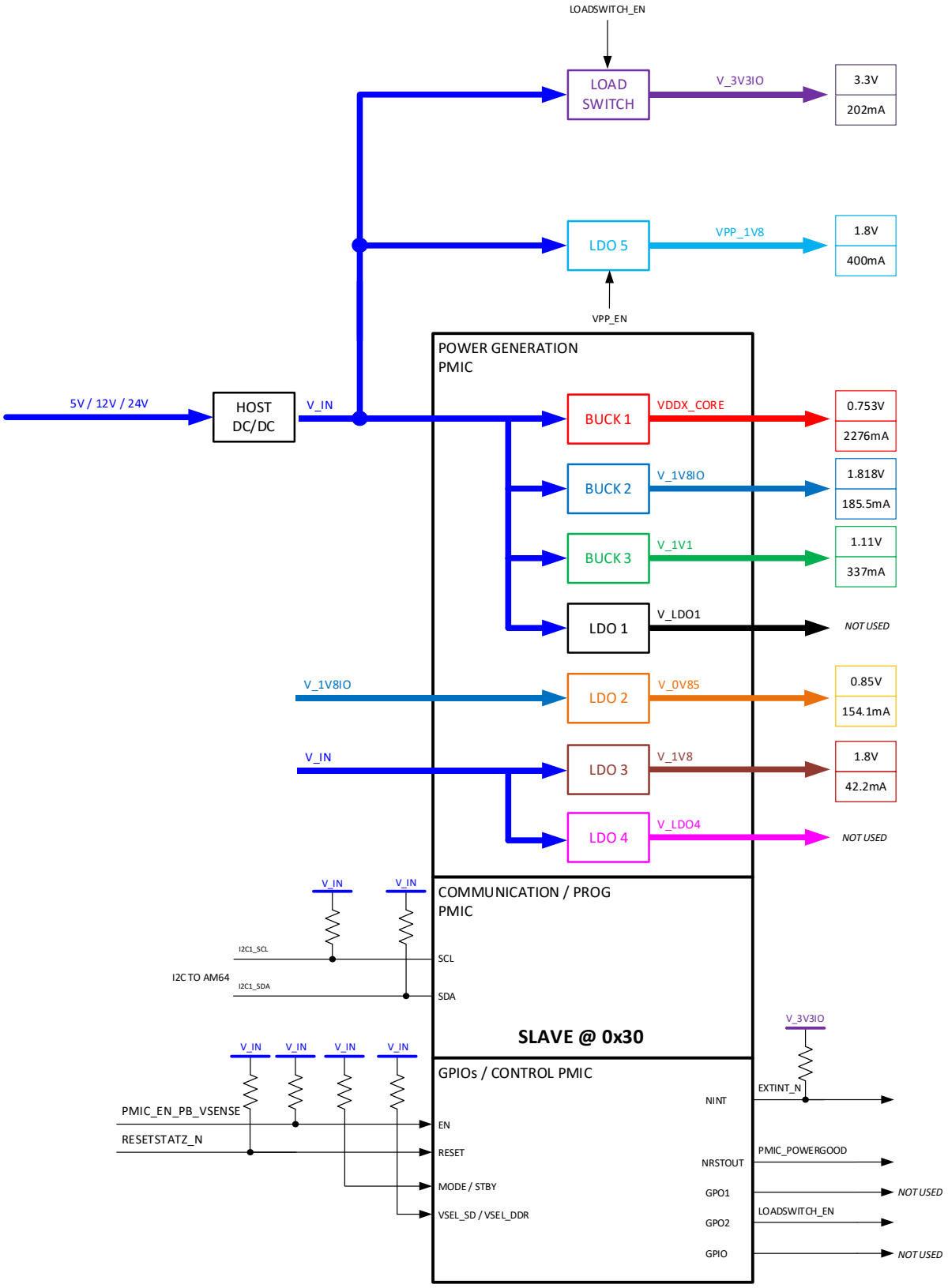

Schneider Electric	**AM64 BRICK** Electronic Design		
	Document Reference Number: **GEX95646xx**	*Revision:* **05**	*Sheet:* 17/164

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Below table covers Fault handling of the PMIC:

Topology	Fault	ACTIVE or STBY state
BUCK & LDO	Residual voltage shutdown Fault *	Fault triggers a sequence shutdown to INITIALIZE state
BUCK & LDO	Residual voltage	Fault does not trigger state change
BUCK & LDO	Timeout *	Fault triggers a sequenced shutdown to INITIALIZE state
BUCK & LDO	Undervoltage	Fault triggers a sequenced shutdown to INITIALIZE state
BUCK & LDO	Overcurrent	Fault triggers a sequenced shutdown to INITIALIZE state
BUCK & LDO	Short to GND	Fault triggers a sequenced shutdown to INITIALIZE state
BUCK & LDO	Temperature Warning	Fault triggers a sequenced shutdown to INITIALIZE state
BUCK & LDO	Temperature shutdown	Fault triggers an immediate shutdown to INITIALIZE state
3V3 V_IN	Undervoltage	Fault triggers an immediate shutdown to OFF state (not sequenced)
3V3 V_IN	Overvoltage	Fault triggers an immediate shutdown to OFF state (not sequenced)
VDD1P8	Under or Overvoltage	Fault triggers an immediate shutdown to OFF state (not sequenced)

* NOTE: Residual voltage shutdown fault and Timeout faults can only occur during a power down

4.1.1.3 Output Voltages

The Main power converters for the BRICK supplies is the TPS65220 PMIC. Below the current capabilities of each power rails and associated power element.

Topology	Input Voltage	Output Voltage (typ) / Rail Name	Current Capability
BUCK 1	3V3 V_IN	0.75V / VDDX_CORE	3.5 A
BUCK 2	3V3 V_IN	1.8V / V_1V8IO	2 A
BUCK 3	3V3 V_IN	1.1V / V_1V1	2 A
LDO 1	3V3 V_IN	*NA*	400 mA
LDO 2	V_1V8IO	0.85V / V_0V85	400 mA
LDO 3	3V3 V_IN	1.8V / V_1V8	300 mA
LDO 4	3V3 V_IN	*NA*	300 mA
LDO 5	3V3 V_IN	1.8V / VPP_1V8	500 mA
LOAD SWITCH	3V3 V_IN	3.3V V_IN / V_3V3IO	6 A

4.1.1.4 Input Decoupling Capacitor

The non-volatile memory configuration of the PMIC is described in a dedicated chapter below in this document. To justify all component choices of the design we just quote register parameters of the PMIC in front of the schematic.

All Buck regulators of the PMIC are preconfigured in HIGH BANDWIDTH & FORCED PWM mode.

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Pin Name	Setting	Register Name	Field Name	Value	Description
VSEL_SD / VSEL_DDR	Function selection	MFP_1_CONFIG	VSEL_DDR_SD	0x1	VSEL pin configured as SD to set the voltage on the VSEL_RAIL
	Rail	MFP_1_CONFIG	VSEL_RAIL	0x0	LDO1
	pin polarity (only applicable if VSEL_DDR_SD=0x1)	MFP_1_CONFIG	VSEL_SD_POLARITY	0x0	LOW: 1.8V / HIGH: LDOx_VOUT register setting
MODE / STBY	function selection	MFP_2_CONFIG	MODE_STBY_CONFIG	0x2	MODE and STBY
	pin polarity	MFP_1_CONFIG	MODE_STBY_POLARITY	0x0	[if configured as MODE] LOW: auto-PFM / HIGH: forced PWM. [if configured as a STBY] LOW: STBY state / HIGH: ACTIVE state.
MODE / RESET	function selection	MFP_2_CONFIG	MODE_RESET_CONFIG	0x1	RESET
	reset selection	MFP_2_CONFIG	WARM_COLD_RESET_CONFIG	0x1	WARM RESET
	pin polarity	MFP_1_CONFIG	MODE_RESET_POLARITY	0x0	[if configured as mode] LOW: auto-PFM / HIGH: forced PWM. [if configured as RESET] LOW: reset / HIGH: normal operation.

PMIC Rail	Register Name	Field Name	Value	Description
Bucks Switching Mode (Global for all Buck regulators)	BUCKS_CONFIG	BUCK_FF_ENABLE	0x0	Quasi-fixed frequency mode
	BUCKS_CONFIG	BUCK_SS_ENABLE	0x0	Spread spectrum disabled
BUCK1	BUCK1_VOUT	BUCK1_VSET	0x6	0.750V
	BUCK1_VOUT	BUCK1_UV_THR_SEL	0x0	-5% UV detection level
	BUCK1_VOUT	BUCK1_BW_SEL	0x1	high bandwidth
BUCK2	BUCK2_VOUT	BUCK2_VSET	0x24	1.800V
	BUCK2_VOUT	BUCK2_UV_THR_SEL	0x0	-5% UV detection level
	BUCK2_VOUT	BUCK2_BW_SEL	0x1	high bandwidth
	BUCKS_CONFIG	BUCK2_PHASE_CONFIG	0x3	270 degrees (only applicable if Bucks are configured for fixed frequency)
BUCK3	BUCK3_VOUT	BUCK3_VSET	0x14	1.100V
	BUCK3_VOUT	BUCK3_UV_THR_SEL	0x0	-5% UV detection level
	BUCK3_VOUT	BUCK3_BW_SEL	0x1	high bandwidth
	BUCKS_CONFIG	BUCK3_PHASE_CONFIG	0x2	180 degrees (only applicable if Bucks are configured for fixed frequency)

Extract from [REF7]

Considering this switching mode the minimum decoupling input BUCK capacitor for each regulators according to the datasheet is: 3.9µF min and 4.7µF typical.

For LDO the minimum decoupling input LDO capacitor is: 1.6µF min 2.2µF typical.

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6.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

POS			MIN	NOM	MAX	UNIT
3.1.10a	C_{OUT_B1}, C_{OUT_B2}, C_{OUT_B3}	BUCKx Output Capacitance, forced PWM or auto-PFM, high bandwidth case	30		220	µF
3.1.10b	C_{OUT_B1}, C_{OUT_B2}, C_{OUT_B3}	BUCKx Output Capacitance, fixed frequency, high BW case	48		144	µF
3.1.11	V_{FB_B1}, V_{FB_B2}, V_{FB_B3}	BUCKx FB Pins	0		5.5 (2)	V
3.1.12	V_{PVIN_LDO1}, V_{PVIN_LDO2}	LDO Input Voltage	1.5		5.5 (2)	V
3.1.13	V_{PVIN_LDO1}, V_{PVIN_LDO2}	LDO Input Voltage in bypass mode	1.5		3.6	V
3.1.15	V_{VLDO1}, V_{VLDO2}	LDO Output Voltage Range	0.6		3.4	V
3.1.16	C_{PVIN_LDO1}, C_{PVIN_LDO2}	LDO Input Capacitance	1.6	2.2		µF
3.1.17	C_{VLDO1}, C_{VLDO2}	LDO Output Capacitance	1.6	2.2	20	µF
3.1.18	V_{PVIN_LDO3}, V_{PVIN_LDO4}	LDO Input Voltage	2.2		5.5 (2)	V
3.1.19	V_{VLDO3}, V_{VLDO4}	LDO Output Voltage Range	1.2		3.3	V
3.1.20	C_{PVIN_LDO34}	LDO Input Capacitance	2.2	4.7		µF
3.1.21	C_{VLDO3}, C_{VLDO4}	LDO Output Capacitance	1.6	2.2	30 (3)	µF
3.1.22	V_{VDD1P8}	VDD1P8 pin	0		1.8	V
3.1.23	C_{VDD1P8}	Internal Regulator Decoupling Capacitance	1	2.2	4	µF
3.1.24	C_{VSYS}	VSYS Input Decoupling Capacitance	1	2.2		µF
3.1.25	V_{nINT}, $V_{nRSTOUT}$	Digital Outputs	0		3.4	V
3.1.26	V_{GPO1}, V_{GPO2}, V_{GPIO}	Digital Outputs	0		5.5 (2)	V
3.1.27	V_{SCL}, V_{SDA}	I2C Interface	0		3.4	V
3.1.28	$V_{EN/PB/VSENSE}$, $V_{MODE/STBY}$, $V_{MODE/RESET}$, $V_{VSEL_SD/VSEL/DDR}$	Digital Inputs	0		5.5 (2)	V
3.3.1	$T_{A_}$	Operating free-air temperature	–40		125	°C
3.3.2	$T_{J_}$	Operating junction temperature	–40		150	°C

Extract from [REF5]

We are using Dedicated 10µF Input capacitor for each buck inputs. Therefor an additional of 3 decoupling capacitors is also populated to sustain transient load. The average input decoupling capacitors is 19µFcomposed of:

Common input BUCK / LDO capacitors:

- 1x 22µF HUA36515 10VDC X7R 1206 C41,
- 1x 4.7µF TME10696 6.3VDC X6S 0402 C37,
- 1x 100nF HUA30500 25VDC X7R 0402 C38,

Power Rails dedicated input BUCK capacitors:

- V_1V1
  - 1x 10µF HUA15709 10VDC X7R 0805 C26,
- V_1V8IO
  - 1x 10µF HUA15709 10VDC X7R 0805 C29,
- VDDX_CORE
  - 1x 10µF HUA15709 10VDC X7R 0805 C25,

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Power Rails dedicated input LDO capacitors (LDO1 and LDO4 are unused in the design):

- V_0V85 LDO2
  - 1x 4.7µF TME10696 6.3VDC X6S 0402 C32,

- V_1V8 LDO3 & LDO4 (Same input pins on component)
  - 1x 4.7µF TME10696 6.3VDC X6S 0402 C34,

- LDO1
  - No dedicated decoupling capacitor (LDO is not used in the design), actually using the common decoupling capacitor between BUCK and LDO.

4.1.1.5 Output Decoupling Capacitor

According to the datasheet the minimum output BUCK capacitor is 30µF and the minimum output LDO capacitor is 1.6µF.

6.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

POS			MIN	NOM	MAX	UNIT
3.1.10a	C_{OUT_B1}, C_{OUT_B2}, C_{OUT_B3}	BUCKx Output Capacitance, forced PWM or auto-PFM, high bandwidth case	30		220	µF
3.1.10b	C_{OUT_B1}, C_{OUT_B2}, C_{OUT_B3}	BUCKx Output Capacitance, fixed frequency, high BW case	48		144	µF

Extract from [R5]

We apply 45.32µF on each BUCK output, Output BUCK decoupling capacitors are composed of:

- V_1V1
  - 2x 22µF HUA36515 10VDC X7R 1206 C20, C23,
  - 1x 1µF TME10670 6.3VDC X6S 0201 C187,
  - 1x 220nF TME09627 6.3VDC X6S 0201 C203,
  - 1x 100nF HUA30500 25VDC X7R 0402 C165,

- V_1V8IO
  - 2x 22µF HUA36515 10VDC X7R 1206 C31, C36,
  - 1x 1µF TME10670 6.3VDC X6S 0201 C167,
  - 1x 220nF TME09627 6.3VDC X6S 0201 C202,
  - 1x 100nF HUA30500 25VDC X7R 0402 C156,

- VDDX_CORE
  - 2x 22µF HUA36515 10VDC X7R 1206 C19, C22,
  - 1x 1µF TME10670 6.3VDC X6S 0201 C92,
  - 1x 220nF TME09627 6.3VDC X6S 0201 C95,
  - 1x 100nF HUA30500 25VDC X7R 0402 C88,

We apply different output LDO capacitors value depending on the scenario described below:

- V_0V85 LDO2
  - 2x 4.7µF TME10696 6.3VDC X6S 0402 C33, C39,
  - 1x 100nF HUA30500 25VDC X7R 0402 C97,

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- V_1V8 LDO3
  - 3x 4.7µF TME10696 6.3VDC X6S 0402 C114, C28, C30,
  - 1x 100nF HUA30500 25VDC X7R 0402 C99,

- LDO1
  - 1x 4.7µF TME10696 6.3VDC X6S 0402 C35,

- LDO4
  - 1x 4.7µF TME10696 6.3VDC X6S 0402 C40,

According to the datasheet the Internal 1V8 Regulator must be decoupled by a capacitor in the value range between 1µF min and 4.7µF max.

Internal 1V8 Regulator decoupling capacitor:

- VDD1P8
  - 1x 4.7µF TME10696 6.3VDC X6S 0402 C21,

As the power rail of VDD1P8 = 1.8V and the capacitor voltage is 6.3VDC, due to voltage derating we can assure to fit with requirement 1µF < C < 4.7µF. in the full temperature range.

4.1.1.6 Inductors selection

Although there are 3 different BUCKS in the PMIC, the only difference is in the buck input supply voltage supported.

We'll only show the parameter from the BUCK 1 converter and apply it to BUCK 2 and BUCK 3 as there are identical in the datasheet, please refer to the full document where we extract the parameter.

6.5 BUCK1 Converter

over operating free-air temperature range (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics							
5.1.1a	V_{IN_BUCK1}	Input voltage[1]	Buck supply voltage, maximum VSYS	2.5		5.5	V
5.1.1b	V_{OUT_BUCK1}	Buck Output Voltage configurable Range	Output voltage configurable in 25mV-steps for 0.6V ≤ V_{OUT} ≤ 1.4V, in 100mV steps for 1.4V < V_{OUT} ≤ 3.4V	0.6		3.4	V
5.1.4	$V_{OUT_STEP_LOW}$	Output voltage Steps	0.6V ≤ V_{OUT} ≤ 1.4V		25		mV
5.1.5	$V_{OUT_STEP_HIGH}$	Output voltage Steps	1.5V ≤ V_{OUT} ≤ 3.4V		100		mV
5.1.6a	$V_{OUT_ACC_DC_PWM}$	DC Output Voltage Accuracy in forced PWM mode, low and high BW case	I_{OUT} = I_{OUT_MAX}, V_{OUT} = 0.6V to 3.4V, V_{IN} - V_{OUT} > 700 mV forced PWM, low BW case	–1.5%		1.5%	
5.1.6b	$V_{OUT_ACC_DC_PFM}$	DC Output Voltage Accuracy in auto-PFM mode, low and high BW case	I_{OUT} = 1mA, V_{OUT} = 0.6V to 3.4V, V_{IN} - V_{OUT} > 500 mV auto-PFM, low BW case	–3.0%		3.5%	
5.1.6c	$V_{OUT_ACC_DC_FF}$	DC Output Voltage Accuracy in Fixed Frequency mode, low and high BW case	I_{OUT} = I_{OUT_MAX}, V_{OUT} = 0.6V to 3.4V, V_{IN} - V_{OUT} > 1000 mV fixed frequency, low BW case	–1.5%		1.5%	
5.3.1	I_{OUT_MAX}	Maximum Operating Current				3.5	A
5.4.1	L_{SW}	Output Inductance	DCR = 50mΩ max	330	470	611	nH
5.4.2a	C_{OUT}	Output Capacitance in auto-PFM or forced PWM for low BW case	ESR = 10mΩ max	10		75	µF
5.4.2b	C_{OUT_FF}	Output Capacitance in fixed frequency for low BW case	ESR = 10mΩ max	12		36	µF
5.4.3a	$C_{OUT_HIGH_BW}$	Output Capacitance in auto-PFM or forced PWM for high BW case	ESR = 10mΩ max	30		220	µF
5.4.3b	$C_{OUT_HIGH_BW_FF}$	Output Capacitance in fixed frequency for high BW case	ESR = 10mΩ max	48		144	µF

Extract from [REF5]

According to the datasheet the inductor value must be between 330nH min and 611nH max. As shown previously in the document BUCK regulators are configured in FORCED PWM mode so the frequency switch is 2.3Mhz.

To optimize the bill of material for cost, we decided to use same Inductor for all BUCK regulators and so select it in front of the most powerful one which is BUCK1 with 3.5A current capability with DCR 25mΩ (<50mΩ required).

With all those parameters we select the inductor for each BUCK:

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- BUCK 1
  - 1x 470nH TME05961 0.025Ω 4.5A 0806 L1,
- BUCK 2
  - 1x 470nH TME05961 0.025Ω 4.5A 0806 L2,
- BUCK 3
  - 1x 470nH TME05961 0.025Ω 4.5A 0806 L3,

4.1.1.7 Power Budget

Power Budget estimation is based on the worst-case estimation ([REF3] and [REF4]) .
All interfaces of the AM64 are configured on max performance and speed. This is not realistic and do not represent the reality but considering this case the BRICK has enough margin to address all possible HOST configuration.

Below the global power consumption synthesis:

Section	Power rail name	Voltage (Volt)	Current estimated on each power rail (mA)		Power estimated on each power rail (W)	
		Typ	Typ	Max	Typ	Max
Brick	VDDX_CORE		1648,0	2276,0	1,24	1,71
	V_0V85		89,4	154,1	0,08	0,13
	V_1V8		42,2	42,2	0,08	0,08
	V_1V1		337,5	208,2	0,37	0,23
	V_1V8IO		96,8	185,5	0,17	0,32
	V_3V3IO		134,7	202,0	0,44	0,67
	3V3 V_IN		**1195,0**	**1662,8**	**3,94**	**5,49**

Note:

1. VPP_1V8 is not in this table because we only consider it to fuse the OTP worst case consumption on this power during burning is 400mA. In nominal state the consumption in negligeable, the Voltage regulator is in HIGH Z state.

   VPP_1V8 current consumption.pdf
2. Host MUST consider 3V3 V_IN power consumption in order to design his own DC/DC converter if the "different input voltage stage" solution is selected. It is strongly recommended to take 6W as a minimum design capability of 3V3 V_IN and so 7.2W on Input power rail.

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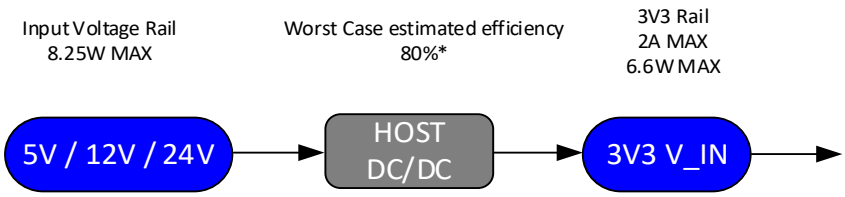

*NOTE : 80% estimated efficiency do not exclude system Thermal analyse

4.1.1.8 Power Sequence

This section describes power sequence requirements using diagrams and associated notes. Each power sequence diagram demonstrates the sequential order expected. The order of the rails, including GPOs for external rails and the nRSTOUT pin is defined by the Non-Volatile Memory embedded inside the PMIC. For cost optimization, BRICK is using the default configuration of the PMIC and does not need any programming of the sequence power up.

Starting the power up sequence the device checks if the voltage on all rails fell below the short to ground threshold to avoid starting into a pre biased rail. The sequence is timing based and all timing parameters are defined in PMIC registers.

During power up sequence previous rail must have passed its UnderVoltage threshold (ref to 4.1.1.11.3), else subsequent rail will not be enabled. In addition, PMIC will only proceed the next power rail sequence if the previous one has passed the Undervoltage threshold, else subsequent rail will not be enabled.

In this case the sequence is interrupted due to fault on rail and PMIC powers down. After the Fault power down sequence PMIC will attempt to power up two more times. If both of those retries fail to achieve the power up sequence PMIC will stay in INITIALIZE state until 3V3 V_IN is power cycled.

At initial power up, PMIC monitors the 3V3 V_IN supply voltage and allow power up sequence only if the VSYSPOR_Rising threshold is passed.

Important Note:

The V_3V3IO is distributed through a loadswitch. As the enable pin of this switch is pulled up to the V_3V3IO at the first power up (COLD START) of the brick the V_3V3IO start up is not controlled by the PMIC. This function is called FSD (First Supply Detect).

For the WARM power up PMIC has the full controlled on the startup of the V_3V3IO as it is described by both power up sequences below.

The BRICK can be interfaced with I/Os which can be supplied by powers not managed by the PMIC, the HOST_PWR_EN is mandatory to be used as EXTERNAL POWER UP signal in order to synchronize internal BRICK power up AND external BRICK power supply to avoid any latch up (because most of the I/Os are not “fail safe”).

This signal is realized by the AND gate U13 which is supplied through th V_IN input voltage of the BRICK. The reason is due to the FSD function this gate may have input signal before V_3V3IO is on. In order to avoid any latch up on component we let U13 been supplied by V_IN.

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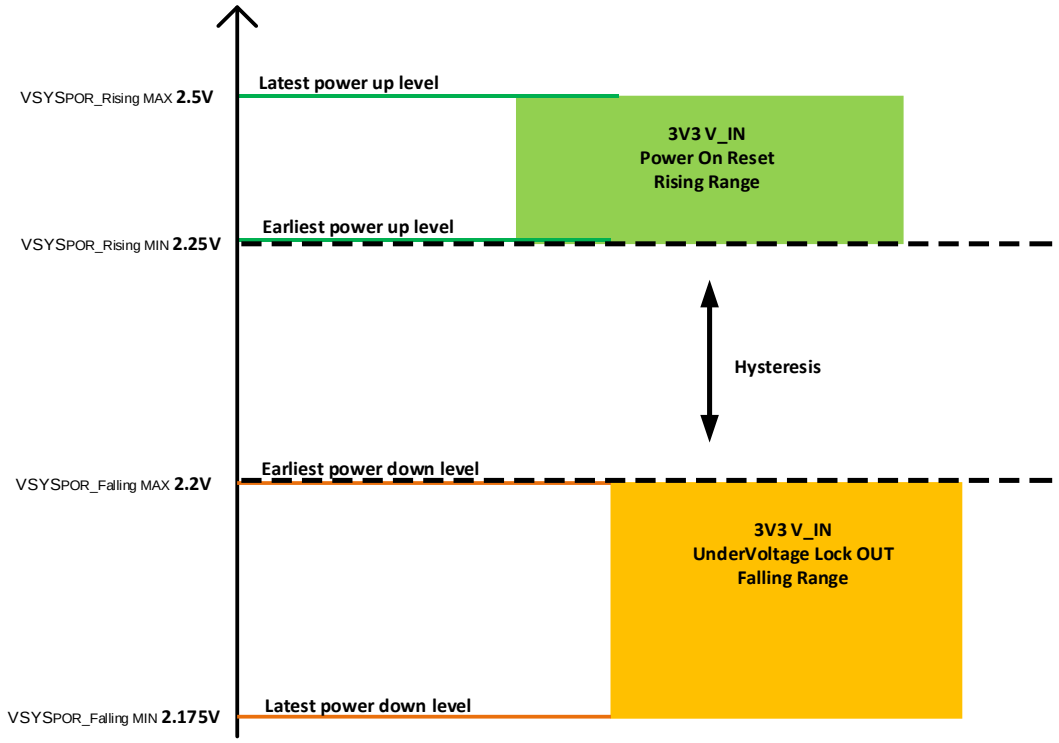

Power up and Power down sequence are completely independent and describe below.

An OFF request or a shutdown fault will trigger the power down sequence. The OFF request may be triggered by a falling edge on the PMIC's ENABLE pin or by an I2C command to I2C_OFF_REQ in MFP_CTRL register.

An I2C triggered shut down will require a renewed-ON request on the ENABLE pin. In our configuration this ON request is either a low going edge followed by a high going edge on ENABLE pin or a power cycle on 3V3 V_IN.

Falling edge deglitch time for ENABLE pin $t_{DEGL_EN/VSENSE_I2C}$ = 120µs.

The Power down sequence is gated by the previous rail being discharged under the short to ground threshold voltage. If that does not occur during the defined time slot, the power down of subsequent rails is paused until threshold is reached. If the short to ground threshold isn't reached until 8 times the slot duration the power down sequence continues.

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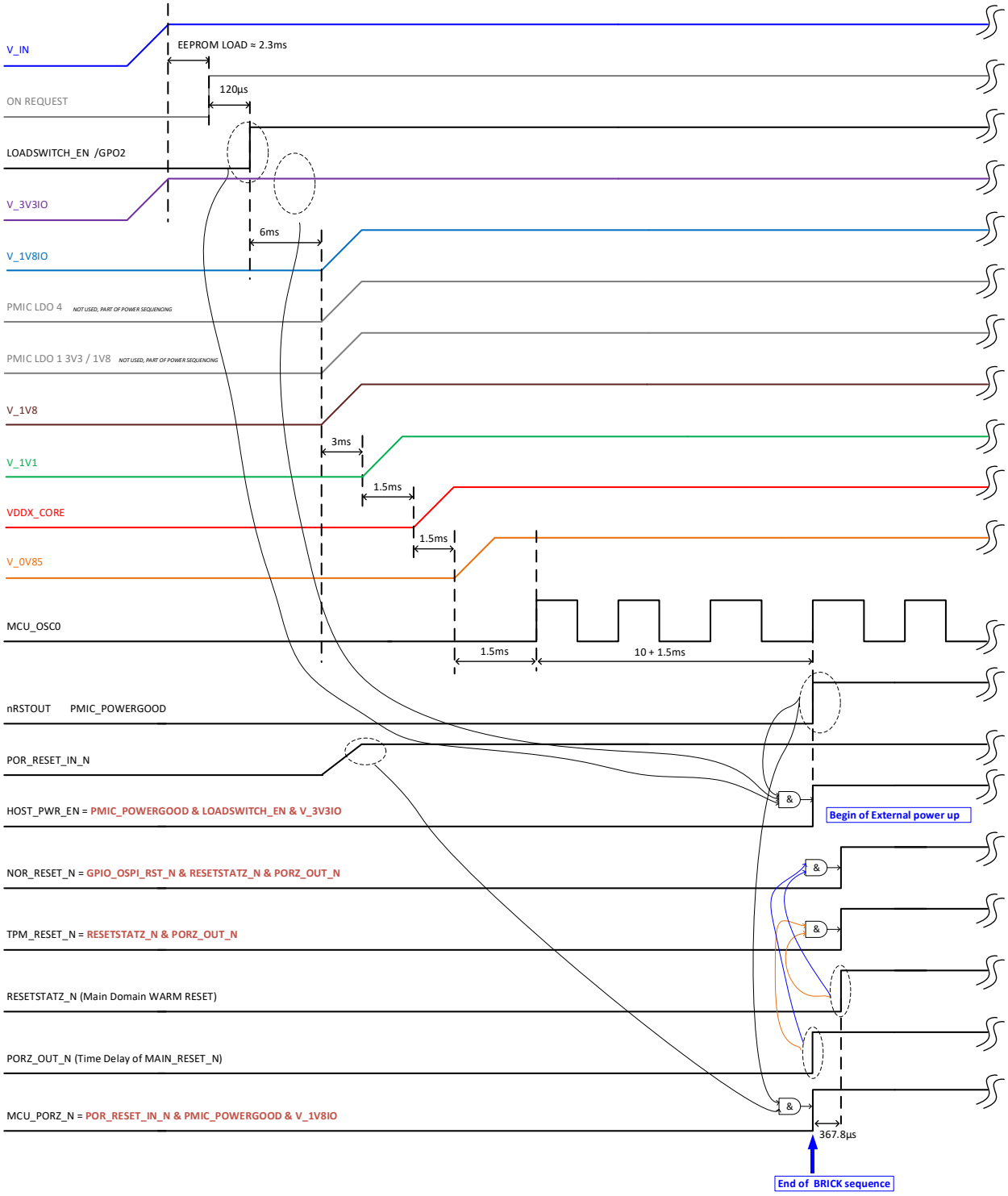
1rst Power UP (COLD Start)
WITHOUT DRIVES ON POR_RESET_IN_N
WITHOUT DRIVES ON GPIO_OSPI_RST



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	Document Reference Number: **GEX95646xx**	*Revision:* **05**	*Sheet:* 26/164
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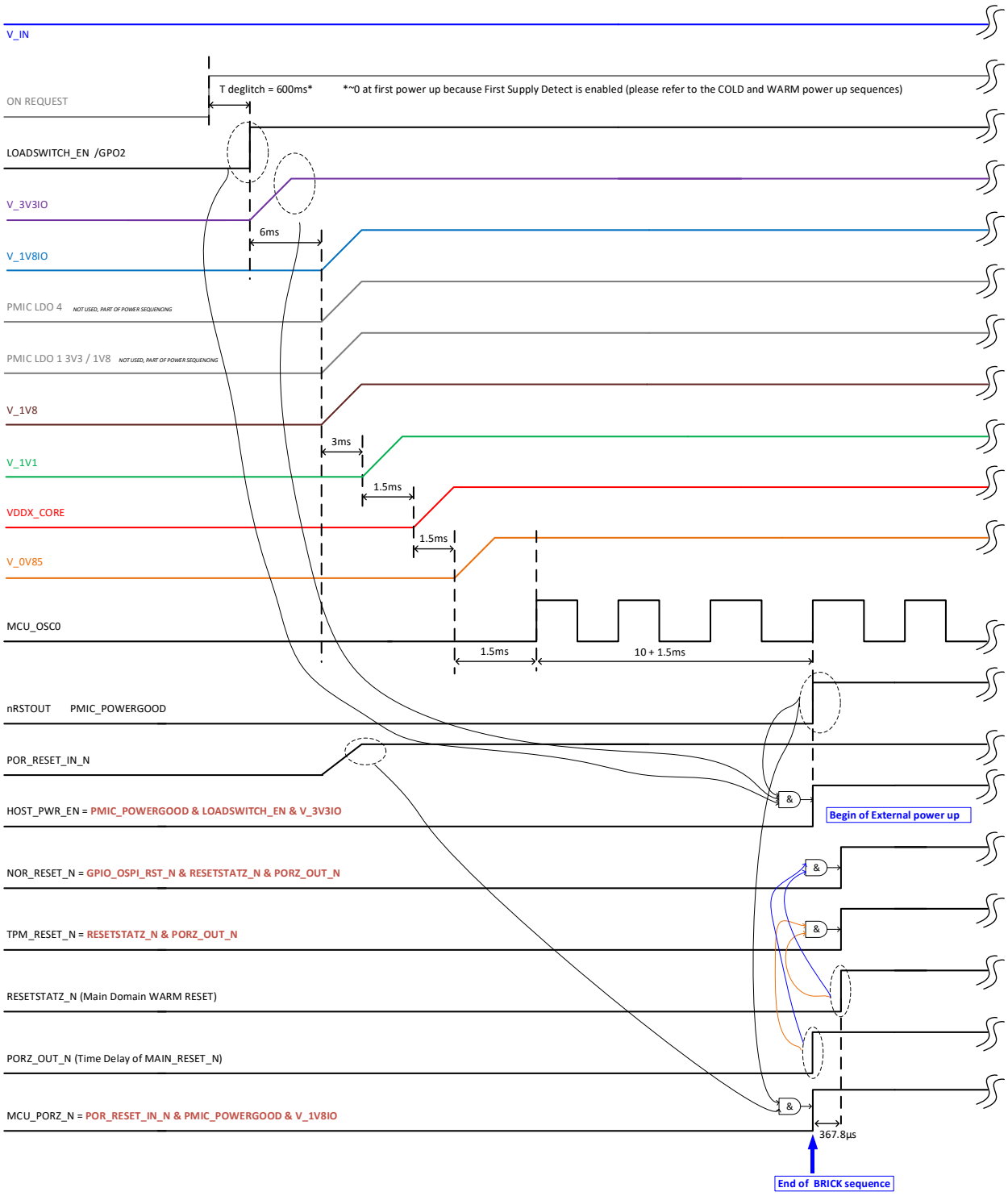
Warm Power UP
WITHOUT DRIVES ON POR_RESET_IN_N
WITHOUT DRIVES ON GPIO_OSPI_RST



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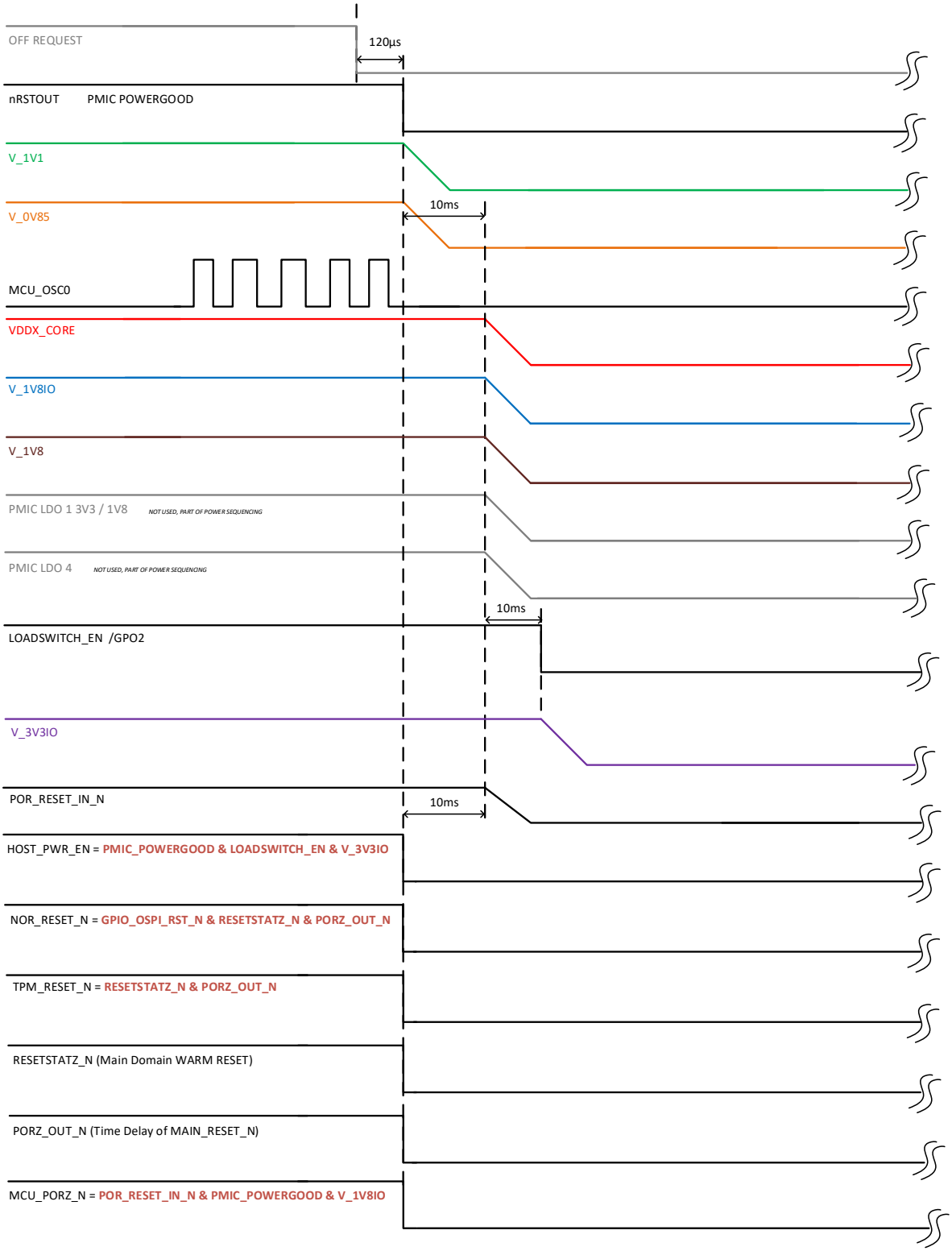
Power DOWN sequencing & RESET
WITHOUT DRIVES ON POR_RESET_IN_N
WITHOUT DRIVES ON GPIO_OSPI_RST



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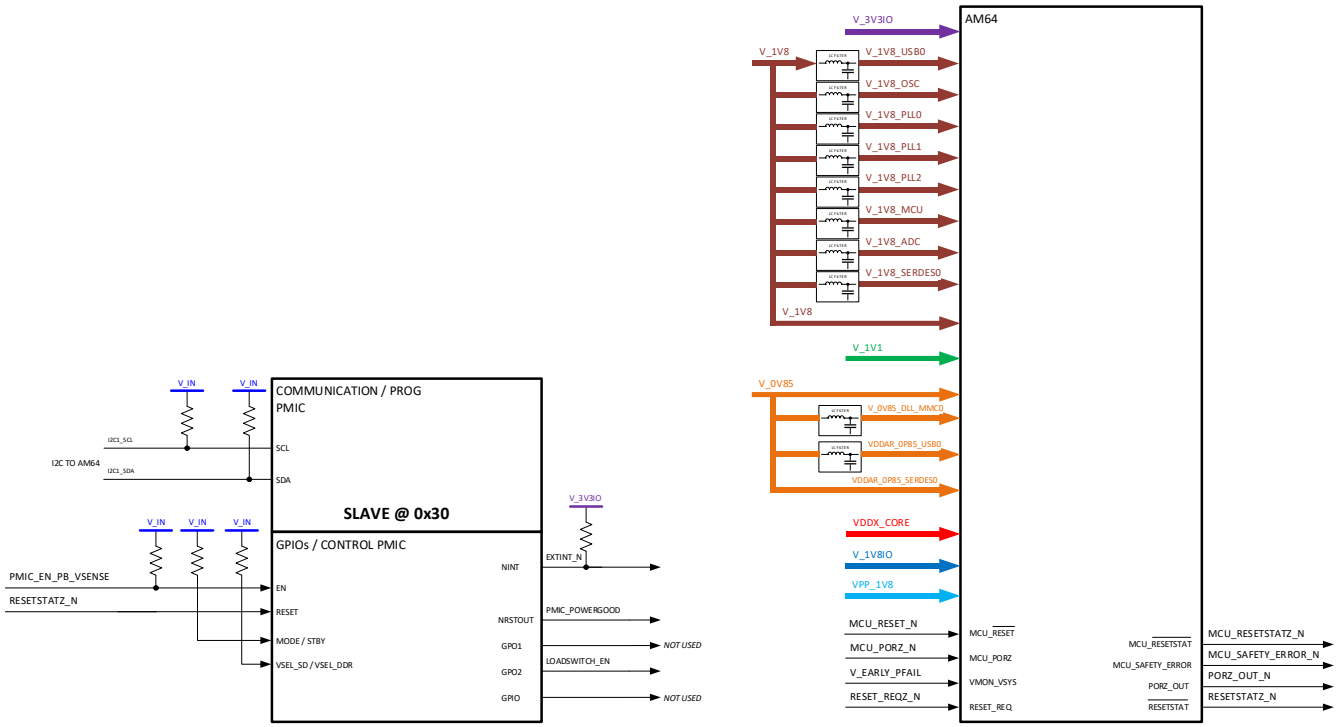
4.1.1.9 PMIC Interfaces

4.1.1.9.1 PMIC I2C

PMIC is directly interfaced with the AM64 by I2C through the I2C0.
The default I2C address is 30h (8 bits address) equal to 48d according to [REF5].

I2C transactions are ignored during the following situations:

- When PMIC is entering INITIALIZE state (from any state). I2C access is denied before EEPROM loading (for about 2.3ms, see power up sequence),
- During processing of a WARM reset, I2C access is denied for 60µs,
- While beginning transition into INITIALIZE, I2C access is denied for 80µs.



I2C pull up can be connected to external VIO (not a PMIC power supply) voltage up to recommended 3.4V.
It can operate at speed of 100KHz/400KHz/1MHz with VIO = 3.3V or 1.8V.
Pull up will be connected to 3V3_IO according to TI EVM SK, to ensure that I2C0 bank is powered with the same 3V3_IO.

4.1.1.9.2 PMIC nINT interrupt pin

TPS6522053 has an interrupt request output pin connected to the AM64 through the NINT signal. NINT signal is an open drain signal which is pulled low for fault conditions. This signal will be released and go back to high state only if triggered bit in INT_SOURCE register is cleared.

4.1.1.9.3 PMIC nRSTOUT pin

Reset output (nRSTOUT) is an open drain output, intended to release the RESET to the AM64 at the end of the power up sequence. This signal is HIGH when the power up sequence is finished without any fault detection. The

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signal is driven low if fault condition is detected, on WARM and COLD reset request or on power down sequence request.

4.1.1.9.4 PMIC MODE/RESET pin

This pin is in WARM RESET mode in our application. RESET pin is edge sensitive and apply a deglitch time. This signal needs to be hold down for longer than tDEGLITCH_RESET (TBD by TI, time not yet specified in the datasheet) to cause a WARM RESET.

During this WARM RESET, all enabled rails remain on. If HOST has managed the Dynamic Voltage Scaling, output voltage of rails is reset and get back to the boot voltage value.

Specifically, following configurations get reset to their boot-value: BUCK1_VSET, BUCK2_VSET, BUCK3_VSET, LDO1_VSET, LDO2_VSET, LDO1_BYP_CONFIG, LDO2_BYP_CONFIG and VSEL_SD_I2C_CTRL.

All other bits, even in the same register, will remain at their current state, i.e. LDOx_LSW_CONFIG, BUCKx_BW_SEL, BUCKx_UV_THR_SEL and the MFP_1_CONFIG register bits will NOT get reset during a WARM-reset.

4.1.1.9.5 PMIC VSEL_SD/VSEL_DDR pin

VSEL pin is in VSEL_SD mode as it is configured by default in MFP_1_CONFIG register. This means BUCK3 output voltage will stabilize his output voltage to 1.1V and LDO1 output voltage is settled between 3.3V (VSEL_SD is High) and 1.8V (VSE_SD is low).

This functionality is not implemented, AM64 has its own internal LDO to manage switches between 3.3V and 1.8V.

4.1.1.10 PMIC Functional Modes

4.1.1.10.1 Modes of operation

4.1.1.10.1.1 OFF State

In OFF state PMIC is not yet or insufficiently supplied. Neither internal logic nor external rails are available.
If 3V3 V_IN exceeds VSYS Power-On Reset threshold and internal 1V8 supply rail is in regulation PMIC will enter the INITIALIZE state.

4.1.1.10.1.2 INITIALIZE State

In INITIALIZE state the PMIC is completely shut down except for a few circuits to monitor ENABLE pin. At this point PMIC is reading its memory and loads registers.

Entry to INITIALIZE state is gated if any one of the thermal sensors is above the TWARM_Rising threshold and WARM-detection is not masked. The EEPROM loading takes about 2.3ms. The power-up sequence can only execute after the EEPROM-load and if all rails are discharged below the VBUCKx_SCG_TH respectively VLDOx_SCG_TH threshold.

If INITIALIZE state was entered from OFF state, bit POWER_UP_FROM_OFF in POWER_UP_STATUS_REG register will be set and will remain set until a write-1-clear is issued. Read-out of this bit allows to determine if INITIALZE state was entered from OFF state or due to a Shut-down-fault or OFF-request.

In INITIALIZE state, the nINT pin status depends on faults and their masking. If no faults are present or nINT-reaction for those are masked, nINT-pin will be pulled high, provided a V_3V3IO-voltage for the pull-up is available.

To transition from the INITIALIZE state to the ACTIVE state, the ON request must occur:

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- The ENABLE pin is HIGH.

4.1.1.10.1.3 ACTIVE State

The ACTIVE state is the normal mode of operation when the system is up and running. All enabled buck converters and LDOs are operational and can be controlled through the I2C. ACTIVE state can also be entered from STBY state by de-asserting the STBY pin HIGH or by I2C command.

To transition to STBY state, the STBY pin must be forced or an I2C command to STBY_I2C_CTRL in MFP_CTRL register must be issued.

To transition to INITIALIZE state, one of the following OFF_Request must occur:

- ENABLE pin is LOW,
- An I2C OFF Request is issued.

If a shutdown fault (SD_Fault) occurs while in the ACTIVE state, PMIC will sequence down the active outputs and transition to the INITIALIZE state. In case of shut down fault, no renewed-on request is required, PMIC will power up again if ENABLE input is still above the VIH-threshold (ENABLE pin considered level sensitive).

4.1.1.10.1.4 STBY State

For the moment BRICK hasn't integrated drivers to manage this feature. This chapter is just to inform HOST that feature is available and can be realized through the associated interface.

STBY state is a low-power mode of operation intended to support system standby. The mode can be entered by the MODE/STBY pin or by an I2C command to STBY_I2C_CTRL in MFP_CTRL register. Typically, the majority of power rails are turned off with the exception of rails required to the AM64 during this state. Which rails power down in STBY state can be configured in STBY_1_CONFIG and STBY_2_CONFIG registers.

During STBY state monitoring functions are still available and enabled:

- Undervoltage,
- Short to ground,
- Over current detection,
- Thermal warning,
- Thermal shut down.

The PMIC enters ACTIVE state if I2C command is received. Before starting the STBY to ACTIVE sequence, disabled rails are discharged. In case this fails to complete within 80ms, PMIC runs into a timeout condition and transitions to INITIALIZE state. At this step PMIC sets bit TIMEOUT in the INT_TIMEOUT_RV_SD register and the fault flags for the rail that caused the shutdown.

The sequence into and out of STBY state is the same as for power down respectively for power-up. Rails that remain on in STBY are skipped, but their respective slots are executed.

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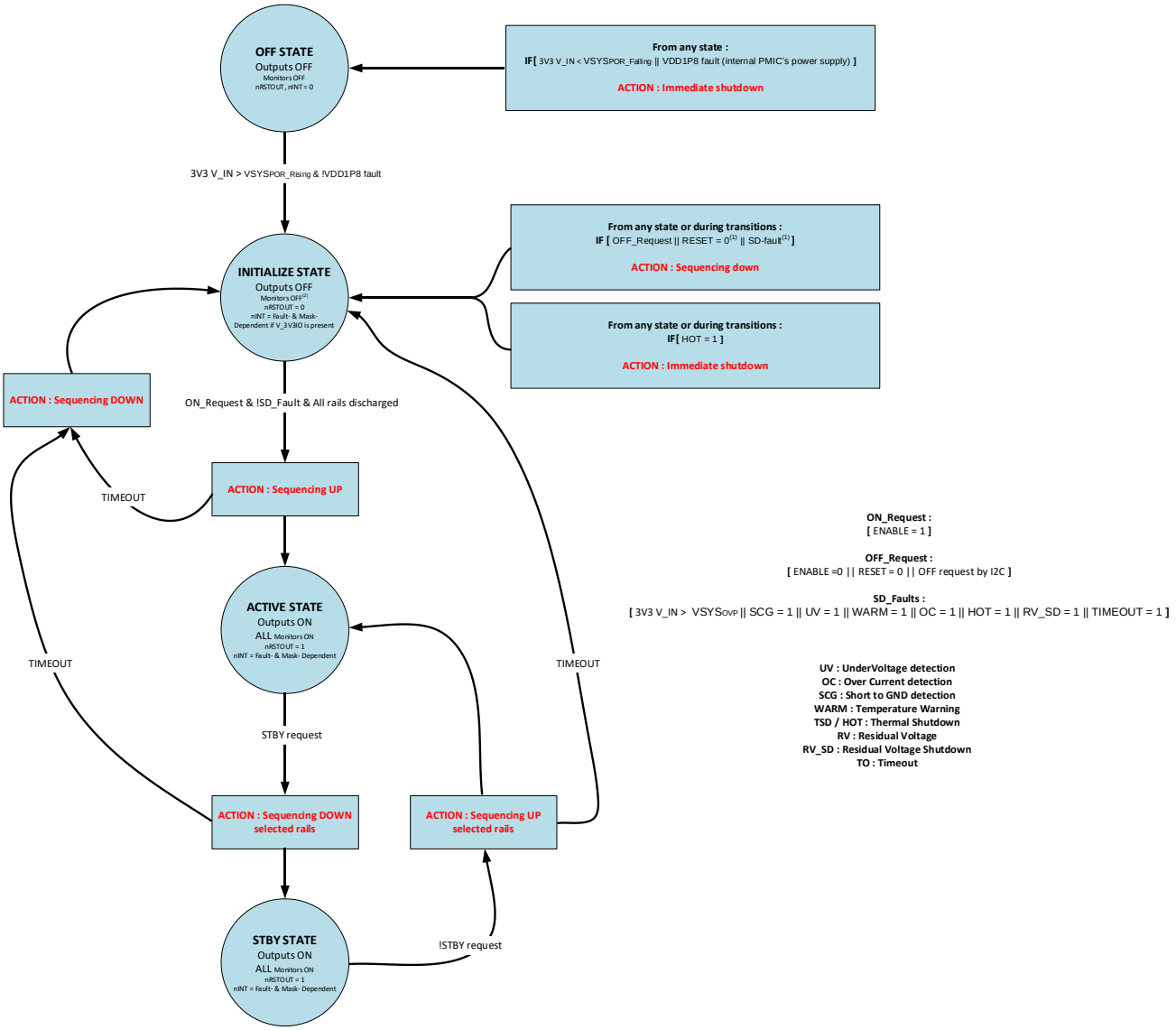
4.1.1.10.2 Diagram of operations



4.1.1.11 PMIC Non-Volatile Memory Configuration TPS6522053

The following sections describe the default configuration on the EEPROM-backed registers. The NVM configuration described in this document is ideal for the following application:

- Processor: AM62, AM64
- CORE voltage: 0.75V
- Memory: LPDDR4
- Input Supply V_IN: 3.3V

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4.1.1.11.1 PMIC Device ID

This section lists all the register settings to identify the supported temperature and the NVM ID with the corresponding revision that represent a list of default register settings.

Register Name	Field Name	Value	Description
TI_DEV_ID	TI_DEVICE_ID	0x80	Device specific ID code to identify supported ambient and junction temperature.
NVM_ID	TI_NVM_ID	0x53	Identification code for the NVM ID
FACTORY_CONFIG_2	NVM_REVISION	0x2	Identification code for the NVM revision
I2C_ADDRESS_REG	I2C_ADDRESS	0x30	I2C address

4.1.1.11.2 PMIC Enable settings

This section describes the PMIC rails that are enabled in Active and Standby state. Any rail that is disabled by default has the option to be enabled through I2C once the device is in Active state and I2C communication is available.

Enable settings in ACTIVE state:

PMIC Rail	Register Name	Field Name	Value	Description
BUCK1	ENABLE_CTRL	BUCK1_EN	0x1	Enabled
BUCK2	ENABLE_CTRL	BUCK2_EN	0x1	Enabled
BUCK3	ENABLE_CTRL	BUCK3_EN	0x1	Enabled
LDO1	ENABLE_CTRL	LDO1_EN	0x1	Enabled
LDO2	ENABLE_CTRL	LDO2_EN	0x1	Enabled
LDO3	ENABLE_CTRL	LDO3_EN	0x1	Enabled
LDO4	ENABLE_CTRL	LDO4_EN	0x1	Enabled
GPO1	GENERAL_CONFIG	GPO1_EN	0x0	The GPO1 function is disabled. The output state is low.
GPO2	GENERAL_CONFIG	GPO2_EN	0x1	The GPO2 function is enabled. The output state is Hi-Z.
GPIO	GENERAL_CONFIG	GPIO_EN	0x0	The GPIO function is disabled. The output state is low.

N.B.: LDO1 & LDO4 are not used inside the brick.

Enable settings in STBY state:

PMIC Rail	Register Name	Field Name	Value	Description
BUCK 1	STBY_1_CONFIG	BUCK1_STBY_EN	0x1	Enabled in STBY Mode
BUCK 2	STBY_1_CONFIG	BUCK2_STBY_EN	0x1	Enabled in STBY Mode
BUCK 3	STBY_1_CONFIG	BUCK3_STBY_EN	0x1	Enabled in STBY Mode
LDO 1	STBY_1_CONFIG	LDO1_STBY_EN	0x1	Enabled in STBY Mode
LDO 2	STBY_1_CONFIG	LDO2_STBY_EN	0x1	Enabled in STBY Mode
LDO 3	STBY_1_CONFIG	LDO3_STBY_EN	0x1	Enabled in STBY Mode
LDO 4	STBY_1_CONFIG	LDO4_STBY_EN	0x1	Enabled in STBY Mode
GPO 1	STBY_2_CONFIG	GPO1_STBY_EN	0x0	Disabled in STBY Mode
GPO 2	STBY_2_CONFIG	GPO2_STBY_EN	0x1	Enabled in STBY Mode
GPIO	STBY_2_CONFIG	GPIO_STBY_EN	0x0	Disabled in STBY Mode

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4.1.1.11.3 PMIC Regulators Voltage settings

This section describes how each of the PMIC power resources were configured.

BUCK Regulators settings:

PMIC Rail	Register Name	Field Name	Value	Description
Bucks Switching Mode (Global for all Buck regulators)	BUCKS_CONFIG	BUCK_FF_ENABLE	0x0	Quasi-fixed frequency mode
	BUCKS_CONFIG	BUCK_SS_ENABLE	0x0	Spread spectrum disabled
BUCK1	BUCK1_VOUT	BUCK1_VSET	0x6	0.750V
	BUCK1_VOUT	BUCK1_UV_THR_SEL	0x0	-5% UV detection level
	BUCK1_VOUT	BUCK1_BW_SEL	0x1	high bandwidth
BUCK2	BUCK2_VOUT	BUCK2_VSET	0x24	1.800V
	BUCK2_VOUT	BUCK2_UV_THR_SEL	0x0	-5% UV detection level
	BUCK2_VOUT	BUCK2_BW_SEL	0x1	high bandwidth
	BUCKS_CONFIG	BUCK2_PHASE_CONFIG	0x3	270 degrees (only applicable if Bucks are configured for fixed frequency)
BUCK3	BUCK3_VOUT	BUCK3_VSET	0x14	1.100V
	BUCK3_VOUT	BUCK3_UV_THR_SEL	0x0	-5% UV detection level
	BUCK3_VOUT	BUCK3_BW_SEL	0x1	high bandwidth
	BUCKS_CONFIG	BUCK3_PHASE_CONFIG	0x2	180 degrees (only applicable if Bucks are configured for fixed frequency)

Note:

- *When Bucks are configured for quasi-fixed frequency (BUCK_FF_ENABLE=0x0), changing the switching mode between auto-PFM and forced-PWM can be triggered by I2C (MODE_I2C_CTRL) or with one of the multi-function pins (MODE/RESET or MODE/STBY) if one of them is configured as MODE. "Forced PWM" has priority over "Auto PFM".*
- *"BUCK2_PHASE_CONFIG", "BUCK3_PHASE_CONFIG" and "BUCK_SS_ENABLE" are only applicable when the Buck regulators are configured for fixed frequency (BUCK_FF_ENABLE=0x1).*

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LDO Regulators settings:

PMIC Rail	Setting	Register Name	Field Name	Value	Description
LDO1	LDO1 output voltage	LDO1_VOUT	LDO1_VSET	0x36	3.300V
	LDO1 configuration	LDO1_VOUT	LDO1_LSW_CONFIG	0x0	Not Applicable (LDO1 not configured as loadswitch)
		LDO1_VOUT	LDO1_BYP_CONFIG	0x1	LDO1 configured as Bypass (only applicable if LDO1_LSW_CONFIG=0x0)
	LDO1 UV threshold	GENERAL_CONFIG	LDO1_UV_THR	0x0	-5% UV detection level (only applicable if configured as LDO)
LDO2	LDO2 output voltage	LDO2_VOUT	LDO2_VSET	0x5	0.850V
	LDO2 configuration	LDO2_VOUT	LDO2_LSW_CONFIG	0x0	Not Applicable (LDO2 not configured as loadswitch)
		LDO2_VOUT	LDO2_BYP_CONFIG	0x0	LDO2 configured as LDO (only applicable if LDO2_LSW_CONFIG=0x0)
	LDO2 UV threshold	GENERAL_CONFIG	LDO2_UV_THR	0x0	-5% UV detection level (only applicable if configured as LDO)
LDO3	LDO3 output voltage	LDO3_VOUT	LDO3_VSET	0x18	1.800V
	LDO3 configuration	LDO3_VOUT	LDO3_LSW_CONFIG	0x0	LDO Mode
	LDO ramp configuration	LDO3_VOUT	LDO3_SLOW_PU_RAMP	0x1	Slow ramp for powerup (~3ms)
	LDO3 UV threshold	GENERAL_CONFIG	LDO3_UV_THR	0x0	-5% UV detection level (only applicable if configured as LDO)
LDO4	LDO4 output voltage	LDO4_VOUT	LDO4_VSET	0x26	2.500V
	LDO4 configuration	LDO4_VOUT	LDO4_LSW_CONFIG	0x0	LDO Mode
	LDO ramp configuration	LDO4_VOUT	LDO4_SLOW_PU_RAMP	0x1	Slow ramp for powerup (~3ms)
	LDO4 UV threshold	GENERAL_CONFIG	LDO4_UV_THR	0x0	-5% UV detection level (only applicable if configured as LDO)

Note:

- *If a LDO is configured in bypass-mode or LSW-mode, UV-detection is not supported.*
- *If an LDO is configured in bypass-mode, the corresponding PVIN_LDOx supply must match the configured output voltage in the LDOx_VOUT register.*
- *If LDO is configured as load-switch (LSW_mode), the desired voltage does not need to be configured in the LDOx_VOUT register.*
- *In bypass- or LSW-mode, the LDO acts as a switch, where VOUT is VIN minus the drop over the FET-resistance.*
- *If LDO1 or LDO2 is configured as bypass, it allows voltage and function changes between LDO (VOUT=1.8V) and VOUT=VSET register setting. This voltage/function change can be triggered by hardware (using the VSEL_SD pin when configured as SD) or by software (VSEL_SD_I2C_CTRL).*

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4.1.1.11.4 PMIC EN / PB / VSENSE Settings

The EN/PB/VSENSE pin is used to enable or disable the PMIC. This pin can be configured in one of three ways: EN, PB or VSENSE. The table below shows the default configuration on TPS6522053.

As the FSD (First supply detection) feature is enabled, the device goes from "No Power" to "Active" state, executing the power-up sequence as soon as the voltage on V_IN is above the POR threshold. In this scenario, the EN/PB/VSENSE pin is ignored ONLY during the first power-up.

Register Name	Field Name	Value	Description
MFP_2_CONFIG	EN_PB_VSENSE_CONFIG	0x00	Device Enable Configuration
MFP_2_CONFIG	EN_PB_VSENSE_DEGL	0x0	short (typ: 120us if configured as EN or VSENSE)
MFP_2_CONFIG	PU_ON_FSD	0x1	First Supply Detection (FSD) Enabled.

4.1.1.11.5 PMIC Multi-Function pin settings

This section describes how each of the multi-function pins were configured.

Pin Name	Setting	Register Name	Field Name	Value	Description
VSEL_SD / VSEL_DDR	Function selection	MFP_1_CONFIG	VSEL_DDR_SD	0x1	VSEL pin configured as SD to set the voltage on the VSEL_RAIL
	Rail	MFP_1_CONFIG	VSEL_RAIL	0x0	LDO1
	pin polarity (only applicable if VSEL_DDR_SD=0x1)	MFP_1_CONFIG	VSEL_SD_POLARITY	0x0	LOW: 1.8V / HIGH: LDOx_VOUT register setting
MODE / STBY	function selection	MFP_2_CONFIG	MODE_STBY_CONFIG	0x2	MODE and STBY
	pin polarity	MFP_1_CONFIG	MODE_STBY_POLARITY	0x0	[if configured as MODE] LOW: auto-PFM / HIGH: forced PWM. [if configured as a STBY] LOW: STBY state / HIGH: ACTIVE state.
MODE / RESET	function selection	MFP_2_CONFIG	MODE_RESET_CONFIG	0x1	RESET
	reset selection	MFP_2_CONFIG	WARM_COLD_RESET_CONFIG	0x1	WARM RESET
	pin polarity	MFP_1_CONFIG	MODE_RESET_POLARITY	0x0	[if configured as mode] LOW: auto-PFM / HIGH: forced PWM. [if configured as RESET] LOW: reset / HIGH: normal operation.

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4.1.1.11.6 PMIC OverCurrent Deglitch settings

This section describes the default settings for the over current deglitch. When any of these registers are set (value = 1b), it enabled the long-deglitch option for the corresponding rail.

Register Name	Field Name	Value	Description
OC_DEGL_CONFIG	EN_LONG_DEGL_FOR_OC_BUCK1	0x0	Deglitch duration for OverCurrent signals for BUCK1 (High-Side Overcurrent, Low-Side Overcurrent and Low-Side Reverse/Negative OverCurrent) is ~20us
OC_DEGL_CONFIG	EN_LONG_DEGL_FOR_OC_BUCK2	0x0	Deglitch duration for OverCurrent signals for BUCK2 (High-Side Overcurrent, Low-Side Overcurrent and Low-Side Reverse/Negative OverCurrent) is ~20us
OC_DEGL_CONFIG	EN_LONG_DEGL_FOR_OC_BUCK3	0x0	Deglitch duration for OverCurrent signals for BUCK3 (High-Side Overcurrent, Low-Side Overcurrent and Low-Side Reverse/Negative OverCurrent) is ~20us
OC_DEGL_CONFIG	EN_LONG_DEGL_FOR_OC_LDO1	0x0	Deglitch duration for OverCurrent signals of LDO1 is ~20us
OC_DEGL_CONFIG	EN_LONG_DEGL_FOR_OC_LDO2	0x0	Deglitch duration for OverCurrent signals of LDO2 is ~20us
OC_DEGL_CONFIG	EN_LONG_DEGL_FOR_OC_LDO3	0x0	Deglitch duration for OverCurrent signals of LDO3 is ~20us
OC_DEGL_CONFIG	EN_LONG_DEGL_FOR_OC_LDO4	0x0	Deglitch duration for OverCurrent signals of LDO4 is ~20us

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4.1.1.11.7 PMIC MASK settings

This section describes the settings that are masked by default and the effect they have on the device state as well as the nINT pin.

	Register Name	Field Name	Value	Description
Mask effects on device state and nINT pin	MASK_CONFIG	MASK_EFFECT	0x03	no state change, nINT reaction, bit set for Faults
UV Mask	INT_MASK_UV	BUCK1_UV_MASK	0x0	un-masked (Faults reported)
	INT_MASK_UV	BUCK2_UV_MASK	0x0	un-masked (Faults reported)
	INT_MASK_UV	BUCK3_UV_MASK	0x0	un-masked (Faults reported)
	INT_MASK_UV	LDO1_UV_MASK	0x0	un-masked (Faults reported)
	INT_MASK_UV	LDO2_UV_MASK	0x0	un-masked (Faults reported)
	INT_MASK_UV	LDO3_UV_MASK	0x0	un-masked (Faults reported)
	INT_MASK_UV	LDO4_UV_MASK	0x0	un-masked (Faults reported)
Power-up retries/ attempts	INT_MASK_UV	MASK_RETRY_COUNT	0x0	Device does retry up to 2 times, then stay off
Die Temperature	MASK_CONFIG	SENSOR_0_WARM_MASK	0x0	un-masked (Faults reported)
	MASK_CONFIG	SENSOR_1_WARM_MASK	0x0	un-masked (Faults reported)
	MASK_CONFIG	SENSOR_2_WARM_MASK	0x0	un-masked (Faults reported)
	MASK_CONFIG	SENSOR_3_WARM_MASK	0x0	un-masked (Faults reported)
Masking bit to control whether nINT pin is sensitive to PushButton (PB)	MASK_CONFIG	MASK_INT_FOR_PB	0x1	masked (nINT not sensitive to any PB events)
Masking bit to control whether nINT pin is sensitive to RV (Residual Voltage)	MASK_CONFIG	MASK_INT_FOR_RV	0x0	un-masked (nINT pulled low for any RV events during transition to ACTIVE state or during enabling of rails)

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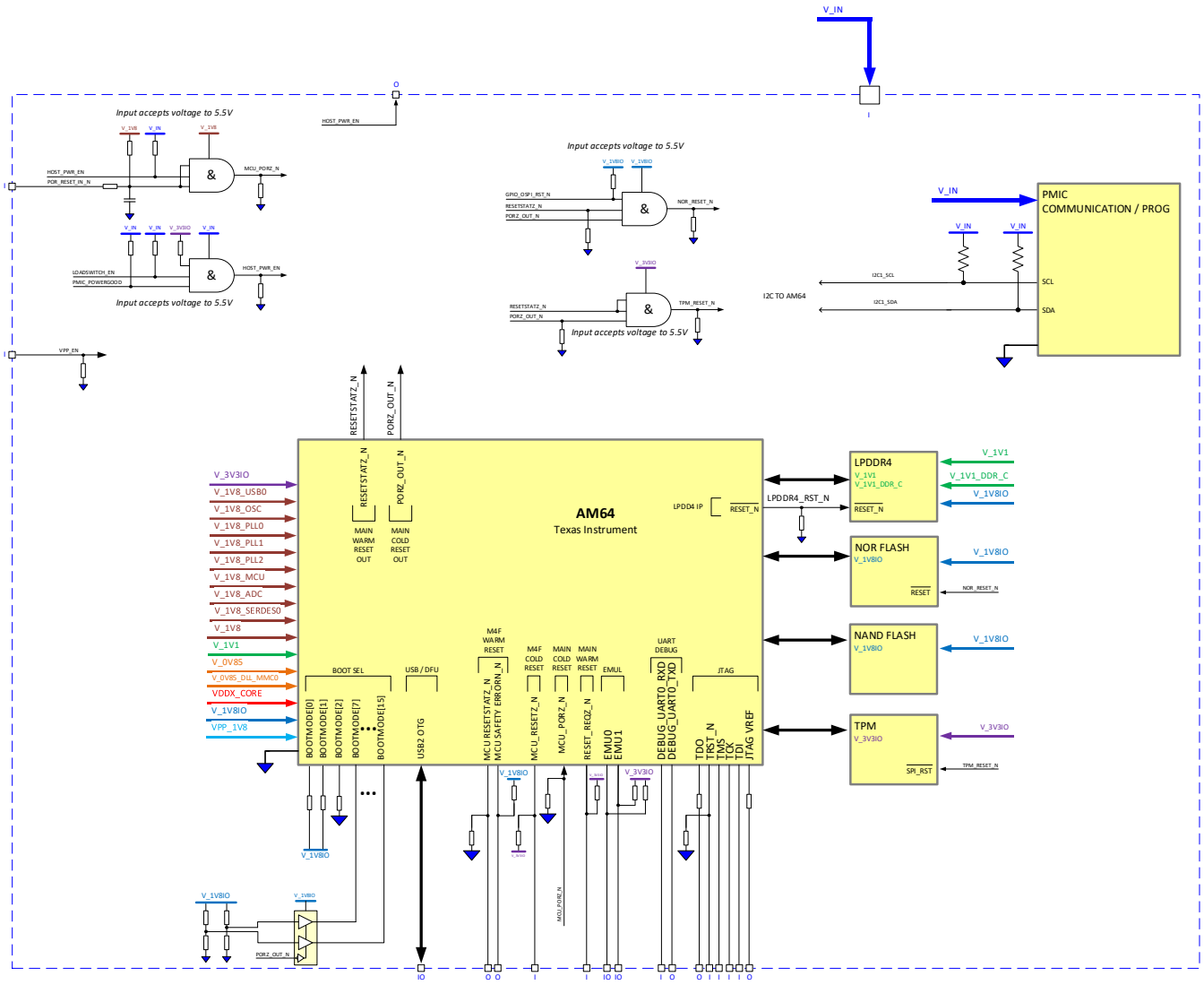
4.1.2 AM64 Reset Chain / Testability

4.1.2.1 Testability Interface



4.1.2.2 JTAG

AM64 support IEEE 1149.1 and IEEE 1149.6 interface. IEEE 1149.1 is historical standard that allow Standard test access port (i.e.: debug) and Boundary Scan feature especially in DC mode. For testing AC connections (SERDES with serial coupling capacitor for instance), IEEE 1149.6 fit this feature.
JTAG interface is enhanced with EMU0/1 debug trace signals.

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Table 13-1. JTAG Interface Signals

SignalName	I/OType[1]	Description
TRSTn	I	*Test Reset*. Initializes and disables the test interface.
TCK	I	*Test Clock*. Controls the timing of the test interface independently from any system clocks. TCK is pulsed by the equipment controlling the test and not by the tested device.
TMS	I	*Test Mode Select*. Controls the transitions of the test interface state machine.
TDI	I	*Test Data Input*. Supplies the data to the JTAG registers.
TDO	O/Z	*Test Data Output*. Used to serially output the data from the JTAG registers to the equipment controlling the test.

(1) I = Input; I/O = Input or output; O = Output; O/Z = Output or three-state

13.3.2.2 Trigger and Debug Boot Mode Interface

Table 13-2. Trigger and Debug Boot Mode Interface Signals

Signal Name	I/O Type[1]	Description
EMU0	I/O	Channel 0 trigger or boot mode select
EMU1	I/O	Channel 1 trigger or boot mode select

(1) I = Input; I/O = Input or output; O = Output; O/Z = Output or three-state

4.1.2.2.1 JTAG Debug connector

Debug interfaces include two additional signals: EMU0/EMU1 which are sampled on rising edge of MCU_PORz deassertion.

According to [REF1], the AM64 EMU0/EMU1 behaviour is:

Table 13-4. Debug Boot Modes

Sample Time	EMU1	EMU0	Boot Mode	Behavior
MCU_PORz deassertion	0	0	Reserved	Reserved for future use
	0	1	Reserved	Reserved for future use
	1	0	Wait-In-Reset (WIR)	Device will remain quiescent until a debug connection is established and the debugger releases WIR. This mode is useful for debugging boot sequences.
	1	1	Normal	Device boots normally. Debug can connect at any time but the context will be post-boot.

It will be managed outside the brick into AETHENA board BQT15769.

4.1.2.2.2 JTAG Boundary Scan (BSDL)

TI provide a BDSL description file for AM64, available on TI's website.
There are some restrictions and advice:

- `NOTE: The silicon does not support boundary scan on the mmc0_ds pad.`
- `attribute DESIGN_WARNING of AM64 : entity is`

```
   " According to simulation, BSD JTAG TAP may not work correctly unless  "&
   " device has completed RESET sequence first.                          "&
   " Forcing PORz low then release (no clock pulses required) would meet "&
   " the requirement.                                                    "&
   "                                                                     "&
   " Note that boundary scan registers with disable result WEAK1 are     "&
   " open drain type pins, which will require external pull-ups for      "&
   " test to perform correctly.                                          "&
   "                                                                     "&
   " In order to enter bscan mode correctly, TMS must be low at the      "&
   " rising edge of TRSTz and at least one cycle after TRSTz is high.    ";
```


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Into the brick there is no other BDSL component capability is available, but BSDL could we use to check pullup/down or short on AM64 pins. Furthermore, BSDL could be used also for 'pseudo-functional' test of external device, like NOR Flash or NAND Flash read/write access.

EMU0/1 are also sample on TRSTn deassertion :

Table 13-5. Boundary Scan Compliance

Sample Time	EMU1	EMU0	Boundary Scan Compliance	Behavior
TRSTn deassertion	0	1	Boundary Scan Enabled	The device's Boundary Scan TAP is connected to the device's JTAG interface.
	0	0		
	1	0	Boundary Scan Disabled	The device's SWJ-DP is connected to the device's JTAG interface.
	1	1		

Please check more information available on chap 13-3 of [REF1].

4.1.2.2.3 Layout recommendations

According to [REF2] table 7-146 :

Table 7-146. Trace Timing Conditions

PARAMETER			MIN	MAX	UNIT
OUTPUT CONDITIONS					
C_L	Output load capacitance		2	5	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(Trace\ Mismatch)}$	Propagation delay mismatch across all traces	VDDSHV3 = 1.8V		200	ps
		VDDSHV3 =3.3V		100	ps

We apply following recommendations on all JTAG + EMU0/1 signals:

	sprsp56e recommendation	BRICK SETTINGS
Max Trace Length	-	100mm
Skew inter signal (VDDSHV3=1.8V)	200ps max	100ps max
Skew inter signal (VDDSHV3=3.3V)	100ps max	
Signals single ended impedance		50Ω±10%
#vias per signal	-	4 max
Signals to noisy signal (e.g. : clock)	-	2W
Signals to quiet signal	-	2W

In our case EMU0/1 are powered by VDDSHV_MCU (3.3V), and we constraint the design to 100ps.

According to [REF2], table 6-80 EMU0/1, TCK,TDI,TMS advise to pull up this signal when used externally; it will be managed outside the brick into AETHENA board BQT15769.

N.B : TRC_DATAx traces are not supported by the brick because of not provided outside the brick.

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4.1.3 Reset Architecture

The device Power-On Reset is controlled by the external pin MCU_PORZ. This pin is driven by external Power good circuit which is the PMIC in our implementation. The MCU_PORZ pin is held low during the entire power up phase with an additional delay of 11.5 ms for the high frequency oscillator clock to stabilize.

AM6442 is divided into two separate functional reset domains, MCU reset domain and MAIN reset domain (each containing specific processing cores and peripherals).

- MCU reset domain: Managed by the MCU domain Power Sleep Controller, this includes Arm Cortex-M4F MCU Processor (M4FSS).
- MAIN reset domain: Managed by the MAIN domain Power Sleep Controller,

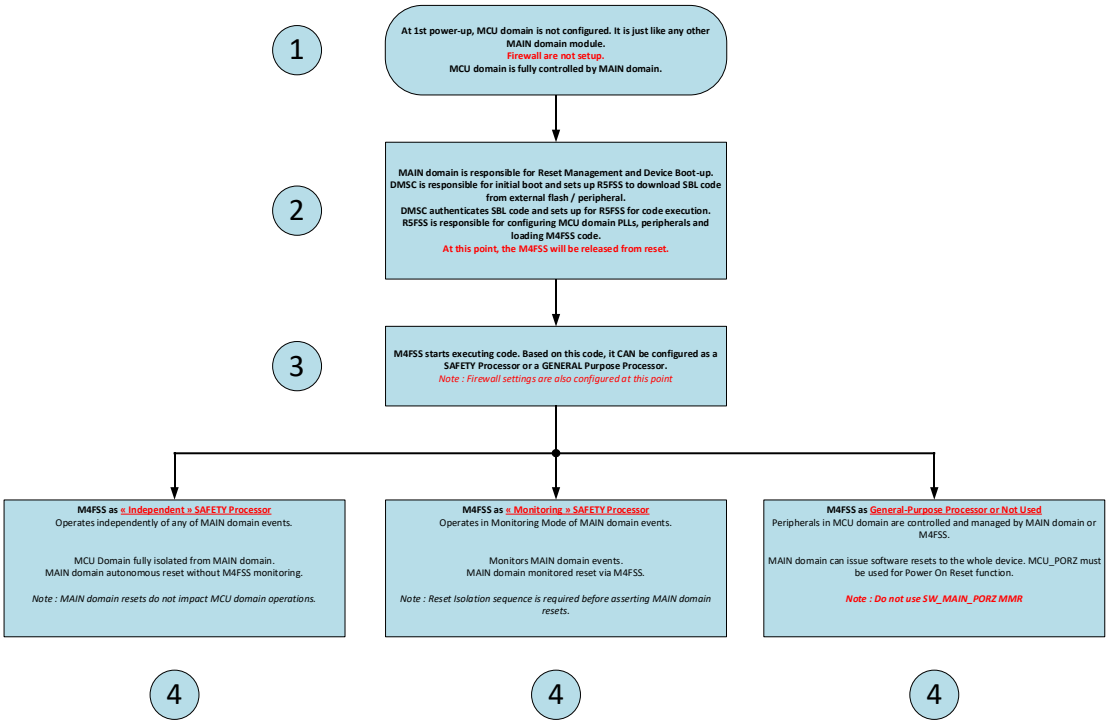
This includes:

- The high-performance application Arm Cortex-A53 cores (A53SS),
- Device management and security controller (DSMC-L),
- Real time performance Arm Cortex-R5 cores (R5FSS)
- Programmable Real-time Unit Subsystem and Industrial Communication Subsystem Gigabit (PRU_ICSSG) cores.

The MCU and MAIN domains can be configured to have independent warm reset pins via software:

- MCU_RESETZ and RESETZ_REQ.

By default, these two pins have the same effect and will act as a warm reset source for both MAIN and MCU domains. When the MCU domain is configured for reset isolation, MAIN domain resets will only reset the MAIN domain and the MCU domain will remain unaffected by all MAIN domain resets.



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4.1.3.1 MAIN domain supported resets

- Power-On Reset (POR):
  - MAIN domain software POR,

- Warm Resets :
  - RESETz_REQ device pin,
  - MAIN domain ESM error reset,
  - MAIN domain software warm reset,
  - DMSC-L warm reset,
  - DSMC-L cold reset,

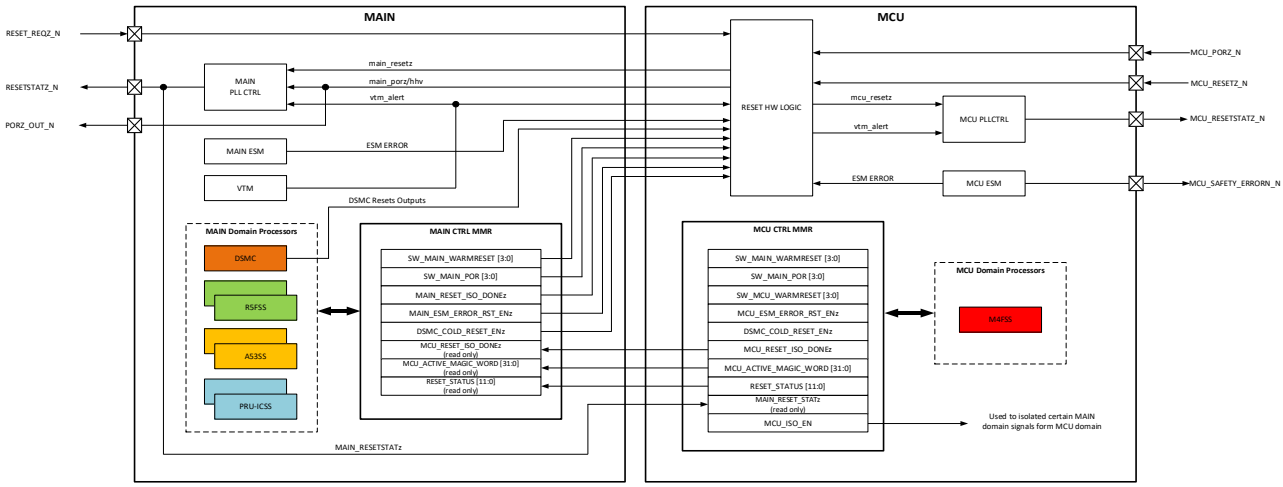
- Local module Reset:
  - MAIN domain Local Power Sleep Controller (LPSC) module local reset.

4.1.3.2 MCU domain supported resets

- Power-On Reset (POR) :
  - MCU_PORz device pin,

- Warm Resets :
  - MCU_RESETz device pin,
  - MCU domain software warm reset,
  - MCU domain ESM error reset,
  - Device Management Security Controller (DSMC-L) cold reset,

- Local module Reset :
  - MCU domain Local Power Sleep Controller (LPSC) module local reset.



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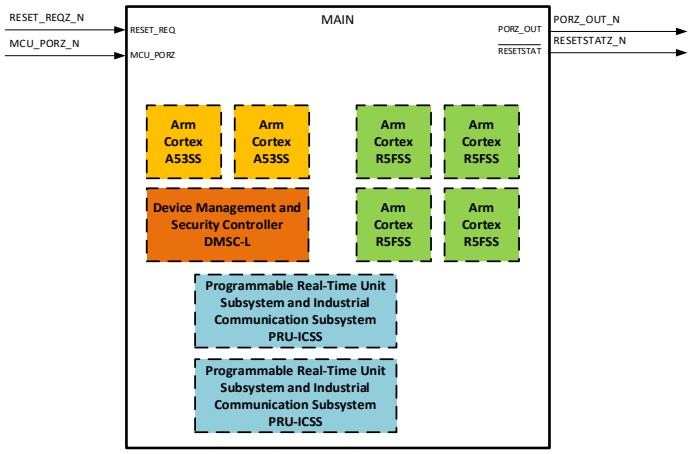
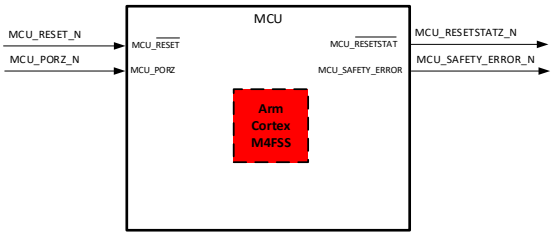
4.1.3.3 Reset sources

BRICK Reset architecture :





Note : The MCU_PORz pin located on MCU controlled the Power-On Reset of the entire SoC. Even if the independent reset configuration is enabled this pin remains the POR signal of the MAIN and MCU domains.

See below signals description.

Reset Name	Device Domain	Reset Type	Pin / Register / Internal
MCU_PORZ_N	MCU / MAIN	Hardware POR	MCU_PORz HW pin
SW_MAIN_PORz	MAIN	Software POR	Registers: CTRLMMR_RST_CTRL CTRLMMR_MCU_RST_CTRL
MCU_RESETZ_N	MCU	Hardware WARM reset	MCU_RESETz HW pin
SW_MCU_WARMRSTz	MCU	Software WARM reset	Register: CTRLMMR_MCU_RST_CTRL
RESET_REQZ_N	MAIN	Hardware WARM reset	RESETz_REQ HW pin
SW_MAIN_WARMRSTz	MCU / MAIN	Software WARM reset	Registers: CTRLMMR_RST_CTRL CTRLMMR_MCU_RST_CTRL
VTM	MCU / MAIN	Thermal reset	Internal Signal
ESM_ERORz	MCU / MAIN	ESM error reset	Registers: CTRLMMR_RST_CTRL CTRLMMR_MCU_RST_CTRL
DSMC_COLD_OUT_RST_n	MCU	DMSC-L COLD reset	Internal Signal
DSMC_WARM_OUT_RST_n	MAIN	DMSC-L WARM reset	Internal Signal

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4.1.3.4 SW_MAIN_PORz reset

This reset is a software controlled MAIN domain POR reset defined in CTRLMMR_RST_CTRL and CTRLMMR_MCU_RST_CTRL registers.
This software reset will generate a MAIN domain Power-On Reset. There are two possibilities to execute MAIN domain POR :

1. M4FSS processor will reset the MAIN domain, by writing to the CTRLMMR_MCU_RST_CTRL register,
2. MAIN domain processors will reset itself by writing to the CTRLMMR_RST_CTRL register.

CTRLMMR_MCU_RST_CTRL register :

Bit	Field	Type	Reset	Description
31 - 19	RESERVED	R	0h	Reserved
18	MCU_RESET_ISO_DONE_Z	R / W	0h	MCU can set this bit to block warm reset in the main domain which is useful when the MCU may be accessing main domain resources (peripherals, memory...). In this case, the MCU will be notified via an interrupt that there is an outstanding warm reset request for the main domain. Once notified, MCU needs to finish any outstanding operations in has with main domain resources and then clear this bit. After this bit is cleared, the main domain warm reset will unblocked and the warm reset sequence may continue. 0h - Reset of MAIN domain is not Blocked by MCU Domain 1h - Reset of MAIN domain is Blocked by MCU Domain
17	MCU_ESM_ERROR_RST_EN_Z	R / W	1h	Disable Reset of MCU by ESM 0h - Enabled 1h - Disabled
16	DMSC_COLD_RESET_EN_Z	R / W	0h	Disable Reset of MCU by DMSC 0h - Enabled 1h - Disabled
15 - 12	RESERVED	R	0h	Reserved
11 - 8	SW_MCU_WARMRST	R / W	Fh	This is a fault tolerant bitfield. Causes MCU Domain Warm Reset when set to 4'b0110, Bits will reset to 4'b1111
7 - 4	SW_MAIN_POR	R / W	Fh	This is a fault tolerant bitfield. Causes MAIN domain Power-On Reset when set to 4'b0110, Bits will reset to 4'b1111
3 - 0	SW_MAIN_WARMRST	R / W	Fh	This is a fault tolerant bitfield. Causes MAIN domain Warm Reset when set to 4'b0110, Bits will reset to 4'b1111

MCU domain effect:
- Entire MCU domain is reset isolated,
- MCU IOs are not affected.

MAIN domain effect:
- All modules in MAIN domain are reset,
- IOs will enter High-Heating-Value (High Heating Value, see associated chapter) mode while this reset is active,
- MAIN domain CTRLMMR boot configuration is reset,
- Device boot mode pins will be re-latched after this reset is de-asserted,
- Device will re-boot. During boot-up, R5FSS (secondary boot loader) will poll the CTRLMMR reset status and MCU ACTIVE MAGIC WORD registers and configure MCU domain / M4FSS processor accordingly.

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4.1.3.5 MCU_PORZ_N reset

This is the POR reset signal for the entire device, controlled by the MCU_PORz hardware pin. When LOW, it performs a POR reset on the entire device MCU and MAIN domains and puts all IOs in a safe state (Reset / HHV state).

MCU domain effect:
- All modules in the MCU domain are reset,
- MCU IOs are in High-Heating-Value state (reset state),

When MCU_PORZ_N is de-asserted, MCU IOs will enter the default state defined in the device datasheet. MCU domain will be reconfigured by the R5FSS (secondary bootloader).

MAIN domain effect:
- All modules are reset,
- MAIN IOs are in HHV state.

When MCU_PORZ_N is de-asserted, the MAIN domain IOs will enter default state as defined in the device datasheet. The R5FSS will setup M4FSS as Safety or General-Purpose processor.

It's an input without any internal defined, with specific input buffer (Fail Safe Reset = FS Reset) capability (200mV hysteresis).
We added an external 10KΩ PU, which may be lowered in case of EMC immunity issue.

4.1.3.6 RESET_REQZ_N reset

This reset signal is the MAIN domain warm reset request (Active LOW) controlled by the RESET_REQZ_N hardware pin. When LOW is detected internal reset logic generates an interrupt to processors (A53SS, R5FSS, M4FSS, DMSC-L, ICSSG) so that they can complete the reset isolation sequence before reset is propagated.

The isolation sequence isolates the MCU domain from MAIN domain so that it is protected against glitches when the MAIN domain is reset.

This sequence also ensures that reset isolated-configured modules such as PRU-ICSSG are in reset isolation before propagating the warm reset to MAIN domain.

MCU domain effect:
- Entire MCU domain is reset isolated,
- MCU IOs are not affected.

MAIN domain effect:
- This is a MAIN domain reset request. First, the reset isolation sequence is applied and then the reset is propagated. All modules in MAIN domain are reset except for reset isolated modules and MAIN domain CTRLMMR register bits which are reset only on MAIN_PORz.
- IOs are not affected,
- All processor cores are reset (A53SS, DMSC-L, R5FSS),

The reason for this reset is captured in the CTRLMMR reset source register CTRLMMR_RST_SRC. After reset is de-asserted, device will boot-up. During device boot-up, R5FSS secondary boot loader will read the reset status and MCU ACTIVE MAGIC WORD registers and reconfigure the MCU domain / M4FSS processor accordingly.

It's an input on AM64, with internal PU during and after reset.
If this input is externally unused, we putted a PU 10KΩ to manage it.
If this input is externally used, final user must manage it outside the brick.
Associated MAIN domain WARM reset sequence is described below:

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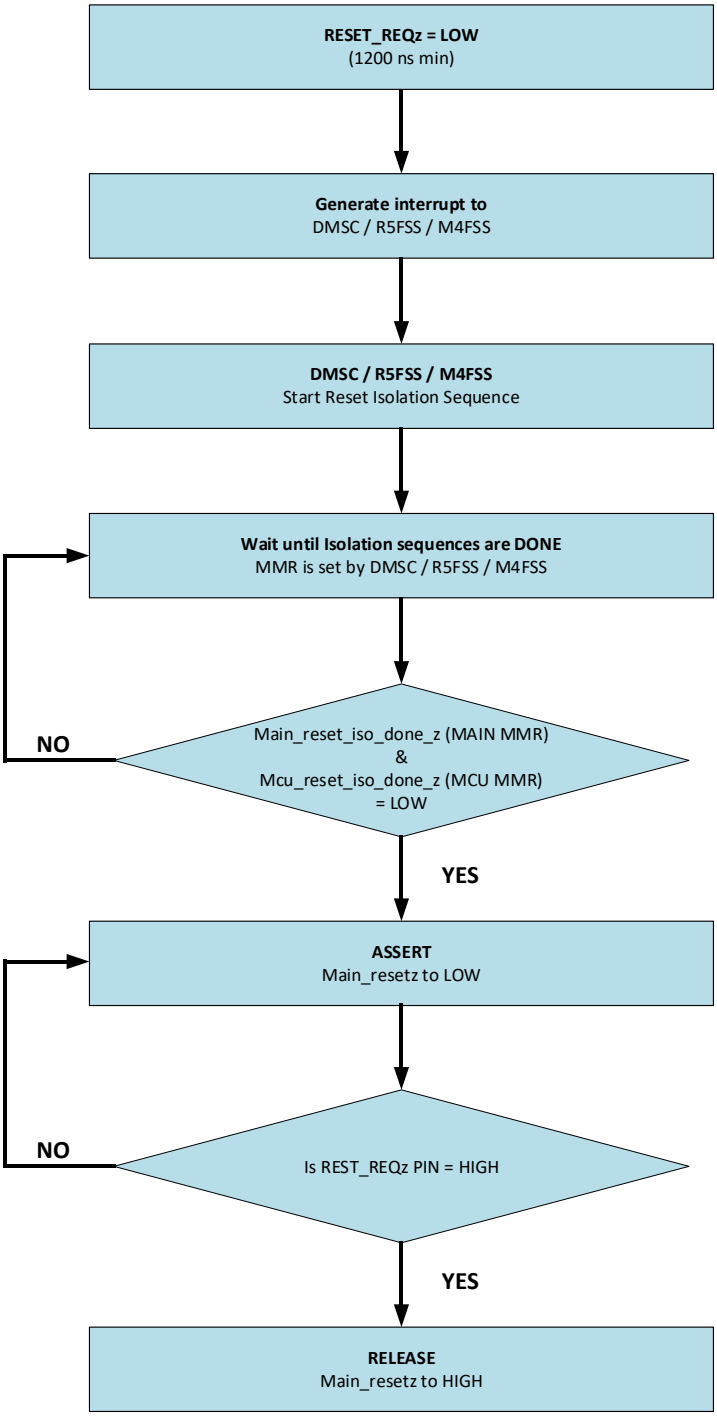
MAIN Domain Warm Reset Sequence



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4.1.3.7 SW_MAIN_WARMRSTz reset

This reset signal is software controlled MAIN domain warm reset defined in CTRLMMR_RST_CTRL and CTRLMMR_MCU_RST_CTRL registers.

The M4FSS will issue a warm reset to the MAIN domain, by writing to the MCU domain CTRLMMR register. The MAIN domain processors will issue a warm reset to the MAIN domain, by writing to the CTRLMMR MAIN domain's register.

NOTE: If end user is targeting SAFETY application by using M4FSS configured as safety processor, he must isolate the M4FSS's reset from this MAIN domain warm reset. A reset isolation sequence for MCU must be complete prior to this reset propagation.

MAIN domain CTRLMMR and MCU domain CTRLMMR registers define a 4-bit field, SW_MAIN_WARMRST[3:0] for generating a software controlled warm reset for the MAIN domain (SW_MAIN_WARMRSTz).

When SW_MAIN_WARMRST[3:0] field is set to "0110", a MAIN domain warm reset is active (SW_MAIN_WARMRSTz = LOW). When SW_MAIN_WARMRST[3:0] is set to any other value, the MAIN domain warm reset is inactive (SW_MAIN_WARMRSTz = HIGH). This bit field is reset to "1111" (Inactive State) by default.

NOTE: This software reset is equivalent to MAIN_RESET_REQz reset signal (RESET_REQz hardware pin) functionality.

MCU domain effect:
- Entire MCU domain is reset isolated,
- MCU IOs are not affected.

MAIN domain effect:
- This is a MAIN domain reset request. First, the reset isolation sequence is applied and then the reset is propagated.
- All modules in MAIN domain are reset except for reset isolated modules and MAIN domain CTRLMMR register bits which are reset only on MAIN_PORz.
- IOs are not affected,
- All processor cores are reset (A53SS, DMSC-L, R5FSS),

The reason for this reset is captured in MAIN domain CTRLMMR reset status register CTRLMMR_RST_STAT. After reset is de-asserted, device will boot-up. During device boot-up, R5FSS (secondary boot loader) will read the reset status and MCU ACTIVE MAGIC WORD registers and reconfigure the MCU domain/M4FSS processor accordingly.

4.1.3.8 MCU_RESETZ_N reset

The MCU_RESETZ_N signal is the warm reset input (active low) to the entire device, controlled by the MCU_RESETZ hardware pin. When active, it resets all modules in the MCU and MAIN domains. MCU_RESETZ will not reset selected CTRLMMR_RST_CTRL and CTRLMMR_MCU_RST_CTRL register bits.

These bits are only reset by MCU_PORZ_N. MCU Domain Effect All modules in MCU domain are reset except for modules and CTRLMMR_MCU_RST_CTRL bits which are reset only on MCU_PORZ_N. IOs are not affected. M4FSS is reset. When MCU_RESETz is de-asserted, the MCU domain needs to be reconfigured by R5FSS (secondary boot loader) in the MAIN domain.

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MAIN Domain effect: All modules in the MAIN domain are reset except for modules and CTRLMMR bits which are reset only on MAIN_PORz. IOs are not affected. All processor cores are reset (A53SS, DMSC-L, and R5FSS). When MCU_RESETz is de-asserted, the device goes through full boot.
The reason for this reset is captured in the CTRLMMR reset source register CTRLMMR_RST_SRC. During device boot-up, the R5FSS (secondary boot loader) will read the CTRLMMR reset status and MCU ACTIVE MAGIC WORD registers and reconfigure the MCU domain/M4FSS processor accordingly.

It's an input which is internally pulled up, in case of EMC immunity issue the external PU of 10KΩ may be lowered.

4.1.3.9 MCU_RESETSTATZ_N

This pin indicates internal MCU_RESETZ_N reset status (active LOW). When LOW, it indicates that the device, both MCU and MAIN domains, are in internal reset state. When HIGH, it indicates that the device, both MCU and MAIN domains, are out of internal reset state.

NOTE : In order for the MAIN domain to come out of reset, RESET_REQZ_N (RESET_REQz hardware pin) must also be de-asserted.

During and after reset, this pin is not PD/PU. This is externally PD with 10KΩ, it is not needed to active internal PD/PU of AM64.

4.1.3.10 SW_MCU_WARMRSTz reset

This is a software MCU domain warm reset defined in MCU domain CTRLMMR. CTRLMMR defines a 4-bit field, SW_MCU_WARMRST[8:11] for generating a software warm reset in the MCU domain (SW_MCU_WARMRSTz).

When SW_MCU_WARMRST[8:11] field is set to "0110", MCU warm reset is active (SW_MCU_WARMRSTz = LOW).

When SW_MCU_WARMRST[8:11] is set to any other value, MCU warm reset is inactive (SW_MCU_WARMRSTz = HIGH). This bit field is reset to "1111" (Inactive State) by default.

NOTE : This reset is equivalent to MCU_RESETZ_N warm reset signal (MCU_RESETz hardware pin) functionality.

MCU domain effect:
- All modules in the MCU domain are reset except for modules and MCU domain CTRLMMR bits which are reset on MCU_PORZ_N,
- IOs are not affected,
- M4FSS processor is reset.

When MCU_RESETZ_N is de-asserted, the device goes through full boot. The reason for this reset is captured in CTRLMMR reset source register CTRLMMR_RST_SRC.

During device boot-up, the R5FSS (secondary boot loader) will read the CTRLMMR reset status and MCU ACTIVE MAGIC WORD and reconfigure the MCU domain / M4FSS processor accordingly.

4.1.3.11 RESETSTATZ_N (MAIN_RESETSTATZ)

This signal is driven by AM64 in order reset PMIC default value (in case of Digital Voltage Scaling for example… but not supported by AM64).

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There is no AM64 internal PU/PD for this signal (during, after reset state), so according to TI EVM SK => PD 10KΩ, it's pull downed by 10KΩ.

4.1.3.12 PORZ_OUT_N

Is driven low during and after reset without any PU/PD. PD with 1K externally for safety/EMC reasons it's PD strongly to prevent tri state buffer of Bootmode on NAND bus during normal operation.

4.1.3.13 HOST_PWR_EN

It's a brick output with 10kΩ PD which can be used externally to enable power up companion chip.

4.1.3.14 POR_RESET_IN_N

It's a brick input, with PU 10kΩ and small RC filtering.

4.1.3.15 DMSC-L resets

4.1.3.15.1 DMSC_COLD_OUT_RST_n MAIN reset

The DMSC-L will issue this reset upon a security error. When this reset is enabled in MAIN domain warm reset. This is an asynchronous type, it takes effect immediately.

NOTE: This reset behavior is same as the RESET_REQZ_N reset signal (RESET_REQz hardware pin).

MCU domain effect:
- Entire MCU domain is reset,
- MCU IOs are not affected.

MAIN domain effect:

This is a MAIN domain reset request. First, the reset isolation sequence is applied and then the reset is propagated.

- All modules in MAIN domain are reset except for reset isolated modules and CTRLMMR register bits which are reset only on MAIN_PORz,
- IOs are not affected,
- All processors cores are reset (A53SS, DSMC-L, R5FSS).

The reason for this reset is captured in CTRLMMR reset status register. After reset is de-asserted, device will boot-up. During device boot-up, R5FSS (secondary boot loader) will read the reset status and MCU ACTIVE MAGIC WORD registers and reconfigure the MCU domain / M4FSS processor accordingly.

4.1.3.15.2 DMSC_WARM_OUT_RST_n MAIN reset

This is a MAIN domain warm reset that is executed from the DMSC-L. This is an asynchronous reset type; it takes effect immediately.

MCU domain effect:
- Entire MCU domain is reset isolated,
- MCU IOs are not affected.

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MAIN domain effect:

This is a MAIN domain reset request. First the reset isolation sequence is applied and then the reset is propagated.

- All modules in MAIN domain are reset except for modules and MAIN domain CTRLMMR registers bits which are reset only on MAIN_PORz.
- IOs are not affected,
- All processor cores are reset (A53SS, DMSC-L, R5FSS).

The reason of this reset is captured in CTRLMMR reset source status register CTRLMMR_RST_SRC. After reset is de-asserted, device will boot-up. During boot-up, R5FSS (secondary boot loader) will read the reset status and MCU ACTIVE MAGIC WORD registers and reconfigure the MCU domain / M4FSS processor accordingly.

4.1.3.15.3 DMSC_COLD_OUT_RST_n MCU reset

The device DMSC-L will issue this reset upon a security error. When this reset is enabled in MCU domain, it causes a whole device warm reset. This DSMC-L reset of the MCU domain is enabled only when the DSMC_COLD_RESET_ENz bit in the MCU domain CTRLMMR is 0.

When the M4FSS is configured as a safety processor, it can block this reset from resetting the MCU domain. This is an asynchronous reset type; it takes effect immediately.

NOTE: This reset behavior is same as MCU_RESETz reset signal (MCU_RESETz hardware pin).

MCU domain effect:

- All modules in MAIN domain are reset except for modules and MAIN domain CTRLMMR registers bits which are reset only on MCU_PORZ_N,
- IOs are not affected,
- M4FSS is reset,

When the MCU_RESETZ_N is de-asserted, the MCU domain will be configured by R5FSS (secondary boot loader) in the MAIN domain.

MAIN domain effect:

- All modules in the MAIN domain are reset except for modules and CTRLMMR bits which are reset only on MAIN_PORz,
- IOs are not affected,
- All processor cores are reset (A53SS, DSMC-L, R5FSS).

When MCU_RESETZ_N is de-asserted, the device goes through full boot. The reason for this reset is captured in CTRLMMR reset source register CTRLMMR_RST_SRC.

During device boot-up, the R5FSS (secondary boot loader) will read the CTRLMMR reset status and MCU ACTIVE MAGIC WORD and reconfigure the MCU domain / M4FSS processor accordingly.

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4.1.4 VTM Thermal Alert reset

The internal VTM module outputs an alert signal (THERM_MAXTEMP_OUTRANGE_ALERT) when the device temperature goes beyond a maximum threshold. This reset signal creates a MCU domain WARM reset.

VTM alert will be active as long as the error condition is true (Device temperature > Maximum temperature threshold). When the error goes away, VTM alert will be de-asserted and device will come out of warm reset.

This signal, when asserted high will cause warm reset similar to MCU_RESETz.

MCU domain effect:

- All modules in MCU domain are reset except for modules and MCU domain CTRLMMR bits which are reset only on MCU_PORz,
- IOs are not affected,

This reset is active as long as the VTM alert is active.

When THERM_MAXTEMP_OUTRANGE_ALERT is de-asserted, the MCU domains needs to be reconfigured by R5FSS (secondary bootloader) in the MAIN domain.

MAIN domain effect:

- All modules in the MAIN domain are reset except for modules and CTRLMMR bits which are reset only on MAIN_PORz,
- IOs are not affected,
- All processor cores are reset A53SS, DSMC-L and R5FSS.

When THERM_MAXTEMP_OUTRANGE_ALERT is de-asserted, the device goes through full initialization procedure. The reason for this reset is captured in the CTRLMMR reset source register CTRLMMR_RST_SRC.

4.1.4.1.1 VTM alert use-case example

VTM sends out a warning signal before generating the MAX Temp Alert. There are 2 different threshold settings for max temperature limits.

The first one has a lower threshold which will generate an interrupt to the processor for taking action to reduce frequency, turn-off power domains, etc. This should eventually lower the temperature and avoid the Max Temp Alert.

If the interrupt does not fix the rising temperature, then the VTM will issue a Max Temp Alert. This will cause a device warm reset. The VTM Max Temp Alert will be active as long as the die temperature is above the programmed threshold.

Device warm reset will default certain power domains to off mode (default at power-up). Software can read the reset status register to poll on the cause of the warm reset. If it is from VTM, then it can wait for additional time before turning on the power domains.

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4.1.5 MAIN ESM_ERRORz reset

This reset issued when a MAIN domain processor (A53SS, DSMC-L and R5FSS) detects a catastrophic software error or a MAIN domain Watchdog timeout event occurs.

Errors in the MAIN domain cause the MAIN ESM module to trigger ESM_ERRORz. This is routed as an internal MAIN domain warm reset when enabled by the MAIN domain CTRLMMR reset control bit MAIN_ESM_ERROR_RST_ENz. This is an asynchronous reset type, it takes effect immediately.

MCU domain effect:

- Entire MCU domain is reset isolated,
- MCU IOs are not affected.

MAIN domain effect:

- All modules in MAIN domain are reset except for reset isolated modules and MAIN domain CTRLMMR bits which are reset only on MAIN_PORz,
- IOs are not affected,

The device will re-boot. During boot-up, R5FSS (secondary boot loader) will poll the CTRLMMR reset registers and reconfigure the MCU domain / M4FSS processor accordingly.

If the device boot fails, and the MCU_SAFETYU_ERRORn level is still LOW, then the device is frozen in this state and need an external device or action to issue the MCU_PORz reset to allow the device to recover from this error.

4.1.6 MCU ESM_ERRORz (MCU_SAFETY_ERRORN)

This reset is issued when the M4FSS detects a catastrophic safety error or a MCU watchdog timeout occurs. Errors in the MCU domain cause the MCU ESM module to trigger ESM_ERRORz. This is routed as a device warm reset then enabled by the MCU domain CTRLMMR bit (MCU_ESM_ERROR_RST_ENz).

This is an asynchronous reset type (takes effect immediately).

MCU domain effect:

- All modules in MCU domain are reset except for reset isolated modules and MCU domain CTRLMMR bits which are reset only on PORz,
- IOs are not affected.

Error is reported on MCU_SAFETY_ERRORN_N pin. When SAFETY_ERROR_RST_n is de-asserted, the MCU domain needs to be reconfigured by the R5FSS (secondary boot loader) in the MAIN domain.

This pin is pull down internally during and after reset and can be optionnaly reconfigured by firmware. We need to add an external PD because this signal is outputted outside the brick.

External hardware (PMIC or secondary MCU safety channel) must issue MCU_PORZ_N to recover from this error.

MAIN domain effect:

- All modules in MAIN domain are reset except for reset isolated modules and MAIN domain CTRLMMR bits which are reset only on PORz,
- IOs are not affected.

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Device will re-boot. During boot-up, the R5FSS (secondary boot loader) will poll the CTRLMMR reset source register and configure the MCU domain/M4FSS processor accordingly.

If the device boot fails, and MCU_SAFETY_ERRORN_N level is still LOW, then an external safety device should issue the MCU_PORZ_N reset to allow the device to recover from the error.

According to [REF2], table 6-80 MCU_SAFETY_ERRORN_N advise to pull down this signal when used externally; it will be managed outside the brick into AETHENA board BQT15769.

4.1.7 High Heating Value reset

IOs support HHV mode during power up. HHV is defined as a state when MCU_PORZ_N signal is driven LOW. HHV allows IO cells to be tri-stated. All IO cells have HHV which is asserted (driven) by HHV generated during MCU_PORZ_N assertion.

There are default pull values during this HHV/ MCU_PORZ_N assertion specified in the device Datasheet for each pin.

All HHV logic controlling the buffer high-impedance and the associated default pull value will be asynchronous.

This diagram demonstrates the timing sequence for the device HHV signals.

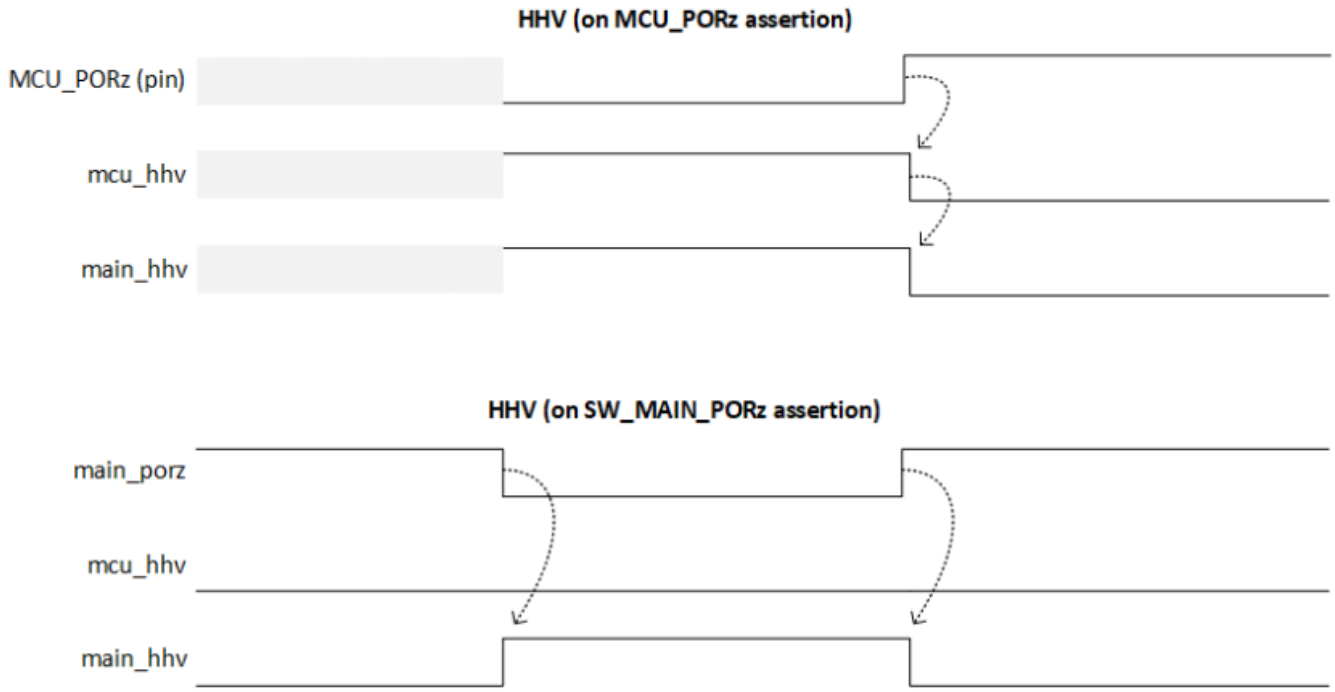

Figure 5-483. HHV Timing Diagram

Extract from [REF1]

BRICK does not implement High Heating Value (HHV) function.

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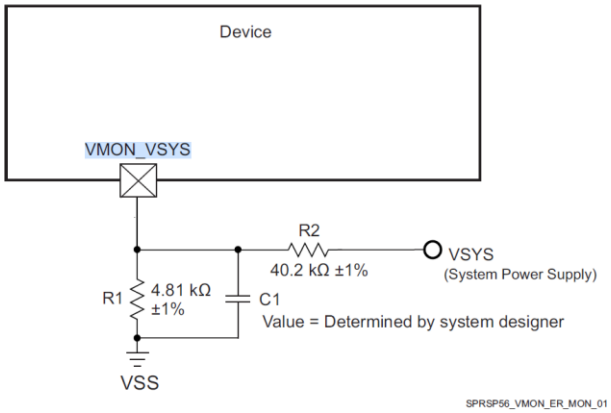
4.1.8 VMON_VSYS

This input allows to monitor external voltage, like incoming system voltage.
The voltage range is about [0V..1V] with a threshold of 0.45V ±3%.
The input leakage current is about 10nA up to 2.5µA so external bridge resistor has to manage that leakage.

5V input monitoring example with -10% trip point:



This allows to detect a trip point from 4.013V to 4.517V (more details into [REF2]).

Please find below formulas for monitoring 3.3V/5V/12V/24V:

R1 value	R1 precision	**R1 real**	R2 value	R2 precision	**R2 real**	Threshold value	Threshold precision	**Threshold real (V)**	**Input Leakage current (A)**	**VSYS Thresholds (V)**	Trip Point	
4810	-1%	**4761,90**	40200	1%	**40602,00**	0,45	3%	**0,4635**	**2,50E-06**	**4,5170**	5V-10%=	4,5
4810	1%	**4858,10**	40200	-1%	**39798,00**	0,45	-3%	**0,4365**	**0**	**4,0123**		
4810	-1%	**4761,90**	24900	1%	**25149,00**	0,45	3%	**0,4635**	**2,50E-06**	**2,9743**	3,3V-10%=	2,97
4810	1%	**4858,10**	24900	-1%	**24651,00**	0,45	-3%	**0,4365**	**0**	**2,6514**		
1870	-1%	**1851,30**	40200	1%	**40602,00**	0,45	3%	**0,4635**	**2,50E-06**	**10,7303**	12V-10%=	10,8
1870	1%	**1888,70**	40200	-1%	**39798,00**	0,45	-3%	**0,4365**	**0**	**9,6343**		
4700	-1%	**4653,00**	204700	1%	**206747,00**	0,45	3%	**0,4635**	**2,50E-06**	**21,5751**	24V-10%=	21,6
4700	1%	**4747,00**	204700	-1%	**202653,00**	0,45	-3%	**0,4365**	**0**	**19,0710**		
4700	-1%	**4653,00**	39500	1%	**39895,00**	0,45	3%	**0,4635**	**2,50E-06**	**4,5373**	5V-10%=	4,5
4700	1%	**4747,00**	39500	-1%	**39105,00**	0,45	-3%	**0,4365**	**0**	**4,0323**		

Please check [REF2] table 6-80 when VMON_VSYS is unused.

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4.1.9 Power Rail Decoupling

This first approach allows to estimate roughly the decoupling needed for each power rails. It's not a precise enough to qualify a design which must be simulated with a power integrity tool in the end.
We assumed that all power deliverers are considered as almost perfect, i.e.: there is no remaining ripple even at high load.
The aim is estimated the behavior of decoupling scheme from the point of view of the sink.

Methodology:

1. Estimate max power consumption with all related interface enabled ([REF3])
2. Estimate max allowable power supply ripple
3. Calculate equivalent max current consumption
4. Calculate equivalent Ztarget with frequency domain range applied
5. Try to stay below Ztarget in frequency domain range using AM64xx Core Design Decoupling.xlsm

4.1.9.1 Max power consumption

All processors run at full frequency, loaded at 100%, all relevant interfaces (PCIe/USB2.0/RGMII/SDcard/EMMC/DDR/…) also running at 100%, T_{jmax} reached: 105°C

	Static Fields
	Calculated Power Outputs

Operating Performance Point (OPP)	
MPU A530/1 Frequency (MHz)	1000
MCU R5F0/1 Frequency (MHz)	800
MCU R5F2/3 Frequency (MHz)	800
MCU M4F Frequency (MHz)	400
ICSSG Frequency (MHz)	333

Processor Core Utilization (%)	
MPU-A530	100%
MPU-A531	100%
MCU-R5F0	100%
MCU-R5F1	100%
MCU-R5F2	100%
MCU-R5F3	100%
MCU-M4F	100%
PRU-ICSSG0	100%
PRU-ICSSG1	100%
Security Accelerator	100%

LVCMOS IO	Mode	IO Utilization (%)
MCU UART	12Mbps	100%
MCU UART	12Mbps	100%
MCU SPI	Master, 25Mbd	100%
MCU SPI	Master, 25Mbd	100%
ICSSG0	Dual Port RGMII 1Gbps	100%
ICSSG1	Dual Port RGMII 1Gbps	100%
Ethernet (CPSW) Port 0	RGMII 1Gbps	100%
OSPI	QSPI SDR 133Mbd	100%
GPMC	GPMC 8b 75 MHz	100%

Peripherals	Mode	Utilization (%)
DDR Type/Rate	LPDDR4 1600	100%
DDR WR %	100%	-
High Speed IO	PCIe G2	100%
USB2	3.3V on	100%
SD card	HS200	100%
eMMC	HS200	100%
ADC	on	-

Estimated Power		
Power Supply	Voltage (V)	Power (W)
VDD_CORE	0,75	1,707
VDDAR_CORE	0,85	0,131
VDDA_1V8	1,8	0,076
VDD_DDR4 (without DIMM)	1,1	0,229
SOC_DVDD1V8	1,8	0,057
SoC_DVDD3V3	3,3	0,528
Total		2,729

General	
Junction Temperature (°C)	105
Power Estimation Mode	Max

Note: This power estimation spreadsheet provides power consumption estimat measured and simulated data; they are provided "as is" and are not guaranteed specified precision. Power consumption depends on electrical parameters, silic variations, environmental conditional and use cases running on the processor d operation. Actual power consumption should be verified in the real system.

4.1.9.2 Voltage Ripple

First of all, check min/max power supply supported by AM64xx (from all sinks:AM64 have most restrictive voltage tolerance, so it guides the whole Z_{TARGET})

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Powered by	Chip Power rail name	Voltage (Volt)	Voltage Tolerance (Volt)		Voltage Tolerance (%)	
		Typ	Min	Max	Min	Max
VDDX_CORE	VDD_CORE	0,75	0,715	0,79	-4,7%	5,3%
V_0V85	VDDAR_CORE	0,85	0,81	0,895	-4,7%	5,3%
V_1V8	VDDA_1V8	1,8	1,71	1,89	-5,0%	5,0%
V_1V1	VDDS_DDR4	1,1	1,06	1,17	-3,6%	6,4%
V_1V8IO	SOC_DVDD1V8	1,8	1,71	1,89	-5,0%	5,0%
V_3V3IO	SOC_DVDD3V3	3,3	3,135	3,465	-5,0%	5,0%
VPP_1V8	VPP_1V8	1,8	1,71	1,89	-5,0%	5,0%

(data extracted from [REF2])

Then check voltage tolerances provided by PMIC & TLV75518.

These power supplies are provided by PMIC TPS6522053 which have its own output tolerances @ respective I_{OUT_MAX}:

PMIC output	Chip Power rail name	Voltage (Volt)	Voltage Tolerance (Volt)		Voltage Tolerance (%)	
		Typ	Min	Max	Min	Max
BUCK1	VDD_CORE	0,75			-1,5%	1,5%
LDO2	VDDAR_CORE	0,85	-0,011	0,011	-1,3%	1,3%
LDO3	VDDA_1V8	1,8			-1,1%	1,1%
BUCK3	VDDS_DDR4	1,1			-1,5%	1,5%
BUCK2	SOC_DVDD1V8	1,8			-1,5%	1,5%
pmic input	SOC_DVDD3V3	3,3			-2,0%	2,0%
TLV75518	**Chip Power rail name**	**Voltage (Volt)**	**Voltage Tolerance (Volt)**		**Voltage Tolerance (%)**	
		Typ	Min	Max	Min	Max
	VPP_1V8	1,8	1,71	1,89	-1,2%	1,2%

(data extracted from [REF5])

In the end, calculate a moderated ripple voltage margin:

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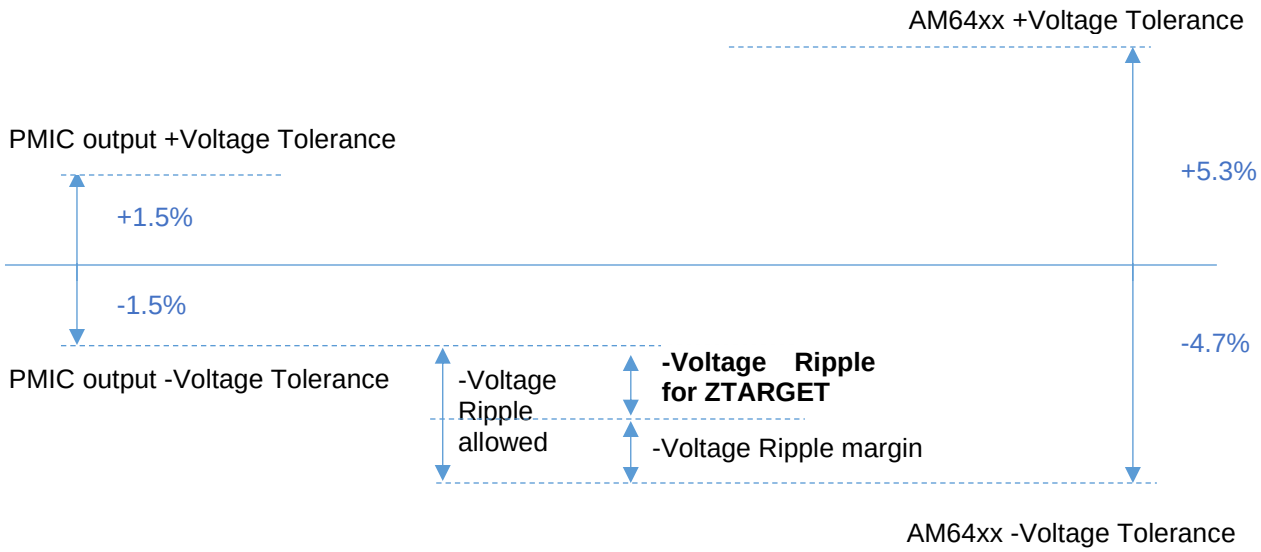

VDD_CORE Example

- VDD_CORE, let's consider that PMIC output is perfectly filtered, there is no intrinsic ripple voltage. So voltage ripple allowable would be: -4.7%-(-1.5%) =-3.2% With a margin /2, Voltage Ripple for Z_{TARGET} become -1.6%
- VDDAR_CORE, allowable ripple would be -4.7%-(-1.3%) =-3.4% => Voltage Ripple for Z_{TARGET} become -1.7%
- VDDA_1V8, allowable ripple would be -5%-(-1.1%) =-3.9% => Voltage Ripple for Z_{TARGET} become -1.95%
- VDDS_DDR4, allowable ripple would be -3.6%-(-1.5%) =-2.1% => Voltage Ripple for Z_{TARGET} become -1.05%
- SOC_DVDD1V8, allowable ripple would be -5%-(-1.5%) =-3.5% => Voltage Ripple for Z_{TARGET} become -1.75%
- SOC_DVDD3V3, allowable ripple would be -5%-(-2%)=-3% => Voltage Ripple for Z_{TARGET} become -1.5% arbitrary (it miss 3V3 output tolerance)
- VPP_1V8, allowable ripple would be -5%-(-1.2%)=-3.8% => Voltage Ripple for Z_{TARGET} become -1.9%

4.1.9.3 Ztarget

Most of manufacturers define Z_{TARGET} as:

$$Z_{TARGET} = \left[\frac{Voltage\ Rail \times \frac{\%\ Ripple}{100}}{Maximum\ Dynamic\ Current} \right]$$

According tosprac76e_Sitara™ Processor Power Distribution Networks.pdf, Texas Instrument define Z_{TARGET} as:

$$Z_{TARGET} = \frac{\text{Voltage Rail} \times \%\text{Ripple}}{0.5 \times \text{IMax}}$$

Where Z_{TARGET} is elaborated with a variation of 50% of Imax current to respect requested ripple voltage margin.

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Z Target for AM64						
Power Supply Rail name	Voltage Rail	% Ripple	Pmax	Imax (A)	Ztarget (ohm)	Ztarget selected (ohm)
VDD_CORE	0,75	1,6%	1,7	2,27	0,011	0,011
VDDAR_CORE	0,85	1,9%	0,131	0,15	0,210	0,030
VDDA_1V8	1,8	2,0%	0,076	0,04	1,663	0,100
VDD_DDR	1,1	1,0%	0,665	0,60	0,036	0,030
SOC_DVDD1V8	1,8	1,8%	0,057	0,03	1,989	0,050
SOC_DVDD3V3	3,3	1,5%	0,528	0,16	0,619	0,050
VPP_1V8	1,8	1,9%		0,40	0,171	0,100

4.1.9.4 Decoupling VDD_CORE (V_0V75)

xPERSO1	HUA43319	HUA15709	TME00744	HUA25833	HUA42895	HUA31098	TME03438	1CAP005642	10N25V0201
47uF	22uF	10uF	4,7uF	1uF	470nF	220nF	100nF	47nF	10nF
6,3V	10V	10V	10V	10V	10V	16V	6,3V	10V	25V
X7R	X5R	X7R	X5R	X7R	X7R	X7R	X5R	X7R	X7R
10,00%	20,00%	10,00%	10,00%	10,00%	10,00%	10,00%	10,00%	10,00%	10,00%
#1 actual	#2 actual	#3 actual	#4 actual	#5 actual	#6 actual	#7 actual	#8 actual	#9 actual	#10 actual
0,92	0,93	1,06	0,95	1,13	1,11	1,04	0,96	1,03	0,99
43,016E-06	20,350E-06	10,550E-06	4,453E-06	1,128E-06	519,350E-09	229,831E-09	96,476E-09	48,410E-09	9,940E-09
928,032E-12	928,032E-12	919,941E-12	838,555E-12	928,032E-12	838,555E-12	838,555E-12	757,704E-12	838,555E-12	757,704E-12
3,000E-03	20,000E-03	4,000E-03	16,000E-03	14,802E-03	20,000E-03	21,278E-03	30,000E-03	10,000E-03	70,000E-03
	1		1	2	2	3	8		
2	2	2	2	2	2	2	2	2	2
1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09
400	400	400	400	400	400	400	400	400	400
1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12
2,046E-09	2,046E-09	2,038E-09	1,956E-09	2,046E-09	1,956E-09	1,956E-09	1,875E-09	1,956E-09	1,875E-09
xPERSO1	HUA43319	HUA15709	TME00744	HUA25833	HUA42895	HUA31098	TME03438	1CAP005642	10N25V0201

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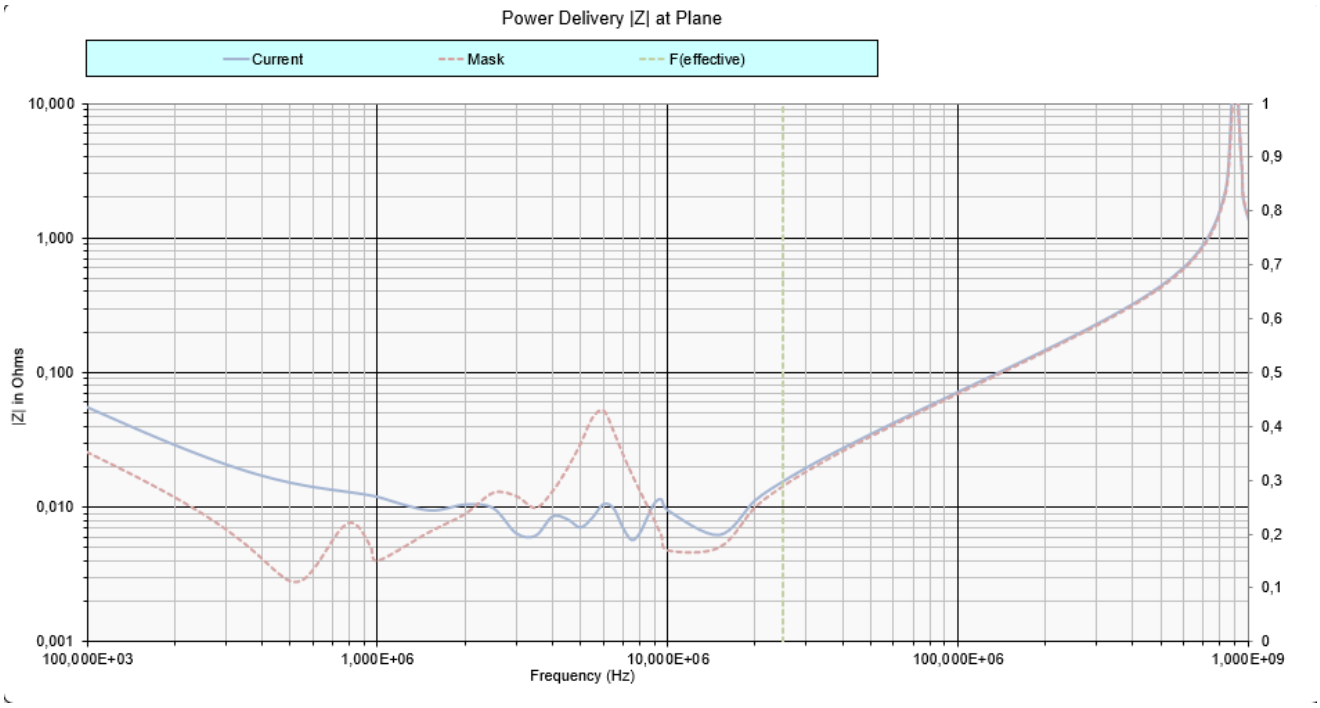
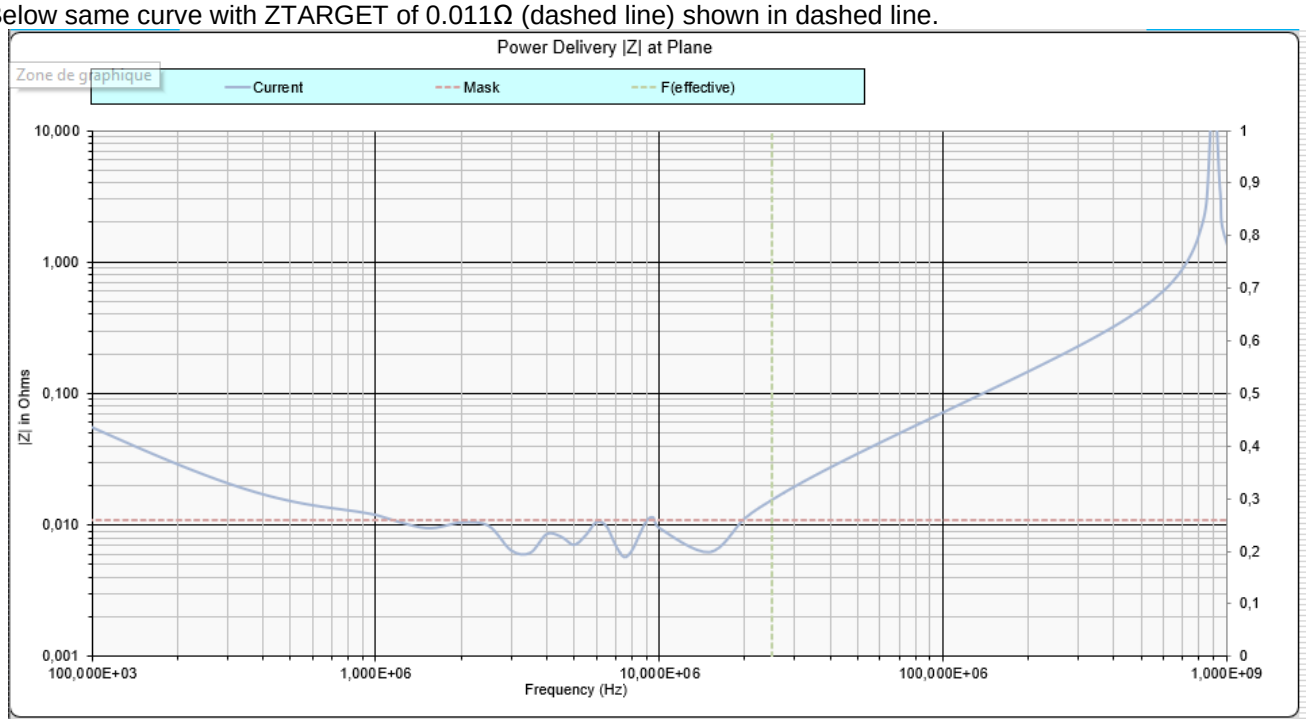
Let's compare EVM SK rev2 (dashled trace) vs our proposal (blue trace), with a Z_{TARGET} of 0.011Ω:



Below same curve with ZTARGET of 0.011Ω (dashed line) shown in dashed line.



In this behavior it seems that we've improved decoupling.

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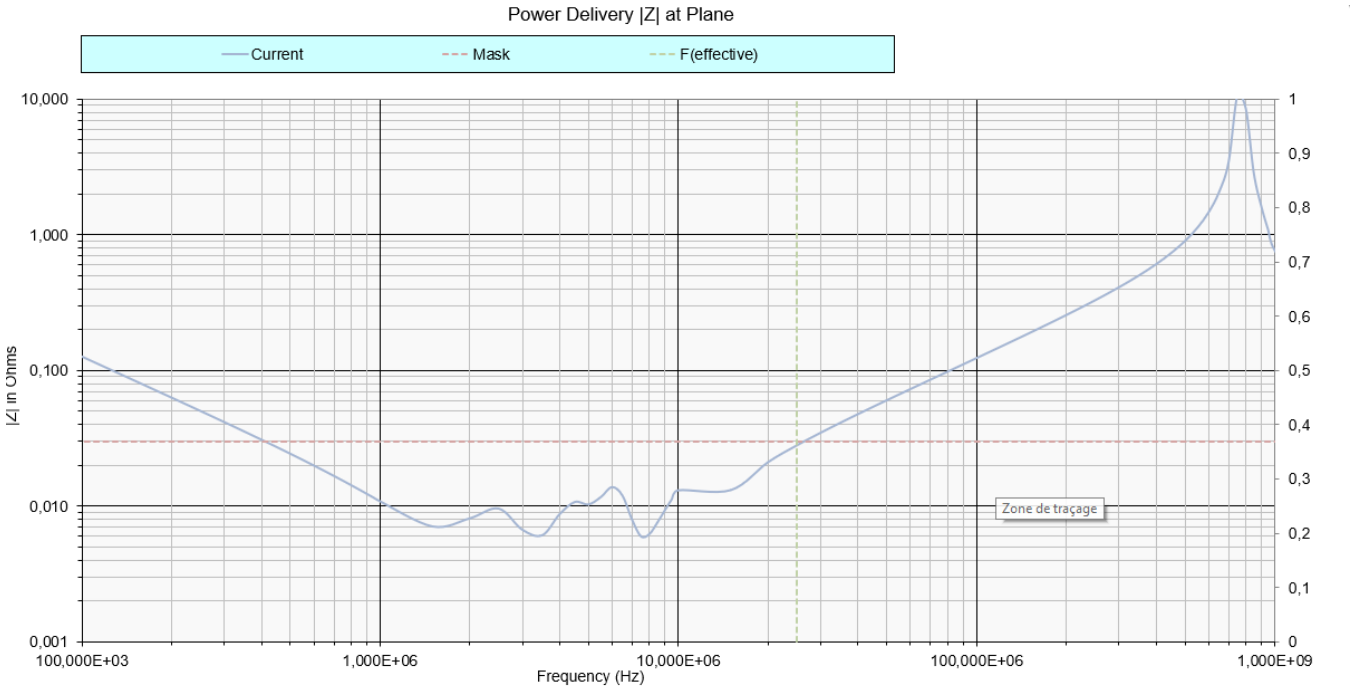
4.1.9.5 Decoupling VDDAR_CORE (V_0V85)

HUA43319	HUA15709	TME00744		xPERSO2	HUA25833	HUA42895	HUA31098	TME03438	1CAP005642	10N25V0201
22uF	10uF	4,7uF		2,2uF	1uF	470nF	220nF	100nF	47nF	10nF
10V	10V	10V		10V	10V	10V	16V	6,3V	10V	25V
X5R	X7R	X5R		X5R	X7R	X7R	X7R	X5R	X7R	X7R
20,00%	10,00%	10,00%		10,00%	10,00%	10,00%	10,00%	10,00%	10,00%	10,00%
#1 actual	#2 actual	#3 actual	#4 actual	#5 actual	#6 actual	#7 actual	#8 actual	#9 actual	#10 actual	#11 actual
0,92	1,05	0,94		0,92	1,13	1,09	1,05	0,95	1,03	0,99
20,130E-06	10,530E-06	4,420E-06		2,013E-06	1,133E-06	512,770E-09	229,969E-09	95,206E-09	48,222E-09	9,932E-09
928,032E-12	919,941E-12	838,555E-12		757,704E-12	928,032E-12	838,555E-12	838,555E-12	757,704E-12	838,555E-12	757,704E-12
20,000E-03	4,000E-03	16,000E-03		8,000E-03	14,802E-03	20,000E-03	21,278E-03	30,000E-03	10,000E-03	70,000E-03
		2	2		2	1	3	2		
2	2	2	2	2	2	2	2	2	2	2
1,118E-09	1,118E-09	1,118E-09		1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09
400	400	400	400	400	400	400	400	400	400	400
1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12
2,046E-09	2,038E-09	1,956E-09		1,875E-09	2,046E-09	1,956E-09	1,956E-09	1,875E-09	1,956E-09	1,875E-09
HUA43319	HUA15709	TME00744	n/a	xPERSO2	HUA25833	HUA42895	HUA31098	TME03438	1CAP005642	10N25V0201



Z_{TARGET} is much lower than 0.030Ω targeted @25MHz.

4.1.9.6 Decoupling VDD_LPDDR4 (V_1V1)

According to datasheet [REF2] :

> case, VDD_MMC0 and VDD_DLL_MMC0 may be operated at a nominal voltage
> (3) VDDS_DDR and VDDS_DDR_C shall be sourced from the same power source.
> (4) The VMON_VSYS pin provides a way to monitor the system power supply. For m

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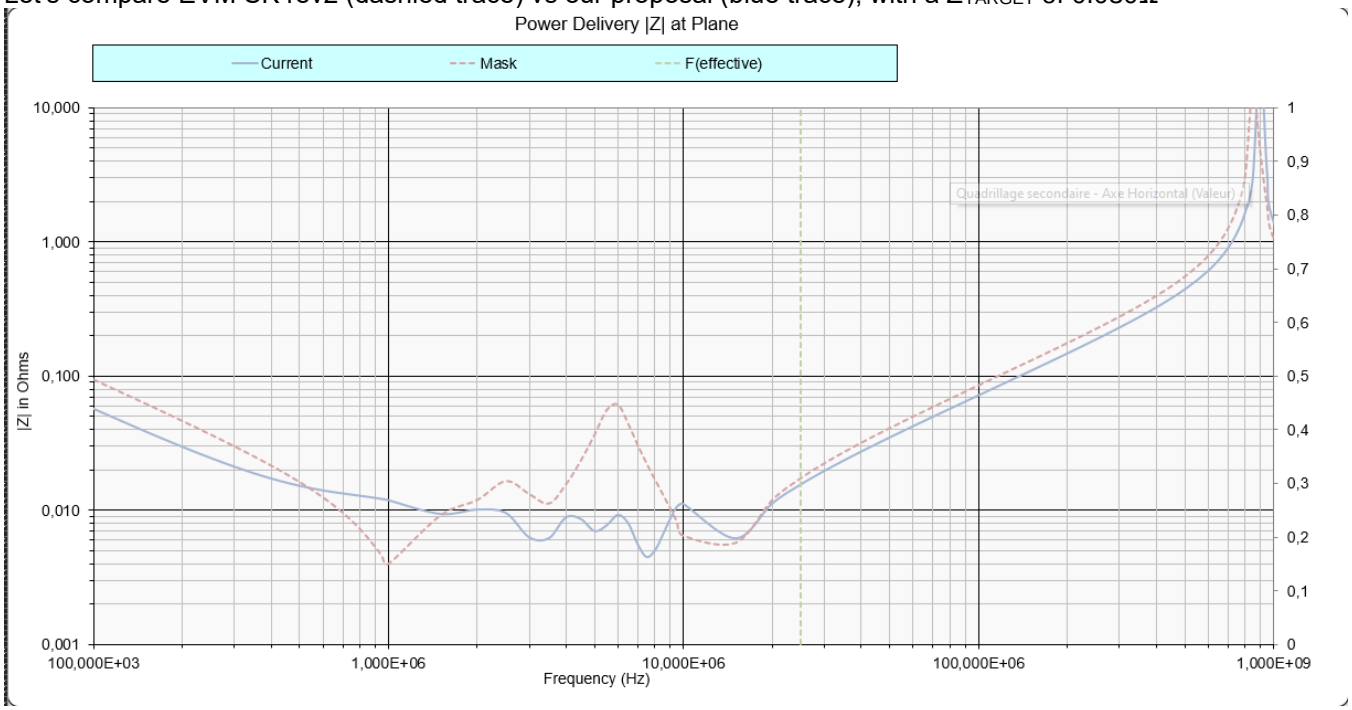
HUA43319	HUA15709	TME00744	HUA25833	HUA42895	HUA31098	TME03438	1CAP005642	10N25V0201
22uF	10uF	4,7uF	1uF	470nF	220nF	100nF	47nF	10nF
10V	10V	10V	10V	10V	16V	6,3V	10V	25V
X5R	X7R	X5R	X7R	X7R	X7R	X5R	X7R	X7R
20,00%	10,00%	10,00%	10,00%	10,00%	10,00%	10,00%	10,00%	10,00%
#1 actual	#2 actual	#3 actual	#4 actual	#5 actual	#6 actual	#7 actual	#8 actual	#9 actual
0,87	1,04	0,91	1,14	1,06	1,05	0,92	1,01	0,99
19,228E-06	10,380E-06	4,296E-06	1,136E-06	497,260E-09	230,313E-09	92,032E-09	47,470E-09	9,912E-09
928,032E-12	919,941E-12	838,555E-12	928,032E-12	838,555E-12	838,555E-12	757,704E-12	838,555E-12	757,704E-12
20,000E-03	4,000E-03	16,000E-03	14,802E-03	20,000E-03	21,278E-03	30,000E-03	10,000E-03	70,000E-03
1		1	2	2	4	7		
2	2	2	2	2	2	2	2	2
1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09
400	400	400	400	400	400	400	400	400
1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12
2,046E-09	2,038E-09	1,956E-09	2,046E-09	1,956E-09	1,956E-09	1,875E-09	1,956E-09	1,875E-09
HUA43319	HUA15709	TME00744	HUA25833	HUA42895	HUA31098	TME03438	1CAP005642	10N25V0201

Let's compare EVM SK rev2 (dashled trace) vs our proposal (blue trace), with a Z_{TARGET} of 0.030Ω



We reach 0.030Ω at 25MHz are required

Below same curve with Z_{TARGET} of 0.030Ω shown in dashled line:

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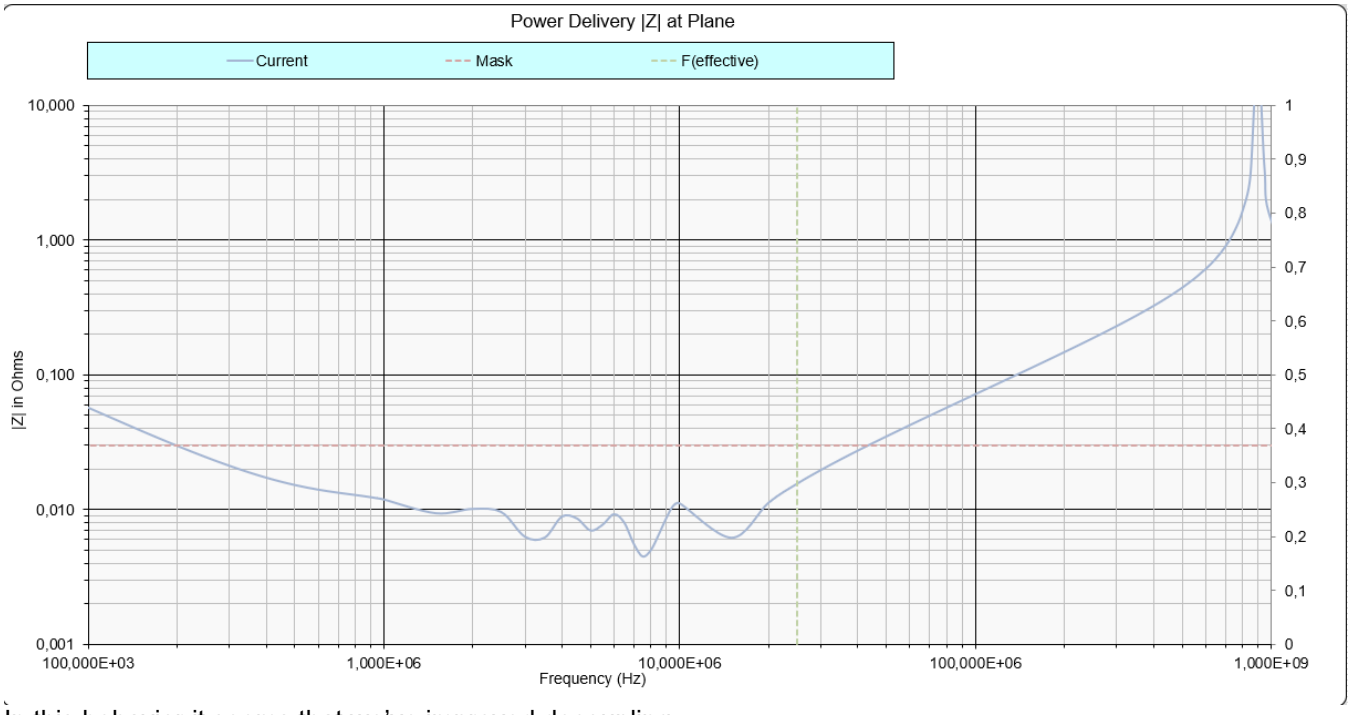

In this behavior it seems that we've improved decoupling.

4.1.9.7 Decoupling V_1V8IO (SOC_DVDD1V8)

HUA43319	HUA15709	TME00744	HUA25833	HUA42895	HUA31098	TME03438	1CAP005642	10N25V0201
22uF	10uF	4,7uF	1uF	470nF	220nF	100nF	47nF	10nF
10V	10V	10V	10V	10V	16V	6,3V	10V	25V
X5R	X7R	X5R	X7R	X7R	X7R	X5R	X7R	X7R
20,00%	10,00%	10,00%	10,00%	10,00%	10,00%	10,00%	10,00%	10,00%
#1 actual	#2 actual	#3 actual	#4 actual	#5 actual	#6 actual	#7 actual	#8 actual	#9 actual
0,89	0,95	0,80	1,11	0,97	1,03	0,82	0,94	0,99
15,224E-06	9,540E-06	3,769E-06	1,108E-06	457,780E-09	226,050E-09	82,286E-09	44,180E-09	9,856E-09
928,032E-12	919,941E-12	838,555E-12	928,032E-12	838,555E-12	838,555E-12	757,704E-12	838,555E-12	757,704E-12
20,000E-03	4,000E-03	16,000E-03	14,802E-03	20,000E-03	21,278E-03	30,000E-03	10,000E-03	70,000E-03
1		1	1	1	2	3		
2	2	2	2	2	2	2	2	2
1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09
400	400	400	400	400	400	400	400	400
1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12
2,046E-09	2,038E-09	1,956E-09	2,046E-09	1,956E-09	1,956E-09	1,875E-09	1,956E-09	1,875E-09
HUA43319	HUA15709	TME00744	HUA25833	HUA42895	HUA31098	TME03438	1CAP005642	10N25V0201

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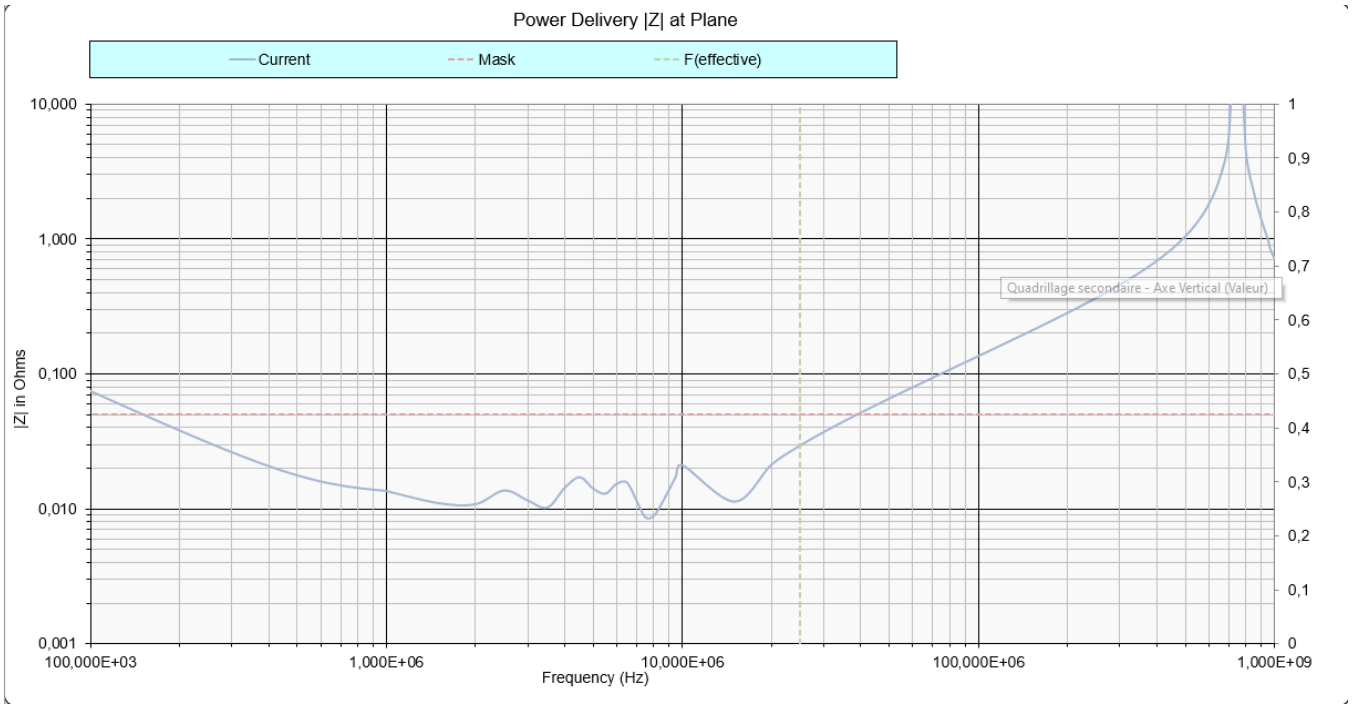

We reach 0.050Ω on all bandwidth are required.

4.1.9.8 Decoupling V_3V3IO (SOC_DVDD3V3)

HUA43319	HUA15709	TME00744	HUA25833	HUA42895	HUA31098	TME03438	1CAP005642	10N25V0201
22uF	10uF	4,7uF	1uF	470nF	220nF	100nF	47nF	10nF
10V	10V	10V	10V	10V	16V	6,3V	10V	25V
X5R	X7R	X5R	X7R	X7R	X7R	X5R	X7R	X7R
20,00%	10,00%	10,00%	10,00%	10,00%	10,00%	10,00%	10,00%	10,00%
#1 actual	#2 actual	#3 actual	#4 actual	#5 actual	#6 actual	#7 actual	#8 actual	#9 actual
0,41	0,73	0,56	0,97	0,77	0,86	0,62	0,74	0,96
9,108E-06	7,280E-06	2,637E-06	974,000E-09	360,960E-09	188,650E-09	62,095E-09	34,827E-09	9,576E-09
928,032E-12	919,941E-12	838,555E-12	928,032E-12	838,555E-12	838,555E-12	757,704E-12	838,555E-12	757,704E-12
20,000E-03	4,000E-03	16,000E-03	14,802E-03	20,000E-03	21,278E-03	30,000E-03	10,000E-03	70,000E-03
1	0	1	2	2	2	8		
2	2	2	2	2	2	2	2	2
1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09
400	400	400	400	400	400	400	400	400
1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12
2,046E-09	2,038E-09	1,956E-09	2,046E-09	1,956E-09	1,956E-09	1,875E-09	1,956E-09	1,875E-09
HUA43319	HUA15709	TME00744	HUA25833	HUA42895	HUA31098	TME03438	1CAP005642	10N25V0201

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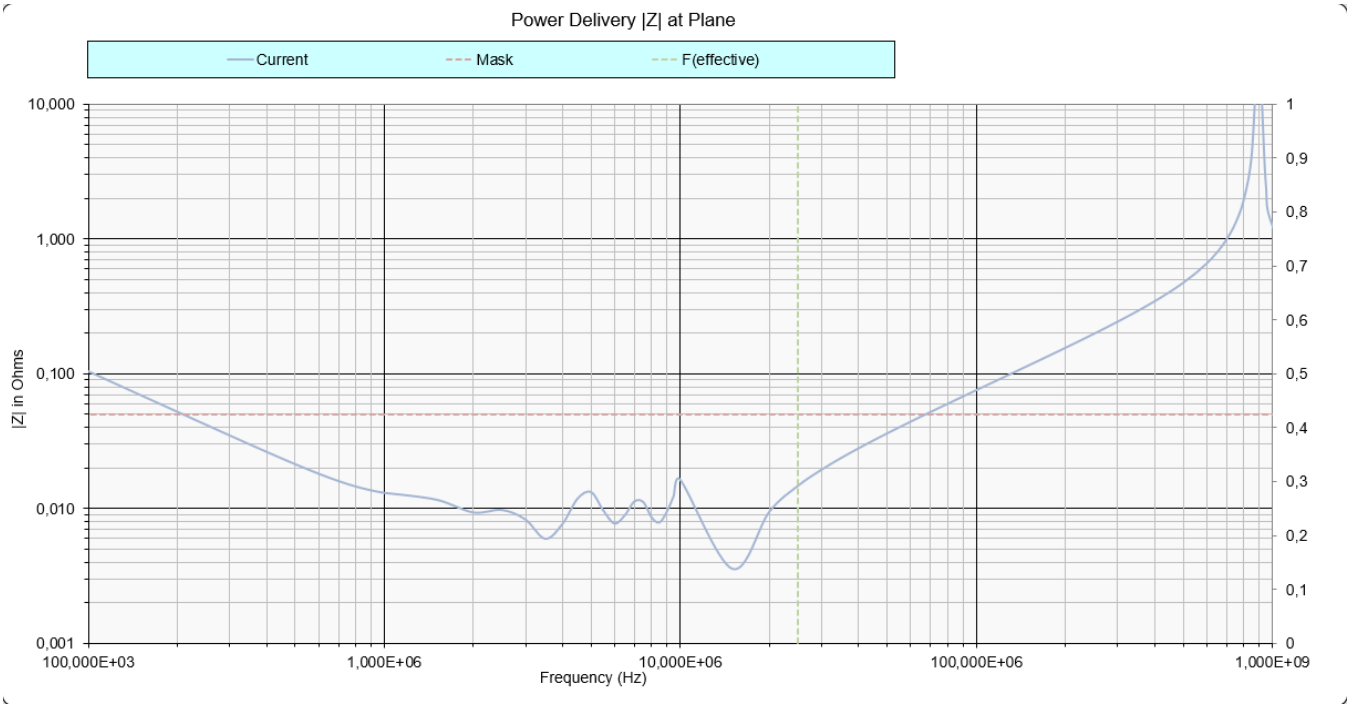

We reach 0.050Ω on all bandwidth are required.

4.1.9.9 Decoupling VDDA_* (Analog Power supplies)

According to T.I. email we must follow what was done on eval board: Processors forum_ AM6442_ VDDA_X p

4.1.9.9.1 Decoupling VDDA_0P85_SERDES0 / VDDA_0P85_SERDES0_C

According to EVM SK rev2 decoupling is done by ferrite bead BLM15AG221SN1D 200ohm@100MHz 450mA@125°C + 2.2µF//3x100nF//3x10nF.
We decide to choose: CO031068: BLM15PD121SN1D 120ohm@100MHz 900mA@125°C +2.2µF // 220nF // 3x100nF //3 x 10nF

4.1.9.9.2 Decoupling VDDA_1P8_SERDES0

According to EVM SK rev2 decoupling is done by ferrite bead BLM15AG221SN1D 200ohm@100MHz 450mA@125°C + 4.7µF // 100nF // 10nF.
We decide to choose: CO031068: BLM15PD121SN1D 120ohm@100MHz 900mA@125°C + 4.7µF // 100nF // 10nF

4.1.9.9.3 Decoupling VDDA_0P85_USB0

According to EVM SK rev2 decoupling is done by ferrite bead BLM15AG221SN1D 200ohm@100MHz 450mA@125°C + 2.2µF // 100nF// 10nF.
We decide to choose: CO031068: BLM15PD121SN1D 120ohm@100MHz 900mA@125°C + 2.2µF // 100nF // 10nF

4.1.9.9.4 Decoupling VDDA_1P8_USB0

According to EVM SK rev2 decoupling is done by ferrite bead BLM15AG221SN1D 200ohm@100MHz 450mA@125°C + 4.7µF // 100nF// 10nF.

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We decide to choose: CO031068: BLM15PD121SN1D 120ohm@100MHz 900mA@125°C + 4.7µF // 100nF // 10nF

4.1.9.9.5 Decoupling VDD_DLL_MMC0

According to EVM SK rev2 decoupling is done by ferrite bead BLM15AG221SN1D 200ohm@100MHz 450mA@125°C + 4.7µF // 100nF// 10nF.
We decide to choose : CO031068: BLM15PD121SN1D 120ohm@100MHz 900mA@125°C + 4.7µF // 100nF // 10nF

4.1.9.9.6 Decoupling VDDA_PLL0 / VDDA_PLL1 / VDDA_PLL2

According to EVM SK rev2 decoupling is done by ferrite bead BLM15AG221SN1D 200ohm@100MHz 450mA@125°C + 1µF // 100nF// 10nF.
We decide to choose : CO031068: BLM15PD121SN1D 120ohm@100MHz 900mA@125°C + 1µF // 100nF // 10nF

4.1.9.9.7 Decoupling VDDA_MCU

According to EVM SK rev2 decoupling is done by ferrite bead BLM15AG221SN1D 200ohm@100MHz 450mA@125°C + 4.7µF // 100nF// 10nF.
We decide to choose : CO031068: BLM15PD121SN1D 120ohm@100MHz 900mA@125°C + 4.7µF // 100nF // 10nF

4.1.9.9.8 Decoupling VDDA_ADC

According to EVM GP rev2 decoupling is done by ferrite bead BLM15AG221SN1D 200ohm@100MHz 450mA@125°C + 4.7µF // 100nF// 10nF.
We decide to choose : CO031068: BLM15PD121SN1D 120ohm@100MHz 900mA@125°C + 4.7µF // 100nF // 10nF

4.1.9.10 Decoupling CAP_VDDS*

According to application note [REF6] : there is 8 internal LDO which must be decoupled by a 1µF , excepted CAP_VDDSHV_MMC1 which require a 3.3µF ±20%. 3.3µF is not a so common capacitor value, so we decide to split it into 2.2µF ±10%(TME21304) + 1µF ±20%(TME10670).

CAP_VDDSHV_MMC1.pdf

This specific CAP_VDDSHV_MMC1 is really needed according to this E2E forum exchange:

4.1.9.11 Decoupling Tips&Tricks

On AM64 SK rev2 evalboard from TI, there is NFM15 from murata used as 2 ball pin capacitors, which solve some decoupling density issue.
This a 3 points capacitor with low parasitic inductance.
Check :
https://www.murata.com/products/capacitor/ceramiccapacitor/overview/lineup/smd/nfm
https://article.murata.com/en-global/article/basics-of-noise-countermeasures-lesson-11

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4.1.10 CPSW3G-PRU (RGMII MII)

AM64 Brick will provide many xMII interfaces :

- 2 x RGMII from CPSW3G
- 2 x RGMII from PRU
- 1 x MII from PRU

4.1.10.1 RGMII CPSW3G pin usage

CPSW3G_RGMII1 cannot be used as RGMII boot mode, here is pin assignment (according to [REF17]):

AM64			**BRICK**	***AETHENA board (informative only)***
Device Pin	Module Name	BALL	I/O port	*net name*
PRG0_PRU1_GPO7	RGMII1_RD0	W5	GPIO1_27	*CPSW3G_RGMII1_RD0*
PRG0_PRU1_GPO9	RGMII1_RD1	Y5	GPIO1_29	*CPSW3G_RGMII1_RD1*
PRG0_PRU1_GPO10	RGMII1_RD2	V6	GPIO1_30	*CPSW3G_RGMII1_RD2*
PRG0_PRU1_GPO17	RGMII1_RD3	V5	GPIO1_37	*CPSW3G_RGMII1_RD3*
PRG0_PRU0_GPO9	RGMII1_RX_CTL	W6	GPIO1_9	*CPSW3G_RGMII1_RX_CTL*
PRG0_PRU0_GPO10	RGMII1_RXC	AA5	GPIO1_10	*CPSW3G_RGMII1_RXC*
PRG1_PRU1_GPO7	RGMII1_TD0	V15	GPIO0_72	*CPSW3G_RGMII1_TD0*
PRG1_PRU1_GPO9	RGMII1_TD1	V14	GPIO0_74	*CPSW3G_RGMII1_TD1*
PRG1_PRU1_GPO10	RGMII1_TD2	U10	GPIO0_75	*CPSW3G_RGMII1_TD2*
PRG1_PRU1_GPO17	RGMII1_TD3	AA14	GPIO0_19	*CPSW3G_RGMII1_TD3*
PRG1_PRU0_GPO9	RGMII1_TX_CTL	U15	GPIO0_54	*CPSW3G_RGMII1_TX_CTL*
PRG1_PRU0_GPO10	RGMII1_TXC	Y10	GPIO0_55	*CPSW3G_RGMII1_TXC*
PRG1_MDIO0_MDIO	MDIO0_MDIO	AA6	GPIO0_85	*CPSW3G_MDIO0_MDIO*
PRG1_MDIO0_MDC	MDIO0_MDC	Y6	GPIO0_86	*CPSW3G_MDIO0_MDC*

CPSW3G_RGMII2 can be used in RGMII boot mode, please check chapter ETHERNET RGMII BOOT MODE.

AM64			**BRICK**	***AETHENA board (informative only)***
Device Pin	Module Name	BALL	I/O port	*net name*
PRG1_PRU1_GPO0	RGMII2_RD0	W11	GPIO0_65	*CSPW3G_RGMII2_RD0*
PRG1_PRU1_GPO1	RGMII2_RD1	V11	GPIO0_66	*CPSW3G_RGMII2_RD1*
PRG1_PRU1_GPO2	RGMII2_RD2	AA12	GPIO0_67	*CPSW3G_RGMII2_RD2*
PRG1_PRU1_GPO3	RGMII2_RD3	Y12	GPIO0_68	*CPSW3G_RGMII2_RD3*
PRG1_PRU1_GPO4	RGMII2_RX_CTL	W12	GPIO0_69	*CPSW3G_RGMII2_RX_CTL*
PRG1_PRU1_GPO6	RGMII2_RXC	U11	GPIO0_71	*CPSW3G_RGMII2_RXC*
PRG1_PRU1_GPO11	RGMII2_TD0	AA10	GPIO0_76	*CPSW3G_RGMII2_TD0*
PRG1_PRU1_GPO12	RGMII2_TD1	V10	GPIO0_77	*CPSW3G_RGMII2_TD1*
PRG1_PRU1_GPO13	RGMII2_TD2	U10	GPIO0_78	*CPSW3G_RGMII2_TD2*
PRG1_PRU1_GPO14	RGMII2_TD3	AA11	GPIO0_79	*CPSW3G_RGMII2_TD3*
PRG1_PRU1_GPO15	RGMII2_TX_CTL	Y11	GPIO0_80	*CPSW3G_RGMII2_TX_CTL*
PRG1_PRU1_GPO16	RGMII2_TXC	Y10	GPIO0_81	*CPSW3G_RGMII2_TXC*

N.B: MDIO0_MDC & MDIO0_MDIO is shared for the 2 RGMII CPSW3G_RGMII1 & CPSW3G_RGMII2.

4.1.10.2 RGMII CPSW3G max output load

All AM64 timing and switching characteristics are described with a load between 3pf and above all 30pf (according to [REF2]):

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7.10.3 System Timing

For more details about features and additional description information on the subsystem multiplexing signals, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

Table 7-4. System Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.5		V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	3	30	pF

Concerning especially CPSW3G :

7.10.5.1.3 CPSW3G RGMII Timing

Table 7-26, Table 7-27, Table 7-28, Figure 7-26, Table 7-29, Table 7-30, and Figure 7-27 present timing conditions, requirements, and switching characteristics for CPSW3G RGMII.

Table 7-26. CPSW3G RGMII Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	2.64	5	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	20	pF

So, Ethernet Phy + PCB net routing outside the brick must respect this max load of 20pF, in order to respect RGMII timing constraints (125MHZ DDR).

Concerning MDIO the constraint is more flexible :

Table 7-19. CPSW3G MDIO Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.9	3.6	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	10	470	pF

4.1.10.3 RMII CPSW3G pin usage

TO BE COMPLETED

4.1.10.4 RGMII PRU pin usage

COPRO1_PRG0_RGMMI1 have the following pin usage:

AM64			**BRICK**	***AETHENA board (informative only)***
Device Pin	Module Name	BALL	I/O port	*net name*
PRG0_PRU0_GPO0	PRG0_RGMII1_RD0	Y1	GPIO1_0	*COPRO1_PRG0_RGMII1_RD0*
PRG0_PRU0_GPO1	PRG0_RGMII1_RD1	R4	GPIO1_1	*COPRO1_PRG0_RGMII1_RD1*
PRG0_PRU0_GPO2	PRG0_RGMII1_RD2	U2	GPIO1_2	*COPRO1_PRG0_RGMII1_RD2*
PRG0_PRU0_GPO3	PRG0_RGMII1_RD3	V2	GPIO1_3	*COPRO1_PRG0_RGMII1_RD3*
PRG0_PRU0_GPO4	PRG0_RGMII1_RX_CTL	AA2	GPIO1_4	*COPRO1_PRG0_RGMII1_RX_CTL*
PRG0_PRU0_GPO6	PRG0_RGMII1_RXC	T3	GPIO1_6	*COPRO1_PRG0_RGMII1_RXC*
PRG0_PRU0_GPO11	PRG0_RGMII1_TD0	Y3	GPIO1_11	*COPRO1_PRG0_RGMII1_TD0*
PRG0_PRU0_GPO12	PRG0_RGMII1_TD1	AA3	GPIO1_12	*COPRO1_PRG0_RGMII1_TD1*
PRG0_PRU0_GPO13	PRG0_RGMII1_TD2	R6	GPIO1_13	*COPRO1_PRG0_RGMII1_TD2*
PRG0_PRU0_GPO14	PRG0_RGMII1_TD3	V4	GPIO1_14	*COPRO1_PRG0_RGMII1_TD3*
PRG0_PRU0_GPO15	PRG0_RGMII1_TX_CTL	T5	GPIO1_15	*COPRO1_PRG0_RGMII1_TX_CTL*
PRG0_PRU0_GPO16	PRG0_RGMII1_TXC	U4	GPIO1_16	*COPRO1_PRG0_RGMII1_TXC*
PRG0_MDIO0_MDIO	PRG0_MDIO0_MDIO	P2	GPIO1_40	*COPRO1_COPRO2_PRG0_MDIO0_MDIO*

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PRG0_MDIO0_MDC	PRG0_MDIO0_MDC	P3	GPIO1_41	*COPRO1_COPRO2_PRG0_MDIO0_MDC*

COPRO2_PRG0_RGMMI2 have the following pin usage:

AM64			**BRICK**	***AETHENA board (informative only)***
Device Pin	Module Name	BALL	I/O port	*net name*
PRG0_PRU1_GPO0	PRG0_RGMII2_RD0	Y2	GPIO1_20	*COPRO2_PRG0_RGMII2_RD0*
PRG0_PRU1_GPO1	PRG0_RGMII2_RD1	W2	GPIO1_21	*COPRO2_PRG0_RGMII2_RD1*
PRG0_PRU1_GPO2	PRG0_RGMII2_RD2	V3	GPIO1_22	*COPRO2_PRG0_RGMII2_RD2*
PRG0_PRU1_GPO3	PRG0_RGMII1_RD3	T4	GPIO1_23	*COPRO2_PRG0_RGMII2_RD3*
PRG0_PRU1_GPO4	PRG0_RGMII2_RX_CTL	W3	GPIO1_24	*COPRO2_PRG0_RGMII2_RX_CTL*
PRG0_PRU1_GPO6	PRG0_RGMII2_RXC	R5	GPIO1_26	*COPRO2_PRG0_RGMII2_RXC*
PRG0_PRU1_GPO11	PRG0_RGMII2_TD0	W4	GPIO1_31	*COPRO2_PRG0_RGMII2_TD0*
PRG0_PRU1_GPO12	PRG0_RGMII2_TD1	Y4	GPIO1_32	*COPRO2_PRG0_RGMII2_TD1*
PRG0_PRU1_GPO13	PRG0_RGMII2_TD2	T6	GPIO1_33	*COPRO2_PRG0_RGMII2_TD2*
PRG0_PRU1_GPO14	PRG0_RGMII2_TD3	U6	GPIO1_34	*COPRO2_PRG0_RGMII2_TD3*
PRG0_PRU1_GPO15	PRG0_RGMII2_TX_CTL	U5	GPIO1_35	*COPRO2_PRG0_RGMII2_TX_CTL*
PRG0_PRU1_GPO16	PRG0_RGMII2_TXC	AA4	GPIO1_36	*COPRO2_PRG0_RGMII2_TXC*

N.B: PRG0_MDIO0_MDIO & PRG0_MDIO0_MDC is shared for the 2 RGMII COPRO1_PRG0_RGMMI1 & COPRO2_PRG0_RGMMI2.

COPRO1_PRG0_RGMMI1 and COPRO2_PRG0_RGMMI2 is not available for bootmode purpose.

4.1.10.5 RGMII PRU max output load

Concerning PRU:

Table 7-135. PRU_ICSSG RGMII Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate	VDD = 1.8V	1.44	5	V/ns
		VDD = 3.3V	2.65	5	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance		2	20	pF

So, Ethernet Phy + PCB net routing outside the brick must respect this max load of 20pF, in order to respect RGMII timing constraints (125MHZ DDR for GbE).

Concerning MDIO it's more flexible and may support an additional capacitor on the bus end:

Table 7-127. PRU_ICSSG MDIO Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.9	3.6	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	10	470	pF

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4.1.10.6 MII PRU pin usage

~~COPRO1_PRG0_RGMMI1~~ have the following pin usage:

AM64			BRICK	*AETHENA board (informative only)*
Device Pin	Module Name	BALL	I/O port	*net name*
PRG1_PRU0_GPO0	PR1_MI0_RXD0	Y7	GPIO0_45	*COPRO2_PRG1_PRU0_GPIO0*
PRG1_PRU0_GPO1	PR1_MI0_RXD1	U8	GPIO0_46	*COPRO2_PRG1_PRU0_GPIO1*
PRG1_PRU0_GPO2	PR1_MI0_RXD2	W8	GPIO0_47	*COPRO2_PRG1_PRU0_GPIO2*
PRG1_PRU0_GPO3	PR1_MI0_RXD3	V8	GPIO0_48	*COPRO2_PRG1_PRU0_GPIO3*
PRG1_PRU0_GPO4	PR1_MII0_RXDV	Y8	GPIO0_49	*COPRO2_PRG1_PRU0_GPIO4*
PRG1_PRU0_GPO5	PR1_MII0_RXER	V13	GPIO0_50	*COPRO2_PRG1_PRU0_GPIO5*
PRG1_PRU0_GPO6	PR1_MII_MR0_CLK	AA7	GPIO0_51	*COPRO2_PRG1_PRU0_GPIO6*
PRG1_PRU0_GPO8	PR1_MI0_RXLINK	W13	GPIO0_53	*COPRO2_PRG1_PRU0_GPIO8*
PRG1_PRU0_GPO11	PR1_MII0_TXD0	AA8	GPIO0_56	*COPRO2_PRG1_PRU0_GPIO11*
PRG1_PRU0_GPO12	PR1_MII0_TXD1	U9	GPIO0_57	*COPRO2_PRG1_PRU0_GPIO12*
PRG1_PRU0_GPO13	PR1_MII0_TXD2	W9	GPIO0_58	*COPRO2_PRG1_PRU0_GPIO13*
PRG1_PRU0_GPO14	PR1_MII0_TXD3	AA9	GPIO0_59	*COPRO2_PRG1_PRU0_GPIO14*
PRG1_PRU0_GPO15	PR1_MI0_TXEN	Y9	GPIO0_60	*COPRO2_PRG1_PRU0_GPIO15*
PRG1_PRU0_GPO16	PR1_MII_MT0_CLK	V9	GPIO0_61	*COPRO2_PRG1_PRU0_GPIO16*

4.1.10.7 MII PRU max output load

Table 7-130. PRU_ICSSG MII Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.9	3.6	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	20	pF

4.1.10.8 Layout recommendations

4.1.10.8.1 Max Trace Length

According to E2E TI forum is about : 6” max length
Same length on NXP forum
Same length for National Semi (with recommendation to put these lines in internal layers)
Cadence recommend as short as possible with impedance line matching at 50Ω+-10%.

4.1.10.8.2 RGMII Trace mismatch delay

According to [REF2] :

7.10.5.1.3 CPSW3G RGMII Timing

Table 7-26, Table 7-27, Table 7-28, Figure 7-26, Table 7-29, Table 7-30, and Figure 7-27 present timing conditions, requirements, and switching characteristics for CPSW3G RGMII.

Table 7-26. CPSW3G RGMII Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate		2.64	5	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance		2	20	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces	RGMII[x]_RXC, RGMII[x]_RD[3:0], RGMII[x]_RX_CTL		50	ps
		RGMII[x]_TXC, RGMII[x]_TD[3:0], RGMII[x]_TX_CTL		50	ps

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Table 7-135. PRU_ICSSG RGMII Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate	VDD = 1.8V	1.44	5	V/ns
		VDD = 3.3V	2.65	5	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance		2	20	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces	RGMII[x]_RXC, RGMII[x]_RD[3:0], RGMII[x]_RX_CTL		50	ps
		RGMII[x]_TXC, RGMII[x]_TD[3:0], RGMII[x]_TX_CTL		50	ps

	sprsp56e recommendation	BRICK SETTINGS
Max trace length	-	<6”
CPSW3G skew inter signals RX group(RXC+RDx+RX_CTL)	50ps max	50ps max
CPSW3G skew inter signals TX group(TXC+TDx+TX_CTL)	50ps max	
PRU_ICSSG skew inter signals RX group(RXC+RDx+RX_CTL)	50ps max	50ps max
PRU_ICSSG skew inter signals TX group(TXC+TDx+TX_CTL)	50ps max	
signals single ended impedance		50Ω±10%
#vias per signal	-	2 max
signals to noisy signal (e.g. : clock)	-	3W
signals to quiet signal	-	2W

4.1.10.8.3 Damping resistor

According to [REF6], 22Ω damping resistor will be added in series, on each driver side (close to AM64 for TX signal and close to PHY for RX signals).
Thanks to very small brick size, these damping resistors will be managed outside the brick.

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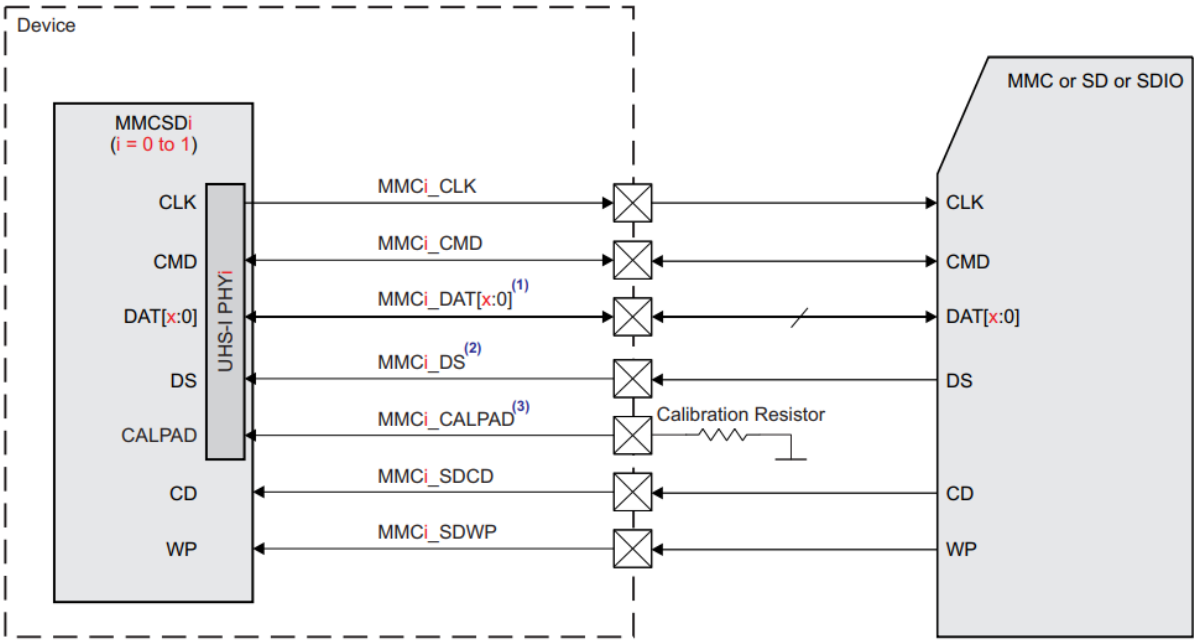
4.1.11 MMC0

MMC0 Host Controller provides accessibility to external eMMc/MMC/SD devices. MMC0 is a dedicated 1.8V interface mostly used to address eMMC interface but can also be used for connection to 1, 4, 8-bit devices.



(1) x = 7 for MMCSD0 (8-bit wide data bus); x = 3 for MMCSD1 (4-bit wide data bus);
(2) Used for HS400 mode (MMCSD0 Only);
(3) Used for PHY Calibaration Resistor (MMCSD0 Only);

4.1.11.1 MMC0 supported features

Multi-Media Card Support:

- eMMC Electrical Standard 5.1 (JESD84-B51)
- Backward compatible with earlier eMMC standards
- Legacy MMC SDR:
  - 1.8 V, 8-bit bus width, 0-25 MHz, 25 MBps
  - 1.8 V, 4-bit bus width, 0-25 MHz, 12.5 MBps
  - 1.8 V, 1-bit bus width, 0-25 MHz, 3.125 MBps
- High Speed SDR:
  - 1.8 V, 8-bit bus width, 0-50 MHz, 50 MBps
  - 1.8 V, 4-bit bus width, 0-50 MHz, 25 MBps
  - 1.8 V, 1-bit bus width, 0-50 MHz, 6.25 MBps
- High Speed DDR:
  - 1.8 V, 8-bit bus width, 0-50 MHz, 100 MBps
  - 1.8 V, 4-bit bus width, 0-50 MHz, 50 MBps
- HS200 SDR:
  - 1.8 V, 0-200 MHz, 8-bit bus width, 200 MBps
  - 1.8 V, 0-200 MHz, 4-bit bus width, 100 MBps

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4.1.11.2 MMC0 Signals

MMC0_CLOCK signal embeds dedicated serial resistor of 33Ω to prevent over / under shoot of the signal. This value depends on the design / PCB Layout application. It must be adjusted during the technical verification after measurement.

Table 12-3692. MMCSDi I/O Signals

Module Pin	Device Level Signal	I/O(1)	Description	Module Pin Reset Value
		MMCSD0		
CLK	MMC0_CLK(3)	O	External Clock	0x0
CMD	MMC0_CMD	I/O	Command Line	0x0
DAT[7:0]	MMC0_DAT[7:0]	I/O	Data Signals	0x0
DS	MMC0_DS	I	Data Strobe	0x0
CALPAD	MMC0_CALPAD(2)	A	PHY Calibration Resistor	HiZ
		MMCSD1		
CLK	MMC1_CLK	O	External Clock	0x0
CMD	MMC1_CMD	I/O	Command Line	0x0
DAT[3:0]	MMC1_DAT[3:0]	I/O	Data Signals	0x0
WP	MMC1_SDWP	I	SD Card Write Protect	0x1
CD	MMC1_SDCD	I	SD Card Detect	0x0

(1) I = Input; O = Output; HiZ = High Impedance; A = Analog
(2) An external 10 kΩ ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.
(3) This output signal is also used as a retiming input. It is also recommended to place a 33 Ω resistor in series (close to the SoC) to avoid signal reflections.

Every signal except CALPAD can be pulled up/down internally by the AM6442. In the schematic there isn't any external pull up/down on all the MMC0_DATx, MMC0_CLOCK, MMC0_CMD as the brick does not embeds the eMMC. Final user must integrate the PULL UP/DOWN on each signal according to his application.
MMC0_DS pin is recommended by T.I. to have a 10KΩ pull down close to AM64.

MMC0_CALPAD is a dedicated Analog pin for the eMMC PHY and as it is recommended in the AM6442 datasheet it is pull downed in the design by 10k resistor to the GND_LOCAL.

4.1.11.3 Layout recommendations

According to [REF2] table 7-67 :

Table 7-67. MMC0 Timing Conditions

PARAMETER			MIN	MAX	UNIT
		PCB CONNECTIVITY REQUIREMENTS			
$t_{d(Trace\ Delay)}$	Propagation delay of each trace	All modes	126	756	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces	Legacy SDR, High Speed SDR		100	ps
		High Speed DDR, HS200		8	ps

	sprsp56e recommendation	BRICK SETTINGS
Propagation delay	[126..756]ps	[126..756]ps

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Max skew inter signals (SDR, high speed SDR)	100ps max	8ps max
Max skew inter signals (HS DDR, HS200)	8ps max	
signals single ended impedance		50Ω±10%
#vias per signal	-	2 max
signals to noisy signal (e.g. : clock)	-	50 mils (1270µm)
signals to quiet signal	-	30 mils (762µm)

4.1.12 MMC1 (SDCARD)

4bits SDIO interface
This is a “locked resource” of the brick.

4.1.12.1 SD Card Specification summary

It was decided to add SD card support on AETHENA board (it was on Bestla board on former design). Specifications are:

- Micro SD Card format
- Push – push connector
- Mechanical card presence detector
- SDIO interface
- Up to “HS - High speed” bus speed (25MBytes/s) compatibility
- Able to be used as boot ad/or storage device

4.1.12.2 MMCSD signals

According to [REF2], AM64 can support all these SDCARD speeds:

7.10.5.12.2 MMC1 - SD/SDIO Interface

MMC1 interface is compliant with the SD Host Controller Standard Specification 4.10 and SD Physical Layer Specification v3.01 as well as SDIO Specification v3.00 and it supports the following SD Card applications:

- Default speed
- High speed
- UHS–I SDR12
- UHS–I SDR25
- UHS–I SDR50
- UHS–I SDR104
- UHS–I DDR50

According to Part1_Physical_Layer_Simplified_Specification_Ver6.00.pdf signaling in 1.8V is required for all UHS-I speeds:

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- Bus Speed Mode (using 4 parallel data lines)
  (1) Default Speed mode: 3.3V signaling, Frequency up to 25 MHz, up to 12.5 MB/sec
  (2) High Speed mode: 3.3V signaling, Frequency up to 50 MHz, up to 25 MB/sec
  (3) SDR12: UHS-I 1.8V signaling, Frequency up to 25 MHz, up to 12.5MB/sec
  (4) SDR25: UHS-I 1.8V signaling, Frequency up to 50 MHz, up to 25MB/sec
  (5) SDR50: UHS-I 1.8V signaling, Frequency up to 100 MHz, up to 50MB/sec
  (6) SDR104: UHS-I 1.8V signaling, Frequency up to 208 MHz, up to 104MB/sec
  (7) DDR50: UHS-I 1.8V signaling, Frequency up to 50 MHz, sampled on both clock edges, up to 50MB/sec
  (8) UHS156: UHS-II RCLK Frequency Range 26MHz - 52MHz, up to 1.56Gbps per lane.
  (9) UHS624: UHS-II RCLK Frequency Range 26MHz- 52MHz, up to 6.24Gbps per lane.

In order to handle that requirement (switchable signaling between 3.3V and 1.8V), AM64 provides in internal switchable LDO :

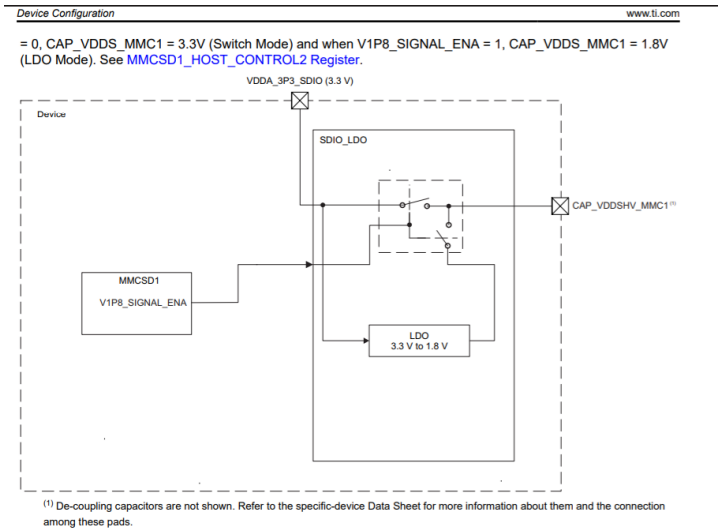

Figure 5-588. SDIO_LDO Top-Level Overview

Furthermore, there are 2 peripherals for MMC/SD card device (MMCSD0 and MMCSD1). Because of electrical and boot constraints, AM64 Technical Reference Manual recommends connecting SD card to MMCSD1 peripheral (because only MMCSD1 have internal LDO, not MMCSD0).

According to [REF2], it is recommended to connect to VSS unused pin if switchable LDO is not used :

H15 K15	VDDA_3P3_SDIO CAP_VDDSHV_MMC1	If SDIO_LDO is not used to power VDDSHV5, each of these balls must be connected directly to VSS.

This is handled by have a separate power for VDDA_3P3_SDIO + VDDSHV5 pins:

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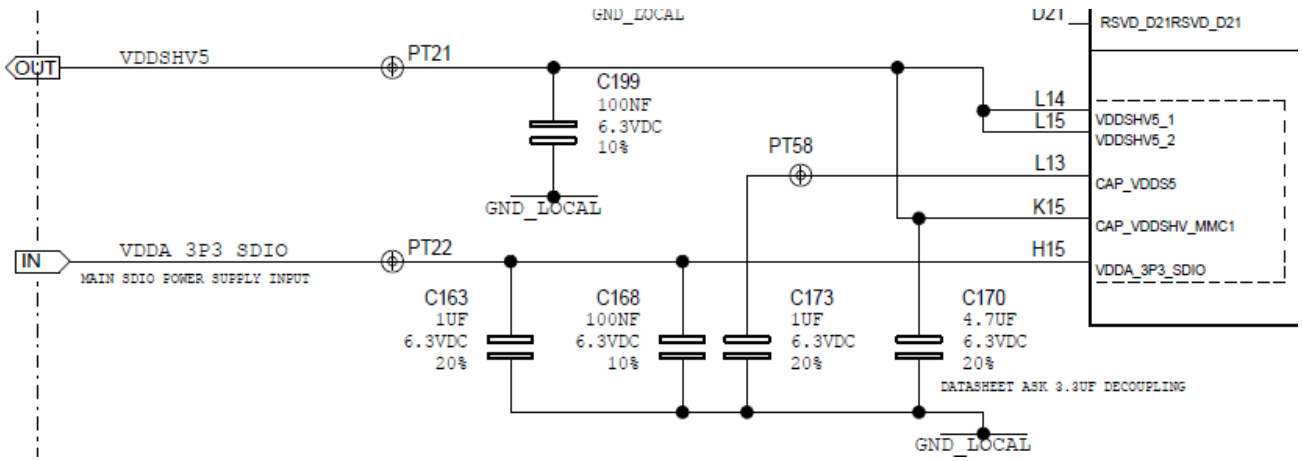

If user want to use an external switchable LDO, he must use VDDSHV5 as an input by powering it externally with a 3.3V or switchable 3.3V/1.8V and disconnect K15 ball.
Brick manages this configurations:

Internal SDIO_LDO : VDDA_3P3_SDIO should be connect to V_3V3IO to handle power sequence requirements, and VDDSHV5 would be used externally for pull up SDCARD Data & Cmd signals and ESD protection on them.

A 33Ω series resistor (SPN **HUA19826**) has been added to CLK signal to lower ringing effects. On layout, this resistor must be placed close to AM64.

10kΩ Pull-up resistors should be on DAT[0:3] and CMD signals in order to not let floating these net when SDCARD is not present (it's the same case for all I/O undriven).
This will be managed outside the brick into AETHENA board.

ESD protections (SPN **HUA34493**) should be added on signals since MMC/SD card is handled by hand.
This will be managed outside the brick into AETHENA board.

4.1.12.3 SD Card slot

Micro SD Card chosen is SPN **HUA27336**.

Connector's shield must be connected to ground.

4.1.12.4 Card Detect signal

AM64 requires a card detect signal to boot from MMCSD controller (low level when card inserted). Chosen card slot has a mechanical switch-based card detection feature. This kind of card detection allows both SD and MMC use, because MMC requirements does not specify any internal card detection feature. In addition, AM64 can't detect card with DAT3/CD signal feature.

AM64 SD card detect signal must be tied HIGH without card and tied LOW when a card is inserted. A falling edge (HIGH to LOW level signal) allows dynamic insertion detection and rising edge allow dynamic removal detection.

On microSD card connector M3 and M4 pin are both side of mechanical switch. M4 must be connected to ground and M3 to a pull-up resistor and AM64 MMC1_SDCD input pin. Because AM64 MMC1_SDCD input pin includes an internal pull-up resistor (enable by default), no external resistor is required.

AM64 internal pull-up resistor value is: min 15 KΩ, typ 20KΩ, max 25KΩ.

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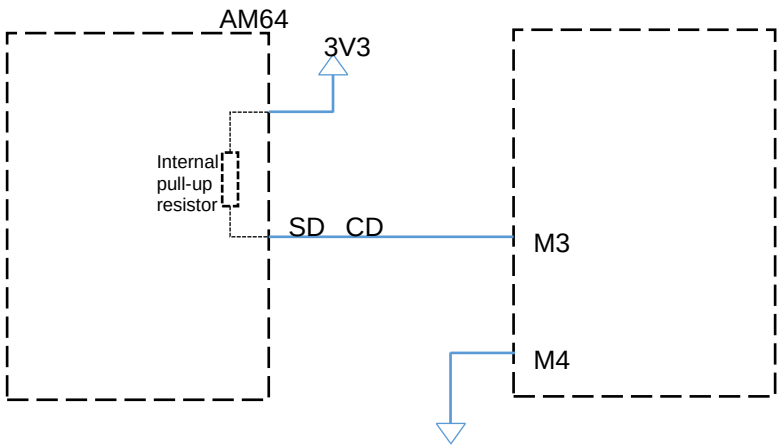

Figure 1 : SD Card detection signal connection

4.1.12.5 Layout recommendations

According to [REF2] table 7-76 :

Table 7-76. MMC1 Timing Conditions

PARAMETER			MIN	MAX	UNIT
PCB Connectivity Requirements					
$t_{d(Trace\ Delay)}$	Propagation delay of each trace	UHS–I DDR50	240	1134	ps
		All other modes	126	1386	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces	UHS–I DDR50, UHS–I SDR104		20	ps
		All other modes		100	ps

	sprsp56e recommendation	BRICK SETTINGS
Propagation delay (UHS-I DDR50)	[240..1134]ps	[240..1134]ps
Propagation delay (all other modes)	[126..1386]ps	
Max skew inter signals (UHS-I DDR50 or SDR104)	20ps max	20ps max
Max skew inter signals (all other modes)	100ps max	
signals single ended impedance		50Ω±10%
#vias per signal	-	2 max
signals to noisy signal (e.g. : clock)	-	50 mils (1270µm)
signals to quiet signal	-	30 mils (762µm)

4.1.13 I2C

According to [REF2] only I2C0 & MCU_I2C0 are full I2C compliant with standard (open drain IOPAD).
/!\ If user plan to re-use theses 2 I2C0 interface as GPIO, there will be present with open drain buffer interface (IOD) only : no IO buffer interface available.
All others: I2C1, I2C2, I2C3, MCU_I2C1 have pseudo I2C interface (LVCMOS push pull).
[REF6] talk about too fast falling edge driver (<2ns) which are not I2C compliant with standard.
[REF16] table 11 show a minimum value of T_{RISE} and T_{FALL} of $20xV_{DD}/5.5$= 12ns:

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Symbol	Parameter	Conditions	Standard-mode		Fast-mode		Fast-mode Plus		Unit
			Min	Max	Min	Max	Min	Max	
t_r	rise time of both SDA and SCL signals		-	1000	20	300	-	120	ns
t_f	fall time of both SDA and SCL signals [2] [5] [6] [7]		-	300	20 × (V_{DD} / 5.5 V)	300	20 × (V_{DD} / 5.5 V) [8]	120 [7]	ns

4.1.14 I/O

Most of AM64xx I/Os are dual voltage LVCMOS3.3/LVCMOS1.8, depending on associated bank powering.
Most of AM64xx I/Os are not fail-safe (doesn't support to be driven externally until bank powered). I/Os which support this feature are I/O type buffer with **FS** naming into [REF2].

Unused I/O must have their banks powered.
Internal PU/PD resistor are specified only to hold a voltage when a ball is unconnected. When a ball is connected to a track, manufacturer recommend strongly to add external PU/PD resistor to support coupled noise sources on this signal track.
If a ball is left unconnected without internal PU/PD then the I/O could be damaged, it has managed outside the brick.

Concerning levels and max ouput capacitor load please check Chap. 7.10.5.7 GPIO of [REF2].

4.1.15 Debug UART

UART0 RXD/TXD is provided for debug purpose. It will be managed outside the brick into AETHENA board BQT15769 (using FTDI uart over USB).

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4.2 LPDDR4 External RAM

Integrated in MAIN domain: one instance of DDR Subsystem (DDRSS) is used as an interface to external RAM devices which can be utilized for storing program or data. DDRSS provides the following main features:

- Support LPDDR4 memory types
- 16-bit memory bus interface with in-line ECC
- System bus interface: little Endian only with 128-bit data width
- Configuration bus Interface: little Endian only with 32-bit data width
- Support of dual rank configuration
- Support of automatic idle power saving mode when no or low activity is detected
- Class of Service (CoS) - three latency classes supported
- Prioritized refresh scheduling
- Statistical counters for performance management

Even if the DDRSS supports DDR4 interface as the Schneider policy and strategy is LPDDR4 oriented BRICK only supports LPDDR4 interface.

From [REF8] :

Table 3-2. Compatible JEDEC LPDDR4 Devices

Number	Parameter	MIN	MAX	UNIT
1	Data Rate (1) (2)		1600	MT/s
2	Channel Bit Width	x16	x16	Bits
3	Channels	1	1	-
4	Ranks	1	1	-
5	Die	1	1	-
6	Device Count	1	1	-

(1) Refer to the device data manual for supported data rates.
(2) SDRAMs in faster speed grades can be used, provided they are properly configured to operate at the supported data rates. Faster speed grade SDRAMs may have faster edge rates, which may affect signal integrity. SDRAMs with faster speed grades must be validated on the target board design.

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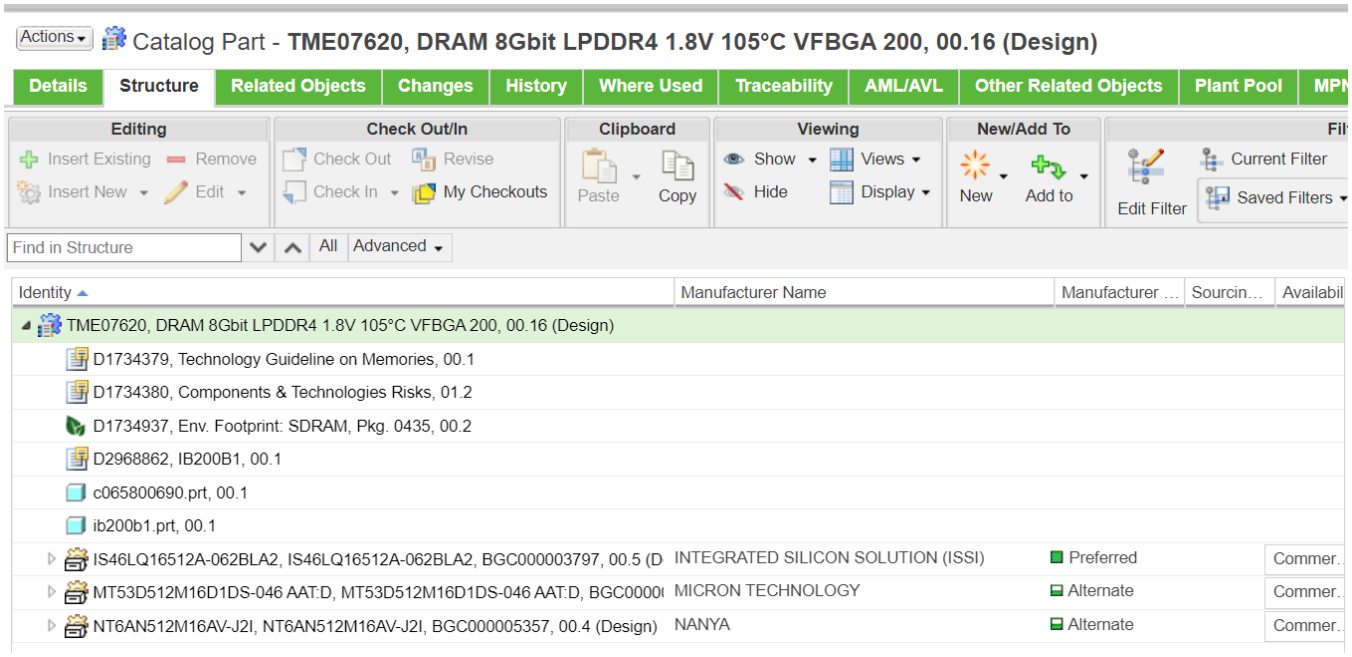
4.2.1 LPDDR4 Supported Devices

- TME07620 version 00.16 (DRAM 8Gbit LPDDR4 1.8V 105°C VFBGA 200)
  - ISSI IS46LQ16512A-062BLA2
  - MICRON MT53D512M16D1DS-046 AAT:D
  - NANYA NT6AN512M16AV-J2



LPDDR4 supports many different implementation topologies but the BRICK and AM6442 only support a single 16-bit channel for LPDDR4.

Below schematic illustrates the supported 16-bit, single-rank, single-channel LPDDR4 implementation.

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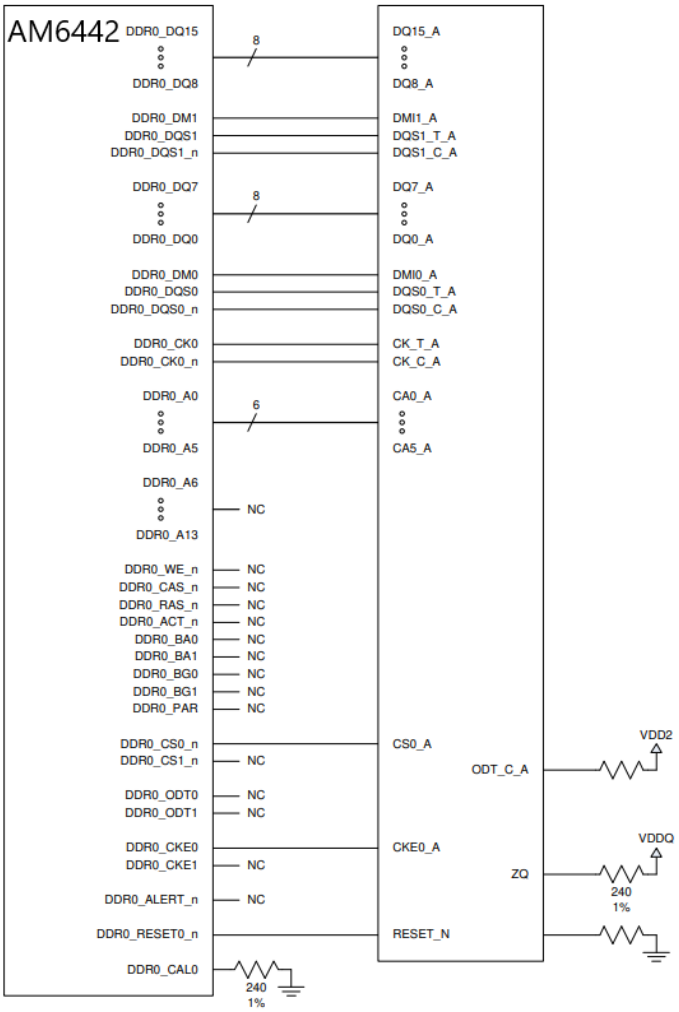

Figure 3-1. 16-Bit, Single-Rank, Single Channel LPDDR4 Implementation

Extract from [REF8]

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4.2.2 LPDDR4 Power Rail Decoupling

4.2.2.1 LPDDR4 Max power consumption

We use technical file from MICRON TN5301_LPDDR4_System_Power_Calculator_TypicalUserCase.xlsx, worst case is the condition “IDD4R Maximum read burst current”:

Parameter	Condition	VDD1 Value	VDD2 Value	VDDQ Value	Units
V_{DD}	Maximum V_{DD}	1,95	1,17	1,17	V
	Minimum V_{DD}	1,7	1,06	1,06	V
I_{DD4R}	Maximum read burst current	3,8	380	76,8	mA

4.2.2.2 LPDDR4 Voltage Ripple

Powered by	Chip Power rail name	Voltage (Volt)	Voltage Tolerance (Volt)		Voltage Tolerance (%)	
		Typ	Min	Max	Min	Max
V_1V1	VDDS_DDR4	1,1	1,06	1,17	-3,6%	6,4%
V_1V8IO	SOC_DVDD1V8	1,8	1,7	1,95	-5,6%	8,3%

(data extracted from datasheet TME07620_micron_MT53xxx.pdf.pdf)

PMIC output	Chip Power rail name	Voltage (Volt)	Voltage Tolerance (Volt)		Voltage Tolerance (%)	
		Typ	Min	Max	Min	Max
BUCK1	VDD_CORE	0,75			-1,5%	1,5%
LDO2	VDDAR_CORE	0,85			-1,1%	1,1%
LDO3	VDDA_1V8	1,8			-1,1%	1,1%
BUCK3	VDDS_DDR4	1,1			-1,5%	1,5%
BUCK2	SOC_DVDD1V8	1,8			-1,5%	1,5%
pmic input	SOC_DVDD3V3	3,3			?	?
TLV75518	**Chip Power rail name**	**Voltage (Volt)**	**Voltage Tolerance (Volt)**		**Voltage Tolerance (%)**	
		Typ	Min	Max	Min	Max
	VPP_1V8	1,8	1,71	1,89	-1,2%	1,2%

- VDDS_DDR4, allowable ripple would be -3.6%-(-1.5%) =-2.1% => Voltage Ripple for Z_{TARGET} become -1.05%

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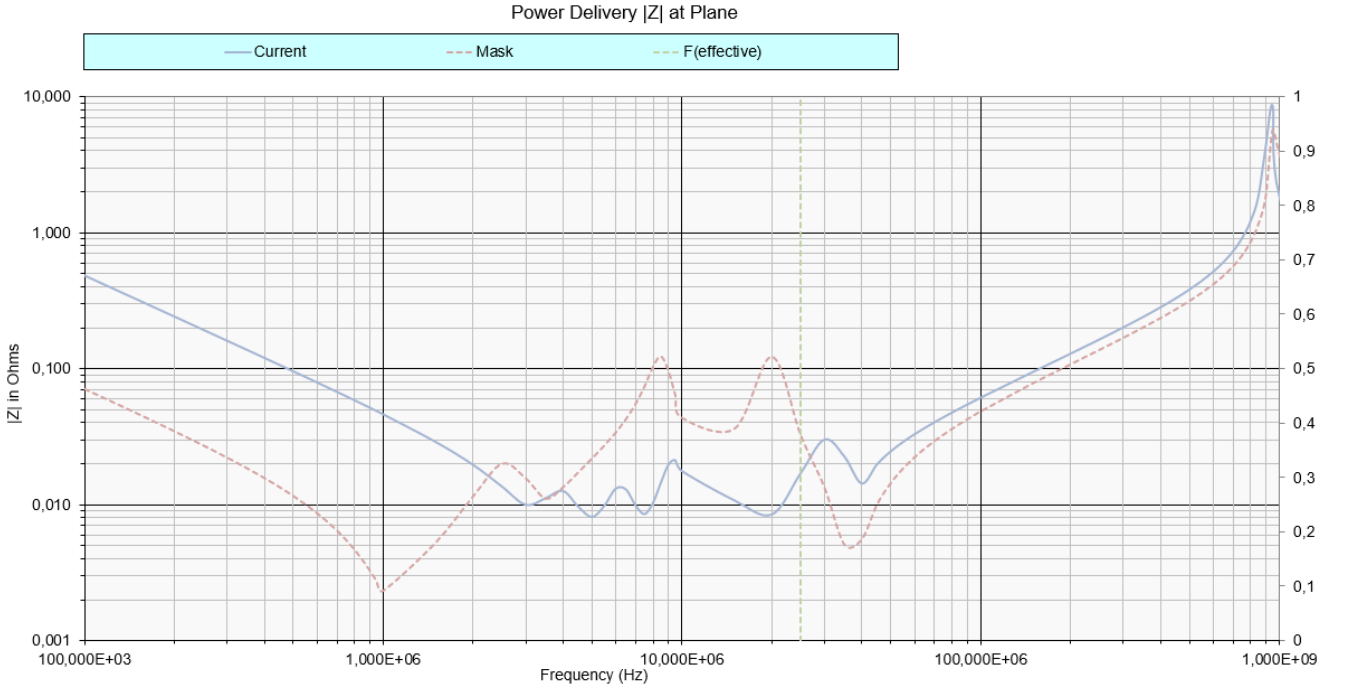
- SOC_DVDD1V8, allowable ripple would be -5.6%-(-1.5%) =-4.1% => Voltage Ripple for Z_{TARGET} become -2.05%

4.2.2.3 LPDDR4 PDN Ztarget

Z Target for LPDDR4						
Power Supply Rail name	Voltage Rail	% Ripple	Pmax	Imax (A)	Ztarget (ohm)	Ztarget selected (ohm)
VDD_DDR	1,1	1,1%		0,457	0,051	0,030
SOC_DVDD1V8	1,8	2,1%		0,004	19,895	0,100

4.2.2.4 LPDDR4 Decoupling V_1V1 (VDD_LPDDR)

xPERSO1	HUA43319	HUA15709	TME00744	xPERSO2	HUA25833	HUA42895	HUA31098	TME03438	1CAP005642	10N25V0201
47uF	22uF	10uF	4,7uF	2,2uF	1uF	470nF	220nF	100nF	47nF	10nF
6,3V	10V	10V	10V	10V	10V	10V	16V	6,3V	10V	25V
X7R	X5R	X7R	X5R	X5R	X7R	X7R	X7R	X5R	X7R	X7R
10,00%	20,00%	10,00%	10,00%	10,00%	10,00%	10,00%	10,00%	10,00%	10,00%	10,00%
#1 actual	#2 actual	#3 actual	#4 actual	#5 actual	#6 actual	#7 actual	#8 actual	#9 actual	#10 actual	#11 actual
0,84	0,87	1,04	0,91	0,87	1,14	1,06	1,05	0,92	1,01	0,99
39,622E-06	19,228E-06	10,380E-06	4,296E-06	1,923E-06	1,136E-06	497,260E-09	230,313E-09	92,032E-09	47,470E-09	9,912E-09
928,032E-12	928,032E-12	919,941E-12	838,555E-12	757,704E-12	928,032E-12	838,555E-12	838,555E-12	757,704E-12	838,555E-12	757,704E-12
3,000E-03	20,000E-03	4,000E-03	16,000E-03	8,000E-03	14,802E-03	20,000E-03	21,278E-03	30,000E-03	10,000E-03	70,000E-03
					1	2	2	4	6	4
2	2	2	2	2	2	2	2	2	2	2
1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09
400	400	400	400	400	400	400	400	400	400	400
1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12
2,046E-09	2,046E-09	2,038E-09	1,956E-09	1,875E-09	2,046E-09	1,956E-09	1,956E-09	1,875E-09	1,956E-09	1,875E-09
xPERSO1	HUA43319	HUA15709	TME00744	xPERSO2	HUA25833	HUA42895	HUA31098	TME03438	1CAP005642	10N25V0201



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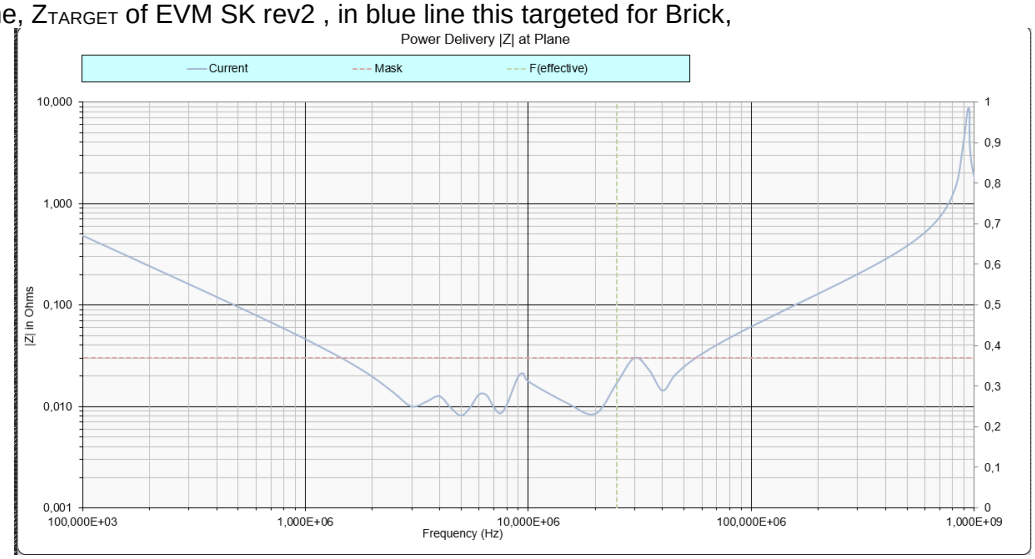
In dashed line, Z_{TARGET} of EVM SK rev2 , in blue line this targeted for Brick,



We're able to reach 0.030Ω. For low frequency <1MHz, PMIC will be localized close to LPDDR so we will benefit from its low frequency decoupling.

4.2.2.5 LPDDR4 Decoupling V_1V8IO (SOC_DVDD1V8)

HUA43319	HUA15709	TME00744	xPERSO2	HUA25833	HUA42895	HUA31098	TME03438	1CAP005642	10N25V0201
22uF	10uF	4,7uF	2,2uF	1uF	470nF	220nF	100nF	47nF	10nF
10V	10V	10V	10V	10V	10V	16V	6,3V	10V	25V
X5R	X7R	X5R	X5R	X7R	X7R	X7R	X5R	X7R	X7R
20,00%	10,00%	10,00%	10,00%	10,00%	10,00%	10,00%	10,00%	10,00%	10,00%
#1 actual	#2 actual	#3 actual	#4 actual	#5 actual	#6 actual	#7 actual	#8 actual	#9 actual	#10 actual
0,69	0,95	0,80	0,69	1,11	0,97	1,03	0,82	0,94	0,99
15,224E-06	9,540E-06	3,769E-06	1,522E-06	1,108E-06	457,780E-09	226,050E-09	82,286E-09	44,180E-09	9,856E-09
928,032E-12	919,941E-12	838,555E-12	757,704E-12	928,032E-12	838,555E-12	838,555E-12	757,704E-12	838,555E-12	757,704E-12
20,000E-03	4,000E-03	16,000E-03	8,000E-03	14,802E-03	20,000E-03	21,278E-03	30,000E-03	10,000E-03	70,000E-03
				1			4		4
2	2	2	2	2	2	2	2	2	2
1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09
400	400	400	400	400	400	400	400	400	400
1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12
2,046E-09	2,038E-09	1,956E-09	1,875E-09	2,046E-09	1,956E-09	1,956E-09	1,875E-09	1,956E-09	1,875E-09
HUA43319	HUA15709	TME00744	xPERSO2	HUA25833	HUA42895	HUA31098	TME03438	1CAP005642	10N25V0201

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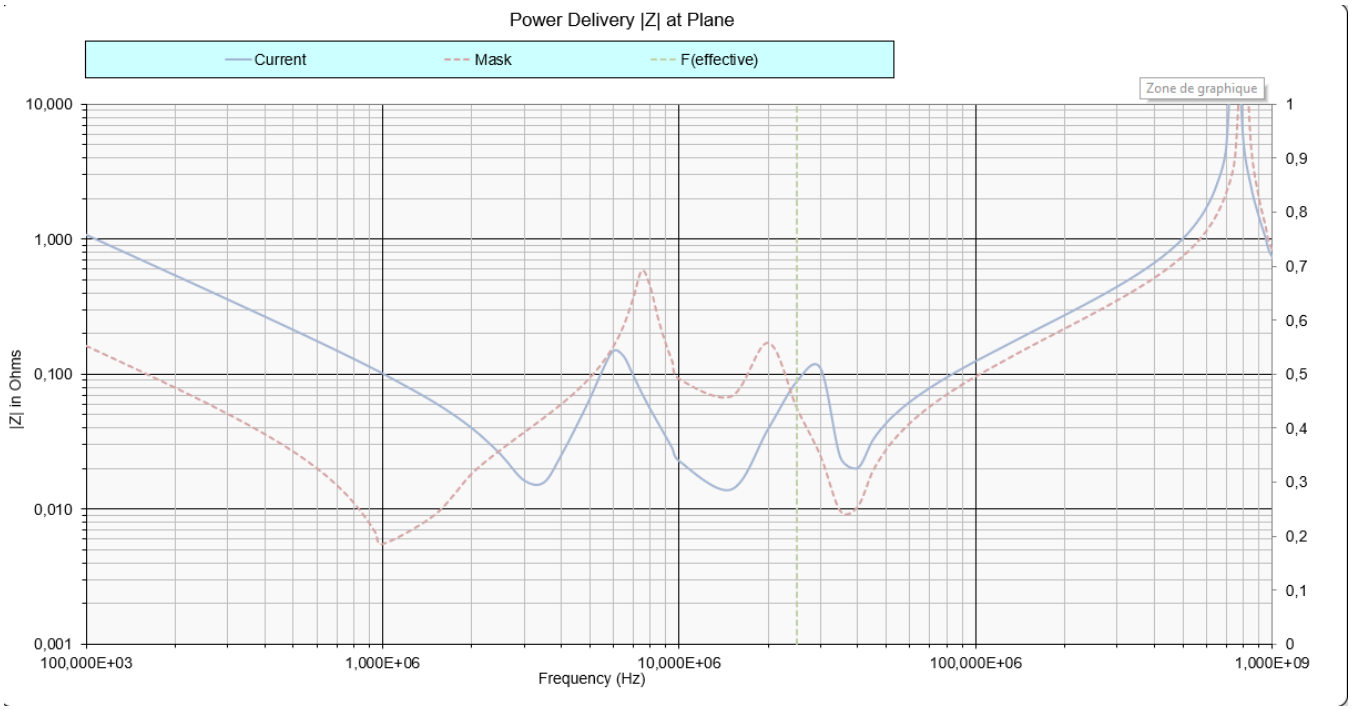
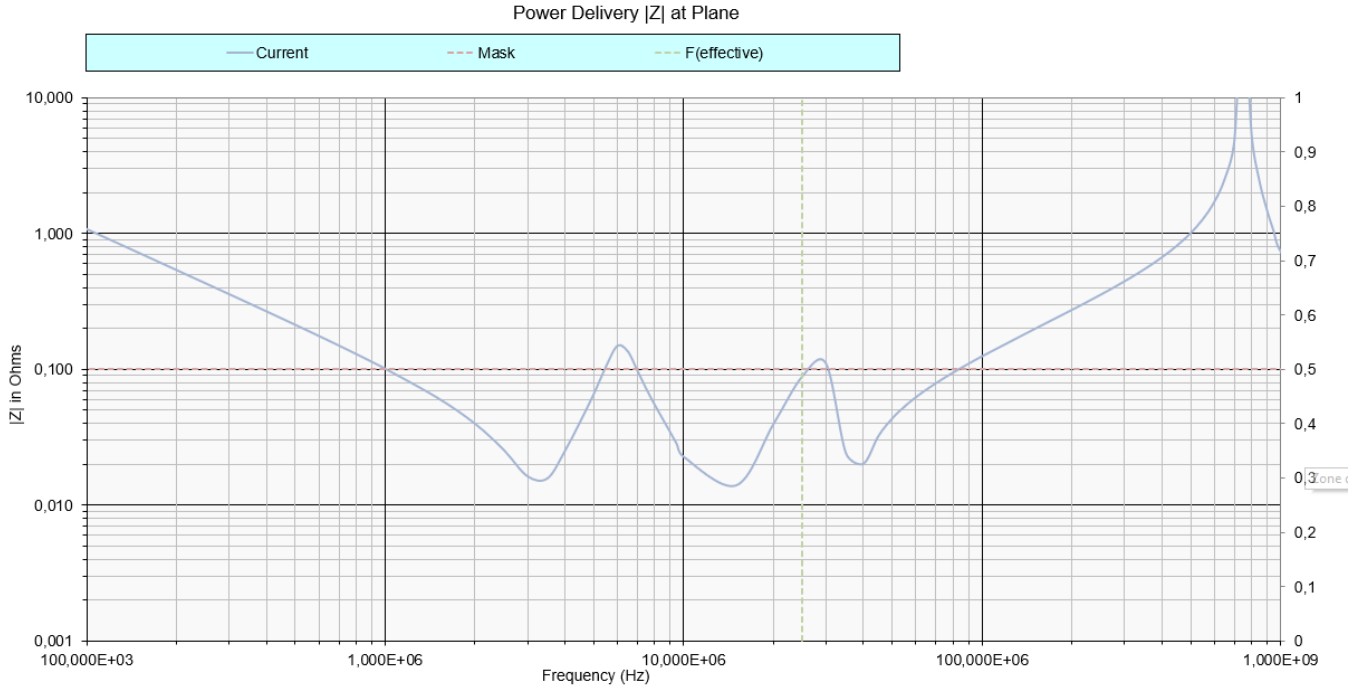


In dashed line, Z_{TARGET} of EVM SK rev2, in blue line this targeted for Brick



Just to remind: power consumption is about 3.8mA, Z_{TARGET} computed is about 38Ω set to 0.10Ω, so we can consider that we're able to reach 0.10Ω

4.2.2.6 Check LPDDR4 device between EVM SK rev2 and AM64 Brick

On EVM SK rev2 (LPDDR4 device MT53E1G16D1FW-046 WT:A) have this current consumption :

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V_{DD2} = 1.06–1.17V; V_{DDQ} = 1.06-1.17V; V_{DD1} = 1.70–1.95V

Symbol	Supply	T_C/4266 Mb/s		Unit	Note
		85°C	95°C		
I_{DD4R1}	V_{DD1}	4.50	4.70	mA	2, 3
I_{DD4R2}	V_{DD2}	270.00	285		
I_{DD4RQ}	V_{DDQ}	79.62	79.6		

On Brick (LPDDR4 MT53D512M16D1DS-046 AAT:D) we have such current consumption :

Parameter	Supply	T_C/4266 Mb/s			Unit	Note
		95°C	105°C	125°C		
I_{DD4R1}	V_{DD1}	3.8	3.8	4.7	mA	2, 3
I_{DD4R2}	V_{DD2}	380	380	390		
I_{DD4RQ}	V_{DDQ}	76.8	76.8	76.8		

Brick have cd VDD2+VDDQ power consumption higher of (380+76.8)/(285/79.6)=+25%

4.2.3 LPDDR4 pins recommendations

4.2.3.1 LPPDR4 signal termination

LPDDR4 signal memories have software configurable on die termination for the data groupnets. The DDR Subsystem of the AM6442 also contains software configurable on die termination for the address / control group nets. Thus, termination is not required on any DDR signals for an LPDDR4 configuration.

4.2.3.2 LPDDR4 VREF Routing

LPDDR4 memories generate their own VREFCA and VREFDQ internally for the address / command bus and data bus, respectively. Similarly, the DDR PHY also provides its own reference voltage for the data group nets during reads. Thus, unlike DDR3 and DDR4, VREF does not need to be generated on the board, and there is no required VREF routing for an LPDDR4 configuration.

4.2.3.3 LPDDR4 VTT

Unlike DDR3 and DDR4, there is no required termination on the PCB of the address/control bus of an LPDDR4 configuration. All termination is handled internally (on-die). Thus, VTT does not apply for LPDDR4.

4.2.3.4 LPDDR4 Data group topologies

The data line topology is always point-to-point for LPDDR4 implementations and is separated into two different byte routing groups. No need to match length both data byte0 and byte1.

4.2.3.5 LPDDR4 DDR0_CAL0

According to [REF2] this is I/O pad calibration resistor which need a 240Ω±1% 5.2mW tied to VSS => HUA28861 complies with that.

4.2.3.6 LPDDR4 RESET_N

This pin has no internal PU/PD, there is no specific recommendations. On TI EVM GP, this pin is PU to DDR4 voltage. On TI EVM SK this pin PD to VSS.

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We decide to PD moderately to VSS this pin for safety reasons: not let this net floating during power-on sequence.

On AM64 side this pin is not configurable, and there is no internal PU/PD.

4.2.3.7 LPDDR4 ODT (ODT_CA)

As it is strictly recommended in the document [REF8] ODT_CA is connected to VDD2 of LPDDR4 which corresponds to V_1V1.

4.2.3.8 LPDDR4 ZQ external calibration resistor

ZQ external resistor is 240 1% HUA28861 as recommended in below datasheet extract.

ZQ External Resistor, Tolerance, and Capacitive Loading

To use the ZQ CALIBRATION function, a 240 ohms, ±1% tolerance external resistor must be connected between the ZQ pin and V_{DDQ}.

If the system configuration shares the CA bus to form a x32 (or wider) channel, the ZQ pin of each die's x16 channel must use a separate ZQCAL resistor.

4.2.4 LPDDR4 Timing constraint

Following section detail the routing specification and layout guidelines applied to the LPDDR4 brick interface.

4.2.4.1 LPDDR4 Net Classes definition

Routing rules are applied to signals in groups called net classes. Each net class contains signals with same routing requirements. Below table lists the CLOCK net classes for the LPDDR4 interface as defined by TI.

Table 3-4. Clock Net Class Definitions

Clock Net Class	Processor Pin Names
CK	DDR0_CK0 / DDR0_CK0_n
DQS0	DDR0_DQS0 / DDR0_DQS0_n
DQS1	DDR0_DQS1 / DDR0_DQS1_n

Table 3-5. Signal Net Class Definitions

Signal Net Class	Associated Clock Net Class	Processor Pin Names
ADDR_CTRL	CK	DDR0_A[5:0], DDR0_CS0, DDR0_CKE0
BYTE0	DQS0	DDR0_DQ[7:0], DDR0_DM0
BYTE1	DQS1	DDR0_DQ[15:8], DDR0_DM1

Extract from [REF8]

4.2.4.2 LPDDR4 CLOCK and ADDR_CTRL routing specification

Below table lists the limits for the individual segments that comprise the routing from the AM6442 to the SDRAM.

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Table 3-6. CK and ADDR_CTRL Routing Specifications

Number	Parameter	MIN	MAX	UNIT
LP4_ACRS1	Propagation delay of net class CK, RSAC1		500(1)	ps
LP4_ACRS2	Propagation delay of net class ADDR_CTRL, RSAC2		500(1)	ps
LP4_ACRS3	Skew within net class CK (DDR0_CK0 to DDR0_CK0_n Skew)		0.4	ps
LP4_ACRS4	Skew across net class ADDR_CTRL (RSAC2)		3	ps
LP4_ACRS5	Skew across ADDR_CTRL net class and associated CK clock net class (RSAC1 to RSAC2)		3	ps
LP4_ACRS6	Vias per trace		3(1)	vias
LP4_ACRS7	Via count difference		1(2)	vias
LP4_ACRS8	Center-to-center CK to other LPDDR4 trace spacing(3)	4w		
LP4_ACRS9	Center-to-center ADDR_CTRL to other LPDDR4 trace spacing(3)	4w		
LP4_ACRS10	Center-to-center ADDR_CTRL to other ADDR_CTRL trace spacing(3)	3w		
LP4_ACRS11	CK center-to-center spacing(4) (5)	See notes below		
LP4_ACRS12	CK spacing to other net(3)	4w		

(1) Max value is based upon conservative signal integrity approach. This value could be extended only if detailed signal integrity analysis of rise time and fall time confirms desired operation.
(2) Via count difference may increase by 1 only if accurate 3-D modeling of the signal flight times – including accurately modeled signal propagation through vias – has been applied to ensure all segment skew maximums are not exceeded.
(3) Center-to-center spacing is allowed to fall to minimum 2w for up to 500 mils of routed length (only near endpoints).
(4) CK spacing set to ensure proper differential impedance.
(5) The user must control the impedance so that inadvertent impedance mismatches are not created. Generally speaking, center-to center spacing should be either 2w or slightly larger than 2w to achieve a differential impedance equal to twice the single-ended impedance, Zo, on that layer.

Extract from [REF8]

Configuration	TI max propagation delay	BRICK max propagation delay	Parameter
LPDDR4	500 ps	500 ps	Propagation delay of net class CK
LPDDR4	500 ps	500 ps	Propagation delay of net class ADDR_CTRL
LPDDR4	0,4 ps	0,4 ps	Skew within net class CK (Static Phase)
LPDDR4	3 ps	1,5 ps	Skew accross net class ADDR_CTRL
LPDDR4	3 ps	1,5 ps	Skew accross ADDR_CTRL net class and associated CK CLOCK net class

Configuration	TI MIN	BRICK MIN	Parameter
LPDDR4	4W	2W	LPDDR4 ADDR_CTRL Center to center spacing to all signals

Crosstalk analysis and Signal integrity power aware simulations have been performed. Results are inside the associated simulation reports.

4.2.4.3 LPDDR4 DATA group routing specification

Below table contains the routing specifications for the Byte0 and Byte1 routing groups. Each signal net class and its associated clock net class is routed and matched independently.

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It is not required nor recommended to match the lengths across all byte lanes. Length matching is only required within each byte.

Table 3-7. Data Group Routing Specifications

Number	Parameter	MIN	MAX	UNIT
LP4_DRS1	Propagation delay of net class DQSx (RSD1)		500	ps
LP4_DRS2	Propagation delay of net class BYTEx (RSD2)		500	ps
LP4_DRS3	Skew within net class DQSx (DDR0_DQSx to DDR0_DQSx_n skew)		0.4	ps
LP4_DRS4	Skew across net class DQSx and BYTEx (RSD1 to RSD2 skew)(1) (2)		2	ps
LP4_DRS5	Skew within net class BYTEx (DQ/DM to DQ/DM skew)(1)		2	ps
LP4_DRS6	Vias Per Trace		2(4)	vias
LP4_DRS7	Via Count Difference		0(3)	vias
LP4_DRS8	RSD1 center-to-center spacing (between clock net class)(5)	4w		
LP4_DRS9	RSD1 center-to-center spacing (within clock net class)(6) (7)	See notes below		
LP4_DRS10	RSD2 center-to-center spacing (between signal net class)(5)	4w		
LP4_DRS11	RSD2 center-to-center spacing (within signal net class)(5)	3w		

(1) Length matching is only done within a byte. Length matching across bytes is neither required nor recommended.
(2) Each DQS pair is length matched to its associated byte.
(3) Via count difference may increase by 1 only if accurate 3-D modeling of the signal flight times – including accurately modeled signal propagation through vias – has been applied to ensure DQn skew and DQSn to DQn skew maximums are not exceeded.
(4) Max value is based upon conservative signal integrity approach. This value could be extended only if detailed signal integrity analysis of rise time and fall time confirms desired operation.
(5) Center-to-center spacing is allowed to fall to minimum 2w for up to 500 mils of routed length (only near endpoints).
(6) DQS pair spacing is set to ensure proper differential impedance.
(7) The user must control the impedance so that inadvertent impedance mismatches are not created. Generally speaking, center-to center spacing should be either 2w or slightly larger than 2w to achieve a differential impedance equal to twice the single-ended impedance, Zo, on that layer.

Extract from [REF8]

Configuration	TI max propagation delay	BRICK max propagation delay	Parameter
LPDDR4	500 ps	500 ps	Propagation delay of net class DQSx
LPDDR4	500 ps	500 ps	Propagation delay of net class BYTEx
LPDDR4	0,4 ps	0,4 ps	Skew within net class DQSx (Static Phase)
LPDDR4	2 ps	1 ps	Skew accross net class DQSx and BYTEx
LPDDR4	2 ps	1 ps	Skew within net class BYTEx

Configuration	TI MIN	BRICK MIN	Parameter
LPDDR4	4W	2W	LPDDR4 DQSx and BYTEx Center to center spacing to all signals

4.2.4.4 LPDDR4 physical routing specification

To ensure good signaling performance, the following general board design guidelines are recommended by TI:

- Avoid crossing plane splits in the signal reference planes.
- Some signals require a ground (also called VSS) reference plane to obtain the needed signal integrity. Some may even need it on both sides.

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- Use the widest trace that is practical between decoupling capacitors and memory modules.
- Minimize inter-symbol interference (ISI) by keeping impedances matched.
- Minimize crosstalk by isolating sensitive signals, such as strobes and clocks, and by using a proper PCB
- stack-up.
- Avoid return path discontinuities by adding vias or capacitors whenever signals change layers and reference planes.
- Minimize reference voltage noise through proper isolation and proper use of decoupling capacitors on the reference input pins on the SDRAMs.
- Keep the signal routing stub lengths as short as possible.
- Add additional spacing for clock and strobe nets to minimize crosstalk.
- Maintain a common ground (VSS) reference for all bypass and decoupling capacitors.
- Consider the differences in propagation delays between microstrip and stripline nets when evaluating timing constraints.
- Via-to-via coupling can be a significant part of PCB-level crosstalk. GND shielding vias may need to be inserted between adjacent signal vias.
- Via stubs affect signal integrity. Via back-drilling may be required in some instances to improve signal integrity.

Table 1-1. PCB Stack-up Specifications

Number	Parameter	MIN	TYP	MAX	UNIT
PS1	PCB routing plus plane layers	6			
PS2	Signal routing layers	3			
PS3	Full VSS reference layers under DDR routing region (1)	1			
PS4	Full VDDS_DDR power reference layers under the DDR routing region (1)	1			
PS5	Number of reference plane cuts allowed within DDR routing region (2)			0	
PS6	Number of layers between DDR routing layer and reference plane (3)			0	
PS7	PCB routing feature size		4		Mils
PS8	PCB trace width, w		4		Mils
PS9	Single-ended impedance		40		Ω
PS10	Differential impedance		80		Ω
PS11	Impedance control (4)	Z-10%	Z	Z+10%	Ω

(1) Ground reference layers are preferred over power reference layers. Return signal vias need to be near layer transitions. When using power reference layers, include bypass caps to accommodate reference layer return current, as the trace routes switch routing layers.
(2) No traces should cross reference plane cuts within the DDR routing region. High-speed signal traces crossing reference plane cuts create large return current paths, which can lead to excessive crosstalk and EMI radiation. Beware of reference plane voids caused by via antipads, as these also cause discontinuities in the return current path.
(3) Reference planes are to be directly adjacent to the signal layer, to minimize the size of the return current loop.
(4) Z is the nominal singled-ended impedance selected for the PCB specified by PS9 and PS10.

Extract from [REF8]

	spracu1a TI recommendations	**BRICK SETTINGS**
Single Ended Impedance	40Ω±10%	40Ω±10%
Differential Impedance	80Ω±10%	Managed by physical constraint (not electrical)

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4.2.5 LPDDR4 On-Die Terminations

The ODT (On-Die Terminations) configuration must be managed by firmware.
The u-boot SPL firmware for A53 core is managing the LPDDR configuration of the JEDEC parameters.
The configuration is built based on a TI online tool available here: https://dev.ti.com/sysconfig/#/start

Firmware team is injecting the generated configuration through the Yocto recipes. Firmware documentation can be found here: https://pages.github.schneider-electric.com/MPU-platform/am64x

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4.3 NOR Flash

NOR Flash Implementation brick description
Following the requirement of flexibility and considering the possible use of XIP for very low-cost application of the brick we decided to implement the NOR interface on the OSPI.

AM6442 has only one OSPI interface and the supported / NOT supported features are described in the macro-component datasheet.

We have double implemented the NOR Flash for further application:

1. SPI usage,
2. QSPI usage,
3. OSPI usage.

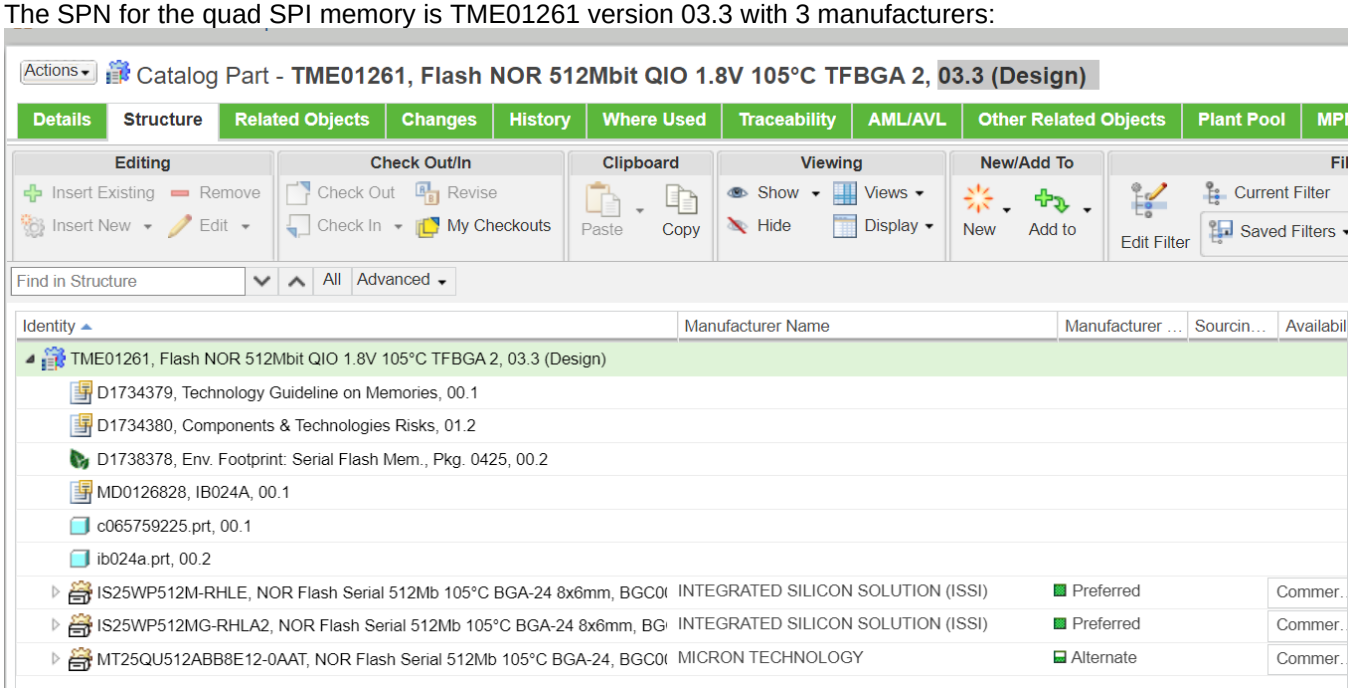
For SPI/QSPI operation, the following implementation is chosen:

- 1V8 voltage supply because it is the only voltage supported by NOR memory for HIGH-speed operation and OSPI compatibility (Double implementation pin to pin compatible on layout),
- Quad I/O capable chip,
- BGA24 pitch 1mm package because it is the package which is allowing the broadest range of densities among several suppliers, between 8MB and 256MB.

4.3.1 QSPI /OSPI Variant PCBA

4.3.1.1 Quad-SPI CONFIGURATION

The AM64xx Brick design supports both quad and octal memory.
The SPN for the quad SPI memory is TME01261 version 03.3 with 3 manufacturers:



1. ISSI: IS25WP512M-RHLE
2. ISSI: IS25WP512MG-RHLA2
3. Micron: MT25QU512ABB8E-0AAT

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Selected Quad SPI memories are fully pin to pin compatible and both support the JEDEC Standard No. 251 C chapter 5.4 xSPI Signal Protocols (Expanded Serial Peripheral Interface xSPI) protocol 1S-1S-1S SPI One IO signal used during command transfer, command modifier transfer, and data transfer. All phases are SDR.

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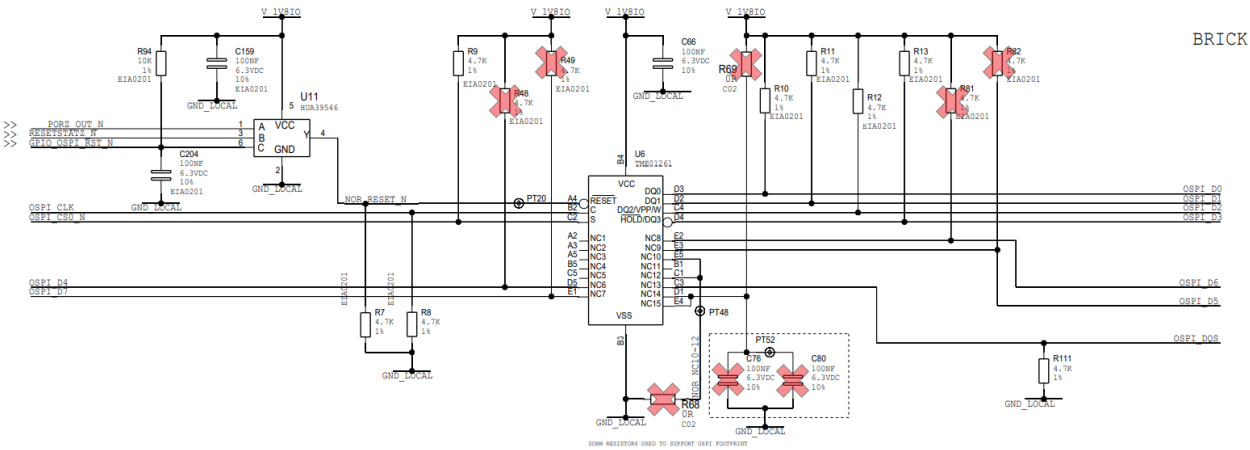
In case of using Quad SPI memory the following implementation regarding schematic is recommended:

MEMORY, QSPI NOR FLASH



QSPI BOM Configuration:

- U6 -> TME01261
- R48 -> NOT POPULATED
- R49 -> NOT POPULATED
- R68 -> NOT POPULATED
- R69 -> NOT POPULATED
- R81 -> NOT POPULATED
- R82 -> NOT POPULATED
- C76 -> NOT POPULATED
- C80 -> NOT POPULATED

4.3.1.2 Octal-SPI CONFIGURATION

The reference device for the octal-SPI memory is Micron's MT35XU512ABA1G12-0AAT (no SPN assigned already).
This device has an internal ECC engine and the pin A5 (which is RFU = Reserved for Future Use in the quad-SPI version) is an INT# output open drain (recommended external PUs 2.5kOhm).

When ECC engine detects an internal ECC event it generates an interrupt. If the INT# (A5) pin function is enabled, the interrupt is sent to the host. Need to underline the fact that this pin is OPTIONAL, if its function is not enabled, the pin can be left floating.
It was decided to not over constraint the brick design by outputting the pin A5, so this pin is located close to the brick edge and available to user which could need it.

As today no user clearly identified to support OSPI on NOR Flash with the ECC engine usage we decided not to implement this function on the BRICK.

The selected octal memory features:

- compliance to Jedec xSPI standard (JESD251) as reported on the 1st page of the datasheet
- Single die
- 512Mb density
- 24-ball T-PBGA 5x5
- Automotive grade
- Has internal ECC engine (not used)

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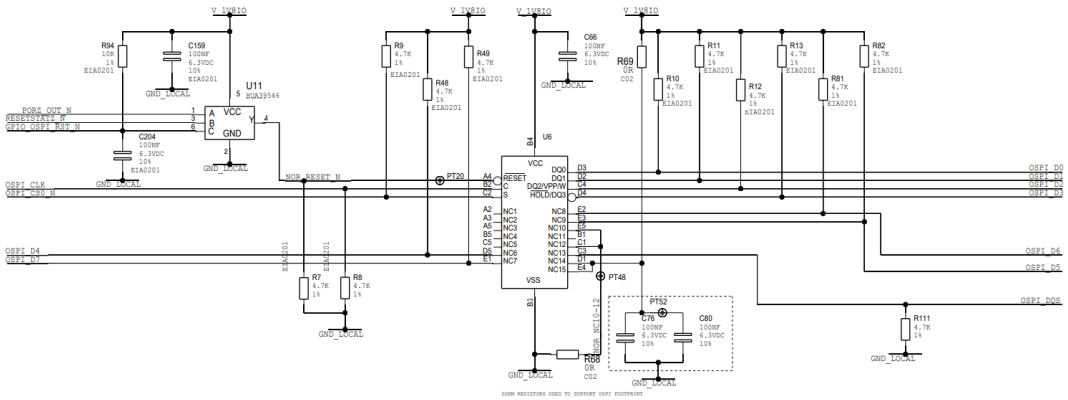
- Operating temp -40 to 105
- Max freq: 166MHz (166Mbps) in SDR mode and 200MHz (400Mbps) in DDR mode
- XIP
- Sector size: 128KB
- Boot in SDRx1
- Support Octal DDR protocol
- Support Extended SPI protocol with octal commands
- Already in production since 2017

In case of using OSPI memory the following implementation regarding schematic is recommended:

MEMORY,OSPI NOR FLASH



OSPI BOM Configuration:

- U6 -> MT35XU512ABA1G12-0AAT

4.3.2 NOR Flash GPIO_OPSI_RST_N

This signal is not driven nor PU/PD during and after reset. We put a 10KΩ externally. There is no SW necessary for this with PU/PD.

4.3.3 Power Rail Decoupling

4.3.3.1 Max power consumption

According to ISSI max current consumption is about:

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9.3 DC CHARACTERISTICS

(Under operating range)

Symbol	Parameter		Condition		Min	Typ[2]	Max	Units
I_{CC1}	V_{CC} Active Read current[3]		NORD			13	16	mA
			FRD Single at 133MHz			16	20	
			FRD Dual at 133MHz			18	22	
			FRD Quad at 133MHz			22	27	
			FRD Single at 104MHz			15	19	
			FRD Dual at 104MHz			17	21	
			FRD Quad at 104MHz			20	24	
			FRD Single DTR at 66MHz			15	19	
			FRD Dual DTR at 66MHz			17	21	
			FRD Quad DTR at 66MHz			21	26	
I_{CC2}	V_{CC} Program Current		CE# = V_{CC}	85°C		30	35	mA
				105°C			35	
				125°C			35	
I_{CC3}	V_{CC} WRSR Current		CE# = V_{CC}	85°C		60	80	
				105°C			80	
				125°C			80	
I_{CC4}	V_{CC} Erase Current (SER/4SER/BER32/4BER32/ BER64/4BER64)		CE# = V_{CC}	85°C		30	35	
				105°C			35	
				125°C			35	
I_{CC5}	V_{CC} Erase Current (CE)		CE# = V_{CC}	85°C		60	80	
				105°C			80	
				125°C			80	
I_{SB1}	V_{CC} Standby Current CMOS	IS25LP	CE# = V_{CC}, V_{IN} = GND or V_{CC} [4]	85°C		21	90[6]	µA
				105°C			140[6]	
				125°C			260	
		IS25WP		85°C		21	90[6]	uA
				105°C			140[6]	
				125°C			260	
I_{SB2}	Deep power down current	IS25LP	CE# = V_{CC}, V_{IN} = GND or V_{CC} [4]	85°C		17	35[6]	µA
				105°C			50[6]	
				125°C			90	
		IS25WP		85°C		1	35[6]	
				105°C			50[6]	
				125°C			90	
I_{LI}	Input Leakage Current		V_{IN} = 0V to V_{CC}				±2[5]	µA
I_{LO}	Output Leakage Current		V_{IN} = 0V to V_{CC}				±2[5]	µA
V_{IL}[1]	Input Low Voltage				-0.5		$0.3V_{CC}$	V
V_{IH}[1]	Input High Voltage				$0.7V_{CC}$		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage		I_{OL} = 100 µA				0.2	V
V_{OH}	Output High Voltage		I_{OH} = -100 µA		V_{CC} - 0.2			V

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According to MICRON max current consumption is about:

DC Characteristics and Operating Conditions

Table 48: DC Current Characteristics and Operating Conditions

Notes apply to entire table.

Parameter	Symbol	Test Conditions	Typ	Max	Unit
Input leakage current	I_{LI}		–	±2	µA
Output leakage current	I_{LO}		–	±2	µA
Standby current (IT range)	I_{CC1}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	20	100	µA
Standby current (AT range)		S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	20	200	µA
Standby current (UT range)		S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	20	300	µA
Deep power-down current (IT range)	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	2	50	µA
Deep power-down current (AT range)		S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	5	100	µA
Deep power-down current (UT range)		S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	5	150	µA
Operating current (fast-read extended I/O)	I_{CC3}	C = 0.1V_{CC}/0.9V_{CC} at 166 MHz, DQ1 = open	–	20	mA
		C = 0.1V_{CC}/0.9V_{CC} at 54 MHz, DQ1 = open	–	8	mA
Operating current (fast-read dual I/O)		C = 0.1V_{CC}/0.9V_{CC} at 166 MHz, DQ = open	–	25	mA
Operating current (fast-read quad I/O), IT and AT range		C = 0.1V_{CC}/0.9V_{CC} at 166 MHz STR or 80 MHz DTR, DQ = open	–	28	mA
		C = 0.1V_{CC}/0.9V_{CC} at 90 MHz DTR, DQ = open	–	31	mA
Operating current (fast-read quad I/O), UT range		C = 0.1V_{CC}/0.9V_{CC} at 133 MHz STR or 80 MHz DTR, DQ = open	–	28	mA
Operating current (PROGRAM operations)	I_{CC4}	S# = V_{CC}	–	35	mA
Operating current (WRITE operations)	I_{CC5}	S# = V_{CC}	–	35	mA
Operating current (erase)	I_{CC6}	S# = V_{CC}	–	35	mA

Notes:
1. All currents are RMS unless noted. Typical values at typical V_{CC} (3.0/1.8V); V_{IO} = 0V/V_{CC}; T_C = +25°C.
2. Standby current is the average current measured over any time interval 5µs after S de-assertion (and any internal operations are complete).
3. Deep power-down current is the average current measured 5ms over any 5ms time interval, 100µs after the ENTER DEEP POWER-DOWN operation (and any internal operations are complete).
4. All read currents are the average current measured over any 1KB continuous read. No load, checker-board pattern.
5. All program currents are the average current measured over any 256-byte typical data program.

On EVM SK board decoupling is done by bulk 4.7µF+3x100nF for OSPI INFINEON S28HS512TGABHM010 (typical current= 50mA).

Schematics anticipate the use of OSPI (MICRON MT35XU512ABA1G12-0AAT)

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According to MT35XU512ABA1G12-0AAT datasheet max current consumption is about:

DC Characteristics and Operating Conditions

Table 48: DC Current Characteristics and Operating Conditions

Note 1 applies to entire table

Parameter	Symbol	Test Conditions	Typ	Max	Unit	Notes
Input leakage current	I_{LI}	–	–	±2	µA	
Output leakage current	I_{LO}	–	–	±2	µA	
Standby current (IT range)	I_{CC1}	$S = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}	25	100	µA	2
Standby current (AT range)	I_{CC1}	$S = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}	25	200	µA	2
Standby current (UT range)	I_{CC1}	$S = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}	25	300	µA	2
Deep power-down current (IT range)	I_{CC2}	$S = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}	2	50	µA	3
Deep power-down current (AT range)	I_{CC2}	$S = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}	2	100	µA	3
Deep power-down current (UT range)	I_{CC2}	$S = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}	2	150	µA	3
Operating current (FAST READ EXTENDED I/O)	I_{CC3}	$C = 0.1\ V_{CC}/0.9V_{CC}$ at 133 MHz, DQ1 = open	–	16	mA	4
		$C = 0.1\ V_{CC}/0.9V_{CC}$ at 54 MHz, DQ1 = open	–	8	mA	4
Operating current (Octal SDR command)		$C = 0.1\ V_{CC}/0.9V_{CC}$ at 166 MHz, DQ = open	–	60	mA	
Operating current (Octal DDR command)		$C = 0.1\ V_{CC}/0.9V_{CC}$ at 200 MHz, DQ = open	–	70	mA	
Operating current (PROGRAM operations)	I_{CC4}	$S\# = V_{CC}$	–	40	mA	5
Operating current (WRITE operations)	I_{CC5}	$S\# = V_{CC}$	–	24	mA	
Operating current (ERASE operations)	I_{CC6}	$S\# = V_{CC}$	–	35	mA	

Notes: 1. Currents are RMS unless noted. Typical values are at V_{CC} (1.8V); $V_{IO} = 0V/V_{CC}$; $T_C = +25°C$.
2. Standby current is an average calculated 5µs after S# deassertion and completion of any internal operation.
3. Deep power-down current is an average calculated during a 5ms time interval 100µs after completion of any internal operation.
4. Read current is an average calculated during a 1KB continuous READ operation without load, in a checker-board pattern.
5. Program current is an average measured over a 256-byte data PROGRAM operation.

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4.3.3.2 Voltage Ripple

PMIC OUTPUT TOLERANCE						
PMIC output	Chip Power rail name	Voltage (Volt)	Voltage Tolerance (Volt)		Voltage Tolerance (%)	
		Typ	Min	Max	Min	Max
BUCK2	SOC_DVDD1V8	1,8			-1,5%	1,5%

According to ISSI datasheet IS25WP512M (ISSI_25LX-WX512M.pdf) Vcc_{MIN} = 1.65V

According to MICRON datasheet MT25QU512ABB8E12-0AAT (TME01261_micron_mt25qu512abb.pdf) Vcc_{MIN}= 1.7V

Worst case tolerance take into account :1.7V :

QSPI NOR FLASH POWER SUPPLY TOLERANCE						
Powered by	Chip Power rail name	Voltage (Volt)	Voltage Tolerance (Volt)		Voltage Tolerance (%)	
		Typ	Min	Max	Min	Max
V_1V8IO	SOC_DVDD1V8	1,8	1,7	2	-5,6%	11,1%

SOC_DVDD1V8, allowable ripple would be -5.6%-(-1.5%)=-4.1% => Voltage Ripple for Z_{TARGET} become -2.05%

4.3.3.3 Ztarget

Let's maximize current consumption from 80mA to 100mA (to take in consideration future OSPI NOR Flash double with margin to anticipate changes on consumption)

Z TARGET FOR NOR QSPI						
Power Supply Rail name	Voltage Rail	% Ripple	Pmax	Imax (A)	Ztarget (ohm)	Ztarget selected (ohm)
SOC_DVDD1V8	1,8	2,1%		0,100	0,738	0,200

This makes Z_{TARGET} to 0,2Ω.

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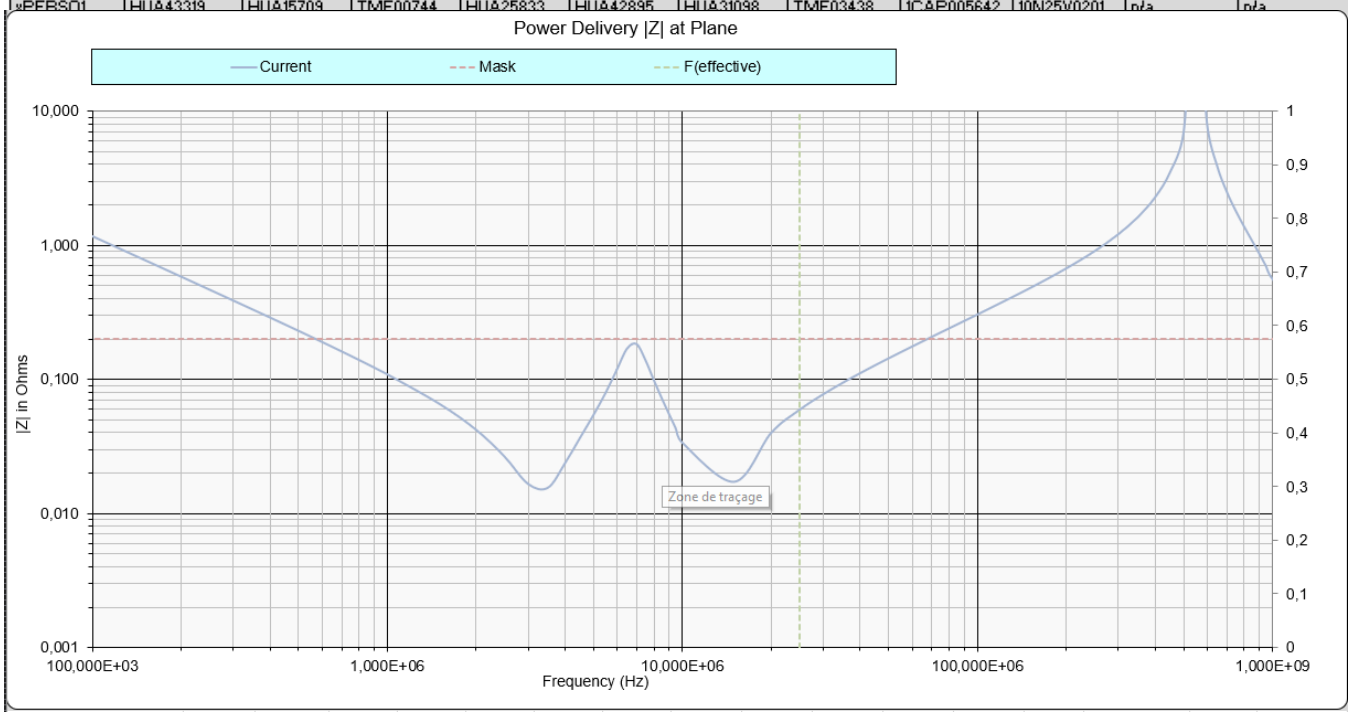
4.3.3.4 Decoupling V_1V8IO (SOC_DVDD1V8)

CapA #1	CapA #2	CapA #3	CapA #4	CapA #5	CapA #6	CapA #7	CapA #8	CapA #9	CapA #10	CapA #11	CapA #12
xPERSO1	HUA43319	HUA15709	TME00744	HUA25833	HUA42895	HUA31098	TME03438	1CAP005642	10N25V0201		
47uF	22uF	10uF	4,7uF	1uF	470nF	220nF	100nF	47nF	10nF		
6,3V	10V	10V	10V	10V	10V	16V	6,3V	10V	25V		
X7R	X5R	X7R	X5R	X7R	X7R	X7R	X5R	X7R	X7R		
10,00%	20,00%	10,00%	10,00%	10,00%	10,00%	10,00%	10,00%	10,00%	10,00%		
#1 actual	#2 actual	#3 actual	#4 actual	#5 actual	#6 actual	#7 actual	#8 actual	#9 actual	#10 actual	#11 actual	#12 actual
0,66	0,69	0,95	0,80	1,11	0,97	1,03	0,82	0,94	0,99		
30,819E-06	15,224E-06	9,540E-06	3,769E-06	1,108E-06	457,780E-09	226,050E-09	82,286E-09	44,180E-09	9,856E-09		
928,032E-12	928,032E-12	919,941E-12	838,555E-12	928,032E-12	838,555E-12	838,555E-12	757,704E-12	838,555E-12	757,704E-12		
3,000E-03	20,000E-03	4,000E-03	16,000E-03	14,802E-03	20,000E-03	21,278E-03	30,000E-03	10,000E-03	70,000E-03		
				1			3				
2	2	2	2	2	2	2	2	2	2	2	2
1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09		
400	400	400	400	400	400	400	400	400	400	400	400
1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12
2,046E-09	2,046E-09	2,038E-09	1,956E-09	2,046E-09	1,956E-09	1,956E-09	1,875E-09	1,956E-09	1,875E-09		
xPERSO1	HUA43319	HUA15709	TME00744	HUA25833	HUA42895	HUA31098	TME03438	1CAP005642	10N25V0201	n/a	n/a



4.3.4 NOR Flash Timing Constraint

Brick embeds timing constraint on NOR Flash which is defined below.

4.3.4.1 NOR Flash supported physical implementation

Considering layout constraint brick can't support all sampling mode embeds in the AM64xx. The brick PCB Layout only support those listed sampling methods:

1. No loopback, Internal PHY Loopback and internal Pad Loopback
    a. The xSPI Clock output pin of the AM64xx must be connected to the Clock input pin of the attached xSPI memory,
    b. The signal propagation delay from the xSPI Clock output of the AM64xx to the attached memory Clock input buffer must be equal or less than 450ps,

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2. DQS (only available in Octal SPI devices)
    a. The OSPI Clock output pin of the AM64xx must be connected to the Clock input pin of the attached OSPI memory,
    b. The DQS pin of the AM64xx must be connected to the DQS input buffer memory.

4.3.4.2 NOR Flash **NOT** supported physical implementation

External Board Loopback is neither supported nor implemented in the brick. PCB Layout constraint is too important and can't be compatible with other sampling mode supported.

4.3.4.3 NOR Flash Timing constraint manager

According to the datasheet of the AM64xx the most important timing constraint is the Octal SPI DQS application (not Quad SPI).

Table 7-92. OSPI0 Timing Conditions

PARAMETER		MODE	MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate		1	6	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance		3	10	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(Trace\ Delay)}$	Propagation delay of OSPI0_CLK trace	No Loopback Internal PHY Loopback Internal Pad Loopback		450	ps
	Propagation delay of OSPI0_LBCLKO trace	External Board Loopback	2L(1) - 30	2L(1) + 30	ps
	Propagation delay of OSPI0_DQS trace	DQS	L(1) - 30	L(1) + 30	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch of OSPI0_D[7:0] and OSPI0_CSn[3:0] relative to OSPI0_CLK	All modes		60	ps

(1) L = Propagation delay of OSPI0_CLK trace

Configuration	TI max propagation delay	BRICK max propagation delay	TI matching delay	BRICK matching delay
QSPI / SPI	450ps	400ps	CLOCK target, ±60ps for xSPI_DAT[x], xSPI_CS[x]	CLOCK target, ±20ps for xSPI_DAT[x], xSPI_CS[x]
OSPI	450ps	400ps	CLOCK target, ±60ps for xSPI_DAT[x], xSPI_CS[x] CLOCK target, ±30ps for DQS	CLOCK target, ±20ps for xSPI_DAT[x], xSPI_CS[x] CLOCK target, ±20ps for DQS

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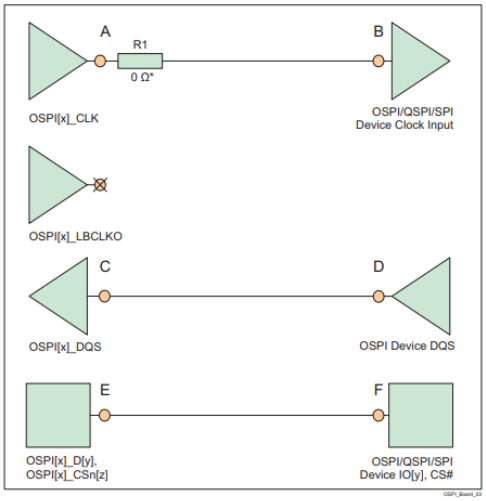
9.2.2.3 DQS (only available in Octal SPI devices)

- The OSPI[x]_CLK output pin must be connected to the CLK input pin of the attached OSPI/QSPI/SPI device
- The DQS pin of the attached OSPI/QSPI/SPI device must be connected to OSPI[x]_DQS pin
- The signal propagation delay from the attached OSPI/QSPI/SPI device DQS pin to the OSPI[x]_DQS pin (D to C) must be approximately equal to the signal propagation delay from the OSPI[x]_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B)
- The signal propagation delay of each OSPI[x]_D[y] and OSPI[x]_CSn[z] pin to the corresponding attached OSPI/QSPI/SPI device data and control pin (E to F, or F to E) must be approximately equal to the signal propagation delay from the OSPI[x]_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B)
- 50 Ω PCB routing is recommended along with series terminations, as shown in Figure 9-3
- Propagation delays and matching:
  - (D to C) = ((A to B) ± 30 ps)
  - (E to F, or F to E) = ((A to B) ± 60 ps)

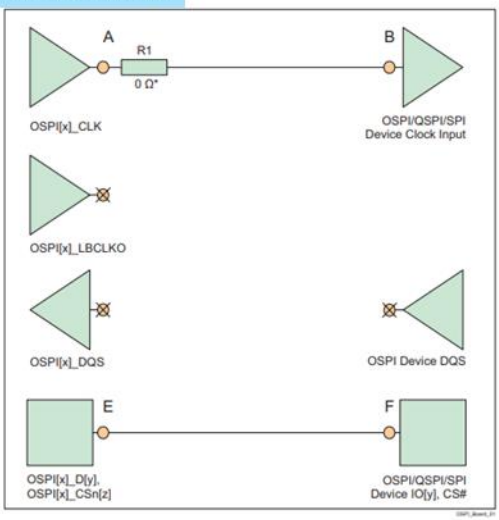


* 0 Ω resistor (R1), located as close as possible to the OSPI[x]_CLK pin, is a placeholder for fine tuning, if needed.

Figure 9-3. OSPI Connectivity Schematic for DQS

9.2.2.1 No Loopback, Internal PHY Loopback, and Internal Pad Loopback

- The OSPI[x]_CLK output pin must be connected to the CLK input pin of the attached OSPI/QSPI/SPI device
- The signal propagation delay from the OSPI[x]_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B) must be ≤ 450 ps (~7cm as stripline or ~8cm as microstrip)
- The signal propagation delay of each OSPI[x]_D[y] and OSPI[x]_CSn[z] pin to the corresponding attached OSPI/QSPI/SPI device data and control pin (E to F, or F to E) must be approximately equal to the signal propagation delay from the OSPI[x]_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B)
- 50 Ω PCB routing is recommended along with series terminations, as shown in Figure 9-1
- Propagation delays and matching:
  - (A to B) ≤ 450 ps
  - (E to F, or F to E) = ((A to B) ± 60 ps)



* 0 Ω resistor (R1), located as close as possible to the OSPI[x]_CLK pin, is placeholder for fine tuning, if needed.

Figure 9-1. OSPI Connectivity Schematic for No Loopback, Internal PHY Loopback, and Internal Pad Loopback

Extract from [REF2]

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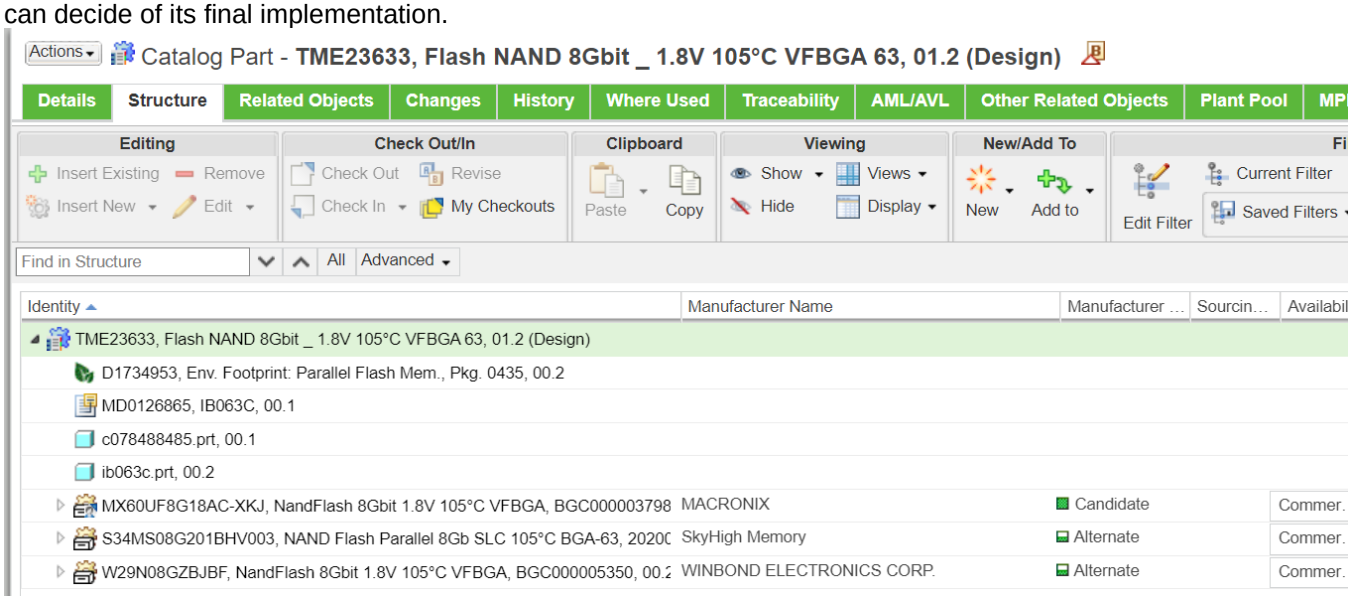
4.4 NAND flash

The AM6442 has 1 General Purpose Memory Controller interfaced with NAND.
The NAND memory is included in the macro component TME23633 version 01.2 but it can be modified, and user can decide of its final implementation.



Currently, the TME23633 contains 3 MPNs:

- Macronix MX60UF8G18AC-XKJ
- SkyHigh S34MS08G201BHV003
- Winbond Electronics W29N08GZBJBF

The following implementation is chosen:

- 1V8 voltage, 3V3 operation can be supported (user must adapt NAND reference and bank voltage attribution on AM64xx),
- VFBGA63 standard package because:
  - The VFBGA is only 9x11mm.
  - Among all the recommended suppliers (Winbond, SkyHigh, Macronix…), it has been checked that all the package/density/voltages combinations are existing in the most common density range (i.e. from 1 to 8Gb).

Only Specific parameter of this design is the pull up resistors applied to the following signals:

- NAND_CE_N -> Pull up resistor 4.7K to V_1V8IO,
- NAND_RB_N -> Pull up resistor 4.7K to V_1V8IO,
- NAND_WP_N -> Pull down resistor 2.4K to GND_LOCAL.

4.4.1 NAND Flash Timing Constraint

Brick embeds timing constraint on NAND Flash which is defined below.

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4.4.1.1 NAND Flash supported physical implementation

The physical layout implementation support NAND Flash asynchronous mode.

4.4.1.2 NAND Flash Timing constraint manager

Table 7-51. GPMC Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate		1.65	4	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance		5	20	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(Trace\ Delay)}$	Propagation delay of each trace	133 MHz Synchronous Mode	140	360	ps
		All other modes	140	720	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces			200	ps

Extract from AM64x Sitara™ Processors datasheet (Rev. E) am6442.pdf

Configuration	TI max propagation delay	BRICK max propagation delay	TI matching delay	BRICK matching delay
NAND	720ps	650ps	200ps propagation delay mismatch across all traces	100ps propagation delay mismatch across all traces

4.4.2 NAND Flash Max Power consumption

TME23633:
MICRON MT29F8G08ADBFAH4-AAT:F

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Sequential read current ECC off	$^tRC = {}^tRC$ (MIN); CE# = V_{IL}; I_{OUT} = 0mA	I_{CC1}	–	13	20	mA	1, 2
Sequential read current ECC on	$^tRC = {}^tRC$ (MIN); CE# = V_{IL}; I_{OUT} = 0mA	I_{CC1}	–	25	35	mA	2, 6
Program current ECC off	–	I_{CC2}	–	13	20	mA	1, 2
Program current ECC on	–	I_{CC2}	–	20	25	mA	2, 6
Erase current	–	I_{CC3}	–	15	20	mA	1, 2, 6

SKYHIGH S34MS08G201BHV003.pdf

Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
Power On Current		I_{CC0}	FFh command input after power on	—	—	50 per device	mA
Operating Current	Sequential Read	I_{CC1}	$t_{RC} = t_{RC}$ (min) CE# = V_{IL}, I_{OUT} = 0 mA	—	15	30	
	Program	I_{CC2}	Normal	—	15	30	
			Cache	—	15	30	
	Erase	I_{CC3}	—	—	15	30	

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4.4.2.1 Voltage Ripple

PMIC OUTPUT TOLERANCE						
PMIC output	Chip Power rail name	Voltage (Volt)	Voltage Tolerance (Volt)		Voltage Tolerance (%)	
		Typ	Min	Max	Min	Max
BUCK2	SOC_DVDD1V8	1,8			-1,5%	1,5%

According to datasheet MICRON MT29F8G08ADBFAH4 (TME01645_MICRON_MT29F8G08ADBFAH4.pdf)
Vcc_{MIN}= 1.7V

According to datasheet SKYHIGH S34MS08G201BHV003 (TME01645_SKYHIGH_S34MS08G201BHV003.pdf)
Vcc_{MIN}= 1.7V

NAND FLASH POWER SUPPLY TOLERANCE						
Powered by	Chip Power rail name	Voltage (Volt)	Voltage Tolerance (Volt)		Voltage Tolerance (%)	
		Typ	Min	Max	Min	Max
V_1V8IO	SOC_DVDD1V8	1,8	1,7	1,95	-5,6%	8,3%

SOC_DVDD1V8, allowable ripple would be -5.6%-(-1.5%) =-4.1% => Voltage Ripple for Z_{TARGET} become -2.05%

4.4.2.2 Ztarget

Let's maximize current consumption from 35mA to 100mA (to take in consideration future NAND Flash capacity)

Z TARGET FOR NOR QSPI						
Power Supply Rail name	Voltage Rail	% Ripple	Pmax	Imax (A)	Ztarget (ohm)	Ztarget selected (ohm)
SOC_DVDD1V8	1,8	2,1%		0,100	0,738	0,200

This makes Z_{TARGET} to 0,2Ω.

4.4.2.3 Decoupling V_1V8IO (SOC_DVDD1V8)

xPERSO1	HUA43319	HUA15709	TME00744	HUA25833	HUA42895	HUA31098	TME03438	1CAP005642	10N25V0201	TME10670
47uF	22uF	10uF	4,7uF	1uF	470nF	220nF	100nF	47nF	10nF	1uF
6,3V	10V	10V	10V	10V	10V	16V	6,3V	10V	25V	6,3V
X7R	X5R	X7R	X5R	X7R	X7R	X7R	X5R	X7R	X7R	X6S
10,00%	20,00%	10,00%	10,00%	10,00%	10,00%	10,00%	10,00%	10,00%	10,00%	20,00%
#1 actual	#2 actual	#3 actual	#4 actual	#5 actual	#6 actual	#7 actual	#8 actual	#9 actual	#10 actual	#11 actual
0,66	0,69	0,95	0,80	1,11	0,97	1,03	0,82	0,94	0,99	0,83
30,819E-06	15,224E-06	9,540E-06	3,769E-06	1,108E-06	457,780E-09	226,050E-09	82,286E-09	44,180E-09	9,856E-09	831,429E-09
928,032E-12	928,032E-12	919,941E-12	838,555E-12	928,032E-12	838,555E-12	838,555E-12	757,704E-12	838,555E-12	757,704E-12	757,704E-12
3,000E-03	20,000E-03	4,000E-03	16,000E-03	14,802E-03	20,000E-03	21,278E-03	30,000E-03	10,000E-03	70,000E-03	9,000E-03
					2		1			
2	2	2	2	2	2	2	2	2	2	2
1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09	1,118E-09
400	400	400	400	400	400	400	400	400	400	400
1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12	1,397E-12
2,046E-09	2,046E-09	2,038E-09	1,956E-09	2,046E-09	1,956E-09	1,956E-09	1,875E-09	1,956E-09	1,875E-09	1,875E-09
xPERSO1	HUA43319	HUA15709	TME00744	HUA25833	HUA42895	HUA31098	TME03438	1CAP005642	10N25V0201	TME10670

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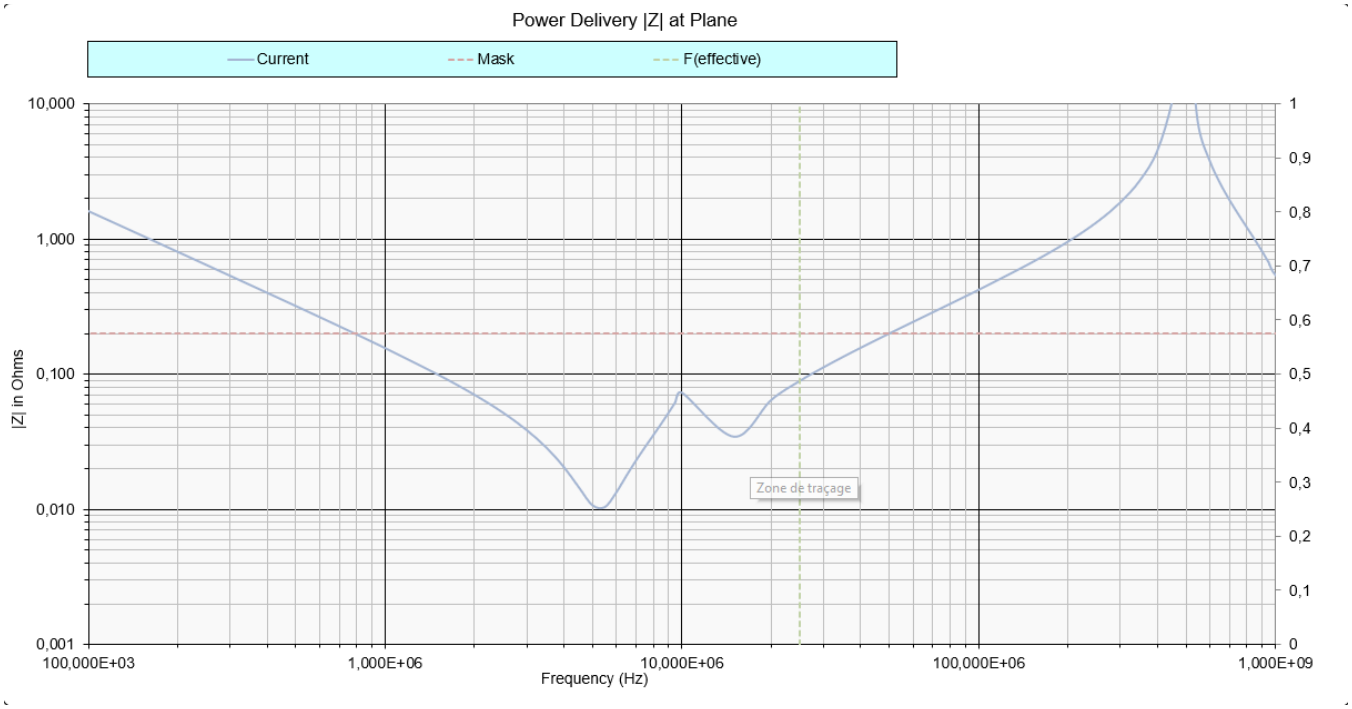

4.5 TPM

4.5.1 TPM choice

Corporate decided to advise us the usage of TME03151 version 0.3.2 as ST33HTPH2X32AHD8. As the TPM could be shared by another peripheral added by the final user we dedicated the interface of the TPM on the SPI0 of the AM64xx.

TME03151, MCU ARM SecurCore SC300 290kB VQFN 32, 03.2 (Design)				
D1748821, TPM-FAIL Vulnerability, 01.2				
D1748829, EME Lab Report 183605H-1, 00.1				
D1748830, Environment Footprint_Micro_VQFN_Package, 00.2				
D1753672, TN1309 ST33TPHF2xyyy security, 00.1				
D2962749, IF032HM1NV, 00.1				
D2964219, Refusal of a second source to SPN TME031, 00.1				
MD0128191, IF032HM1, 00.2				
c030504038.prt, 00.2				
if032hm1.prt, 00.5				
if032hm1nv.prt, 00.1				
ST33HTPH2X32AHD4, MICRO ARM SECURCORE SC300 290KBytes VQFN	STMICROELECTRONICS	Rejected	Validate...	Commer.
ST33HTPH2X32AHD8, MICRO ARM SECURCORE SC300 290KBytes VQFN	STMICROELECTRONICS	Alternate	Validate...	Commer.

4.5.2 TPM GPIOS

4.5.2.1 TPM GPIO_PP

GPIO_PP is used to indicate physical presence. It is internally pull down by the TPM. The Physical Presence (PP) pin should be connected if platform implementation (at boot level) uses a hardware physical presence function. As

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today it is not defined at the corporate level which strategy must be implemented at the boot level this signal is an input of the brick and be used either by external peripheral or reconnect to an AM64xx GPIO.

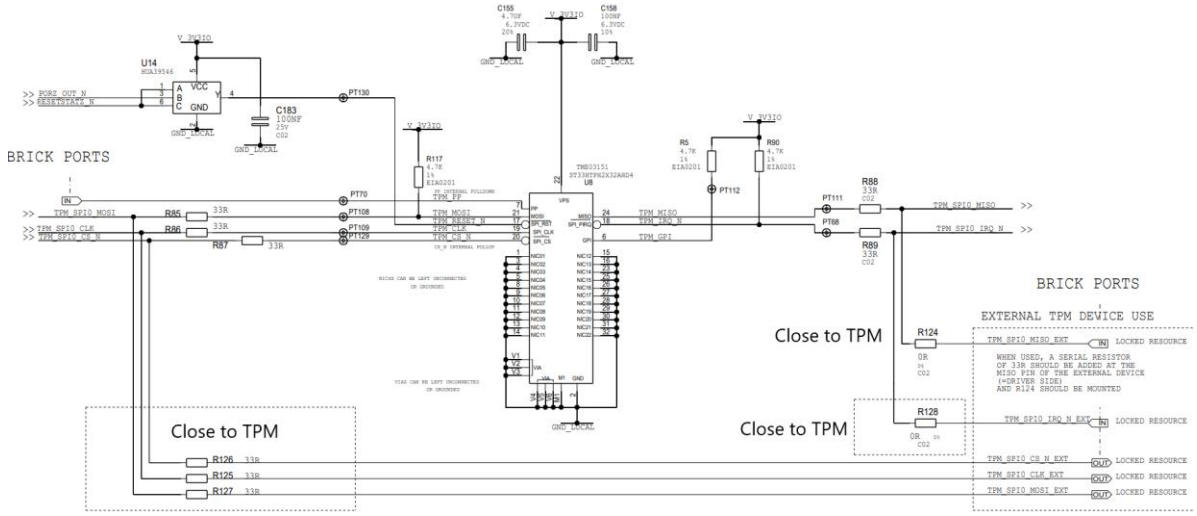
4.5.2.2 TPM GPI

GPI is used for activation and deactivation of the TPM Standby mode. It is externally pulled up through 4.7K to V_3V3IO. It is also internally pulled up by the TPM. The double pull-up resistor implementation is coming from lake of details in the datasheet the value of this pull-up resistor is not given. Considering EMC immunity and robustness we decided to implement this external pull up resistor.

4.5.3 TPM PCBA variant

We double implement the external access to the TPM by implementing or not resistors.

4.5.3.1 Schematic, TPM **with** external access



Schematic consideration:

In this configuration (TPM with external peripheral access) a modification on BOM is needed. The only consideration from user is the 33Ω online resistor to be added on SPI signals coming from the external peripheral.

This online resistor value must be adjusted during technical verification and measurement. Could be removed if the external peripheral drive is adapted to the line length only after verification and measurement.

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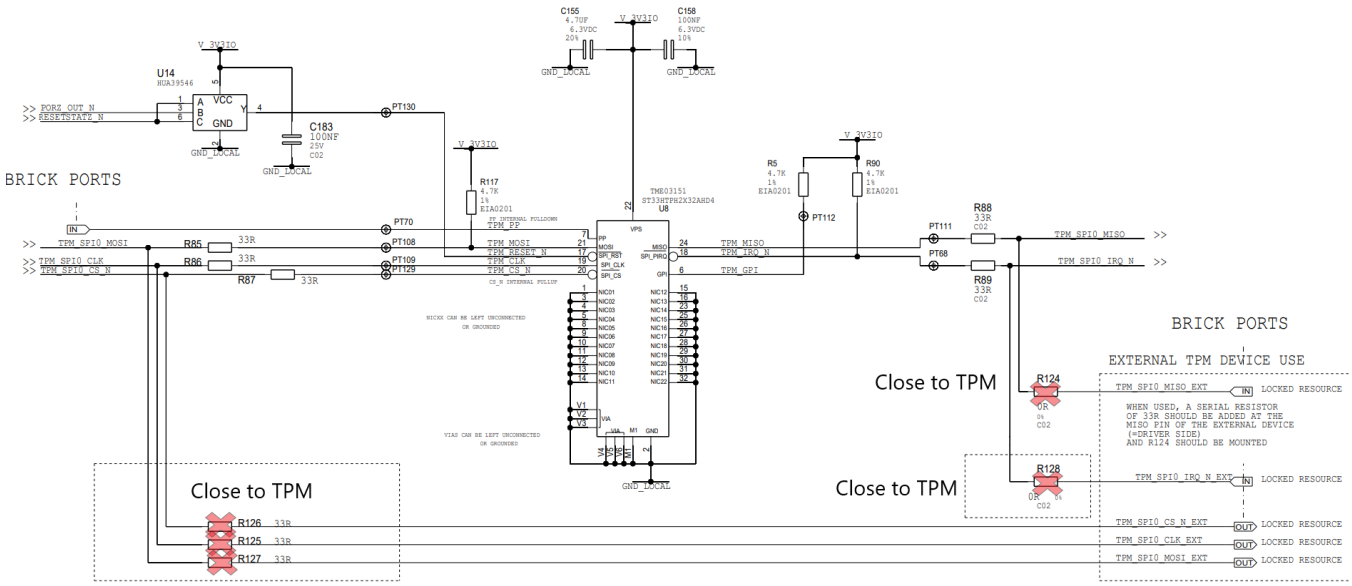
4.5.3.2 Schematic, TPM **without** external access



BOM Configuration:

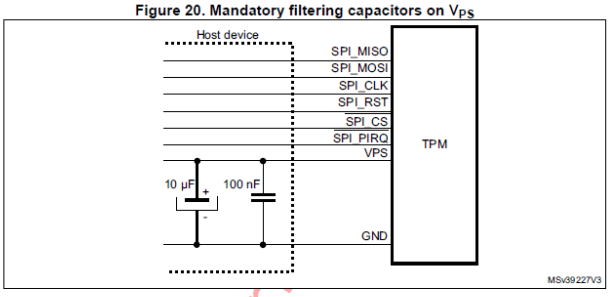
- R124 -> NOT POPULATED,
- R125 -> NOT POPULATED,
- R126 -> NOT POPULATED,
- R127 -> NOT POPULATED,
- R128 -> NOT POPULATED.

4.5.4 Decoupling

11.2 Power supply filtering

As mentioned in *Section 3: Pin and signal description on page 13*, the power supply of the circuit must be filtered using the circuit shown in *Figure 20*.

Figure 20. Mandatory filtering capacitors on V_{PS}



1. 10 µF and 100 nF are recommended values. The minimum required capacitor value is 2.1 µF (2 µF in parallel with 100 nF).

According to [REF9] : 4.7µF (TME10696) +100nF (HUA30500) chosen to respect decoupling > 2.1µF

Table 63. Maximum V_{PS} rising slope

Symbol	Parameter	Value	Unit
S_{VPS}	Maximum VPS rising slope	3.3	V/µs

VPS is powering by V_3V3IO, provided by load switch output TPS22965DSGR (TME02587)

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Output slew rate of TPS22965 is controlled by CT pin, which is left floating, meaning, that output rise time will be about: 136µs according to [REF10] :

Table 1. Rise Time vs CT Capacitor

CT (pF)	TYPICAL VALUES at 25°C with a 25 V X7R 10% CERAMIC CAPACITOR on CT(1)						
	VIN = 5 V	VIN = 3.3 V	VIN = 1.8 V	VIN = 1.5 V	VIN = 1.2 V	VIN = 1.05 V	VIN = 0.8 V
0	180	136	94	84	74	70	60
220	547	378	232	202	173	157	129
470	962	654	386	333	282	252	206
1000	1983	1330	765	647	533	476	382
2200	4013	2693	1537	1310	1077	959	766
4700	8207	5490	3137	2693	2200	1970	1590
10000	17700	11767	6697	5683	4657	4151	3350

(1) Rise time (µs) 10% - 90%, C_L = 0.1 µF, C_{IN} = 1 µF, R_L = 10 Ω, V_{BIAS} = 5 V

Slew rate will be (10%-90% of 3.3V) / 136µs = 0.8*3.3/136µs= 0.019V/µs.
So Max S_{VPS} is well respected 3.3V/µs >> 19mV/µs

4.5.5 Layout recommendations summary

TO BE COMPLETED basic info on timings

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4.6 Oscillator (crystal)

According to [REF2] here is crystal implementation

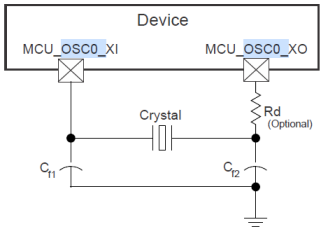

Figure 7-17. MCU_OSC0 Crystal Implementation

With electrical crystal specifications:

Table 7-17. MCU_OSC0 Crystal Circuit Requirements

PARAMETER				MIN	TYP	MAX	UNIT
F_{xtal}	Crystal Parallel Resonance Frequency				25		MHz
F_{xtal}	Crystal Frequency Stability and Tolerance		Ethernet RGMII and RMII not used			±100	ppm
			Ethernet RGMII and RMII using derived clock			±50	
$C_{L1+PCBXI}$	Capacitance of C_{L1} + C_{PCBXI}			12		24	pF
$C_{L2+PCBXO}$	Capacitance of C_{L2} + C_{PCBXO}			12		24	pF
C_L	Crystal Load Capacitance			6		12	pF
C_{shunt}	Crystal Circuit Shunt Capacitance	ESR_{xtal} = 30 Ω	25 MHz			7	pF
		ESR_{xtal} = 40 Ω	25 MHz			5	pF
		ESR_{xtal} = 50 Ω	25 MHz			5	pF
ESR_{xtal}	Crystal Effective Series Resistance					(1)	Ω

(1) The maximum ESR of the crystal is a function of the crystal frequency and shunt capacitance. See the C_{shunt} parameter.

Table 7-18. MCU_OSC0 Switching Characteristics - Crystal Mode

PARAMETER		MIN	TYP	MAX	UNIT
C_{XI}	XI Capacitance			1.44	pF
C_{XO}	XO Capacitance			1.52	pF
C_{XIXO}	XI to XO Mutual Capacitance			0.01	pF
t_s	Start-up Time		4		ms

PROPOSAL TME00175 :

	DSX221G	MDX22104	25,0-JXS22-10	Q24FA20
Temp Range	-40+105°C	-40+105°C	-40+105°C	-40+105°C
C_{load}	10pF	10pF	10pF	10pF
C_{shunt}	2pF max	4pF max	<5pF	2pF max
ESR	80Ω max	80Ωmax	30Ω to 60Ωmax	80Ωmax
Aging	?	±5ppm max	<±3ppm	±1ppm
Tolerance	±20ppm	±20ppm	±20ppm	±20ppm
Stability	±20ppm	±20ppm	±20ppm	±20ppm
Drive Strength	10µW recommended up to 200µW max	25µW recommended up to 100µW	10µW recommended up to 100µW	1µW min up to 100µW

4.6.1 C_{load}

According to [REF2] chap 7.10.4.1.1.1:

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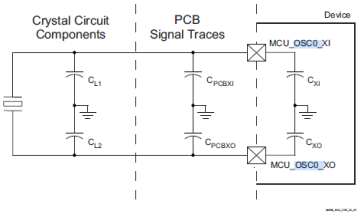
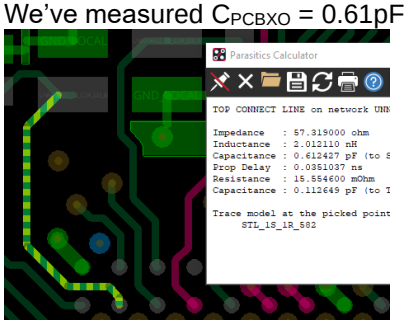


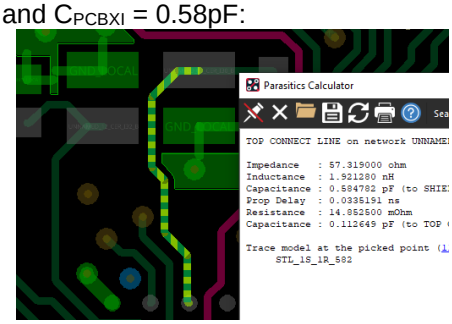
Figure 7-19. Load Capacitance

$$C_L = [(C_{L1} + C_{PCBXI} + C_{XI}) \times (C_{L2} + C_{PCBXO} + C_{XO})] / [(C_{L1} + C_{PCBXI} + C_{XI}) + (C_{L2} + C_{PCBXO} + C_{XO})]$$

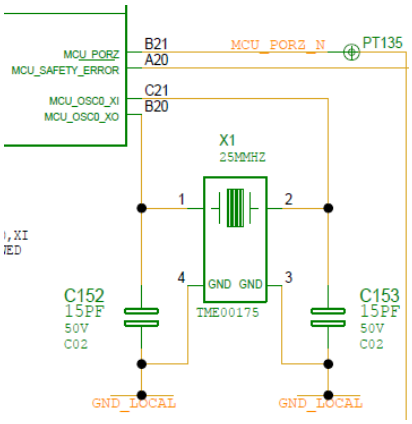
To determine the value of C_{L1} and C_{L2}, multiply the capacitive load value C_L by 2. Using this result, subtract the combined values of $C_{PCBXI} + C_{XI}$ to determine the value of C_{L1} and the combined values of $C_{PCBXO} + C_{XO}$ to determine the value of C_{L2}. For example, if C_L = 10 pF, C_{PCBXI} = 2.9 pF, C_{XI} = 0.5 pF, C_{PCBXO} = 3.7 pF, C_{XO} = 0.5 pF, the value of $C_{L1} = [(2C_L) - (C_{PCBXI} + C_{XI})] = [(2 \times 10\text{ pF}) - 2.9\text{ pF} - 0.5\text{ pF})] = 16.6$ pF and $C_{L2} = [(2C_L) - (C_{PCBXO} + C_{XO})] = [(2 \times 10\text{ pF}) - 3.7\text{ pF} - 0.5\text{ pF})] = 15.8$ pF

Assuming that C_{PCBXI} & $C_{PCBXBXO}$ & C_{L1} & C_{L2} are equivalent on layout that those calculated by T.I, so C_L=10pF of TME00175 and C_{L1}=C_{L2}=15pF fit the requirements.
We've measured C_{PCBXO} = 0.61pF and C_{PCBXI} = 0.58pF:





C_{XImax}= 1.44pF
C_{XOmax}=1.52pF
C_{L1}= 2*10pF-0.58pF-1.44pF= 17.98pF
C_{L2}= 2*10pF-0.61pF-1.52pF= 17.87pF



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4.6.2 C_{shunt}

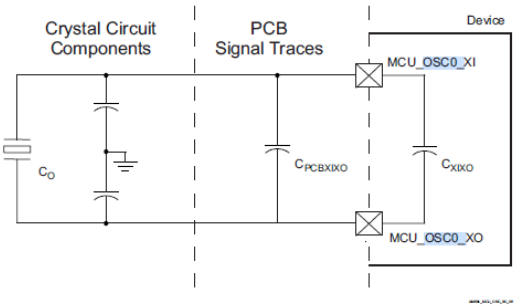
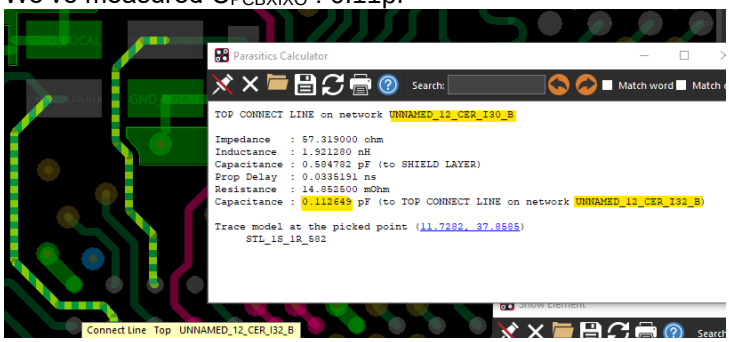


Figure 7-20. Shunt Capacitance

$C_{shunt} \geq C_O + C_{PCBXIXO} + C_{XIXO}$

For example, the equation would be satisfied when the crystal being used is 25 MHz with an ESR = 30 Ω, $C_{PCBXIXO}$ = 0.04 pF, C_{XIXO} = 0.01 pF, and shunt capacitance of the crystal is less than or equal to 6.95 pF.

ESR_{xtal} have maximum value of 40-80Ω (depending on the manufacturer), C_{shunt} will be in upper range of the above table 7-17 => 5pF.
$C_o \approx$ 4pF highest value of C_{shunt} provided by manufacturer.
We've measured $C_{PCBXIXO}$: 0.11pF



$C_{XIXOmax}$= 0.01pF
C_{shunt} = 5pF >= 4pF +0.11pF+ 0.01pF

C_o fills the requirement.
To minimize $C_{PCBXIXO}$ there is a tradeoff between minimize the EMC emission => minimize the area loop made by X_I / X_O tracks without increase $C_{PCBXIXO}$. If needed a GND track between both can help to reduce it.

4.6.3 Stability/Tolerance

Frequency stability of ±20ppm fit the above requirement of ±50ppm.
Frequency tolerance of ±20ppm fit the above requirement of ±50ppm.
Aging of ±5ppm fit also.
F_{XTAL} tolerance means that the ∑ tolerance+stability+aging must be <±50ppm: 20+20+~5 <±50ppm fit the requirement (assuming that we take in account aging only for 1st year).

For information purpose:
PCIe REFCLK requirement: ±300ppm ([REF18])
USB 3.1 Gen1 requirement: ±300ppm (Universal Serial Bus (USB) 3.1 Specification, revision 1.0)

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4.6.4 Drive Strength

Eval board are fitter with 100µW max drive strength (GP EVM), so TME00175 worst case have same max value of 100µW.

4.6.5 Startup time

Oscillator interface will be stable ≈ 4ms (typ) after VDD_CORE (VDDX_CORE 0.75V) & VDDS_OSC (V_1V8) rise:

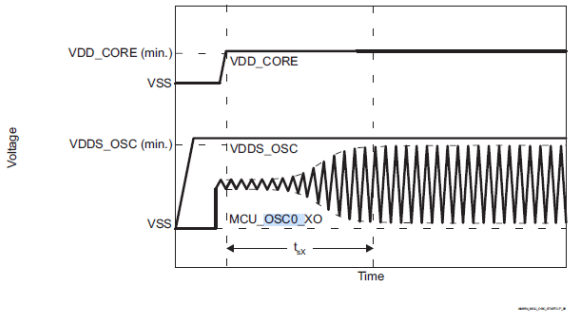

Figure 7-18. MCU_OSC0 Start-up Time

4.6.6 TI Evaluation boards

4.6.6.1 GP

On EVM GP crystal part number is **ABM10W-25.0000MHZ-8-K1Z-T3** with following features:

- Operating Temp: -55 to +125°C
- C_{load} = 8pF
- C_{shunt} = 1 to 2pF
- ESR: 35 to 50Ω max
- Aging 1 year ±2ppm
- Freq Tolerance ±10ppm
- Freq Stability ±50ppm
- Drive level 10 typ up to 100µW max

4.6.6.2 SK

On EVM SK crystal part number is **XRCGB25M000F3M00R0** with following features:

- Operating Temp: -30 to +85°C
- C_{load} = 6pF
- C_{shunt} =? pF
- ESR: 150Ω max
- Aging 1 year ±5ppm
- Freq Tolerance ±30ppm
- Freq Stability ±40ppm
- Drive level 300µW max

4.7 RTC

Will be managed outside the brick into AETHENA board BQT15769

4.8 Boot modes

BOOTMODE pins allow to select many different booting modes. Theses pins must be driven during reset mode. BOOTMODE [15.0] pins are split into 2 groups:

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- BOOTMODE [15..8] = GPIO0[30..23]
- BOOTMODE [7..0] = GPMC0_AD[7..0] (i.e. : address/data of Flash NAND)

The BOOTMODE [7..0] group is shared with NAND data.

4.8.1 Boot modes configuration

According to [REF1]:

Table 4-2. BOOTMODE Pin Mapping

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Reserved	Backup Boot Mode Config	Backup Boot Mode			Primary Boot Mode Config			Primary Boot Mode				PLL Config		

We selected a 25MHz crystal for the brick, then no change needed for bit B0, B1 and B2:

Table 4-3. PLL Reference Clock Selection

PLL Config Pins			Ref Clock (MHz)
B2	B1	B0	
0	0	0	19.2
0	0	1	20
0	1	0	24
0	1	1	25
1	0	0	26
1	0	1	27[(1)]
1	1	0	Reserved
1	1	1	Reserved

(1) USB DFU boot mode is not supported with the reference clock of 27 MHz.

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Other bits allow to select external primary device boot and backup device boot.

Primary Boot Mode Config							Primary Boot Mode
B9	B8	B7	B6	B5	B4	B3	
Reserved	Reserved	Reserved	0	0	0	0	Reserved
Reserved	Iclk	Csel	0	0	0	1	OSPI
Reserved	Iclk	Csel	0	0	1	0	QSPI
Reserved	Mode	Csel	0	0	1	1	SPI
Clkout	0	Link Info	0	1	0	0	Ethernet RGMII
Clkout	Clk src	0	0	1	0	1	Ethernet RMII
Bus reset	Reserved	Addr	0	1	1	0	I2C
Reserved	Reserved	Reserved	0	1	1	1	UART
Port	Reserved	Fs/raw	1	0	0	0	MMCSD Boot (SD Card Boot or eMMC Boot using UDA)
Reserved	Reserved	Reserved	1	0	0	1	eMMC Boot
Core Volt	Mode	Lane Swap	1	0	1	0	USB
Reserved	Reserved	Reserved	1	0	1	1	GPMC NAND
Reserved	Reserved	Reserved	1	1	0	0	GPMC NOR
Reserved	Reserved	Clocking	1	1	0	1	PCIe
SFPD	Read Cmd	Mode	1	1	1	0	xSPI
Reserved	Reserved	No/Dev	1	1	1	1	No-boot/Dev boot

Backup Boot Config	Backup Boot Mode Selection			Backup Boot Mode Selected
B13	B12	B11	B10	
Reserved	0	0	0	None
Mode	0	0	1	USB
Reserved	0	1	0	Reserved
Reserved	0	1	1	UART
IF	1	0	0	Ethernet
Port	1	0	1	MMCSD
Reserved	1	1	0	SPI
Reserved	1	1	1	I2C

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4.8.1.1 Supported Boot modes

Boot mode	Comments for the brick
OSPI	Supported inside the brick
QSPI	Supported inside the brick
SPI	QSPI/OSPI mounted devices support SPI boot inside the brick
RGMII	Supported outside the brick
RMII	Supported outside the brick with limitations
I2C	Supported outside the brick with limitations
UART	Supported outside the brick
SD Card (MMC1)	Supported outside the brick
eMMC (MMC0)	Supported outside the brick
USB	Supported outside the brick with limitations
GPMC NOR	Not supported
GPMC NAND	Supported but not implemented because Not advised by firmware as not “raw data” compatible during secure boot (signature verification), due to (bad) blocks management
PCIe	Supported outside the brick with limitations
No boot/ Dev boot mode	Supported inside the brick

N.B: According to chapter 3.1.5 , please check erratas for potential limitations

4.8.1.2 OSPI boot mode

Octal SPI Flash memories support various protocols, however the OSPI boot mode will only support specific OSPI BootLoader operation. As stated in the AM6442 the Flash memory need to be compliant with the JEDEC xSPI standards JESD251 and JESD216D.

- JESD251 is the Expanded Serial Peripheral Interface (xSPI) For Non-Volatile Memory Devices,
- JESD216D is Serial Flash Discoverable Parameters (SFDP).

4.4 Boot Modes

4.4.1 OSPI, xSPI, QSPI, SPI Boot

The following apply to all or multiple boot modes that are SPI related.

- Octal SPI flash memories support various protocols, however, the OSPI boot mode of the device will only support a specific protocol defined in OSPI Bootloader Operation. If the flash memory is complaint with JEDEC xSPI standards JESD251 and JESD216D, then xSPI boot mode is additionally supported. Refer to the xSPI boot mode description for further details.
- When using a OSPI\xSPI\QSPI\SPI flash device greater than 128Mb, a flash device package with a RESET signal must be used. The reason is that the ROM only uses 3-byte addressing mode (address is 24 bits). To address the full memory address range, software will typically switch to 4-byte addressing mode. If a reset to the processor occurs (for example, due to a warm reset), the ROM will execute expecting 3-byte addressing mode, but the flash will have been left in 4-byte addressing mode. For the flash device to return to 3-byte addressing mode, it must be reset using this signal. This typically can be achieved by using the RESET signal on the flash memory device. The ROM does not issue a software reset command.
- When booting from any of the SPI boot modes, BOOTMODE pin settings depend on operation during normal operation:
  - To support high-speed OSPI with the DQS signal during normal operation, set BOOTMODE8=1 to use internal iclk during boot and ensure signal LBCLKO is a no connect (that is, absolutely no trace can be connected to LBCLKO). The ROM boot operates OSPI at low speed (50 MHz), and during normal operation the OSPI interface can use the DQS signal to operate the interface at high speeds.
  - To support high-speed OSPI or QSPI without DQS signal (that is, using the LBCLKO signal to support loopback clock), then set BOOTMODE8=0 to use external clock during boot. In this case, ROM boot and normal operation use the externally looped back clock signal LBCLKO. Board designers should refer to the device specific data sheet to undertstand board routing guidelines for the LBCLKO signal.
  - To support only low-speed OSPI\xSPI\QSPI\SPI operation (that is, <=50-MHz OSPI clock), set BOOTMODE8=1 to use internal iclk, and ensure signal LBCLKO is a no connect (that is, absolutely no trace can be connected to LBCLKO). Operation for both ROM boot and normal operating mode clock the interface at low speed and use the internally pad looped back clock. The DQS and LBCLKO signals are not used during boot or normal operation

Extract from [REF1]

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To achieve the AM6442 requirements selected Flash device has the RESET dedicated pin. This RESET signal is the NOR_RESET_N which is driven by either the power-on reset or the warm reset of the AM6442 or the dedicated GPIO_OSPI_RESET_N.

Those signals prevent the execution of the 4 bytes addressing configuration of the Flash whereas 3 bytes addressing of the AM6442 due to a warm reset.
Selected Component for the OSPI application is the MT35XU512ABA which is fully compatible with the JESD standards recommended by TI.

Micron Confidential and Proprietary

Micron

512Mb, 1.8V Xccela™ Flash Memory
Features

Micron Xccela™ Flash Memory

1.8V, Octal I/O, 4KB, 32KB, 128KB, Sector Erase
MT35XU512ABA

Features

- SPI-compatible Xccela™ bus interface
  - Octal DDR protocol
  - Extended-SPI protocol with octal commands
- Xccela™ is JEDEC xSPI standard compliant
- Single and double transfer rate (SDR/DDR)
- Clock frequency
  - 166 MHz (MAX) in SDR (166 MB/s)
  - 200 MHz (MAX) in DDR (400 MB/s) with DQS
- Execute-in-place (XIP)
- PROGRAM/ERASE SUSPEND operations
- Volatile and nonvolatile configuration settings
- Software reset
- Reset pin available
- 3-byte and 4-byte address modes – enable memory access beyond 128Mb
- Dedicated 64-byte OTP area outside main memory
  - Readable and user-lockable
  - Permanent lock with PROGRAM OTP command
- Erase capability
  - Bulk erase
  - Sector erase 128KB uniform granularity
  - Subsector erase 4KB, 32KB granularity
- Security and write protection
  - Volatile and nonvolatile locking and software write protection for each 128KB sector
  - Nonvolatile configuration locking
  - Password protection
  - Protection management register offering enhanced security features
  - Hardware write protection: nonvolatile bits (BP[3:0] and TB) define protected area size
  - Program/erase protection during power-up
  - CRC detects accidental changes to raw data
- Electronic signature
  - JEDEC-standard 3-byte signature
  - Extended device ID: two additional bytes identify device factory options
- JESD47I-compliant
  - Minimum 100,000 ERASE cycles per sector
  - Data retention: 20 years (TYP)

Options	Marking
• Voltage	
– 1.7–2.0V	U
• Density	
– 512Mb	512
• Device stacking	
– Monolithic	A
• Device Generation	B
• Die revision	A
• Configuration	
– Boot in SDR x1	1
– Boot in DDR x8	2
• Sector Size	
– 128KB	G
• Packages – JEDEC-standard, RoHS-compliant	
– 24-ball T-PBGA 05/6mm x 8mm (5 x 5 array)	12
• Security features	
– Standard security	0
• Special options	
– Standard	S
– Automotive	A
• Operating temperature range	
– From –40°C to +85°C	IT
– From –40°C to +105°C	AT
– From –40°C to +125°C	UT

Extract from Micron Xccela Flash Memory datasheet MT35XU512ABA

4.8.1.2.1 OSPI boot ROM hardware configuration

Brick supports and implements both High speed OSPI WITH DQS signal and Low speed OSPI.

- High Speed OSPI boot ROM WITH DQS signal:
  - BOOTMODE [8] = 1, This parameter is set to use internal clock iclk. The ROM OSPI boot operates at 50Mhz. After boot operation, the interface will switch in normal operation using DQS signal to operate in high speed. LBCKO pin must be unconnected, no trace at all.
  - BOOTMODE [7] = 0, This parameter selects the OSPI_CSn0 signal as chip select.

- Low Speed OSPI boot ROM Configuration:

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- BOOTMODE [8] = 1, This parameter is set to use the internal clock iclk. The ROM OSPI boot and normal operating mode clock the interface at low speed and use the internally pad looped back clocks. The DQS and LBCLKO signals are not used during boot and normal operation.
- BOOTMODE [7] = 0, This parameter selects the OSPI_CSn0 signal as chip select.

4.8.1.2.2 OSPI boot PIN usage

OSPI pin usage table summarizes pin configuration for OSPI boot device.

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Tx En/Dis	Pinmux Sel
OSPI0_CLK	OSPI0_CLK	Disable	Up	0	Disable	Enable	0
OSPI0_LBCLKO	OSPI0_LBCLKO	Disable	Up	0	Enable	Enable	0
OSPI0_DQS	OSPI0_DQS	Disable	Up	0	Enable	Disable	0
OSPI0_D0	OSPI0_D0	Enable	Up	0	Enable	Enable	0
OSPI0_D1	OSPI0_D1	Enable	Up	0	Enable	Enable	0
OSPI0_D2	OSPI0_D2	Enable	Up	0	Enable	Enable	0
OSPI0_D3	OSPI0_D3	Enable	Up	0	Enable	Enable	0
OSPI0_D4	OSPI0_D4	Enable	Up	0	Enable	Enable	0
OSPI0_D5	OSPI0_D5	Enable	Up	0	Enable	Enable	0
OSPI0_D6	OSPI0_D6	Enable	Up	0	Enable	Enable	0
OSPI0_D7	OSPI0_D7	Enable	Up	0	Enable	Enable	0
OSPI0_CSn0	OSPI0_CSn0	Enable	Up	0	Disable	Enable	0
OSPI0_CSn1	OSPI0_CSn1	Enable	Up	0	Disable	Enable	0

Note

All signals in the table will be configured even though some may not be used by this particular boot mode.

Extract from [REF1]

Highlighted device pins are the implemented signals.

4.8.1.2.3 OSPI boot parameter

Boot parameter is composed of:

- Common Header boot parameter:
  - Length
  - Checksum
  - Peripheral
  - PLL Config
- Peripheral section:
  - All interface supported boot of the AM6442 are listed in this section.

The purpose is that Hardware configuration and Firmware configuration need to be exactly matched in order to ensure proper boot processing. Below tables regrouping the Common Header part and specific parameters to consider for proper boot application.

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Boot Parameter Table Common Header

Byte Offset	Size (bytes)	Name	Description
0	2	Length	The length of the table
2	2	Checksum	Ones complement checksum over length bytes in the table. If 0 the checksum is not validated.
4	2	Peripheral	Identifies the boot peripheral and format of the table after the common header. See Table 4-39
6	2	Reserved	Reserved
8	4	Timeout	Timeout for this boot mode, in milliseconds
12	4	Magic	Magic value 0x01AD0911
16	40	PLL Config 0	PLL Configuration 0. See Table 4-40
56	40	PLL Config 1	PLL Configuration 1
96	40	PLL Config 2	PLL Configuraiton 2
136	40	PLL Config 3	PLL Configuration 3
176	40	PLL Config 4	PLL Configuration 4
216	40	PLL Config 5	PLL Configuration 5

Extract from [REF1]

Boot Peripheral Selection

Peripheral Field Value	Description
0	Sleep (No boot)
10	Ethernet Reserved
20	Ethernet BOOTP/TFTP (general)
21	Ethernet RGMII specific
22	Ethernet RMII specific
30	PCIe
31	PCIe 1-lane
32	PCIe 2-lane
40	I2C
50	SPI
60	UART
70	USB DFU
71	USB Reserved
72	USB Host MSC
80	QSPI
85	OSPI
90	Reserved
100	MMCSD Card (general)
101	eMMC (general)
102	MMC 1-bit
103	MMC 4-bit
104	MMC 8-bit
110	GPMC NOR
120	Reserved
130	xSPI
140	GPMC NAND

Extract from [REF1]

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OSPI/QSPI/SPI Boot Parameter Table

Byte Offset	Size (bytes)	Name	Default Value	Description
256	1	Port	0	Physical port number
257	1	Mode on	From Pins	If non-zero, the mode byte will be sent
258	1	Instruct Width	From Pins	Number of pins used to send instructions (1, 2, 4, 8)
259	1	Address Width	From Pins	Number of pins used to send address (1, 2, 4, 8)
260	1	Data Width	From Pins	Number of pins used to received data (1, 2, 4, 8)
261	1	Address Size	24	24, and 32 bits are the valid address sizes
262	1	Mode	0	OSPI clock polarity and phase mode
263	1	CSEL	From Pins	Chip select number (0–3)
264	1	Read Cmd	From Pins	Command used to read read data
265	1	Mode byte	0	Value used for the mode byte (when active)
266	1	Dummy Cycles	From pins	Number of dummy cycles sent after the read command
267	1	clkRecovery	From pins	Clock recovery
268	1	dqsEnable	0	Enable DQS
269	1	Reserved	0	Reserved
270	2	Module Freq	0	The OSPI module frequency after PLL enable, in kHz. If 0, ROM code uses the value from the module clock tables.
272	4	Bus Frequency	From pins	The OSPI bus frequency, in kHz
276	4	Delay	0x08080808 or 0x01010101	The chip select read delays. Default value is based on the read command
280	4	Tap Delay	0xFFFFFFFF	The read tap selection. If 0xFFFFFFFF, the ROM code will scan the taps to find the best delay. The result will then overwrite the value in this table.
284	4	Internal Clk	From pins	0 = external (dqs) 1 = internal
288	4	notDAC	From pins	When 0, DAC mode is used
292	4	Read Index	0	Index to the active read address (0-1)
296	4	Read Addr 0	0x000000	The initial flash read address
300	4	Read Addr 1	0x400000 (0x4000 SPI)	Backup read address
304	4	Reserved	0	Reserved
308	4	Reserved	0	Reserved

Extract from [REF1]

OSPI boot mode is not eXecute In Place (XIP). ROM code first copies boot image into on-chip RAM and then executes it.

4.8.1.3 QSPI boot mode

Hardware recommendation, Standard compatibility and RESET signal constraint are the same as OSPI BOOT MODE. Refer to OSPI BOOTMODE chapter.

4.8.1.3.1 QSPI boot ROM hardware configuration

- High Speed QSPI boot ROM WITH DQS signal:
  - BOOTMODE [8] = 1, This parameter is set to use internal clock iclk. The ROM QSPI boot operates at 50Mhz. After boot operation, the interface will switch in normal operation using DQS signal to operate in high speed. LBCKO pin must be unconnected, no trace at all.
  - BOOTMODE [7] = 0, This parameter selects the OSPI_CSn0 signal as chip select.

- Low Speed QSPI boot ROM configuration:

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- BOOTMODE [8] = 1, This parameter is set to use the internal clock iclk. The ROM QSPI boot and normal operating mode clock the interface at low speed and use the internally pad looped back clocks. The DQS and LBCLKO signals are not used during boot and normal operation.
- BOOTMODE [7] = 0, This parameter selects the OSPI_CSn0 signal as chip select.

4.8.1.3.2 QSPI boot PIN usage

OSPI pin usage table summarizes pin configuration for QSPI boot device on port 0.

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Tx En/Dis	Pinmux Sel
OSPI0_CLK	OSPI0_CLK	Disable	Up	0	Disable	Enable	0
OSPI0_LBCLKO	OSPI0_LBCLKO	Disable	Up	0	Enable	Enable	0
OSPI0_DQS	OSPI0_DQS	Disable	Up	0	Enable	Disable	0
OSPI0_D0	OSPI0_D0	Enable	Up	0	Enable	Enable	0
OSPI0_D1	OSPI0_D1	Enable	Up	0	Enable	Enable	0
OSPI0_D2	OSPI0_D2	Enable	Up	0	Enable	Enable	0
OSPI0_D3	OSPI0_D3	Enable	Up	0	Enable	Enable	0
OSPI0_CSn0	OSPI0_CSn0	Enable	Up	0	Disable	Enable	0
OSPI0_CSn1	OSPI0_CSn1	Enable	Up	0	Disable	Enable	0
OSPI0_CSn2	OSPI0_CSn2	Enable	Up	0	Disable	Enable	0
OSPI0_CSn3	OSPI0_CSn3	Enable	Up	0	Disable	Enable	0

Note

All signals in the table will be configured even though some may not be used by this particular boot mode.

Extract from [REF1]

Highlighted device pins are the implemented signals.

4.8.1.3.3 QSPI boot parameter

Refer to OSPI Boot Parameter chapter 3.8.1.1.3 for detailed Common Herder boot, Peripheral and Parameter table.

QSPI boot mode is not eXecute in Place (XiP). ROM code first copies boot image into on-chip RAM and then executes it.

4.8.1.4 SPI boot mode

Hardware recommendation, Standard compatibility and RESET signal constraint are the same as OSPI BOOT MODE. Refer to OSPI BOOTMODE chapter.

4.8.1.4.1 SPI boot ROM Hardware configuration

- BOOTMODE[8]:
  - BOOTMODE[8] = 0 -> SPI Mode selected is Mode 0,
  - BOOTMODE[8] = 1 -> SPI Mode selected is Mode 3.

- BOOTMODE[7] = 0, Boot Flash is on Chip Select 0.

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4.8.1.4.2 SPI boot PIN usage

SPI pin usage table summarizes pin configuration for SPI boot device using OSPI module.

SPI Port 0 Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Tx En/Dis	Pinmux Sel
OSPI0_CLK	OSPI0_CLK	Disable	Up	0	Disable	Enable	0
OSPI0_LBCLKO	OSPI0_LBCLKO	Disable	Up	0	Enable	Enable	0
OSPI0_DQS	OSPI0_DQS	Disable	Up	0	Enable	Disable	0
OSPI0_D0	OSPI0_D0	Enable	Up	0	Enable	Enable	0
OSPI0_D1	OSPI0_D1	Enable	Up	0	Enable	Enable	0
OSPI0_CSn0	OSPI0_CSn0	Enable	Up	0	Disable	Enable	0
OSPI0_CSn1	OSPI0_CSn1	Enable	Up	0	Disable	Enable	0
OSPI0_CSn2	OSPI0_CSn2	Enable	Up	0	Disable	Enable	0
OSPI0_CSn3	OSPI0_CSn3	Enable	Up	0	Disable	Enable	0

Note

All signals in the table will be configured even though some may not be used by this particular boot mode.

Extract from [REF1]

Highlighted device pins are the implemented signals.

4.8.1.4.3 SPI boot parameter

Refer to OSPI Boot Parameter chapter 3.8.1.1.3 for detailed Common Herder boot, Peripheral and Parameter table.

SPI boot mode supports the 1S-1S-1S mode **ONLY** (Bit width = 1, Single Data Rate).

OSPI0_D0 will have data transfers FROM the AM6442 TO the Flash device.
OSPI0_D1 will have data transfers FROM the Flash device TO the AM6442.

The Command and Address issued are 8 bits and 24 bits respectively. The Read Command that is issued for SPI is 0x03. There are no dummy cycles issued after the read command. The frequency of operation supported is 6.250Mhz.

SPI boot mode is not eXecute In Place (XIP). ROM code first copies boot image into on-chip RAM and then executes it.

4.8.1.5 xSPI boot mode

The xSPI protocol defines 1S-1S-1S mode for general backwards compatibility, and 8D-8D-8D for maximum throughput (where bit-width (1 or 8) and data rate (Single Data Rate or Double Data Rate).

For 1S-1S-1S mode of operation (Bit-width =1, Single Data Rate). The Command and Address issued are 8 bits and 24 bits respectively. The Read Command that is issued is 0x0B.The frequency of operation supported is 50Mhz.

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For 8D-8D-8D mode of operation (Bit-width =8, Double Data Rate). The Command and Address issued are 8 bits and 32 bits respectively. The Read Command that is issued is 0x0B or 0xEE.The frequency of operation supported is 25 Mhz.

For SFDP mode ROM starts operation in 1S-1S-1S mode reads SFDP header from flash memory to get 8D-8D-8D switching sequence, Read Command, CMD Extension and Byte Order. SFDP parsing of ROM is described below and on successful parsing ROM will issue 8D-8D-8D command switching sequence and then will read the boot image in 8D-8D-8D mode with read command specified in SFDP header.

4.8.1.5.1 xSPI boot ROM hardware configuration

- BOOTMODE [9]:
  - BOOTMODE [9] = 0 SFDP disabled,
  - BOOTMODE [9] = 1 SFDP enabled,

- BOOTMODE [8]:
  - BOOTMODE [8] = 0 0x0B Read Command,
  - BOOTMODE [8] = 1 0xEE Read Command,

- BOOTMODE [7]:
  - BOOTMODE [7] = 0 1S-1S-1S mode @ 50Mhz,
  - BOOTMODE [7] = 1 8D-8D-8D mode @ 25Mhz,

4.8.1.5.2 xSPI boot Pin usage

xSPI Port 0 Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Tx En/Dis	Pinmux Sel
OSPI0_CLK	OSPI0_CLK	Disable	Up	0	Disable	Enable	0
OSPI0_LBCLKO	OSPI0_LBCLKO	Disable	Up	0	Enable	Enable	0
OSPI0_DQS	OSPI0_DQS	Disable	Up	0	Enable	Disable	0
OSPI0_D0	OSPI0_D0	Enable	Up	0	Enable	Enable	0
OSPI0_D1	OSPI0_D1	Enable	Up	0	Enable	Enable	0
OSPI0_D2	OSPI0_D2	Enable	Up	0	Enable	Enable	0
OSPI0_D3	OSPI0_D3	Enable	Up	0	Enable	Enable	0
OSPI0_D4	OSPI0_D4	Enable	Up	0	Enable	Enable	0
OSPI0_D5	OSPI0_D5	Enable	Up	0	Enable	Enable	0
OSPI0_D6	OSPI0_D6	Enable	Up	0	Enable	Enable	0
OSPI0_D7	OSPI0_D7	Enable	Up	0	Enable	Enable	0
OSPI0_CSn0	OSPI0_CSn0	Enable	Up	0	Disable	Enable	0
OSPI0_CSn1	OSPI0_CSn1	Enable	Up	0	Disable	Enable	0
OSPI0_CSn2	OSPI0_CSn2	Enable	Up	0	Disable	Enable	0
OSPI0_CSn3	OSPI0_CSn3	Enable	Up	0	Disable	Enable	0

Note

All signals in the table will be configured even though some may not be used by this particular boot mode.

Extract from [REF1]

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Highlighted device pins are the implemented signals.

4.8.1.5.3 xSPI boot parameter

xSPI Boot Parameter Table

Byte Offset	Size (bytes)	Name	Default Value	Description
256	1	Port	0	Physical port number
257	1	Mode on	From Pins	If non-zero, the mode byte will be sent
258	1	Instruct Width	From Pins	Number of pins used to send instructions (1, 8)
259	1	Address Width	From Pins	Number of pins used to send address (1, 8)
260	1	Data Width	From Pins	Number of pins used to received data (1, 8)
261	1	Address Size	24	24 and 32 bits are the valid address sizes
262	1	Mode	0	QSPI clock polarity and phase mode
263	1	CSEL	From Pins	Chip select number (0–3)
264	1	Read Cmd	From Pins	Command used to read read data
265	1	Mode byte	0	Value used for the mode byte (when active)
266	1	Dummy Cycles	From pins	Number of dummy cycles sent after the read command
267	1	clkRecovery	From pins	Clock recovery
268	1	dqsEnable	0	Enable DQS
269	1	ddrEnable	From pins	OSPI DDR mode operation
270	2	Module Freq	0	The QSPI module frequency after PLL enable, in kHz. If 0, ROM code uses the value from the module clock tables.
272	4	Bus Frequency	From pins	The QSPI bus frequency, in kHz
276	4	Delay	0x08080808 or 0x01010101	The chip select read delays. Default value is based on the read command
280	1	SFDP	From Pins	Enables SFDP parser for 1S-1S-1S to 8D-8D-8D switching
282	4	Tap Delay	0xFFFFFFFF	The read tap selection. If 0xFFFFFFFF, the ROM code will scan the taps to find the best delay. The result will then overwrite the value in this table.
286	4	Internal Clk	From pins	0 = external (dqs) 1 = internal
290	4	inDAC	From pins	When 0, XIP mode is used
294	4	Read Index	0	Index to the active read address
298	4	Read Addr 0	0x000000	The initial flash read address
302	4	Read Addr 1	0x400000	Backup read address

Extract from [REF1]

4.8.1.6 Ethernet RGMII boot mode

This boot mode is available for the brick and following the pin usage all signals are constraints in PCB layout according to it.
Furthermore, this boot mode is also available as backup boot mode.

4.8.1.6.1 RGMII boot ROM Hardware configuration

- BOOTMODE [9]:
  - BOOTMODE [9] = 0 25MHz not generated on CLKOUT0,

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- BOOTMODE [9] = 1 25MHz generated on CLKOUT0,

- BOOTMODE [8]:
  - BOOTMODE [8] = 0 Must be set to 0 for enable internal TX delay,
  - BOOTMODE [8] = 1 Reserved,

- BOOTMODE [7]:
  - BOOTMODE [7] = 0 MDIO PHY scan used for link parameter,
  - BOOTMODE [7] = 1 Link parameter programmed by software,

In case of backup bootmode, BOOTMODE [13] select RGMII or RMII interface :

Table 4-22. Ethernet Backup Boot Configuration Field

BOOTMODE Pins	Field	Value	Description
13	Interface	0	RGMII with internal Tx delay
		1	RMII with external clock source

4.8.1.6.2 RGMII boot pin usage

RGMII pin usage table summarizes pin configuration for RGMII boot device using external PHY.

Table 4-23. RGMII Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Tx En/Dis	Pinmux Sel
PRG1_PRU1_GPO0	RGMII2_RD0	Disable	Down	0	Enable	Disable	4
PRG1_PRU1_GPO1	RGMII2_RD1	Disable	Down	0	Enable	Disable	4
PRG1_PRU1_GPO2	RGMII2_RD2	Disable	Down	0	Enable	Disable	4
PRG1_PRU1_GPO3	RGMII2_RD3	Disable	Down	0	Enable	Disable	4
PRG1_PRU1_GPO4	RGMII2_RX_CTL	Disable	Down	0	Enable	Disable	4
PRG1_PRU1_GPO6	RGMII2_RXC	Disable	Down	0	Enable	Disable	4
PRG1_PRU1_GPO11	RGMII2_TD0	Disable	Down	0	Disable	Enable	4

Table 4-23. RGMII Pin Usage (continued)

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Tx En/Dis	Pinmux Sel
PRG1_PRU1_GPO12	RGMII2_TD1	Disable	Down	0	Disable	Disable	4
PRG1_PRU1_GPO13	RGMII2_TD2	Disable	Down	0	Disable	Disable	4
PRG1_PRU1_GPO14	RGMII2_TD3	Disable	Down	0	Disable	Disable	4
PRG1_PRU1_GPO15	RGMII2_TX_CTL	Disable	Down	0	Disable	Disable	4
PRG1_PRU1_GPO16	RGMII2_TXC	Disable	Down	0	Disable	Disable	4
PRG1_MDIO0_MDIO	MDIO0_MDIO	Enable	Up?	0	Enable	Enable	4
PRG1_MDIO0_MDC	MDIO0_MDC	Enable	Up?	0	Disable	Enable	4

Please check RGMII boot Pin usage chapter for GPIO assignments.

4.8.1.6.3 RGMII boot parameter

Refer to chap 4.4.5.1 Ethernet Bootloader Operation of [REF1]

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Note that booting from RGMII requires that an attached PHY be configured for RGMII-ID Mode immediately upon exiting reset: AM64 implement RGMII_ID on the TX channel, and external PHY must implement RGMII_ID on RX channel (not on TX channel because AM64 do it). The ROM will not make this configuration change to the PHY.

4.8.1.7 Ethernet RMII boot mode

This boot mode is available in term of ballout, but there are no specific design constraints for theses RMII signals (PRG1_PRU0_GPO10 for instance).
RGMII boot mode is preferred because design is constraint according to it.

4.8.1.7.1 RMII boot ROM hardware configuration

- BOOTMODE [9] = 0 50MHz not generated on CLKOUT0,
  - BOOTMODE [8]:
    - BOOTMODE [8] = 0 50MHz external source to RMII_REF_CLK and to external Ethernet PHY input clock (CLKOUT0 is unused),
    - BOOTMODE [8] = 1 Invalid configuration
- BOOTMODE [9] = 1 50MHz generated on CLKOUT0,
  - BOOTMODE [8]:
    - BOOTMODE [8] = 0 CLKOUT0 is configured to 50MHz and connect to both RMII_REF_CLK and to external Ethernet PHY input clock,
    - BOOTMODE [8] = 1 Invalid configuration,
- BOOTMODE [7]:
  - BOOTMODE [7] = 0 Must be set to 0,
  - BOOTMODE [7] = 1 Reserved,

4.8.1.7.2 RMII boot pin usage

RMII pin usage table summarizes pin configuration for RMII boot device using external PHY.

Table 4-24. RMII Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Tx En/Dis	Pinmux Sel
PRG1_PRU1_GPO4	RMII2_RX_ER	Disable	Down	0	Enable	Disable	5
PRG1_PRU0_GPO10	RMII_REF_CLK	Disable	Down	0	Enable	Disable	5
PRG1_PRU1_GPO0	RMII2_RXD0	Disable	Down	0	Enable	Disable	5
PRG1_PRU1_GPO1	RMII2_RXD1	Disable	Down	0	Enable	Disable	5
PRG1_PRU1_GPO11	RMII2_TXD0	Disable	Down	0	Disable	Enable	5
PRG1_PRU1_GPO12	RMII2_TXD1	Disable	Down	0	Disable	Enable	5
PRG1_PRU1_GPO15	RMII2_TX_EN	Disable	Down	0	Disable	Enable	5
PRG1_PRU1_GPO13	RMII2_CRS_DV	Disable	Down	0	Enable	Disable	5
PRG1_PRU0_GPO7[(1)]	CLKOUT0	Disable	Down	0	Disable	Enable	5
PRG1_MDIO0_MDIO	MDIO0_MDIO	Enable	Up	0	Enable	Enable	4
PRG1_MDIO0_MDC	MDIO0_MDC	Enable	Up	0	Disable	Enable	4

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4.8.1.7.3 RMII boot parameter

Refer to chap 4.4.5.1 Ethernet Bootloader Operation of [REF1].

4.8.1.8 I2C boot mode

Not fully implemented in the BRICK: I2C pullup must be managed outside the brick.

In the I2C boot mode, the ROM Code configures the Main Domain I2C0 in controller mode. The I2C controller drives the I2C target where the image is stored. The image is copied to the internal RAM and is executed from there. If the image is not recognized, the ROM will attempt to read the image at offset 0x8000. This is the only redundant image supported by the ROM.

ROM code will read 0x800 bytes before processing the data. The last block must be padded to the next 0x800 byte boundary, and it must be padded with zeros.

The boot code does not support byte address to bus address wrapping. So, the maximum image size that can be access is 64 kbytes. For example, if the read address is 0xFF00, the read size is 0x200 and the I2C bus address is 0x50, then 0x100 bytes will be read from 0xFF00 at bus address 0x50, followed by 0x100 bytes from 0x0000 at bus address 0x50. The bus address does not increment when the address rolls over.

4.8.1.8.1 I2C boot ROM hardware configuration

- BOOTMODE [9]:
  - BOOTMODE [9] = 0, Hung bus reset attempt after 1ms,
  - BOOTMODE [9] = 1, NO hung bus reset attempted.

- BOOTMODE [8]:
  - BOOTMODE [8] = 0, EEPROM's address is 0x50,
  - BOOTMODE [8] = 1, EEPROM's address is 0x51.

4.8.1.8.2 I2C boot pin usage

I2C Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Tx En/Dis	Pinmux Sel
I2C0_SCL	I2C0_SCL	Enable	Up	0	Enable	Enable	0
I2C0_SDA	I2C0_SDA	Enable	Up	0	Enable	Enable	0

Extract from [REF1]

4.8.1.8.3 I2C boot parameter

ROM Code will start reading I2C EEPROM at the specified I2C bus address. This read will be done beginning at the specified base address offset. Data will be read in 2KB chunks. The data will be stored at the address specified in the boot header. It will continue reading image data until a complete image has been read. When the complete image has been read, the ROM code will branch to the start address of the image.

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I2C Boot Parameter Table

Byte Offset	Size (bytes)	Name	Default Value	Description
256	1	Port	0	Physical port number
257	1	Mode	From Pins	0x4E = I2C Controller, 0x72 = I2C target
258	1	Dev Addr	From Pins	I2C address when target mode (0x10 or 0x11)
259	1	Reserved	0	Reserved
260	4	Mod Clock	0	I2C Module input clock. If 0, it is computed by ROM code.
264	2	Bus Freq	400	I2C Controller mode bus frequency, in kHz
266	2	Bus Addr	From Pins	I2C Controller mode storage device's address (0x50 or 0x51)
268	2	Read Index	0	Index to the active read offset (0 or 1)
270	2	Read Offset 0	0x0000	I2C Controller mode read offset
272	2	Read Offset 1	0x8000	I2C Controller mode backup read offset
274	2	Reserved	0	Reserved
276	2	Reserved	0	Reserved
280	2	Busy Timeout	From pins	Number of µs before a bus recovery is attempted. In units of microseconds in Q3 number format. Value of 0 disables bus recovery attempts.

Extract from [REF1]

4.8.1.9 UART boot mode

4.8.1.9.1 UART boot ROM hardware configuration

ROM Code always configure the UART0 port to 115200 KBauds, 8-n-1 mode, and the XMODEM protocol is used to transfer the boot data.

4.8.1.9.2 UART boot pin usage

UART Port 0 Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Tx En/Dis	Pinmux Sel
UART0_TXD	UART0_TXD	Enable	Up	0	Disable	Enable	0
UART0_RXD	UART0_RXD	Enable	Up	0	Enable	Disable	0

Extract from [REF1]

Highlighted device pins are the implemented signals.

4.8.1.9.3 UART boot parameter

Once the ROM Code configures the UART, it sends the UART pings for few seconds, which can be seen in the host. The pings consist of an ASCII capital C character. The UART boot mode supports only the CRC mode of XMODEM and does not support CHECKSUM mode. Both 128- and 1024-bytes block sizes are supported.

Before the ping from the device stops, HOST must load the boot image using the XMODEM protocol.

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UART Boot Parameter Table

Byte Offset	Size (bytes)	Name	Default Value	Description
256	1	Magic	0x49	Required Magic value
257	1	Protocol	63 (0x3F)	Specifies the transfer protocol = XMODEM
258	2	Reserved	0	Reserved
260	1	Max error Count	10	Error count resulting in boot abort
261	1	Ack timeout	3	Timeout in seconds on ack
262	1	Char timeout	20	Inter-character timeout in milliseconds
263	1	Reserved	0	Reserved
264	4	Port	From Pins	Physical port number
268	4	Mod Ref Clk	48000	Module reference clock, in kHz
272	4	Data Rate	115200	Baud rate (bps)
276	1	Parity	0	0=none, 1=odd, 2=even
277	1	Data bits	8	Only 8 data bit width is supported
278	1	Stop bits	2	Stop bits in Q7.1 format (2 = 1 stop bit)
279	1	Flow Control	0	0=none, 1= RTS/CTS
280	1	Over sample	16	Only 16× and 13× oversample are supported
281	1	Magic 2	0xB7	Required magic value

Extract from [REF1]

4.8.1.10 SD Card MMCSD1 boot mode

SD Card boot is only available on Port 1 of the MMCSD controller (MMCSD1). MMCSD1 is a locked resource of the BRICK. BOOT on SD Card is not implemented inside the BRICK, but as the interface could be available from outside, user can decide to implement it.
All SDCARD power management will be managed outside the brick into AETHENA board BQT15769., and special attention should be taken to insure that pins default value drive correctly the external load switch.

4.8.1.10.1 SD Card MMCSD1 boot ROM hardware configuration

The IOs on this port support both 1.8V and 3.3V operation, as well as dynamic voltage change. Thus, this port can support initial operation at 3.3V and remain at this voltage for legacy SD Cards, or support initial operation at 3.3V and change to 1.8V after ROM boot for UHS-I SD Cards. All those dynamic voltage changes are managed by the VDDSH5 output supply voltage of the BRICK. It is by firmware and a dedicated register which controlled the change between 1.8V and 3.3V.

Table 4-16. SD Card Boot Configuration Fields

SD Card Boot Configuration Fields			
BOOTMODE Pins	**Field**	**Value**	**Description**
9 (13[(1)])	Port	0	Reserved
		1	MMC Port 1 (4 bit width). This bit must be set to 1
7	FS/Raw	0	Filesystem mode
		1	Raw Mode

(1) When MMCSD is the backup mode.

Extract from [REF1]

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4.8.1.10.2 SD Card MMCSD1 boot pin usage

SD Card BOOT on Port 0 is not supported.

MMCSD1 pin configuration done by ROM code for SD Card boot device:

Table 4-17. SD Card (MMCSD1) Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Tx En/Dis	Pinmux Sel
MMC1_DAT3	MMC1_DAT3	Disable	NA	0	Enable	Enable	0
MMC1_DAT2	MMC1_DAT2	Disable	NA	0	Enable	Enable	0
MMC1_DAT1	MMC1_DAT1	Disable	NA	0	Enable	Enable	0
MMC1_DAT0	MMC1_DAT0	Disable	NA	0	Enable	Enable	0
MMC1_CLK	MMC1_CLK	Disable	NA	0	Disable	Enable	0
MMC1_CLKLB	MMC1_CLKLB	Disable	NA	0	Disable	Enable	0
MMC1_CMD	MMC1_CMD	Disable	NA	0	Enable	Enable	0
MMC1_SDCD	MMC1_SDCD	Disable	NA	0	Enable	Disable	0

Note

MMC1_CLKLB signal is not pinned out on the device. The pinmux configuration enables the input buffer of the internal loopback clock.

Note

MMC1_SDWP is not configured by ROM since the ROM never writes to the SD card.

Extract from [REF1]

Highlighted device pins are the implemented signals.

4.8.1.10.3 SD Card MMCSD1 boot parameter

The ROM will boot from SD Cards using one of these methods:

- User Data Area (UDA) in raw mode
- User Data Area (UDA) in filesystem mode

The ROM is capable of booting from any size SD Card because the MMCSD controller is responsible for addressing. Only single data rate with backward compatible interface timing is supported. The MMCSD module depends on proper voltage level on the SD Card detect signal (SDCD).

If SDCD=1, the ROM will assume the card is not present and will fail the boot mode.
The SDCD must be 0 for the ROM to continue to attempt to boot.
Card detects using DAT3 is not supported.

If the card is detected, the initial discovery phase is performed:

1. Send CMD 0. (GO IDLE, both for MMC and SD)
2. Send CMD 55. If the card responds, then the card type is assumed to be SD. On timeout the code sends CMD 1. If there is a response, then the card type is MMC.

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The ROM Code will start reading from the MMCSD memory boot sector, or filesystem, as specified by the BOOTMODE pins. Only FAT32 and FAT16 formats are supported in filesystem mode. It will continue reading data from the memory and storing it in internal RAM until a complete image has been read.

In RAW mode only, the ROM supports a redundant image at offset 0x400000 in case the initial image fails to be recognized. When the complete image has been read and found in good integrity, the ROM Code will branch to the address defined in the Boot Info field of the boot header.

When SD Card boot is used as a backup boot option, only User Data Area (UDA) in filesystem mode is supported. Raw mode is not supported. Additionally, boot will only occur in 1-bit mode during backup booting.

Table 4-49. MMCSD/eMMC Boot Parameter Table

Byte Offset	Size (bytes)	Name	Default Value	Description
256	1	Port	From Pins	Physical port number
257	1	eMMC	From Pins	0 = SD/MMC, else eMMC
258	1	bootAck	1 for eMMC 0 for SD/MMC	If 1 and in eMMC mode the controller expects a boot ack from the eMMC
259	1	Media	1 for eMMC 0 for SD/MMC	0 = auto detect card type 1 = MMC 2 = SD
260	1	busWidth	8 for eMMC From Pins for SD/MMC	Number of data pins (1, 4, or 8). If 0, max supported pins of the port are used.
261	1	bootAlt	1 for eMMC 0 for SD/MMC	If 1 and in eMMC mode, the controller uses the alt boot method (CMD1 with arg 0xFFFF_FFFA) to initiate data transfer
262	1	sigVolt	0x18 for port0 0x33 for port1	Sets the signal voltage for the controller. 0x18 = 1.8V 0x33 = 3.3V
263	1	Reserved	0	Reserved
264	4	Max Bus Freq	0	Max bus frequency in kHz. If 0, the value is determined by reading the CSD register from the card (still maxes out at 25 MHz)
268	4	refClkkHz	0	Module reference clock frequency, in kHz. If 0, the ROM code computes the value.
272	4	respTimeout	40000	The timeout period on initial card read, in milli-seconds, Q3 number format
276	128	Filename	"\tiboot3.bin"	For SD/MMC, boot filename in 16-bit Unicode characters (max 64)
404	4	Mode	0x1144D091	0x1144D091 = file system boot 0x1144C180 = raw image boot
408	4	CardIsInit	0	0 = card not yet initialized 1 = card has been initialized
412	4	Rsvd	0	Reserved
416	4	RawIndex	0	Current active read offset (0 or 1)
420	4	Rsvd	0	Reserved
424	4	Raw Offset 0	0x000000	Raw read offset
428	4	Raw Offset 1	0x400000	Backup raw read offset
432	4	Rsvd	0	Reserved
436	4	Rsvd	0	Reserved

Extract from [REF1]

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4.8.1.11 eMMC boot mode

Not applicable: BRICK does not implement eMMC memory but as the interface could be available from outside, user can decide to implement it.

4.8.1.11.1 eMMC boot ROM hardware configuration

Booting from an eMMC device is only available on Port 0 of the MMCSD controller (MMCSD0). Booting from an eMMC device is not available on Port1 (MMCSD1).

The IOs associated with MMCSD0 port only support 1.8V eMMC operation The ROM will boot from eMMC devices using one of these methods:

- User Data Area (UDA) in raw mode -> BOOTMODE [6…3] = 0b1000
- User Data Area (UDA) in filesystem mode -> BOOTMODE [6…3] = 0b1000
- eMMC boot mode (alternate) -> BOOTMODE [6…3] = 0b1001

Table 4-4. Primary Boot Mode Selection (continued)

Primary Boot Mode Config							Primary Boot Mode
B9	B8	B7	B6	B5	B4	B3	
Reserved	Iclk	Csel	0	0	1	0	QSPI
Reserved	Mode	Csel	0	0	1	1	SPI
Clkout	0	Link Info	0	1	0	0	Ethernet RGMII
Clkout	Clk src	0	0	1	0	1	Ethernet RMII
Bus reset	Reserved	Addr	0	1	1	0	I2C
Reserved	Reserved	Reserved	0	1	1	1	UART
Port	Reserved	Fs/raw	1	0	0	0	MMCSD Boot (SD Card Boot or eMMC Boot using UDA)
Reserved	Reserved	Reserved	1	0	0	1	eMMC Boot
Core Volt	Mode	Lane Swap	1	0	1	0	USB
Reserved	Reserved	Reserved	1	0	1	1	GPMC NAND
Reserved	Reserved	Reserved	1	1	0	0	GPMC NOR
Reserved	Reserved	Clocking	1	1	0	1	PCIe
SFPD	Read Cmd	Mode	1	1	1	0	xSPI
Reserved	Reserved	No/Dev	1	1	1	1	No-boot/Dev boot

Extract from [REF1]

4.8.1.11.2 eMMC boot pin usage

eMMC with MMCSD0 has no pin mux options, thus no pin mux configuration is necessary.

4.8.1.11.3 eMMC boot parameter

To boot from UDA in either raw or filesystem mode, choose bootmode "MMCSD Boot" (see Table 4-4). A special alternate boot mode is available with eMMC devices which allows the ROM to boot from an image that is in a separate boot partition in the eMMC. To boot from this mode, choose "eMMC Boot" (see Table 4-4).

The ROM Code will start reading from the memory boot sector, filesystem, or boot partition as specified by the BOOTMODE pins. Only FAT32 and FAT16 formats are supported in filesystem mode. It will continue reading data from the memory and storing it in internal RAM until a complete image has been read.

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In RAW mode only, the ROM supports a redundant image at offset 0x400000 in case the initial image fails to be recognized. When the complete image has been read and found in good integrity, the ROM Code will branch to the address defined in the Boot Info field of the boot header.

When eMMC boot is used as a backup boot option, only User Data Area (UDA) in filesystem mode is supported. Raw mode is not supported. Additionally, boot will only occur in 1-bit mode during backup booting. This means during backup booting only one IO will be used to transfer data boot.

Table 4-49. MMCSD/eMMC Boot Parameter Table

Byte Offset	Size (bytes)	Name	Default Value	Description
256	1	Port	From Pins	Physical port number
257	1	eMMC	From Pins	0 = SD/MMC, else eMMC
258	1	bootAck	1 for eMMC 0 for SD/MMC	If 1 and in eMMC mode the controller expects a boot ack from the eMMC
259	1	Media	1 for eMMC 0 for SD/MMC	0 = auto detect card type 1 = MMC 2 = SD
260	1	busWidth	8 for eMMC From Pins for SD/MMC	Number of data pins (1, 4, or 8). If 0, max supported pins of the port are used.
261	1	bootAlt	1 for eMMC 0 for SD/MMC	If 1 and in eMMC mode, the controller uses the alt boot method (CMD1 with arg 0xFFFF_FFFA) to initiate data transfer
262	1	sigVolt	0x18 for port0 0x33 for port1	Sets the signal voltage for the controller. 0x18 = 1.8V 0x33 = 3.3V
263	1	Reserved	0	Reserved
264	4	Max Bus Freq	0	Max bus frequency in kHz. If 0, the value is determined by reading the CSD register from the card (still maxes out at 25 MHz)
268	4	refClkkHz	0	Module reference clock frequency, in kHz. If 0, the ROM code computes the value.
272	4	respTimeout	40000	The timeout period on initial card read, in milli-seconds, Q3 number format
276	128	Filename	"\tiboot3.bin"	For SD/MMC, boot filename in 16-bit Unicode characters (max 64)
404	4	Mode	0x1144D091	0x1144D091 = file system boot 0x1144C180 = raw image boot
408	4	CardIsInit	0	0 = card not yet initialized 1 = card has been initialized
412	4	Rsvd	0	Reserved
416	4	RawIndex	0	Current active read offset (0 or 1)
420	4	Rsvd	0	Reserved
424	4	Raw Offset 0	0x000000	Raw read offset
428	4	Raw Offset 1	0x400000	Backup raw read offset
432	4	Rsvd	0	Reserved
436	4	Rsvd	0	Reserved

Extract from [REF1]

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4.8.1.12 USB boot mode

4.8.1.12.1 USB boot ROM hardware configuration

USB BOOT supports two different configurations:

- Host (MSC Boot)
- DFU (USB device firmware upgrade)

Below the configuration needed on associated BOOTMODE pins

Table 4-25. USB Boot Configuration Fields

USB Configuration Fields for Primary Boot Mode			
BOOTMODE Pins	**Field**	**Value**	**Description**
9	CoreVoltage	0	0.85V core voltage
		1	0.75V core voltage
8 (13[(1)])	Mode	0	DFU (USB device firmware upgrade)
		1	Host (MSC boot)
7	Lane Swap	0	D+/D- lines are not swapped
		1	D+/D- lines are swapped

(1) When USB is the backup mode.

Extract from [REF1]

BOOTMODE [9] = 1 because the core voltage value corresponds to the core voltage of the AM6442.
USB backup is not supported because VDDx_CORE =0.75V into the brick (0.85V needed).

4.8.1.12.2 USB boot Pin usage

USB Port 0 is used for USB Boot.

Table 4-26. USB Port 0 Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Tx En/Dis	Pinmux Sel
USB0_DRVVBUS	USB0_DRVVBUS	Enable	Down	0	Disable	Enable	0

Note

Note that other USB pins do not have pin mux options. USB_DRVVBUS is configured in DFU mode even though it is not used.

Note on USB backup boot

- The USB backup boot option allows only 0.85 V core voltage
- Lane Swap (D+/D- lines) are not allowed

Configurability (pins) of these options do not exist in the USB backup boot mode.

Extract from [REF1]

4.8.1.12.3 USB boot MSC parameter

The USB boot mode is used to read the boot image from an external USB Host.
USB boot common header must precede the USB boot parameter.

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Table 4-53. USB MSC Boot Parameter Table

Byte Offset	Size (bytes)	Name	Default Value	Description
256	4	Port	From pins	Physical port number. Always set to 0.
260	4	Base address 0	From pins (port)	Base address of USB subsystem (CMN)
264	4	Base address 1	From pins (port)	Base address of controller
268	4	phyBaseAddress	From pins (port)	Base address of USB PHY module
272	4	modRefClkkHz	varies	Module reference clock, in kHz
276	2	Vendor ID	0x0451	USB vendor ID. Read from control registers.
278	2	Product ID	0x6164	USB product ID. Read from control registers.
280	2	BCD Device	0	Binary Coded Decimal device release number
284	4	String Table addr	0x4182BCA8	Pointer to the string table in RAM
288	2	Vendor String offset	0	Offset to vendor string in string table
290	2	Prod string offset	0	Offset to product string in string table
292	2	Serial num string offset	0	Offset to serial number string in string table
294	2	Timeout	5000	USB timeout in milliseconds
296	2	Mode	1	1 = DFU ≠1 = MSC Mode 1 = backup DFU, 2 = backup MSC
298	1	Lane reverse	From pins	Set to non-zero for lane reverse
299	1	CoreVoltage	From pins	USB Core Voltage 0 = 0.85V, 1 = 0.75V
300	64	FileName	tiboot3.bin	Boot file name

Extract from [REF1]

4.8.1.12.4 USB boot DFU parameter

In DFU mode, the ROM will attempt an enumeration for 60 seconds, after which the boot mode will fail. If a successful enumeration is achieved, the ROM Code will start reading from the external host as specified by the BOOTMODE pins.

It will continue reading data from the memory and storing it in internal RAM until a complete image has been read. When the complete image has been read and found in good integrity, the ROM Code will branch to the address defined in the Boot Info field of the boot header.

DFU Device:

- Vendor ID = 0x451,
- Product ID = 0x6165,
- Device ID = 0.

USB DFU boot must be preceded with the common boot parameters.

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Table 4-52. USB DFU Boot Parameter Table

Byte Offset	Size (bytes)	Name	Default Value	Description
256	4	Port	From pins	Physical port number. Always set to 0.
260	4	Base address 0	From pins (port)	Base address of USB subsystem (CMN)
264	4	Base address 1	From pins (port)	Base address of controller
268	4	phyBaseAddress	From pins (port)	Base address of USB PHY module
272	4	modRefClkkHz	varies	Module reference clock, in kHz
276	2	Vendor ID	0x0451	USB vendor ID. Read from control registers.
278	2	Product ID	0x6165	USB product ID. Read from control registers.
280	2	BCD Device	0x200	Binary Coded Decimal device release number
284	4	String Table addr	0x4182A76C	Pointer to the string table in RAM
288	2	Vendor String offset	0	Offset to vendor string in string table
290	2	Prod string offset	32	Offset to product string in string table
292	2	Serial num string offset	64	Offset to serial number string in string table
294	2	Timeout	5000	USB timeout in milliseconds
296	2	Mode	1	1 = DFU ≠1 = MSC Mode 1 = backup DFU, 2 = backup MSC
298	1	Lane reverse	From pins	Set to non-zero for lane reverse
299	1	CoreVoltage	From pins	USB Core Voltage 0 = 0.85V, 1 = 0.75V
300	4	Block Size	4096	DFU Block Size

Extract from [REF1]

4.8.1.12.5 USB boot DFU limitations

In USB DFU and PCIe boot modes, the boot image is processed in image mode, meaning that the image is entirely loaded in internal RAM at address 0x70001000 before the certificate is validated.

This introduces two limitations compared to the other boot modes:

1. Once the image is validated, it needs to be relocated by the DMSC to its final location to be ready for execution. Since the source and destination for the copy are both in internal RAM, the user needs to ensure the reloaction address is either in a lower address (0x70000000-0x71000000) or in a higher address beyond the end of the image (0x71000000 + size of image). If this is not followed, the image relocation will corrupt itself while copying, resulting in a boot failure. The relocation address is defined in the certificate.

2. Because the downloaded image is at offset 0x70001000 it also means that both DFU and PCIe maximum image size are 4Kbytes less than with the other boot mode.

There is FW limitation in term of image size and mapping, please check chap 4.4.6.2 of [REF1].

4.8.1.13 GPMC NAND boot mode

This function is not implemented in the BRICK but as BRICK embeds NAND Flash user can implement it.

Still in investigation on the BRICK, the NAND Flash selected under PDM TME01645 is composed of two references:

1. MICRON which is fully compatible with AM6442 NAND Boot requirements,

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2. SKYHIGH which is dual die component with different architecture and page size.

AM6442 ROM only supports boot from ONFI 1.0 compatible 8-bit parallel NAND memory up to 2Gbytes in size connected to GPMC CS0 with the following geometries:

- 2Kbyte page and spare area of at least 64 bytes or
- 4Kbyte page size and spare area of at least 128 bytes.

4.8.1.13.1 GPMC NAND boot ROM hardware configuration

In order to boot with GPMC interface on NAND BOOTMODE [6…3] = 0b1011.

Table 4-4. Primary Boot Mode Selection (continued)

Primary Boot Mode Config							Primary Boot Mode
B9	B8	B7	B6	B5	B4	B3	
Reserved	Iclk	Csel	0	0	1	0	QSPI
Reserved	Mode	Csel	0	0	1	1	SPI
Clkout	0	Link Info	0	1	0	0	Ethernet RGMII
Clkout	Clk src	0	0	1	0	1	Ethernet RMII
Bus reset	Reserved	Addr	0	1	1	0	I2C
Reserved	Reserved	Reserved	0	1	1	1	UART
Port	Reserved	Fs/raw	1	0	0	0	MMCSD Boot (SD Card Boot or eMMC Boot using UDA)
Reserved	Reserved	Reserved	1	0	0	1	eMMC Boot
Core Volt	Mode	Lane Swap	1	0	1	0	USB
Reserved	Reserved	Reserved	1	0	1	1	GPMC NAND
Reserved	Reserved	Reserved	1	1	0	0	GPMC NOR
Reserved	Reserved	Clocking	1	1	0	1	PCIe
SFPD	Read Cmd	Mode	1	1	1	0	xSPI
Reserved	Reserved	No/Dev	1	1	1	1	No-boot/Dev boot

Extract from [REF1]

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4.8.1.13.2 GPMC NAND boot pin usage

GPMC NAND Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Tx En/Dis	Pinmux Sel
GPMC0_AD0	GPMC0_AD0	Disable	Down	0	Enable	Enable	0
GPMC0_AD1	GPMC0_AD1	Disable	Down	0	Enable	Enable	0
GPMC0_AD2	GPMC0_AD2	Disable	Down	0	Enable	Enable	0
GPMC0_AD3	GPMC0_AD3	Disable	Down	0	Enable	Enable	0
GPMC0_AD4	GPMC0_AD4	Disable	Down	0	Enable	Enable	0
GPMC0_AD5	GPMC0_AD5	Disable	Down	0	Enable	Enable	0
GPMC0_AD6	GPMC0_AD6	Disable	Down	0	Enable	Enable	0
GPMC0_AD7	GPMC0_AD7	Disable	Down	0	Enable	Enable	0
GPMC0_ADVn_ALE	GPMC0_ADVn_ALE	Disable	Up	0	Disable	Enable	0
GPMC0_OEn_Ren	GPMC0_OEn_Ren	Disable	Up	0	Disable	Enable	0
GPMC0_Wen	GPMC0_Wen	Disable	Up	0	Disable	Enable	0
GPMC0_BEOn_CLE	GPMC0_BEOn_CLE	Disable	Up	0	Disable	Enable	0
GPMC_WAIT0	GPMC_WAIT0	Enable	Up	0	Enable	Disable	0
GPMC0_WPn	GPMC0_WPn	Disable	Down	0	Disable	Enable	0
GPMC0_CSn0	GPMC0_CSn0	Enable	Up	0	Disable	Enable	0

Extract from [REF1]

4.8.1.13.3 GPMC NAND boot parameter

GPMC NAND boot must be preceded with the common header boot parameters.

Table 4-55. GPMC NAND Boot Parameter Table

Byte Offset	Size (bytes)	Name	Default Value	Description
256	4	Ref Clk kHz	From pins	Specifies the module ref clock.
260	4	Page Size	0	Page size in bytes 2048 or 4096
264	1	Chip Select	0	Chip Select
265	1	Ad Mux	0	Address/data multiplexing
266	1	Data Bus Width	8	Data bus width. Valid values are 8 and 16
267	1	AD rows	0	Number of Row address
268	1	AD columns	0	Number of Column address cycles
269	1	ECC Nibbles	0	Size of BCH remainder in nibbles. 0 if no ECC, 26 for BCH8
270	2	Current Valid Block	0xFFFF	Block number of last known good block
272	2	Pages per Block	0	Number of pages in a block
274	2	Reserved	0	Reserved
276	4	Current Read Index	0	Active read index
280	4	Read Offset[0]	0	Offsets from base of GPMC NAND memory
284	4	Read Offset[1]	0x400000	Offsets from base of GPMC NAND memory

Extract from [REF1]

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4.8.1.13.4 GPMC NOR boot mode

Not applicable, BRICK only implements GPMC interface with NAND Memory.

4.8.1.14 PCIe boot mode

PCIe boot mode is available for the brick, AM64 act as device (at Gen2 only) which expose 6 BARs, one of which of 2MByte is accessed by an external root complex to copy the boot image.

There are specifics recommendations outside the brick in term of reset (POR_RESET_IN_N management) and PCIe powering.

Also, it is obvious that the USB 3.1 interface must not be used because SERDES are used for PCIe purpose.

4.8.1.14.1 PCIe boot ROM hardware configuration

- BOOTMODE [7]:
  - BOOTMODE [7] = 0 PHY clock from external pins,
  - BOOTMODE [7] = 1 PHY clock from internal source,

According to E2E forum REFCLK_bootmode.pdf, PCIe bootmode always act as endpoint, so REFCLK is provided by external rootcomplex. The BOOTMODE [7] bit allows to select is REFCLK is common clock architecture or separate clocking architecture.

4.8.1.14.2 PCIe boot Pin usage

Table 4-28. PCIe Pin Usage

Device Pin	Module Signal	Pull Enable	Pull Direction	Driver Index	Rx En/Dis	Tx En/Dis	Pinmux Sel
UART1_CTSn	PCIE0_CLKREQn	Enable	Down	0	Enable	Enable	3

PCIE0_CLKREQn is available outside the but, is not recommended to be used, because this I/O is no able to be support an external voltage of 3.3V on this pin, when AM64 is powered off. Just pull up this PCIe signal, as it is managed outside the brick into AETHENA board BQT15769.

4.8.1.14.3 PCIe boot parameter

According to chap 4.4.7.1 PCIe bootloader operation of [REF1] all parameters are fixed, and loading process is described also.

4.8.1.14.4 PCIe boot limitations

There is FW limitation in term of image size and mapping, please check chap 4.4.7.2 of [REF1].

4.8.1.15 No-boot/Dev boot mode

4.8.1.15.1 No-boot/Development boot Hardware configuration

- BOOTMODE [7]:
  - BOOTMODE [7] = 0 Development Boot,
  - BOOTMODE [7] = 1 No Boot

Theses specifics boot modes may be interesting when bypassing DMSC ROM boot or MCU R5 ROM is needed. For further information please check chap 4.4.11 of [REF1].

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4.8.2 Boot mode tristate buffers

4.8.2.1 Layout recommendations

All reserved BOOTMODE pin must be tied high or low via pull resistors (not left floating because no internal PU or PD).

Concerning BOOTMODE [7..0], if NAND is used in 1 clock divide mode, internal GPMC_FCLK could be up to 133MHz, so BOOTMODE[7..0] could toggle up to this clock rate; this implies to have buffer as close as possible to GPMC0_AD bus to minimize stub effect, and to support NAND access cycle up to 133MHz.

According to datasheet [REF2]:

7.10.5.8.3 GPMC and NAND Flash — Asynchronous Mode

Table 7-56 and Table 7-57 present timing requirements and switching characteristics for GPMC and NAND Flash — Asynchronous Mode.

Table 7-56. GPMC and NAND Flash Timing Requirements – Asynchronous Mode

see Figure 7-52

NO.	PARAMETER	DESCRIPTION	MODE[4]	MIN MAX 133 MHz	UNIT
GNF12[1]	$t_{acc(d)}$	Access time, input data GPMC_AD[15:0][3]	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J[2]	ns

(1) The GNF12 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of the read cycle and after GNF12 functional clock cycles, input data is internally sampled by the active functional clock edge. The GNF12 value must be stored inside AccessTime register bit field.

(2) J = AccessTime × (TimeParaGranularity + 1) × GPMC_FCLK[3]

Concerning BOOTMODE [15..8] this will be manage outside the brick with tristate buffers into AETHENA board BQT15769 by minimizing stub on theses lines.

4.8.2.2 Timing constraints

According to datasheet [REF2]:

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Table 7-12. BOOTMODE Timing Requirements

see Figure 7-12

NO.	PARAMETER		MIN	MAX	UNIT
RST23	$t_{su(BOOTMODE-PORz_OUT)}$	Setup time, BOOTMODE[15:00] before PORz_OUT high (External MCU PORz event or Software SW_MAIN_PORz)	3*S(1)		ns
RST24	$t_{h(PORz_OUT - BOOTMODE)}$	Hold time, BOOTMODE[15:00] after PORz_OUT high (External MCU PORz event, Software SW_MAIN_PORz)	0		ns

(1) S = MCU_OSC0_XI/XO clock period

Table 7-13. PORz_OUT Switching Characteristics

see Figure 7-12

NO.	PARAMETER		MIN	MAX	UNIT
RST25	$t_{d(MCU_PORzL-PORz_OUT)}$	Delay time, MCU_PORz active (low) to PORz_OUT active (low)	0		ns
RST26	$t_{d(MCU_PORzH-PORz_OUT)}$	Delay time, MCU_PORz inactive (high) to PORz_OUT inactive (high)	0		ns
RST27	$t_{w(PORz_OUTL)}$	Pulse Width Minimum PORz_OUT low (MCU_PORz, SW_MAIN_PORz)	1200		ns

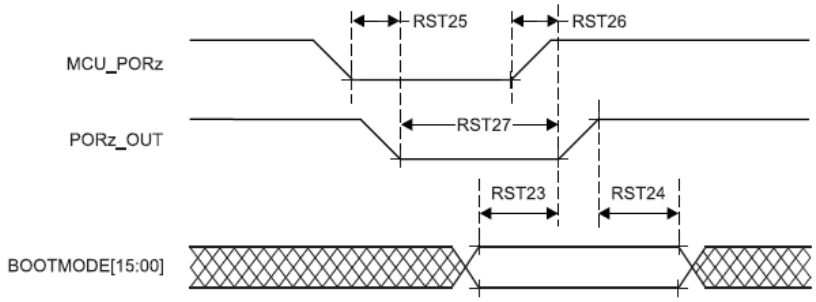

Figure 7-12. BOOTMODE Timing Requirements and PORz_OUT Switching Characteristics

It means that BOOTMODE pin must be driven by PORz_OUT signal (active low).
In our case MCU_OSC0 =25MHz, RST23 min = 3*S= 120nS
RST27 is x10 RST23, so there is no setup time issue on RST23.

4.8.2.3 TI EVM

TI EVM SK revB (and GP EVM) use a SN74AVC8T245RHL in order to isolate BOOTMODE setting in bootmode vs running mode.
Furthermore, they add 1.1K series resistor in order to more minimize buffer load effect.
Input capacitor on B side is about 7pf (according to datasheet SCES517J_n74avc8t245.pdf):

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	T_A = 25°C			−40°C to +85°C		−40°C to +125°C		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
C_{io}	A or B port	V_O = 3.3 V or GND	3.3 V	3.3 V		6			7			pF

4.8.2.4 BRICK

Into the brick buffer TME08242 74LVC244ABQ,115 (DHVQFN20 4.6mmx2.6mm pitch 0.5mm) is used, only 1 direction with only 1 power supply.
BOOTMODE pin (GPMC) are related to VDDSHV3 power supply (1.8V).

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Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; V_O = 5.5 V or GND; V_{CC} = 3.6 V [2]	-	±0.1	±5	-	±20	µA

Parasitic C_{OUT} is not specified, only leakage current is specified with a very low value which shouldn't interfere after boot mode sequence.

SOT8020-1 (DHXQFN20) package could reduce size to 3.2mx2.0mm pitch 0.4mm.

4.9 AM64 ADC

AM64 provide an ADC (8 inputs multiplexed, 12 bits, up to 4MSPS), which are outputted off the brick, to monitor external phenomena.

According to [REF2] all unused ADC must be tied to VSS :

(3) Any unused ADC0_AIN inputs must be pulled to VSS through a resistor or connected directly to VSS when VDDA_ADC is connected to a power source.

4.9.1 AM64 ADC electrical characteristics:

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ADC_AIN[7:0]}$	Full-scale Input Range		VSS		VDDA_ADC0	V
$R_{ADC_AIN[0:7]}$	Input Impedance of ADC0_AIN[7:0]	f = input frequency		[1/((65.97 × 10^{-12}) × f)]		Ω
I_{IN}	Input Leakage	ADC0_AIN[7:0] = VSS			4	µA
		ADC0_AIN[7:0] = VDDA_ADC0			10	µA
C_{IN}	Input Sampling Capacitance			5.5		pF

VDDA_ADC0 is about 1.8V filtered by ferrite bead CO031068 (120Ω@100MHz 1.3A) + 4.7µF//100nF.

Negative (ADC0_REFN) and Positive (ADC0_REFP) reference voltages are connected respectively to VSS and VDDA_ADC. According [REF2] :

(4) The ADC0_REFP and ADC0_REFN reference inputs are analog inputs which must be treated like high transient power supply rails, where ADC0_REFN is expected to be connected directly to the PCB ground plane along with all other VSS pins, and ADC0_REFP is connected to a power source capable of providing at least 4mA of current. ADC0_REFP may be connected to the same power source as VDDA_ADC0 if the voltage tolerance of the supply provides an acceptable accuracy for the ADC reference. A high frequency decoupling capacitor must be connected directly between ADC0_REFP and ADC0_REFN. The high frequency decoupling capacitor should be placed in the ball array on the back side of the PCB and connected directly to the ADC0_REFP and ADC0_REFN pins with vias. ADC0_REFP may be connected to VSS if ADC0 is not used and VDDA_ADC0 has been connected to VSS. The high frequency decoupling capacitor described above will not be required if ADC0 is not used and ADC0_REFP is connected to VSS. See the *Pin Connectivity Requirements* section for more information on ADC0 connectivity.

ADC0_REFP pin filtering directly on pin with high frequency capacitor TME00673 (10nF).

Estimated ADC input resistor on frequency range (from AM64 datasheet):

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F (Hz)	R adc_in (Mohm)
50	303,168
100	151,584
500	30,317
1000	15,158
5000	3,032
10000	1,516
20000	0,758
50000	0,303
100000	0,152
500000	0,030
1000000	0,015
5000000	0,003

All overvoltage/ESD protection will be managed close to ADC source signal (outside the brick).

There is also 2 optional ADC external trigger (ADC_EXT_TRIGGER0 & ADC_EXT_TRIGGER1) available on GPIO1_43/GPIO1_54 & GPIO1_58/GPIO1_48).

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4.10 PCIe

4.10.1 Supported standards

The PCIe interface is compliant with the electrical parameters specified in PCI Express® Base Specification Revision 4.0, February 19, 2014 (PCI_Express_Base_4.0_Rev0.3_February19-2014.pdf).

8.4.2.17 Peripheral Component Interconnect Express (PCIe)

The PCIe subsystem supports the following main features:

- Dual mode – root port (RP) or end point (EP) modes. Selectable through bootstrap pins.
- 1-lane configuration with up to 5.0GT/lane.
- 62.5/125 MHz operation on PIPE interface for Gen1/Gen2 respectively
- Constant 32-bit PIPE width for Gen1/Gen2 modes
- Maximum outbound payload size of 128 bytes
- Maximum inbound payload size of 128 bytes
- Maximum remote read request size of 4K bytes
- Maximum number of nonposted outstanding transactions: 8 on each VBUSM interface.
- Four virtual channels (4VC)
- Resizable BAR capability
- SRIS support
- Power Management
  - L1 Power Management Substate support
  - D1 support
  - L1 Power Shutoff support
- Legacy, MSI, and MSI-X interrupt support
- 32 outbound address translation regions
- Precision time measurement (PTM)

And also compliant with [REF11] (PCI Express Card ElectroMechanical).

4.10.2 Bandwidth

PCIe interface support revision 4.0 limited to Gen2 (or Gen1) bandwidth:

PCI Express link performance[47][48]

Version	Intro-duced	Line code		Transfer rate per lane[i][ii]	Throughput[i][iii]				
					x1	x2	x4	x8	x16
1.0	2003	NRZ	8b/10b	2.5 GT/s	0.250 GB/s	0.500 GB/s	1.000 GB/s	2.000 GB/s	4.000 GB/s
2.0	2007			5.0 GT/s	0.500 GB/s	1.000 GB/s	2.000 GB/s	4.000 GB/s	8.000 GB/s
3.0	2010		128b/130b	8.0 GT/s	0.985 GB/s	1.969 GB/s	3.938 GB/s	7.877 GB/s	15.754 GB/s
4.0	2017			16.0 GT/s	1.969 GB/s	3.938 GB/s	7.877 GB/s	15.754 GB/s	31.508 GB/s
5.0	2019			32.0 GT/s	3.938 GB/s	7.877 GB/s	15.754 GB/s	31.508 GB/s	63.015 GB/s
6.0	2022	PAM-4 FEC	1b/1b FLIT	64.0 GT/s 32.0 GBd	7.563 GB/s	15.125 GB/s	30.250 GB/s	60.500 GB/s	121.000 GB/s
7.0	2025 (planned)			128.0 GT/s 64.0 GBd	15.125 GB/s	30.250 GB/s	60.500 GB/s	121.000 GB/s	242.000 GB/s

4.10.3 REFCLK

There are 3 RefClk architectures:

- Common Refclk (CC) = same Refclk for Root Complex & Endpoint, transmitted additionnaly to data
- Data Clocked (DC) = Refclk is embedded into Data Stream (require a recovery PLL and use RefClk as reference clock design)
- Independent Refclks(IR) = Root Complex & Endpoint have their own Refclk (require a recovey PLL for data stream, and there is another independent local clock)

AM64 seems to support only common refclk architecture (CC).

When AM64 is configured as root complex, SoC will provided RefClk (SERDES0_REFCLK0). Otherwise, AM64 will be used as endpoint and RefClk will be provided by PCIe connector to SERDES0_REFCLK0, which is in fact bidirectional.

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According to Errata sprz457g.pdf #i2236 AM64 rev2.0 can generate a clean jitter free RefClk, it is no longer necessary to be managed outside the brick with a multiple output clock buffer (like on EVM GP).

Chap 8.6.2 and 8.6.3 of the standards ([REF18]) show RefClk parameters independent of data rate:

Table 8-17: REFCLK DC Specifications and AC Timing Requirements

Symbol	Parameter	100 MHz Input		Unit	Note
		Min	Max		
Rising Edge Rate	Rising Edge Rate	0.6	4.0	V/ns	2, 3
Falling Edge Rate	Falling Edge Rate	0.6	4.0	V/ns	2, 3
V_{IH}	Differential Input High Voltage	+150		mV	2
V_{IL}	Differential Input Low Voltage		-150	mV	2
V_{CROSS}	Absolute crossing point voltage	+250	+550	mV	1, 4, 5
$V_{CROSS\ DELTA}$	Variation of V_{CROSS} over all rising clock edges		+140	mV	1, 4, 9
V_{RB}	Ring-back Voltage Margin	-100	+100	mV	2, 12
T_{STABLE}	Time before V_{RB} is allowed	500		ps	2, 12
$T_{PERIOD\ AVG}$	Average Clock Period Accuracy	-300	+2800	ppm	2, 10, 13
$T_{PERIOD\ ABS}$	Absolute Period (including Jitter and Spread Spectrum modulation)	9.847	10.203	ns	2, 6
$T_{CCJITTER}$	Cycle to Cycle jitter		150	ps	2
V_{MAX}	Absolute Max input voltage		+1.15	V	1, 7
V_{MIN}	Absolute Min input voltage		- 0.3	V	1, 8
Duty Cycle	Duty Cycle	40	60	%	2
Rise-Fall Matching	Rising edge rate (REFCLK+) to falling edge rate (REFCLK-) matching		20	%	1, 14
Z_{C-DC}	Clock source DC impedance	40	60	Ω	1, 11

Table 8-18: Data Rate Independent Refclk Parameters

Symbol	Description	Limits	Units	Notes
F_{REFCLK}	Refclk Frequency	99.97 (min), 100.03 (max)	MHz	
F_{SSC}	SSC frequency range	30 (min), 33 (max)	kHz	3
$T_{SSC-FREQ-DEVIATION}$	SSC deviation	-0.5 (min), 0.0 (max)	%	3
$T_{TRANSPORT-DELAY}$	Tx-Rx transport delay	12 (max)	ns	1, 4
$T_{SSC-MAX-FREQ-SLEW}$	Max SSC df/dt	1250	ppm/us	2, 3

Notes:

1. Parameter is relevant only for common Refclk architecture.
2. Measurement is made over 0.5µsec time interval with an 1st order LPF with an f_c of 60x the modulation frequency.
3. When testing the a device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.
4. There are form factors (for example topologies including long cables) that may exceed the transport delay limit. Extra jitter from the large transport delay must be accounted by these form factor specifications.

NB: SSC means Spread Spectrum Clock.
This capability is supported by AM64 (see chap 5.4.5.4.2 of [REF1]) on PLL0/1/2/8/12/14; but there are some deepest restrictions.

Chap 8.6.1 show that $Z_{DIF}F$ = 100Ω±10%

Chap 2.1.1 of the [REF11] ask to respect:

- Overall maximum trace length < 15”
- On endpoint side (i.e. : add-in card) trace length < 4”
- a transport delay between clock and data < 12ns
- matched length < 5 mils (static phase < 5 mils)

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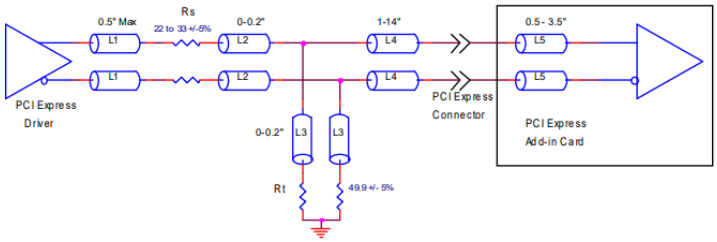
PCIE_REFCLK_2.pdf

According to T.I. E2E forum , REFCLK interface have HCSL driver/receiver interface; wich requires termination resistor:
Renesas give some advices about HCSL drivers :

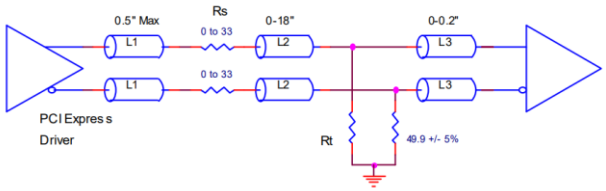
Figure 1. Termination for Applications Where Driver and Receiver will be on Separate PCBs



The implementation choose for PCIe is connector+Add_in card. So R_S & R_T will be placed close to source according above diagram.

In case of PCIe back plane implementation, the following diagram must be implemented:

Figure 2. Termination for Applications Where a Point-to-Point Connection can be Used



NB: To better understand where are located each component, please take a look a L1/L2/L3 length

4.10.4 PERST#

PERST is the fundamental reset (pull-push IO) which allow to disable all interface of PCIe endpoint according to [REF11] chapter 2.2.1:

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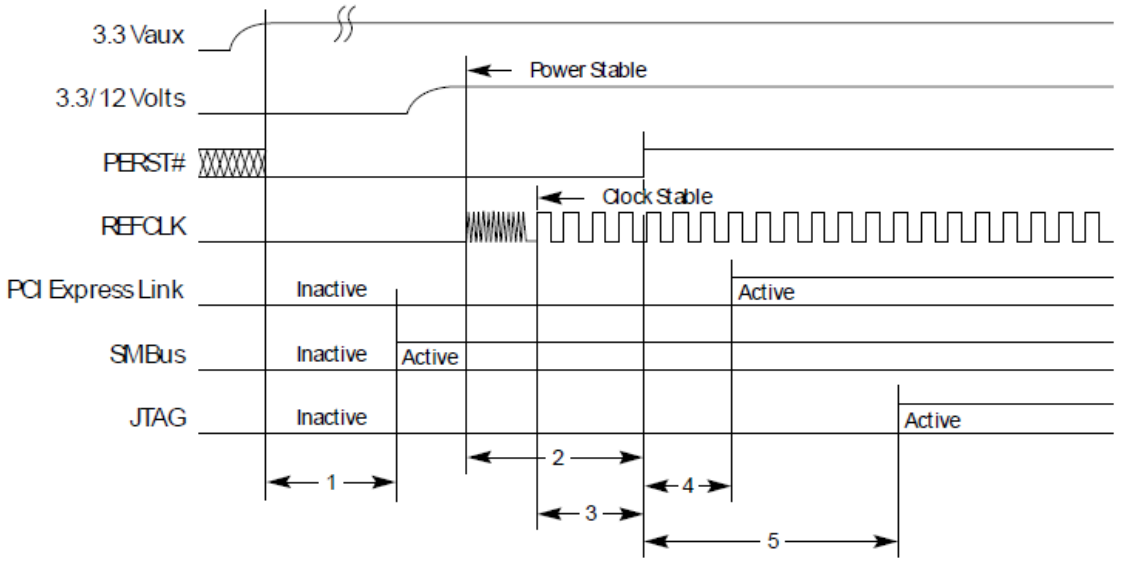

1. 3.3Vaux stable to SMBus driven (optional). If no 3.3Vaux on platform, the delay is from +3.3V stable
2. Minimum time from power rails within specified tolerance to PERST# inactive (T_{PVPERL})
3. Minimum clock valid to PERST# inactive ($T_{PERST\text{-}CLK}$)
4. Minimum PERST# inactive to PCI Express link out of electrical idle
5. Minimum PERST# inactive to JTAG driven (optional)

OM14742B

Figure 8: Power Up

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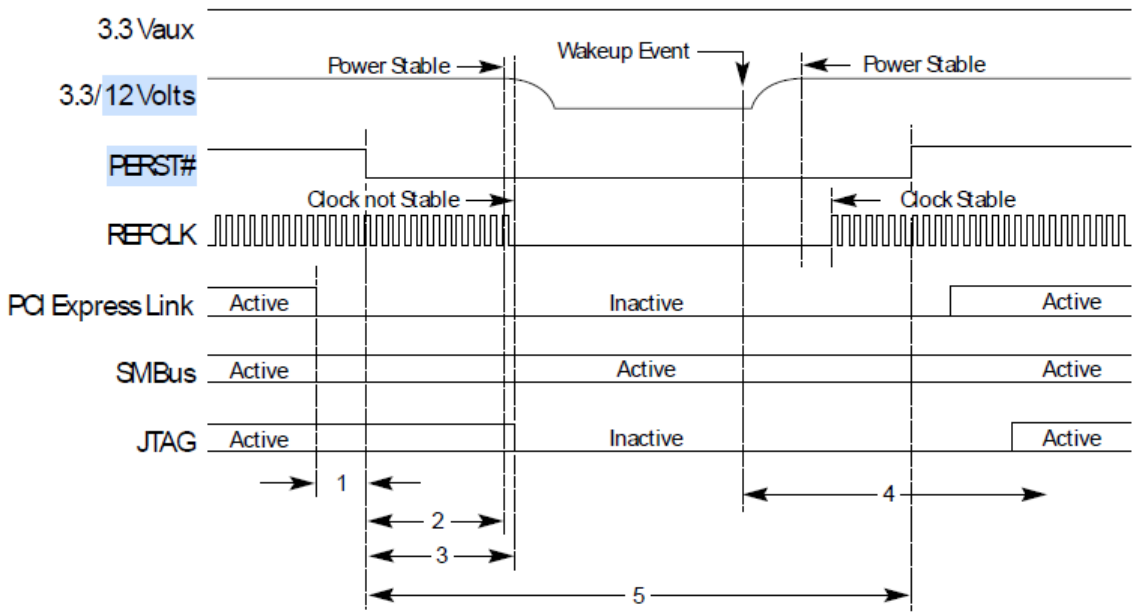

1. The PCI Express link will be put into electrical idle prior to PERST# going active.
2. PERST# goes active before the power on the connector is removed.
3. Clock and JTAG go inactive after PERST# goes active.
4. A wakeup event resumes the power to the connector, restarts the clock, and the sequence proceeds as in power up.
5. The minimum active time for PERST# is T_{PERST}.

OM14743E

Figure 9: Power Management States

PERST assertion helps endpoint to not lock its PLL on REFCLK until REFCLK is stable (prevent not falling into unknow state due to metastability).
PERST de-assertion helps also root complex and device to not drive their SERDES until PERST de-assert.

When AM64 is root complex he must drive PERST#.
When AM64 is in endpoint he must receive and be reset by this signal coming for PCIe connector.
These features are managed outside the brick into AETHENA board BQT15769.

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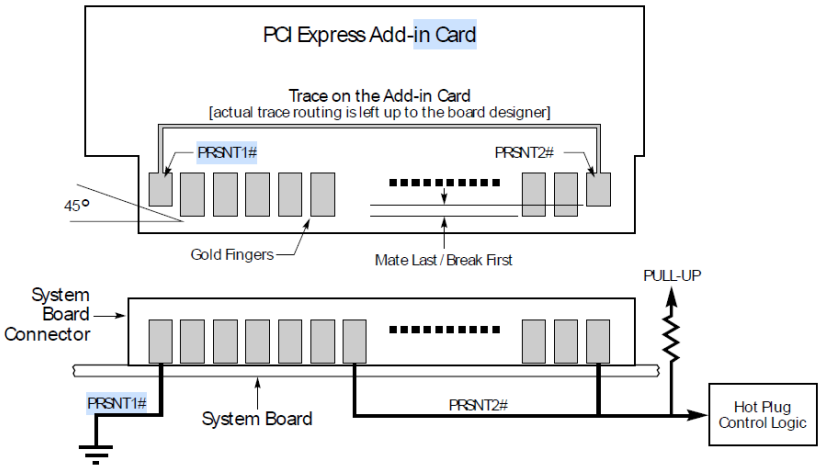
4.10.5 PRSNT1# & PRSNT2#

According to [REF11] , these signals are used for Hotplug detection and also to determine the size of the Add-in card (in our case it's not used):



This is managed into AETHENA board.

4.10.6 CLKREQ#

According to [REF11] , it's an optional open drain active low signal driven by the card-in endpoint to request REFCLK to be available by root complex.
It's mainly used for low power Link mode L1 entry/exit substate.
When unused, it has to be pullup according Chap 2.7.1 of [R11] :
10KΩ to +3.3V PCIe (not 3.3Vaux).

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Table 3: Auxiliary Signal DC Specifications – PERST#, WAKE#, CLKREQ#, SMBus and PWRBRK#

Symbol	Parameter	Conditions	Min	Max	Unit	Notes
V_{IL1}	Input Low Voltage		-0.5	+0.8	V	2, 6, 7
V_{IH1}	Input High Voltage		+2.0	V_{cc3_3} + 0.5	V	2, 6, 7
V_{IL2}	Input Low Voltage		-0.5	+0.8	V	4
V_{IH2}	Input High Voltage		+2.1	+3.3 Vaux + 0.5	V	4
V_{OL1}	Output Low Voltage	4.0 mA		+0.2	V	1, 3
V_{HMAX}	Max High Voltage			V_{cc3_3} + 0.5	V	3
V_{OL2}	Output Low Voltage	4.0 mA		+0.4	V	1, 4
I_{in}	Input Leakage Current	0 to +3.3 V	-10	+10	µA	2, 4, 7
I_{lkg}	Output Leakage Current	0 to +3.3 V	-50	+50	µA	3, 5
C_{in}	Input Pin Capacitance			7	pF	2, 7
C_{out}	Output (I/O) Pin Capacitance			30	pF	3, 4
$R_{PULL-UP}$	Pull-up Resistance		9	60	kΩ	8

Notes:

1. Open-drain output a pull-up is required on the system board. There is no V_{OH} specification for these signals. The number given is the maximum voltage that can be applied to this pin.
2. Applies to PERST#.
3. Applies to WAKE# and CLKREQ#.
4. Applies to SMBus signals SMBDAT and SMBCLK.
5. Leakage at the pin when the output is not active (high impedance).
6. Applies to WAKE# issued by Switch Downstream Ports and Root Complex for signaling of OBFF indications as received at the input of the Endpoint(s).
7. Applies to PWRBRK#.
8. Applies to CLKREQ# pull-up on host system.

This signal is present into AM64 (PCIE0_CLKREQn) as alternate function of ball D16; into TI EVM GP this pin is not connected to PCIe connector and used to another purpose.

By default, this signal is GPIO1_58 ball D16, if required it has to be activated in the sysconfig tool in PCIe group. For instance, it would be connected to CLKREQ# signal pin connector with 10KΩ external dedicated pullup.

4.10.7 WAKE#

Is an optional open drain active low signal to wake up PCIe links & reference clock or for OBFF (Optimized Buffer Flush/ Fill) mechanism.
In our case we do not support WAKE# function, so it has to be pullup according to Chap 2.7.1 of [REF11]:
10KΩ to +3.3V PCIe (not 3.3Vaux).

4.10.8 JTAG

They are optional signals to support IEEE 1149.1 (Test Access port and Boundary Scan).
We won't use this feature on PCIe connector, so pin will be left unconnected.

4.10.9 SMBus (SMBCLK/SMBDAT)

They are optional signal open drain architecture. It's based on the principle of I^2C operations.
It will be managed outside the brick into AETHENA board.

4.10.10 PERn0 & PERp0

For 2.5GT/s the UI is defined as 400ps (1 UI = 1/(2 x Freq) = 1/(2*1.25E^9 Hz), and 200ps for 5GT/s.
In short 2.5GT/s @1.25GHz and 5GT/s @2.5GHz.

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PCIe standard support lane polarity inversion recovery mechanism: see [REF18]

According to Chap 4.7.7 / 4.7.8 / 4.7.9 of [REF11], it requires electrical features:

- Max skew (static phase) within differential pair < 2.5mils for add-in card and < 5mils for system. We support both case (Endpoint and Root complex), so the worst applies.
- Differential impedance in range 68-105Ω (100Ω ±5% for more confidence)
- For add-in card propagation delay from receiver/transmitter to connector <750ps

Chap 4.8 of [REF11] specifies all eye diagram recommendations.

A maximum of 2 vias is allowable, avoid stub and respect has much a possible these kind of recommendations for return path and reference ground place and additional GND via (extract of Ti slaae45 Layout Guidelines of PCIe® Gen 4.0.pdf):

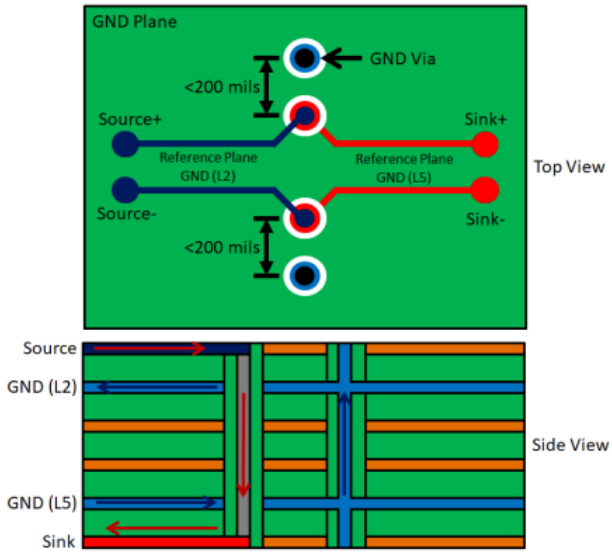

Figure 2-3. Differential Pair Via Return Path With GND Vias

Also slaae45 Layout Guidelines of PCIe® Gen 4.0.pdf mains recommendation are :

Table 2-1. Parameters of PCIe® Standard

Parameter	Value
Frequency	PCIe® Gen 1: 1.25 GHz (2.5 Gbps)
	PCIe® Gen 2: 2.5 GHz (5 Gbps)
	PCIe® Gen 3: 4 GHz (8 Gbps)
	PCIe® Gen 4: 8 GHz (16 Gbps)
AC Coupling Capacitors	AC capacitors required: 75 nF–220 nF
Polarity Reversal	Allowed
Max Intra-Pair Skew	5 mils
Max Inter-Pair Skew	No Inter-pair specification
Trace Impedance	PCIe® Gen 1 and 2:100 Ω ±5% differential; 50 Ω ±5% single ended
	PCIe® Gen 3 and 4: 85 Ω ±5% differential; 42.5 Ω ±5% single ended

Finally [REF15] summarize many informations :

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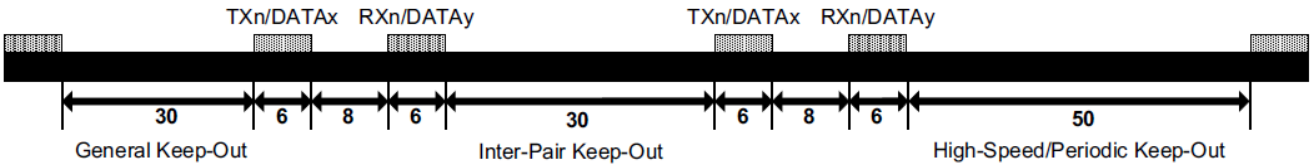


Figure 3-1. USB3/SATA/PCIe/HDMI/SGMII/CSI Differential Signal Spacing (mils)

Table A-6. AM64x

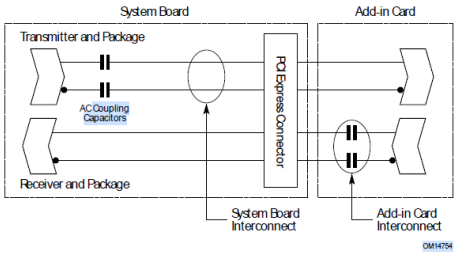
Parameter	MIN	TYP	MAX	Unit
USB3.1 GEN1 Tracelength (Total)			5500	Mils
PCI-Express (PCIe) Tracelength (Total)			5500	Mils
USB2.0 Tracelength (Total)		4000	12000	Mils
SuperSpeed Insertion Loss at 2.5GHz (device to connector)	Refer to USB Specification			dB
Skew within any USB3/PCIe differential pair			5	Mils
Skew between all PCIe RX pairs (Total)			6	ns
Skew between all PCIe TX pairs (Total)			1.5	ns
Skew within any USB2.0 differential pair			50	Mils
USB2.0 DP or DM pair differential impedance	81	90	99	Ohms
SuperSpeed SSRX or SSTX pair differential impedance	90.25	95	99.75	Ohms
PCI-Express RX or TX pair differential impedance	90.25	95	99.75	Ohms
Number of stubs allowed on any differential pair trace (Total)			0	Stubs
Number of vias allowed on any USB3/PCIe differential trace (Total)			2	Vias
Number of vias allowed on each USB2.0 differential trace (Total)			4	Vias
Number of test points permitted on any differential pair trace (Total)			0	Test Points
Differential pair to clock or high-speed periodic signal trace spacing	50			Mils
Differential pair to any other signal trace spacing	30			Mils

4.10.11 PETn0 & PETp0

Same specification as PERn0/PERp0 + AC coupling capacitors.

4.10.11.1 AC coupling capacitor

Chap 4.6.2 of [REF11] requires AC coupling capacitor on TX side:



Chap 8.3.9 of [REF18] requires values between:

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C_{TX}	AC Coupling Capacitor	176 (min) 265 (max)	nF	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.
$Z_{TX\text{-}DIFF\text{-}DC}$	DC differential Tx impedance	120 (max)	Ω	Low impedance defined during signaling. The minimum value is bounded by $RL_{TX\text{-}DIFF\text{-}}$

So 220nF is a good value. This will be managed outside the brick.

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Void ground plane under component pad to decrease loss:

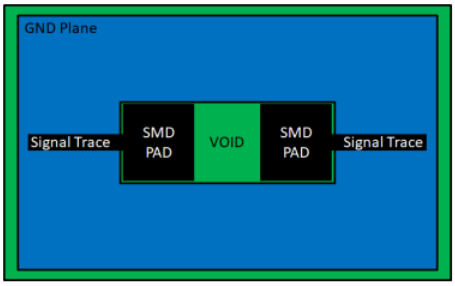

Figure 2-5. Void Below Surface Mount Devices

(There will be always another reference ground plane in the deeper layers)

4.10.12 Layout recommendations summary

According to chapter PER & PET we will apply following layout constraints:

	PCIe rev4.0 std recommendations	TI SPRAAR7J recommendations	BRICK SETTINGS
AC capacitor	220nF±20%	75-220nF (SLAAE45)	220nF+-10% 0402$_{max}$ size
Polarity reversal	authorized	Authorized (SLAAE45)	authorized
Max trace length	-	5500 mils (139mm)	5500 mils (139mm)
REFCLK trace max length	<15” (381mm)		
REFCLK trace card_in length	<4” (101mm)		<4” (101mm)
System board static phase	<5mils (127µm)	<5mils (127µm)	<5mils (127µm)
Add-in card static phase	<2.5mils (50.8µm)		<2.5mils (50.8µm)
Skew between PER pairs	-	6ns $_{max}$ (RX)	n.a. (only 1 pair)
Skew between PET pairs	-	1.5ns $_{max}$ (TX)	n.a. (only 1 pair)
REFCLK (pair) to PER/PET (pair) prop. delay	<12ns	-	<12ns
Add-in card prop. delay (by pair)	<750ps	-	<750ps
REFCLK differential pair	100Ω±10%	95Ω±5%	95Ω±5%
PER/PET differential pair	68-105Ω		
PER/PET single ended	-		n.a.
Stub length (track or via)	-	<15mils (381µm) (SLAAE45)	<15mils (381µm)
#Vias per pair	-	2 max	2 max
Pair to noisy signal (e.g. : clock)	-	50 mils (1270µm)	50 mils (1270µm)
Pair to quiet signal	-	30 mils (762µm)	30 mils (762µm)

Please check [REF2] table 6-80 when SERDES is unused for I/O powering.

Reminder: layout brick specifications are PCIe and USB3.1 compatible. If one specification change for PCIe, impact must be checked on USB3.1 side also; and vice versa.

4.10.13 Other AM64 pin recommendations

4.10.13.1 SERDES0_REXT

According to [REF1] chap 12.2.3.2.1, it requires a 3.01KΩ±1%.

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4.10.14 Powering

+12V/+3.3V/+3.3Vaux rails
All power rails will be managed outside the brick into AETHENA board BQT15769.

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4.11 USB HOST/DEVICE/OTG

According to [REF2] AM64 provide a USB Subsystem System which handle these features:

8.4.2.22 Universal Serial Bus Subsystem (USBSS)

The Universal Serial Bus Subsystem (USBSS) module supports the following main features:

General USB interface:
- Compliant with USB 3.1 specification
- Compliant with xHCI 1.1 specification
- Port configurable as:
  - USB host:
    - SuperSpeed Gen 1 (5 Gbps)
    - High-speed (480 Mbps)
    - Full-speed (12 Mbps)
    - Low-speed (1.5 Mbps)
  - USB device/peripheral:
    - High-speed (480 Mbps)
    - Full-speed (12Mbps)
  - USB Dual-Role device

USB Host mode features:
- 64 slots
- Up to 96 periodic simultaneous endpoints
- 256 primary streams
- MSI
- Root hub

USB0 interface is compliant with Universal Serial Bus Revision 2.0 Specification dated April 27, 2000 including ECNs and Errata as applicable.
USB0 instance is compliant with the USB3.1 SuperSpeed Transmitter and Receiver Normative Electrical Parameters as defined in the Universal Serial Bus 3.1 Specification, Revision 1.0, July 26, 2013.
Subsytem overview with external signals:

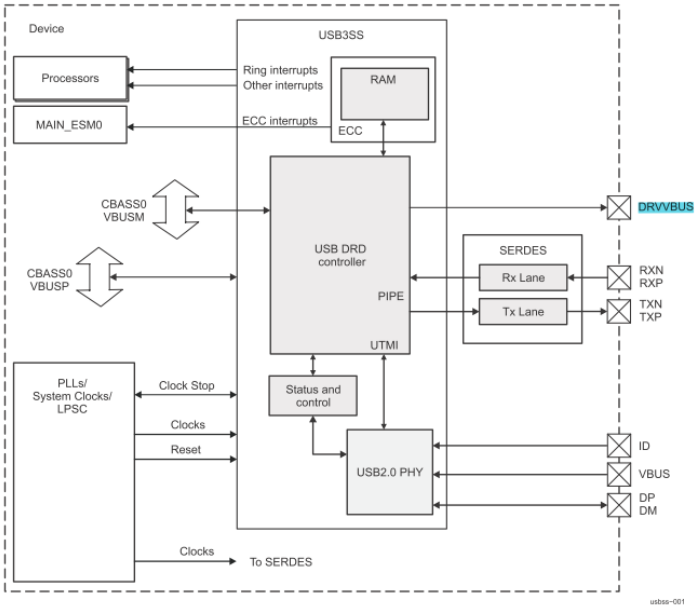

Figure 12-1280. USB Subsystem Overview

4.11.1 USB0_ID

USBSS (USB SubSystem) handle Host/Device/OTG (=dual Role) by sensing USB0_ID pin, according to [REF1] is not very clear on USB_ID internal pullup capability:

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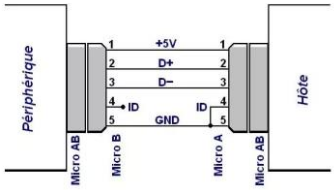
- Host: USB0_ID signal grounded
- Device: USB0_ID signal left floating
- OTG : USB0_ID signal is floating or grounded depending of the attached cable type (micro A or micro B) :



According to Universal Serial Bus Revision 2.0 Specification dated April 27, 2000 & USB_OTG_and_EH_2-0-version 1_1a.pdf & Micro-USB_1_01.pdf, R_{ID} should be lower than $10\Omega_{MAX}$ (shorted to ground) or greater than $100k\Omega_{MIN}$ (left floating).

According E2E forum, let USB0_ID pin floating is enough to operate in device mode.
Same conclusion on EVM GP rev.C: left floating for OTG.

AM64 USB0_ID forum.pdf

Furthermore according to [REF2] :

(7) The USB0_ID pin is connected to analog circuits in the USB0 PHY. The analog circuits source a known current while measuring voltage, to determine the resistance value (RID), if connected to VSS through a resistor. This pin should be connected to VSS for USB host operation, or left unconnected for USB device operation, and should never be connected to any external voltage source.

So, the pin is current sourced and voltage sensed to detect a connection to VSS (R_{ID} measurement).

According to TI support, this pin can detect different R_{ID} values described into BC1.2 plus errata 2012-3-15.pdf:

RE_ USB0_ID floating pin_.msg

ACA ID pull-down, OTG device as A-device	R_{ID_A}	1), 2), 4)	122	126	kΩ	6.2.4
ACA ID pull-down, OTG device as B-device, can't connect	R_{ID_B}	1), 2), 4)	67	69	kΩ	6.2.4
ACA ID pull-down, OTG device as B-device, can connect	R_{ID_C}	1), 2), 4)	36	37	kΩ	6.2.4
ACA ID pull-down when ID_OTG pin is floating	R_{ID_FLOAT}	2), 3)	220		kΩ	6.2.4
ACA ID pull-down when ID_OTG pin is grounded	R_{ID_GND}	2), 3)		1	kΩ	6.2.4

And TI doesn't recommend connecting any resistor to any voltage, excepted VSS.

Furthermore, according to Micro-USB_1_01.pdf, RID should be <10Ω or >100kΩ:

Table 4-2. Micro-A Plug Pin Assignments

Contact Number	Signal Name	Typical Wiring Assignment
1	VBUS	Red
2	D-	White
3	D+	Green
4	ID	<Ra_PLUG_ID
5	GND	Black
Shell	Shield	Drain Wire

The ID pin on a Micro-A plug shall be connected to the GND pin. The ID pin on a Micro-B plug is not connected or is connected to ground by a resistance of greater than Rb_PLUG_ID (100kΩ MIN). An On-The-Go device is required to be able to detect whether a Micro-A or Micro-B plug is inserted by determining if the ID pin resistance to ground is less than Ra_PLUG_ID (10Ω MAX) or if the resistance to ground is greater than Rb_PLUG_ID . Any ID resistance less than Ra_PLUG_ID shall be treated as ID = FALSE and any resistance greater than Rb_PLUG_ID shall be treated as ID = TRUE.

More precisely MicroUSB ECN.pdf recommend having Rb_PLUG_ID > 1MΩ (=R_{ID} >1MΩ).

According to TI's recommendation, we left USB0_ID floating to handle Device/OTG feature.

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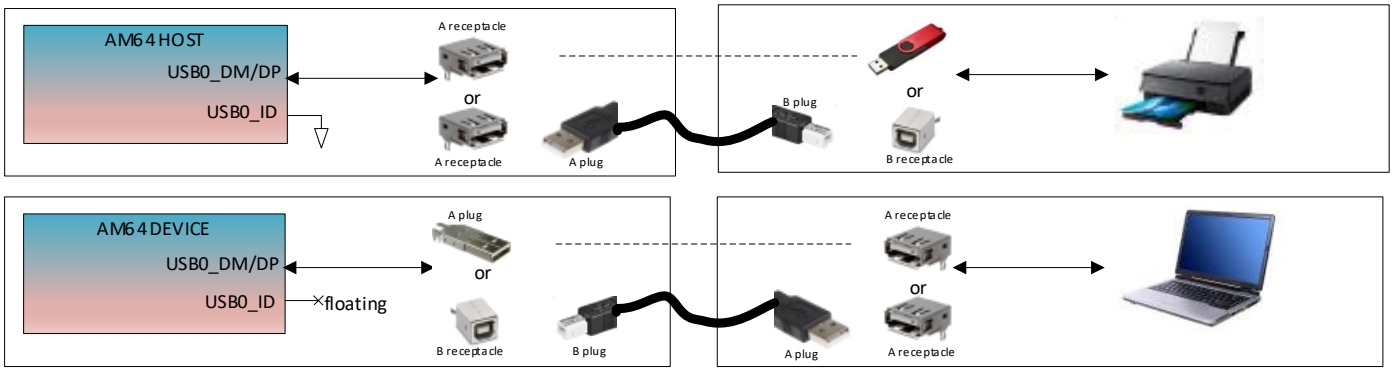
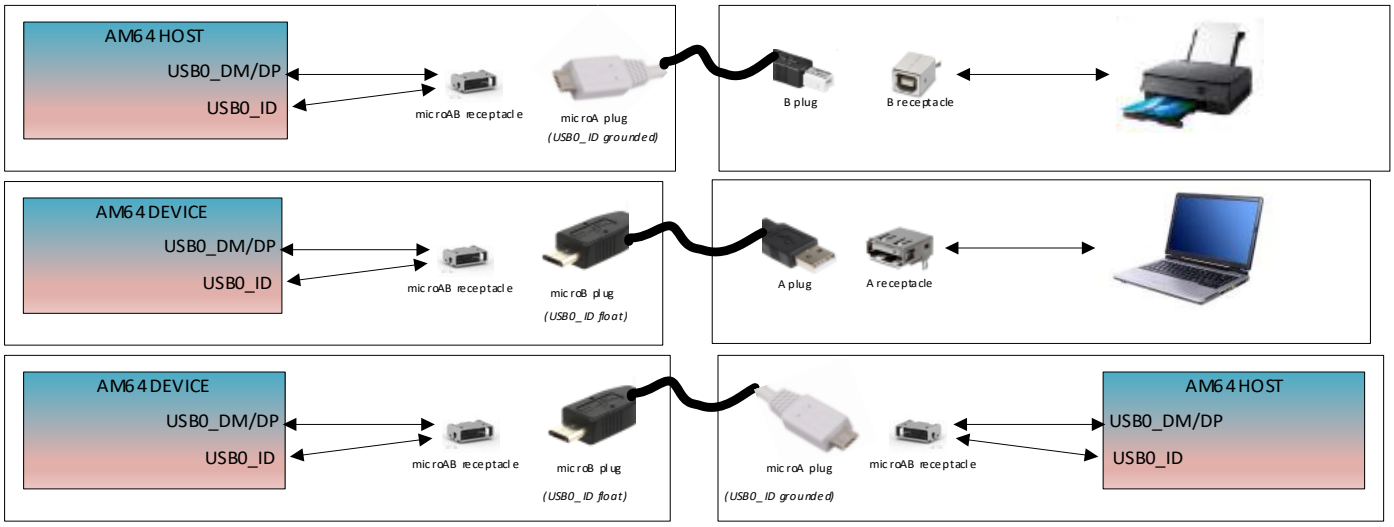
4.11.1.1 Use cases

Without using OTG function feature : type ‘A’ connector/plug define HOST side, and type ‘B’ connector/plug define DEVICE side :



When using OTG function, it can be done by using microAB receptacle connector, which can receive microA or microB plug. In this case, the USB0_ID signal connected to microAB receptacle connector is grounded into microA plug, or left floating into microB plug:



In the last use case using microB plug ⇔ microA plug cable, thanks to HNP (Host Negociation Protocol), it’s possible to exchange HOST/DEVICE role without disconnect/swap cable/reconnect.

4.11.2 USB0_VBUS

VBUS could rise to 5.5V according USB3.1 specification.
According to [REF2], USB0_VBUS pin maximum rating is about 3.6V :

PARAMETER		MIN	MAX	UNIT
Steady-state max voltage at all other IO pins(5)	USB0_VBUS(6)	-0.3	3.6	V
	USB0_ID(7)	-0.3	3.6	
	All other IO pins	-0.3	IO supply voltage + 0.3	V

The same datasheet recommends the following architecture to handle with VBUS up to 30V (automotive constraints):

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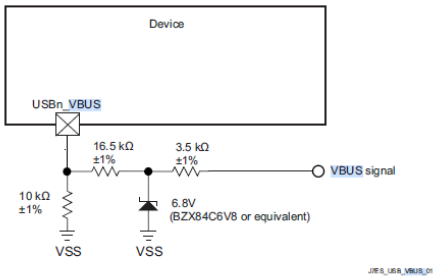
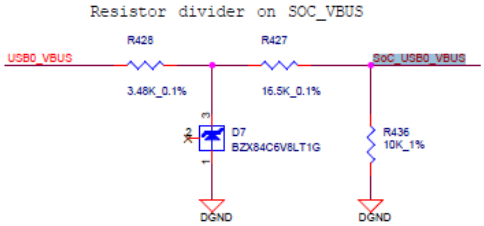


Figure 9-4. USB VBUS Detect Voltage Divider / Clamp Circuit

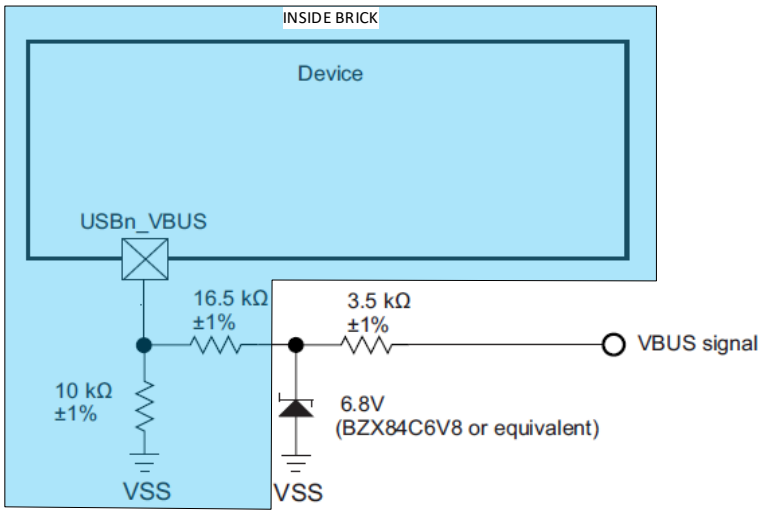
which is implemented on EVM GP & SK:



5 volt compatible VBUS pin	This function is not possible because the USB2 PHY implements 3.3v ESD on the VBUS pin. Note: The VBUS signal should be applied to a 20k/10k voltage divider which divides the potential by 3. This allows the VBUS signal to go up to 10.75 volts before exceeding the VBUS pin maximum of 3.63 volts.

Resistor bridge 1/3 (10K/20K) equivalent architecture will be implemented partially:

- into the brick:
  10K/16.5K
- outside the brick:
  3.46K/Zener 6V8 (which allow to user to add or not Zener protection for VBUS >5.5V).



USB0_VBUS max absolute rating is about 3.6V, and max voltage 3.465V.

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4.11.3 USB0_DRVVBUS

USB0_DRVVBUS allow to drive an external to the brick load switch (which should include short/overload protection) which control USB VBUS power depending on the AM64 role (host or device).
Logic level is LVCMOS3.3 output, active high.
Note: When USB BOOTMODE is selected in DFU mode, then USB0_DRVVBUS is configured even if unused => take care when using it in simple GPIO mode.

A 10KΩ must be added outside the brick to manage default pin value; will be managed outside the brick into AETHENA board BQT15769.

4.11.4 USB0_RCALIB

According to [REF2] Rcalib should be 499Ω 1% 7.2mW

USB0_RCALIB (1)	A	Pin to connect to calibration resistor	U17
USB0_VBUS (2)	A	USB Level-shifted VBUS Input	T14

(1) An external 499 Ω ±1% resistor must be connected between this pin and VSS. The maximum power dissipation for the resistor is 7.2mW. No external voltage should be applied to this pin.

SPN HUA28863 is connected to VSS 499Ω 1% 100pmm 63mW.

4.11.5 USB0_DM / USB0_DP

According to [REF15], isolation of DM/DP pair should be at least 5W (5 times the track width) for standard signal, and 8W for clock signals:

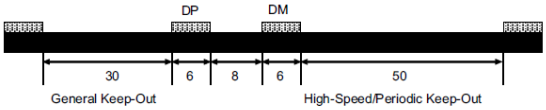

Figure 3-2. USB2 Differential Signal Spacing (mils)

Table A-6. AM64x

Parameter	MIN	TYP	MAX	Unit
USB3.1 GEN1 Tracelength (Total)			5500	Mils
PCI-Express (PCIe) Tracelength (Total)			5500	Mils
USB2.0 Tracelength (Total)		4000	12000	Mils
SuperSpeed Insertion Loss at 2.5GHz (device to connector)	Refer to USB Specification			dB
Skew within any USB3/PCIe differential pair			5	Mils
Skew between all PCIe RX pairs (Total)			6	ns
Skew between all PCIe TX pairs (Total)			1.5	ns
Skew within any USB2.0 differential pair			50	Mils
USB2.0 DP or DM pair differential impedance	81	90	99	Ohms
SuperSpeed SSRX or SSTX pair differential impedance	90.25	95	99.75	Ohms
PCI-Express RX or TX pair differential impedance	90.25	95	99.75	Ohms
Number of stubs allowed on any differential pair trace (Total)			0	Stubs
Number of vias allowed on any USB3/PCIe differential trace (Total)			2	Vias
Number of vias allowed on each USB2.0 differential trace (Total)			4	Vias
Number of test points permitted on any differential pair trace (Total)			0	Test Points
Differential pair to clock or high-speed periodic signal trace spacing	50			Mils
Differential pair to any other signal trace spacing	30			Mils

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Into this layout guidelines file, there is a lot of basic layout principles to follow.

4.11.6 USB 2.0 Layout recommendations summary

	USB2.0 standard	spraar7j TI SPRAAR7J recommendations	BRICK SETTINGS
Polarity reversal	NOT authorized	-	NOT authorized
Max trace length	T_{FSCBL} < 26ns (~396mm(*)) $T_{Driver\ to\ connector}$ < 4ns (~61mm(*))	4” to 12” (101.6mm to 304.8mm)	50mm
Static phase	<100ps or <600mils (whole datapath pcb+connector+cable)	<50mils (1270µm)	<50mils (1270µm)
DM/DP differential pair impedance	Z_O = 90Ω±15%	90Ω±10%	90Ω±10%
DM/DP common impedance	Z_{CM} = 30Ω±30%	-	30Ω±30%
Stub (track or via)	-	<15mils (381µm)	<15mils (381µm)
#vias per pair	-	4 max	2 max

(*) = using rules of thumb of 150ps/1” or 6”/1ns

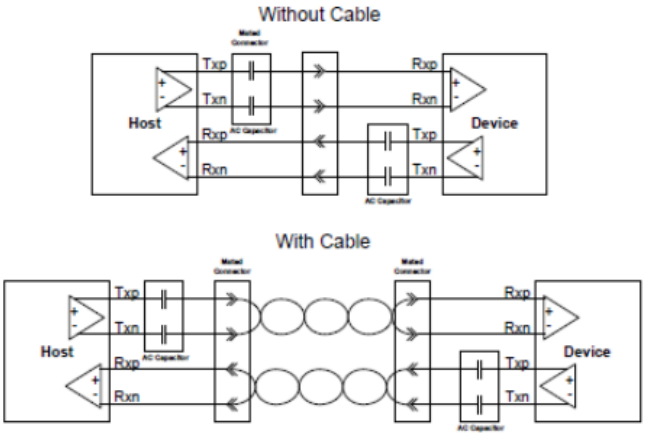
4.11.7 USB 3.1

4.11.7.1 Supported standard and functions

According to [REF2], AM64 is compliant with USB 3.1 rev 1.0 standard.
Superspeed is limited to Gen1 speed (5Gbps=2.5GHz), and only available for HOST role (not device).

4.11.7.2 AC coupling capacitor

According to [REF12] AC capacitors required on the TX data lane (optional on RX side).
According to [REF13] Figure 6-5 :



According to [REF14] optional AC coupling capacitor could be placed like that:

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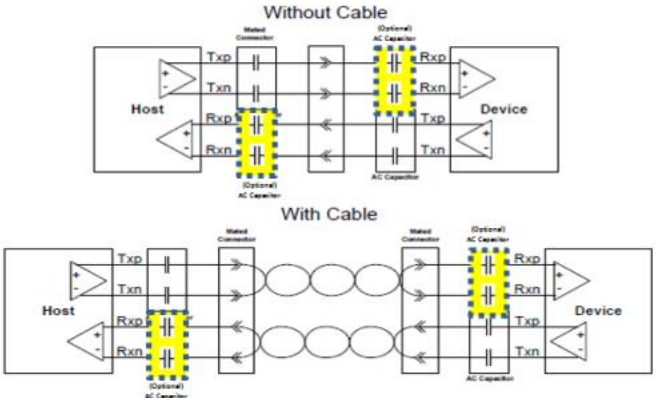

Beware to respect overall minimum capacitor value of 75nF (100nF on TX side and 330nF on RX side ~= 76Ω).

4.11.7.3 USB 3.1 Layout recommendation summary

According to [REF15] :

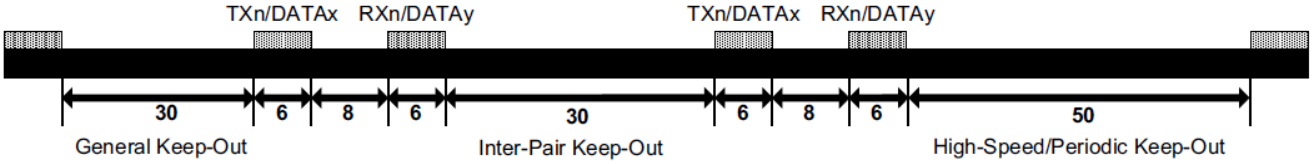

Figure 3-1. USB3/SATA/PCIe/HDMI/SGMII/CSI Differential Signal Spacing (mils)

Table A-6. AM64x

Parameter	MIN	TYP	MAX	Unit
USB3.1 GEN1 Tracelength (Total)			5500	Mils
PCI-Express (PCIe) Tracelength (Total)			5500	Mils
USB2.0 Tracelength (Total)		4000	12000	Mils
SuperSpeed Insertion Loss at 2.5GHz (device to connector)	Refer to USB Specification			dB
Skew within any USB3/PCIe differential pair			5	Mils
Skew between all PCIe RX pairs (Total)			6	ns
Skew between all PCIe TX pairs (Total)			1.5	ns
Skew within any USB2.0 differential pair			50	Mils
USB2.0 DP or DM pair differential impedance	81	90	99	Ohms
SuperSpeed SSRX or SSTX pair differential impedance	90.25	95	99.75	Ohms
PCI-Express RX or TX pair differential impedance	90.25	95	99.75	Ohms
Number of stubs allowed on any differential pair trace (Total)			0	Stubs
Number of vias allowed on any USB3/PCIe differential trace (Total)			2	Vias
Number of vias allowed on each USB2.0 differential trace (Total)			4	Vias
Number of test points permitted on any differential pair trace (Total)			0	Test Points
Differential pair to clock or high-speed periodic signal trace spacing	50			Mils
Differential pair to any other signal trace spacing	30			Mils

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	USB 3.1 standard	TI SPRAAR7J recommendations	BRICK SETTINGS
AC capacitor	75-200nF (gen1) 75-265nF (gen2)	75-220nF (SLAAE45)	220nF+-10% 0402$_{max}$ size
Polarity reversal	Authorized	Authorized (SLAAE45)	Authorized
Max trace length	-	5500 mils (139mm)	5500 mils (139mm)
Static phase (intrapair skew)	<15ps/m	<5mils (127µm)	<5mils (127µm)
Interpair skew	n.a.		
SSRX/SSTX pair differential impedance	90Ω±5Ω	95Ω±5%	95Ω±5%
SSRX/SSTX single ended	45Ω±3Ω		n.a.
Stub length (track or via)	-	<15mils (381µm) (SLAAE45)	<15mils (381µm)
#Vias per pair	-	2 max	2 max
Pair to noisy signal (e.g. : clock)		50 mils (1270µm)	50 mils (1270µm)
Pair to quiet signal		30 mils (762µm)	30 mils (762µm)

(*)= using rules of thumb of 150ps/1” or 6”/1ns

Please check [REF2] table 6-80 when SERDES is unused for I/O powering.

Reminder: layout brick specifications are PCIe and USB3.1 compatible. If one specification change for USB3.1, impact must be checked on PCIe side also; and vice versa.

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4.12 OTP (One Time Programming) eFuse

OTP should be fused for validation that the ROM bootloader well applies a firmware signature verification (responding to SecureBoot needs).

This signal VPP_EN is attended to enable the power supply for programming the OTP eFuses.

Hardware requirements:

- VPP_EN must be disable or left unconnected when not programming OTP registers,
- VPP_EN must be driven HIGH **AFTER** the proper device power-up sequence.

Programming sequence for OTP eFuses:

- Power-on the board per the power-up sequencing. No voltage should be applied on the VPP_EN signal during the power-up and normal operation,
- LOAD the OTP write software required to program the eFuses,
- Drive HIGH the VPP_EN signal to apply the voltage on the VPP terminal,
- Run the software that programs the OTP registers,
- After validating the content of the OTP registers, drive LOW the VPP_EN signal to remove the voltage from the VPP terminal.

If you don't need this feature, simply leave it unconnected at the macrocomponent port level. Internally of the macrocomponent, this net has a pull-down resistor which will keep the net to 0V.

4.12.1 Layout recommendations

Layout tracks/shape must support 400mA rated current, with VPP_{MIN} of 1.71V

From [REF2] §7.8.1. Recommended Operation Conditions for OTP eFuse Programming :

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
VDD_CORE	Supply voltage range for the core domain during OTP operation; OPP NOM (BOOT)	See *Recommended Operating Conditions*			V
VPP	Supply voltage range for the eFuse ROM domain during normal operation without hardware support to program eFuse ROM		NC(1)		V
	Supply voltage range for the eFuse ROM domain during normal operation with hardware support to program eFuse ROM		0		V
	Supply voltage range for the eFuse ROM domain during OTP programming(2)	1.71	1.8	1.89	V
$I_{(VPP)}$	VPP current			400	mA
$SR_{(VPP)}$	VPP Slew Rate			6E+4	V/s
T_J	Operating junction temperature range while programming eFuse ROM.	0	25	85	°C

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