

Skills for Life!



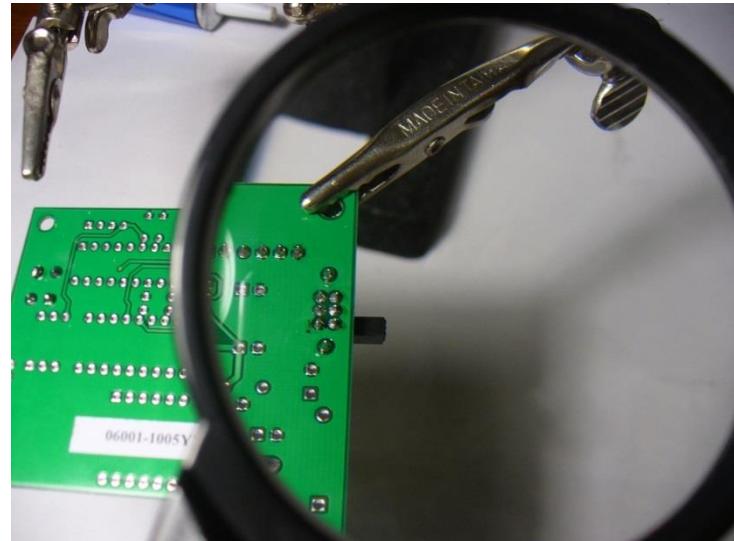
■ Department of Electrical and Electronics Skills

STUDENT HANDBOOK

Electronic Circuits Troubleshooting

IENX2215

2020



Prepared by
Industrial Electronics Skills Team

Electronic Circuits Troubleshooting



IENX 2215

Table of Contents

UNIT 1: INTRODUCTION.....	2
REVIEW OF DIGITAL ELECTRONICS:	3
UNIT 2: COMBINATIONAL CIRCUITS	6
BOOLEAN EQUATIONS.....	7
Exercise 1: Application of Logic Gates	9
Exercise 2: Equivalent Logic Circuits	14
CIRCUIT SIMPLIFICATION USING A KARNAUGH MAP	18
Exercise 3: Verification of Karnaugh Maps	22
Exercise 4: Multiplexer.....	27
Exercise 5: Demultiplexer	33
Exercise 6: Multiplexer/Demultiplexer	39
Exercise 7: Magnitude Comparator Circuits	44
UNIT 3: SEQUENTIAL CIRCUITS.....	49
SR FLIP-FLOP	50
D FLIP-FLOP.....	52
CLOCK SIGNALS.....	52
JK AND T FLIP-FLOPS	53
Exercise 8: JK Flip-Flop	55
Exercise 9: JK Flip-Flop Connected as D-Type	61
Exercise 10: Building Sequential Circuits with Flip-Flops.....	64
Exercise 11: Characteristics of a D-Type Shift Register.....	68
Exercise 12: Binary/BCD Counters and 7-Segment Decoders.....	73
Exercise 13: Analog Switch and Multivibrator IC Circuits	83
Exercise 14: Three-State Logic Circuits	97
Exercise 15: D/A and A/D Converter Circuit	102
UNIT 4: OPTOELECTRONICS	112
Exercise 16: State Indicators	113
Exercise 17: Bar-Graph Display	116
Exercise 18: 7-Segment Display	120
Exercise 19: Ancillary Circuits.....	124
Exercise 20: Exercise 18: Photoconductive Cells	128
APPENDIX 1: INTERNAL CONNECTION OF BASIC ICS	132

Unit 1: Introduction

Review of Digital Electronics:

Numbering Systems

The traditional decimal numbering system has been the standard for everyday use and for sciences like math, physics, etc. However, this system is not easy to convert to electrical signals where data transmission and processing is required. Therefore, a new binary system was proposed. The binary system has only two numbers 0 and 1 and larger numbers can be represented with more digits or bits. The number 2 for instance is expressed as 10. Later on, the binary system became the way to also convert real-life values or states to electrical signals. 0 and 1 can be used to describe day and night, sunny or cloudy, whether a football player has the ball or not, whether a student is present or absent, etc.

The hexadecimal system (base 16) was also introduced to make it easier to deal with large binary numbers. The table below shows some decimal numbers and their binary and hexadecimal equivalents:

Decimal	Binary	Hex
0	0	0
1	1	1
2	10	2
3	11	3
4	100	4
5	101	5
6	110	6
7	111	7
8	1000	8
9	1001	9
10	1010	A
11	1011	B
12	1100	C
13	1101	D
14	1110	E
15	1111	F

Logic Gates

Converting numbers or states to 0 and 1 is not useful by itself. We need to be able to use these binary values in circuits to give out a result when certain conditions are met. The logic gates that we studied in Electronic Circuits are the basic building blocks of circuits that allow this type of processing.

AND		
A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

OR		
Q	B	Q
0	0	0
0	1	0
0	0	0
1	1	1

NOT	
A	Q
0	1
1	0

Boolean Expression

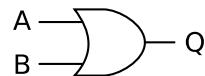
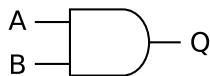
$$Q = A \cdot B$$

Or $Q = AB$

$$Q = A + B$$

$$Q = \bar{A}$$

Symbol



XOR		
A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

NAND		
Q	B	Q
0	0	1
0	1	1
0	0	1
1	1	0

NOR		
A	B	Q
0	0	1
0	1	0
1	0	0
1	1	0

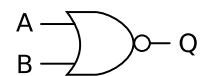
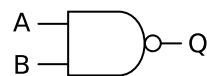
Boolean Expression

$$Q = A \oplus B$$

$$Q = \overline{A \cdot B}$$

$$Q = \overline{A + B}$$

Symbol



XNOR		
A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

Boolean Expression

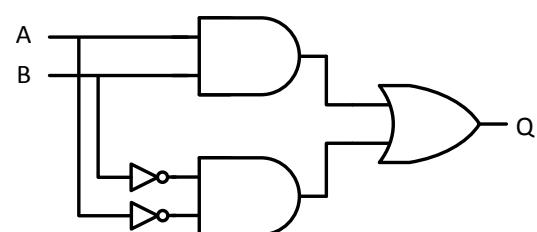
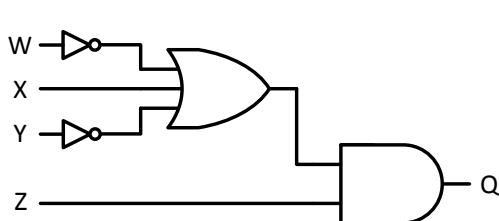
$$Q = \overline{A \oplus B}$$

Symbol



Exercises:

1. Convert $(70)_{10}$ to binary and hexadecimal.
2. Add the following two binary numbers $(101110)_2 + (1100)_2$.
3. Draw the circuits represented by the following Boolean equations:
 - a) $Q = XY + \bar{Y}Z$
 - b) $F = \overline{(A + B)} \cdot C$
4. Write down the Boolean equation of these circuit diagrams:
 - a)
 - b)



Unit 2:

Combinational Circuits

Boolean Equations

Functions can be written in different forms and perform the same output. For example,

$$F_1 = A + B$$

$$F_2 = \overline{A}B + \overline{A}\overline{B} + A\overline{B}$$

The truth table can be constructed for the above equation as:

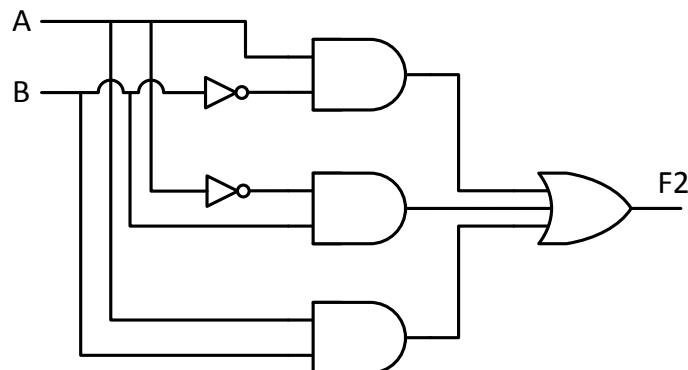
A	B	F1	F2
0	0	0	0
0	1	1	1
1	0	1	1
1	1	1	1

Since functions can have different forms, circuits can be constructed in different ways with different number of gates and connections but still have same output. Take a look at the circuits in the figure below; they both give the same output.

F1



F2



The simple circuit of F1 has less number of gates and is preferred since it is cheaper and easier to construct, test and troubleshoot.

1. Building a Digital Circuit to Do a Certain Task

To build a digital circuit that can do a certain task, we need to follow 4 steps. As an example, let's try to build a digital circuit controls the light in a classroom. The conditions for the light are as follows: The light should be ON whenever there is someone is inside the room or when the door of the room is open. The light should be off when there is nobody inside and the door is closed.

Step 1: Determine the input and the output

From the description of problem, we have two inputs which are “status of the door” and “status of the room”. The output will be the status of the light.

Step 2: Assign values for the given Conditions

Let's call the status of the room R and give it 0 when it's empty and 1 when it's occupied. For the door we will use D and give it 1 when the door is open and 0 when it's closed. Finally, L for the light and give it 0 when it's off and 1 when it's on.

Room Status (R)	
empty	0
occupied	1

Door Status (D)	
Open	1
Closed	0

Light Status(L)	
On	1
Off	0

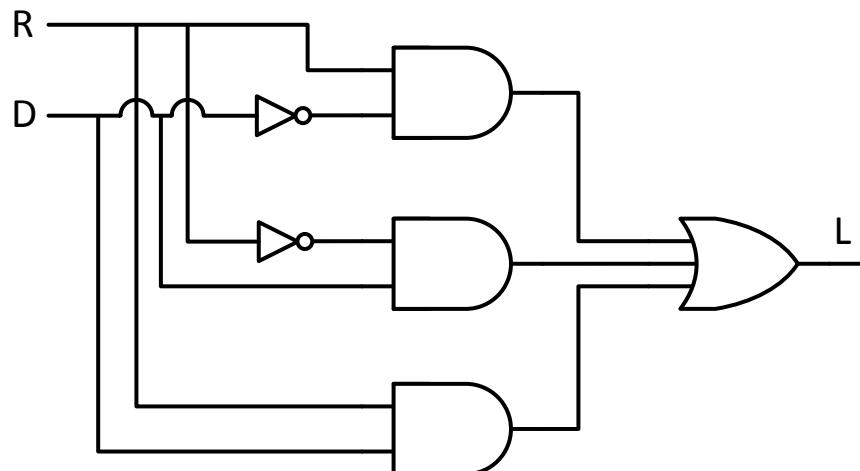
Step 3: Make truth table for the operation of the circuit

Input		Output
R	D	L
0	0	0
0	1	1
1	0	1
1	1	1

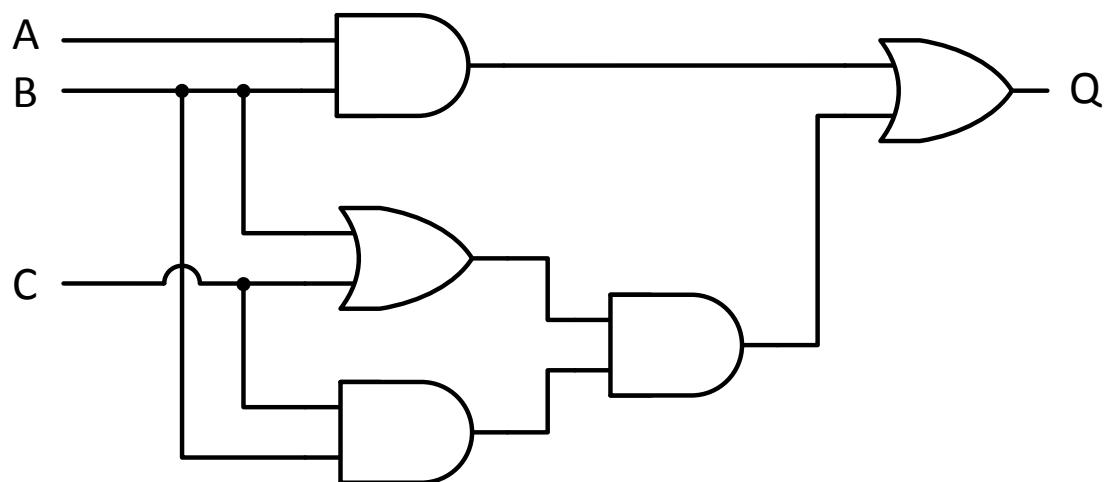
Step 4: Construct a Boolean Function from the truth table above

We choose status when the output is one

$$L = \bar{R}D + R\bar{D} + RD$$



Exercise 1: Application of Logic Gates



Objectives:

- Construct a circuit using the AND, OR and NOT logic gate.
- Appreciate the important functions of logic gates through practical applications
- Discuss the operations and functions of the logic gates through practical applications.

Equipment:

No	Name	Qty.
1.	Breadboard	1 Pc
2.	Set of IC's	-
3.	LED Probe	1 Pc
4.	Multimeter	1 Pc

Procedure:

In this exercise, you are required to find electronic solutions to several case and implement and test these solutions

Case 1:

We need to construct a circuit for a bank security system. The circuit should turn the alarm ON whenever the alarm is enabled and the front doors are opened. Construct the circuit and write down its truth table.

Case 2:

We want to design logic for an automobile warning buzzer using combinational logic. The buzzer should activate if the headlights are ON and the driver's door is opened, or if the key is in the ignition and the door is opened. *Hint: start with writing the Boolean equation of the problem.*

Review questions:

- 1) List the steps involved to construct an equation?

.....

- 2) How do you identify the number of inputs?

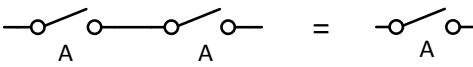
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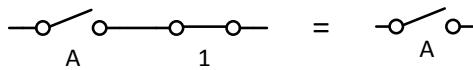
- 3) Why is this type of circuit called "combinational logic"?

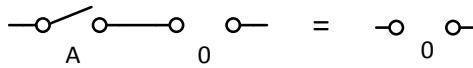
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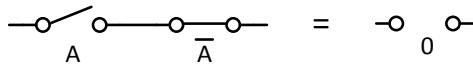
- 4) List advantages and disadvantages of this circuit.

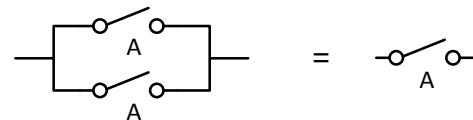
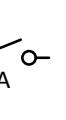
Logic Identities:

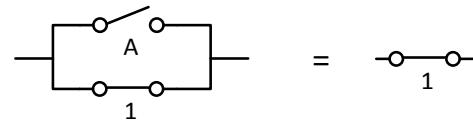
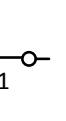
1  =  $A \cdot A = A$

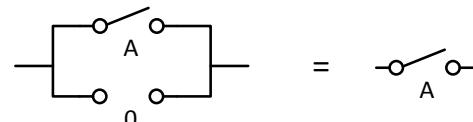
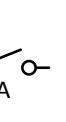
2  =  $A \cdot 1 = A$

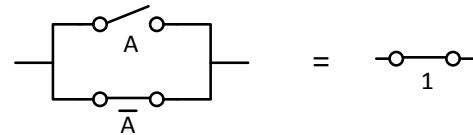
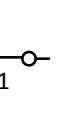
3  =  $A \cdot 0 = 0$

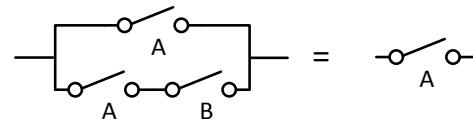
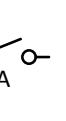
4  =  $A \cdot \bar{A} = 0$

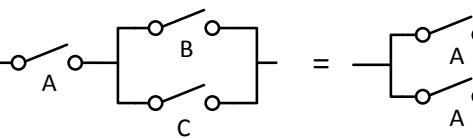
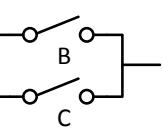
5  =  $A + A = A$

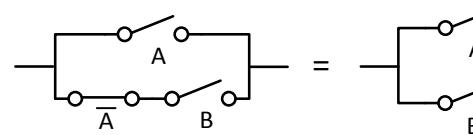
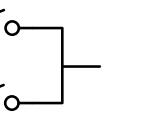
6  =  $A + 1 = 1$

7  =  $A + 0 = A$

8  =  $A + \bar{A} = 1$

9  =  $A + A \cdot B = A$

10  =  $A \cdot (B + C) = A \cdot B + A \cdot C$

11  =  $A + \bar{A} \cdot B = A + B$

12  $(A + B) \cdot (C + D) = A \cdot (C + D) + B \cdot (C + D)$

DeMorgan's Theorems

In addition to the fundamental logic identities listed above and on the previous page, there are two other identities that are commonly used when simplifying logic expressions with Boolean algebra. These are known as DeMorgan's Theorems:

$$\overline{A + B} = \overline{A} \cdot \overline{B}$$

$$\overline{A \cdot B} = \overline{A} + \overline{B}$$

Circuit Simplification Using Boolean Algebra - Worked Examples

1. A circuit is required to produce an output function F :

$$\mathbf{F} = \mathbf{A} \cdot \bar{\mathbf{B}} + \bar{\mathbf{A}} \cdot \mathbf{B} + \bar{\mathbf{A}} \cdot \bar{\mathbf{B}}$$

Show the circuit required and devise a simplified circuit.

$$F = A \cdot \bar{B} + \bar{A} \cdot B + \bar{A} \cdot \bar{B}$$

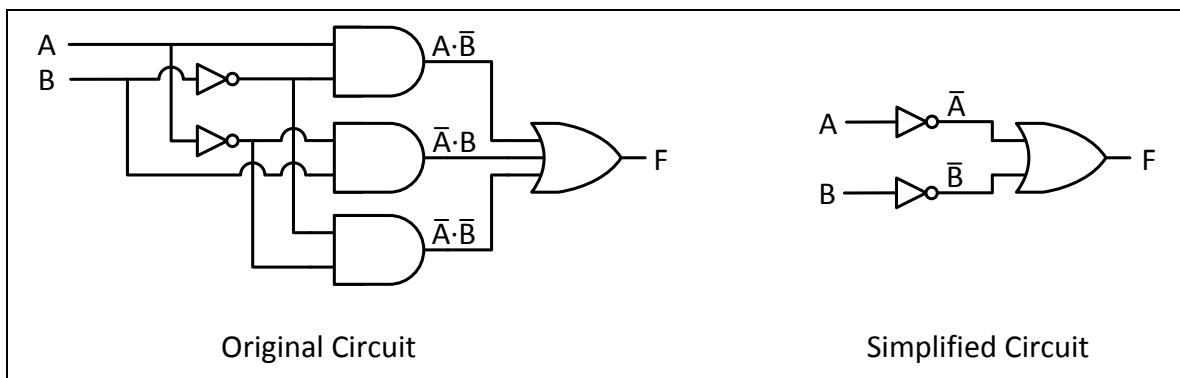
using identity 10

$$F = A \cdot \bar{B} + \bar{A}$$

since $B + \bar{B} = 1$ (identity 8)

$$F = \bar{A} + \bar{B}$$

since $\bar{A} + A \cdot \bar{B} = \bar{A} + \bar{B}$ (identity 11)



The original circuit requires two NOT, three 2-input AND and a 3-input OR gate. The simplified version requires two NOT gates and a 2-input OR gate.

Note that this can be further reduced to a single 2-input NAND gate by $\overline{A \cdot B} = \overline{A} + \overline{B}$ using the second of DeMorgan's theorems:

2. A circuit is required to produce an output function $F: F = (\overline{A} + \overline{B}) \cdot (\overline{\overline{A}} + B) \cdot (\overline{\overline{A}} + \overline{B})$

Show the circuit required and devise a simplified circuit.

$$F = (\overline{A} + \overline{B}) \cdot (\overline{\overline{A}} + B) \cdot (\overline{\overline{A}} + \overline{B})$$

$$F = [A(\overline{A} + B) + \overline{B}(\overline{A} + B)] \cdot (\overline{\overline{A}} + \overline{B}) \quad (\text{identity 12})$$

$$F = (A \cdot \overline{A} + A \cdot B + \overline{A} \cdot \overline{B} + \overline{B} \cdot B) \cdot (\overline{\overline{A}} + \overline{B}) \quad (\text{identity 10})$$

$$F = A \cdot B \cdot (\overline{A} + \overline{B}) + \overline{A} \cdot \overline{B} \cdot (\overline{A} + \overline{B}) \quad (\text{identity 12})$$

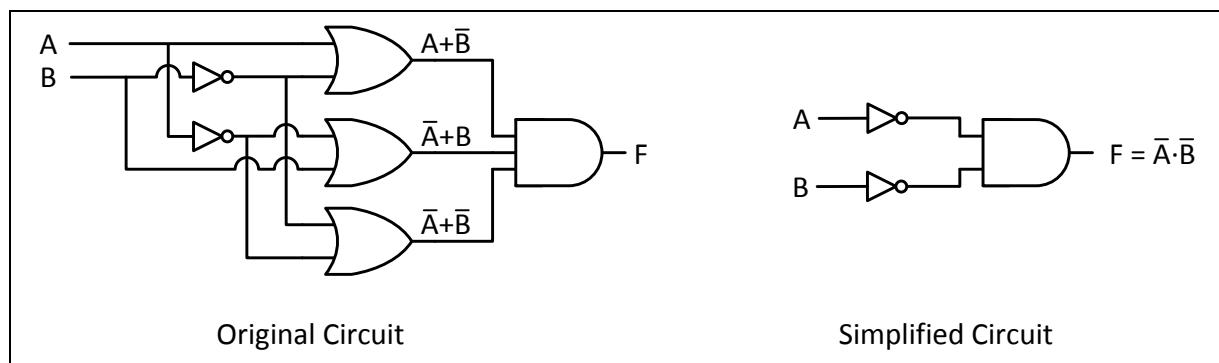
$$F = (A \cdot B + \overline{A} \cdot \overline{B}) \cdot (\overline{A} + \overline{B}) \quad \text{since } A \cdot \overline{A} \& B \cdot \overline{B} = 0 \text{ (identity 4)}$$

$$F = A \cdot \overline{A} \cdot B + A \cdot B \cdot \overline{B} + \overline{A} \cdot \overline{A} \cdot \overline{B} + \overline{A} \cdot \overline{B} \cdot \overline{B} \quad (\text{identity 10})$$

$$F = \overline{A} \cdot \overline{A} \cdot \overline{B} + \overline{A} \cdot \overline{B} \cdot \overline{B} \quad \text{since } A \cdot \overline{A} = 0 \& B \cdot \overline{B} = 0 \text{ (identity 4)}$$

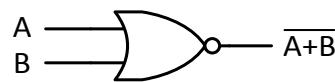
$$F = \overline{A} \cdot \overline{B} + \overline{A} \cdot \overline{B} \quad \text{since } \overline{A} \cdot \overline{A} = \overline{A} \& \overline{B} \cdot \overline{B} = \overline{B} \text{ (identity 1)}$$

$$F = \overline{A} \cdot \overline{B} \quad (\text{identity 5})$$



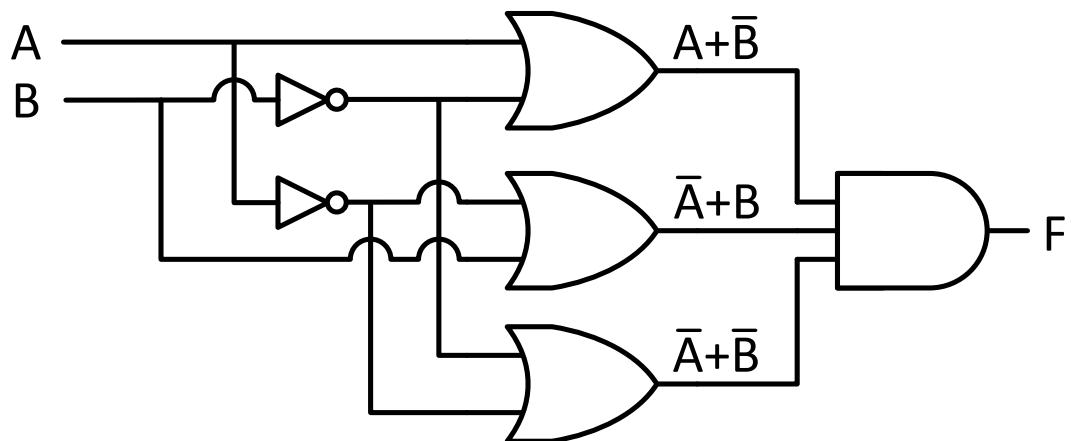
Note that using the first of DeMorgan's theorems can again further reduce the number of gates: $\overline{A + B} = \overline{A} \cdot \overline{B}$

So we can write $F = A + B$ which is the function of a single NOR gate:



Further Simplification

Exercise 2: Equivalent Logic Circuits



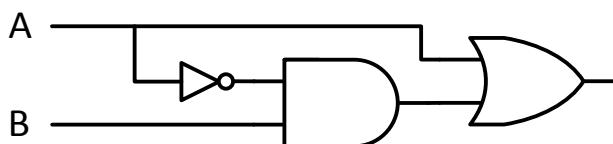
Objectives:

- Derive gate function from a Boolean expression.
 - Make measurements on logic circuits to determine the equivalence of logic expressions.
 - Appreciate the important functions of logic gates through practical applications and troubleshooting
 - To test and identify the output of the circuit.

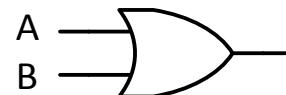
Equipment:

No	Name	Qty.
1.	Breadboard	1 Pc
2.	Set of IC's	-
3.	LED Logic Probe	1 Pc
4.	Multimeter	1 Pc

Circuit Diagram:



(a)



(b)

Procedure:

1. Based on the given circuit diagram, what IC(s) are needed in order to connect the said diagram?

.....
.....
.....

2. Construct the given diagram (a) and (b) on a breadboard. The internal connections of the ICs can be found in Appendix 1 at the end of the book.
 3. Apply the input voltage levels shown in the truth tables shown below and note down the outputs.

Inputs		Output
A	B	
0	0	
0	1	
1	0	
1	1	

Circuit (a)

Inputs		Output
A	B	
0	0	
0	1	
1	0	
1	1	

Circuit (b)

4. Write down your comment regarding the results.

.....

.....

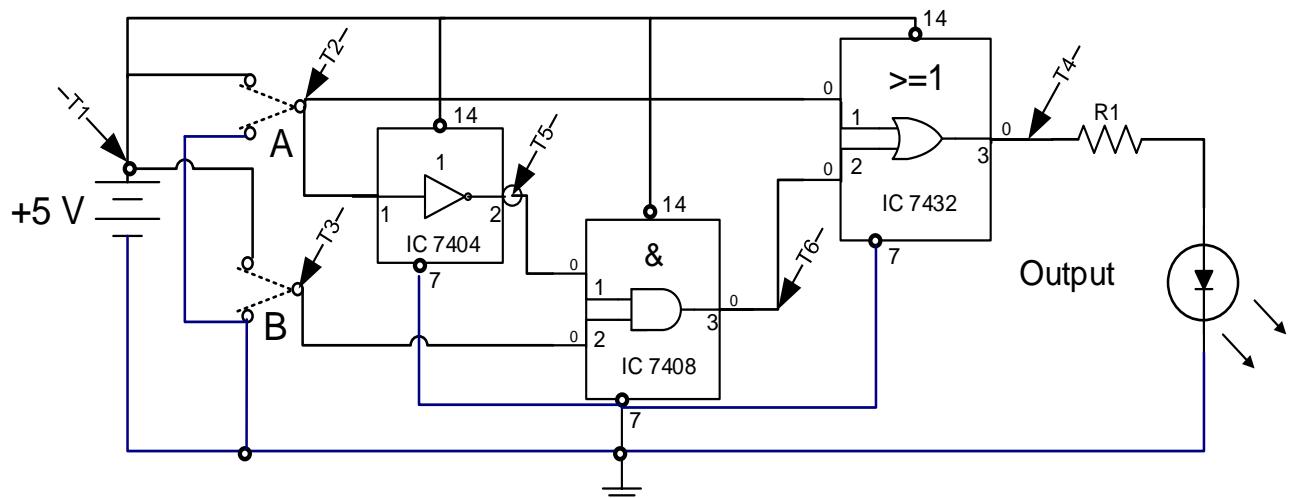
.....

5. Write down the logic expression of diagram 'a' and diagram 'b':

.....

.....

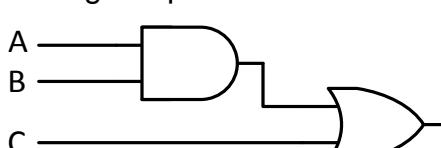
6. Measure and write down all voltages of the test points shown in the figure below:



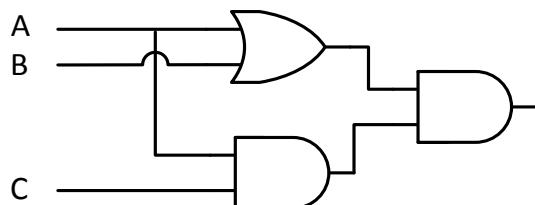
Wiring Diagram and Test Points for troubleshooting

Condition of Switch 1 = up 0 = down			Voltages from multimeter					
			T1 (Source)	T2 (Input A)	T3 (Input B)	T4 (OR Output)	T5 (NOT Output)	T6 (AND Output)
For Diagram “a”	0	0						
	0	1						
	1	0						
	1	1						

Review Questions:

- The logic gate producing an output $A \cdot B$ is:
 - AND
 - OR
 - NAND
 - NOR
- The logic gate producing an output $A + B$ is:
 - AND
 - OR
 - NAND
 - NOR
- The logic gate producing an output $A \cdot B + \bar{A} \cdot \bar{B}$ is :
 - AND
 - EXOR
 - NAND
 - EXNOR
- The logic expression for the circuit shown is:
 
 - $(A+B) \cdot C$
 - $A+B \cdot C$
 - $A \cdot B + C$
 - $A \cdot (B+C)$

- The logic expression for the circuit shown is:



- $A+B+A \cdot C$
- $A \cdot B+(A+C)$
- $A+B \cdot A \cdot C$
- $(A+B) \cdot A \cdot C$

Circuit Simplification Using a Karnaugh Map

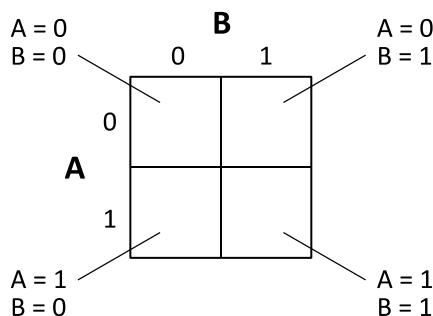
In the previous lesson, we saw how Boolean algebra could be used to reduce a logic expression to its simplest form.

Another popular technique that can be used to simplify a logic function is to use a **Karnaugh map**. This is similar in many respects to a truth table, except that the variables are represented along two axes instead of one.

Each combination of inputs has its own square within the map. A function with two input variables (A,B) would therefore require a map of 4 squares, while the map for a function with three input variables (A,B,C) would contain 8 squares.

Two-Variable Karnaugh Map

The Karnaugh map below is for a function with two input variables:

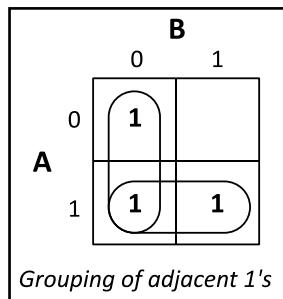
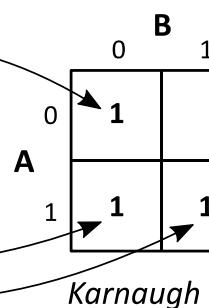


Note that the top left-hand square corresponds to the input combination A=0, B=0, and that only one input bit changes when you move from one square to the next.

We will now create a Karnaugh map based on the truth table shown below. The first step is to place a '1' in each square of the Karnaugh map where the input combination results in logic 1 output. This is illustrated below:

Inputs		Output
A	B	
0	0	1
0	1	0
1	0	1
1	1	1

Truth Table



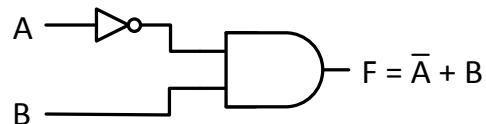
The next step is to identify groups of two adjacent 1's (also groups of four 1's or eight 1's in larger maps) by circling them. Each circled group will represent a new term in the simplified Boolean expression.

In our example we have two groups, so there will be two ORed terms in our simplified expression.

For the horizontal group at the bottom of the map, A is always 1, whatever the value of B. For the vertical group on the left of the map, B is always 0, irrespective of the value of A. The resulting terms are A and B respectively, so the simplified expression is:

$$F = \bar{A} + B$$

which could be implemented using the gate arrangement shown on the right:



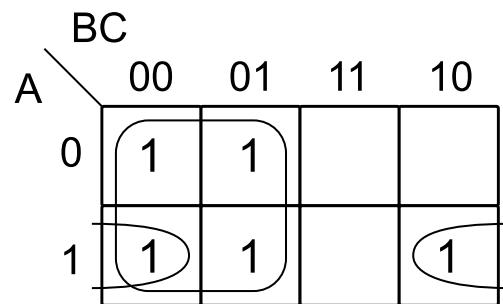
Simplified Gate Arrangement

Three-Variable Karnaugh map

Below is an example of a Karnaugh map for a three-variable logic function. The truth table from which it was derived is shown alongside it.

Inputs			Output
A	B	C	
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Truth Table

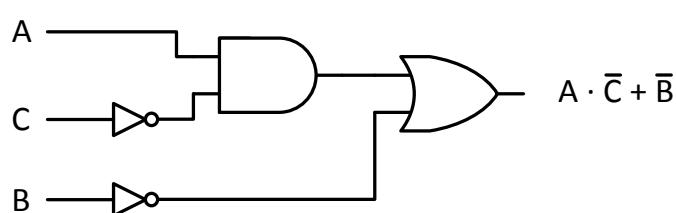


Karnaugh Map

Note that the axes of the Karnaugh map are once again arranged so that only one input bit changes between adjacent squares (this is why the column headings are in the sequence 00, 01, 11, 10). Also, as this example shows, you can treat the left and right edges of the map as being joined (hence the circle around the bottom left and bottom right squares). The top and bottom edges of the map may be considered to be connected together in a similar way.

The simplified logic expression is therefore:

$$F = A \cdot \bar{C} + \bar{B}$$



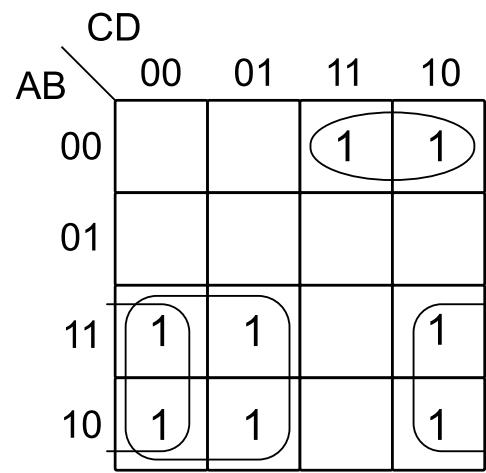
Four-Variable Karnaugh Map

The same rules apply for a four-variable Karnaugh map. When working with a lot of digital design circuits, it helps to make a short notation that describes the truth table. The table below can also be written as:

$$Q(A, B, C, D) = \sum m(2, 3, 8, 9, 10, 12, 13, 14)$$

where m refers to the minterms or product terms in which the output is 1.

Inputs				Output
A	B	C	D	
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

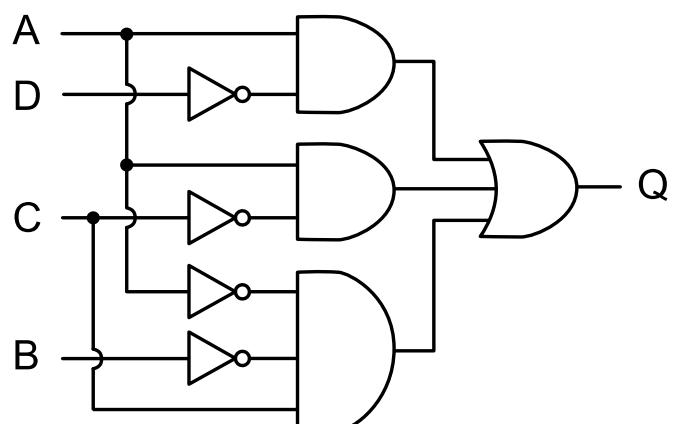


Truth Table

The simplified logic expression becomes:

$$Q = A\bar{C} + A\bar{D} + \bar{A}\bar{B}C$$

And the resulting circuit is shown on the right.



Summary of Karnaugh Map Rules

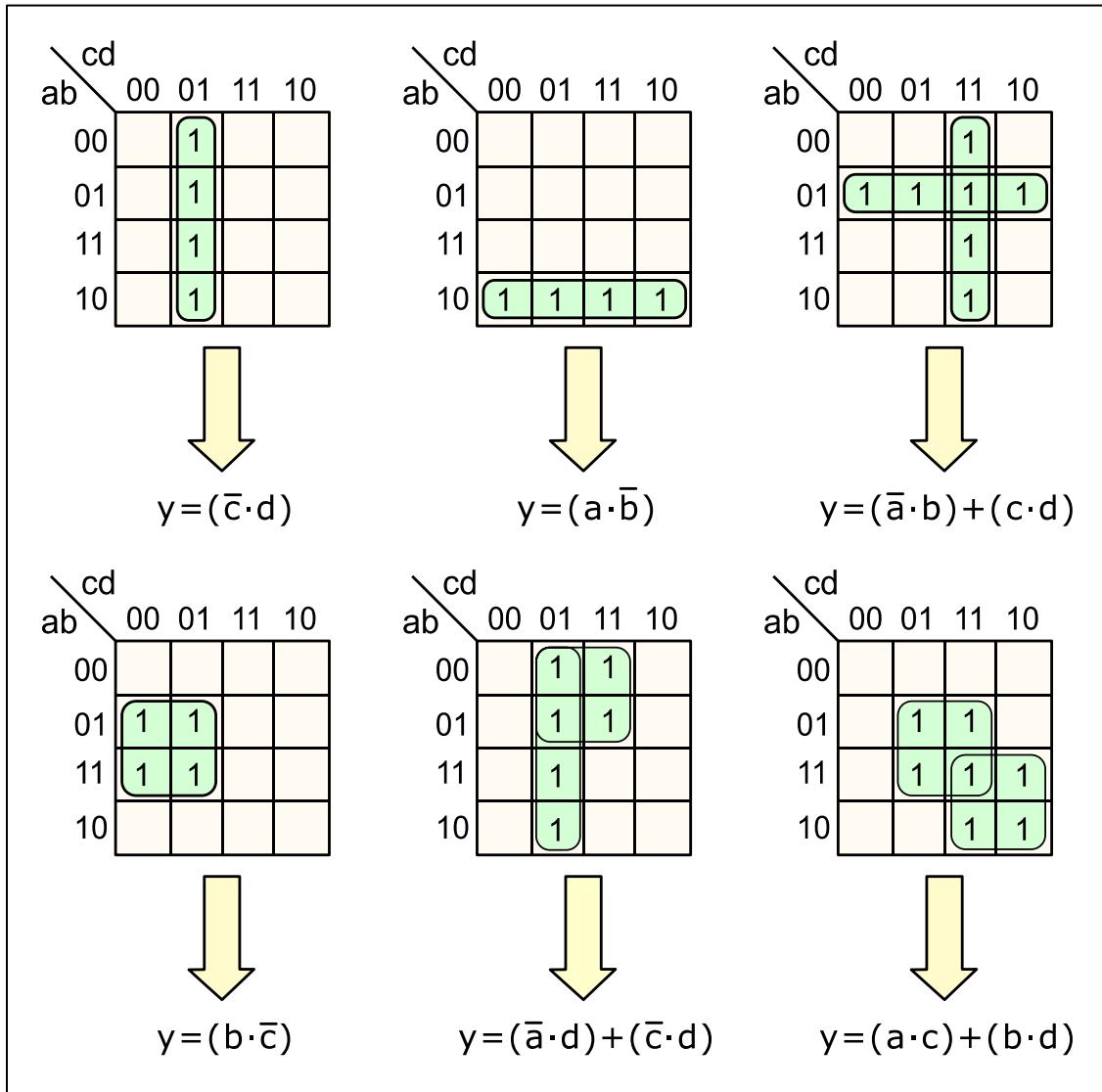
- Groups may not include any cell containing a zero
- Groups may be horizontal or vertical, but not diagonal
- Groups must contain 1, 2, 4, 8, or in general 2^n cells
- Each group should be as large as possible
- Each cell containing a one must be in at least one group
- Groups may overlap
- Groups may wrap around the table
- There should be as few groups as possible, as long as this does not contradict any of the previous rules

Review Questions:

Build the circuits described in these equations. Start by writing down the truth table and Karnaugh map. Then determine the simplified logic expression and draw the circuits:

1. $Q(A, B, C) = \sum m(0, 1, 3)$
2. $Q(X, Y, Z) = \sum m(0, 2, 3, 5)$
3. $F(A, B, C, D) = \sum m(0, 2, 6, 8, 12, 14)$

Exercise 3: Verification of Karnaugh Maps



Objectives:

- Derive a Karnaugh Map from a truth table
- Deduce the logic functions represented by two- and three-variable Karnaugh maps.
- Verify by observation the simplified logic functions derived from two- and three-variable Karnaugh maps.
- Troubleshoot the equivalent circuit.

Equipment:

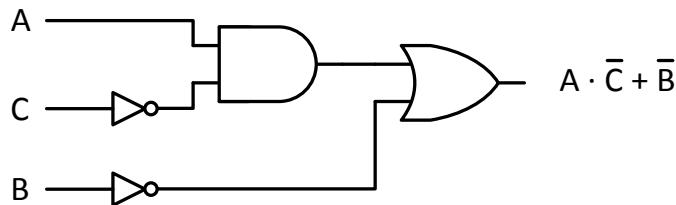
No	Name	Qty.
1.	Breadboard	1 Pc
2.	7404 NOT gates IC	1 Pc
3.	7408 AND gates IC	1 Pc
4.	7432 OR Gates IC	1 Pc
5.	LED Logic Probe	1 Pc
6.	Multimeter	1 Pc

Circuit Diagram:

Circuit 1:



Circuit 2:



Procedure:

1. Connect circuit 1 as shown above

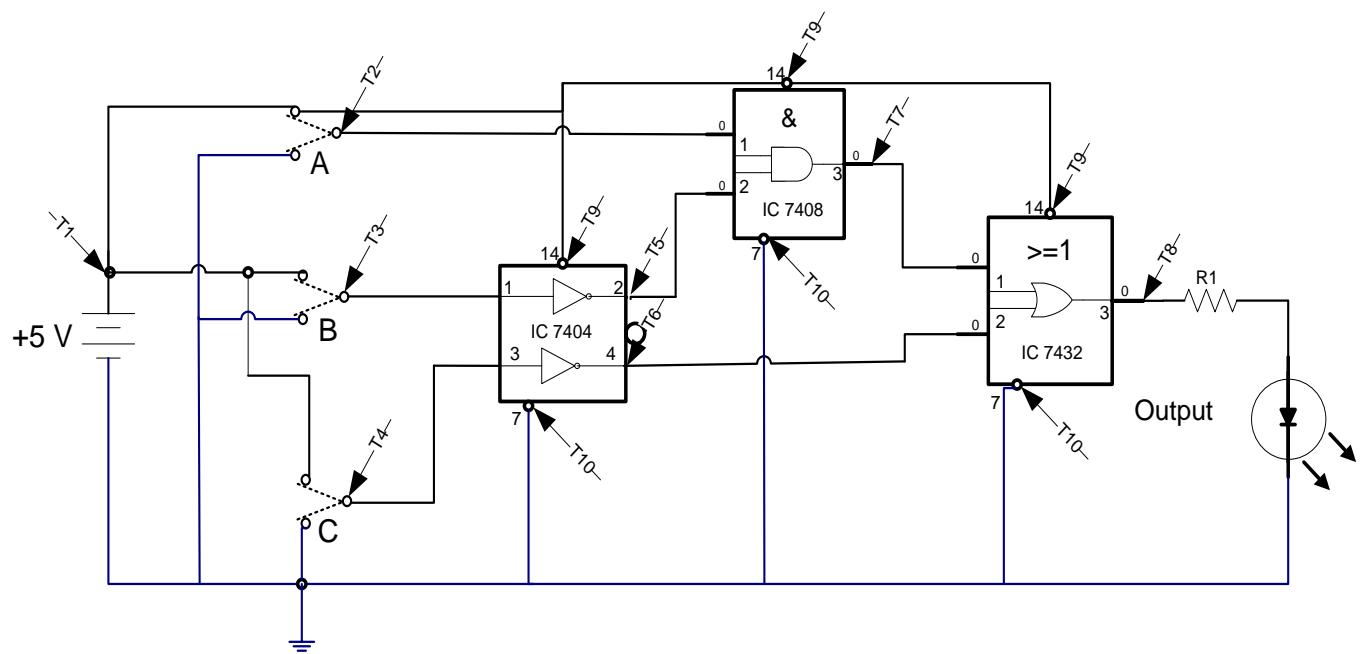
Inputs		Output
A	B	
0	0	
0	1	
1	0	
1	1	

2. Complete the truth table on the right and compare the results with the solution from the previous lesson (the two-variable Karnaugh map). Write down your observations
-
.....

3. Build circuit 2 on a breadboard and complete the truth table below. Compare the results with the solution in the previous lesson of a 3-variable Karnaugh map.

Inputs			Output
A	B	C	
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

4. Write down all voltage measurements of the test points shown in the figure below:

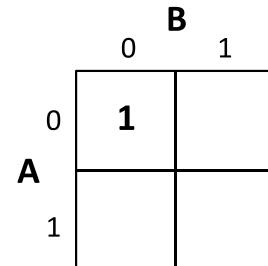


Wiring Diagram and Test Points for troubleshooting

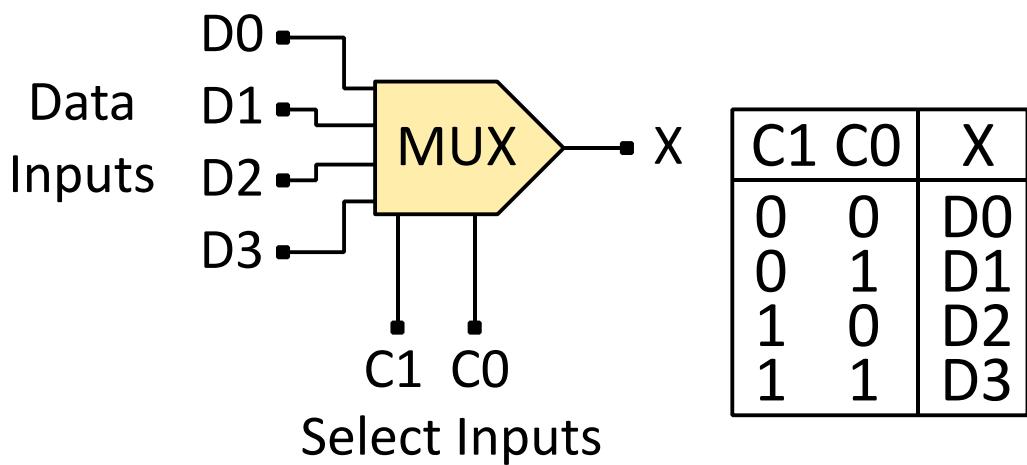
Condition of Switch 1 = up 0 = down			Voltages from multimeter										
Base from Circuit 2	A	B	C	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10
	0	0	0										
	0	0	1										
	0	1	0										
	0	1	1										
	1	0	0										
	1	0	1										
	1	1	0										
	1	1	1										

Review Questions:

1. A three-Variable Karnaugh map contains:
 - a. Two squares.
 - b. Eight squares.
 - c. Four squares.
 - d. Sixteen squares.
2. If a four-Variable Karnaugh map is given, it contains:
 - a. Two squares.
 - b. Eight squares.
 - c. Four squares.
 - d. Sixteen squares.
3. The top and left-hand edges of a Karnaugh map can be considered as being connected to:
 - a. the left-hand and right-hand edges respectively.
 - b. the left-hand and bottom edges respectively.
 - c. the bottom and right-hand edges respectively.
 - d. each other.
4. The Karnaugh map shown represents the function of:
 - a. a NAND gate.
 - b. a NOR gate.
 - c. an OR gate.
 - d. an EXOR gate.



Exercise 4: Multiplexer

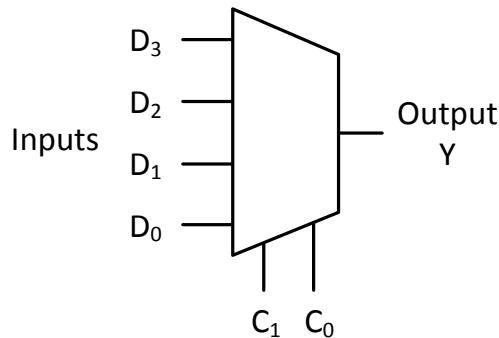


Objectives:

- To understand the logic states for multiplexer circuits.
- Relate inputs to outputs for multiplexer circuits.
- Diagnose faults in multiplexer circuits.

Discussion:

A multiplexer is a circuit designed to switch one of several input lines through to a single common output line by the application of a control signal.



Control		Inputs				Output
C ₁	C ₀	D ₃	D ₂	D ₁	D ₀	Y
0	0	1	0	0	1	1
0	1	1	0	0	1	0
1	0	1	0	0	1	0
1	1	1	0	0	1	1

Figure 1

Figure 1 shows a block diagram of a 4-input multiplexer and its truth table for the input state D₃, D₂, D₁, D₀ = 1,0,0,1.

With the control setting C₁, C₀ = 0, 1 (decimal 1) the logic state at input D₁ is fed to the output, that is, logic 0.

Similarly, for control settings C₁, C₀ = 1, 0 & 1, 1 the outputs are 0 & 1 as shown.

Applications:

The multiplexer can be used whenever a choice needs to be made between several output signals. A simple example is when multiple audio signals are to be connected to one sound system (see Figure 2). A rotary switch can be built so that it switches between the different cases on the select inputs. And if the signal to be delivered consists of more than one wire, a multiplexer is needed for each one of the wires.

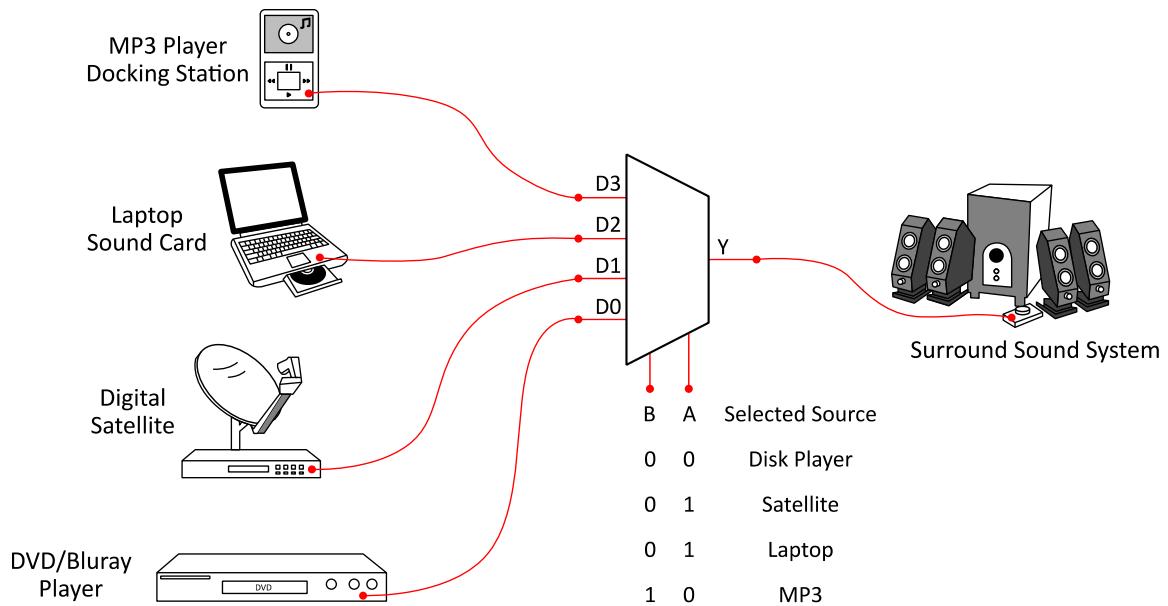
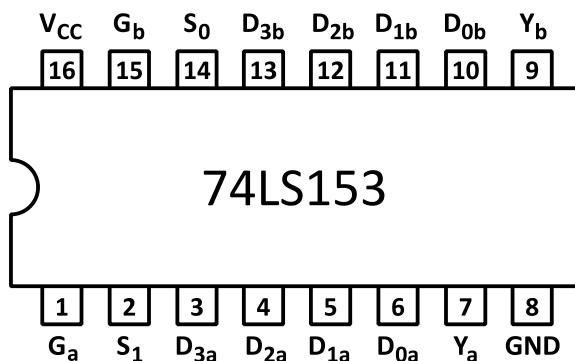


Figure 2: Multiplexing Several Audio Signals to One Sound System

Pin Layout



Function Table

Select Inputs		Data Inputs				Strobe	Output
S ₁	S ₀	D ₀	D ₁	D ₂	D ₃	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs S₁ and S₀ are common to both sections

H = HIGH Level

L = LOW Level

X = Don't Care

Figure 3: Connection Diagram & Function Table of Dual 4-1 Multiplexer 74153

Circuit Diagram:

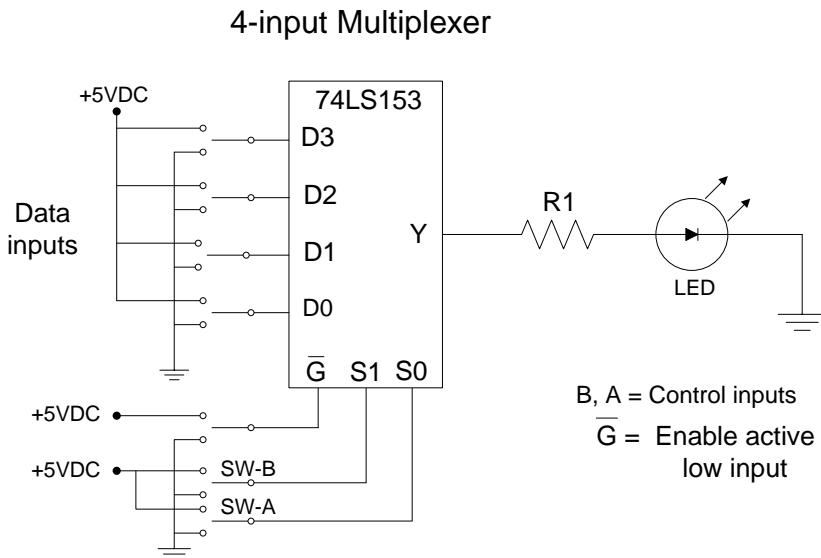


Figure 4

Equipment:

No	Name	Qty.
1.	Breadboard	1 Pc
2.	Multiplexer IC 74LS153	1 Pc
3.	SPDT switch	7 Pcs.
4.	LED	1 Pc
5.	Resistor (250Ω)	1 Pc

Procedure:

1. Assemble the circuit as shown in Figure 4.
2. With the bread board power supply ON, set the input G to logic 0 and set the control input (S1=0, S1=0).
3. Set D0 and D3 to logic 0, note the output logic level. Record the value in Table 1.
4. Set D0 to logic 1 and note the output logic level. Record the value in Table 1.

5. Set D1 - D3 momentarily to logic 1 and note the output state. There will be no change of output since only the input D0 is connected to the output for the control setting of zero.
6. Now set the control and inputs D0-D3 as indicated in Table 1, noting the output logic state for each combination of settings. Record the values in the table.

Control		Inputs				O/P
S1	S0	D3	D2	D1	D0	Y
0	0	0	0	0	0	
0	0	0	0	0	1	
0	1	0	0	0	0	
0	1	0	0	1	0	
1	0	0	0	0	0	
1	0	0	1	0	0	
1	1	0	0	0	0	
1	1	1	0	0	0	

Table 1

With the control and input settings as for the last set of readings in Table 1, set input G to logic 1 and note the effect on the output. You should note that the output changes from logic 1 to logic 0. The input G is an output gate enable input, the bar indicating that the input is active in the low (logic 0) state.

Troubleshooting:

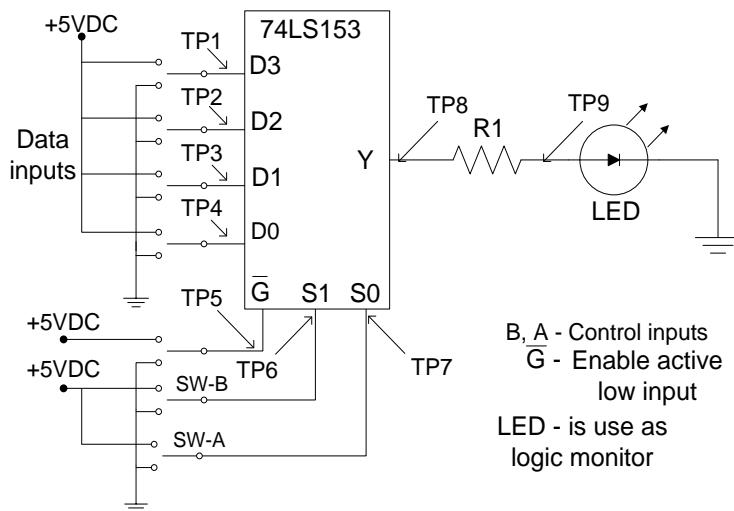


Figure 5: Simplified Circuit Diagram and Test Points of 4-input Multiplexer

Procedure:

With the bread board power supply ON:

1. Set the control and inputs settings (please refer to Table 1). Initiate faults, and verify the voltages in every test points.
2. With the logic 1, the voltage reading must be +5VDC and with the logic 0, the voltage reading must be 0 volt.
3. If not, check the SPDT switches and connecting leads for possible loose wiring connections. Perform circuit continuity test if necessary.
4. Record the results in the table provided below.

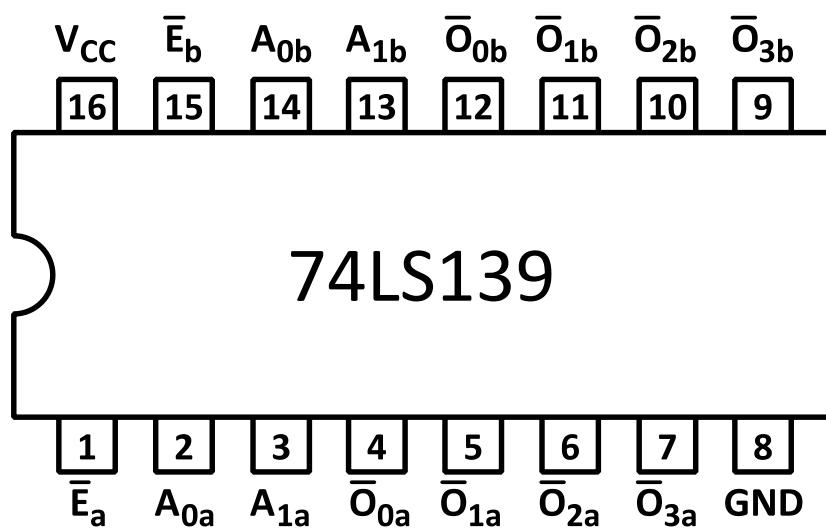
Test Points	Voltage Readings	
	Normal Condition	Fault Condition
TP1		
TP2		
TP3		
TP4		
TP5		
TP6		
TP7		
TP8		
TP9		

Table 2

Review Questions:

1. What is a multiplexer circuit?
2. Draw the sample block diagram of a 4 input multiplexer and its truth table.
3. A 4-input multiplexer has inputs D3, D2, D1, D0 set 1,1,0,0 and its output is logic 0. The possible control settings C1, C0 are:
 - a) 0,0 or 1,0
 - b) 0,1 or 1,0
 - c) 0,0 or 0,1
 - d) 0,1 or 1,1

Exercise 5: Demultiplexer



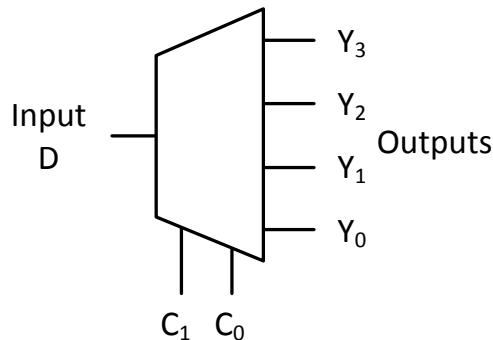
Objectives:

- Understand the logic states for Demultiplexer circuits.
- Relate inputs to outputs for Demultiplexer circuits.
- Diagnose faults in Demultiplexer circuits.

Discussion:

A demultiplexer is a circuit designed to switch one input line through to several output lines by the application of a control signal.

Figure 6 shows a block diagram of a one input to one of four output lines demultiplexer and its truth table for the input states shown. Only one output line is selected at any time, this depending on the control setting, and the data on the selected output data line corresponds with the data at the input at that time. All the unselected output lines are shown as logic level 1, that is they have floated up to logic 1.



Control		Input	Output			
C ₁	C ₀	D	Y ₃	Y ₂	Y ₁	Y ₀
0	0	1	1	1	1	1
0	1	0	1	1	0	1
1	0	0	1	0	1	1
1	1	1	1	1	1	1

Figure 6

For example, for control setting C₁, C₀ = 0,0, output line Y₀ is selected to be fed with data at the input, that is, logic 1. The other outputs have floated up to logic1. Similarly, for control setting C₁, C₀ = 0,1, the output line Y₁ is selected to be fed with data at the input, that is, logic 0. The other outputs are at logic level 1.

The pin layout of a 1-4 demultiplexer integrated circuit is shown in Figure 7.

Logic Diagram:

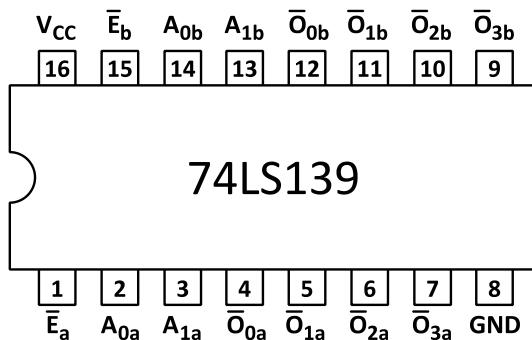


Figure 7: Dual 1-of-4 decoder/Demultiplexer 74LS139

Circuit Diagram:

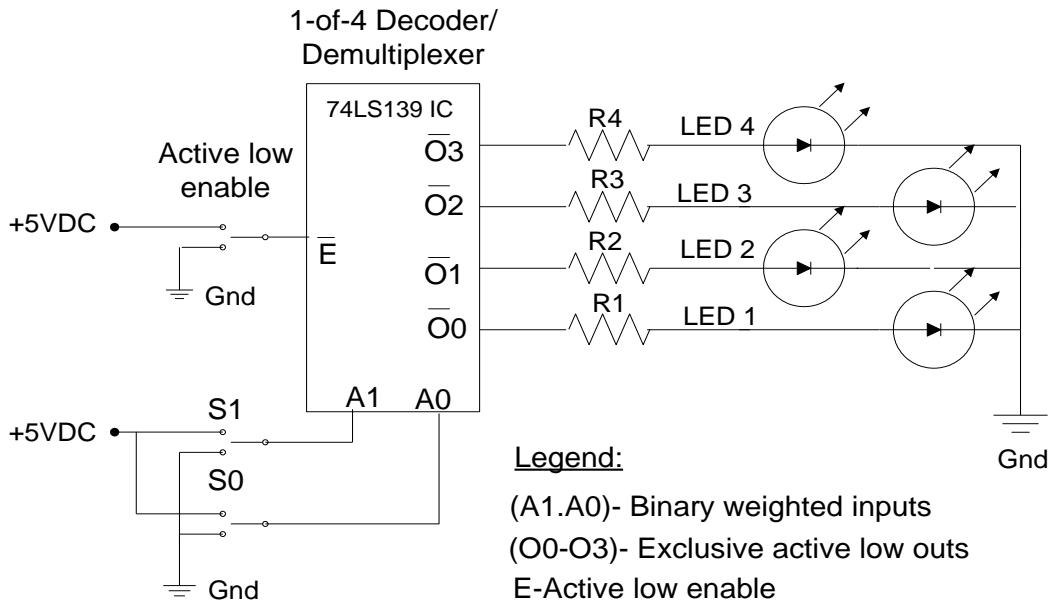


Figure 8: 1 of 4 Decoder/ Demultiplexer

Equipment:

No	Name	Qty.
1.	Breadboard	1 Pc
2.	Demultiplexer IC 74LS139	1 Pc
3.	SPDT switch	3 Pc
4.	LED	4 Pc
5.	Resistor (250Ω)	4 Pc
6.	Multimeter	1 Pc

Procedure:

1. Assemble the circuit as shown in Figure 8.
2. With breadboard power supply ON, set input \overline{E} to logic 0 and set the control inputs ($A_1=0$, $A_0=0$). Note the logic level of each output line and record the values in the first row of Table 3.
3. Set input \overline{E} to logic 1, note the logic level of the outputs and record the values in the second row of Table 3.
4. Now set the control inputs and input \overline{E} as indicated in each of the remaining rows of Table 3, record the logic state of all outputs for each combination of settings.

Control		I/P	Outputs			
A1	A0	\overline{E}	\overline{O}_3	\overline{O}_2	\overline{O}_1	\overline{O}_0
0	0	0				
0	0	1				
0	1	0				
0	1	1				
1	0	0				
1	0	1				
1	1	0				
1	1	1				

Table 3

Trouble shooting:

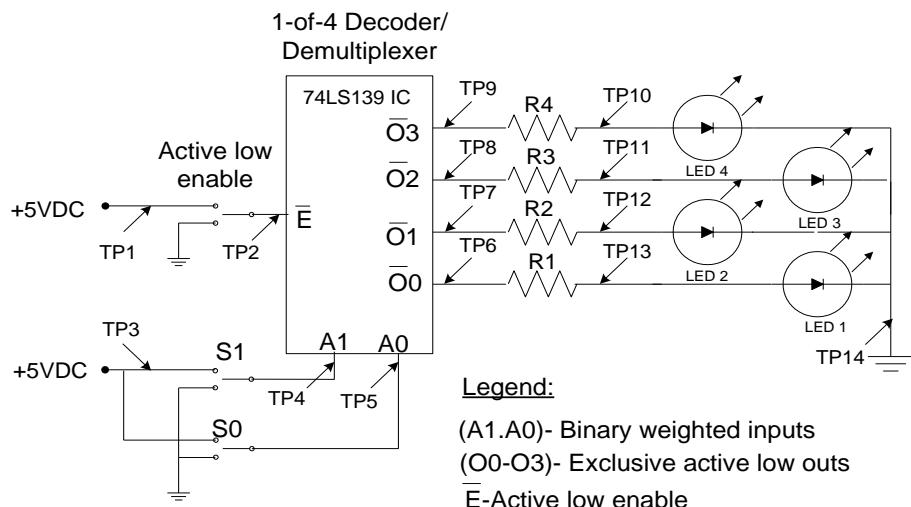


Figure 9: Simplified circuit diagram and test points (TP)

Procedure:

1. With the bread board power supplies on, use the multimeter and perform voltage check in every test points, as shown in Figure 9.
2. Set the control and inputs settings base on the Table 3. At logic 1 the volt meter must read 5VDC and at logic 0 the volt meter must read zero volts. If not, check the connecting leads and SPDT switches for possible loose wiring connection.
3. Record the voltage readings in the Table 4 below.

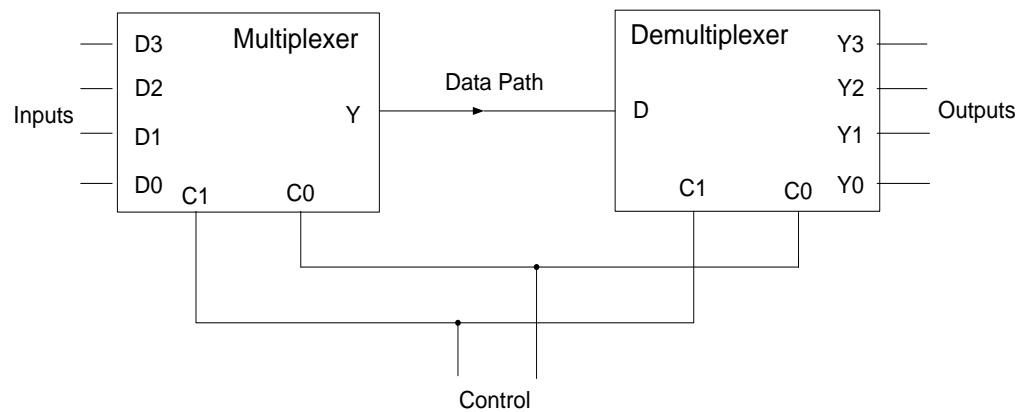
	TP1	TP2	TP3	TP4	TP5	TP6	TP7	TP8	TP9	TP 10	TP 11	TP 12	TP 13	TP 14
Normal Condition														
Fault Condition														

Table 4

Review Questions:

1. What is a Demultiplexer circuit?
 2. Draw the sample block diagram of a 1-input to 1 of 4 output lines demultiplexer and its truth table.
 3. A demultiplexer has outputs Y3, Y2, Y1, and Y0 at levels 0,1,0,0. The input, I/P, and control settings, C1, C0, active high, are:
 - a) I/P=0, C1,C0=0,1
 - b) I/P=0, C1,C0=1,0
 - c) I/P=1 C1,C0=0,1
 - d) I/P=1, C1,C0=1,0

Exercise 6: Multiplexer/Demultiplexer



Objectives:

- Understand the logic states for Multiplexer/ Demultiplexer circuits.
- Relate inputs to outputs for Multiplexer/ Demultiplexer as one circuit.
- Diagnose faults in Multiplexer/ Demultiplexer circuits.

Discussion:

Figure 10 shows a multiplexer and demultiplexer interconnected to form a communication system between two locations, the data being transmitted in digital form with the digits being transmitted one at a time in sequence. This method of transmission is referred to as serial and requires only one data line irrespective of the number of input data lines in the system.

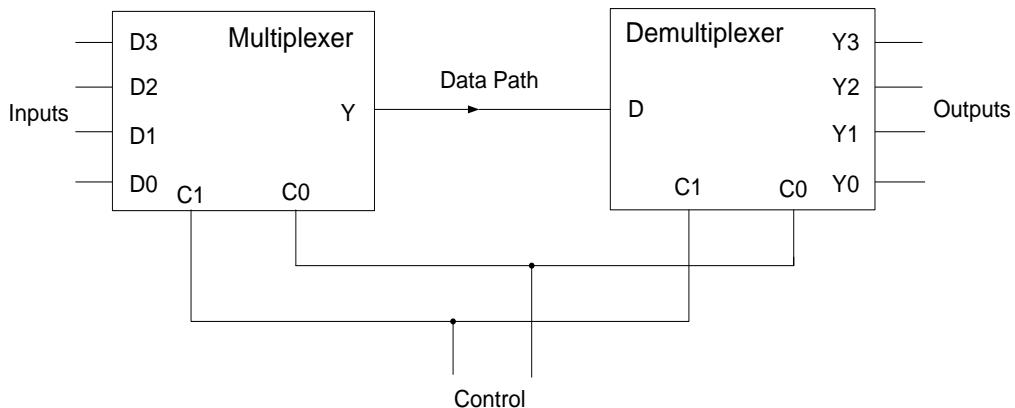


Figure 10

With the control input set to 0, the data at input D0 is fed to output Y0.
With the control input set to 1, the data at input D1 is fed to output Y1.
With the control input set to 2, the data at input D2 is fed to output Y2.
With the control input set to 3, the data at input D3 is fed to output Y3.

At each setting of the control input, a sequence of coded digital data can be transferred between the two locations, and hence the system represents a multi-channel communication system with the number of channels equal to the number of inputs.

A system where all the data inputs are transferred simultaneously is referred to as a parallel system. This system requires a number of data lines equal to the number of inputs. The serial system is therefore more economical, particularly for the larger number of input lines.

Circuit Diagram:

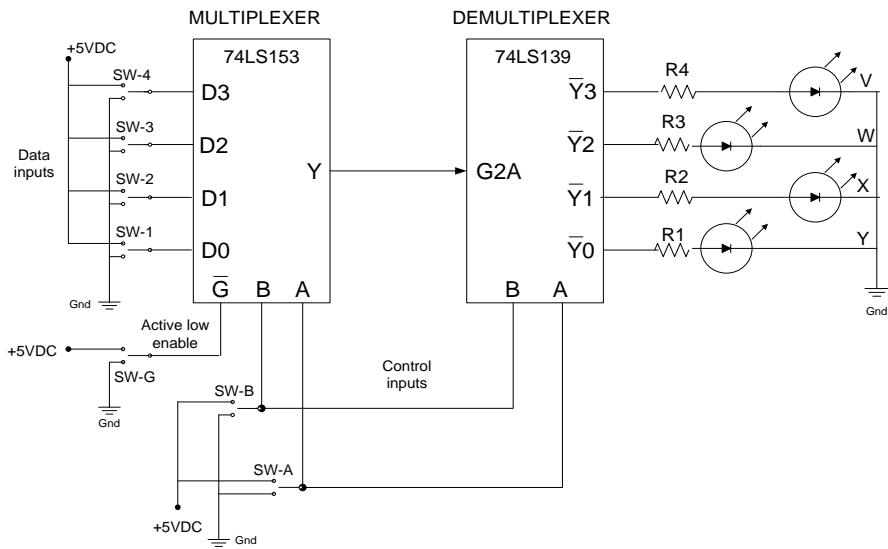


Figure 11: Simplified Multiplexer/Demultiplexer Circuits using 74LS153/74LS139

Equipment:

No.	Name	Qty.
1	Breadboard	1pc.
2	Multiplexer IC 74LS153	1pc.
3	Demultiplexer IC 74LS139	1pc.
4	SPDT switch	7 pcs.
5	LED	4 pcs.
6	Resistor (250Ω)	4 pcs.

Procedure:

1. Assemble the circuit as shown in the circuit diagram Figure 11.
2. With the breadboard power supply ON, set G to logic 0 and set B, A to zero.
3. Set the inputs D3, D2, D1, D0 to 1001, note the logic levels of the outputs again and record these values in Table 5.
4. Now set the control inputs B, A to 1, 0, and 1, 1 as indicated in Table 5, noting the logic states of all outputs for each combination of settings. Record the values in Table 5.
5. Repeat the procedure with the inputs D3, D2, D1, D0 set to 0110.

Inputs				Control		Outputs			
D3	D2	D1	D0	B	A	\bar{Y}_3	\bar{Y}_2	\bar{Y}_1	\bar{Y}_0
1	0	0	1	0	0				
1	0	0	1	0	1				
1	0	0	1	1	0				
1	0	0	1	1	1				
0	1	1	0	0	0				
0	1	1	0	0	1				
0	1	1	0	1	0				
0	1	1	0	1	1				

Table 5

Note from your readings that the active lines corresponds with the decimal value of the control binary inputs, the data on the input active line is then being transferred to the output active line. All inactive lines are at logic 1.

For example, with B, A set 0,0 (Decimal 0), the data on D0 is transferred to \bar{Y}_0 .

Trouble Shooting:

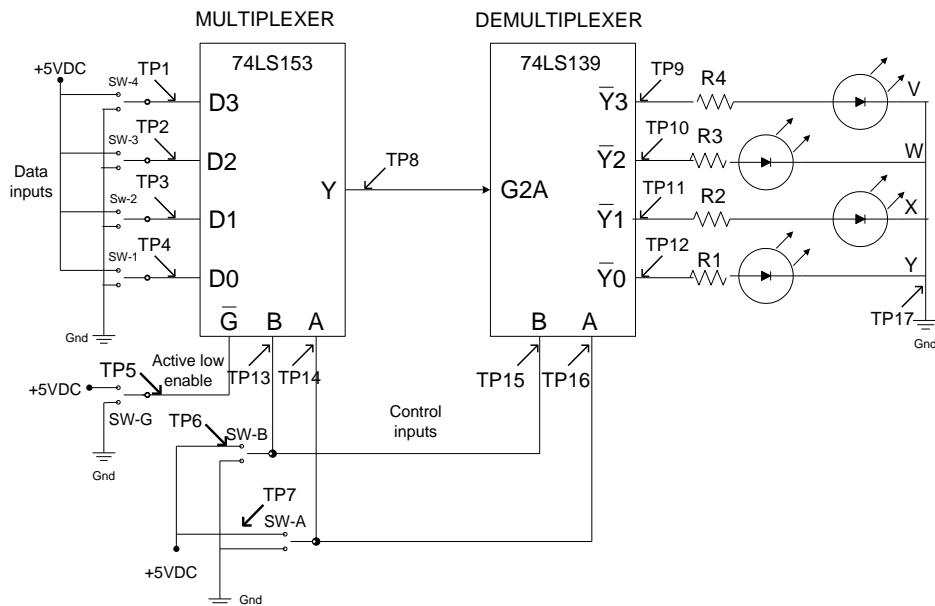


Figure 12: Multiplexer/Demultiplexer Circuit and Test Points (TP)

Procedure:

1. With the bread board power supply on, use the multimeter and perform voltage check in every test points as shown in Figure 12.
2. Set the control and inputs settings base on the Table 5. At logic 1 the volt meter must read 5VDC and at logic 0 the volt meter must read zero volts. If not, check the connecting leads and SPDT switches for possible lose wiring connection.
3. Record the results in the Table 6 below.

Test Points	Voltage Reading:		Test Points	Voltage Reading	
	Normal Condition	Fault Condition		Normal Condition	Fault Condition
TP1			TP7		
TP2			TP8		
TP3			TP9		
TP4			TP10		
TP5			TP11		
TP6			TP12		

Table 6

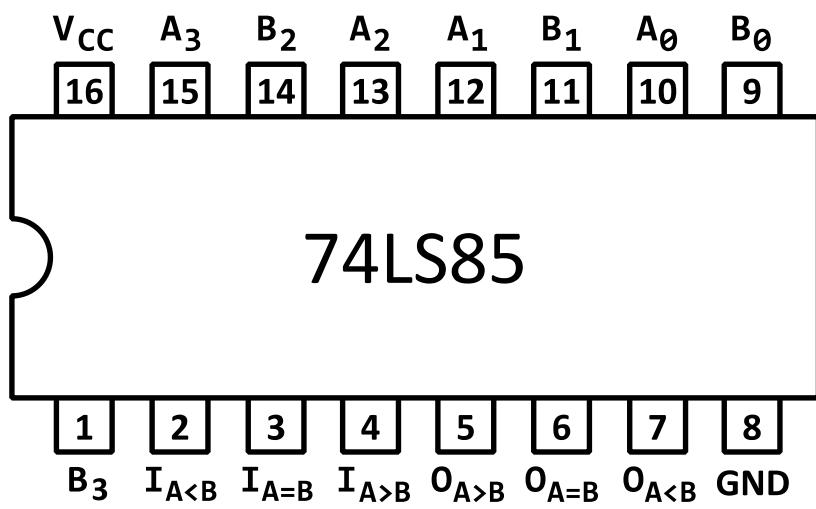
Review Question:

1. What is the characteristic of Multiplexer/Demultiplexer circuit?

2. The multiplexer/Demultiplexer circuit used in this exercise has inputs D3, D2, D1, D0 set 1,0,1,0 and control input setting B,A = 0,1. Output states Y3, Y2, Y1, Y0 are:

- a. a) 1,1,1,0 b) 1,1,0,1 c) 1,0,1,1 d) 1,1,1,1

Exercise 7: Magnitude Comparator Circuits



SN54/74LS85

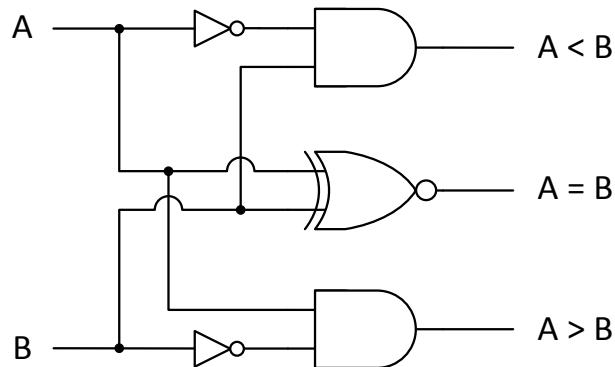
Objectives:

- Determine from observation the logic states for magnitude comparator circuits.
- Relate inputs to outputs for a 2-input magnitude comparator.
- Diagnose faults in magnitude comparator circuits.

Discussion:

Magnitude comparator circuits compare two input values (A and B) and normally give outputs indicating whether $A=B$, or if $A > B$ or $A < B$.

A circuit and the truth table for a single digit magnitude comparator using AND, Not and EX-NOR gates is shown in Figure 13.



Inputs		Outputs		
A	B	A < B	A = B	A > B
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

Figure 13

In this exercise, we will create a 2-bit comparator circuit that only deals with the case when the two input numbers are equal or not.

Circuit Diagram:

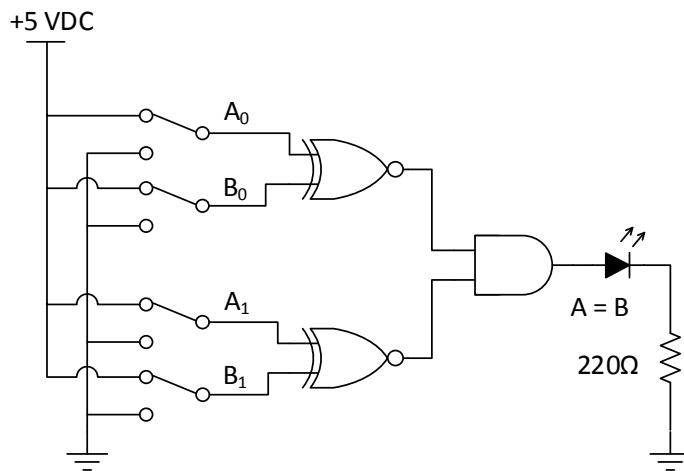


Figure 14: Two-bit Equal Input Magnitude Comparator Circuit

Equipment:

No	Name	Qty
1	Breadboard	1 pc
2	XNOR Gate 74LS266 IC	1 pc
3	AND Gate 74LS08 IC	1 pc
4	LED (use as indication)	3 pc
5	Resistors 220Ω	3 pc
6	Short links and connecting leads	-----
7	Multimeter	1 pc

Procedure:

1. Connect the circuit as shown in Figure 14.
2. Connect A_1, A_0, B_1, B_0 to switches and the outputs to an LED.
3. With the breadboard power supplies ON, obtain the truth table for the circuit, setting the inputs as shown in Table 7 and noting the state of the. Record the values in Table 7.

Input A		Input B		Output ($A = B$)
A_1	A_0	B_1	B_0	
0	0	0	0	
0	1	0	1	
1	0	1	0	
1	1	1	1	
0	0	1	0	
0	1	1	0	

Table 7

The first four input settings represent conditions with both pairs of inputs (A_1, B_1 and A_0, B_0) equal. The fifth represent conditions with one pair of inputs (A_1, B_1) unequal, and the other pair (A_0, B_0) equal. The last setting represents conditions with both pairs of inputs unequal.

Trouble Shooting:

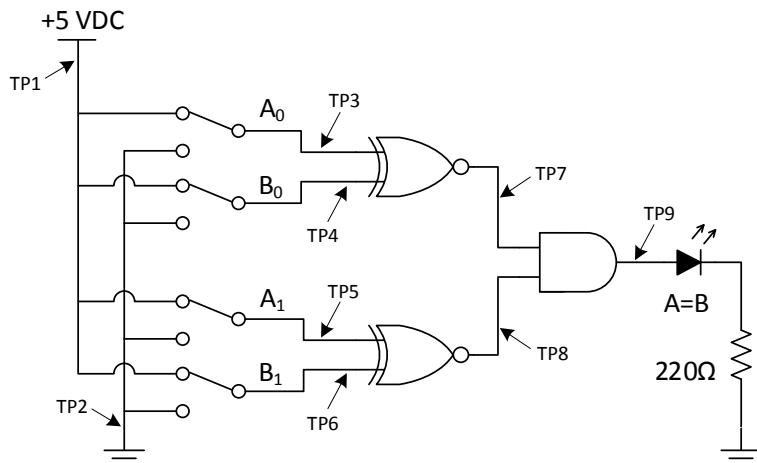


Figure 15: Magnitude Comparator Circuit and Test Points

Procedure:

1. With the bread board power supply ON, apply input A & input B (please refer to Table 7 for the input settings). Verify the output through logic monitor or LED'S. Initiate fault and perform voltage check in every test point as shown in Figure 15.
2. Record the results in the Table 8 during normal condition and during fault condition.
3. Check SPDT switch position and connecting leads for possible loose wiring connection.

Test Points	Voltage Reading:	
	Normal Condition	Fault Condition
TP1		
TP2		
TP3		
TP4		
TP5		
TP6		
TP7		
TP8		
TP9		

Table 8

Review Questions:

1. What is a magnitude comparator circuit?
 2. A two input magnitude comparator with inputs A & B has input A1, A0 set 0,1 and the output A less than B is logic level 1. Possible input states B1, B0 are:
 - a. 0,0 or 0,1
 - b. 0,1 or 1,0
 - c. 0,1 or 1,1
 - d. 1,0 or 1,1
 3. A 2-input magnitude comparator with inputs A & B has input A1, A0 set 1,0 and the output A greater than B is logic level 1. Possible input states B1, B0 are:
 - a. 0,0 or 0,1
 - b. 0,1 or 1,0
 - c. 0,1 or 1,1
 - d. 1,0 or 1,1

Unit 3: Sequential Circuits

The circuits we studies so far were all combination circuits, where the output relies solely on the inputs. While these circuits are capable of doing interesting operations, it is important in some designs to store information between different operations. For example, some car stereo systems use one button to skip to the next audio track, and also to scan for the next radio channel. The state of the stereo determines the function of the button. Another example is when the buttons on a vending machine do not respond unless enough money is inserted into the machine. There are multiple ways to store information; we will look at the simplest and most common component, the flip-flop.

SR Flip-Flop

The SR flip-flop can be constructed from two cross-coupled NOR or NAND gates. The flip-flop has two inputs; the Set input turns the output Q to 1 while the Reset input brings it to 0. The new and interesting function here is when the Set and Reset inputs are kept at 0. The flip-flop holds the output at the state it was in, effectively storing it. The last case where the Set and Reset are both put to 1 is undefined; i.e. the state of Q cannot be predicted. It also does not make sense to set and reset the flip-flop at the same time.

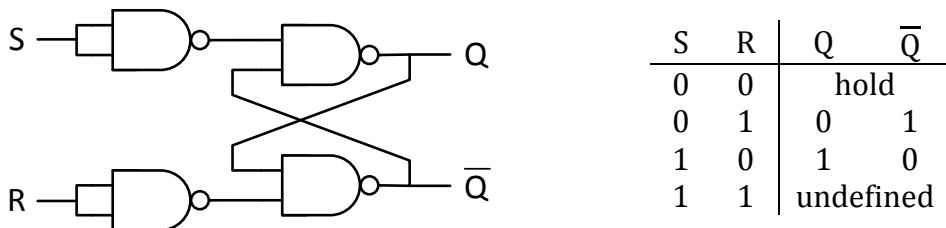


Figure 16: SR Flip Flop with NAND Gates

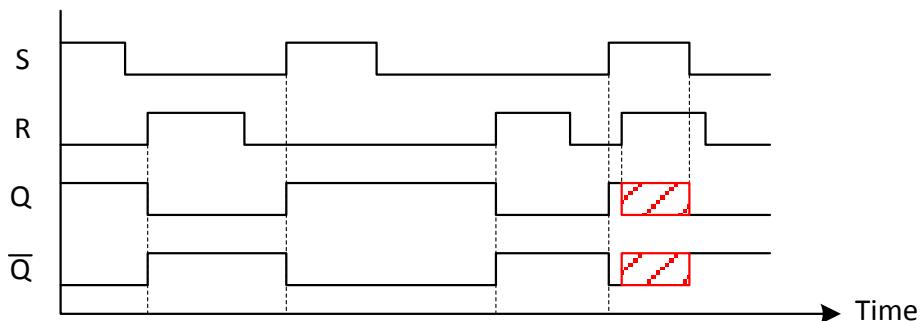


Figure 17: A Sample Timing Diagram of an SR Flip-Flop

At some point, it became important to add an enable signal to the flip-flop so that the inputs can be used for something else without disturbing the value stored in the flip-flop. The enable input can easily be done by ANDing it with the S and R inputs. This flip-flop is called “Gated SR Flip-Flop”.

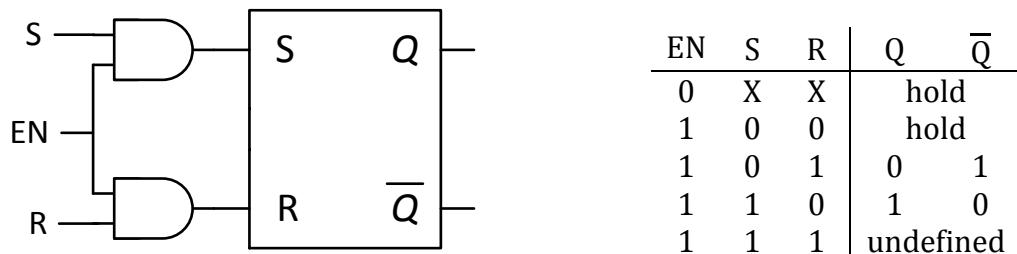


Figure 18: SR Flip-Flop with an Enable Input

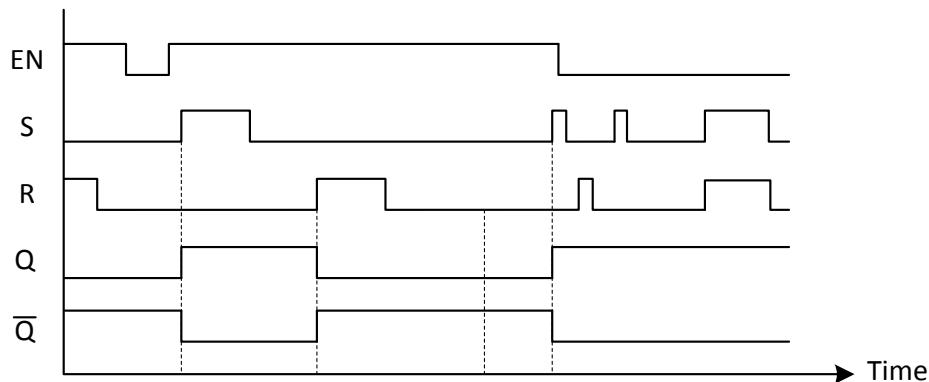


Figure 19: A Sample Timing Diagram of a Gated SR Flip-Flop

Later again, some sequential designs experienced limitations with having to set the enable line before changing the flip-flop’s storage; therefore, two asynchronous S and R were added to the gated flip-flop. These inputs have more priority over the regular S and R inputs and do not rely on the enable line to function. These two inputs are sometimes referred to as “Preset” and “Clear” to distinguish them from the Set and Reset inputs. This flip-flop is called an “Asynchronous SR Flip-Flop.”

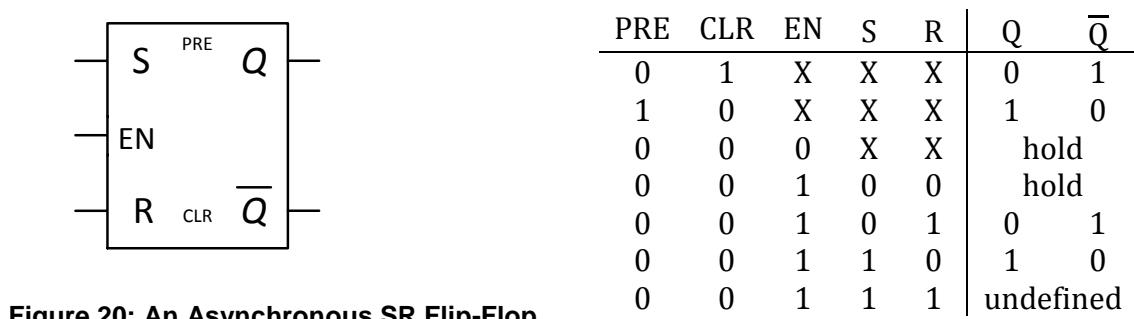
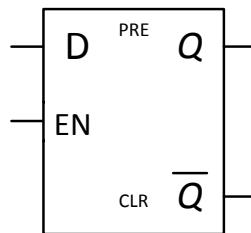


Figure 20: An Asynchronous SR Flip-Flop

D Flip-Flop

The D flip-flop can be constructed by connecting the D input line to both the S and R inputs of an SR flip-flop, but inverting the D signal before it reaches the R input. This eliminates the undefined condition from the truth table. The enable line works to either store the value of D or fetch a new value. The D flip-flop also has an asynchronous variant.



PRE	CLR	EN	D	Q	\bar{Q}
0	1	X	X	0	1
1	0	X	X	1	0
0	0	0	X	hold	
0	0	1	0	0	1
0	0	1	1	1	0

Figure 21: Asynchronous D Flip-Flop

Clock Signals

A clock signal is a particular type of signal that oscillates between a high and a low state and is utilized to coordinate actions of digital circuits. The clock signal ensures that the flow of states in digital systems is synchronized and the operations through them serialized. Circuits may become active at either the rising edge (positive-edge-triggered), falling edge (negative-edge-triggered), or in the case of double data rate, both in the rising and falling edges of the clock cycle. The example below shows the effect of replacing the enable input of the D flip-flop with a clock signal. Also note in this example that the Preset and Clear inputs are active-low, meaning they activate when they are 0 instead of 1.

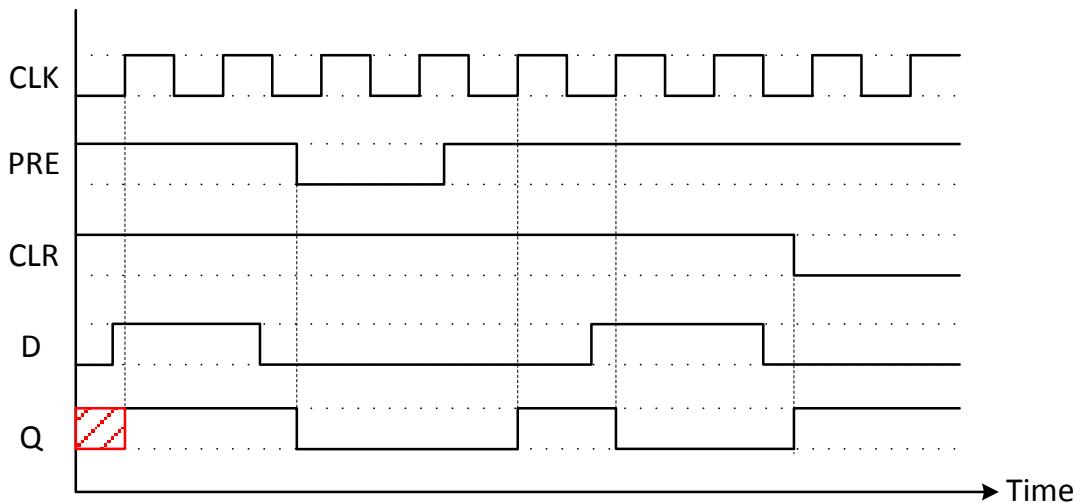
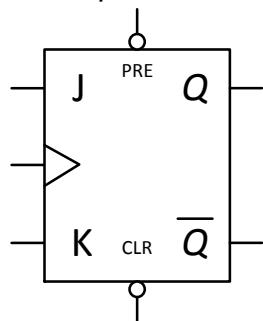


Figure 22: A Timing Diagram for a Positive-Edge-Triggered Asynchronous D Flip-Flop

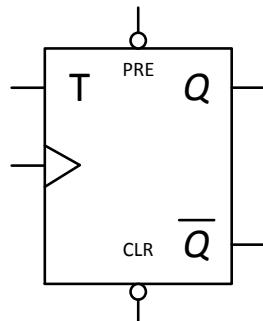
JK and T Flip-Flops

The last two types of flip-flops we will look at are the JK and T flip-flops. The JK flip-flop is similar in operation to the SR flip-flop except when both inputs are 1, the output toggles with the JK flip-flop. Toggling means the output will be 0 if it was 1 and 1 if it was 0. The T flip-flop is just a JK flip flop with the J and the K inputs connected together; thereby making the flip-flop toggle at every clock pulse if the input is 1.



PRE	CLR	CLK	J	K	Q
0	1	X	X	X	1
1	0	X	X	X	0
1	1	not↑	X	X	hold
1	1	↑	0	0	hold
1	1	↑	1	0	1
1	1	↑	0	1	0
1	1	↑	1	1	toggle

Figure 23: A JK Flip-Flop



PRE	CLR	CLK	T	Q
0	1	X	X	1
1	0	X	X	0
1	1	not↑	X	hold
1	1	↑	1	0
1	1	↑	0	1

Figure 24: A T Flip-Flop

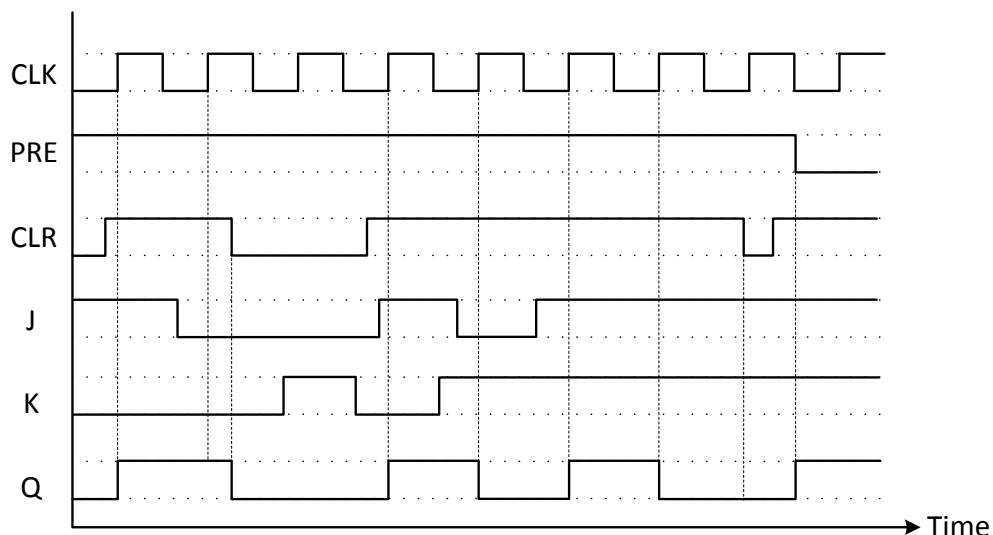
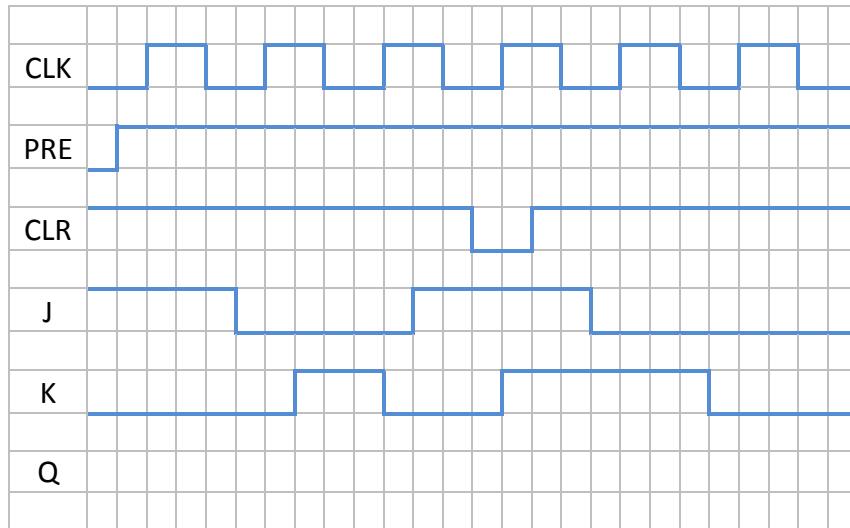
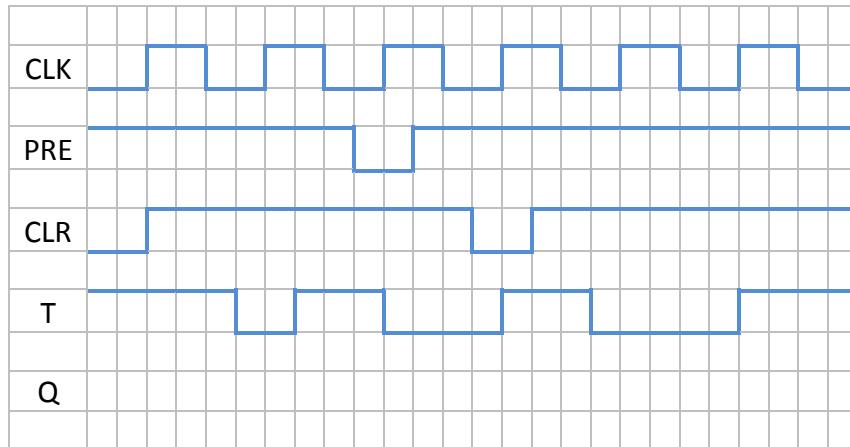


Figure 25: A Sample Timing Diagram of a Positive Edge-Triggered JK Flip-Flop

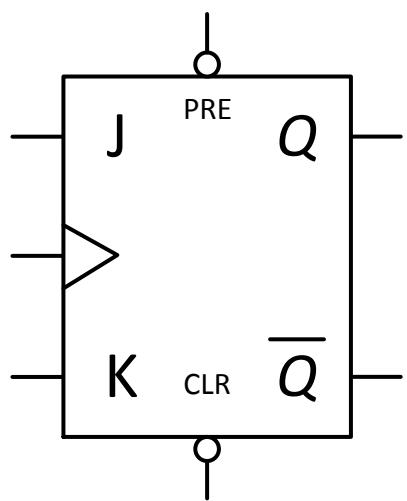
Review Questions

1. What are sequential circuits?

2. Complete the timing diagrams shown below. The flip-flops are all negative edge-triggered and the PRE and CLR inputs are active LOW.



Exercise 8: JK Flip-Flop



Objectives:

- Recognize the difference between an R-S flip-flop and a J-K flip-flop with respect to the way in which “memory” is set and reset
- Appreciate the advantages of a JK flip flop.

Discussion:

The JK flip-flop is a type of flip-flop which means it can be used to store one bit of data. The data can be a number, part of a number or a letter, or a circuit state value. The value stored can be observed in the output Q. The JK flip-flop works by responding to the J and K inputs as shown in Figure 26. The JK flip-flop has the advantage of having a toggle function when both J and K are set to 1, an input combination that results in an invalid state in the SR flip-flop.

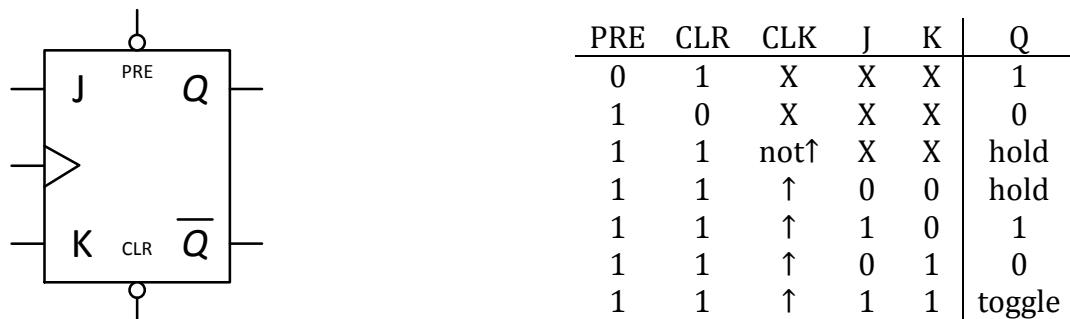


Figure 26: A JK Flip-Flop

Logic Diagram:

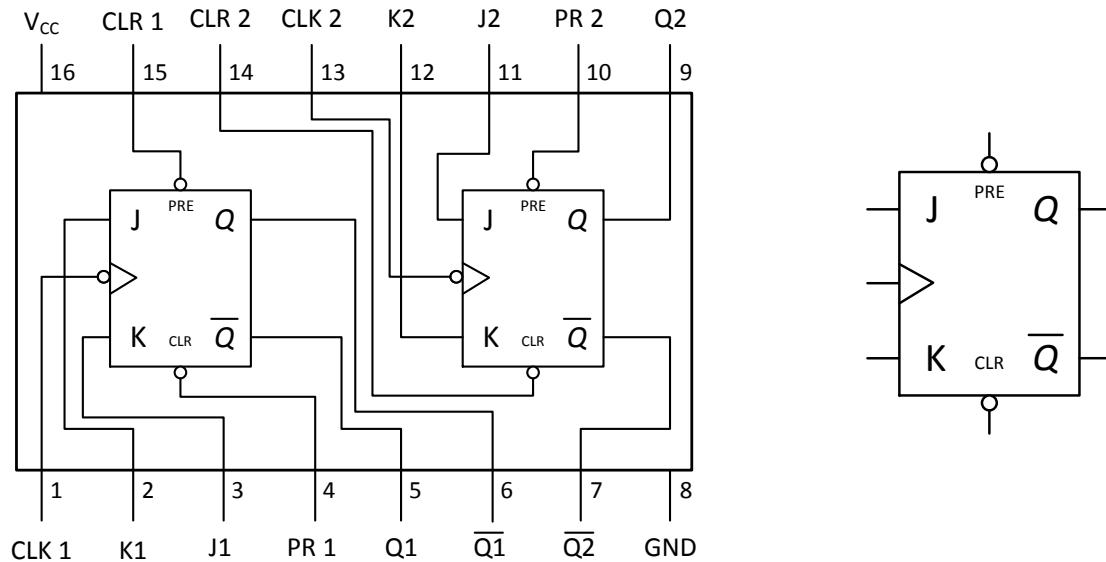


Figure 27: Internal Connections of the 74112 (Dual JK Flip-Flop)

Equipment:

No.	Description	Qty.
1	AC/DC power supply	1 Pc
2	Digital multimeter	1 Pc
3	Toggle Switch	2 Pcs
4	Bread board	1 Pc
5	74LS112 Flip flop IC	1 Pc
6	Connection wires (jumpers), 0.5 mm ²	1 Pc

Procedure:

- Using the pin configuration diagram in Figure 27, mount the 74LS112 IC on a breadboard. Use a toggle switch for the inputs (S, C) and LEDs for the outputs. Apply V_{CC} and Ground to the proper pins on the IC. Place the S & C inputs to logic '0' initially.
- Turn on the power supply. Using a logic probe or VOM, measure and record the logic state of the outputs.
- Fill the truth table below.

PRE	CLR	J	K	Clk	Q	\bar{Q}
1	1	0	0	↓		
1	1	0	1	↑		
1	1	0	1	↓		
1	1	1	0	↑		
1	1	1	0	↓		
1	1	1	1	↑		
1	1	1	1	↓		

Table 9

- Complete the timing diagram below.

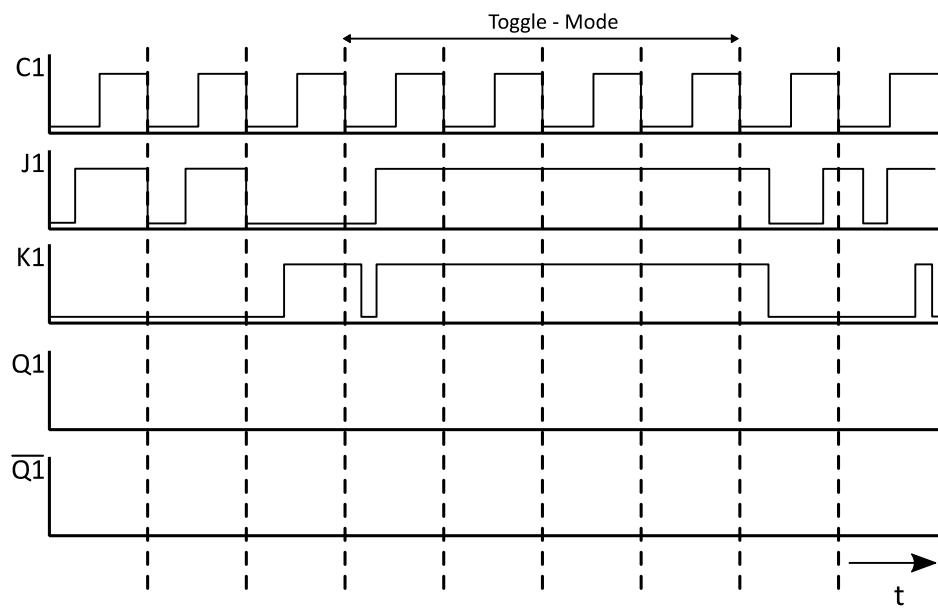


Figure 28

Troubleshooting:

1. Apply a pulse to the PR input.
- a. Proper Result: Q=high, Flip-flop Preset

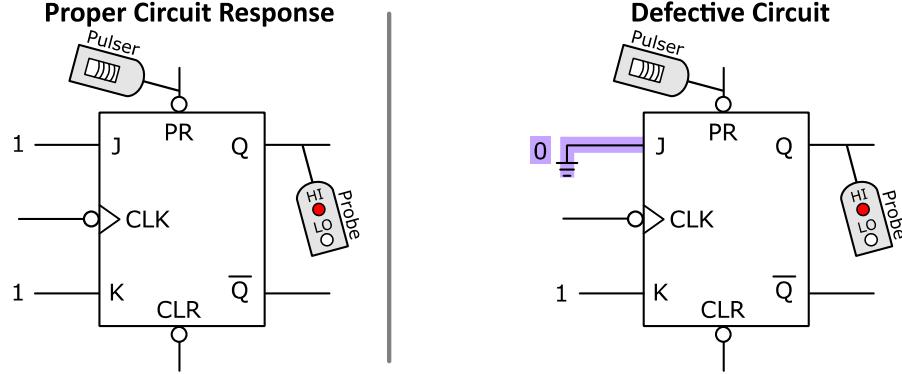


Figure 29

2. Apply a pulse to the CLR input

- a. Proper Result: Q= low, flip-flop is cleared

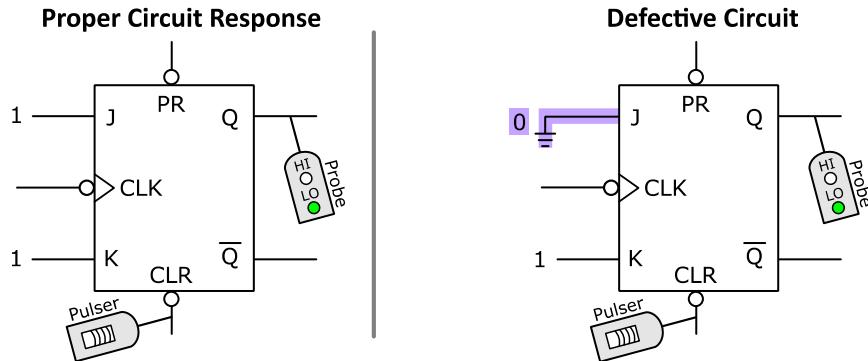


Figure 30

3. Apply a pulse to the CLK circuit.

- a. Proper result: Q=high, flip-flop toggled

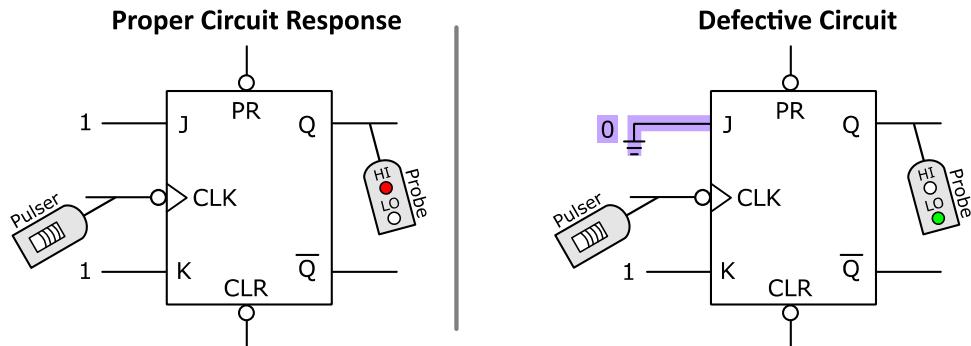


Figure 31

1. Apply a pulse to the PR input.

a. Proper Result: Q= high, flip-flop preset

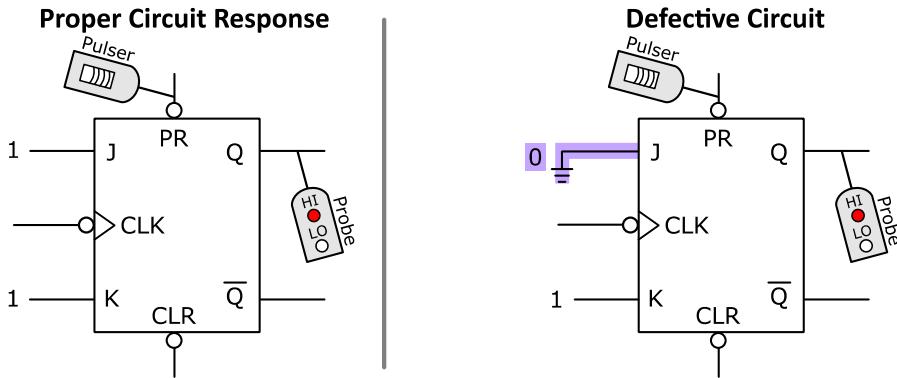


Figure 32

2. Apply a pulse to the CLK input

a. Proper result: Q= low, flip-flop toggled

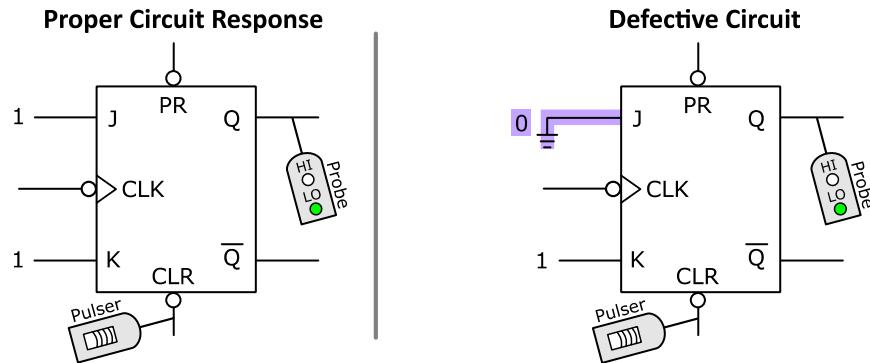


Figure 33

3. Apply a pulse to the CLK input.

a. Proper result: Q=high, flip-flop toggled

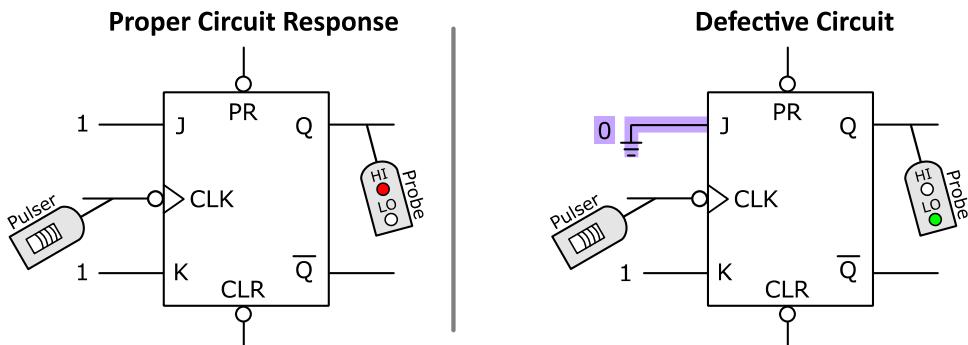
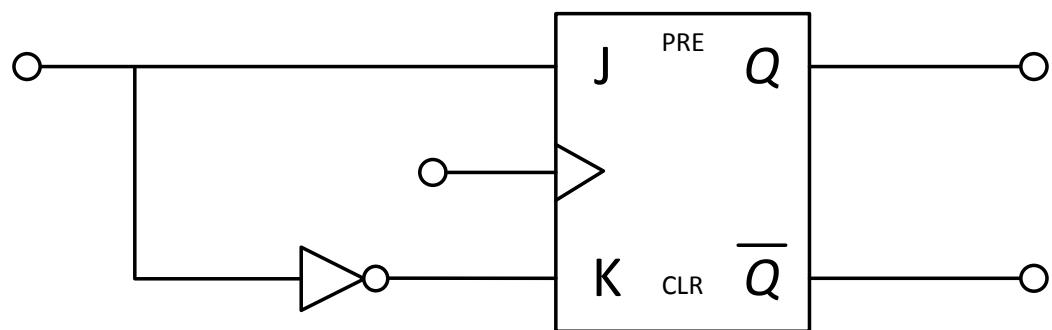


Figure 34

Exercise 9: JK Flip-Flop Connected as D-Type



Objectives:

- Determine the operation of a J-K flip flop when connected as a D-type
- Predict the inputs for a given output condition.

Discussion:

The D flip-flop is a very simple that stores the value of the D in the flip-flop which shows it on the Q output. The clock is the only control input that decides whether to hold the value or fetch a new value for D. The D flip-flop can be constructed from a JK flip-flop by connecting the D input to the J directly and connecting its complement to the K input.

Logic Diagram:

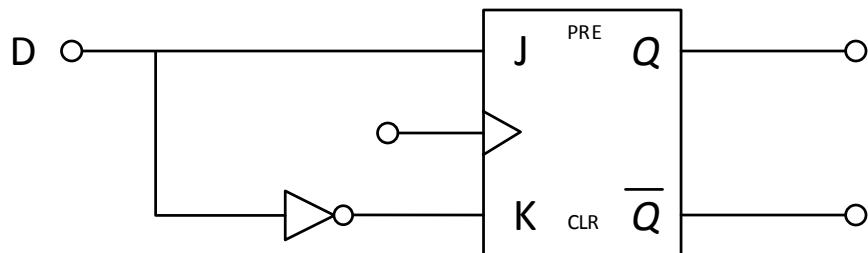


Figure 35

Equipment:

No.	Description	Qty.
1	Logic Probes	1 Pc
2	LEDs	2 Pcs
3	Bread board	1 Pc
4	7404 Hex NOT gate IC	1 Pc
5	74112 Dual J-K Flip-Flop with preset and clear	1 Pc
6	Connection wires (jumpers), 7.5 mm ²	1 Pc

Procedure:

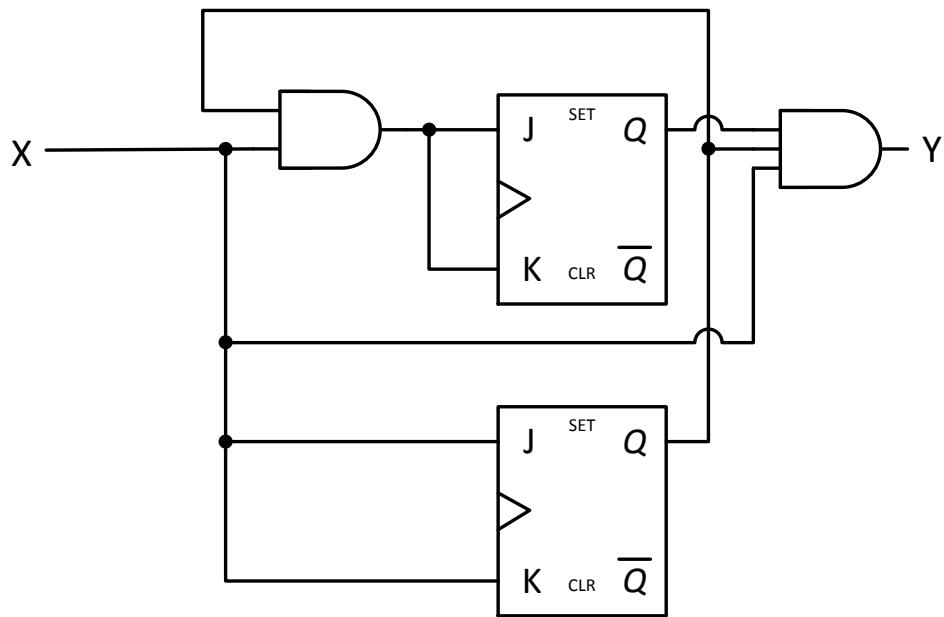
- A D- flip-flop can be implemented from a J-K flip-flop and an inverter.
Connect the J – K inputs to either the D or \bar{D} signal to cause circuit to behave like a D flip-flop.
- Using the pin configuration diagram in Figure 35, mount the 74LS112 IC and 7404 IC on a breadboard. Connect the inputs and outputs. Use a toggle switch for the inputs (S, C). Apply VCC and Ground to the proper pins on the IC. Place the S & C inputs to logic ‘0’ initially.
- Complete the table below.

PRE	CLR	D	CLK	Q
1	1	0	↓	
1	1	1	↑	
1	1	1	↓	
1	1	0	↑	
1	1	0	↓	

Table 10

- For the D-type flip flops and the J-K flip flops which of the following statements, regarding the device clocking is true?
 - a. D & J-K types are edge-triggered, both on the positive side.
 - b. D & J-K types are edge-triggered, both on the negative side.
 - c. D & J-K types are edge-triggered, D positive, J-K negative edge.
 - d. D & J-K types are edge-triggered, D active high, J-k active low.

Exercise 10: Building Sequential Circuits with Flip-Flops



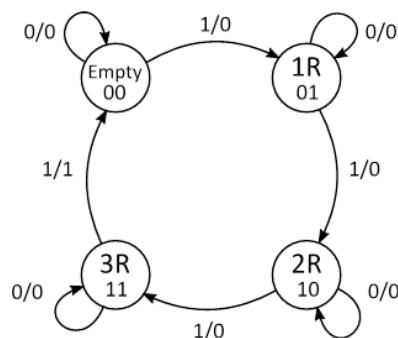
Objectives:

- To appreciate the importance of flip-flops in a practical setting.

Discussion:

The ability of flip-flops to store data makes them useful for creating circuits that transition between different states and respond to inputs differently. In this exercise, we introduce one example of such case. We are to build a circuit for a coffee machine that serves a cup of coffee when 4 riyals are inserted into it.

To build such circuit, we first draw a state diagram that represents each state by a circle. The transition of one state to the next is indicated by an arrow with the input condition that caused the transition. For example, the machine moves from the empty state to the 1R (1 riyal) state if the input is 1 (if a riyal is inserted into the machine). The circuit keeps moving every time a riyal is inserted until we reach the 3R state. If an additional riyal is inserted, the output is switched to 1 and the circuit returns to the empty state.



From the state diagram, we can derive a state table that shows the present state and next state at each input case.

present state		X	next state		Y
Q _A	Q _B		Q _{A+}	Q _{B+}	
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	1	0
1	1	1	0	0	1

The next step is to choose a flip-flop type. Sequential problems can be solved with any flip-flop, but using the JK flip-flop usually produces the simplest circuit. We need to determine the inputs at J and K that satisfy the transition from the present state and next state for each of our flip-flop outputs. To do that, the excitation table for the flip-flop is very useful.

Q	Q+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Excitation Table For
the JK FF

Q _A	Q _B	X	Q _{A+}	Q _{B+}	Y	J _A	K _A	J _B	K _B
0	0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	0	X	1	X
0	1	0	0	1	0	0	X	X	0
0	1	1	1	0	0	1	X	X	1
1	0	0	1	0	0	X	0	0	X
1	0	1	1	1	0	X	0	1	X
1	1	0	1	1	0	X	0	X	0
1	1	1	0	0	1	X	1	X	1

Then we simplify the output as well as the flip-flop inputs using Karnaugh maps.

X	Q _A Q _B	J _A
	00 01 11 10	
0		X X
1	1 X	X

$$J_A = XQ_B$$

X	Q _A Q _B	K _A
	00 01 11 10	
0	X X	
1	X X 1	

$$K_A = XQ_B$$

X	Q _A Q _B	J _B
	00 01 11 10	
0		X X
1	1 X X 1	

$$J_B = X$$

X	Q _A Q _B	K _B
	00 01 11 10	
0	X	
1	X 1 1 X	

$$K_B = X$$

X	Q _A Q _B	Y
	00 01 11 10	
0		
1		1

$$Y = XQ_AQ_B$$

Lastly, we draw the circuit now that we have all required information (Figure 36).

Logic Diagram:

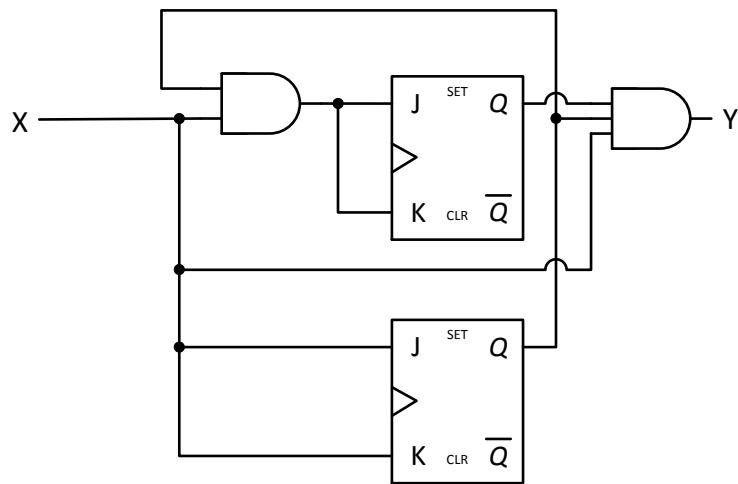


Figure 36

Equipment:

No.	Description	Qty.
1	Function generator with integrated AC/DC power supply	1 Pc
2	Breadboard	1 Pc
4	LEDs	2 Pcs
5	74112 JK Flip-Flop IC	1 Pc
6	7408 Quad two-input AND gate IC	1 Pc
9	Connection wires (jumpers), 0.5 mm ²	1 Pc

Procedure:

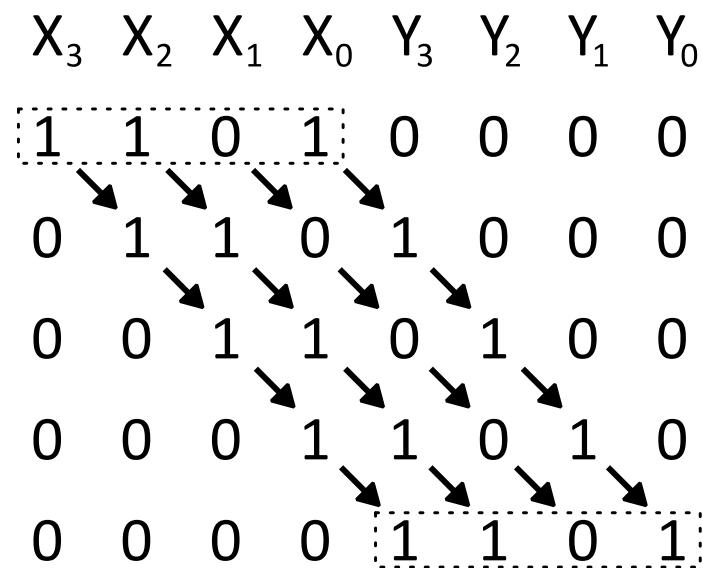
1. Connect the circuit shown in the Logic Diagram section
2. Connect X to a switch and Y to an LED. Also connect QA and QB to two separate LEDs; this helps in debugging the circuit.
3. Connect the clocks of the two flip-flops to a push-button switch or a pulse generator.
4. Turn on the power supply and test whether or not the circuit works as expected. Fill out the results in Table 11.

Q _A	Q _B	X	CLK	Q _{A+}	Q _{B+}	Y
0	0	0	↓			
0	0	1	↓			
0	1	0	↓			
0	1	1	↓			
1	0	0	↓			
1	0	1	↓			
1	1	0	↓			
1	1	1	↓			

Table 11

5. Does the result match with the table in the discussion?

Exercise 11: Characteristics of a D-Type Shift Register



Objectives:

To the shift register using flip flop and verifying the function of the 74F174 shift register IC.

Discussion:

Shift Registers

Binary data can be shifted from one flip-flop to the next on each clock pulse. The shift from left to right here is the kind of data transfer that occurs in a serial transfer.

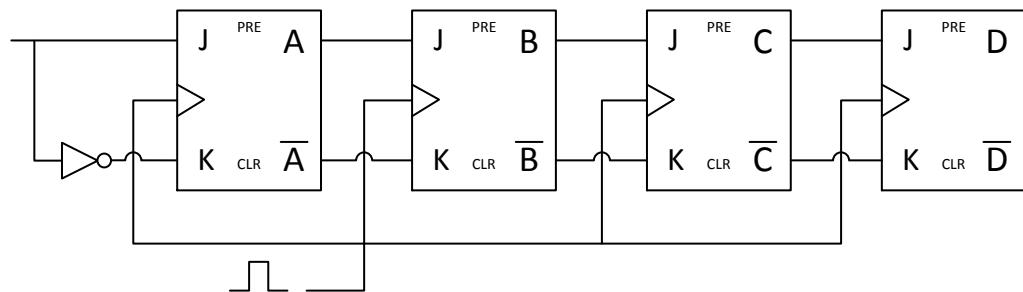


Figure 37

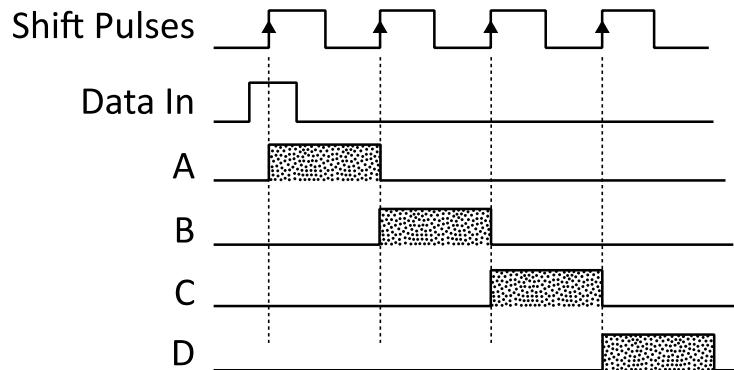


Figure 38

Serial Data Transfer

As an example of serial data transfer using the shift register approach, a set of four shifts triggered by clock pulses places the contents of the X-register into the Y-register. Since four clock cycles are needed, this form of serial transfer is much slower than parallel transfer, but is simpler and cheaper.

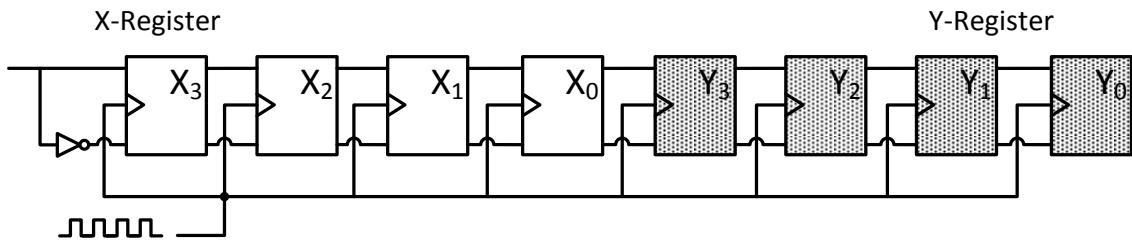


Figure 39

X_3	X_2	X_1	X_0	Y_3	Y_2	Y_1	Y_0
1	1	0	1	0	0	0	0
0	1	1	0	1	0	0	0
0	0	1	1	0	1	0	0
0	0	0	1	1	0	1	0
0	0	0	0	1	1	0	1

Figure 40

Parallel Data Transfer

The illustration below shows the parallel transfer of 8 bits of data from the X Register to the Y Register upon application of an enabling transfer pulse. Clearly, parallel data transfer is faster than serial data transfer, but serial transfer has the advantages of requiring less hardware. These registers are made up of D flip-flops, which can serve as memory locations. The information in the X Register is intact after the transfer to the Y Register, so this process shows a possible scenario for accessing digital information stored in memory.

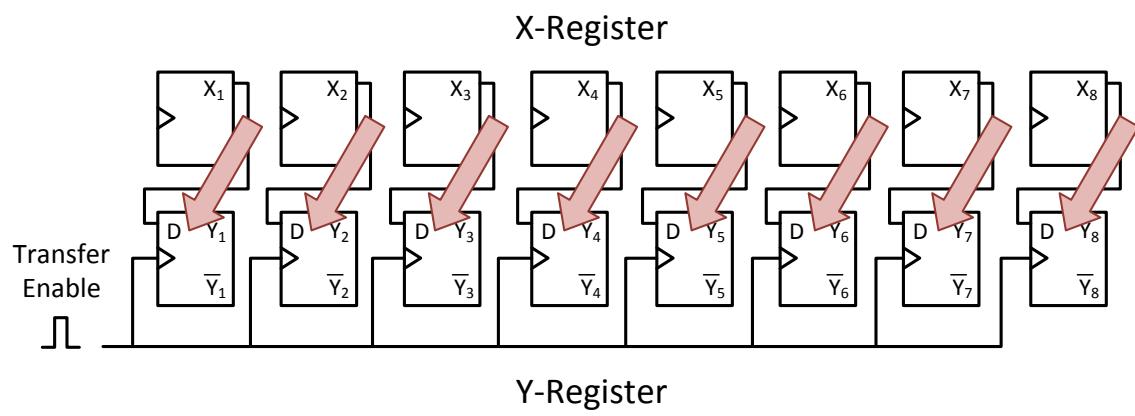
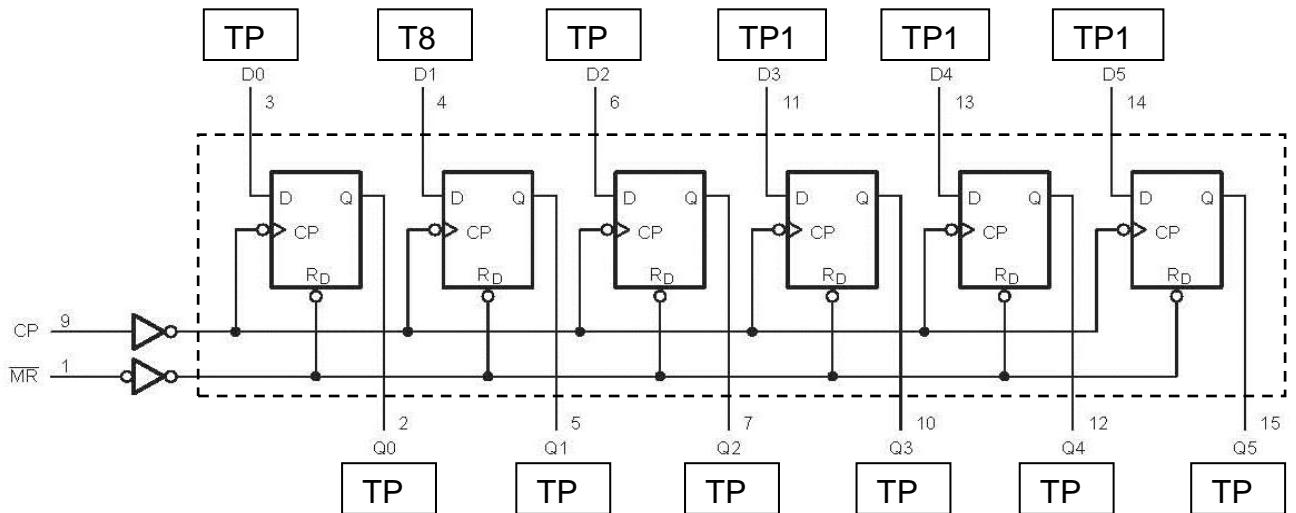


Figure 41

Logic Diagram:



V_{cc} = Pin 16

GND = Pin 8

Figure 42

Equipment:

No.	Description	Qty.
1	Function generator with integrated AC/DC power supply	1 Pc
2	Digital multimeter	1 Pc
3	Logic Probes	1 Pc
4	LED's	2 Pcs
5	Bread board	1 Pc
6	74174Hex D-Type flip flop	1 Pc
7	Pulse Generator	1 Pc
8	Connection wires (jumpers), 7.5 mm ²	1 Pc

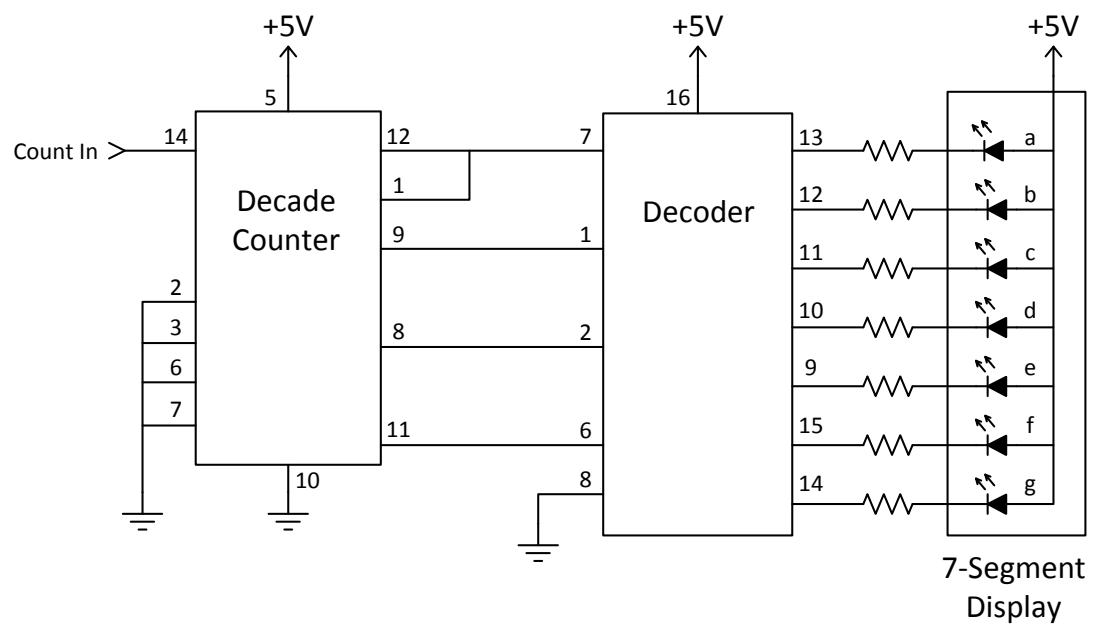
Procedure:

1. Assemble the circuit as shown in Figure 42.
2. Ensure that the power switch of the IC trainer is turned off.
3. Plug every IC chip into the proper socket.
4. Connect all IC's pins required for verifying the given function table.
5. Once all connections have been done, turn on the power.
6. According to the function table apply the four modes of the universal shift register and verify the correct functioning of the chip.
7. After finishing the experiment, turn off the power switch, disconnect the wires, take out all IC chips from the breadboard, and put back everything you have used.

Test Point	Test Point
TP1 = V	TP7 = V
TP2 = V	TP8 = V
TP3 = V	TP9 = V
TP4 = V	TP10 = V
TP5 = V	TP11 = V
TP6 = V	TP12 = V

Table 12

Exercise 12: Binary/BCD Counters and 7-Segment Decoders



Objective:

1. Observe the operation of a binary up/down counter.
2. Predict the operation of a binary and BCD up/down counter under known input conditions.
3. Diagnose faults in binary counter, BCD counter and 7-segment decoder/driver/display circuits.

Discussion:

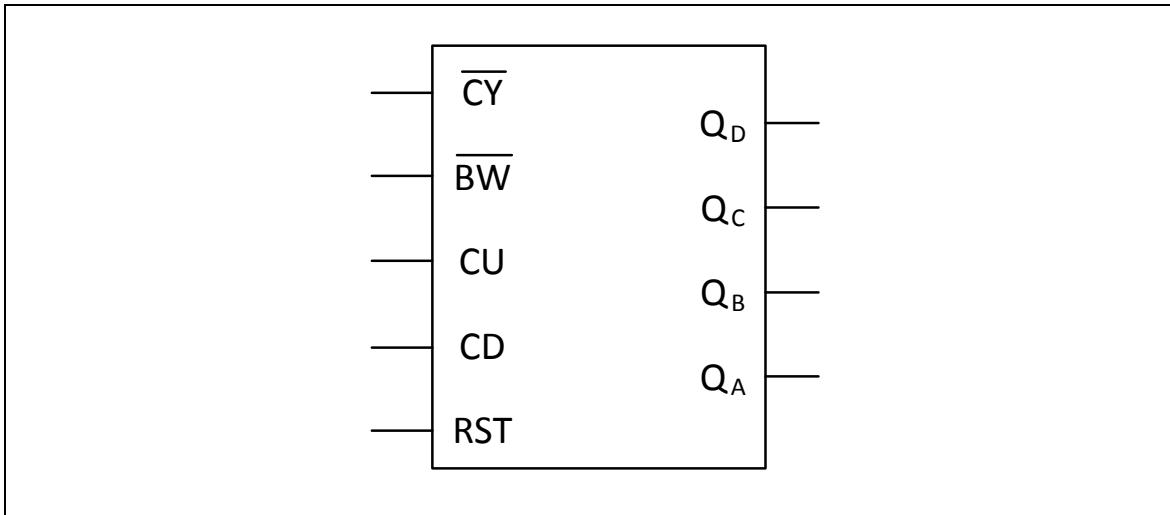


Figure 43

Figure 43 shows a block diagram of a 4-bit binary UP/DOWN counter with the normal input/output facilities.

CU: Count UP input, active on a positive going input signal.

CD: Count DOWN input, active on a positive going input signal.

RST: Reset count input, active high.

Q_A : Least significant binary output.

Q_B : Next significant binary output.

Q_C : Next significant binary output.

Q_D : Most significant binary output.

CY: Carry signal, active low. This produces a negative output pulse when counting UP and the count is changing from maximum (15) to zero (0).

BW: Borrow signal, active low. This produces a negative output pulse when counting DOWN and the count is changing from zero (0) to maximum (15).

Table below shows the sequential binary outputs for counting UP and counting DOWN conditions

Count	Q _D	Q _C	Q _B	Q _A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Count Up

Binary Up/Down Counting

Count	Q _D	Q _C	Q _B	Q _A
0	0	0	0	0
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1

Count Down

Table 13

Table below shows the sequential binary outputs for a binary coded decimal UP/DOWN counter, the count resetting to zero after a count of 9.

Count	Q _D	Q _C	Q _B	Q _A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Count Up

BCD Up/Down Counting

Count	Q _D	Q _C	Q _B	Q _A
0	0	0	0	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1

Count Down

Table 14

Figure 44 below shows the binary output and carries waveform for a ripple through binary UP counter, the stages clocking on the negative going edge of the input pulses.

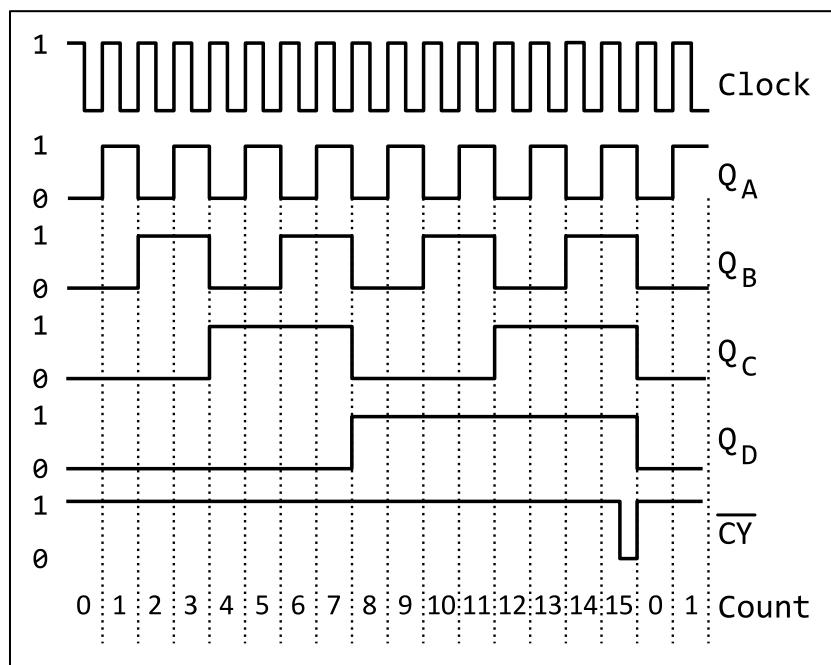


Figure 44

Figure 45 below shows the binary output and borrow waveforms for a ripple through binary DOWN counter, the stages clocking on the positive going edge of the input pulses.

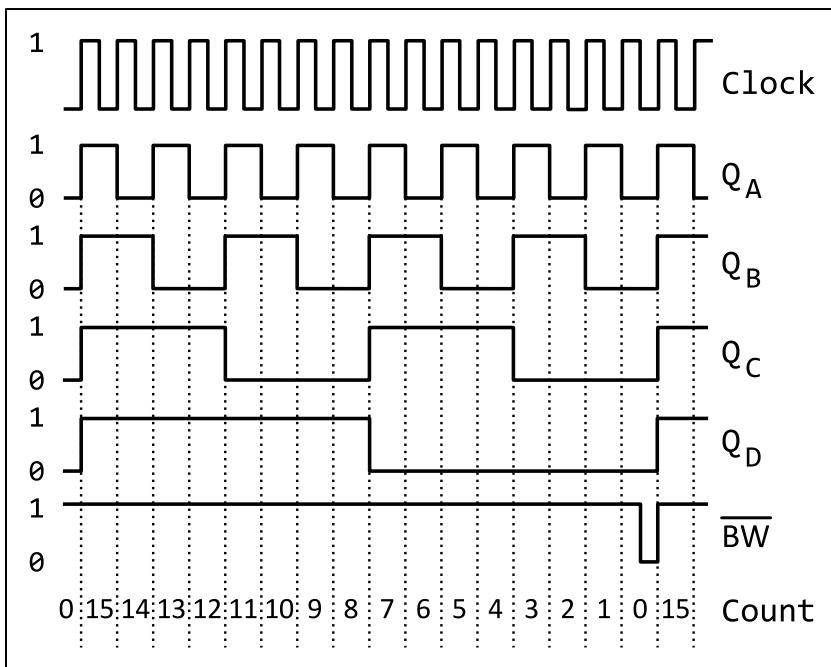


Figure 45

Circuit Diagram:

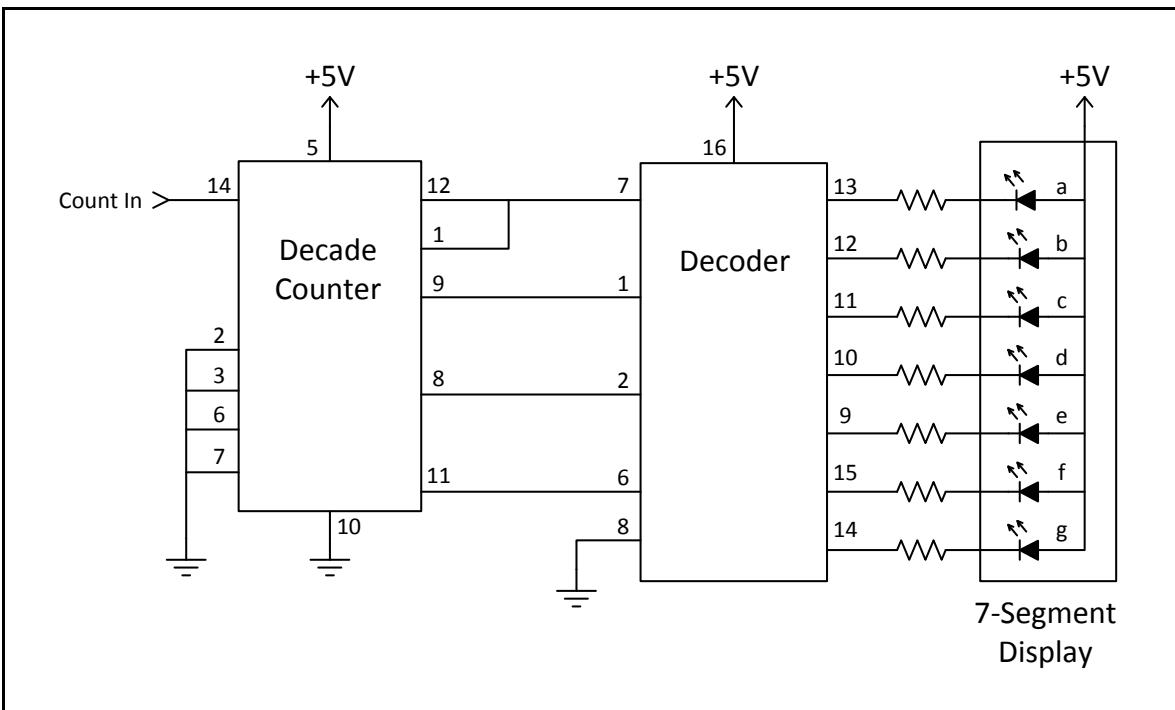
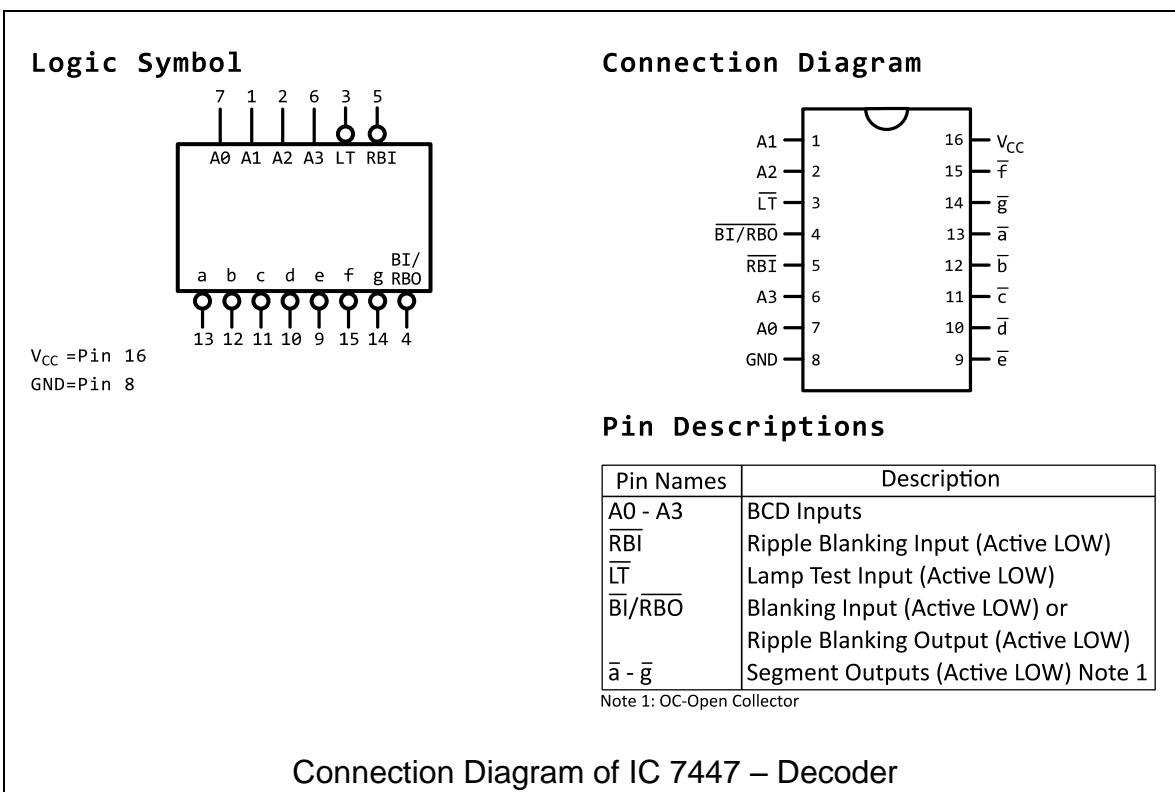


Figure 46



Connection Diagram								Reset/Count Truth Table							
INPUT A	NC	Q _A	Q _D	GND	Q _B	Q _C		Reset Inputs		Output					
14	13	12	11	10	9	8		R0(1)	R0(2)	R9(1)	R9(2)	Q _D	Q _C	Q _B	Q _A
								H	H	L	X	L	L	L	L
								H	H	X	L	L	L	L	L
								X	X	H	H	H	L	L	H
								X	L	X	L			COUNT	
								L	X	L	X			COUNT	
								L	X	X	L			COUNT	
								X	L	L	X			COUNT	

Figure 47: Connection Diagram of IC 7490

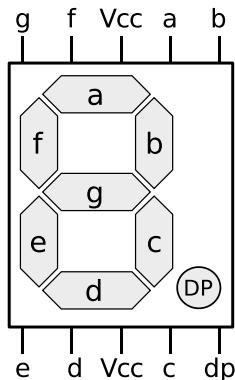


Figure 48: 7-Segment Common-Anode Display Reference

Equipment:

Sr.	Name	Quantity
1	470 or 330 Ohm 8-DIP resistor network	1 pc
2	7490 TTL BCD Counter IC	1 pc
3	7447 TTL Seven Segment Display Driver IC	1 pc
4	Common-Anode 7-Segment LED Display	1 pc
5	Board, Sockets for ICs, Wire	-

Notes:

- All pulses to be counted are to be TTL compatible. They should not exceed 5V and not fall below ground.
- You can add more digits by building a second (or third, or fourth, etc...) circuit and connecting the pin 11-6 junction of the 74LS90 and 74LS47 to pin 14 of the 74LS90 in the other circuit. You can keep expanding this way to as many digits as you want.

Procedure:

1. Insert shorting leads and connect the circuit as shown in Figure 46.
2. Set the Oscilloscope control as follows
 - a) Time base control to ms/div, trigger selector to CH.2, AC dual trace.
 - b) CH.1 Y amplifier gain to 2V/div, DC input
 - c) CH.2 Y amplifier gain to 2V/div, DC input
3. With the module Power supplies switched ON, press the single clock or pushbutton repeatedly and at each press note the counter output states and the corresponding 7-segment display. Note that the UP counter counts every time you press the pushbutton.
4. Record the results in Table 15.
5. Repeat the process, pressing the single clock or pushbutton repeatedly counts in DOWN, the count decreasing when the switch is released.
6. With the oscilloscope set for negative triggering, note the CH.1 and CH.2 waveform, these representing the counter outputs Q_A and Q_B respectively, and sketch them on the axes provided. (Fig. 13.5)

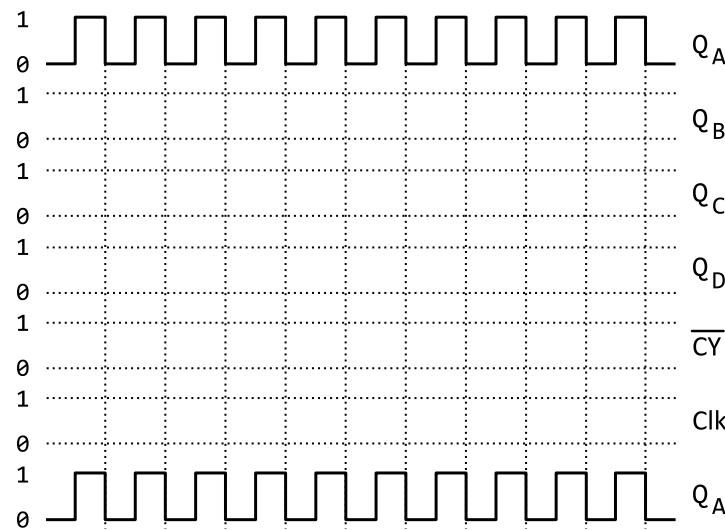


Figure 49

7. With the Module Power Supplies switched ON and with Code Switch A set to logic level 0, press the Single Shot Clock Switch E repeatedly and at each press note the counter output states and the corresponding 7-Segment display. Record the results in Table 15. Note that the counter counts UP each time the switch is pressed, the count increasing when the switch is released, that is, the count increases on the positive going edge of the clock pulse.

Pulse	Q_D	Q_C	Q_B	Q_A	7-Segment Display
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					

Table 15

8. Repeat the procedure to obtain and sketch the following waveform.
9. Connect clock output to channel 1 of the oscilloscope. Connect clock output to Channel 1 of the oscilloscope. Connect the output of Q_A to Channel 2. Observe the clock pulses and Q_A and record their timing waveforms.
10. Connect Q_A to Channel 1 of the oscilloscope and Q_B to Channel 2, and record their timing waveforms.
11. Repeat Step 7 with Q_B connected to Channel 1 and Q_C connected to Channel 2.
12. Repeat Step 7 with Q_C connected to Channel 1 and Q_D connected to Channel 2.
13. Sketch the timing relationship of the clock and the four outputs in one composite diagram showing at least 16 clock cycles.

Fault Diagnosis Procedures:

The fault diagnosis procedure should therefore be as follows:

1. Take readings at the test points as instructed in the worksheet.
2. Identify the possible faults from consideration of the readings obtained.
3. Carry out further tests (at the IC pins if necessary) to confirm the actual fault. IC pins configuration should be consulted for the IC pin numbers. LED's can be ignored as far as fault diagnosis is concerned - their function is only to act as indicators.

Ensure that you carry out your measurements on the correct IC number and at the correct pin numbers of that IC. When taking measurements at IC pins, be careful not to short-circuit adjacent pins.

Circuit Diagram:

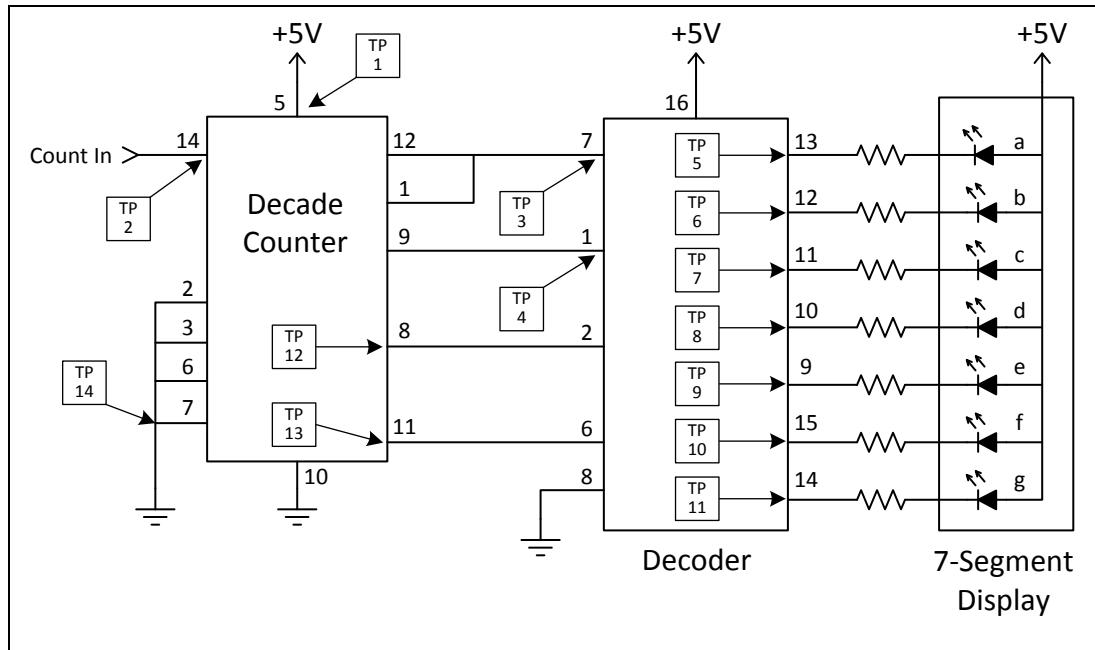


Figure 50

Procedure

1. Connect the circuit shown in the diagram Figure 50.
2. Switch the power supply ON, test and fill-up the Table 16.

Sr no.	Component Testing	Std Values	Voltage
1	R1		
2	R2		
3	R3		
4	R4		
5	IC 7490 & 7447		
9	S1-switch	Contacts	
11	TP1		
12	TP2		
13	TP3		
14	TP4		
15	TP5		

16	TP6		
17	TP7		
18	TP8		
19	TP9		
20	TP10		
21	TP11		
22	TP12		
23	TP13		
24	TP14		

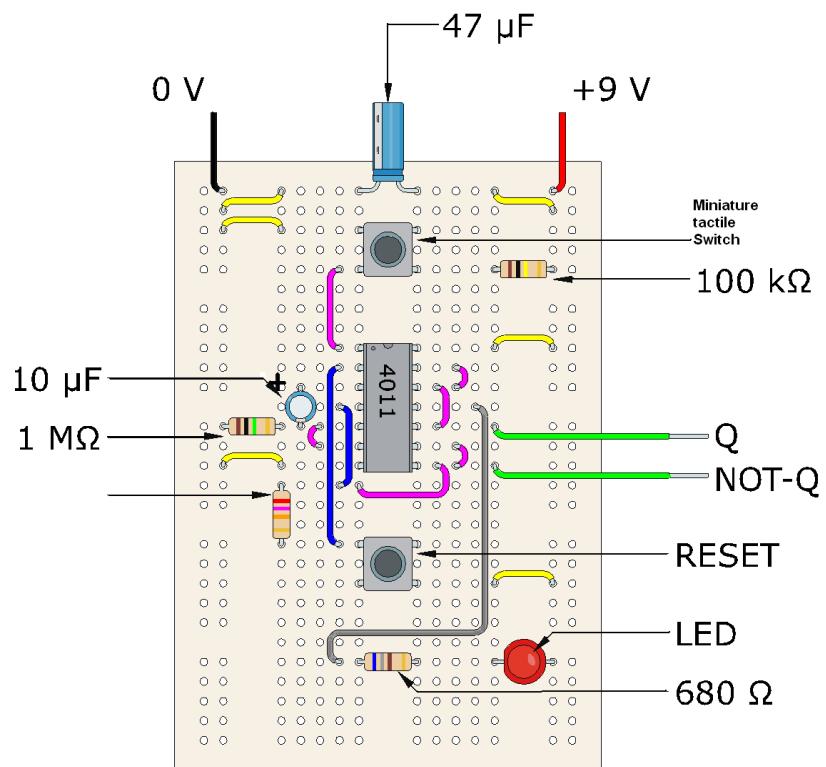
Table 16

- Note: It may be necessary to carry-out IC pin test (refer to IC config) to determine the actual fault if any from the IC.
- 3. Carry out further test to find the fault.

Review Question:

1. For the binary counter and the count waveforms of Fig 13.5, which of the following statements is true? When counting UP, the stages trigger on:
 - a) the positive going edge of clock input and positive going edge of the preceding stage.
 - b.) the positive going edge of clock input and negative going edge of the preceding stage.
 - c.) the negative going edge of clock input and negative going edge of the preceding stage.
 - d.) the negative going edge of clock input and positive going edge of the preceding stage.
2. For the binary counter and the count waveforms of Fig 13.5, which of the following statements is true? When counting DOWN, the stages trigger on:
 - a.) the positive going edge of clock input and positive going edge of the preceding stage.
 - b.) the positive going edge of clock input and negative going edge of the preceding stage.
 - c.) the negative going edge of clock input and negative going edge of the preceding stage.
 - d.) the negative going edge of clock input and positive going edge of the preceding stage.
3. For the binary counter, which of the following statements is true? An indication of a 'carry' (CY) signal is represented by:
 - a.) a positive pulse when counting UP at decimal count change 15 - 0.
 - b.) a negative pulse when counting UP at decimal count change 15 - 0.
 - c.) a positive pulse when counting DOWN at decimal count change 0 - 15.
 - d.) a negative pulse when counting DOWN at decimal count change 0- 15.
4. Modify the circuit so it counts from 0 to 6.

Exercise 13: Analog Switch and Multivibrator IC Circuits

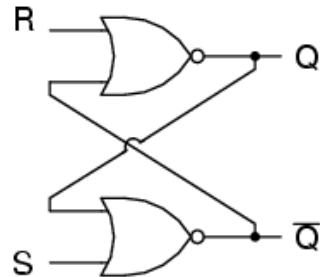


Objectives:

1. Recognize the operation of an astable, a monostable and a bistable circuit.
2. Observe the operation of an analog switch, an S-R latch and an astable circuit.
3. Predict the behavior of an analog switch and S-R latch circuits under known input conditions.
4. Determine the unstable and stable state duration for a monostable multivibrator circuit.
5. Diagnose faults in analog switch and S-R latch circuits.
6. Diagnose faults in astable and monostable multivibrator circuits.

Discussion:

The S-R latch

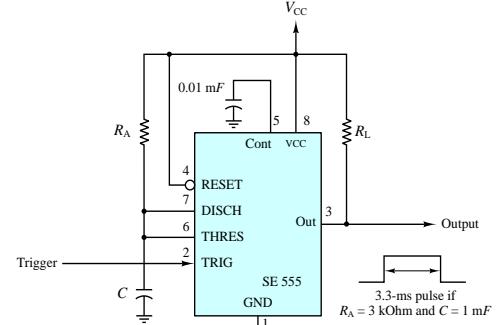


A bistable multivibrator has two stable states, as indicated by the prefix bi in its name. Typically, one state is referred to as set and the other as reset. The simplest bistable device, therefore, is known as a set-reset, or S-R, latch.

S	R	Q	\bar{Q}
0	0	latch	latch
0	1	0	1
1	0	1	0
1	1	0	0

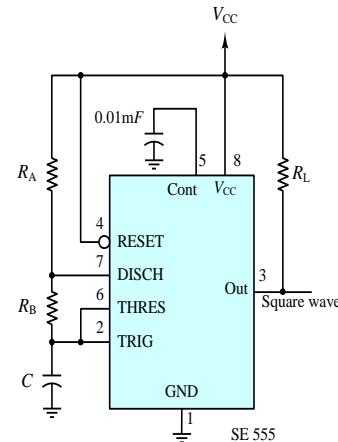
Monostable Multivibrator

A monostable multivibrator has one energy storing element in its feedback paths, resulting in one stable and quasi-stable state. It can be switched, or triggered, to its quasi-stable state; then returns to the stable state after the time delay.



Astable Multivibrator

An astable or free-running multivibrator has two energy-storing element in its feedback paths, resulting in two quasi-stable state. It continuously switches between these two states without external excitation.



Circuit Diagram:

Part 1: S – R Latch bistable

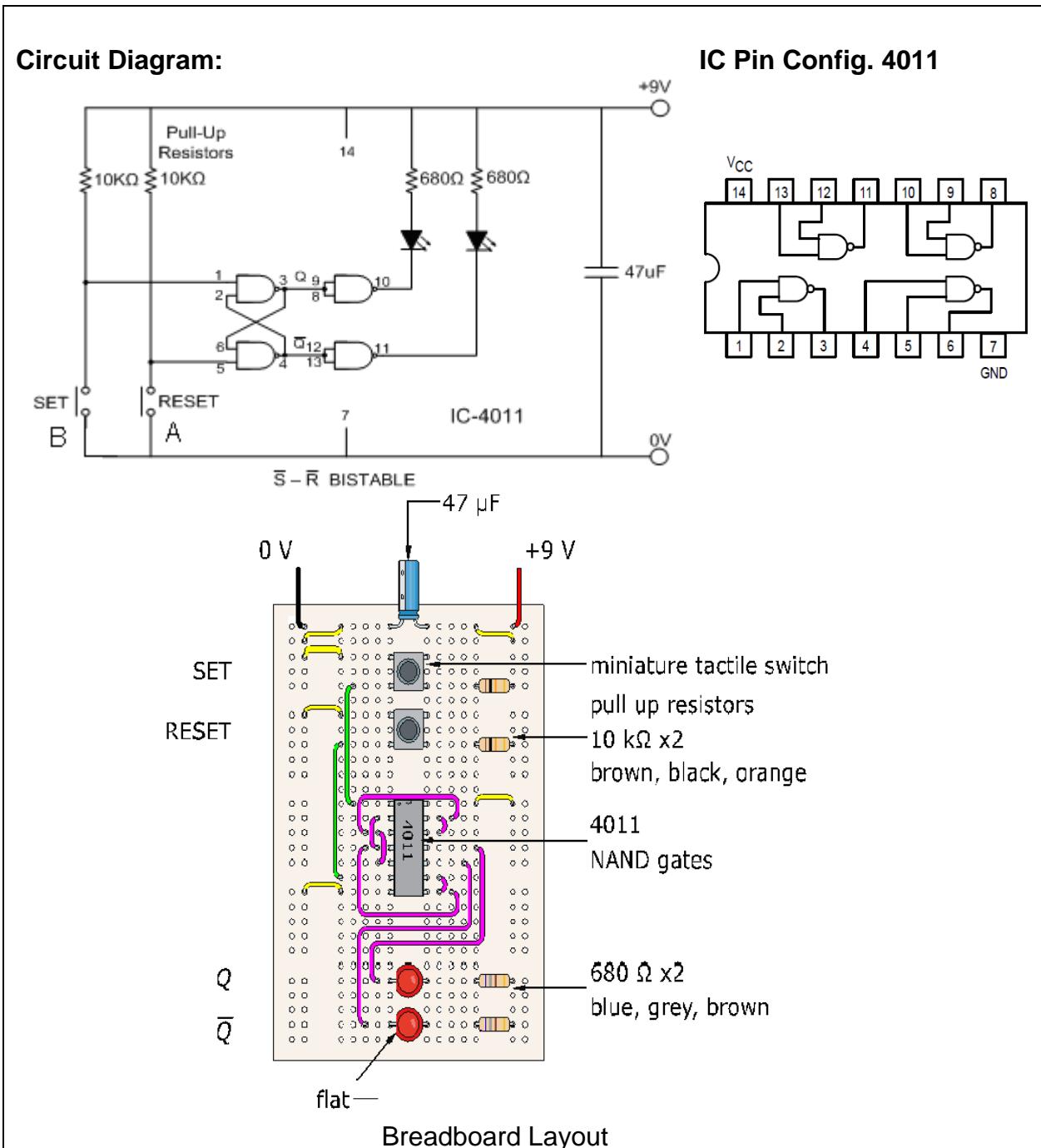


Figure 51

Equipment:

No.	Description	Qty.
1	IC 4011	1pc
2	Resistor 680 ohms	2pcs
3	Resistor 10 kΩ	2pcs
4	Capacitor 47µF	1pc
5	Breadboard	1pc
6	Connecting wires	1pc
7	Function Generator	1pc
8	LED	2pcs
9	Multimeter	1pc
10	Miniatot tactile switch	2pcs

Procedure 1

1. Connect the circuit as shown in Figure 51
2. Set switches A and B to ON.
 - **Note** the effect of alternately setting switch A to logic 0 and back to logic 1, then switch B to logic 0 and back to logic 1. You should note that operation of switch A resets the Q output to logic 0 and switch B sets the Q output to logic 1. Once set, and with both inputs at logic 1, the output state is stable in one of the two states shown in the first two rows of Table
3. Switch the power supply ON.
4. Complete the truth table for the circuit for the settings shown in Table 17.

B S	A R	LED		LED	
		Q	Q+	Q	Q+
1	1	1		0	
1	1	0		1	
1	0	1		0	
1	0	0		1	
0	1	1		0	
0	1	0		1	
0	0	1		0	
0	0	0		1	

Table 17

Procedure 2: Fault Diagnosis of S-R bistable

The fault diagnosis procedure should therefore be as follows:

1. Take readings at the test points as instructed in the worksheet.
2. Identify the possible faults from consideration of the readings obtained.
3. Carry out further tests (at the IC pins if necessary) to confirm the actual fault. IC pins configuration should be consulted for the IC pin numbers. LED's can be ignored as far as fault diagnosis is concerned - their function is only to act as indicators.

Ensure that you carry out your measurements on the correct IC number and at the correct pin numbers of that IC. When taking measurements at IC pins, take care not to short-circuit adjacent pins.

Circuit Diagram:

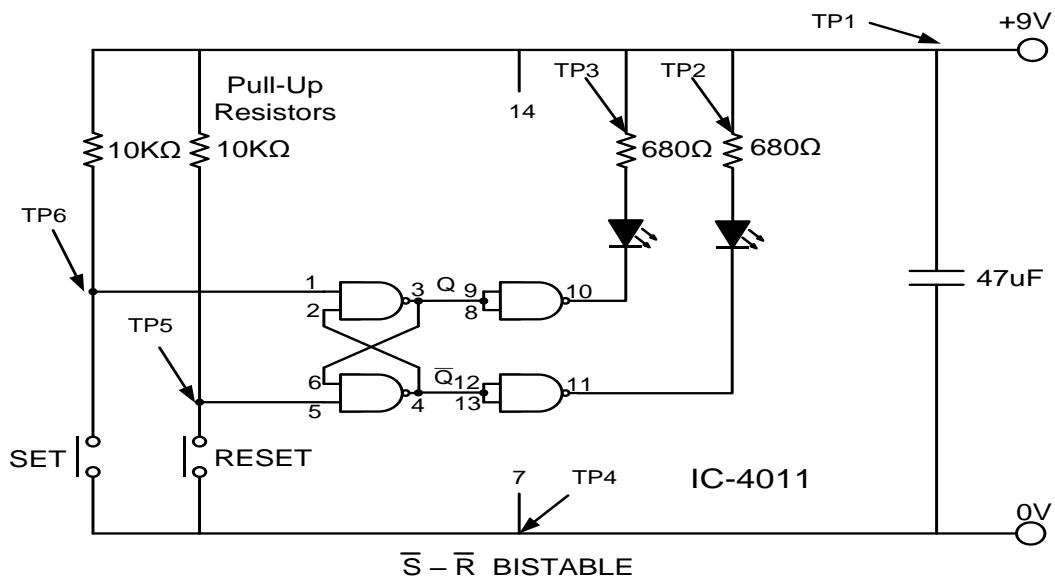


Figure 52

Procedure:

1. Connect the circuit diagram as shown in Figure 52.
 2. Switch the power supply ON, test and fill-up the Table 18

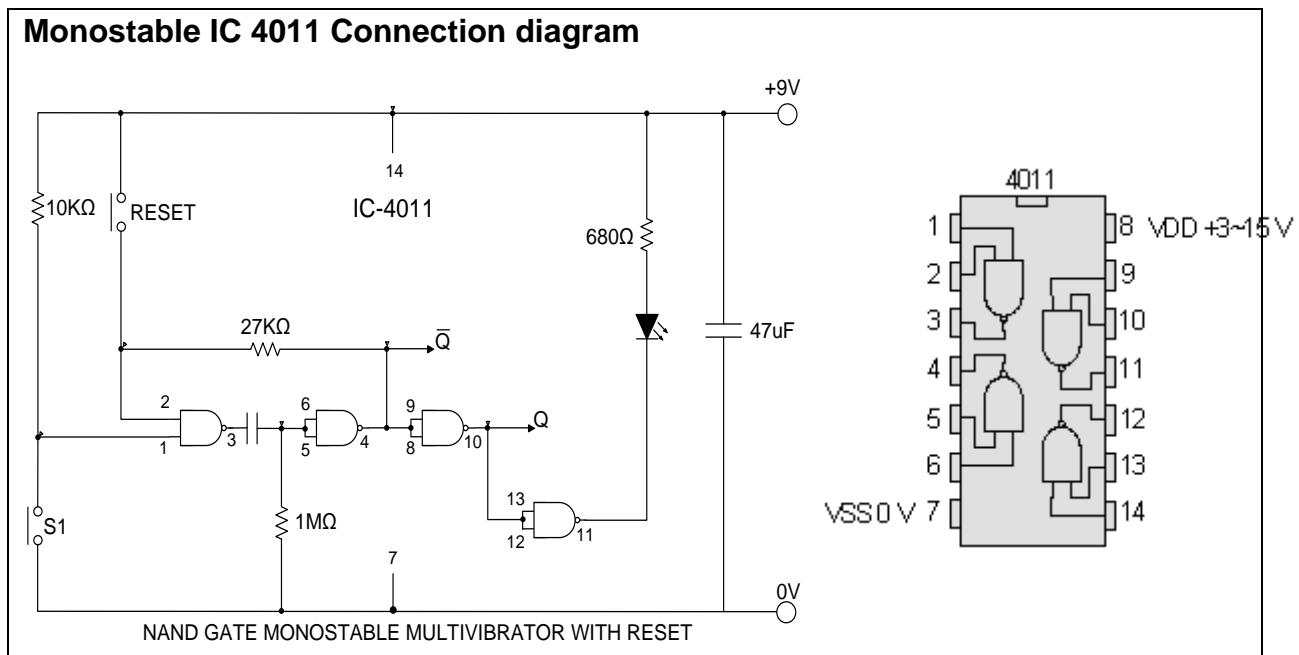
Sr no.	Component Testing	Std Values	Voltage
1	R1		
2	R2		
3	R3		
4	R4		
5	IC 4011		
9	S-switch	Contacts	
10	R-switch	Contacts	
11	TP1		
12	TP2		
13	TP3		
14	TP4		
15	TP5		
16	TP6		

Table 18

- Note: It may be necessary to carry-out IC pin test (refer to IC config) to determine the actual fault if any from the IC.

3. Carry out further test to find the fault.

Part 2: Characteristics of a Monostable Multivibrator



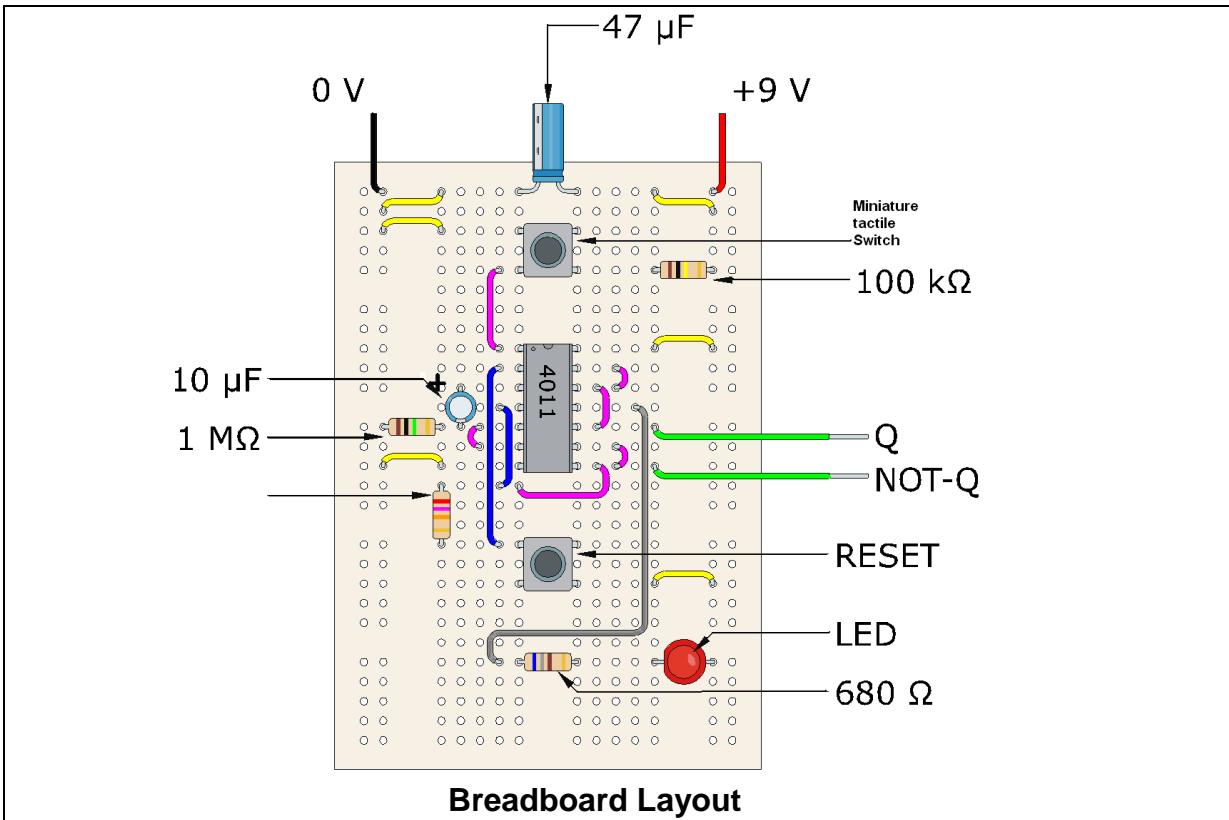


Figure 53

Equipment:

No.	Description	Qty.
1	IC 4011	1 pc
2	Resistor 680 ohms	1 pc
3	Resistor 100 kΩ	1 pc
4	Resistor 1MΩ	1 pc
5	Capacitor 47μF	1 pc
6	Capacitor 10μF	1 pc
7	Breadboard	1 pc
8	Connecting wires	1 set
9	Function Generator	1 pc
10	LED	1 pc
11	Multimeter	1 pc
12	Miniator tactile switch	1 pc

Procedure 1:

1. Connect the circuit as shown in Figure 53
2. Switch the Module Power Supplies ON and note the states of the monostable outputs Q & \bar{Q} . You will note that Q is at logic level 0 and \bar{Q} at logic level 1. This is the stable state of the circuit.

3. Press the single shot clock push button to initiate an active low trigger signal to the monostable circuit and note the effect on the output states. You will note that the Q output changes to logic level 1 for a short time as indicated by a brief 'blip' on monitor LED W. This is the unstable state and occurs each time the single shot clock button is pressed.
4. Set up the Oscilloscope as follows:
5. Time base control to 2.0ms/div, trigger selector to AC, dual trace operation.
6. CH. 1 Y amplifier gain to 2V/div, DC input.
7. CH.2 Y amplifier gain to 2V/div, DC input.
8. Positions the CH.1 trace 3 divisions down from the top of the display.
9. Position the CH.2 trace 1 division up from the bottom of the display.
10. Set the Signal generator to 50Hz, square wave, 12Vpeak-to-peak amplitude (+12V and 0V voltage levels)

11. Set the Signal generator to 50Hz, square wave, 12Vpeak-to-peak amplitude (+12V and 0V voltage levels)
12. Repeat the procedure for signal generator trigger input frequencies of 100, 150 and 200Hz, completing the Q output waveforms for each frequency in Figure 54. You will find that the duration of the unstable state remains constant for all input frequencies.

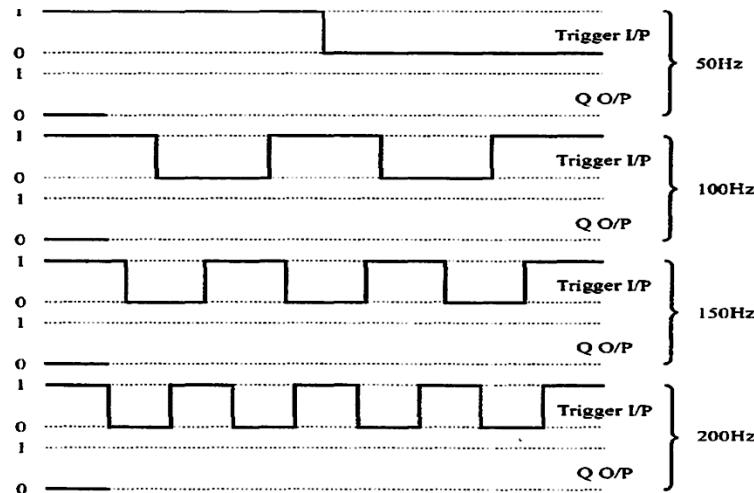


Figure 54

Procedure 2: Fault Diagnosis of Monostable multivibrator

The fault diagnosis procedure should therefore be as follows:

1. Take readings at the test points as instructed in the worksheet.
2. Identify the possible faults from consideration of the readings obtained.
3. Carry out further tests (at the IC pins if necessary) to confirm the actual fault.

IC pins configuration should be consulted for the IC pin numbers. LED's can be ignored as far as fault diagnosis is concerned - their function is only to act as indicators.

Ensure that you carry out your measurements on the correct IC number and at the correct pin numbers of that IC. When taking measurements at IC pins, take care not to short-circuit adjacent pins.

Circuit Diagram:

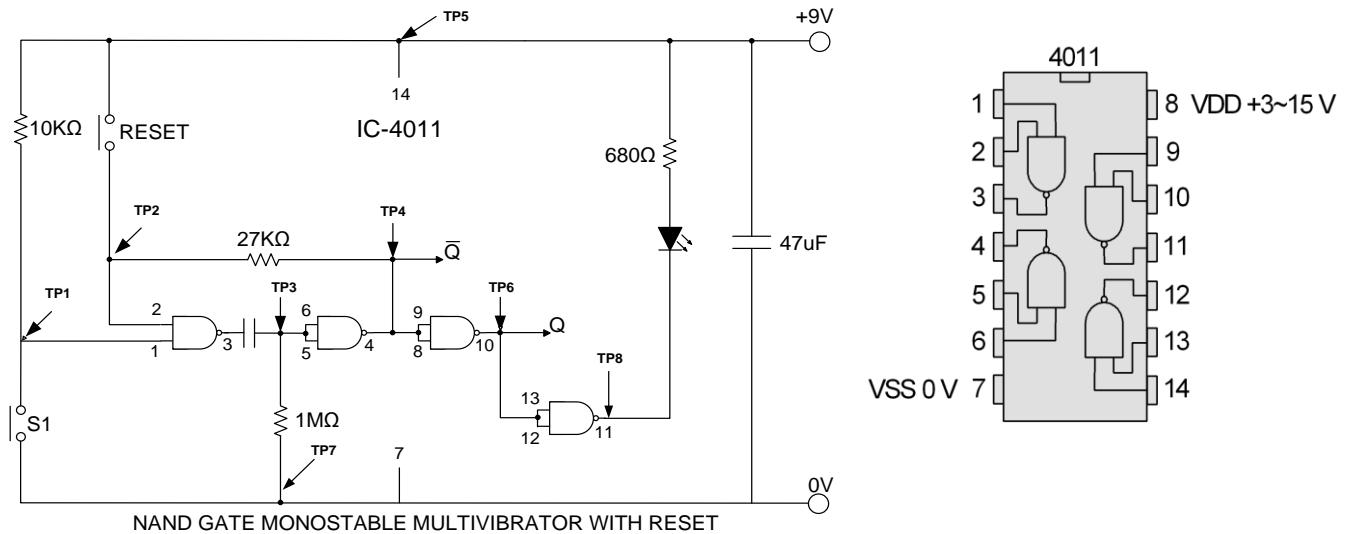


Figure 55

Procedure

1. Connect the circuit shown in the diagram in Figure 55.
2. Switch the power supply ON, test and fill-up the Table 19.

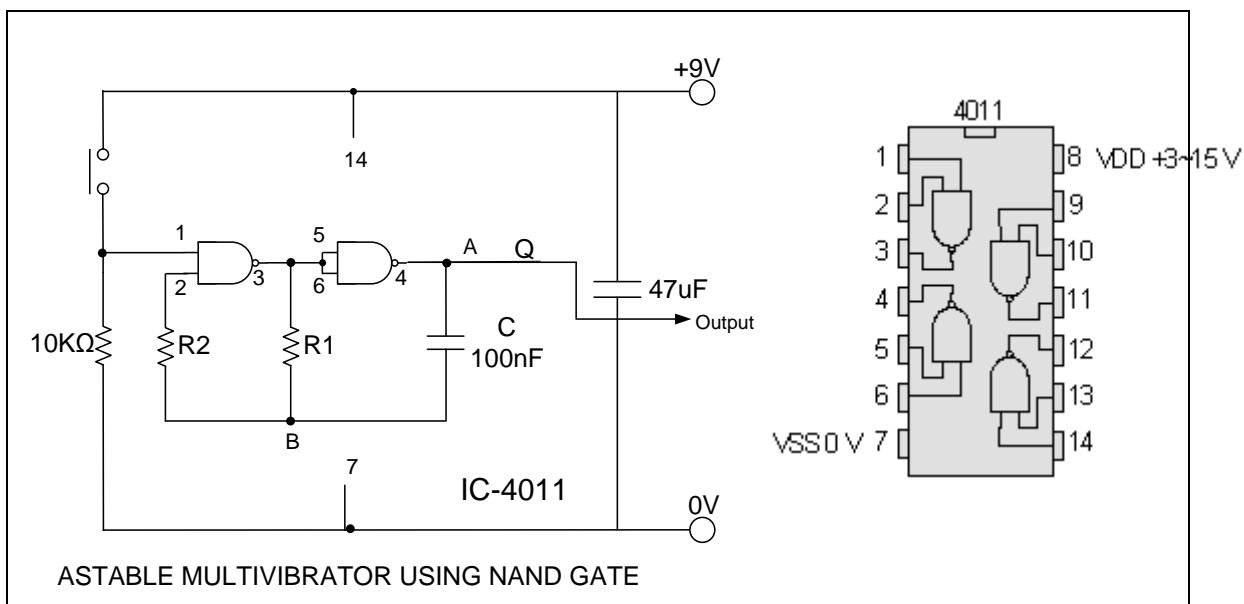
Sr no.	Component Testing	Std Values	Voltage
1	R1		
2	R2		
3	R3		
4	R4		
5	IC 4011		
9	S1-switch	Contacts	
10	R-switch	Contacts	
11	TP1		
12	TP2		
13	TP3		
14	TP4		
15	TP5		
16	TP6		
17	TP7		
18	TP8		

Table 19

- Note: It may be necessary to carry-out IC pin test (refer to IC config) to determine the actual fault if any from the IC.

3. Carry out further test to find the fault.

Part 3 Characteristics of an Astable IC (4011)



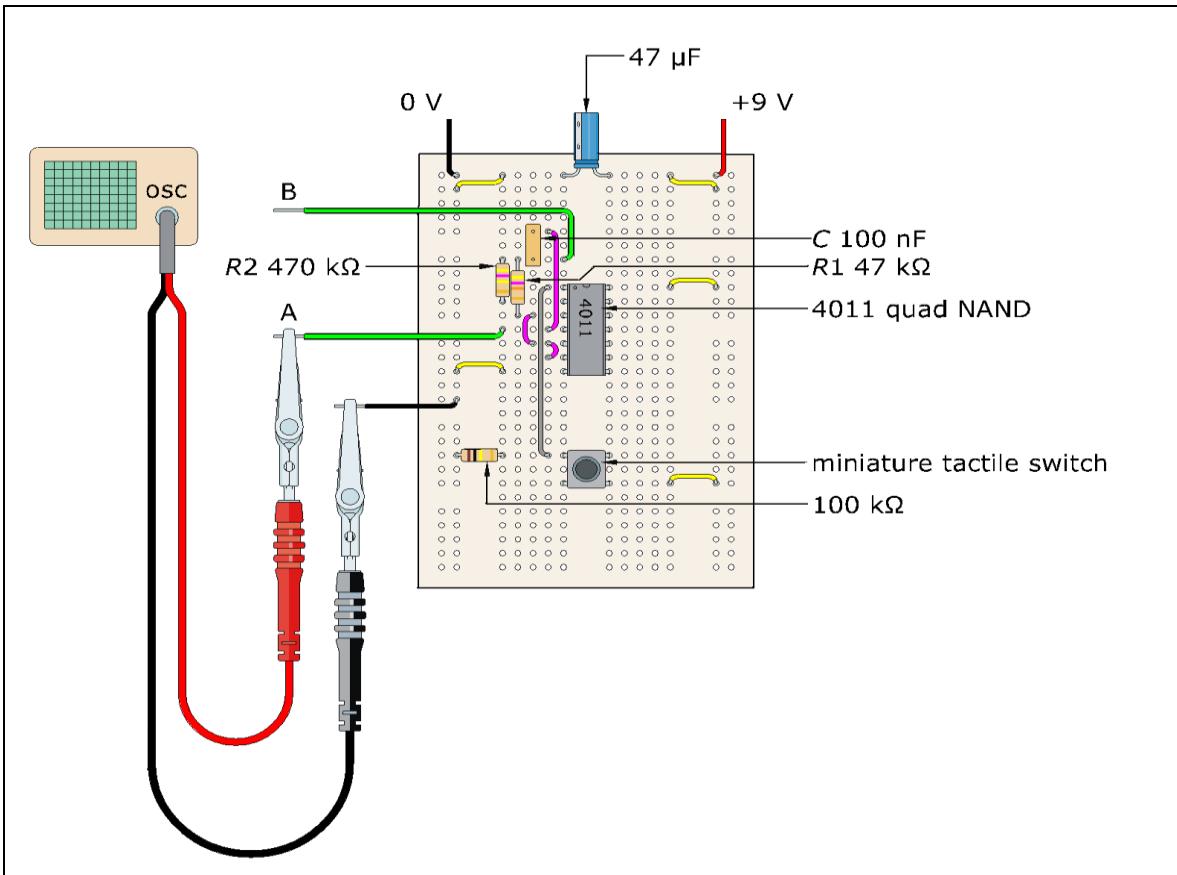


Figure 56

Equipment:

No.	Description	Qty.
1	IC 4011	1pc
2	Resistor 47k ohms(R1)	1pc
3	Resistor 470 kΩ (R2)	1pc
4	Resistor 100kΩ	1pc
5	Capacitor 47μF	1pc
6	Capacitor 100nF	1pc
7	Breadboard	1pc
8	Connecting wires	1 set
9	Function Generator	1pc
10	LED	1pc
11	Multimeter	1pc
12	Miniatior tactile switch	1pc
13	Oscilloscope	1pc

Procedure 1:

1. Connect the circuit as shown in Figure 56
2. Set the oscilloscope controls as follows:
 - Timebase control to 0.2ms/div, trigger selector to AC, dual trace operation.
 - CH. 1 Y amplifier gain to 2V/div, DC input.
 - CH.2 Y amplifier gain to 2V/div, DC input.
 - Position the CH. 1 trace across the center of the screen.
 - Position the CH. 2 trace across the bottom line of the screen.
3. With the astable frequency control set to 1Hz, switch the Module Power Supplies ON and observe the output states Q, Q and 2Q as indicated by the monitor LED's W, X & Z. The outputs Q and Q should be constantly changing between logic levels 0 & 1 at approximately one second intervals, with the Q output the inverse of Q. The output 2Q changes at a frequency which is double that for Q.
4. Set the astable frequency control to 1kHz and study the CH.1 and CH.2 waveforms on the oscilloscope, CH.1 representing the Q output and CH. 2 representing the Q output.

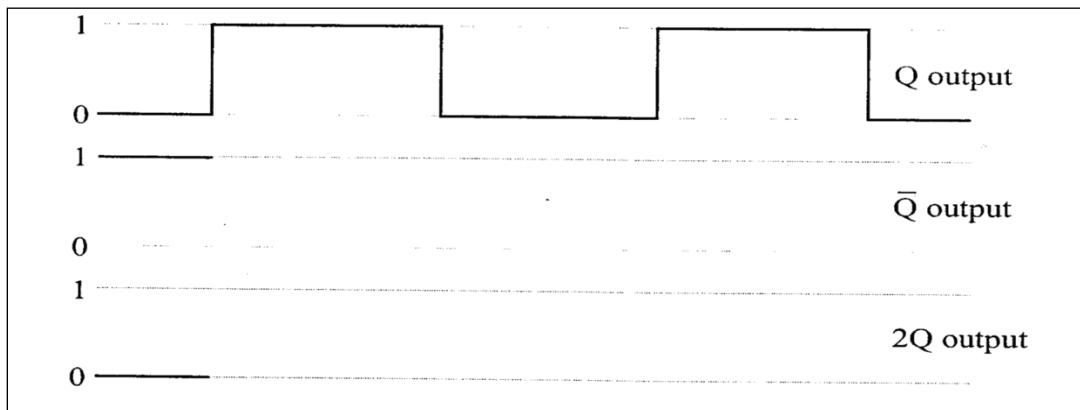


Figure 57

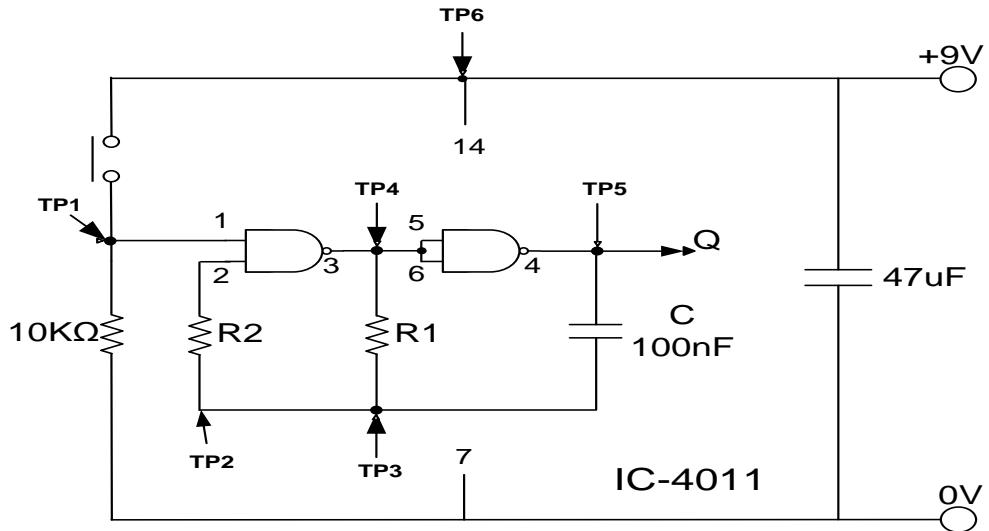
Procedure 2: Fault Diagnosis of Astable Multivibrator

The fault diagnosis procedure should therefore be as follows:

1. Take readings at the test points as instructed in the worksheet.
2. Identify the possible faults from consideration of the readings obtained.
3. Carry out further tests (at the IC pins if necessary) to confirm the actual fault. IC pins configuration should be consulted for the IC pin numbers. LED's can be ignored as far as fault diagnosis is concerned - their function is only to act as indicators.

Ensure that you carry out your measurements on the correct IC number and at the correct pin numbers of that IC. When taking measurements at IC pins, take care not to short-circuit adjacent pins.

Circuit Diagram:



ASTABLE MULTIVIBRATOR USING NAND GATE

Figure 58

Procedure

1. Connect the circuit shown in the diagram.
2. Switch the power supply ON, test and fill-up the Table 20

Sr no.	Component Testing	Std Values	Voltage
1	R1		
2	R2		
3	R3		
4	R4		
5	IC 4011		
9	S1-switch	Contacts	
11	TP1		
12	TP2		
13	TP3		
14	TP4		
15	TP5		
16	TP6		

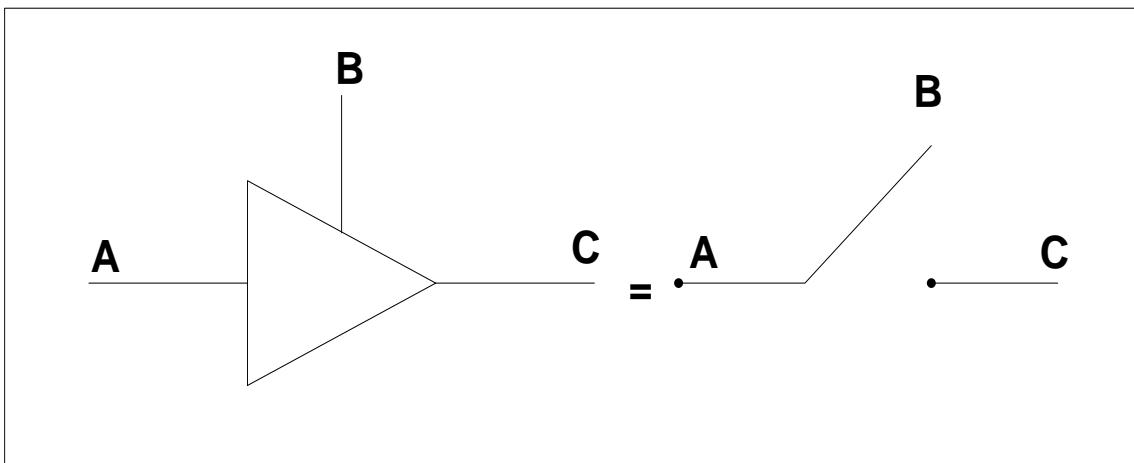
Table 20

- Note: It may be necessary to carry-out IC pin test (refer to IC config) to determine the actual fault if any from the IC.
- 3. Carry out further test to find the fault.

Review Question:

1. For the analog switch used in this exercise, which of the following statements is true?
 - a) With the Select at logic 0, the output voltage is OV.
 - b) With the Select at logic 0, the output voltage corresponds with input A.
 - c) With the Select at logic 0, the output voltage corresponds with input B.
 - d) With the Select at logic 1, the output voltage corresponds with input A.
2. For the S-R latch used in Figure 51, with the inputs both set to logic 0, the Q , \bar{Q} will be:
a) 0,0 b) 0,1 c) 1,0 d) 1,1

Exercise 14: Three-State Logic Circuits

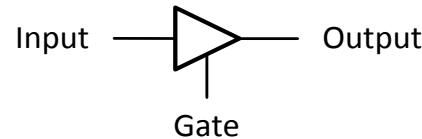


Objectives:

- To determine the logic states for three state logic gate circuits.
- To figure out truth tables for three-state logic circuits.
- Diagnose faults in a three state bi-directional switch circuit.

Discussion:

Three-state logic circuits are circuits where the output can be in one of three possible states: logic level 0, logic level 1 or completely isolated from the internal circuit. The symbol and truth table for the three-state logic device are shown in Figure 59.



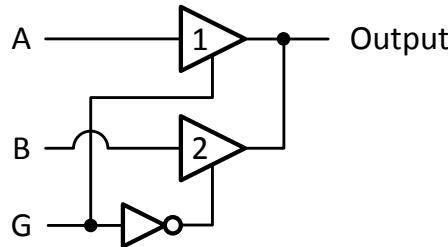
Input	Gate	Output
0	0	Disconnected
0	1	0
1	0	Disconnected
1	1	1

Figure 59

With the gate input at logic level 0, the output is isolated from the circuit. With the gate input at logic level 1, the data at the input is fed to the output.

Note that data flow is one way only, in the direction of input to output.

Figure 60 shows a circuit with two three-state devices connected as a 2-1 Multiplexer.



A	B	Gate	Output
1	0	0	1
1	0	1	0
0	1	0	0
0	1	1	1

Figure 60

With the gate input G at logic 0, the three-state device 1 will be disabled and device 2 will be enabled, since its gate input will be at logic level 1. The output will therefore correspond with the input B to device 2.

Similarly, with the gate input G at logic 1, device 1 will be enabled and device 2 will be disabled. The output will then correspond with the state of input A.

Circuit Diagram:

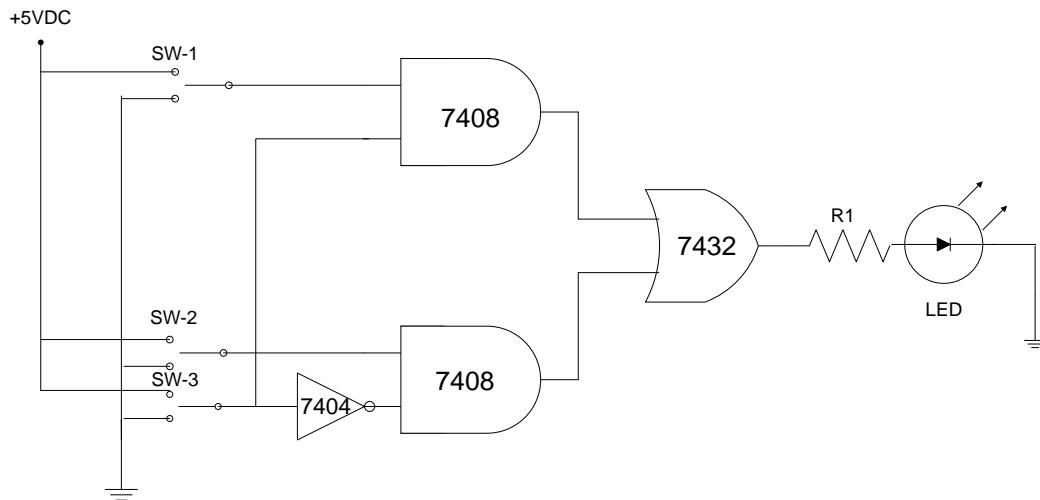


Figure 61: Simplified Three State Logic Circuit

Equipment:

No	Name	Qty
1	Breadboard	1 pc
2	AND Gate 7408 IC	1 pc
3	OR Gate 7432 IC	1 pc
4	Hex Inverter 7404 IC	1 pc
5	LED (use as indication)	1 pc
6	Resistors 250 Ω	1 pc
7	Short links and connecting leads	-----
8	Multimeter	1 pc

Procedure:

1. Assemble the circuit as shown in the diagram Figure 61.
2. With the bread board power supplies ON, obtain the truth table for the circuits, setting the inputs as shown in Table 21.

B	A	Gate	O/P
1	0	0	
1	0	1	
0	1	0	
0	1	1	

Table 21

Trouble Shooting:

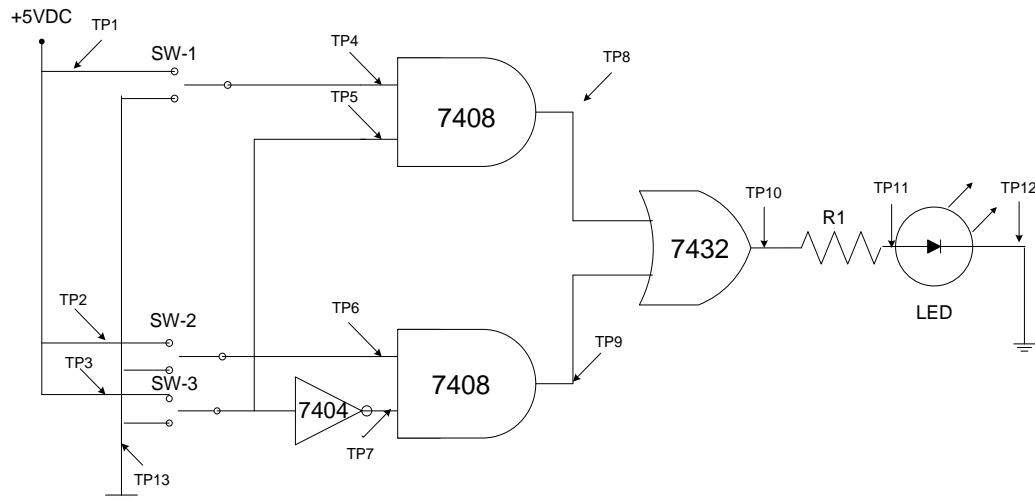


Figure 62

Procedure:

1. Set logic inputs base on the Table 21 and verify the output through logic monitor or LED.
2. Initiate fault and perform voltage check in every test point as shown above.
3. Record the voltage reading in the table provided below during normal condition and during the fault condition.

Test Points	Voltage Reading:		Test Points	Voltage Reading	
	Normal Condition	Fault Condition		Normal Condition	Fault Condition
TP1			TP7		
TP2			TP8		
TP3			TP9		
TP4			TP10		
TP5			TP11		
TP6			TP12		

Table 22

Review Questions:

1. Explain the characteristic of three state logic circuits.
2. For the circuit used in this exercise, the output is at logic level 1. A possible input state is:
 - a) B=1, A=0, G=0
 - b) B=1, A=0, G=1
 - c) B=0, A=1, G=0
 - d) A=0, B=0, G=1

Exercise 15: D/A and A/D Converter Circuit

Objective:

- To understand the basic principles of Digital – Analog and Analog – Digital conversion system.
- Diagnose faults in D-A converter and A-D converter circuits.

Discussion:

The real world consists mostly of analog variables like temperature, speed, sound, etc. In order to interface these variables with a digital circuit or a computer and vice versa, we need to convert between the two systems.

There are multiple ways to convert digital signals to analog voltages. The method we will study here is called the R-2R method.

In this method, each digital input is fed into a series of repetitive arrangement of resistors as shown in Figure 63. This arrangement gives each digital input a weighted contribution to the output analog signal. The 3rd bit for example passes through 2R only, while the first bit has to go through two additional R resistors before it reaches the output.

$$\text{The output voltage due to an input } V_i \text{ at } B_0 = \frac{V_{B0}}{16}$$

$$\text{The output voltage due to an input } V_i \text{ at } B_1 = \frac{V_{B1}}{8}$$

$$\text{The output voltage due to an input } V_i \text{ at } B_2 = \frac{V_{B2}}{4}$$

$$\text{The output voltage due to an input } V_i \text{ at } B_3 = \frac{V_{B3}}{2}$$

The resultant output voltage is the sum of these individual values.

With the digital input levels to B0-B3 either 0 or 1, the output V_o is given by:

$$V_{OUT} = \frac{V_{B0}}{16} + \frac{V_{B1}}{8} + \frac{V_{B2}}{4} + \frac{V_{B3}}{2}$$

The output of the R-2R resistor network has a fixed range (0-3 or 0-2 volts). In order to change that range, the analog output needs to be fed to an operational amplifier. The values of R_f , +V and -V decide the amount of amplification and range the DAC can work with.

The R-2R DAC has a few advantages over other methods. These include:

- Easily scaled to any number of bits
- Easy to manufacture and build because it requires only 2 resistor values

Circuit Diagram:

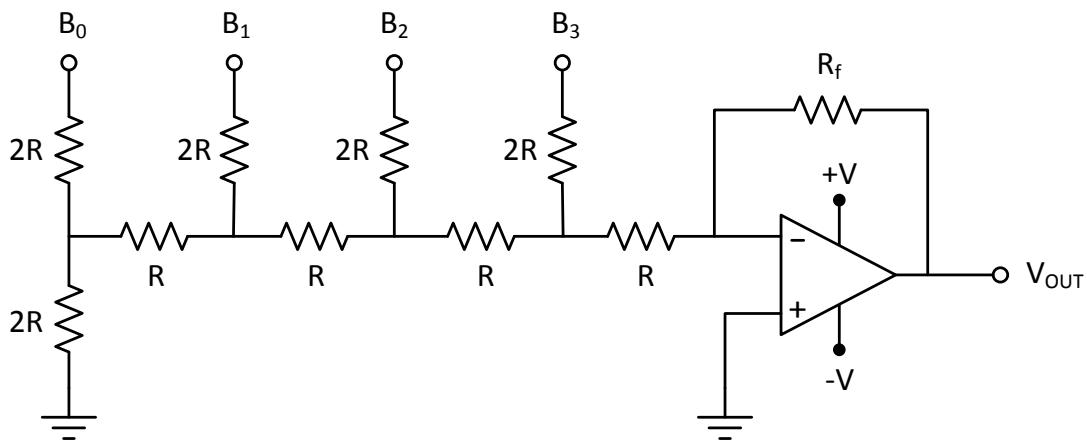


Figure 63: R-2R Digital to Analog Converter

Equipment:

Sr.	Description:	Qty.
1	Bread board	1 pc.
2	Multimeter	1 pc.
3	IC 741	1 pc.
4	Resistors	4 pcs.
5	Connecting leads	-----

Procedure:

1. Assemble the circuit as shown in Figure 63. Set the multimeter to DC voltage range.
2. Set the input B0 – B3 and refer to Table 23 for possible input settings.
3. With the bread board power supply on, measure the output voltages Vo and record the results in Table 23.

Observation Table:

B3	B2	B1	B0	V _O
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Table 23

Trouble Shooting Guide:

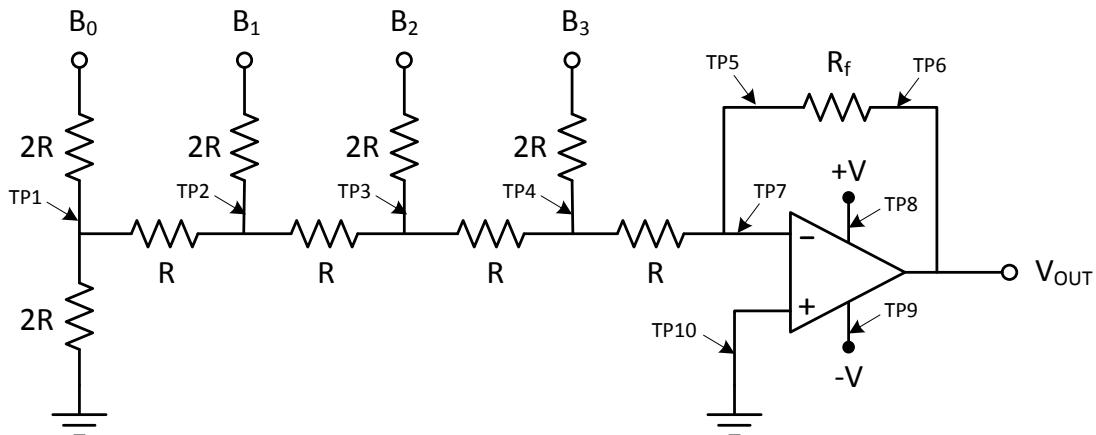


Figure 64: D-A Converter Circuit and Test Points

Procedure:

- Set the input B0-B3. Refer to Table 23 for possible input settings.
- With the bread board power supply ON, set the multimeter at DC voltage range and measure the output voltage V_o .
- Initiate fault condition, for example apply false input values.
- Measure the parameters as shown in the diagnosis Table 24, record the standard and measured values for reference.
- Write in your conclusion the type of faults encountered in this exercise and what are the actions taken to rectify the faults.

Diagnosis Table:

Parameters	Std. Values	Measured Values
TP1		
TP2		
TP3		
TP4		
TP5		
TP6		
TP7		
TP8		
TP9		
TP10		

Table 24

Conclusion:

Type of fault _____

Action Taken _____

Analog to Digital Conversion:

Discussion:

An analog to Digital (A-D) converter uses a D-A converter, a binary counter, a comparator and an AND gate. The circuit for a 4-bit, incremental type, A-D converter is shown below.

The analog input voltage is applied to the positive (+) input of the comparator with the negative (-) input being fed by the D-A converter.

The output of comparator is fed to one input of the AND gate, whose other input is fed by a constant stream of clock pulses.

Under initial conditions the binary Counter is reset to Zero (0000). This sets the output of the D-A converter to zero volts.

With zero volts on the negative input of the comparator and an analog input voltage of greater than zero volts on the positive input, the comparator output is set to logic level 1.

This applies a logic level 1 to the AND gate and enables it. Every time there is a clock pulse, a pulse is fed from the output of the AND gate to the input of the Binary Counter, which counts up in sequence (0001, 0010, 0011 etc).

The output voltage from the D-A converter increases in steps as the count increases and at the step when its output exceeds the value of the analog input voltage, the comparator output will change to logic level 0.

This disables the AND gate and no further pulses will be fed to the counter.

The value in the Binary Counter is held and is the digital equivalent of the analog input voltage.

Circuit Diagram:

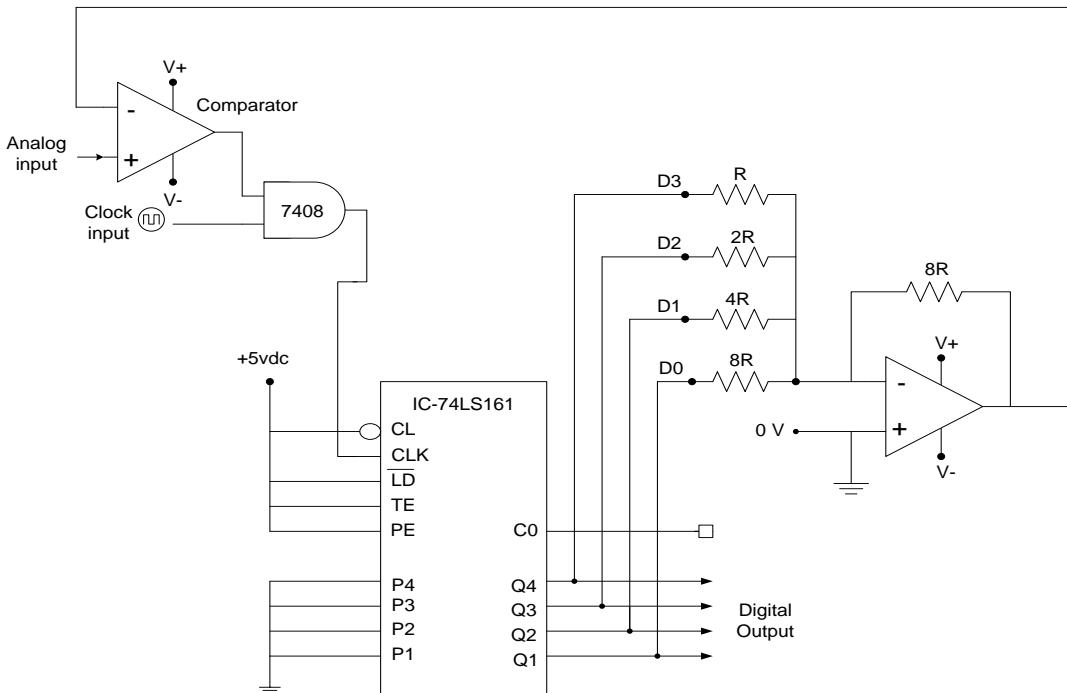


Figure 65: Analog to Digital Converter

Equipment:

Sr no.	Description	Qty.
1	Bread board	1 pc.
2	Multimeter	1 pc.
3	Frequency Generator	1 pc.
4	Comparator IC	1 pc.
5	AND gate IC 7408	1pc.
6	Binary counter 74LS161	1 pc.
7	D-A Conv IC 426	1 pc.
8	Connecting leads	-----

Procedure:

1. Assemble the circuit as shown in Figure 65.
2. Set the multimeter to Dc voltage and set the frequency generator to 1HZ.
3. Set the binary counter RESET (CL) to logic level 0, switch the power supplies on.
4. Set the analog input voltage to 6.75V (connect the multimeter positive lead to the analog input terminal and initiate the counter RESET process by briefly applying a logic level 1. The counter will count UP at 1-second intervals and should stop when the output count is 1110, the voltmeter indicating 7.0V).
5. Reduce the analog input voltage to 4.5V and again reset the counter. The counter should count up to 1,0,1,0 (Q4, Q3, Q2, Q1) and stop, the voltmeter indicating 5.0V.
6. Repeat the procedure for the other input voltage settings given in Table 25 to become familiar with the operation of the system, bearing in mind that the 4-bit D-A converter voltage resolution is in steps of .5V.

Input	D3	D2	D1	D0	Vo
7.25V					
6.75V					
6.25V					
5.75V					
5.25V					
4.75V					
4.25V					
3.75V					
3.25V					
2.75V					
2.25V					
1.75V					
1.25V					
0.75V					
0.25V					
0V					

Table 25

Trouble Shooting:

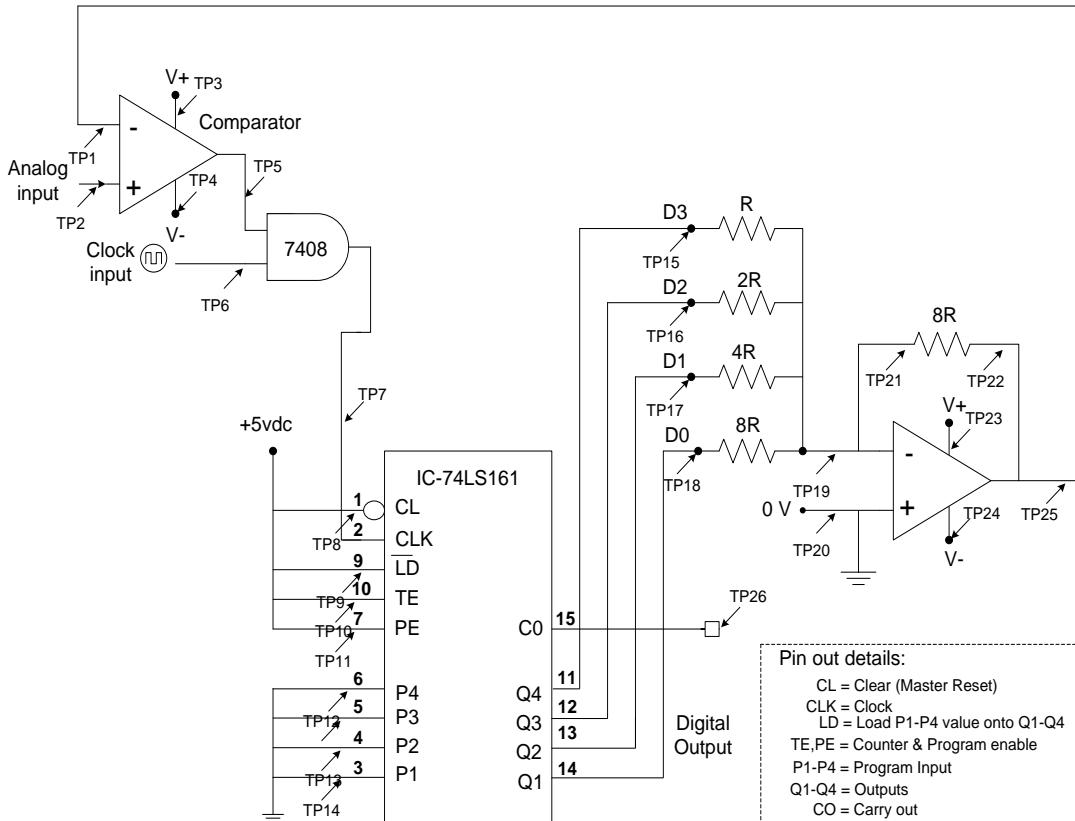


Figure 66: A-D Converter Circuit and Test Points

Procedure:

1. Set the analog input based on Table 26 and measure the voltage output V_o (Figure 66)
2. Initiate false condition, for example open circuit at any of the program inputs P1-P4.
3. Measure the parameters shown in diagnosis Table 26, record the standard and measured values for reference.
4. Write in your conclusion the type of faults encountered in this exercise and what are the actions taken to rectify the faults.

Parameters	Std. values	Measured values
TP1		
TP2		
TP3		
TP4		
TP5		
TP6		
TP7		
TP8		
TP9		
TP10		
TP11		
TP12		
TP13		
TP14		
TP15		
TP16		
TP17		
TP18		
TP19		
TP20		
TP21		
TP22		
TP23		
TP24		
TP25		

Table 26: Diagnosis Table

Conclusion:

Type of fault _____

Action Taken _____

Review Questions:

1. A 4-bit D-A converter has its maximum output voltage set at 12V. The output voltage for a binary input D3, D2, D1, D0 of 1,0,1,0 is:
a) 7.2V b) 7.5V c) 8V d) 10V
2. A 4-bit D-A converter has its maximum output set at 9V. For an output voltage of 3V the binary input D3, D2, D1, D0 is:
a) 0, 1, 1, 0 b) 0,1,0,1 c) 0,1,0,0 d) 0,1,1,1
3. A 4-bit D-A converter has its maximum output voltage set at 10V. For an output voltage of 4V the binary input D3, D2, D1, D0 is:
a) 0, 1, 1, 0 b) 0,1,0,1 c) 0,1,0,0 d) 0,1,1,1
4. A-bit A-D converter has an input voltage range 0-7.5V. For an input voltage of 6.1V the binary output D3, D2, D1, D0 is:
a) 1,0,1,1 b) 1,1,0,0 c) 1,1,0,1 d) 1,1,1,0
5. A 4-bit A-D converter has an input voltage range 0-12V. For an input voltage of 5V the binary output D3, D2, D1, D0 is:
a) 0,1,1,0 b) 0,1,0,1 c) 0,1,0,1 d) 0,1,1,1
6. A 4-bit A-D converter has an input voltage range 0-5V. For an input voltage of 2.9V the binary output D3, D2, D1, D0 is:
a) 1,0,0,0 b) 1,0,0,1 c) 1,0,1,0 d) 1,0,1,1
7. A 4-bit A-D converter has a clock frequency of 1khz and input range of 0-7.5V. The minimum conversion time for an input voltage of 7.5V is:
a) 7.5ms b) 10ms c) 15ms d) 20ms
8. For the A-D circuit used in this exercise, the analog input voltage set to 2.25V, the voltage indicated by the voltmeter will be:
a) 2.5V b) 0V c) 5.0V d) 6.5V

Unit 4: Optoelectronics

Exercise 16: State Indicators

Objective:

- To determine I/V characteristics of filament Lamp.

Discussion:

A state indicator is intended to provide visual evidence of the condition of a circuit. It explains the fact whether the circuit is in energized state or De-energized state. A simple example of an indicator is a filament lamp.

It is significant to consider that the operation of the filament lamp depends on the heating of a tungsten element to white-hot (incandescent) temperature. The lamp is therefore subject to thermal inertia (lag) which limits its speed of operation. It is also a non-linear resistor that requires high current for efficient operation.

Circuit Diagram:

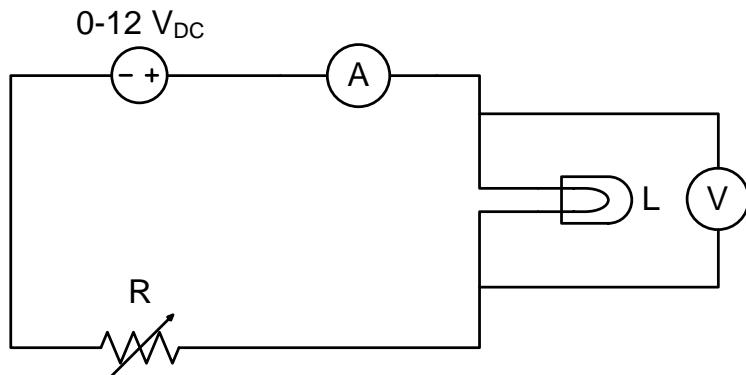


Figure 67

Equipment:

No.	Description	Qty.
1	Filament Lamp, 15V	1
2	Variable DC Power Supply, 0-12V	1
3	Variable Resistor	1
4	Voltmeter	1
5	Ammeter	1
6	Connecting wires (jumpers)	-
7	Breadboard	1

Procedure:

- Construct the circuit is shown in Figure 67 on a breadboard .
- Turn on the power.
- Measure all the corresponding voltages and currents of each voltage setting.
- Record the voltages and current in Table 27.

Observation:

Input Volts	Resistance (r)	Voltage across lamp(v)	Current I
2			
4			
6			
8			
10			
12			

Table 27

Conclusion:

Type of Fault: _____

Action Taken: _____

Troubleshooting:

Circuit Diagram:

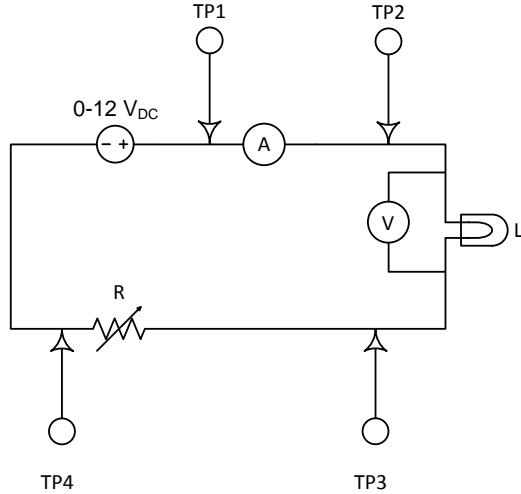


Figure 68

Procedure:

- Construct the circuit on a breadboard as shown in Figure 68.
- Turn on the power and adjust to 12 VDC.
- Measure all the corresponding voltages and currents of each voltage setting.
- Record the voltages and current on Table 28.
- A trouble shooting chart listing standard values and measured values are prepared.
- Fault is determined by comparing standard values with measured values.

Sr no.	Parameters	Std Values	Measured Values
1	Volts		
2	Current		
3	Supply		
4	TP1		
5	TP2		
6	TP3		
7	TP4,		

Table 28

Exercise 17: Bar-Graph Display

Objective:

- To appreciate the importance of display devices.
- To evaluate the operation of a bar graph display IC.

Discussion:

The LM3914 is a monolithic integrated circuit that senses analog voltage levels and drives 10 LEDs, providing a linear analog display. A single pin changes the display from a moving dot to a bar graph. Current drive to the LEDs is regulated and programmable, eliminating the need for resistors. This feature is one that allows operation of the whole system from less than 3V.

The circuit contains its own adjustable reference and accurate 10-step voltage divider. The low-bias-current input buffer accepts signals down to ground.

Equipment

No.	Description	Qty.
1	LM3914 IC	1
2	10-LED strip	1
3	1.21k resistor	1
4	3.83k resistor	1
5	2.2 μ F capacitor	1
6	Connecting wires (jumpers)	-
7	Breadboard	1

Circuit Diagram:

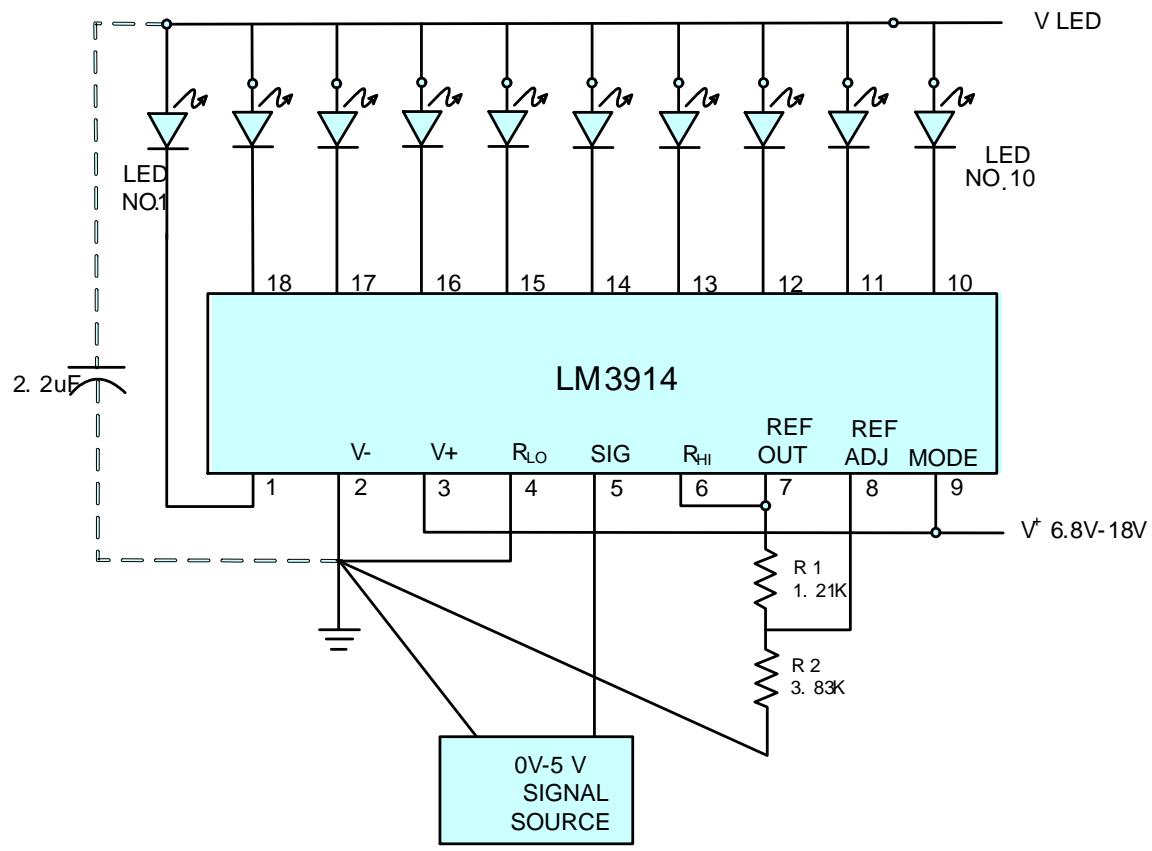


Figure 69

Procedure:

- Using the monolithic IC LM 3914, construct the circuit on a breadboard. As shown in Figure 69.
- Adjust the power supply to 12 volts and connect to pin 9 and GND of the IC.
- Connect the cathodes of LED 2 - 10 to pin 10 -18 and LED1 to pin 1 of the IC.
- A reference signal source is to be connected between pin 2 and pin 7 of the IC.
- Turn the power supply ON.
- Check for the change of indication of LED status for different values of input voltages.

Troubleshooting of Bar Graph Display:

Circuit Diagram:

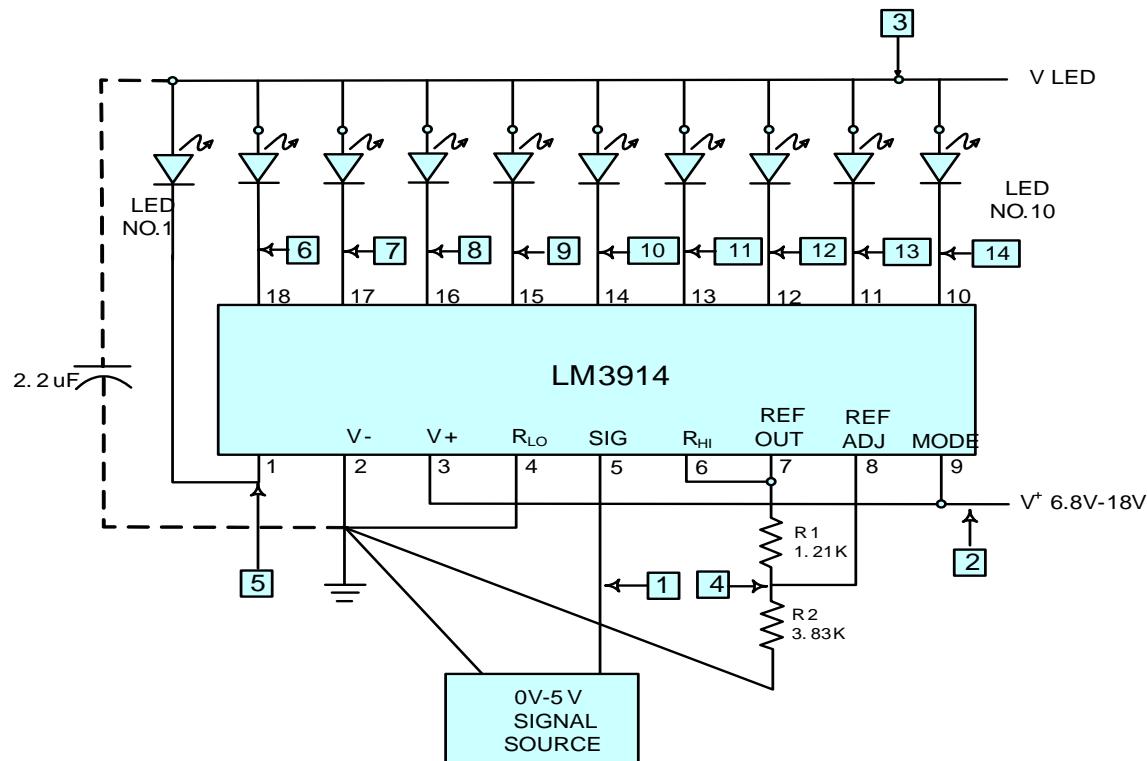


Figure 70

Procedure:

- Construct the circuit on a breadboard using the monolithic IC LM 3940. as shown in Figure 70.
- Adjust the power supply to 12 volts and connect to pin 9 and GND of the IC.
- Connect the cathodes of LED 2 - 10 to pin 10 -18 and LED1 to pin 1 of the IC.
- A reference signal source is to be connected between pin 2 and pin 7 of the IC.
- Turn the power supply ON.
- Check for the change of indication of LED status for different values of input voltages.
- Record the voltages are at the given test points on Table 29.
- Compare the standard and measured values.

Diagnosis Table:

Sr no.	Parameters	Std Values	Measured Values
1	Volts		
2	Ref Supply		
3	LEDS		
4	TP1		
5	TP2		
6	TP3		
7	TP4		
8	TP5		
9	TP6		
10	TP7		
11	TP8		
12	TP9		
13	TP10		
14	TP11		
15	TP12		
16	TP13		
17	TP14		

Table 29

Exercise 18: 7-Segment Display

Objective:

- To appreciate the importance of display devices.
- To evaluate the operation of an LCD 7-Segment display

Discussion:

A liquid crystal display (LCD) is a thin, flat panel used for electronically displaying information such as text, images, and moving pictures. Its uses include monitors for computers, televisions, instrument panels, and other devices ranging from aircraft cockpit displays, to every-day consumer devices such as video players, gaming devices, clocks, watches, calculators, and telephones. Among its major features are its lightweight construction, its portability, and its ability to be produced in much larger screen sizes than are practical for the construction of cathode ray tube (CRT) display technology. Its low electrical power consumption enables it to be used in battery-powered electronic equipment. It is an electronically-modulated optical device made up of any number of pixels filled with liquid crystals and arrayed in front of a light source (backlight) or reflector to produce images in color or monochrome.

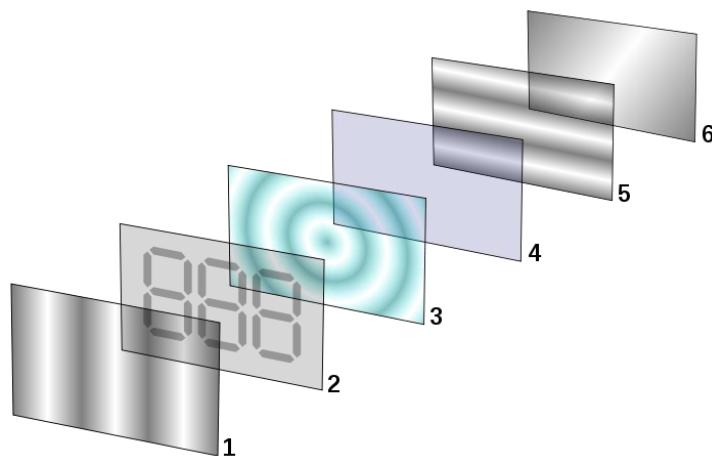


Figure 71

Reflective twisted nematic liquid crystal display.

1. Polarizing filter film with a vertical axis to polarize light as it enters.
2. Glass substrate with [ITO](#) electrodes. The shapes of these electrodes will determine the shapes that will appear when the LCD is turned ON.
Vertical ridges etched on the surface are smooth.
3. Twisted nematic liquid crystal.

4. Glass substrate with common electrode film (ITO) with horizontal ridges to line up with the horizontal filter.
5. Polarizing filter film with a horizontal axis to block/pass light.
6. Reflective surface to send light back to viewer. (In a backlit LCD, this layer is replaced with a light source.)

The LCD we will be using has a small processor that accept commands or data to be entered to the screen. The choice between command and data is determined by the bit entered in the RS input. When the RS input is 0, Table 30 shows the list of commands that can be entered through the data bits.

Command	Code										Description
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears the display and returns the cursor to the home position (address 0)
Return Home	0	0	0	0	0	0	0	0	1	X	Returns the cursor to the home position. Also returns a shifted display to the home position. DD RAM contents remain unchanged
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor move direction and enables/disables the display
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Turns the display ON/OFF (D), or the cursor ON/OFF (C), and blink of the character at the cursor position (B)
Cursor & Display Shift	0	0	0	0	0	1	S/C	R/L	X	X	Moves the cursor and shifts the display without changing the DD RAM contents
Function Set	0	0	0	0	1	DL	N\$	F	X	#	Sets the data width (DL), the number of lines in the display (L), and the character font (F)
	I/D = 1: Increment S = 1: Accompanies display shift S/C = 1: Display shift R/L = 1: Shift to the right DL = 1: 8 bits F = 1: 5 x 10 dots # Set to 1 on 24x4 modules \$ With KS0072 is Address Mode					I/D = 0: Decrement S/C = 0: Cursor move R/L = 0: Shift to the left DL = 0: 4 bits F = 0: 5 x 7 dots					

Table 30: List of LCD commands and their codes

Equipment

No.	Description	Qty.
1	LCD screen 16x2	1
2	8-switch array	1
3	Connecting wires (jumpers)	-
4	Breadboard	1

Circuit Diagram

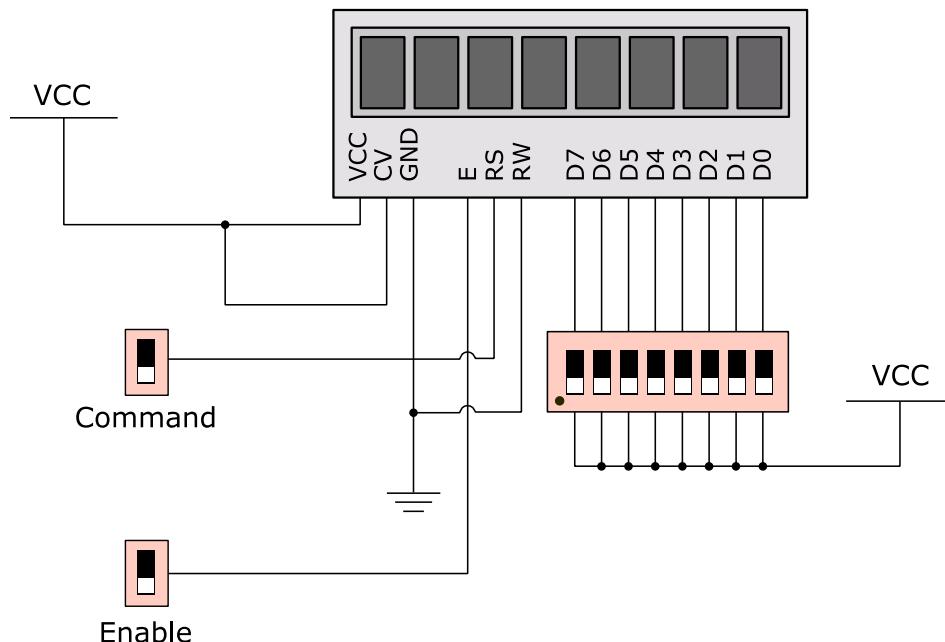


Figure 72

Procedure:

- Connect the circuit as shown in Figure 72.
- Adjust the brightness of the LCD screen if necessary.
- Put the RS (Command) switch to 0 to tell the LCD that you are entering a command (not a character to be displayed)
- Observe that the RW input is always set to 0, which tells the LCD that we intend to write data to it as opposed to read data from it.
- Set the data switches to 0000001. This instructs the LCD to clear the display and put the cursor at the beginning. The LCD does not respond instantly to the command. Set the enable input to 1 and back to 0 to issue the command.
- Now that the display is clear. Set the RS input to 1 so we can enter data to the LCD.

- Set the data switches to 1010111. Then apply a pulse to the enable input to send the letter W to the screen.
- Set the data switches to 1101001 then apply a pulse to the enable input. This enters the letter i.
- Set the data switches to 1101110 then apply a pulse to the enable input. This enters the letter n.
- You should see the word “Win” on the LCD screen.
- Proceed to test different characters and commands of your choosing to the LCD. Refer to Table 30 for the list of commands and Table 31 for the list of characters.

Hex	Char	Hex	Char	Hex	Char	Hex	Char
0	[NULL]	20	[SPACE]	40	@	60	`
1	[START OF HEADING]	21	!	41	A	61	a
2	[START OF TEXT]	22	"	42	B	62	b
3	[END OF TEXT]	23	#	43	C	63	c
4	[END OF TRANSMISSION]	24	\$	44	D	64	d
5	[ENQUIRY]	25	%	45	E	65	e
6	[ACKNOWLEDGE]	26	&	46	F	66	f
7	[BELL]	27	'	47	G	67	g
8	[BACKSPACE]	28	(48	H	68	h
9	[HORIZONTAL TAB]	29)	49	I	69	i
A	[LINE FEED]	2A	*	4A	J	6A	j
B	[VERTICAL TAB]	2B	+	4B	K	6B	k
C	[FORM FEED]	2C	,	4C	L	6C	l
D	[CARRIAGE RETURN]	2D	-	4D	M	6D	m
E	[SHIFT OUT]	2E	.	4E	N	6E	n
F	[SHIFT IN]	2F	/	4F	O	6F	o
10	[DATA LINK ESCAPE]	30	0	50	P	70	p
11	[DEVICE CONTROL 1]	31	1	51	Q	71	q
12	[DEVICE CONTROL 2]	32	2	52	R	72	r
13	[DEVICE CONTROL 3]	33	3	53	S	73	s
14	[DEVICE CONTROL 4]	34	4	54	T	74	t
15	[NEGATIVE ACKNOWLEDGE]	35	5	55	U	75	u
16	[SYNCHRONOUS IDLE]	36	6	56	V	76	v
17	[ENG OF TRANS. BLOCK]	37	7	57	W	77	w
18	[CANCEL]	38	8	58	X	78	x
19	[END OF MEDIUM]	39	9	59	Y	79	y
1A	[SUBSTITUTE]	3A	:	5A	Z	7A	z
1B	[ESCAPE]	3B	;	5B	[7B	{
1C	[FILE SEPARATOR]	3C	<	5C	\	7C	
1D	[GROUP SEPARATOR]	3D	=	5D	I	7D	}
1E	[RECORD SEPARATOR]	3E	>	5E	^	7E	~
1F	[UNIT SEPARATOR]	3F	?	5F	_	7F	[DEL]

Table 31: ASCII table of characters

Exercise 19: Ancillary Circuits

Objective:

To study the working of Amplifier, Comparator and a Latch.

Discussion:

As seen from the figure the circuit is divided into three stages.

- The first stage is an amplifier. In this the operation amplifier using fewer components amplifies the input voltages.
The resistors in the feedback arm decide the gain of the amplifier.
- The second stage is the comparator. In this the reference voltage is applied to one terminal of opamp. The signal output of stage one is compared with this reference voltage of a output in terms of high or low saturation voltage.
- The third stage is a latch circuit.
The output of the 2nd stage is used to drive the latch using the transistor. That in turn operates the relay to which a lamp load is connected.

Equipment

No.	Description	Qty.
1	741 opamp	2
2	A collection of resistors	-
3	LED	1
4	BC104 Transistor	1

Circuit Diagram:

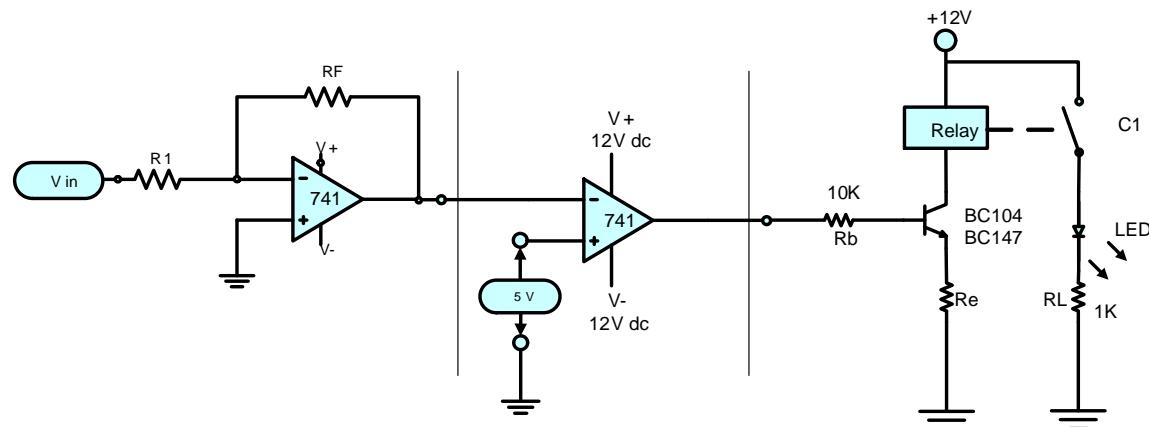


Figure 73

Troubleshooting of Composite Circuit:

- On a breadboard, construct the circuit shown above (Figure 73).
- Record all measurement on Table 32.
- A trouble shooting chart (Table 32) listing standard values and measured values are prepared. On the basis of comparison the area of fault is determined.

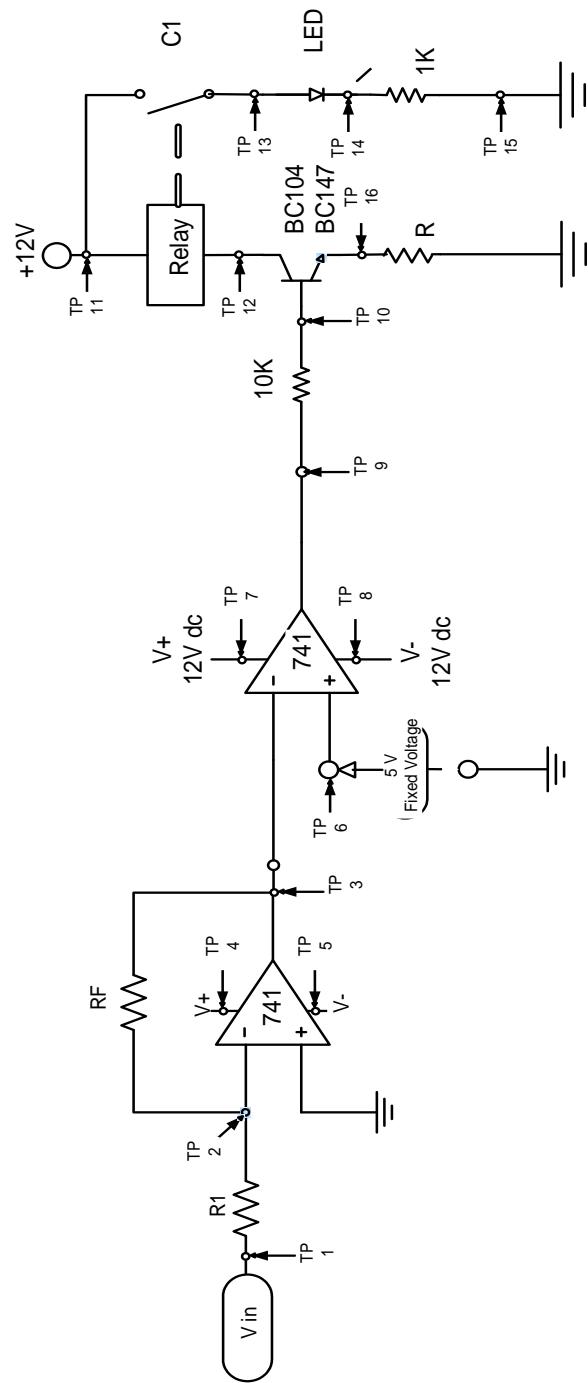


Figure 74

Sr no.	Component Testing	Std Values	Measured values
1	TP1		
2	TP2		
3	TP3		
4	TP4		
5	TP5		
6	TP6		
7	TP7		
8	TP8		
9	TP9		
10	TP10		
11	TP11		
12	TP12		
13	TP13		
14	TP14		
15	TP15		
16	TP16		

Table 32

Conclusion:

Type of Fault: _____
Action Taken: _____

Exercise 20: Exercise 18: Photoconductive Cells

Objective:

- To evaluate the performance and operation of a Light Dependent Resistor.
- To assemble and evaluate the operation of a Photo Detector Circuit.

Discussion:

A Light Dependent Resistor (aka LDR, photoconductor, or photocell) is a device which has a resistance which varies according to the amount of light falling on its surface.

A typical light dependent resistor is shown on the right with the symbol. Different LDR's have different specifications, however the LDR's are fairly standard and have a resistance in total darkness of $1\text{ M}\Omega$, and a resistance of a couple of $\text{k}\Omega$ in bright light ($10\text{-}20\text{k}\Omega$ @ 10 lux, $2\text{-}4\text{k}\Omega$ @ 100 lux).

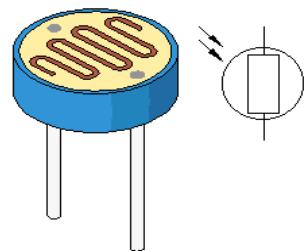


Figure 75

Most semiconductor materials are responsive to incident light in that their properties are affected by light irradiation in a variety of ways. A range of devices are available, and photo conductive cells (light dependent resistors - LDR), photodiodes, phototransistors, and photovoltaic or solar cells.

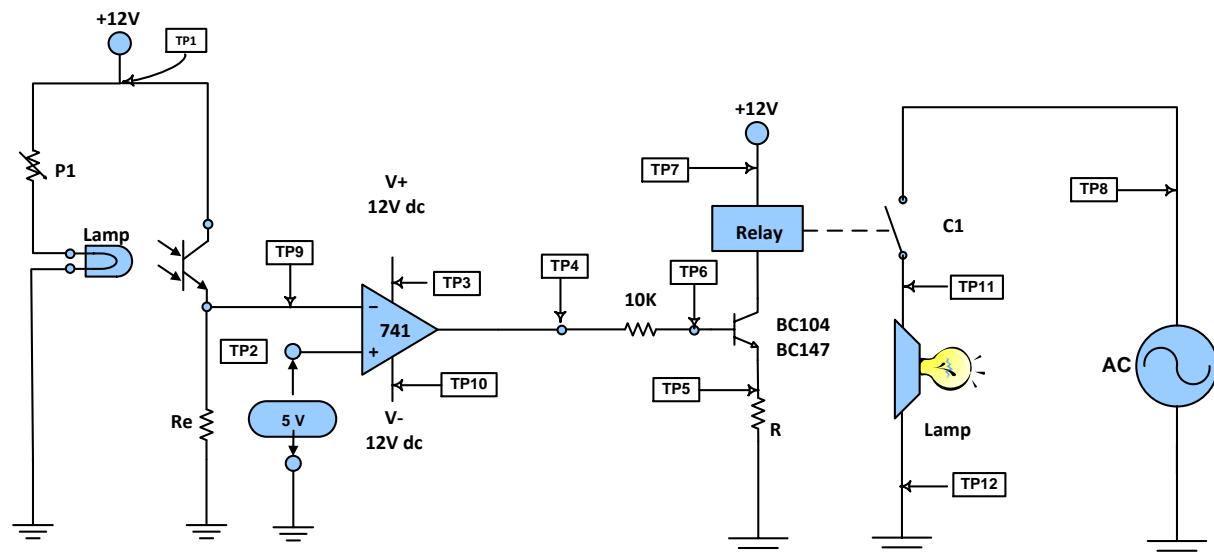


Figure 76

Equipment

No.	Description	Qty.
1	110v lamp	2
2	A collection of resistors	-
3	LED	1
4	BC104 Transistor	1

Circuit Diagram:

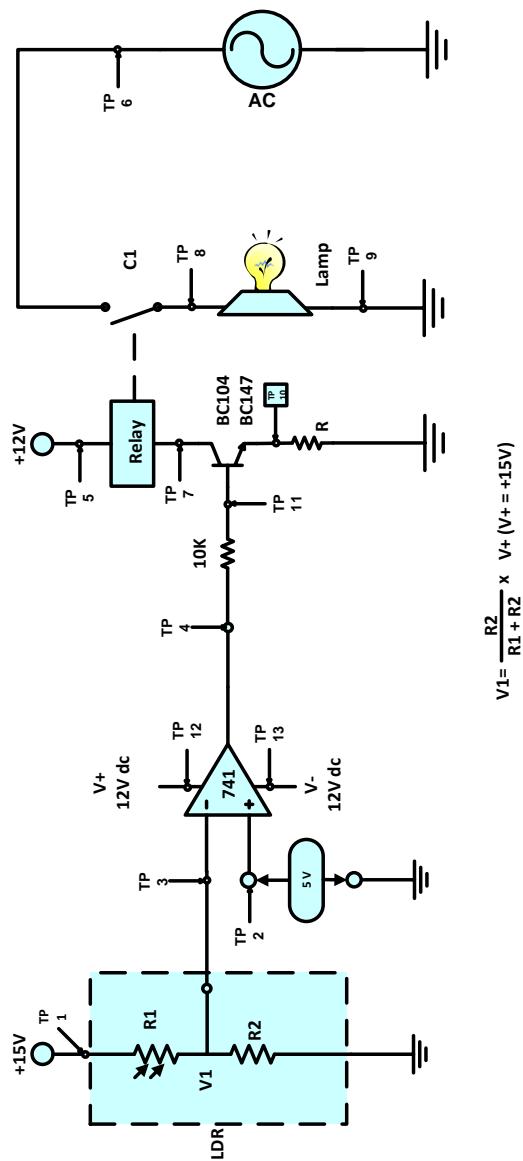


Figure 77

Procedure:

Several test points are shown in the circuit on Figure 77.

Assemble the circuit above on the breadboard.

Adjust the sensitivity.

Without further disturbing the settings make a record of standard signals on mentioned test points on Table 33.

Complete Table 33 below.

Introduce faults and take one more set of reading.

Compare and identify the fault.

Sr no.	Parameters	Standard Values Before Fault	Measured Values After Fault
1	TP1		
2	TP2		
3	TP3		
4	TP4		
5	TP5		
6	TP6		
7	TP7		
8	TP8		
9	TP9		
10	TP10		
11	TP11		

Table 33

Conclusion:

Type of Fault: _____

Action Taken: _____

Review Questions:

1. For the A-D circuit used in this exercise, the analog input voltage is initially set to 3.25V and the counter is briefly reset. The final indicated binary output Q_D , Q_C , Q_B , Q_A is:
a. 0,1,1,0 b. 0,1,1,1 c. 1, 0, 0, 1 d. 1,0,1,0

2. For the A-D circuit used in this exercise, the analog input voltage is initially set to 3.25V and the counter is briefly reset. The final indicated binary output Q_D , Q_C , Q_B , Q_A is:
a. 0,1,1,0 b. 0,1,1,1 c. 1,0,0,1 d. 1,0,1,0

3. For the A-D circuit used in this exercise, the analog input voltage set to 2.25V, the voltage indicated by the voltmeter will be:
a. 2.5V b. 0V c. 5.0V d. 6.5V

Appendix 1: Internal Connection of Basic ICs

