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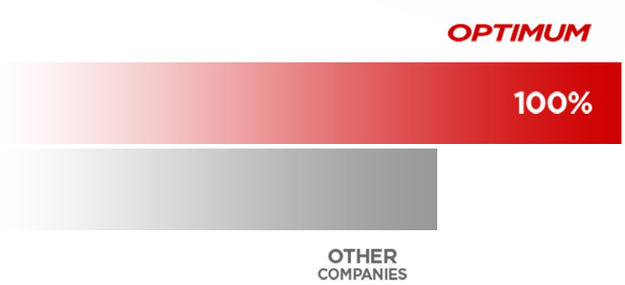

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Library User Guide

PADS Professional Library

Rev 1a

Contents

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Introduction and Setup

Welcome to the PADS Professional Library. This library package contains all the modules that are required for successful design integration between xDX Designer / xDX Databook schematic entry and PADS Professional Layout. It is intended for use with the following software:

- Mentor Graphics – **xDX Designer PADS Professional**
- Mentor Graphics – **PADS Professional Layout**
- Mentor Graphics – **xDM Library Tools PADS Professional**
- Microsoft® – **Access® 2007, 2010 and 2013**

Library Definition

Throughout the documentation, references are made to the following "**Library**" packages:

- xDM Library Tools **PADS Professional Library**
- xDX Databook **Libraries**
- PADS Professional Layout **Cell and PDB Library**

To avoid any confusion about the use of the word "Library," a brief description of each one is outlined below.

x**DM Library Tools Library –** The total package consists of:

- xDX Databook configuration
- Microsoft Access Database
- PADS Professional Layout – PDBs, Cells and xDX Designer symbols

xDX Databook Libraries – Are linked to the various Access database tables. They are able to be searched for parts to include in schematic entry.

PADS Professional Layout Library – Contains the PADS Professional Parts Databases (PDBs). These PDBs reference both the xDX Designer symbols and PADS Professional footprints (Cells), and the pin mapping between them.

Library Folder Structure

The basic folder structure of the Library is as follows:

PADSProVX_Library/
The Mentor xDM Library Tools library folder.
This folder also contains the project template file PADSProVX_Library_Seed_Job.prj which can be used to create new Projects

PADSProVX_Library/DatabookData
The folder that contains the Access Database and xDX Databook configuration file.

- PADSProVX_Library/DatabookData /***Databook.mdb***
  The Access database containing part information.

- PADSProVX_Library/DatabookData /***PADSProVX.dbc***
  The xDX Databook configuration file.

The rest of the folder structure inside the PADSProVX_Library/ folder is the standard Mentor Graphics Central Library structure.

Installation

Use the following procedure to install and configure your PADS Professional Library.

The default directory path for the library is **C:\PADSProVX_Library**.
After you unzip the downloaded PADSProVX_Library.zip you will need to move the library folder to this location.
"**C:**" is referred to as **<libpath>** in the instructions below. If you change the default path, then please substitute your designated path below wherever **<libpath>** appears in these instructions.

Configuration

The aim with the Library, configuration files, and documentation is to provide a design flow in its simplest working form, i.e., place parts from xDX Databook onto an xDX Designer schematic and forward annotate into a PADS Professional PCB layout via a linked Central Library. For use in its simplest form, the only post-installation configuration task that is required is the configuring of the xDX Databook, outlined in Steps 1 to 4 below.
There are many other configuration options and settings for various work flows and add-on toolsets. We do not attempt to cover every single aspect of the Mentor xDX Designer to PADS Professional environment with our documentation. Mentor provides an extensive help system, user guides, and web or phone-based support.

Configure your xDX Databook by using the following instructions to create a Windows ODBC Data Source:

1. Create an ODBC datasource for the xDX Databook by running the windows ODBC Data Source Administrator tool as follows:

    a. Windows 7 64-Bit system / 32-Bit PADS Professional software version -> If the 32-bit version of the software is installed on Windows 64-Bit systems, the ODBC Data Source Administrator must be invoked in 32-Bit mode as follows.
        i. Browse to **C:\Windows\sysWOW64**
        ii. Double click the **odbcad32.exe** file (this is the 32bit version)

    Note: It is important that xDX Databook data sources for 32-Bit systems are created in this manner (via odbcad32.exe), if they are created via **Administrative Tools** they will not run in xDX Databook.

    b. Windows 7 32-Bit system / 32-Bit PADS Professional software version **Control Panel / System and Security / Administrative Tools / Data Sources (ODBC)**.

c. You will now see the following dialog (you may not have the same User Data Sources listed, 64-bit is shown , 32-bit may look different).

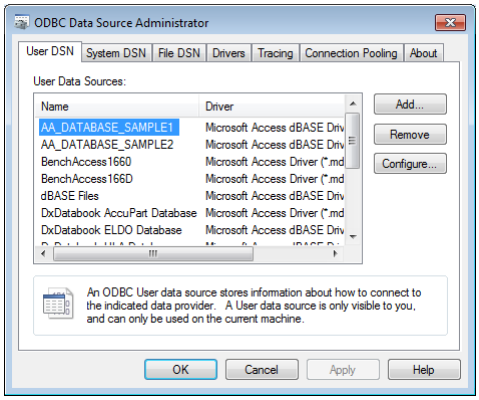

Figure 2.1 ODBC Data Source Administrator

d. Now click the **Add** button to create your new datasource, you should see the following screen:

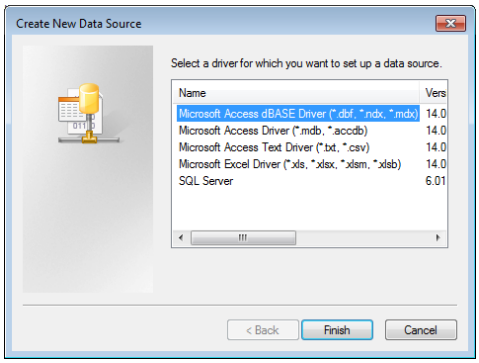

Figure 2.2 Available drivers list

e. Scroll down and select **Microsoft Access Driver (*.mdb)** as the driver and click the **Finish** button.

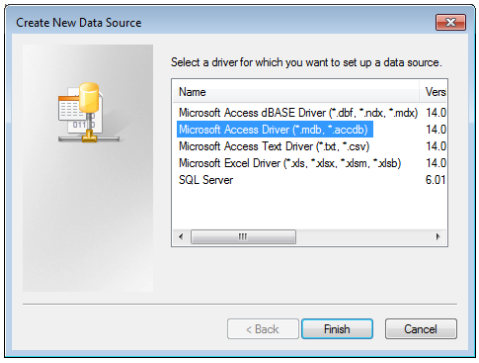

Figure 2.3 Selecting the Microsoft Access (.mdb, *.accdb) driver*

2. Now you see the ODBC Microsoft Access Setup screen. Enter **PADSProVX_Library** as the Data Source Name and optionally a Description of your choice.

   Then click on the **Select…** button and browse to the Central library on your machine and select the file **<libpath>\PADSProVX_Library\DatabookData\Databook.mdb** as the database to use for this DataSource.

   Note: in some cases you may find the system will not allow you to browse for the file outside of the Windows folder. If this happens, Right Click on the **DataSources (ODBC)** tool in Windows and select **Run as Administrator**.

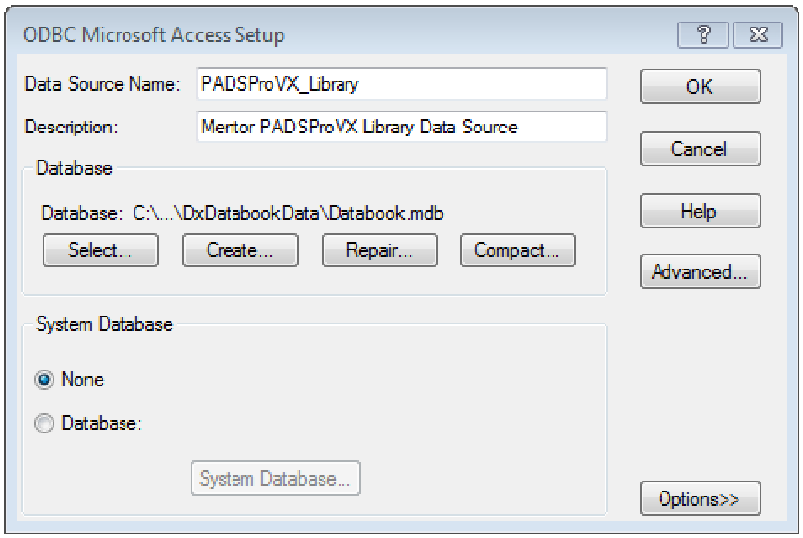

Figure 2.4 Entering the DataSource Name and Description

3. Click **OK** to complete this part and then **OK** again on the **ODBC Data Source Administrator** dialog to complete the DataSource setup procedure.

4. If the location of the library changes, then the datasource defined above will need to be modified to select the new database location. Other xDX Designer settings will need to be changed as well, see Re-Configuration section for detailed information on this.

Project Template File

A project template file is provided with the library for creating new xDX Designer projects: **PADSProVX_Library_Seed_Job.prj**.
This is a xDX Designer project file. You can place this file in your ***<InstallPath>*/SDD_HOME/standard/templates/dxdesigner/expedition** folder. Where ***<InstallPath>*** is the location of your MentorGraphics software installation. Once this file is in this location it will appear in the xDX Designer Dashboard or xDX Designer application itself as a template when you create a new project. Selecting this template when you create a new project will create a project with the library association already linked. In xDX Designer select File > New > Project

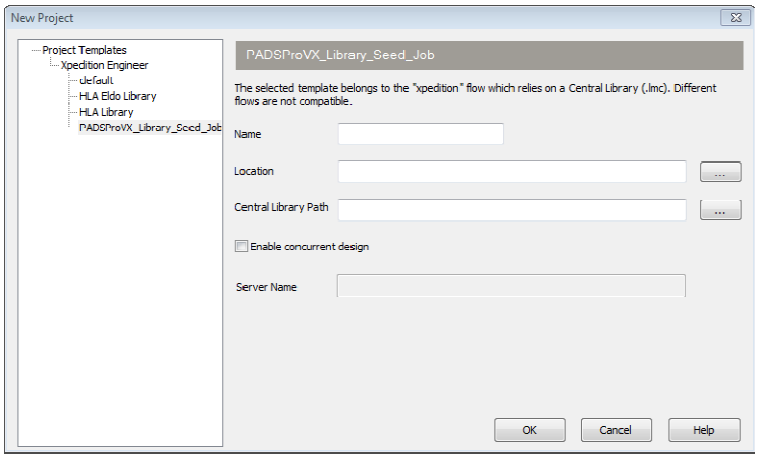

Figure 2.5 xDX Designer New Project Dialog

Select the PADSProVX_Library_Seed_Job template from the list of available templates and enter a project name to create a new xDX Designer project pre linked to the PADS Professional Library.

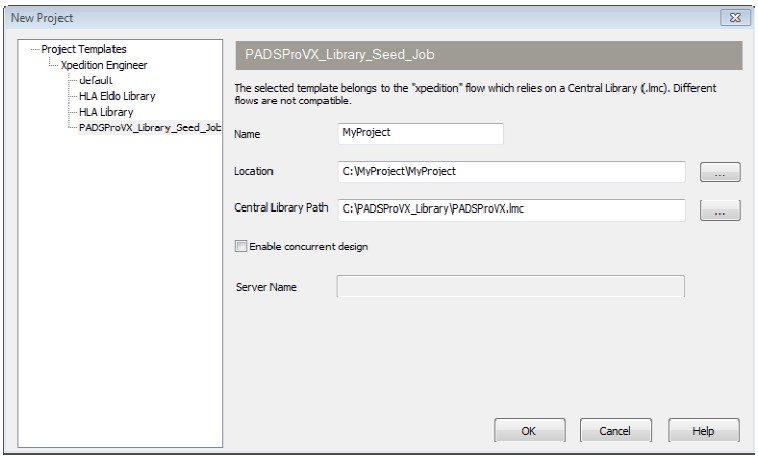

Figure 2.6 Selecting the PADSProVX_Library_Seed_Job project template

Arial or San Serif Font

The symbols in the library have been designed for use with Arial or San Serif text font. This is an extremely important setting because if it is not configured then all text defined in the schematic symbols will appear too large and out of place. This applies to Reference Designator, Pin Name, Pin Number and some visible properties defined for use on symbols. If you are using the symbol library and are seeing fonts other than Arial or San Serif for these items, then follow these instructions to update your configuration. This is a user setting that is not local to the project, it is saved in the xDX Designer.xml file in your WDIR folder so you should only need to change this once. If your environment requires the use of a stroked font then choose San Serif.

To update the active project use the xDX Designer Setup/Settings dialog.

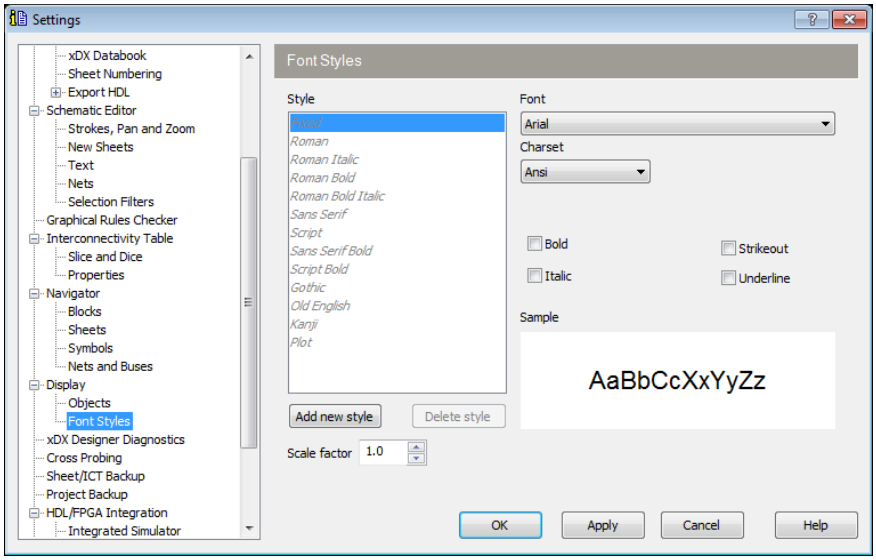

Figure 2.7 Font Settings

PCB Layout Templates

There are multiple PCB Templates provided with the library. The default Mentor Graphics **4 Layer Template** and **8 Layer Template** and all the **Template_xLayer_Formatted** templates are included for use with the Mentor PADS Professional software release.

The installation and configuration are now complete, and everything is in place to enable schematic entry and forward annotation to a PCB layout.

Re-Configuration

If you move the library to use a different path, you must re-configure certain items in existing projects and templates in order for the design flow to work correctly. Re-configure your workflow using the Setup > Settings dialog in xDX Designer and the Setup > Project Editor in PADS Professional Layout.

1. Modify the library paths for the Central Library itself and for Special Components and Border Symbols.

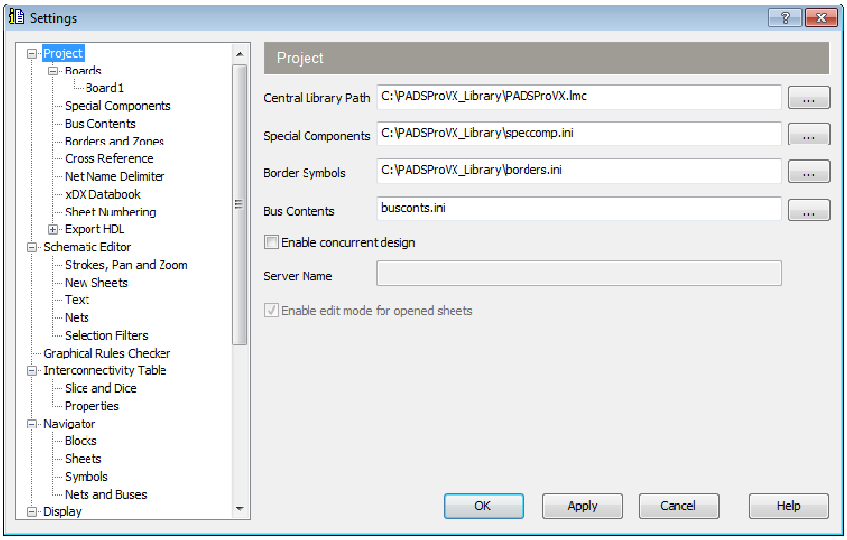

Figure 3.1 Library Path Settings in xDX Designer

2. Define the path to the xDX Databook Configuration (.dbc) file using the Setup/Settings Dialog.

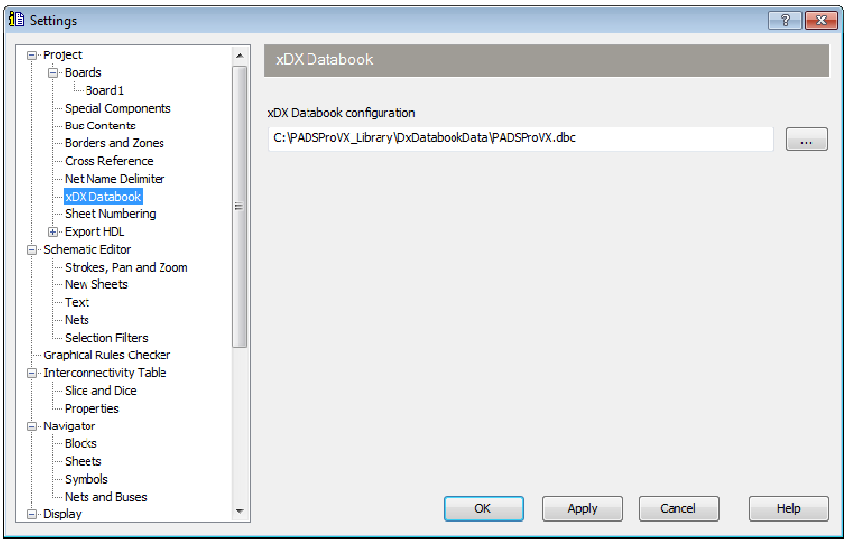

Figure 3.2 xDx Databook Configuration File Location

3. Point to the library location in the PADS Professional Project Editor dialog.

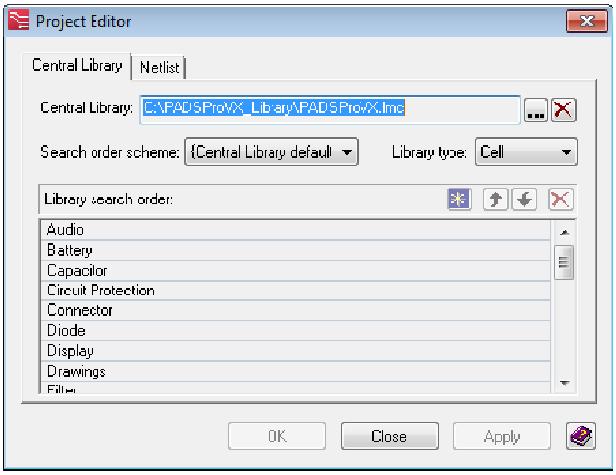

Figure 3.3 Project Editor Settings in PADS Professional PCB

These Project level settings can also be updated by modifying the xDX Designer project (.prj) file directly using a text editor. The Project File supplied with the library contains settings for the default installation path.

Access Database and xDX Databook

Access Database Definition

The PADS Professional library uses a Microsoft® Access® Database, ***Databook.mdb***, as the ODBC data source. Throughout this document it is simply referred to as, "database."

The database is used as a source for device data, which is then attached to symbols in a xDX Designer schematic. This is achieved by placing devices from xDX Databook, which provides the link to the database.

Many different configurations of a database can be used with xDX Designer, such as linked tables and queries, but our aim is to keep things as simple as possible. For this reason the database structure is very basic. The tables are organized according to device types. If a field is not relevant to a particular type of device, it is simply left blank.

Device Data

All of the required data needed to produce a schematic, Bill Of Materials (BOM), and successful forward annotation into PADS Professional is contained in the database. This includes references for:

- xDX Designer symbols
- Manufacturer part numbers
- PADS Professional cells

Various other data are also included for use at the discretion of the end user.

Database Tables

AUDIO – Buzzers, Speakers
BATTERY – Batteries
CAPACITOR* – Capacitors
CIRCUIT PROTECTION – Fuses
CONNECTOR – Connectors, Terminal Blocks
DIODE – Diodes, Bridge Rectifiers, Transient Voltage Suppressors
DISPLAY – LEDs, Optoelectronics, Displays
DOCUMENTATION – Documents
FILTER – Filters
FPGA – FPGAs and configuration
IC – Integrated circuit symbols.
INDUCTOR* – Inductors
MECHANICAL – Hardware, nuts and bolts etc, Mounting Holes
OSCILLATOR – Oscillators and Crystals
RESISTOR* – Resistors and Trimpots
SWITCH – Switches and Relays
TESTPOINTS – Tespoints, pins, pads, ICT
TRANSFORMERS – Transformers
TRANSISTOR – Transistors and MOSFETs

***Note**: The CAPACITOR, INDUCTOR, and RESISTOR tables listed above contain devices that do not have any manufacturer part number data. This allows the user to quickly place these devices without having to know its part number in advance. After placement, part numbers can then be added, or the generic devices can be replaced with actual devices in the schematic. It is also possible to add the part numbers at the BOM level without updating the schematic, if so desired.

Component Libraries

The component libraries in xDX Databook have a one-to-one relationship to the tables in the Access database, ***Databook.mdb***. The component library structure is, therefore, exactly the same as the table structure in the database, ***Databook.mdb***. These tables show up in xDX Databook as the searchable component libraries from which devices are selected and then dragged onto the schematic page. The field structure is as follows.

Property Definition

When devices are placed from xDX Databook, all of the property information that is contained in the database tables is brought into the instance of that device on the schematic.

There are four different xDX Databook field types. They are defined in xDX Databook as:

- **Document** - Provides a link to the document in the query results window
- **Normal** - Normal field type
- **Symbol** - Contains the symbol to be used for a part
- **Unused** - Ignored field type
-

The following table lists all of the fields in the xDX Databook configuration, and the name of the properties in xDX Designer to which they are mapped.

Database Fields

DATABASE FIELD NAME	MAPPED xDX Designer PROPERTY	DESCRIPTION	Library Definition	xDX Databook FIELD TYPE
Part Number	Part Number	Manufacturer part number	Defined	Normal
Symbol	Name of schematic symbol	xDX Designer symbol name	Defined	Symbol
Footprint	Cell Name	PADS Professional cell name	Defined	Normal
Value	Value	Device value	Defined where applicable	Normal
Tolerance	Tolerance	Device tolerance	Defined where applicable	Normal
Rated Voltage	RatedVoltage	Device voltage in volts	Blank - End User Defined	Normal
Rated Current	RatedCurrent	Device current in amps	Blank - End User Defined	Normal
Rated Power	RatedPower	Device power in watts	Blank - End User Defined	Normal
Status	Status	Status	Blank - End User Defined	Normal
Manufacturer Part Number	ManufacturerPN	Manufacturer's part number	Defined	Normal
Manufacturer Name	Manufacturer	Manufacturer's name	Defined	Normal
Manufacturer Part Description	Description	Manufacturer's description of part	Defined	Normal
Manufacturer Link	ManufacturerLink	Link to manufacturer website	Blank - End User Defined	Document
Supplier Part Number	SupplierPN	Supplier's part number	Blank - End User Defined	Normal
Supplier Name	Supplier	Supplier's name	Blank - End User Defined	Normal
Supplier Category	SupplierCategory	Supplier's device category	Blank - End User Defined	Normal
Supplier Sub-Category	SupplierSubCategory	Supplier's device sub-category	Blank - End User Defined	Normal
Supplier Link	SupplierLink	Link to supplier website	Blank - End User Defined	Document
Datasheet Link	Datasheet	Link to datasheet	Blank - End User Defined	Document
Photo Link	Photo	Link to device photo	Blank - End User Defined	Document
Resistance	Resistance	Device resistance	Blank - End User Defined	Normal
Capacitance	Capacitance	Device capacitance	Blank - End User Defined	Normal
Inductance	Inductance	Device inductance	Blank - End User Defined	Normal
Package	Package	Industry standard package name	Defined	Normal
Component Type	Component Type	Device type	Defined	Normal
Cost	Cost	Cost	Blank - End User Defined	Normal
Part Name	Part Name	Part name	Future use	Normal
Part Label	Part Label	Part Label	Future use	Normal
Part ID	Part_ID	PartID	Future use	Unique ID

Figure 4.1 Database Fields

Field Definitions

Fields are described as:

- REQUIRED – essential for successful forward annotation to PADS Professional PCB
- OPTIONAL – preferable to have a value entered, but not essential
- END USER – Value is end-user specific

Part Number

REQUIRED: The manufacturer part number is used for Part Number for all specific devices. In the case of resistor, capacitor and inductor, a generic descriptive part number is used for the base values of each size.
The value in this field is synced to the part number in the corresponding pdb in the LMC.
The part number field value may be replaced by a company's internal part number since the manufacturer part number is also defined in its own field.

Symbol

REQUIRED: The value of this field determines the symbol that will be used when the device is selected from xDX Databook for placement on the schematic. The exclusion of a file extension (.1, .2, etc.) in the symbol name allows the use of any of the multiple symbols with the same name. For example, cap.1, cap.2, cap.3, or cap.4 can all be selected from xDX Databook for any device that has 'cap' as the symbol name. This allows for different rotations and views of the symbol to be selected for placement.
And asterix character at the end of the symbol name allows for all symbols in a Hetero set to become available for placement on the schematic i.e. *xc7vx415t-ff1927**

Footprint

REQUIRED: The value in this field is synced to the cell name used in the PDB entry in the PADS Professional flow.

Value

OPTIONAL: This is the value of discrete devices (RES, CAP, etc.) – in Ohms, Farads, Henrys, or Hertz.
It is only used in Resistor, Capacitor, Inductor and Oscillator.

Tolerance

OPTIONAL: This field contains the device's tolerance.

Rated Voltage

OPTIONAL: This field contains the voltage rating of the device in volts.

Rated Current

OPTIONAL: This field contains the current rating of the device in amps.

Rated Power

OPTIONAL: This field contains the power rating of the device in watts.

Status

END USER: Can be used to record verification that a device entry has been checked.

Manufacturer Part Number

END USER: This field contains the manufacturer's complete part number.

Manufacturer_Name

END USER: This field contains the manufacturer's name.

Manufacturer Part Description

END USER: This field contains the manufacturer's part description.

Manufacturer Link

END USER: This field contains a link to the manufacturer's website.

Supplier Part Number

END USER: This field contains the supplier's part number.

Supplier Name

END USER: This field contains the supplier's name.

Supplier Category

END USER: This field can be used to categorize the device.

Supplier Sub-Category

END USER: This field can be used to categorize the device to a further level.

Supplier Link

END USER: This field contains a link to the supplier's website.

Datasheet Link

END USER: This field contains a link to the datasheet for the device. It can be used to link a path to a repository or to a web address to the datasheet on a manufacturer's website.

Photo Link

END USER: This field contains a link to a photo of the device.

Resistance

END USER: This field contains the resistance of the device.

Capacitance

END USER: This field contains the capacitance of the device.

Inductance

END USER: This field contains the inductance of the device.

Package

END USER: The industry standard package name (0805, SO8, BGA48, etc.) or SMD/THP.
It is NOT the PADS Professional cell name.

Component Type

END USER: This is simply the type of component, e.g., IC, CAPACITOR, etc. It can be used for sorting devices.

COST

END USER: This field is for the end user to record the cost of the device.

Part Name

END USER: This field is for future use to sync to the pdb Part Name in LMC.

Part Label

END USER: This field is for future use to sync to the pdb Part Label in LMC.

Part ID

END USER: This field is for future use.

Searching for Devices

xDX Databook allows the user to find devices very easily with the use of a comprehensive database search engine. Any of the database fields can be searched with a variety of search operators to quickly find the required device.

Note that the value is recorded in the Access database as base units Ohms, Farads, Henrys, and Hertz. For example:

100K is recorded as 100000
100pf is 0.00000000010000
470uf is 0.00047000000000
25MHz is 25000000

But in the xDX Databook and on the schematic, the values show as

100K
100pf
470uf
25MEGHz

This applies to the following tables:

RESISTOR
CAPACITOR
INDUCTOR
OSCILLATOR

Symbols

The Symbols Library's Structure

Short descriptions of Symbol Libraries

Audio	Buzzers and speakers
Battery	Batteries
Capacitor	Capacitors
Circuit Protection	Fuses and circuit breakers
CONNECTOR	Plug and socket symbols for all part types of connectors
Diode	Diodes, Transient Voltage Suppressors and bridge rectifiers
Display	LEDs, Optoelectronics and displays
Documentation	Documentation symbols, bus ripper, page in/out/bi
Filter	Filters
Globals	Power and Ground symbols
IC	Integrated circuit symbols
Inductor	Inductors
Mechanical	Hardware, nuts and bolts etc, Mounting Holes
Oscillator	Oscillators and Crystals
Resistor	Resistors
Switch	Switches and Relays
Transformer	Transformers
Transistor	Transistors and MOSFETs

Typical IC Symbol Structure

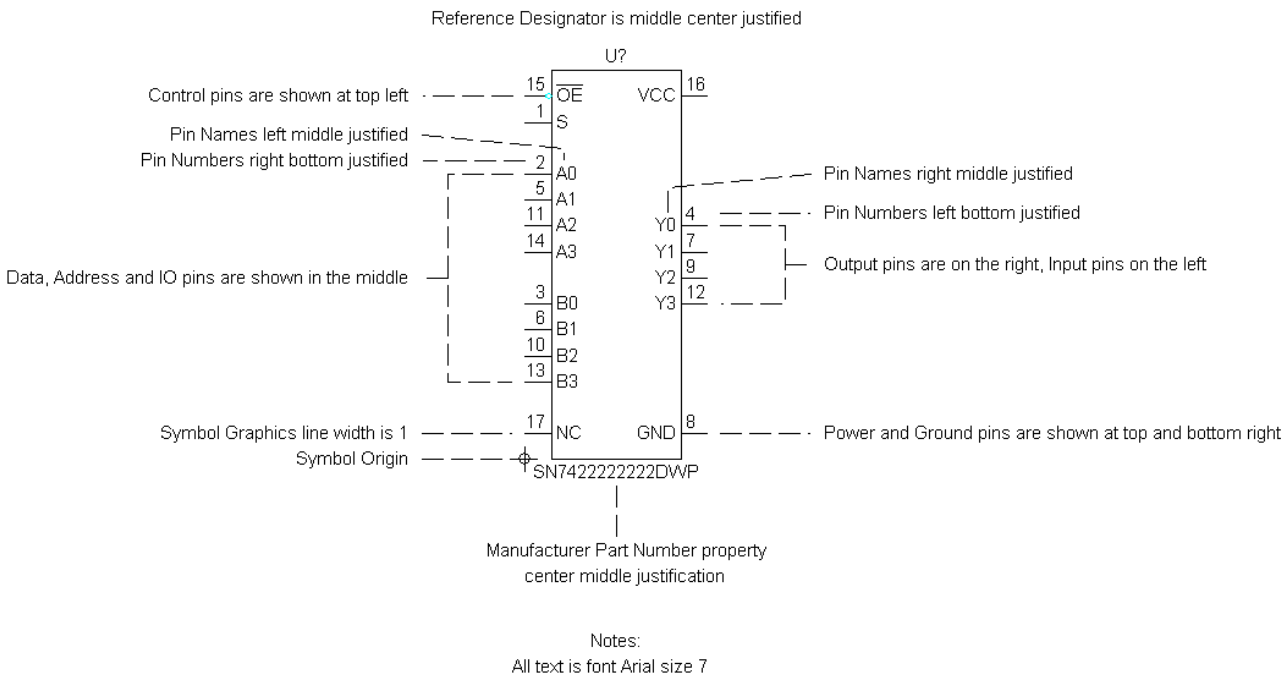

Figure 5.1 Typical IC Symbol Structure

Symbol Naming Conventions

• Symbol Name Prefixes

The symbol prefixes (where used) are self-explanatory as to what part type the component symbol represents, and most are in the form of widely used, industry-standard abbreviations. For example, plg = plug, cap = capacitor, etc.

• Manufacturer part number qualifiers

Many symbols simply use the manufacturer part number as the symbol name qualifier. This convention is mainly used for ICs, but may be used for other symbols where deemed appropriate.
IC symbol naming is in the form of *base manufacturer part number–package*
For example, symbol name lt1618-dfn10h.
Linear Technology part number lt1618 **d**ual **f**lat **n**o lead **10** pin **h**eatsink pad

• Multiple symbol qualifiers

pin group qualifiers (suffix), are used to name the separate symbols used in a device according to the various pin groups; for example, -gnd, -cfg, -bnk2

• Part type qualifiers

As well as using the part type prefixes, many symbols also use other descriptive part type qualifiers in their naming conventions. Most of these qualifiers are readily identifiable as industry standard abbreviations. For example, var = variable, pol = polarized. For a list of part type qualifiers, see the Abbreviations Section later in this document.

• Package type qualifiers

IC symbols *may* contain a package type suffix where devices are available in different package pinouts.
For example, dil = dual in line, qfn = quad flat no lead.
Some generic style IC symbols do not have the suffix.
For example, reg-iioa = regulator with 2 input, an output and an adjust pin in any package

• Pin number qualifiers in symbol names

Symbols have pin number information included in the symbol name. This is our preferred method of making symbols as generic as possible without the need for additional “side” files or attributes to manipulate pin orders and numbers.

For example, the symbol ***“reg-iioa.1”*** can be used for any regulator that has the pinout of 2 x input pins, 1 x output pin and 1 x adjust pin.
“mosfet-n-gdsss” can be used for any n channel mosfet with 1 x gate pin, 1 x drain pin and 3 x source pins

This method enables the use of one symbol for many different devices. This naming convention may be used for any part type having a maximum of 8 pins. A list of the letters used and their meanings can be found in the Abbreviations Section later in this document.

- # File extensions in symbol names

Each symbol is stored in the form of a text file, with the file extension of .1, .2, .3, and so on. Different symbol file extensions are used to depict different views of the device. This enables the user to:

- Place different symbol views that have all of their text in the correct orientation
  All of the widely used 2-pin symbols, such as res and cap, have a symbol with both a .1 and a .2 extension.
  .1 = horizontal view
  .2 = vertical view

- Have symbols that allow for closer placement of symbols without overlapping text/graphics
  These are generally used for pull up or pull down resistor groups.
  .3 = horizontal slimline
  .4 = vertical slimline

- Place different pinout schemes for the same connector
  .1 = all pins on the left side, numbered top to bottom
  .2 = odd pins on the left – even pins on the right, numbered top to bottom
  .3 = pins 1 to x on the left – x+1 to last pin on the right, numbered top to bottom
  .4 = IC style pinout

- Place different views according to “gate level” or “all pins” symbols
  These symbols are usually resistor, capacitor or diode packs. Any device that can be shown as all pins in one symbol or as individual gates can use this method.
  .1 = all pins on one symbol - ***res-pack-4res.1***
  .2 = multiple gates of the same symbol - ***res-pack-4res.2**** *(not in use yet)*

Having the different views reduces the need to continually rotate text to match the view of the symbol.

By not including the file extension in the xDX Databook entry, all symbols with the matching base symbol name are available in the xDX Databook symbol selection window.

- **Pin Text**

Each pin name is unique. Duplicate pin names are not allowed because pins cannot be mapped in the layout tool if there are two pins with the same name.

If more than one pin performs the same function (e.g., a ground connection), then the pin names must still be different. These pins are typically differentiated with the addition of a number at the end of the pin name. For example, GND1, GND2, etc.

PIN NAMES may or may not be visible, depending on the symbol. As a general guide, pin names are not shown on discrete, connector, or logic gate symbols, whereas they are shown on IC symbols.

PIN NUMBERS may or may not be visible, depending on the symbol. As a general guide, pin numbers are not shown on discrete symbols, whereas they are shown on connector and IC symbols.

PIN TYPES are always invisible. Pin types used are IN, OUT, BI, TRI, and ANALOG.

Symbol Pins

- **Pin connection points**

The connection point of a pin is determined by where the pin meets the symbol outline border. This outline appears as a white box around the symbol during symbol editing.
Pins can be moved around and rotated inside the outline, and can be of any length within that outline, but the connection point remains where the pin meets the outline.

- **Pin shapes**

There are four pin shapes on the symbols. Normal and inverted pins consist of the pin only (no drawn graphics are used), whereas the clock pins are a normal pin plus a clock graphic. The dot pins are created with the use of the “invert pin option.”

Normal – active high input or output
Dot – active low input or output
Clock – active high clock input or output
Dot Clock – active low clock input or output

- **Negative logic pins**

Negative logic pins are signified with the use of overbars in the pin name. The overbar is created automatically by checking the “inverted” checkbox in the pin properties dialog. Selecting “invert pin” from the same dialog will give the pin a “dot”/“bubble” pin. The size of the bubble is determined by the user in the schematic Setup – Settings – Advanced section. The recommended size for this library is 0.010

- **Power, ground, and no-connect pins**

All Power, ground and no-connect pins are explicitly shown on the symbols. No implicit pins are used.

Abbreviations

The symbol library makes extensive use of abbreviations in symbol names.

This document is aimed at giving the end user a broad understanding of the abbreviations. While it is extensive, it is not an absolute list of every abbreviation used.

Many of the entities within the library are named without abbreviation and, therefore, do not appear in this index.This document is divided into two sections. The first section contains abbreviations for Part Type Qualifiers, and the second section contains abbreviations for Pin Type Qualifiers.

• Part Type Qualifier Abbreviations

DISCRETES

ABBREVIATION	TYPE
DIO	DIODE
ZENER	ZENER DIODE
SCHTKY	SCHOTTKY DIODE
CAP	CAPACITOR
RES	RESISTOR
IND	INDUCTOR
VAR	VARIABLE
POL	POLARIZED
PACK	MULTIPLE GATES IN DEVICE
BUS	BUSSED

Figure 5.2 Discrete Qualifier Abbreviations

IC

ABBREVIATION	TYPE
OPAMP	OPERATIONAL AMPLIFIER
REG	REGULATOR

Figure 5.3 IC Qualifier Abbreviations

MISC

ABBREVIATION	TYPE
OSC	OSCILLATOR
PLG	CONNECTOR PLUG (MALE)
SKT	CONNECTOR SKT (FEMALE)
XFMR	TRANSFORMER
SIL or SIP	SINGLE ROW IN LINE PINS
DIL or DIP	DUAL ROW IN LINE PINS

Figure 5.4 Miscellaneous Part Abbreviations

- **Pin Type Qualifier Abbreviations**

DIODE PINS

ABBREVIATION	TYPE
K	CATHODE
A	ANODE
BI	BI DIRECTIONAL
UNI	UNI DIRECTIONAL

Figure 5.5 Diode Pin Abbreviations

MOSFET PINS

ABBREVIATION	TYPE
G	GATE
D	DRAIN
S	SOURCE

Figure 5.6 MOSFET Pin Abbreviations

RELAY PINS

ABBREVIATION	TYPE
CL	COIL
CM	COMMON
NC	NORMALLY CLOSED
NO	NORMALLY OPEN

Figure 5.7 Relay Pin Abbreviations

TRANSISTOR PINS

ABBREVIATION	TYPE
C	COLLECTOR
B	BASE
E	EMITTER

Figure 5.8 Transistor Pin Abbreviations

TRIMPOTS

ABBREVIATION	TYPE
MIN	MINIMUM (CCW)
MAX	MAXIMUM (CW)
ADJ	ADJUST (WIPER)

Figure 5.9 Trimpot Pin Abbreviations

IC PINS

ABBREVIATION	TYPE
I	INPUT
O	OUTPUT
G	GROUND
AG	ANALOG GROUND
V	VCC
VE	VEE
VD	VDD
NC	NO CONNECT
ENH	ENABLE HIGH
ENL	ENABLE LOW
RSTH	RESET HIGH
RSTL	RESET LOW
PWR	POWER
ADJ	ADJUST
POS	POSITIVE
NEG	NEGATIVE
VREF	VOLTAGE REFERENCE
FB	FEEDBACK
SHDN	SHUTDOWN
H	HEATSINK PIN / THERMAL PAD

Figure 5.10 IC Pin Abbreviations

Land Pattern Specification

This section describes the naming conventions and parameter used for the land pattern creation in the PADS Professional Library. It is based on the IPC7351B Generic Requirements for Surface Mount Design and Land Pattern Standard.
Land patterns are built to IPC7351B or in some cases, to manufacturer recommended land pattern. The naming conventions clearly denote which has been used later in this document

All units are in millimeters (mm) throughout this document unless otherwise noted.

Note: Not all name modifiers and options defined in this section are used in the library.

Some definitions have been created for future use to ensure uniformity of naming if this document is used.

Naming Convention Overview

The following section details the naming convention for ODA land patterns, padstacks and pads. The land pattern naming convention is based on the IPC7351B land pattern naming convention for IPC type SMD components. Additional conventions are added for ease of identification or due to limitations of the IPC naming convention.

Height :
Except for aluminum electrolytic capacitors and two pin crystals, the height convention is removed from the naming convention to reduce duplication of land patterns where height can be introduced into the design via external toolsets.

Character Limitation:
Land pattern names have a 31 character limitation. The period (.) and space characters will not be used in any library entities. Adhering to these rules for pad, padstack and land pattern names will allow for easier library and layout database translation to other systems when required.

Typography and numbering convention:

All units in the library are metric as follows:

- 2 decimal places resolution for hole sizes.
- 4 decimal places resolution for Pads, Padstacks and hole tolerances.

Square brackets “**[ ]**” are used to indicate optional values.

Forward slash “ ***/*** “ is used to indicate alternate values.

Pad and Padstack Naming

Similar naming is used for Pads and Padstacks in the library.

Pads are named as: **Shape - Dimensions - Optional Modifiers**
Where:
Shape = **C**, **R**, **S** etc. (see Pad and Padstacks Shapes table below).
Dimensions = Xsize **X** Ysize
Optional modifiers = modifiers plus options (see Pad and Padstack Modifiers table below).

Examples:
C2500 = 2.500mm circular pad.
R3000X2250 = 3.000mm x 2.500mm Rectangle pad.

Padstacks are named as: **Type - [Plating] - [Hole Dimensions] - Shape - Pad Dimensions - Optional Modifiers**
Where:
Type = **M**, **S**, **T** etc. (see Padstack Types table below).
Plating = **P** (Plated) or **N** (Non Plated)
Hole Dimensions = Hole Xsize [**X** Ysize]
Shape = **C**, **R**, **S** etc. (see Pad and Padstacks Shapes table below).
Pad Dimensions = Pad Xsize [**X** Ysize]
Optional modifiers = modifiers plus options (see Pad and Padstack Modifiers table below).

Examples:
THP200C3000 = 2.00mm plated through hole with circular 3.000mm pad.
SR0800X0700 = surface mount rectangle pad 0.800mm X 0.700mm.
MHN300 = mounting hole, 3.00mm non plated hole.

Dimensions

Pad dimensions are defined as metric units with 3 decimal places. All dimensions for Pads are 4 digit numbers representing sizes from 0.000 to 9.999mm or 5 digit numbers representing sizes from 10.000 to 99.999mm. Leading and trailing zeros are always shown.

For uniform shaped entities such as Round, Square and Octagonal, only one dimension is needed. For elongated entities such as slotted holes, Rectangle, Obround and Finger pads and padstacks, both X and Y dimensions are given. When both axes are dimensioned the format is Xsize **X** Ysize. (Ex. **1200X1000** = 1.200mm X-axis and 1.000mm Y-axis.

Hole sizes are defined as metric units with 2 decimal places. Hole dimensions are 3 digit numbers for sizes from 0.00 to 9.99mm and 4 digit numbers for sizes from 10.00 to 99.00mm. Leading and trailing zeros are always shown.

Note: Hole size tolerances are 4 digit numbers with 3 decimal places representing tolerances from 0.000 to 9.999mm
Note: Elongated pads and padstacks are always created with the X axis being larger than the Y axis.

Default Conditions

The following table lists default parameters for pads and padstacks.

PARAMETER	DEFAULT CONDITION
Origin	The geometric center of a pad or a padstack. Use the _**OFF** modifier and its options to define an offset origin.
Soldermask	0.100mm diameter larger than the pad size, various soldermask modifiers are defined below.
Solderpaste	The same size as the pad size, various solderpaste modifiers are defined below.
Thermal Ties	There are 4 ties at 45 degrees in a thermal pad. Thermal parameters and modifiers are defined below.
Inner Pads	Square through hole padstacks use round internal pads with diameter equal to surface square pad size.
Via Thermals	Via padstacks default to buried thermal tie connections. Use _THRM to define a via with thermal relief.
Drill Tolerance	Hole tolerance default is +/-0.075mm for holes up to 2.50mm, +/-0.100mm for holes larger than 2.50mm Via holes have a positive tolerance of 0.075mm and a negative tolerance equal to the hole size.

Figure 6.1 Default Padstack Parameters

Soldermask Default

All padstacks have soldermask openings defined unless specifically indicated by the optional modifiers at the end of the name. Default soldermask condition for all padstacks is the same size for both Top Mount and Bottom Mount. The default soldermask size condition is 0.100mm over the pad size or over the drill size for non plated holes where the drill is larger than the pad.

Paste mask Default

All SMD padstacks have paste mask defined and all through padstacks do not have paste mask defined unless specifically indicated by the optional modifiers at the end of the name. Default pastemask condition for all SMD padstacks is the same size for both Top Mount and Bottom Mount. The default solderpaste size condition is the same size as the pad.

Pad and Padstack Shapes

Shapes are defined with 1 or 2 characters. Only Donut and Thermal shapes are defined with two characters, one to define the shape as thermal or donut, and one for the shape of the thermal or donut. The thermal definitions are for pads only and do not appear in padstack names. The following table lists the shapes used for Pads and Padstacks.

SHAPE		DESCRIPTION
C		Circular (Round) Pads (Ex. **C2125** = Circular 2.125mm pad)
S		Square Pads (Ex **S2125** = Square 2.125mm pad)
G		Octagonal Pads (elongated if both X and Y dimensions are given) (Ex. **G2125** = Octagonal 2.125mmpad)
R		Rectangular Pads (Ex. **R2125X1500** = Rectangular 2.125mm X 1.500mm pad)
B		Obround Pads (rounded on both ends) (Ex. **B2125X1500** = Obround 2.125mm X 1.500mm pad)
F		Finger Pads (round one end, square other end) (Ex. **F7000X1500** = Finger 7.000mm X 1.500mm pad)
SU		Custom Pads
DC		Donut Pads Circular (defined with internal and external diameters, see modifiers table below)
DS		Donut Pads Square (defined with internal and external size, see modifiers table below)
TC		Thermal Pads Circular (defined by the drill size) (Ex. **TCD100** = drill 1.00mm)
TS		Thermal Pads Square (defined by the drill size) (Ex. **TSD100** = drill 1.00mm)
TB		Thermal Pads Obround (defined by the drill size) (Ex.**TBD125X100** = drill 1,25 x 1.00mm)
TR		Thermal Pads Rectangular (defined by the drill size) (Ex. **TRD125X100** = drill 1,25 x 1.00mm)

Figure 6.2 Pad & Padstack Shapes

Padstack Types

The Type of a padstack indicates its usage in a design environment. For example, if a padstack is defined as SMD, then the CAD tool knows this is a single layer padstack on either the top or bottom surface and does not expect to find any internal layer entities in the padstack. Type and Shape parameters may be separated with underscore character (_) for more naming clarity. The following table lists the library padstack types and usage.

TYPE	DESCRIPTION
FID	Fiducial. (Ex. **FID_CELL_1000_[smask size]** = 1.000mm diameter fiducial.
MHP	Mounting Hole Plated. (See section 2.17.3 for Mounting Hole naming conventions)
MHN	Mounting Hole Non-plated. (See section 2.17.3 for Mounting Hole naming conventions)
S	Surface Mount (Ex. **SR2000X1550** = surface mount Rectangle 2.000mm X 1.550mm)
SU	Custom padstack (See section 2.18 for custom padstack naming conventions)
T	Through Hole (Ex. **THP110S1600** = through hole plated 1.10mm hole with square 1.600mm pad)
V	Via (Ex. **V025C0550** = Via 0.250mm hole 0.550mm pad

Figure 6.3 Padstack Types

Fiducials

The library includes **FID_CELL** for fiducials built in to cells and **FID_GLOBAL** for fiducials placed on the PCB. The parameters for these are as follows.

FID_CELL_0750 = 0.750mm pad, with 2.250mm soldermask opening.
FID_CELL_1000 = 1.000mm pad, with 2.500mm soldermask opening.
FID_GLOBAL = 1.000mm pad, with 2.400mm soldermask opening.

These may be modified or used as is. The default soldermask opening sizes are show above but alternate soldermask opening sizes or other modifications can be added with further _suffix modifiers

Note: Global fiducials are defined with paste mask the same size as the pad to allow for the solder stencil alignment.

Modifiers

There are many options for both Pads and Padstacks that would make full naming very complex and result in excessively long names. The library uses modifiers at the end of names to define any deviations from default values. Modifiers always appear at the end of the names and there may be multiple modifiers, (separated by underscore characters), present in the name. Modifiers are used to define soldermask, solderpaste, via properties, usage type and other miscellaneous padstack conditions. Some modifiers have optional parameters used to specify entity sizes in one or both axes.

The following tables list the modifiers and options used to customize pads or padstacks. When multiple modifier are required for the same padstack the order of modifiers after the padstack base name should be Top – Internal – Bottom – Solder Mask – Solder Paste – Miscellaneous.

Note that not all modifiers outlined herein are currently used in the library. There are many that are included for future use.

Soldermask Modifiers

The table on the following page lists and defines padstack soldermask modifiers used in the library.

Modifier	Options	Description
NSM		**N**o **S**older **M**ask. There is no mask opening defined on either side of the board.
SSM	[**Xsize** [**X Ysize**]]	**S**pecified **S**ize **M**ask. Defines a non default size mask opening on the mount side for surface mount padstacks or on both sides of the board for through hole padstacks. For through hole padstacks both top and bottom mask openings will be the same. (Ex. **_SSM2250** indicates 2.250mm size mask opening).
SBM	[**Xsize** [**X Ysize**]]	**S**pecified **B**ottom **M**ask. Defines a non default size mask opening on the bottom side of a through hole padstack. The top side mask opening will be the default size unless overridden with another modifier. Not required for surface mount padstacks as **_SSM** would be used. (Ex. **_SBM2250** indicates 2.250mm mask opening on the bottom side).
STM	[**Xsize** [**X Ysize**]]	**S**pecified **T**op **M**ask. Defines a non default size mask opening on the top side of a through hole padstack. The bottom side mask opening will be the default size unless overridden with another modifier. Not required for surface mount padstacks as **_SSM** would be used. (Ex. **_STM2250** indicates 2.250mm mask opening on the top side).
BSM	[**Xsize** [**X Ysize**]]	**B**ottom **S**older **M**ask. Defines a through hole padstack with bottom mask opening only. Use the optional size parameter [**Xsize** [**X Ysize**]] if the mask size is different than the default size. Used for through hole padstacks only. (Ex. **_BSM2250** indicates 2.250mm mask on bottom side with no mask opening on top side).
TSM	[**Xsize** [**X Ysize**]]	**T**op **S**older **M**ask. Defines a through hole padstack with top mask opening only. Use the optional size parameter [**Xsize** [**X Ysize**]] if the mask size is different than the default size. Used for through hole padstacks only. (Ex. **_TSM2250** indicates 2.250mm mask on top side with no mask opening on bottom side).
CAPB	[**Xsize** [**X Ysize**]]	**CAP B**ottom. Defines a bottom side mask cap. The top side has a default size mask opening unless overridden by another modifier. Use the size parameters to specify the actual size of the cap. This modifier is defined primarily for use on via padstacks. See section 2.10 for via capping notes.
CAPT	[**Xsize** [**X Ysize**]]	**CAP T**op. Defines a top side mask cap. The bottom side has a default size mask opening unless overridden by another modifier. Use the size parameters to specify the actual size of the cap. This modifier is defined primarily for use on via padstacks. See section 2.10 for via capping notes.
TNTB		**TeNT B**op. Defines a tented mask, no mask opening, on the bottom side. The top side has the default mask opening unless overridden with another modifier. This modifier is defined primarily for use on via padstacks.
TNTT		**TeNT T**op. Defines a tented mask, no mask opening, on the top side. The bottom side has the default mask opening unless overridden with another modifier. This modifier is defined primarily for use on via padstacks.

Figure 6.4 Soldermask Modifiers

Via Capping Notes

Via capping is a method of producing what is traditionally known as ‘tented’ or ‘covered’ vias. A fab shop will typically leave all vias unmasked to allow proper cleaning of the board after processing, and then ‘cap’ the vias with a secondary process. This requires separate output files to define the via locations to be capped on either the top or bottom of the board. Capping should only be applied on one side of a via to avoid trapped air pockets which can cause blowouts during the assembly process. Capping may be used on both sides of the board but not both sides of the same via. When implementing via capping we suggest using User Draft Layers named **User Via Cap Top** and **User Via Cap Bottom**. These layers will need to be added to your Gerber and ODB output configurations to suit your fabrication and assembly processes.

In PADS we suggest using the same layer names, with User Via Cap Top as layer 16 and User Via Cap Bot as layer 17. The use of the cap layers in this manner means that there will be a maximum of 14 copper layers available before switching to Max Layers.

Solder Paste Modifiers

The following table outlines the modifiers used in the padstack names to represent various solderpaste conditions.

Modifier	Options	Description
NSP		**N**o **S**older **P**aste. There is no paste defined for either side of the board in this padstack.
SSP	[**Xsize** [**X Ysize**]]	**S**pecified **S**ize **P**aste. Defines a specified size solder paste on both sides of the board or only one side for surface mount . Use the size parameters to define the actual size of the solderpaste. The solder paste size defined is used on both sides of the board.
BSP	[**Xsize** [**X Ysize**]]	**B**ottom **S**pecified **P**aste. Defines a specified size solder paste on the bottom side. Use the size parameters to specify the actual size of the solder paste. Top solder paste, if present, is the default size unless overridden with another modifier.
TSP	[**Xsize** [**X Ysize**]]	**T**op **S**pecified **P**aste. Defines a specified size solder paste on the top side. Use the size parameters to specify the actual size of the solder paste. Bottom solder paste, if present, is the default size unless overridden with another modifier.

Figure 6.5 Solder Paste Modifiers

Miscellaneous Padstack Modifiers

Miscellaneous modifiers are used to define any pad or padstack conditions that are not solder mask or solder paste related. These modifiers can define offsets, built in obstructs, different pad size on specific layers etc. The following table lists the modifiers and their usage.

Modifier	Options	Description
BOT		Specifies a **BOT**tom layer surface mount pad.
BTH		**B**uried **TH**ermal. Defines a padstack no plane thermal relief pads defined. The result is that the inner plane connections are buried in solid copper without thermal relief. Some tools do not allow this to be defined in the planes generation phase, particularly when using negative planes. Not used for via padstacks as they default to buried.
BTP	[**Xsize** [**X Ysize**]]	**B**o**T**tom **P**ad size. Defines the size of the bottom layer pad in a through hole padstack when it is not the same size as the top layer pad.
INP	[**Xsize** [**X Ysize**]]	**IN**ternal **P**ad size. Defines the size of the internal layer pad in a through hole padstack when it is not the same size as the top layer pad.
OBS	[**Xsize** [**X Ysize**]]	**OBS**truct shape. Defines a route obstruct associated with the padstack. The obstruct will retain the same geometric shape and origin as the padstack. Use the size parameters to define the actual size of the obstruct.
OFF	[**Xsize** [**X Ysize**]]	**OFF**set origin. Defines a pad or padstack with an origin that is not the geometric center. The offset may be in either the X, Y or both axes. Ex1. For X axis only. _**OFF0290** = Offset 0.290mm in the X axis only. Ex2. For X and Y axes. (_**OFF0290X0200** = Offset 0.290mm in the X axis and 0.200mm in the Y axis). Ex3. For Y axis only (_**OFFY0200** = Offset 0.20mm in the Y axis only). Padstacks with a single axis offset (X OR Y) can be reliably rotated. Padstacks with a dual axes offset (X AND Y) cannot be reliably rotated so all required rotations must be defined. Offset parameters may be either positive or negative. Offsets may be specific to a padstack layer. This is indicated by adding the **OFF** modifier to a layer modifier without a leading "_" Ex4. _**SR1000X0500_SSM1100X0600OFF0050** defines a padstack with a +0.050mm offset solder mask only. Ex5. _**SR1000X0500_SSM1100X0600_OFF0050** defines a padstack with all pads offset +0.05mm.
PCH		**P**un**CH**ed. Defines a hole that is to be punched rather than drilled. Most commonly used to create a square rather than a round hole. The X and Y dimensions of the hole itself are specified in the preceding drill size portion of the name.
PFIT		**P**ress **FIT**. Defines a padstack with a very specific hole size tolerance for press fit pins. The tolerance is usually defined from the component manufacturers datasheet. Since press fit pins are not soldered there is no thermal defined in these padstacks.
TOL	[**+size** [**X -size**]]	Drill **TOL**erance. Defines a specific drill tolerance. Tolerances are specified to 3 significant digits. If the negative tolerance is different than the positive tolerance then the [X-size] parameter is used. **TC1500D1000P_TOL0105** defines a tolerance of +/-0.105mm. **TC1500D1000P_TOL0105X0075** defines a tolerance of +0.105mm/-0.075mm.
VT		**VT** indicates a hole with a Via Tolerance. The positive tolerance is 0.075mm and the negative tolerance is equal to the hole size, allowing for plated closed vias.
UV		**UV**ia. Defines a via as a microvia. The capture pad is often a different size, so use the _INP modifier to define the capture pad size. Since a microvia needs no soldermask, use the _NSM modifier to define this.
THRM		**TH**e**RM**al via. Defines a via with a thermal relief for planes. The default condition for vias in the library is buried in planes. Use this modifier when thermal relief is needed for vias.
BWT		**B**ottom **W**ave **T**echnology. Defines a surface mount padstack with a different size pads, mask and paste for use when bottom mounted for wave soldering. This modifier is also applied to land patterns that use these padstacks.

Figure 6.6 Miscellaneous Padstack Modifiers

Donut Pads

Donut pads are defined with two characters. The first is **D** to define Donut. The second is the donut shape, either **C** (Circular) or **S** (Square). This is followed by two dimensions. The first dimension is the outer diameter of a circular donut or the outer size of a square donut. This is followed by the letters **IDC** (Circular) or **IDS** (Square) and a second dimension, which is the internal diameter of a circular donut or the internal size of a square donut. Other modifiers defined in this document can then be applied to the donut as necessary.

Examples.

- **DC2250IDC1850** defines a circular donut with an outer diameter of 2.250mm and an inner diameter of 1.850mm.
- **DS2250IDS1850_SSM2400_OFF0500** defines a square donut with an outer size of 2.250mm, an inner size of 1.850mm, a specified solder mask on both top and bottom sides of 2.400mm and the entire padstack is offset by 0.500mm in the X axis.

Plane Clearance and Thermals

The plane clearance sizes are based on the drill size. A range of values have been provided based on different ranges of drill sizes in the following table. These values minimize the possibility of overlapping clearance pads on inner planes that can potentially cause a 'slot' to develop. Use the plane clearance calculation to determine the default route obstruct when necessary. The route obstruct dimension may be modified at the librarians discretion to allow for pin to pin spacing issues or screw head diameter issues. When an elongated padstack has X and Y dimensions that fall into different ranges in the table, the range that is correct for each dimension should be used. For example, a padstack of THP270X090B3300X1500 is a slotted hole 2.70mm x 0.90mm with an obround pad 3.300mm x 1.500mm. In this case the clearance in the X dimension is 1.000mm over the drill size, but in the Y dimension it is only 0.500mm over the drill.

Thermal connection pads are also based on the drill size using the ranges defined in the tables below. When more specific control of the thermal pad parameters is needed there are three modifiers available. See the table in Figure 6.10 Thermal Pad Modifiers, for more details about these modifiers.

Figure 6.7 shows the different parts of a thermal relief pad.

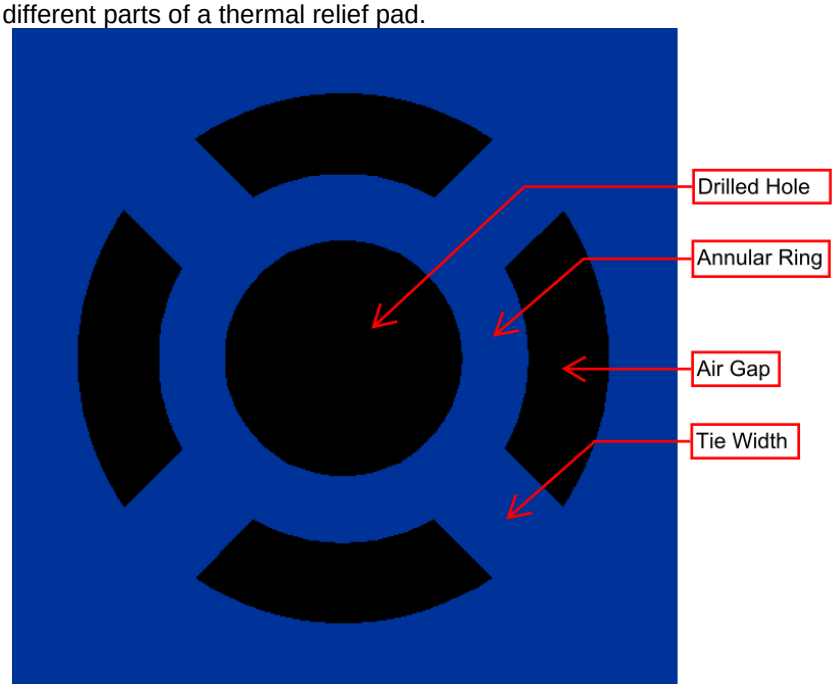

Figure 6.7 Thermal Relief Pad

The following tables define the plane clearance and thermal relief parameters for default condition padstacks based on drilled or slotted hole dimensions.

DRILL DIA RANGE	PLANE CLEARANCE / ROUTE OBSTRUCT	THERMAL ANNULAR RING	THERMAL AIR GAP
0.00 - 0.25mm	DRILL + 0.40mm	DRILL + 0.30mm	0.15mm
> 0.25 - 0.99mm	DRILL + 0.50mm	DRILL + 0.50mm	0.25mm
> 0.99 - 1.5mm	DRILL + 0.75mm	DRILL + 0.75mm	0.30mm
> 1.5mm	DRILL + 1.00mm	DRILL + 1.00mm	0.35mm

Figure 6.8 Plane & Thermal Relief Clearance

*Thermal air gap is the gap between the inside and outside diameters of the thermal relief.

The tie width is more variable and is shown in the following table. For elongated padstacks, the tie width is chosen based on the range in the table that the smaller of the two hole dimensions falls within.

DRILL DIA RANGE	THERMAL TIE WIDTH
0.00 - 0.25mm	0.20mm
> 0.25 - 0.75mm	0.25mm
> 0.75 - 1.10mm	0.30mm
> 1.10 - 1.50mm	0.50mm
> 1.50 - 2.00mm	0.65mm
> 2.00mm	0.80mm

Figure 6.9 Tie Width

Thermal Pad Modifiers

The following modifiers are available to provide a more detailed definition of a thermal pad when the default hole size based thermals are not suitable.

Modifier	Options	Description
G	[**Xsize** [**X Ysize**]]	**G**. Defines the Air Gap in a thermal relief pad. The air gap is the difference between the internal and external diameters of the pad and is the area of copper removed for thermal relief.
T	[**Xsize** [**X Ysize**]]	**T**. Defines the width of the copper spokes connecting the inside of a thermal pad to the plane outside the air gaps.
A	[**Xsize** [**X Ysize**]]	**A**. Defines the annular ring between the drilled hole and the inside of the air gap in a thermal pad.

Figure 6.10 Thermal Pad Modifiers

Thermal Pad Naming Convention

There are two ways to name a thermal pad, drill size based and full detail.

Drill size based naming is simply the shape of the thermal followed by **D** and then the hole size
.
Ex1. **TCD125** Defines a circular thermal pad for a 1.25mm drilled hole.
Ex2. **TBD125X100** Defines an obround thermal pad for a 1.25mm X 1.00mm slotted hole.

Full detail naming is the shape of the thermal followed by **D** and then the drill size the same as the drill size based naming method, and then followed by separate specific parameters for the Annular Ring, Air Gap and Tie Width.
Ex1. **TCD125A0120G0100T0120** Defines a circular thermal pad for a 1.25mm drilled hole with a 0.120mm annular ring, a 0.100mm air gap and four 0.120mm wide thermal ties at 45 degrees.
Ex2. **TBD125X100A0300XG0300T0250** Defines an obround thermal pad for a 1.25mm X 1.00mm slotted hole with a 0.300mm annular ring, a 0.300mm air gap and four 0.250mm thermal ties at 45 degrees.

Mounting Holes

The following defines both non-plated and plated mounting holes parameters.

• Non-Plated Mounting Hole

The following table outlines the default pad size per drill size range for non plated mounting holes:

DRILL DIA RANGE	Non Plated Mount Hole Pad Size
0.20mm - 0.75mm	0.150mm
0.80mm – 1.50mm	0.500mm
1.55mm – 3.00 mm	1.000mm
> 3.00mm	2.000mm

Figure 6.11 Default Non-Plated Pad Size per Drill Size

An octagonal pad is used to indicate a non plated hole, or an Elongated Octagonal pad for a non plated slot. For non plated slotted holes the dimensions of the elongated octagon pad are determined in X and Y axes by the range in table in figure 6.11 that the slot dimension in that axis falls within.

A route obstruct is used around non-plated mounting holes to ensure clearance to copper on all pcb layers. Refer to the table in figure 6.8 to determine the default route obstruct diameter.

• Plated Mounting Hole

The table, Drill dimensions in figure 6.13 outlines the default pad size per drill size range for non plated mounting holes. Pad sizes may often vary from these defaults according to what is required by manufacturer specifications.

If the drill dimensions for a slot through hole falls into different ranges in the table, the annular ring in each axis is based on the range that matches the dimension in that axis.
The clearance to other copper for plated mount holes is controlled in the clearance rules within the layout tool.

• Mounting Hole Naming Convention

The naming convention for mounting holes lists the Plating type first, followed by the hole dimensions, the pad shape, and the pad dimensions as follows:
MH [P/N] Xsize [X Ysize]] PadShape Xsize [X Ysize]
Examples:
MHP300C4000 defines a 3.00mm diameter Plated hole with a 4.000mm diameter circular pad.
MHP250S3800 defines a 2.50mm diameter Plated hole with a 3.800mm square pad.
MHP150X075B2250X1250 defines a 1.50mm X 0.75mm Plated slot with a 2.250mm X 1.250mm obround pad.
MHN300 defines a 3.00mm diameter Non-plated hole. (pad sized according to the table in figure 6.11).
MHN495X445 defines a 4.95mm X 4.45mm Non-plated slot. (pad sized according to the table in figure 6.11).

Note: The only pad shapes used for Non plated holes are octa**G**on and elon**G**ated octagon.

Custom Padstacks

Custom padstacks are padstacks that have freeform shapes. The naming convention is **SU_*suffixes*** . The suffixes can be anything and can include sizes, manufacturer names and part numbers, manufacturer package numbers or anything else that aptly names the padstack.

Example Padstack Names

Padstack Name	Description
V035C0600	via padstack. 0.35 plated hole with a 0.600mm circular pad.
V030C0600_CAPT0600_BSM0450	via padstack. 0.30mm plated hole with a 0.600mm circular pad. The padstack has a Top solder mask cap of 0.600mm and a bottom side defined soldermask of 0.450mm. This is a typical capped top side via padstack with solder mask defined bottom side.
SC1000	surface mount circular padstack of 1.00mm diameter.
SR1050X0600	surface mount rectangular padstack 1.050mm X 0.600mm.
THP065B1150X0800_OFF0100	through hole obround padstack . 0.65mm plated hole with a1.150mm X 0.800mm obround pad and on origin offset by +0.100mm in the X axis only.
MHN330	3.30mm non plated mounting hole.
MHP280C3800	mounting hole padstack. 2.80mm plated hole with a 3.800mm circular pad.
THP050C1000	through hole padstack. 0.50mm plated hole with a 1.000mm circular pad.
THP330S4600	through hole padstack. 3.30mm plated hole with a 4.600mm square pad.

Figure 6.12 Example Padstack Names

Drill Dimensions

Drill diameters are rounded up to the nearest 0.05mm. This table shows the drill size used based on the lead diameter when the hole size is not defined by the manufacturer.

Press fit pins do not follow this rule, they are defined with the size and tolerance specified in the manufacturer data sheet.

The minimum annular ring and pad size for each drill diameter is also referenced. The annular ring may be reduced at the librarian's discretion if the pin to pin spacing is an issue.

LEAD DIA <=	DRILL DIA <=	PAD DIA <=	ANNULAR RING
0.05	0.40	0.90	
0.10	0.45	0.95	
0.15	0.50	1.00	
0.20	0.55	1.05	
0.25	0.60	1.10	
0.30	0.65	1.15	
0.35	0.70	1.20	0.50
0.40	0.75	1.25	
0.45	0.80	1.30	
0.50	0.85	1.35	
0.55	0.90	1.40	
0.60	0.95	1.45	
0.65	1.00	1.50	
0.70	1.05	1.55	
0.75	1.10	1.85	
0.80	1.15	1.90	
0.85	1.20	1.95	
0.90	1.25	2.00	
0.95	1.30	2.05	
1.00	1.35	2.10	
1.05	1.40	2.15	
1.10	1.45	2.20	
1.15	1.50	2.25	0.75
1.20	1.55	2.30	
1.25	1.60	2.35	
1.30	1.65	2.40	
1.35	1.70	2.45	
1.40	1.75	2.50	
1.45	1.80	2.55	
1.50	1.85	2.60	
1.55	1.90	2.65	
1.60	1.95	2.95	
1.65	2.00	3.00	
1.70	2.05	3.05	
1.75	2.10	3.10	
1.80	2.15	3.15	
1.85	2.20	3.20	
1.90	2.25	3.25	1.00
1.95	2.30	3.30	
2.00	2.35	3.35	
2.05	2.40	3.40	
2.10	2.45	3.45	
2.15	2.50	3.50	
2.20	2.55	3.55	
>= 2.25	>= 2.6		1.3

Figure 6.13 drill and pad size parameters

Land patterns

Parts are created to IPC standard or to manufacturer recommended land patterns if IPC does not apply.

Land Pattern Naming Conventions

The naming conventions used in the library are based on IPC7351 naming convention but not exactly the same as IPC7351B.
The key differences are
Land pattern names do not include height; the height is determined at the pdb level.
There is a length (D) dimension added to the land pattern names for dual in line parts such as SOICs and SOPs
Some land patterns retain naming conventions from previous IPC7351 versions .These land patterns conform to IPC7351B, it is only the name that is from the earlier version.

Naming conventions rules

- Units of measure - Dimensions are defined using the metric system. In some instances, imperial (inch) units may be appended to the land pattern name. This is done to reduce confusion between the metric dimension and the commonly used industry name. Each component naming convention will have the resolution defined in its description. An example is the metric 0603, which is commonly known as an industry 0201.
- Leading and trailing zeros - Leading zeros are not required. Trailing zeros are required to meet the components resolution definition.
- Land pattern name length will be a maximum of 31 characters.
- Typographical Convention.
  - The _ (underscore) is used as a separator between different fields of a land pattern name. The underscore may also be used in place of the period (.) character.
  - The – IPC uses the dash as a separator for the pin quantity field, the dash is replaced by an underscore in this library for this purpose. The dash is also used within the pin qty to determine missing numbers of pins, i.e. 24-28 indicates a 28 pin package in which only 24 pins are used.
  - The X (uppercase letter X) is used between dimensions. LengthXWidthXHeight.
  - The M, N, L, Q, suffixes are to appear at the end of every common SMD land pattern name They represent Maximum, Nominal, and Least land size conditions respectively. This rule excludes BGA packaged land patterns where only nominal is defined. The Q suffix denotes that the manufacturer recommended land pattern has been used for the land pattern.
  - THROUGH–HOLE components do not use a density level suffix.
  - The ( ) is used to denote required information to be added to the naming convention.
  - The [ ] is used to denote optional information to be added to the naming convention.
  - Only alphanumerics, underscores “_”, and dashes “–“ are acceptable characters.
  - Defined Suffixes - The suffixes on the following page have been defined for various different component types.

- **Defined Suffixes**

_D####	Length of body of dual in line components, SOIC, SOP etc.
_SKT	Socket as in IC or relay (not used on connectors).
_HS####	Heatsink. Used to denote the pad size for a thermal pad. If used, it will appear immediately prior to M, N, L at the end of the name or at the end for BGA and through-hole package land patterns.
_VIA	Vias. Used for mounting holes with a via ring. If used, it appears immediately prior to M, N, L at the end of the name or at the end for BGA and through-hole package land patterns.
_T or TVIA	Thermal pad or Thermal pad with embedded vias. If used, it appears immediately prior to M, N, L at the end of the name or at the end for BGA and through-hole packages.
_###	Used to define alternate pin numbering scheme where ### = pin numbers/letters when the land pattern is viewed in the IPC defined zero orientation. Typically used on SOT and TO devices. Typical examples are SOT95P237_3_D290_231N, SOT95P237_3_D290_BECN, SOT95P237_3_D290_GSDN.
_P2	Denotes that the positive is pin 2 on polarized packages (default is positive on pin1).
_BIDIR	Bidirectional version of normally polarized devices i.e electrolytic capacitors and diodes etc.
_RA	Denotes Right Angle.
_IS	Optional suffix used to show the commonly used industry wide name for a given part. An example is the metric 0603, which is commonly known as an industry 0201.
_C1	Pin 1 is located at the center of the package instead of the expected corner.
_#	Arbitrary suffix used for denote different cells that would otherwise have the same land pattern name. Start with 1 and increment by 1 for each alternate cell. Denote differences in the description field.
_24-26	Denotes 24 pins in a 26 pin package.
_GW	denotes gull wing leads
_J	Denotes “J” leads.
_PD#	Denotes the physical pin diameter.
_RV	Denotes that a reverse pinout is used i.e. 654321 instead of 123456.
_PMH	Denotes that Plated Mounting Holes are used for mounting pins.
_BWT	Denotes Bottom Wave Technology
_TDN	Denotes tie down holes built in to the land pattern.

Figure 6.14 Defined Suffixes

- **Naming convention IPC table**

Description / Category	IPC Land pattern Name	suffixes
Ball grid array	**BGA**(pitch)**P**(#_of_pin_col)**X**(#_ of_pin_rows)_(Pin_qty) _(body_width**X**length) (DL)	
Ball grid array with different pin spacing in x and y	**BGA**(xpitch)**X**(ypitch)**P**(#_of_pin_col)**X**(#_ of_pin_rows)_(Pin_qty) _(body_width**X**length) (DL)	
Ball grid array with staggered pins	**SBGA**(pitch)**P**(#_of_pin_col)**X**(#_ of_pin_rows)_(Pin_qty) _(body_width**X**length) (DL)	
Capacitor, Chip, Polarized	**CAPCP**(body size)(DL)	_(body_size_ths)
Capacitor, Chip, Non-polarized	**CAPC**(body size)(DL) chip parts >9.99mm in either x or y will have 4 digit body size dimensions for both x and y using X as a separator i.e (9.14mmx10.20mm = 9140X1020)	_(body_size_ths)
Capacitor, Chip, Wire Rectangle	**CAPCWR**(body size)(DL)	_(body_size_ths)
Capacitor, Chip, Array	**CAPAS**_(mfr)_(mfr_sern)_(Pin_qty) (DL)	
Capacitor, Molded, Non-polarized	**CAPM**(body size)(DL)	
Capacitor, Molded, Polarized	**CAPMP**(body size)(DL)	
Capacitor, Aluminum Electrolytic	**CAPAE**(base body width)**W**(height)**H**(DL)	
Ceramic Flat Package	**CFP127P**(Lead Span L1)_(Pin_qty)(DL) **_D**(body_length)	
Column Grid Array	**CGA**(#_of_pin_col)**X**(#_ of_pin_rows)_(Pin_qty)(DL)	
Diode, Molded	**DIOM**(body size)(DL)	
Diode, MELF	**DIOMELF**(body size)(DL)	
Inductor, Chip	**INDC**(body size)(DL) chip parts >9.99mm in either x or y will have 4 digit body size dimensions for both x and y using X as a separator i.e (9.14x10.20 = 9140X1020)	_(body_size_ths)
Inductor, Chip, Array	**INDAS**_(mfr)_(mfr_sern)_(Pin_qty) (DL)	
Inductor, Molded	**INDM**(body size)(DL)	
Inductor, Precision Wire Wound	**INDP(**body size)(DL)	
Plastic Leaded Chip Carrier Square	**PLCC**(pitch)**P**(Lead Span L1)**X**(Lead Span L2)_(Pin_qty)	
Plastic Leaded Chip Carrier Sockets Square	**PLCCS**(pitch)**P**(Lead Span L1)**X**(Lead Span L2)_(Pin_qty)	
Quad Flat Package	**QFP**(pitch)**P**(Lead Span L1)**X**(Lead Span L2)_(Pin_qty)(DL)	

Description / Category	IPC Land pattern Name	suffixes
Ceramic Quad Flat Package	**CQFP**(pitch)**P**(Lead Span L1)**X**(Lead Span L2)_(Pin_qty)(DL)	
Quad Flat No Lead Package	**QFN**(pitch)**P**(body_width)**X**(body_length)_(Pin_qty)_(HS####) or (JEDEC #) OR (CC###)(DL)	
Quad Leadless Ceramic Chip Carrier	**LCC**(body_width)**X**(body_length)**_**(Pin_qty)(DL)	
Quad Leadless Ceramic Chip Carrier (Pin 1 on the Side)	**LCCS**(body_width)**X**(body_length)**_**(Pin_qty)(DL)	
Quad Bottom Chip Carrier	**QBCC**(body_width)**X**(body_length)**_**(Pin_qty)(DL)	
Resistor, Chip	**RESC**(body size)(DL) chip parts >9.99mm in either x or y will have 4 digit body size dimensions for both x and y using X as a separator i.e (9.14x10.20 = 9140X1020)	**_IS**(body_size_ths)
Resistor, Chip, Array	**RESAS** (Pin_qty) _(mfr_sern)_(Pin_qty) (DL)	
Resistor, Molded	**RESM**(body size)(DL)	
Resistor, MELF	**RESMELF**(body size)(DL)	
Small Outline IC, J-Leaded	**SOJ**(pitch)**P**(Lead Span)_(Pin_qty)**_D**(body_length)(DL)	
Small Outline Integrated Circuit 1.27mm Pitch, (Standard SOIC)	**SOIC**(pitch)**P**(Lead Span)_(Pin_qty)**_D**(body_length)(DL)	
Small Outline Package (Non-Standard SOICs) > .50mm pitch, > 1.6mm height	**SOP**(pitch)**P**(Lead Span)_(Pin_qty)**_D**(body_length)(DL)	
Small Outline Diode	**SOD**(Lead Span)(body_width)(DL)	
Small Outline Narrow Dual No Lead Package	**SON**(pitch)**P**_(body_width)**X**(body_length)_(Pin_qty)[Thermal_pad] or (mfr_pkgn) or (mfr_prtn) (DL) or (JEDEC #)	
Small Outline Transistor Package (JEDEC Standard Package)	**SOT**(JEDEC #)[R](DL)	
Small Outline Transistor Package (Generic Package)	**SOT**(pitch)**P**(Lead Span)_(Pin_qty)(DL)	
Transistor Single Outline Package (Generic DPAK)	**TO**(pitch)**P**(Lead Span)_(Pin_qty)**D**(body_length) (DL)	

Figure 6.15 IPC Naming Convention

- **Naming Convention Non IPC table**

Description / Category	IPC Land pattern Name	Notes
Capacitor, SMD	**CAPS**(Pin_qty)_(mfr)_(mfr_pkgn)or(mfr_sern)or (mfr_prtn)(DL)	For any non-chip/non-molded SMD capacitors
Capacitor, Through_hole	**CAPT**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn) or CAPT(Pin_qty)_(pitch)P(body_widthXlength)_PD(PinDia)	
Capacitor, Aluminum Electrolytic, Through_hole, Axial	**CAPAETA**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn) or **CAPAETA**(Pin_qty)_(pitch)**P**(body_width**X**length)	
Capacitor, Aluminum Electrolytic, Through_hole, Radial	**CAPAETR**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn) or **CAPAETR**(Pin_qty)_(pitch)**P**(body_width**X**body_height)	
Capacitor, Variable, SMD	**CAPVS**(Pin_qty)_(mfr)_(mfr_pkgn)or(mfr_sern)or (mfr_prtn)(DL)	
Capacitor, Variable, Through_hole	**CAPVT**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)	
Connector, SMD	(mfr)_(mfr_pn)	
Connector, Through_hole	(mfr)_(mfr_pn)	
Connector, Edge Fingers	**CFIN**_(standrd)_(Pin_qty)_(arbq)pitch, bits, volt lanes etc_(arb#) or **CFIN**(Pin_qty)_(pitch)_(arb#) or **CFIN**_(mfr)_(mfr_pn)	
Connector, Terminal Strip Header , SMD	**CTSS(pitch)P(rows)(angle)(Pin_qty)**	
Connector, Terminal Strip Header , Through_hole	**CTST(pitch)P(rows)(angle)(Pin_qty)**	
Battery, SMD	**BATS**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)(DL)	**BATHS** = BatteryHolder SMD
Battery, Through_hole	**BATT**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)	**BATHT** = BatteryHolder Through Hole
Bridge Rectifier, SMD	**BRIDGS**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)(DL)	
Bridge Rectifier, Through_hole	**BRIDGT**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)	
Crystal, SMD	**XTALS**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)(DL)	Make to manuf. Spec when possible.
Crystal, Through_hole	**XTALT**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)	
Diode, SMD	**DIOS**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)(DL)	For any non-molded/non-melf SMD diodes
Diode, Through_hole	**DIOT**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)	
Diode, Array SMD	**DIOAS**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)(DL)	
Diode, Array Through_hole	**DIOAT**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)	

Description / Category	IPC Land pattern Name	Notes
Filter, SMD	**FILS**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)(DL)	
Filter, Through_hole	**FILT**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)	
Fuse, SMD	**FUSS**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)(DL)	**FUSHS** = FuseHolder SMD
Fuse, Through_hole	**FUST**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)	**FUSHT** = FuseHolder Through Hole.
IC, Dip (body width inside lead leadspan)	**DIP**(pitch)**P**(Lead Span)_(Pin_qty) _**D**(body_length)	
IC, Dip (body width outside lead leadspan) i.e sockets etc	**DIP**(pitch)**P**(Lead Span)_(Pin_qty)_(body_width**X**length)	_SKT
IC, MISC	(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)(DL)	
Inductor, SMD	**INDS**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)(DL)	For any non-chip/non-molded SMD inductors
Inductor, SMD, power inductor	**INDS**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)Q	All power inductors will match the mfg. recommended land pattern.
Inductor, Through_hole	**INDT**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)	
LED, SMD	**LEDS**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)(DL) or **LEDS**(Pin_qty)_(body size)_(mfr)_(DL)	Body size convention may be used for chip type LEDs
LED, Through_hole	**LEDT**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn) or **LEDT**(Pin_qty)_(pitch)**P**(body_width**X**body_height)	
Mechanical	**MEC**(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)	
Miscellaneous, SMD	**PARTTYPES**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)(DL)	**PARTTYPE** = obvious part type abbreviation
Miscellaneous, Through_hole	**PARTTYPET**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)	**PARTTYPE** = obvious part type abbreviation
Module, SMD	**MODS**(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)_(Pin_qty)(DL)	
Module, Through_hole	**MODT**(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)_(Pin_qty)	
Mounting hole plated Metric	**Mx###D###P**_Suff where x### = pad shape and size , D### = drill size x = C for CIRCLE, S for SQUARE, B for OBLONG	.01mm resolution Suff = SSM### for specified solder mask Various other suffixes may be used
Mounting hole non plated Metric	**Mx###D###N**_Suff where x### = pad shape and size , D### = drill size x = C for CIRCLE, S for SQUARE, B for OBLONG	.01mm resolution Suff = OBS### for built in route obstructs or SSM### for specified mask, other suffixes may be used
Mounting hole plated Imperial	**MxI###D###P**_Suff where x### = pad shape and size , D### = drill size x = C for CIRCLE, S for SQUARE, B for OBLONG	.001 inch resolution Suff = SSM### for specified solder mask Various other suffixes may be used

Description / Category	IPC Land pattern Name	Notes
Mounting hole non plated Imperial	**MxI###D###N**_Suff where x### = pad shape and size , D### = drill size x = C for CIRCLE, S for SQUARE, B for OBLONG	.001 inch resolution Suff = OBS### for built in route obstructs or SSM### for specified mask Various other suffixes may be used
Oscillator, SMD	**OSCS**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)(DL)	Made to manuf. Spec when possible.
Oscillator, Through_hole	**OSCLT**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)	
Resistor, SMD	**RESS**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)(DL)	For any non-chip/non-molded SMD resistors
Resistor, Through_hole Mfr specific	**REST**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)	
Resistor, Through_hole Generic Axial	**RESTA**(Pin_qty)**P**(body_width**X**length)	
Resistor, Through_hole Generic Radial	**RESTR**(Pin_qty)**P**(body_width**X**length)	
Resistor Pack, SMD	**RESAS**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)(DL)	
Resistor Pack, Through_hole	**RESAT**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)	
Resistor Pack, Through_hole Generic	**RESAT**(Pin_qty)**P**(body_width**X**length)	
Resistor, Pot SMD	**RESPS**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)(DL)	
Resistor, Pot Through_hole	**RESPT**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)	
Relay, SMD	**RLYS**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)(DL)	**RLYSS** = Relay Socket SMD
Relay, Through_hole	**RLYT**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)	**RLYST** = Relay Socket Through Hole
Sensor, SMD	**SENS**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)	
Sensor, Through_hole	**SENT**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)	
Speaker, SMD	**SPKS**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)(DL)	
Speaker, Through_hole	**SPKT**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)	
Switch, DIP, SMD	**SWDPS**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)(DL)	
Switch, DIP, Through_hole	**SWDPT**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)	
Switch, Push, SMD	**SWPBS**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)(DL)	
Switch, Push, Through_hole	**SWPBT**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)	
Switch, Rotary, SMD	**SWRTS**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)(DL)	

Description / Category	IPC Land pattern Name	Notes
Switch, Rotary, Through_hole	**SWRTT**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)	
Switch, Slide, SMD	**SWSLS**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)(DL)	
Switch, Slide, Through_hole	**SWSLT**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)	
Switch, Toggle, SMD	**SWTGS**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)(DL)	
Switch, Toggle, Through_hole	**SWTGT**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)	
Test point, Pad In Circuit Test	**ICT_TP_SMD** _(IMPERIAL####X####SHAPE)	Shape is RD round, SQ square, R rectangle Name is in imperial units (thou)
Test point, Pad SMD Imperial	**TPIS**_(####X####**PAD**)	.001 inch resolution
Test point, Pad Through_hole Imperial	**TPIT**_(####**DRL**_####**PAD**)	.001 inch resolution
Test point, Pad SMD Metric	**TPMS**_(####X####**PAD**)	.01mm resolution
Test point, Pad Through_hole Metric	**TPMT**_(####**DRL**_####**PAD**)	.01mm resolution
Test point, Part SMD	**TPS**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)(DL)	
Test point, Part Through_hole	**TPT**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)	
Thermistor, SMD	**THR**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)(DL)	
Thermistor, Through_hole	**THR**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)	
Transformer, SMD	**XFMRS**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)(DL)	
Transformer, Through_hole	**XFMRT**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)	
Transient voltage suppressor (transzorb),SMD	**TVSS**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)(DL)	
Transient voltage suppressor (transzorb), Through_hole	**TVST**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)	
Varistor, SMD	**VAR**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)(DL)	
Varistor, Through_hole	**VAR**(Pin_qty)_(mfr)_(mfr_sern)_(CC###) or (mfr_prtn)	
Arbitrary	**(mfr)_(CC##)**	

Figure 6.16 Non IPC Naming Convention

- **Naming Convention Codes**

CODE	Definition	# of Characters
(#_of_pin_col)	# of pin columns	Max 3 characters, min 1 character
(#_of_pin_rows)	# of pin rows	Max 3 characters, min 1 character
(angle)	Straight - S or Right Angle - R	1 Character
(arb#)	Arbitrary number to distinguish mech named similar parts where required	Up to 31 characters in the name
(arbq)	Arbitrary qualifiers can be anything that makes sense	Up to 31 characters in the name
(body_length)	in metric – 11.27mm = 1127	Max 4 char, min 3 characters, .01 resolution
(body_size)	body size in metric, 0603	4 characters
(body_size_ths)	body size in thousandths, 0201	4 characters
(body_width**X**body_height)	in metric – 11.27mm = 1127	Max 4**X**4 char, min 2**X**2 characters, .01 resolution, median dimensions
(body_width**X**length)	in metric – 11.27mm = 1127	Max 4**X**4 char, min 2**X**2 characters, .01 resolution, median dimensions
(density)	STD standard or HD high density	Max 3 characters, min 2 character
(DL)	Density Level, M= Maximum, N= nominal, L= Least, Q = Manufacturer Specified	1 Character. If a surface mount device does not have a density level, assume a density level of Q. Through hole devices and devices that require additional land pattern requirements do not have a density level and are assumed to have a density level of Q.
(ibody_width**X**ibody_height)	in imperial – 0.100inch = 100	Max 4**X**4 char, min 2**X**2 characters, .001 resolution
(ibody_width**X**ilength)	in imperial – 0.100inch = 100	Max 4**X**4 char, min 2**X**2 characters, .001 resolution
(iLead Span) “edge to edge”	in imperial – 0.100inch = 100, 0.050inch pitch = 50	Max 4 characters, min 2 characters, .001 resolution
(ipitch) “pin to pin spacing”	in imperial – 0.100inch = 100, 0.050inch pitch = 50	Max 4 characters, min 2 characters, .001 resolution
(jedec)	Jedec package code	various
(m/f)	Male or female	1 Character
(mtg_qty)	# of mtgholes	Max 2 characters, min 1 character
(Pin_qty)	# of pins	Max 3 characters, min 1 character
(pitch) “pin to pin spacing”	in metric – 1.27mm = 127, .80mm pitch = 80	Max 4 characters, min 2 characters, .01 resolution

CODE	Definition	# of Characters
(ra pin t2h)	Distance from pin tip to cell origin (pin1 on thp, center of pads on smd) in metric – 1.27mm = 127, .80mm pitch = 80	Max 4 characters, min 2 characters, .01 resolution
(rows)	# of rows – S single D dual T triple Q quad	Max 1 characters, min 1 character
(st or rt)	Straight (st) or Right Angle (rt)	2 Characters
(standard)	Industry standard – PCI, ISA, DIMM etc	Up to 31 characters in the name
(HS####)	Head Sink thermal pad dims	Up to 31 characters in the name
(z or blank)	Z = zig zag pad pattern , otherwise leave blank	Max 1 characters, min 0 character

Figure 6.17 Naming Convention Codes

Default Settings

NAME	DESCRIPTION	Value
Assembly Outline Width.	Outline that represents the body outline of the part.	0.1
DFA_BOUND_TOP	Outline that represents the body and pads of the part.	0.0
Land pattern Round off factor	Standard land patterns will be rounded to the nearest.	0.05
Maximum Land pattern Name Length		31 Chrs
Maximum Padstack Name Length		31 Chrs
Minimum Pad to Pad Gap		0.20
Minimum Silkscreen Length		0.35
Minimum Soldermask Width		0.08
Part Number	Height: 0.5mm, Stroke Width: 0.1mm. Placement: Same as Reference Designator (Assy).	
Pin Numbering	All pins, including plated through holes, will have a pin number, unless specified by the customer. No two pins will have the same pin number. Additional pins are assigned the next numerical number if a pin number is not provided. Fiducials well be defaulted as mechanical pins and will not require a pin number.	
Placement Outline	Shape that represents the body and pins of the part.	0
Reference Designator (Assy)	Height: 1mm, Stroke Width: 0.1mm.	
Reference Designator (Silk)	Height: 0.9mm, Stroke Width: 0.13mm. Placement: Outside the body so it is visible when the component is placed.	
Silkscreen Gap	The minimum gap required between the silkscreen and any land pattern.	0.13
Silkscreen Outline Width	Outline that represents the body outline of the part. Does not cover any land pattern.	0.13
Units	The land pattern and pads and padstacks will be drawn in millimeters.	

Figure 6.18 Default Settings

Glossary

The following terms and definitions used herein are to reduce confusion in the terminology across different tools, manufacturers, and other documentation.

Dual row component – A component where the basic land pattern consists of two rows of lands.
Land or Padstack – A single conductive element of a component placed on a printed circuit/wiring board. This can consist of a pad, pastemask, and soldermask.
Heel – The edge of a single land or component termination that is closest to the center of a component.
Heel to heel (H/H) – The distance between two opposing heels or component terminations in a single component.
Land Pattern – The complete physical pattern of a component placed on a printed circuit/wiring board. This can consist of lands, silkscreen outlines, assembly outlines, placement outlines, courtyard outlines, drills, and keepout outlines.
Pad – the conductive part of a land pattern.
Quad component – A component where the basic land pattern consists of two rows and two columns of lands.
Single row component – A component where the basic land pattern consists of a single row of lands.
Termination – a pin, leg, or contact of a component.
Toe – The edge of a single land or component termination that is farthest away from the center of a component.
Toe to toe (T/T) – The distance between two opposing toes or component terminations in a single component.

Generic Components

Many resistors capacitors and inductors are included in the library in generic form, meaning they have no manufacturer part numbers.

The heights of these components are derived from the following sources

Generic chip resistor heights are based on KOA RK73B series

Generic chip capacitor heights are based on TDK “C" series

Generic chip tantalum capacitor heights are based on Panasonic TAJ series

Generic chip inductor heights are based on TDK MLG and VISHAY ISLB series

PART	HEIGHT (mm)	SERIES
RES-01005	0.15	KOA 1F 01005
RES-0201	0.26	KOA 1H 0201
RES-0402	0.4	KOA 1E 0402
RES-0603	0.55	KOA 1J 0603
RES-0805	0.6	KOA 2A 0805
RES-1206	0.7	KOA 2B 1206
RES-1210	0.7	KOA 2E 1210
RES-2010	0.7	KOA 2H 2010
RES-2512	0.7	KOA 3A 2512
CAP-01005	0.2	TDK CC01005 (C0402)
CAP-0201		
CAP-0402	0.5	TDK CC0402 (C1005)
CAP-0603	0.8	TDK CC0603 (C1608)
CAP-0805	1.25	TDK CC0805 (C2012)
CAP-1206	1.6	TDK CC1206 (C3216)
CAP-TANT-3216	1.8	PANASONIC TAJ SERIES
CAP-TANT-3528	2.1	PANASONIC TAJ SERIES
CAP-TANT-6032	2.8	PANASONIC TAJ SERIES
CAP-TANT-7343	4.3	PANASONIC TAJ SERIES
IND-0402	0.55	TDK MLG1005S
IND-0603	0.95	TDK MLG1608
IND-0805	1.45	TDK MLF2012
IND-1008	1.2	TDK MLP2520
IND-1206	1.4	VISHAY ILSB-1206
IND-1210	1.5	VISHAY ILBB-1210
IND-1812	1.75	VISHAY ILBB-1812

Figure 8.1 Generic Components