Learning Maps

Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

Contents

- PCB Design and Analysis
- Custom IC, Analog, and RF Design
- Digital Design and Signoff
- System Design and Analysis
- IC Package Design and Analysis
- Tensilica® Processor IP

cadence®

PCB Design and Analysis Learning Map

Beginner

Advanced

Logic Design

- Allegro® Design Entry HDL Front-to-Back Flow — 3
- Allegro Design Entry HDL Basics — 1
- Allegro System Capture NEW — 1
- Allegro System Architect — 2
- Allegro Design Reuse — 1
- Allegro AMS Simulator — 3
  - Allegro AMS Simulator Advanced Analysis — 1
- Allegro Design Entry Using OrCAD® Capture — 2
- OrCAD CIS — 1
- OrCAD Capture Constraint Manager PCB Flow NEW — 1
- Allegro EDM Design Entry HDL Front-to-Back Flow — 3
- Allegro Team Design Authoring — 1
- Allegro EDM for Engineers and Designers — 1
- Analog Simulation with PSpice® — 3
  - Analog Simulation with PSpice Advanced Analysis — 1

PCB Design

- Allegro PCB Editor Basic Techniques — 3
  - Allegro PCB Editor Intermediate Techniques — 2
  - Allegro PCB Router Basics — 2
  - Allegro PCB Editor Advanced Methodologies — 1
- Allegro High-Speed Constraint Management — 2
- Allegro Update Training NEW — 1
- Advanced Design Verification with the RAVEL Programming Language NEW — 2

SI/PI Analysis

- Essential High-Speed PCB Design for Signal Integrity — 3
- PCB Design at RF – Multi-Gigabit Transmission, EMI Control, and PCB Materials — 2
- Allegro Sigrity™ SI Foundations — 2
- Allegro Sigrity PI — 1
- Sigrity PowerDC™ and OptimizePI™ — 1
- TopXplorer SystemSI for Parallel Bus and Serial Link Analysis — 3
- Model Generation and Analysis using PowerSI, Broadband SPICE and 3D-EM — 3
- Clarity 3D Solver NEW — 1
- Celsius Thermal Solver NEW — 1

Library Development

- Allegro PCB Librarian — 2
- Allegro EDM PCB Librarian NEW — 2
- Allegro EDM for Administrators — 2
- Allegro EDM Administration for OrCAD — 2
- Allegro Design Entry HDL SKILL® Programming Language — 3
- Allegro PCB Editor SKILL Programming Language — 3

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available | Digital Badge Available

IC Package Design and Analysis Learning Map

Beginner

Advanced

IC Package Design

- SiP Layout
- Allegro® Package Designer
- Allegro FPGA System Planner
- Allegro Sigrity Package Assessment and Model Extraction
- OrbitIO™ System Planner
- Advanced Design Verification with the RAVEL Programming Language NEW
- Allegro Package Designer Plus NEW

SI/PI Analysis

- Allegro Sigrity™ SI Foundations
- Allegro Sigrity PI
- Sigrity PowerDC™ and OptimizePI™
- TopXplorer SystemSI for Parallel Bus and Serial Link Analysis
- Model Generation and Analysis using PowerSI, Broadband SPICE, and 3D-EM
- Clarity 3D Solver NEW
- Celsius Thermal Solver NEW

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Custom IC, Analog and RF Design Learning Map

1 of 2 – see next page

Beginner

Advanced

Circuit Design, Simulation, Modeling and RF Design

- Analog Modeling with Verilog-A (3)
  - Mixed-Signal Simulations using Spectre AMS Designer (2)
  - Command-Line Based Mixed-Signal Simulations w/ Xcelium Use Model (1)
  - Behavioral Modeling with Verilog AMS (2)
  - Behavioral Modeling with VHDL-AMS (3)
  - Real Modeling with Verilog-AMS (2)
  - Real Modeling with SystemVerilog NEW (3)
  - SystemVerilog Real Number Modeling (SV-RNM) Based Advanced Verification NEW (5)

- Virtuoso Schematic Editor NEW (L, XL, 2)
- Virtuoso Visualization and Analysis (1)
- Virtuoso® ADE Explorer & Assembler Series NEW
  - **S1** ADE Explorer & Single Test Corner Analysis (0.5)
  - **S2** ADE Assembler & Multi Test Corner Analysis (1)
  - **S3** Sweeping Variables and Simulating Corners (0.5)
  - **S4** Monte Carlo, Real-Time Tuning & Run Plans (0.5)
- Design Checks and Asserts (1)
- Virtuoso® ADE Verifier Series
  - **S1** Setup, Run, & View Verifier Results (1)
  - **S2** Reference Flow and Analog Coverage Using the Setup Library Assistant (1)
- 5G mmWave Handset System Design – **S1** RFIC (Transceiver) Design NEW (1)

- Spectre® Simulator Fundamentals Series
  - **S1** Spectre Basics (1)
  - **S2** Large-Signal (1)
  - **S3** Small-Signal NEW (1)
  - **S4** Spectre MDL (0.5)
- Spectre Accelerated Parallel Simulator (APS) (1)
- Spectre XPS for Mixed-Signal Designs (0.5)
- Virtuoso® Spectre® Pro Series
  - **S1** DC Algorithm NEW (0.5)
  - **S2** AC, XF, STB, Noise (0.5)
  - **S3** Transient Algorithm (0.5)
  - **S4** Fourier Transform (0.5)
  - **S5** Transient Noise (1)
- Spectre® RF Shooting Newton (2)
- Spectre® RF Harmonic Balance (2)

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available | Digital Badge Available

Custom IC, Analog and RF Design Learning Map

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Beginner

Advanced

IC CAD

- SKILL® Language Programming Introduction — NEW — 2
- SKILL Language Programming — 5
- SKILL Development of Parameterized Cells — 2
- SKILL Programming for IC Layout Design — 2
- Advanced SKILL Language Programming — 3

Layout Design and Advanced Nodes

- Virtuoso® Layout Design Basics — L — 1
- Virtuoso Connectivity-Driven Layout Transition — L XL — 2
  - Virtuoso Abstract Generator — GXL — 1
  - Virtuoso Floorplanner — GXL — 1
  - Virtuoso Space-Based Router — GXL — 2
    - Virtuoso Space-Based Router Express — GXL — 0.5

Virtuoso® Layout Pro Series

- T1: Env. and Basic Commands — L — 1
- T2: Create and Edit Commands — L — 1
- T3: Basic Commands — XL — 1
- T4: Advanced Commands — XL — 1 — NEW
- T5: Interactive Routing — XL — 1 — NEW
- T6: Constraint-Driven Flow and Power Routing — XL GXL — 0.5
- T7: Module Generator and Floorplanner — XL GXL — 0.5
- T8: Debugging Layout Issues — L XL — 0.5
- T9: Virtuoso Design Planner — EXL — 2 — NEW

Virtuoso® Advanced-Node – ICADV

- Virtuoso Layout for Adv. Nodes — 2
- T1: Place and Route — 1
- T2: Electromigration — 0.5

Virtuoso® Advanced-Node and Methodology - ICADVM

- Virtuoso Layout for Advanced Nodes and Methodology Platform — NEW — EXL — 0.5

Layout Verification

- Pegasus Verification System — NEW — 2
- Physical Verification System (PVS) — 2
- Physical Verification Language Rules-Writer — 2

Quantus™ Extraction Solution Transistor-Level Series

- T1: Overview and Technology Setup — 0.5
- T2: Parasitic Extraction — 1
- T3: Extracted View Flows and Advanced Features — 0.5
- Transistor Level Power Signoff with Voltus™-Fi — 1.5

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Digital Design and Signoff Learning Map

Beginner

Advanced

Synthesis and Test

- Design For Test Fundamentals
- Genus™ Synthesis Solution with Stylus Common UI
- Low-Power Synthesis Flow with Genus Stylus Common UI (NEW)
- Test Synthesis with Genus Stylus Common UI (NEW)
- Advanced Synthesis with Genus Stylus Common UI
- Fundamentals of IEEE 1801 Low-Power Specification Format
- Modus DFT Software Solution
- Joules™ Power Calculator

Implementation

- Virtuoso® Digital Implementation
- Innovus™ Implementation System (Block)
- Innovus Implementation System (Hierarchical)
- Low-Power Flow with Innovus Implementation System
- Innovus Clock Concurrent Optimization Technology for Clock Tree Synthesis

Silicon Signoff

- Basic Static Timing Analysis
- Tempus™ Signoff Timing Analysis and Closure
- Voltus™ Power-Grid Analysis and Signoff

Equivalence Checking

- Conformal® Equivalence Checking
- Conformal Low-Power Verification
- Conformal ECO

Cadence® RTL-to-GDSII Flow

NEW New Course | # Number of days for instructor-led course | Online Course Available | Digital Badge Available

System Design and Verification Learning Map

Beginner

Advanced

Simulation, Coverage and Debug

- Xcelium™ Simulator NEW — 2
- Cadence® RTL-To-GDSII Flow — 2
- VIP Basic Building Blocks and Usage NEW — 2
- Low-Power Simulation with CPF — 2
- Low-Power Simulation with IEEE1801 UPF — 2
- Foundations of Metric-Driven Verification — 1
- Xcelium Integrated Coverage — 2
- Metric-Driven Verification Using vManager™ — 3
- vManager Tool Usage in Batch Mode — 0.5
- Perspec™ System Verifier - Basic NEW — 5
- Incisive Functional Safety Simulator — 1
- Specman® Fundamentals for Block-Level Environment Developers — 5
- Specman Advanced Verification — 4

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available | Digital Badge Available

System Design and Verification Learning Map

Beginner

Advanced

Design and Verification Languages

- Verilog Language and Application — 4
- Master VHDL For Verilog Engineers — 3
- Real Modeling with Verilog AMS — 2
- Real Modeling with SystemVerilog — 3
- SystemVerilog Real Number Modeling (SV-RNM) Based Advanced Verification — NEW — 5
- Perl for EDA Engineering — 3
- Tcl Scripting for EDA — 3
- SystemVerilog for Design and Verification — 5
  - UVM
    - Essential SystemVerilog for UVM (optional) — 1
    - SystemVerilog Accelerated Verification Using UVM — 4
    - SystemVerilog Advanced Register Verification Using UVM — NEW — 2
- VHDL Language and Application — 5
- Verilog for VHDL Users — 2
- SystemVerilog Assertions — 2
- JasperGold® Formal Fundamentals — 2
- JasperGold® Formal Expert — NEW — 2
- SVA, Formal & JasperGold® Fundamentals for Designers — NEW
- C++ Language Fundamentals for Design and Verification — 2
- SystemC® Language Fundamentals — 3
- SystemC Synthesis with Stratus HLS — 3
- SystemC Transaction-Level Modeling TLM2.0 — 2

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available | Digital Badge Available

Tensilica Processor IP Learning Map

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Tensilica Xtensa LX

- Tensilica® Xtensa® LX Processor Fundamentals — NEW
- Tensilica Xtensa LX Processor Interfaces
- Tensilica Xtensa LX Hardware Verification and EDA
- Tensilica Instruction Extension Language and Design — 1
- Tensilica System Modeling using XTSC — NEW

ConnX DSP

- Tensilica ConnX BBE16EP Baseband Engine — 2
- Tensilica ConnX BBE32EP Baseband Engine — 2
- Tensilica ConnX BBE64EP Baseband Engine — 2

Fusion DSP

- Tensilica Fusion F1 DSP
- Tensilica Fusion G3 DSP — 2
- Tensilica Fusion G6 DSP — 2

HiFi Audio DSP

- Tensilica Audio Codec API — 0.5
- Tensilica HiFi 2/EP/Mini Audio Engine ISA
- Tensilica HiFi 3 Audio Engine ISA
- Tensilica HiFi 4 DSP — NEW
- Tensilica HiFi 5 DSP — NEW

Vision DSP

- Tensilica Vision P5 DSP — 2
- Tensilica Vision P6 DSP — 2
- Tensilica DNA 100 Architecture and Programming — NEW

NEW New Course # Number of days for instructor-led course Online Course Available

Tensilica Processor IP Learning Map

Tensilica Xtensa NX

- Tensilica® Xtensa® NX Processor Fundamentals — NEW
- Tensilica Xtensa NX Processor Interfaces
- Tensilica Xtensa NX Hardware Verification and EDA
- Tensilica Instruction Extension Language and Design — 1
- Tensilica System Modeling using XTSC — NEW

ConnX DSP

- Tensilica ConnX B10 DSP — NEW — 2
- Tensilica ConnX B20 DSP — NEW — 2

Vision DSP

- Tensilica Vision Q7 DSP — NEW

NEW New Course | # Number of days for instructor-led course | Online Course Available