



Learning Maps

Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at <https://www.cadence.com/training>.

Contents

- PCB Design and Analysis
- Custom IC, Analog, and RF Design
- Digital Design and Signoff
- System Design and Analysis
- IC Package Design and Analysis
- Tensilica® Processor IP

PCB Design and Analysis Learning Map

Beginner

Advanced




Beginner



Advanced

Logic Design



Allegro® Design Entry HDL Front-to-Back Flow   3 



Allegro Design Entry HDL Basics  1 

Allegro System Capture   1 

Allegro System Architect  2 



Allegro Design Reuse  1 

Allegro AMS Simulator  3 

Allegro AMS Simulator Advanced Analysis  1 

Allegro Design Entry Using OrCAD® Capture  2 



OrCAD CIS  1



OrCAD Capture Constraint Manager PCB Flow   1

Allegro EDM Design Entry HDL Front-to-Back Flow  3 




Allegro Team Design Authoring  1 

Allegro EDM for Engineers and Designers  1 



Analog Simulation with PSpice®  3 

Analog Simulation with PSpice Advanced Analysis  1 




PCB Design




Allegro PCB Editor Basic Techniques   3 




Allegro PCB Editor Intermediate Techniques   2 

Allegro PCB Router Basics  2 


Allegro PCB Editor Advanced Methodologies  1 


Allegro High-Speed Constraint Management   2 

Allegro Update Training   1 



Advanced Design Verification with the RAVEL Programming Language   2 



SI/PI Analysis



Essential High-Speed PCB Design for Signal Integrity  3

PCB Design at RF – Multi-Gigabit Transmission, EMI Control, and PCB Materials  2




Allegro Sigrity™ SI Foundations  2 




Allegro Sigrity PI  1 

Sigrity PowerDC™ and OptimizePI™  1 



TopXplorer SystemSI for Parallel Bus and Serial Link Analysis  3 




Model Generation and Analysis using PowerSI, Broadband SPICE and 3D-EM  3 



Clarity 3D Solver   1 



Celsius Thermal Solver   1 



Library Development




Allegro PCB Librarian   2 

Allegro EDM PCB Librarian   2 

Allegro EDM for Administrators  2 

Allegro EDM Administration for OrCAD  2 

Allegro Design Entry HDL SKILL® Programming Language  3 

Allegro PCB Editor SKILL Programming Language   3 

 New Course

 Number of days for instructor-led course

   Tiers of Cadence products used in course

 Online Course Available

 Digital Badge Available

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IC Package Design and Analysis Learning Map

Beginner



Advanced

IC Package Design

SiP Layout



Allegro® Package Designer



Allegro FPGA System Planner



Allegro Sigrity Package Assessment and Model Extraction



OrbitIO™ System Planner



Advanced Design Verification with the RAVEL Programming Language **NEW**



Allegro Package Designer Plus **NEW**



SI/PI Analysis

Allegro Sigrity™ SI Foundations



Allegro Sigrity PI



Sigrity PowerDC™ and OptimizePI™



TopXplorer SystemSI for Parallel Bus and Serial Link Analysis



Model Generation and Analysis using PowerSI, Broadband SPICE, and 3D-EM



Clarity 3D Solver **NEW**



Celsius Thermal Solver **NEW**



Beginner



Advanced

NEW

New Course



Number of days for instructor-led course



Tiers of Cadence products used in course

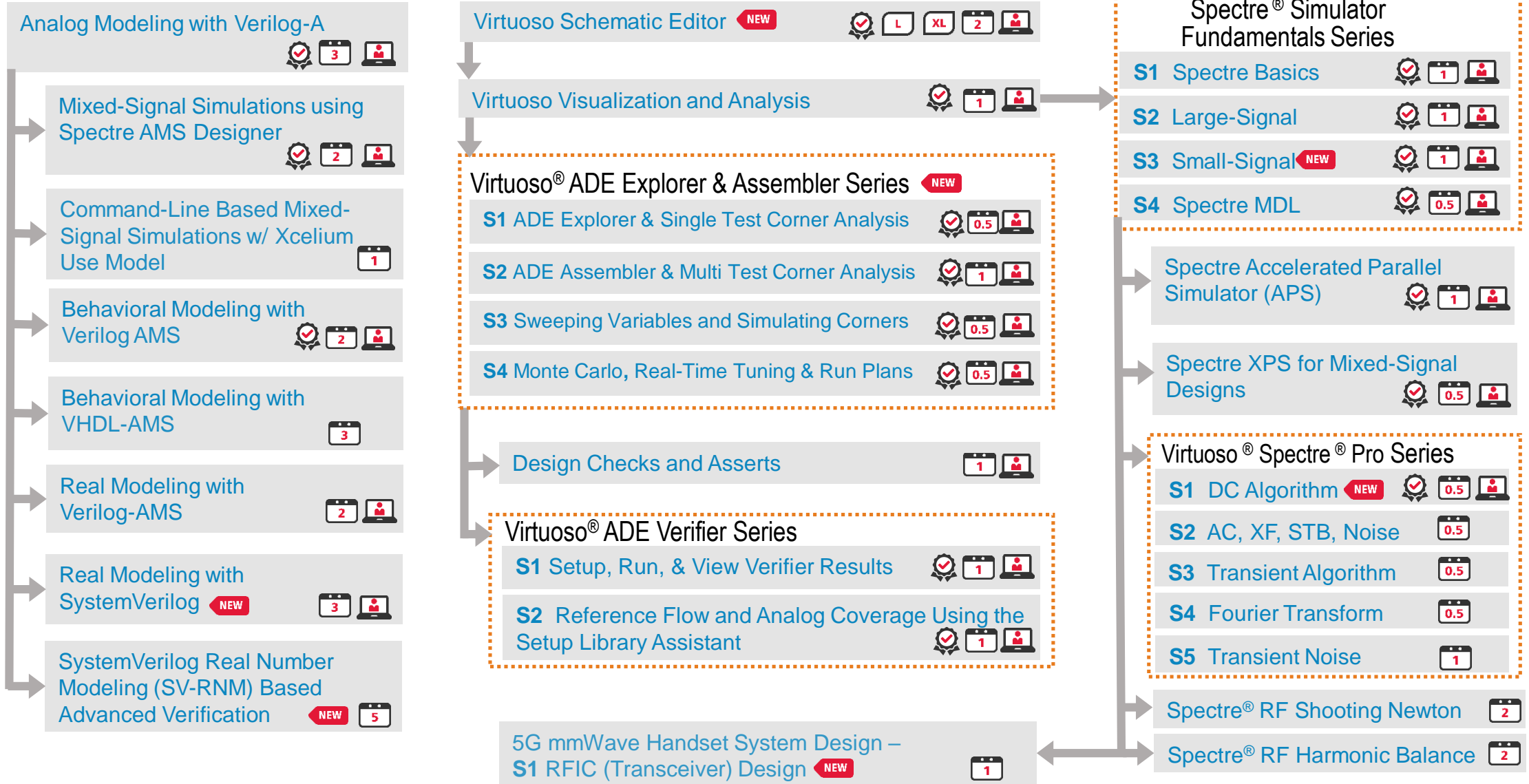


Online Course Available

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Beginner
↓
Advanced

Circuit Design, Simulation, Modeling and RF Design



Beginner
↓
Advanced

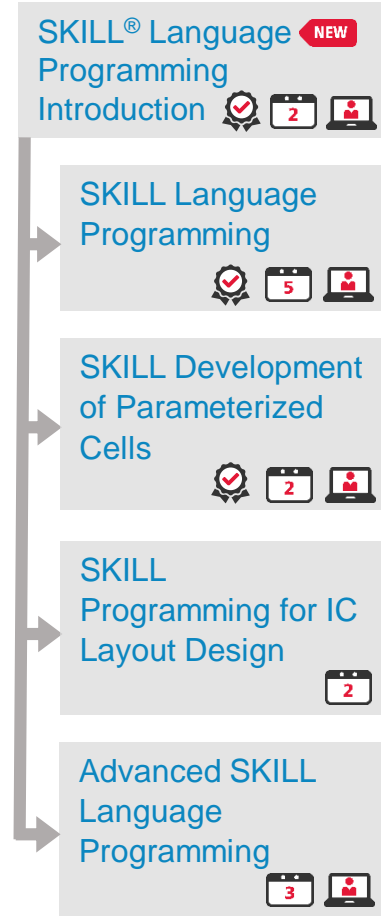
Custom IC, Analog and RF Design Learning Map

2 of 2 – see prior page

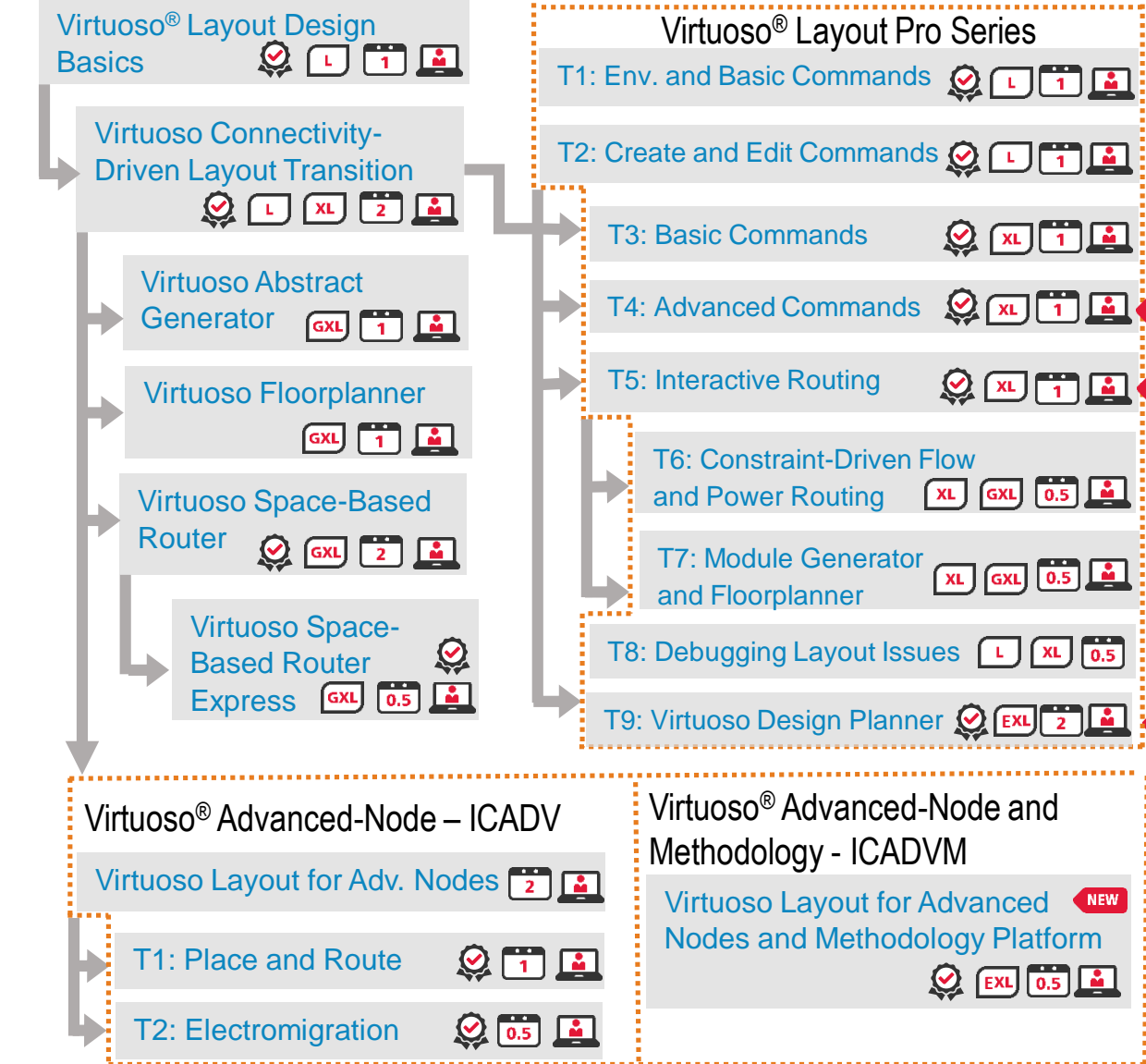
Beginner

Advanced

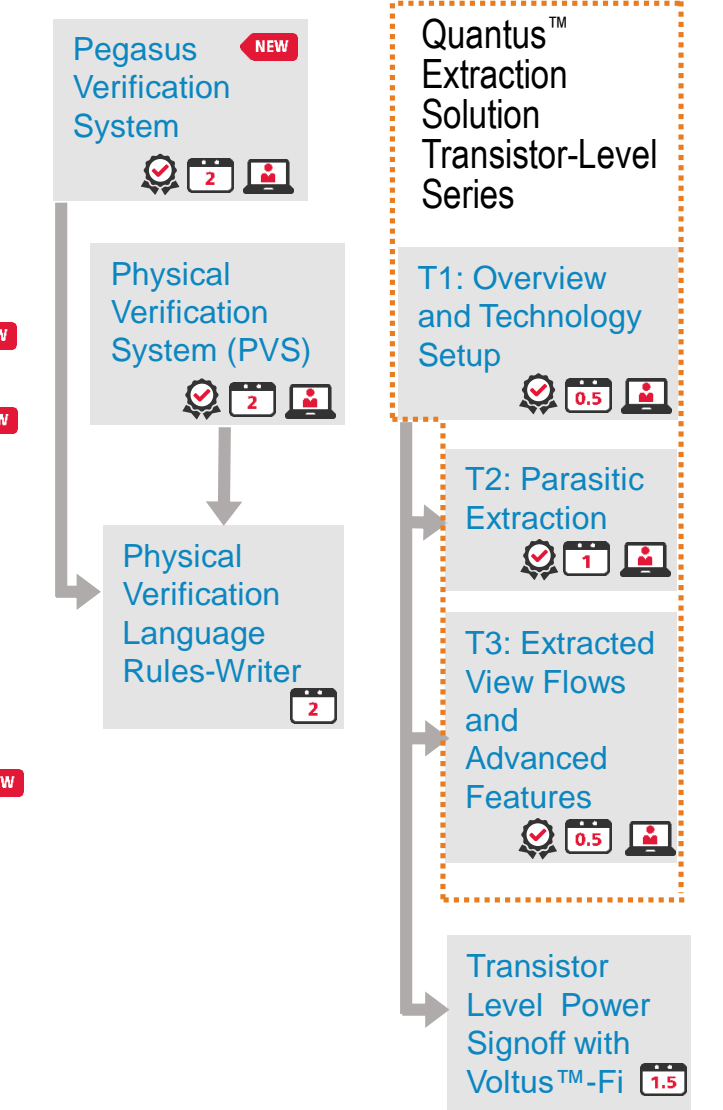
IC CAD



Layout Design and Advanced Nodes



Layout Verification



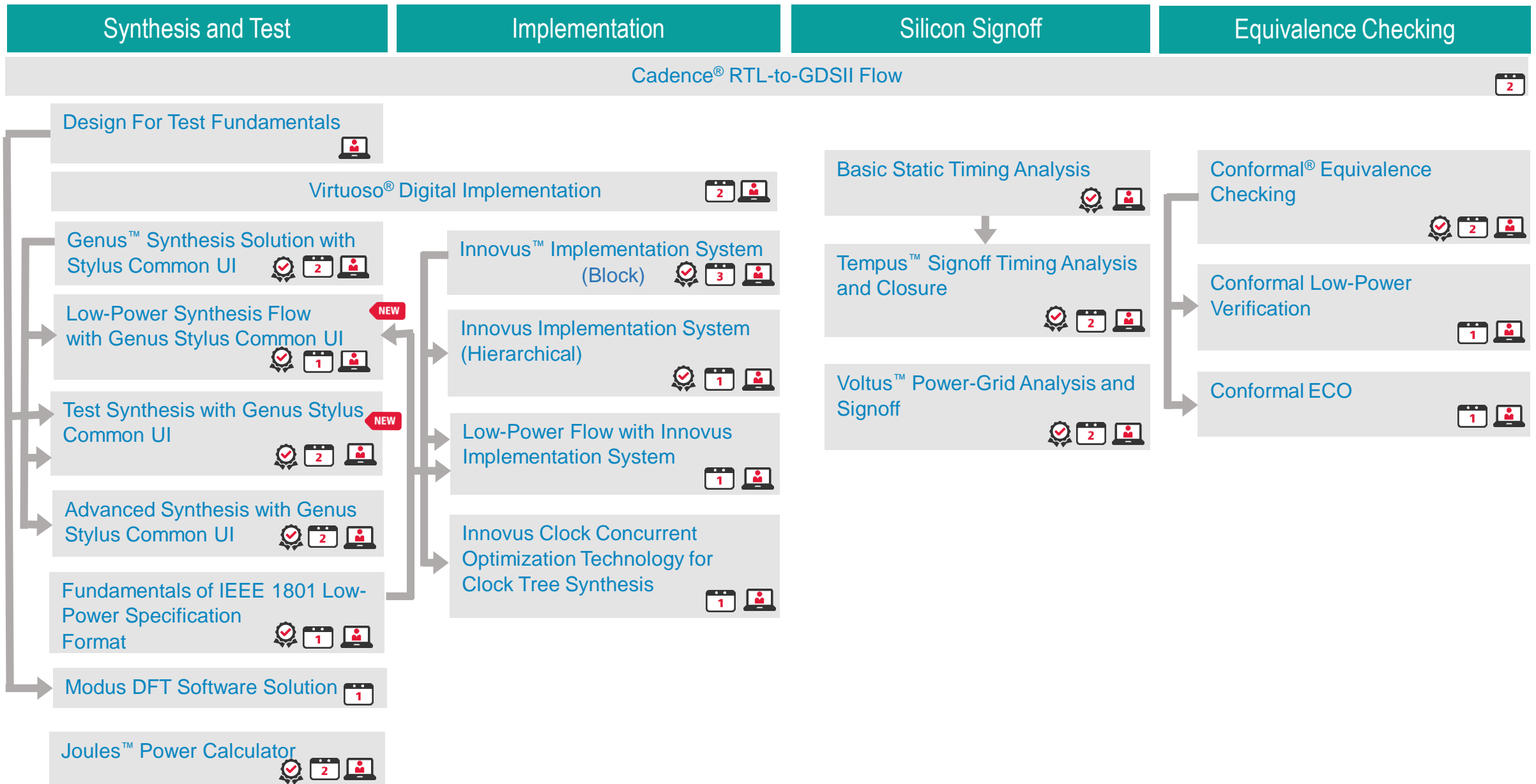
Beginner

Advanced

Digital Design and Signoff Learning Map

Beginner

Advanced



Beginner

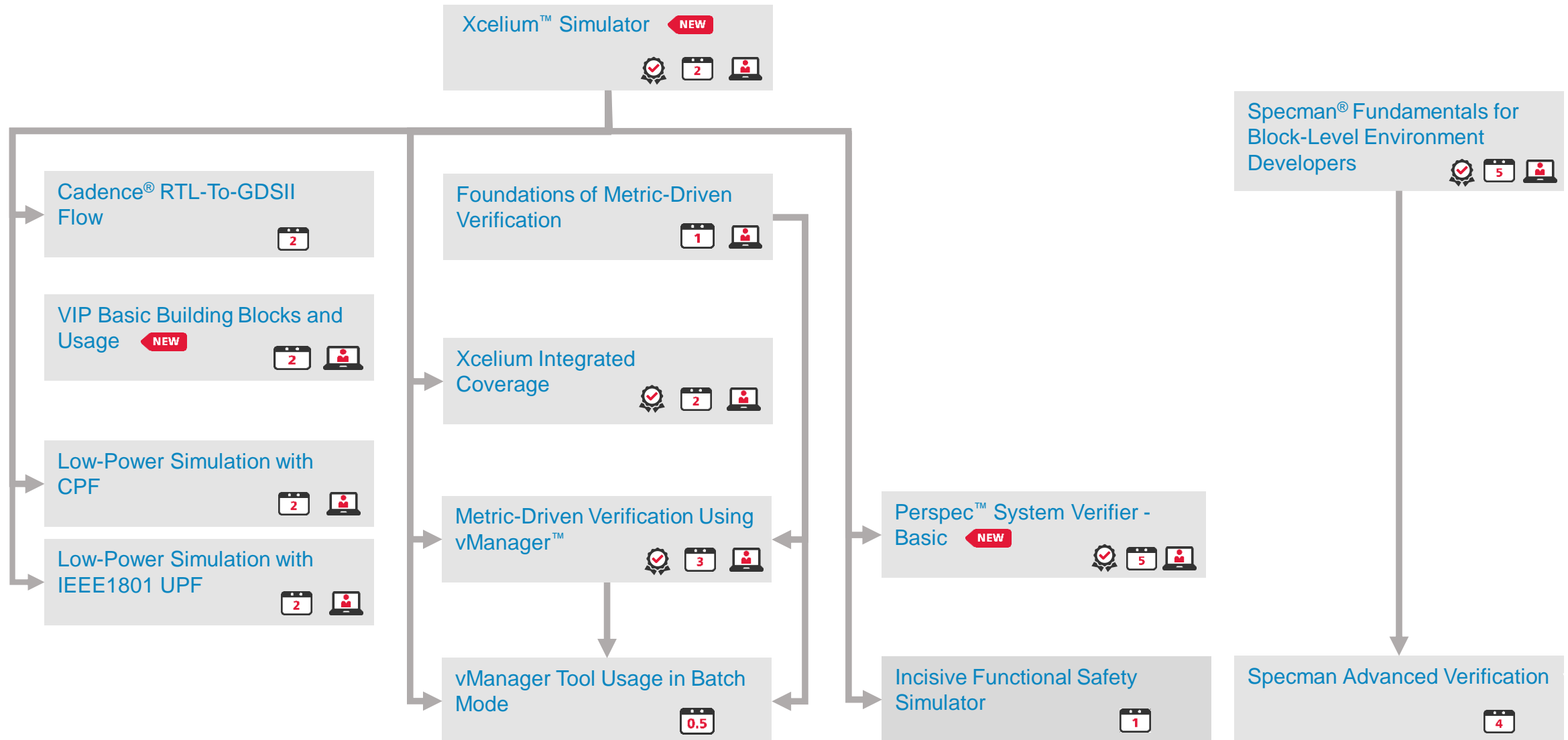
Advanced

System Design and Verification Learning Map

Beginner

Advanced

Simulation, Coverage and Debug



Beginner

Advanced



New Course



Number of days for instructor-led course



Tiers of Cadence products used in course



Online Course Available

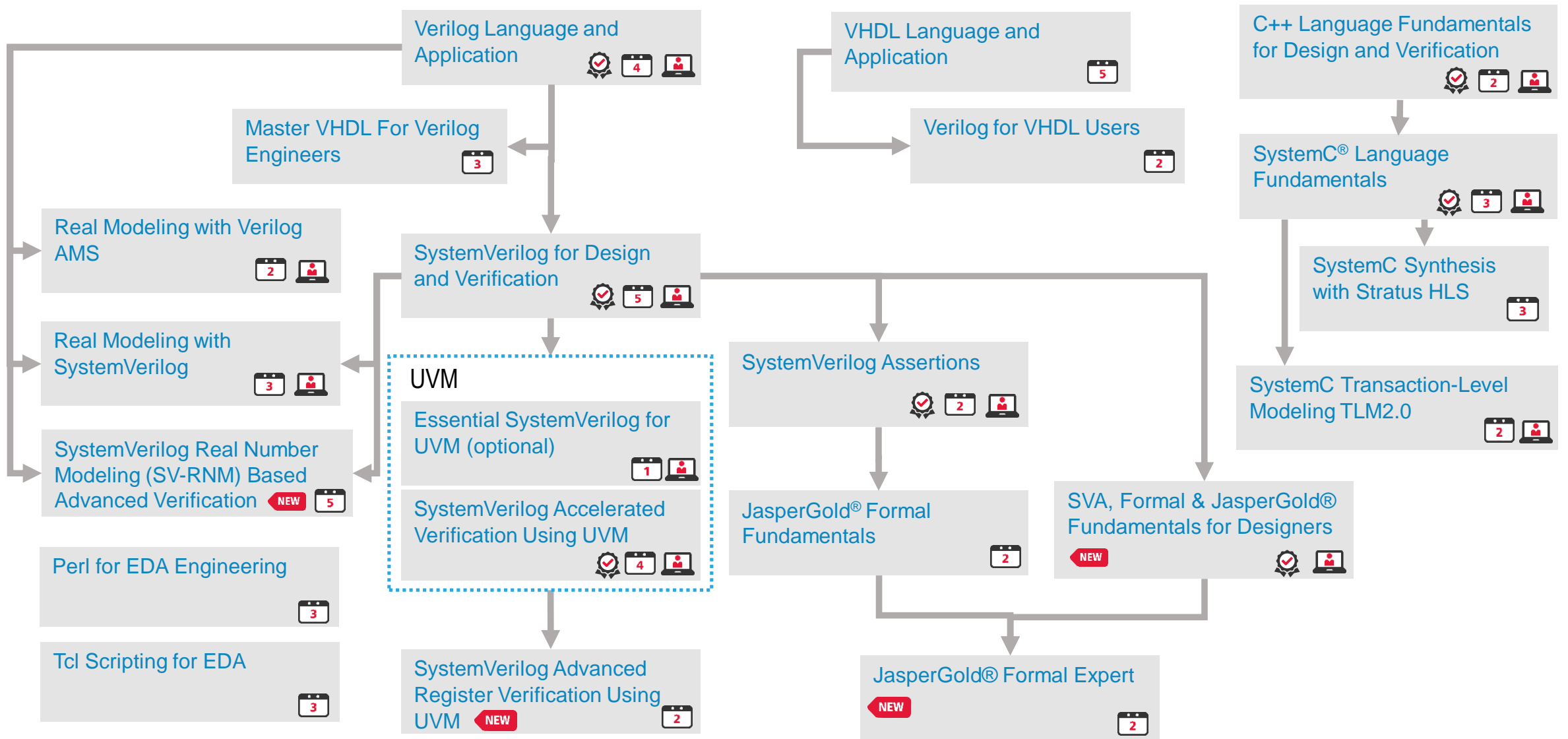


Digital Badge Available

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System Design and Verification Learning Map


Design and Verification Languages



NEW

NEW New Course



 Number of days for instructor-led course



L **XL** **GXL** Tiers of Cadence products used in course

 Online Course Available Digital Badge Available

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Tensilica Processor IP Learning Map

1 of 2 – see next page



Tensilica Xtensa LX

[Tensilica® Xtensa® LX Processor Fundamentals](#)

NEW



[Tensilica Xtensa LX Processor Interfaces](#)



[Tensilica Xtensa LX Hardware Verification and EDA](#)



[Tensilica Instruction Extension Language and Design](#)

1



[Tensilica System Modeling using XTSC](#)

NEW



ConnX DSP

[Tensilica ConnX BBE16EP Baseband Engine](#)

2

[Tensilica ConnX BBE32EP Baseband Engine](#)

2



[Tensilica ConnX BBE64EP Baseband Engine](#)

2

Fusion DSP

[Tensilica Fusion F1 DSP](#)



[Tensilica Fusion G3 DSP](#)

2



[Tensilica Fusion G6 DSP](#)

2

HiFi Audio DSP

[Tensilica Audio Codec API](#)

0.5

[Tensilica HiFi 2/EP/Mini Audio Engine ISA](#)



[Tensilica HiFi 3 Audio Engine ISA](#)



[Tensilica HiFi 4 DSP](#)

NEW



[Tensilica HiFi 5 DSP](#)

NEW



Vision DSP

[Tensilica Vision P5 DSP](#)

2



[Tensilica Vision P6 DSP](#)

2



[Tensilica DNA 100 Architecture and Programming](#)

NEW



NEW

New Course



Number of days for instructor-led course



Online Course Available

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Tensilica Xtensa NX

ConnX DSP

Vision DSP

[Tensilica® Xtensa® NX Processor Fundamentals](#)

NEW



[Tensilica Xtensa NX Processor Interfaces](#)



[Tensilica Xtensa NX Hardware Verification and EDA](#)



[Tensilica Instruction Extension Language and Design](#)

1



[Tensilica System Modeling using XTSC](#)

NEW



[Tensilica ConnX B10 DSP](#)

NEW

2



[Tensilica ConnX B20 DSP](#)

NEW

2

[Tensilica Vision Q7 DSP](#)

NEW





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