EE457: Digital IC Design

Project #2 FALL SEMESTER 2023

Report Cover Sheet*

Due 10/28/2023 by 8PM (-2 pts per hour up to 5 points/day)

PROJECT TITLE: CMOS 8-to-1 MUX

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Topics (Do not change orders of section)	GRADES
Section1: Executive Summary (1/2 page)	Required
Section 2: Introduction and Background	/5
Section 3: Electric Circuit Schematics (TG and Conventional CMOS designs)	/10
Section 4: LTSPICE Simulation for Schematic (TG and Conventional CMOS designs)	/10
Section 5: IRSIM for Schematic (TG and Conventional CMOS designs)	/10
Section 6: Electric Layouts (landscape mode and must legible to see gates) (TG and Conventional CMOS designs)	/25
Section 7: LTSPICE Simulation for Layouts (TG and Conventional CMOS designs)	/10
Section 8: IRSIM for Layout (TG and Conventional CMOS designs)	/10
Section 9: Compare LTSPICE Measurements for Schematic and Layout (must provide comparisons between the two in table format) Provide delays, rise and fall times.	/10
Section 10: Measurements of chip area, number of transistors for the layout (provide a table to compare) and write summary for TG and CMOS designs.	/10
Section 11: Conclusions and References	Required
Late Penalty	
TOTAL	**/100**

*Penalty rules: A) -5pts per day for late submission. After five days, a score of zero will be given, but you are still required to complete the report. B) -2pts for any violations and delays submitted after 8PM.

Contents

1 Executive Summary

The goal of this project was to build an 8-to-1 multiplexer twice, once using transmission gates and once using ordinary CMOS logic. A multiplexer is a combinational logic circuit that allows for one of many inputs to be passed through to a single output. In this case there are 8 inputs, D0 to D7, and the state of output Y reflects the state of the input selected with the select lines S0, S1, and S2. Multiplexers have a variety of uses in digital electronics, most notably in the design of CPUs.

In this project, the multiplexer is realized using the software Electric, which allows us to design a schematic, layout, and icon for the multiplexer. We are also able to export the design to LTSpice in order to run in-depth simulations as well as simulate the designs with the built-in IRSIM.

I designed the transmission gate multiplexer and the CMOS multiplexer with two different philosophies. For the transmission gate design, I used the method that we learned about in class, where each input has its own set of tranmission gates that connect to a single node for the output. For the CMOS design, I chose to create a 2-to-1 multiplexer and then chain them together to build the 8-to-1 multiplexer. Both designs were an interesting challenge.

The simulation component of the project involved generating input signals and then confirming that the designs generates the expected output. In addition, various measurements can be taken within LTSpice with the `.meas` command. These measurements include propagation delay, rise and fall times, and average current draw.

2 Introduction and Background

The multiplexer is a combinational logic circuit that is crucial to many digital designs. Multiplexers allow us to choose which input out of a number of inputs reaches the output using select lines. They can be designed to take any number of inputs, but typically a power of two. The simplest multiplexer design is a 2-to-1 multiplexer: there are two inputs, D0 and D1, and a single output, Y, and the select line, S, determines which of the inputs reach the output. For instance, when a logic 0 is applied to S, whatever digital signal is applied to D0 is output on Y, and when a logic 1 is applied to S, the signal applied to D1 is output on Y. When one input is selected, all other inputs are ignored.

This logic extends to multiplexers with more inputs. A 4-bit multiplexer has four inputs and one output, and two select lines (S1 and S0) are used to select which of the four inputs is output. 00 selects D0, 01 selects D1, 10 selects D2, and 11 selects D3. Multiplexers can be designed with 8 inputs, 16 inputs, 32 inputs, etc., however in the scope of this project we are building an 8-bit multiplexer which has eight inputs and uses three select lines (S2, S1, S0) to determine which input reaches the output. An interesting side note is that multiplexers can pass an analog signal or a digital signal based on how they are designed; the CMOS design can only pass a digital signal, but the transmission gate design can pass an analog signal as well due to the transmission gates acting as closed or open switches. However, passing analog signals is outside of the scope of this project.

In order to create the design for our 8-to-1 multiplexer, we first need to create a function and a truth table to get a better understanding of the logic that powers the multiplexer. Since our CMOS design is based on a 2-to-1 multiplexer, we will start there. The function for the 2-to-1 multiplexer is as follows:

$$Y = \overline{S} \cdot D_0 + S \cdot D_1$$

The working principle is that when $S = 0$ the output is $Y = D_0$ and when $S = 1$ the output is $Y = D_1$. The truth table for this function is provided below in Table 1.

S	**Y**
0	D_0
1	D_1

Table 1: Truth Table for the 2-to-1 multiplexer.

This working principle can be applied to the 8-to-1 multiplexer as well. The function for the 8-to-1 multiplexer is as follows:

$$Y = \bar{S_2}\cdot\bar{S_1}\cdot\bar{S_0}\cdot D_0 + \bar{S_2}\cdot\bar{S_1}\cdot S_0\cdot D_1 + \bar{S_2}\cdot S_1\cdot\bar{S_0}\cdot D_2 + \bar{S_2}\cdot S_1\cdot S_0\cdot D_3 + S_2\cdot\bar{S_1}\cdot\bar{S_0}\cdot D_4 + S_2\cdot\bar{S_1}\cdot S_0\cdot D_5 + S_2\cdot S_1\cdot\bar{S_0}\cdot D_6 + S_2\cdot S_1\cdot S_0\cdot D_7$$

The truth table for the 8-to-1 multiplexer is shown below in Table 2.

$\mathbf{S_2}$	$\mathbf{S_1}$	$\mathbf{S_0}$	**Y**
0	0	0	D_0
0	0	1	D_1
0	1	0	D_2
0	1	1	D_3
1	0	0	D_4
1	0	1	D_5
1	1	0	D_6
1	1	1	D_7

Table 2: Truth Table for the 8-to-1 multiplexer.

The symbol for the 8-to-1 multiplexer, designed in Electric to represent the schematic, is shown in Figure 1.

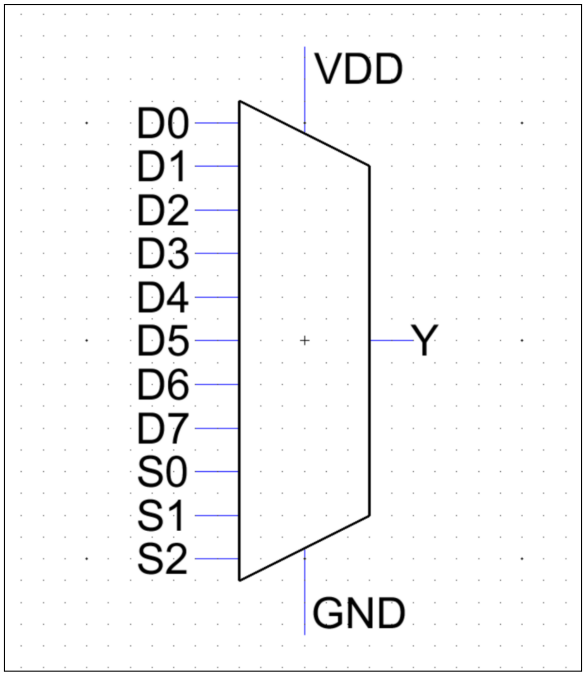

Figure 1: The symbol for the 8-to-1 multiplexer designed in Electric.

As mentioned before, the transmission gate design was made with 8 separate sets of three transmission gates (for S2, S1, and S0). However, the CMOS design was built by chaining together seven 2-to-1 multiplexers. The configuration of these 2-to-1 multiplexers in order to make the 8-to-1 multiplexer is shown in Figure 2.

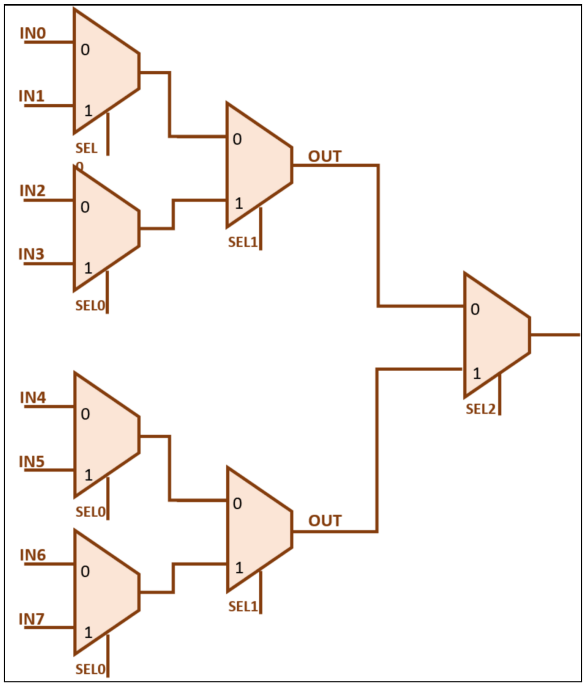

Figure 2: The configuration of seven 2-to-1 multiplexers to create a single 8-to-1 multiplexer.

In order to implement this, we first need to create the 2-to-1 multiplexer. I started with the function $Y = \overline{S} \cdot D_0 + S \cdot D_1$ and implemented it with CMOS logic. Since CMOS logic outputs an inverted signal, we can do one of two things: either invert the function and then implement that, or add an inverter at the end. I chose to add an inverter at the end, since inverting the whole function would involve inverting both D0 and D1 in addition to S. Adding an inverter at the end means we only need two inverters instead of three. The sketch I drew of the schematic is shown in Figure **??**.

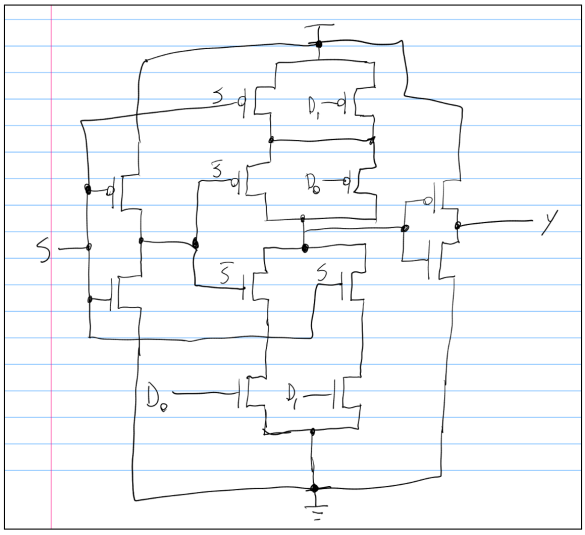

Figure 3: A sketch of the schematic for a single 2-to-1 multiplexer.

The next step was to determine an Euler's Path from the sketch. The Euler's Paths that I determined are shown in Figure 4.

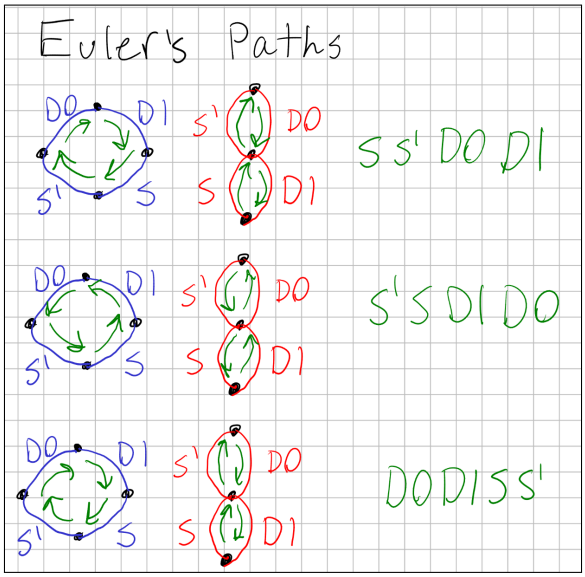

Figure 4: A few Euler's Paths for the 2-to-1 multiplexer.

I decided to use the path $\overline{S}, S, D_1, D_0$ since it seemed to be the most space efficient to me. The stick diagram I sketched based on the Euler's Path chosen is shown in Figure 5.

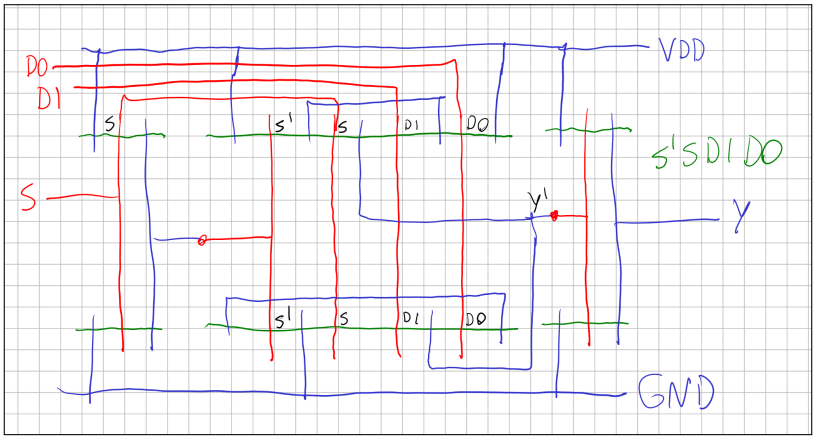

Figure 5: The stick diagram for the 2-to-1 multiplexer.

We now have all of the information we need to begin the design of both the transmission gate and CMOS multiplexers.

3 Electric Circuit Schematics

This section details the design of the schematics for the transmission gate and CMOS designs of the multiplexer.

3.1 Transmission Gate Schematic

The schematic for the transmission gate design of the 8-to-1 multiplexer is shown in Figure 6. The design works by giving each input (D0 through D7) its own set of three transmission gates. Each transmission gate corresponds to one of the select pins, S2, S1, or S0. As shown in table 2, each input corresponds to a specific combination of inputs to the select line. When that combination of the inputs is applied to the select line, the corresponding D input (and only that input) is connected to the output. Since there are eight inputs, there are eight sets of three transmission gates. A closer look at the sets of transmission gates can be seen in Figure 7. Since each transmission gate requires an inverted signal as well as a non-inverted signal to operate, each select pin has its own inverter, which can be seen more clearly in Figure 8.

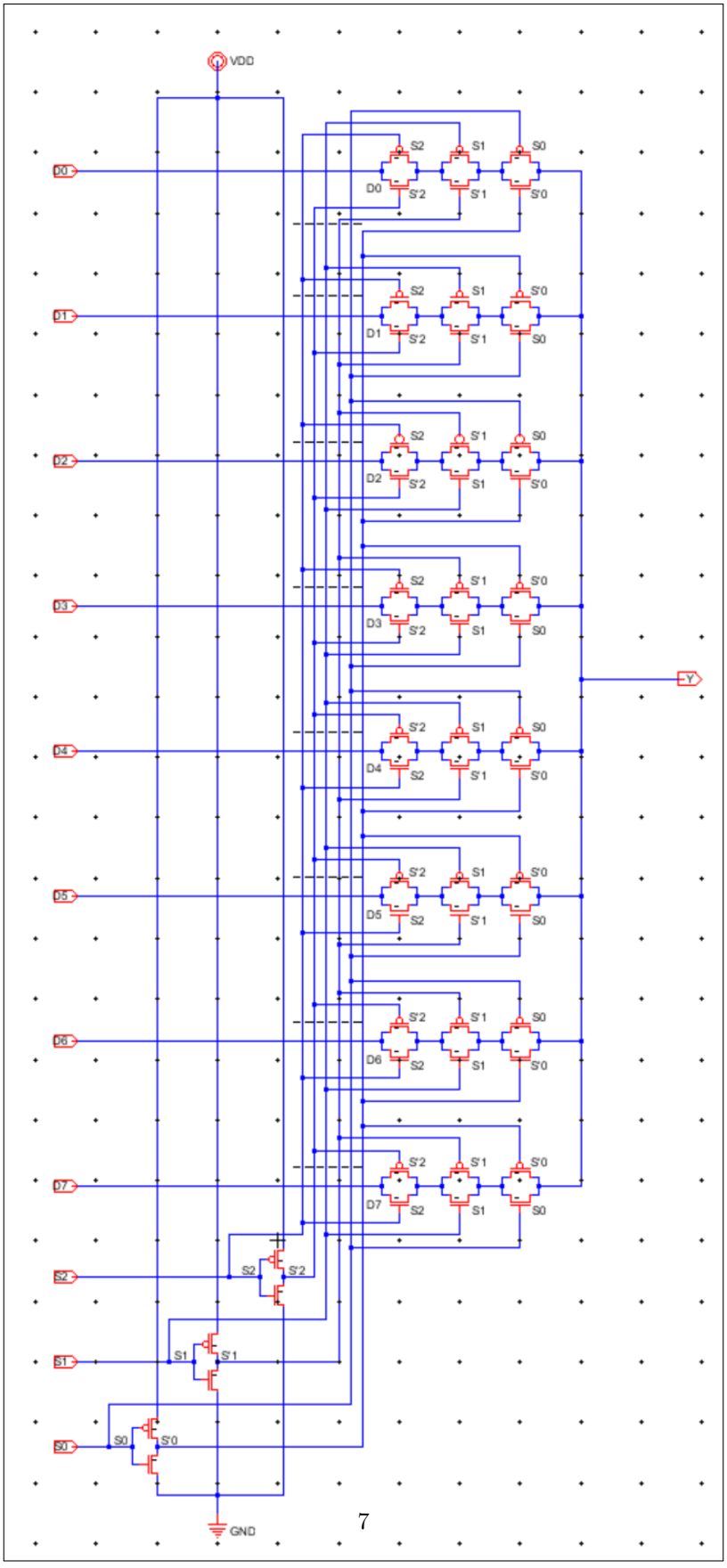

Figure 6: The schematic in Electric for the transmission gate design.

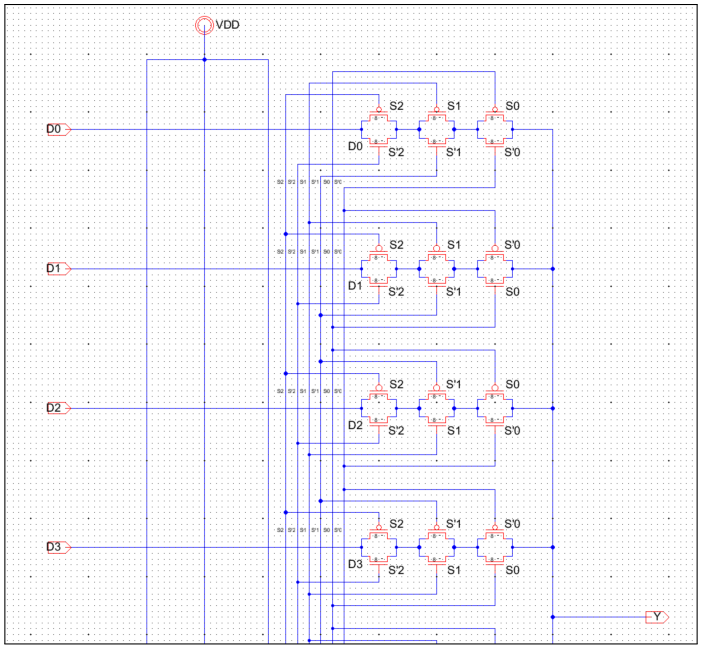

Figure 7: A close up of the schematic showing the sets of transmission gates.

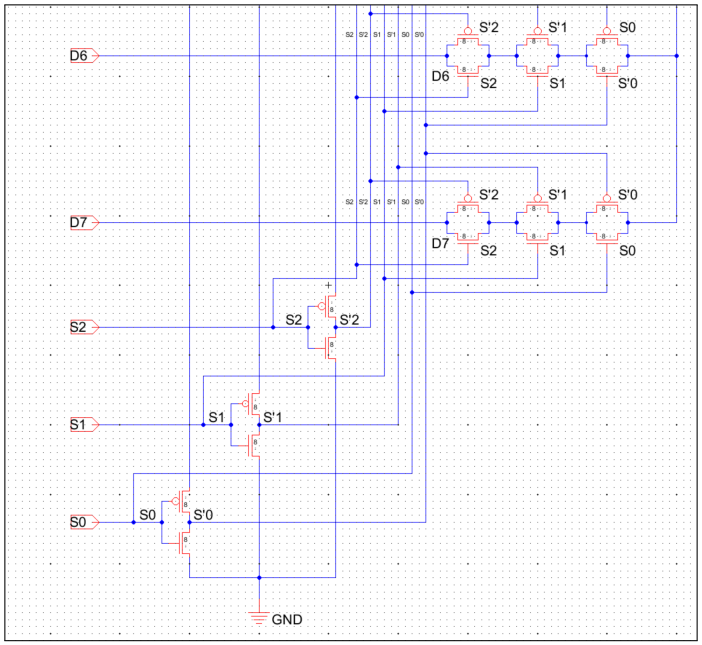

Figure 8: A close up of the schematic showing the inverters which invert the select pins.

3.2 CMOS Schematic

The schematic for the CMOS design of the 8-to-1 multiplexer is simply the 2-to-1 multiplexer schematic sketched in Figure 3 repeated seven times in the configuration shown in Figure 2. However,

there is one change. I realized that having an inverter on the output of each of the 2-to-1 multiplexer was redundant. Only the last stage needs an inverter. This is because while the first stage inverts the output (due to CMOS logic outputting an inverted signal), the second stage will invert it again, cancelling out the first inversion. This saves 12 transistors in the final design. The full schematic is shown in Figure 9.

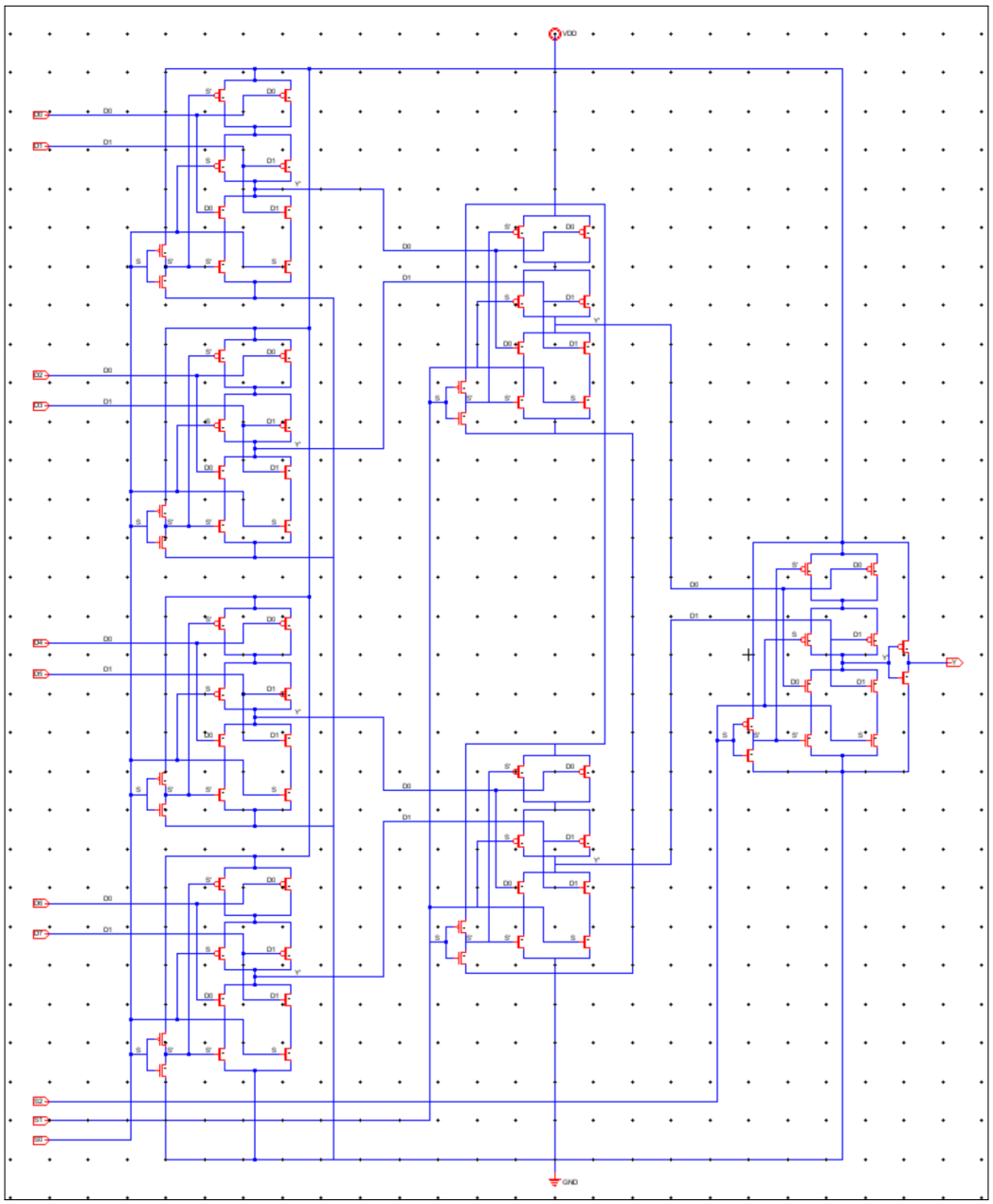

Figure 9: The schematic in Electric for the CMOS design.

Parameter	TG Schematic	TG Layout	CMOS Schematic	CMOS Layout
Rise Time	1.47ns	4.02ns	80.8ps	159ps
Fall Time	7.27ns	1.29ns	39.2ps	119ps
t_{pHL}	273ps	667ps	477ps	793ps
t_{pLH}	239ps	714ps	357ps	763ps
t_p	256ps	690ps	417ps	778ps
Power Draw	8.17nW	2.19nW	473nW	851nW
Chip Dimensions (λ)	N/A	87λ x 429.5λ	N/A	362λ x 120λ
Chip Dimensions (μm)	N/A	15.2μm x 75.2μm	N/A	63.4μm x 21μm
Chip Area(λ^2)	N/A	$37.4*10^3\lambda^2$	N/A	$43.4*10^3\lambda^2$
Chip Area (μm^2)	N/A	$1.14*10^3\mu m^2$	N/A	$1.33*10^3\mu m^2$
Transistor Count	54	54	72	72

Table 3: The measurements results for the XOR gate schematic and layout in LTSpice.

4 Conclusion

In this project, I designed the schematic for an XOR gate using CMOS logic, turned that schematic into a layout, simulated both in LTSpice and IRSIM, and then took measurements on both in LTSpice. I learned a lot in the process about digital IC design, Electric, LTSpice, and the various parameters that make a design good or bad. I enjoyed the process of turning a simple logic gate into a schematic and then into a completed layout far more than I expected, and it was interesting to be able to analyze the final designs with LTSpice and IRSIM.

5 References

[1] EE 457 Lecture 1, 2, and 3
[2] https://cmosedu.com/videos/electric/tutorial3/electric_tutorial_3.htm
[3] https://cmosedu.com/videos/electric/tutorial4/electric_tutorial_4.htm
[4] https://en.wikipedia.org/wiki/XOR_gate