

EE 457: Digital Integrated Circuits

Project #1 Report Cover Sheet

Due: 9/30/2023 by 6PM

PROJECT TITLE: 2-Input CMOS Exclusive OR Gate

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Your report should follow the following items in sequence. <i>Do not change the sequence.</i>	GRADE
Section 1: Executive Summary	/5
Section 2: Background and Approach (Include a truth table)	/5
Section 3: Electric Schematic	/15
Section 4: LTSPICE for Electric schematic	/10
Section 5: IRSIM for Electric schematic	/10
Section 6: Electric Layout	/25
Section 7: LTSPICE for Electric layout (compare with schematic)	/15
Section 8: IRSIM for Electric layout	/10
Section 9: Conclusions and References	/5
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1 Executive Summary

The goal of this project is to design an XOR gate CMOS integrated circuit using the design software Electric. The process of designing the chip involves starting with the boolean logic that makes up an XOR gate, turning that logic into a functioning schematic using CMOS logic, and then turning that schematic into a finished layout. Then, both the schematic and the layout are simulated in both LTSpice and IRSIM to confirm that they function properly, and finally measurements can be taken in LTSpice to further validate the design. Ultimately, this project is an introduction to the process of turning requirements into a finished design and then validating the design using the tools we have learned from creating the inverter.

2 Background

Designing an IC that performs the function of an XOR gate begins with an understanding of what an XOR gate does. The operation, denoted as $F = A \oplus B$ is a boolean logic function that takes inputs A and B and outputs a 0 if they are the same and 1 if they are dissimilar. This behavior can be seen in Table 1. The symbol for the XOR gate is shown in Figure 1. We can break down this logic into the following boolean expressions: $F = A \oplus B = A\bar{B} + \bar{A}B = (A + B)(\bar{A} + \bar{B})$

Input A	Input B	Output F
0	0	0
0	1	1
1	0	1
1	1	0

Table 1: Truth Table for the XOR gate.

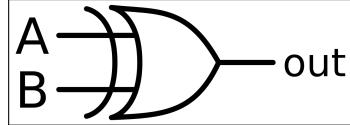


Figure 1: The symbol for the XOR gate.

3 Approach

I chose to start designing the CMOS logic using the function $F = A\bar{B} + \bar{A}B$. The first thing to do is to invert the function, since the output of a CMOS circuit is inverted. Therefore we must invert F and then implement that function in the pull down network. Using De Morgan's Law, we get: $\overline{F} = \overline{A\bar{B} + \bar{A}B} = \overline{A\bar{B}} \cdot \overline{\bar{A}B} = (\bar{A} + B)(A + \bar{B})$ Therefore $(\bar{A} + B)(A + \bar{B})$ will be implemented on the NMOS side. We do this by putting the transistors in parallel for OR and in series for AND. For the pull up network, we put the PMOS transistors in series for OR and in parallel for AND. I sketched out the resulting circuit, as shown in Figure 2.

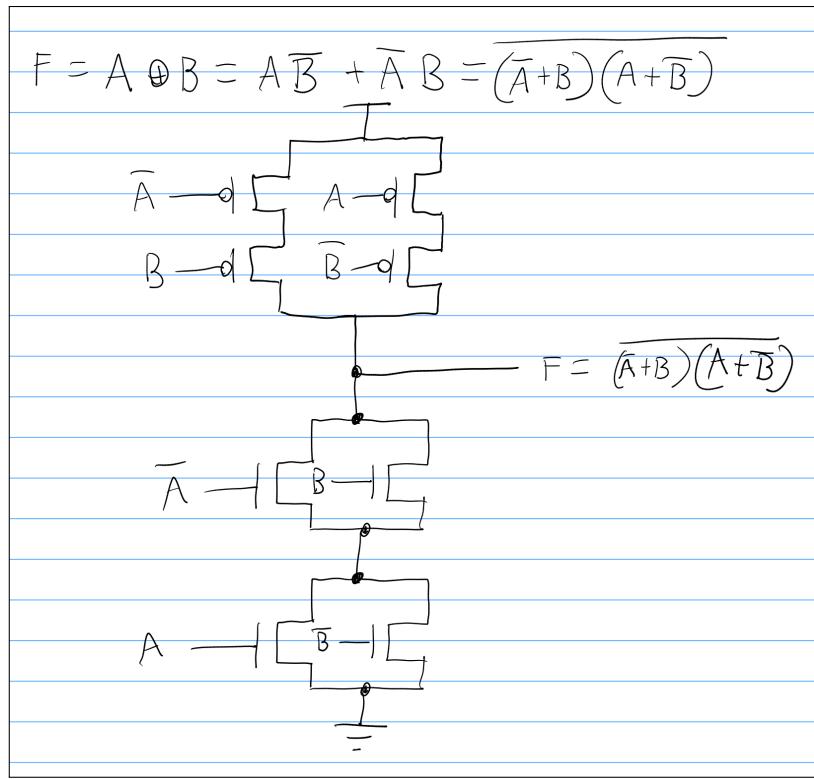


Figure 2: A sketch of the PUN and PDN for implementing the XOR gate.

Since we are only given A and B as inputs and not \bar{A} and \bar{B} as well, we have to invert A and B for the inputs where \bar{A} and \bar{B} are necessary. This requires two inverters at the inputs, as shown in the sketch in Figure 3.

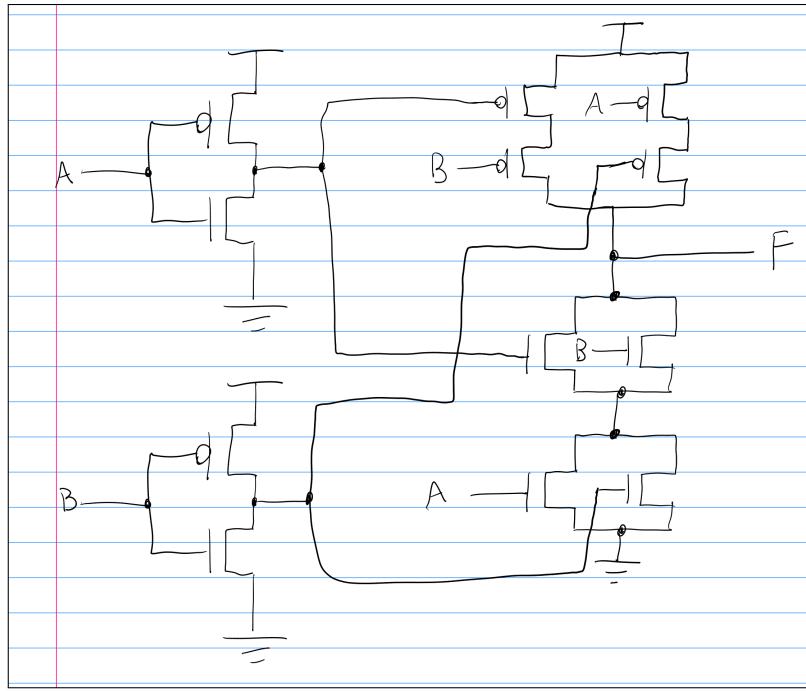


Figure 3: A sketch of the XOR gate in CMOS logic.

4 Schematic in Electric

The sketch of the circuit was then built in the schematic design portion of Electric. The final schematic can be seen in Figure 4. The various nets that feed into the PUN and PDN are labeled to make the schematic easier to read. The transistors were initially chosen to be 8λ wide and 2λ long for PMOS and 4λ wide and 2λ because those are the dimensions that worked best for the inverter that we designed previously. However, we were told to make the PMOS transistors and NMOS transistors the same size, so I made them all 8λ wide and 2λ .

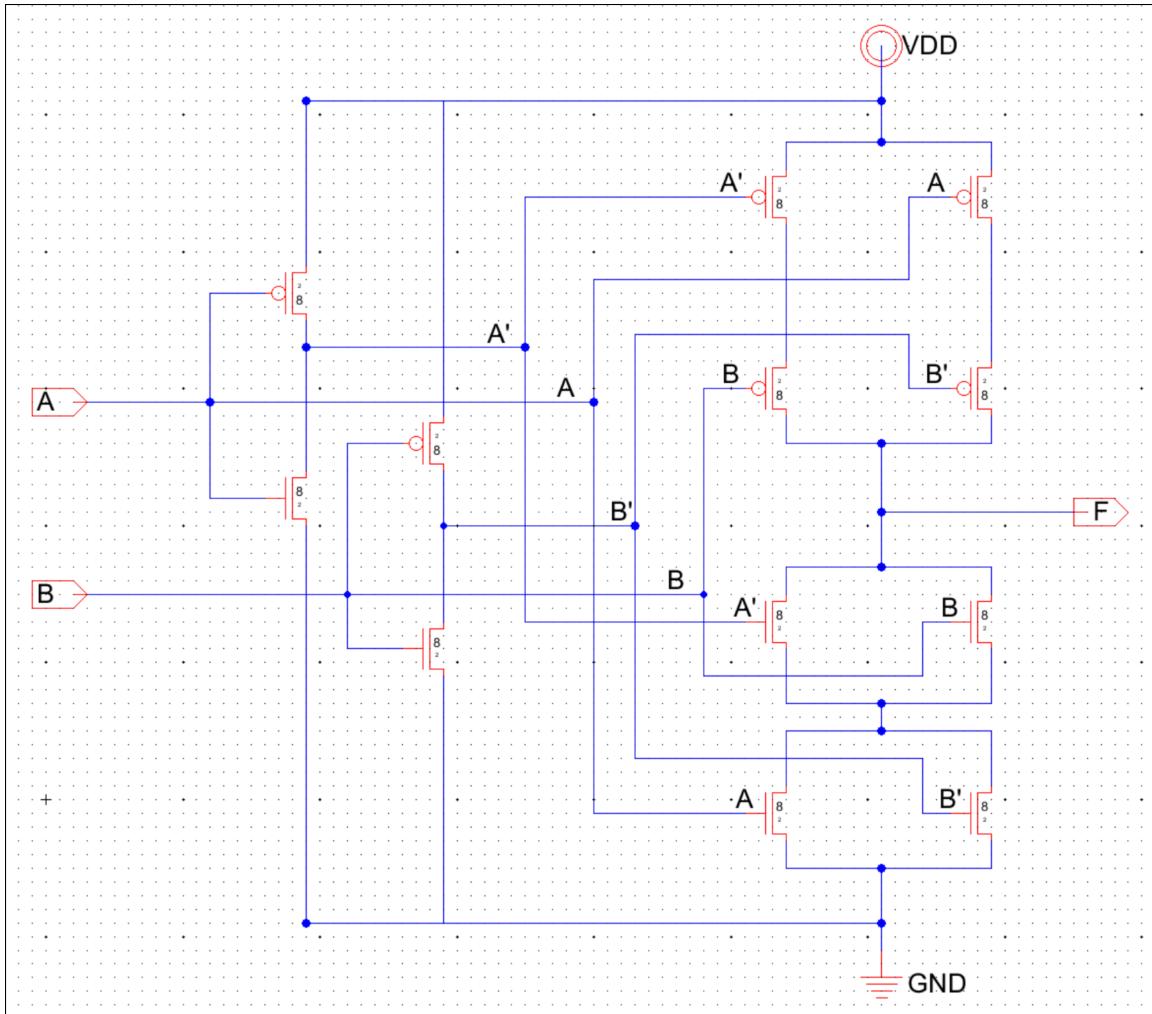


Figure 4: The finished schematic in Electric.

After designing the schematic in electric, it must pass the Design Rule Check (DRC) in order to be simulated properly. The DRC checks to make sure there are no major issues with the schematic. The results of the DRC are shown in Figure 5. The DRC has found no errors and the design can be simulated.

```

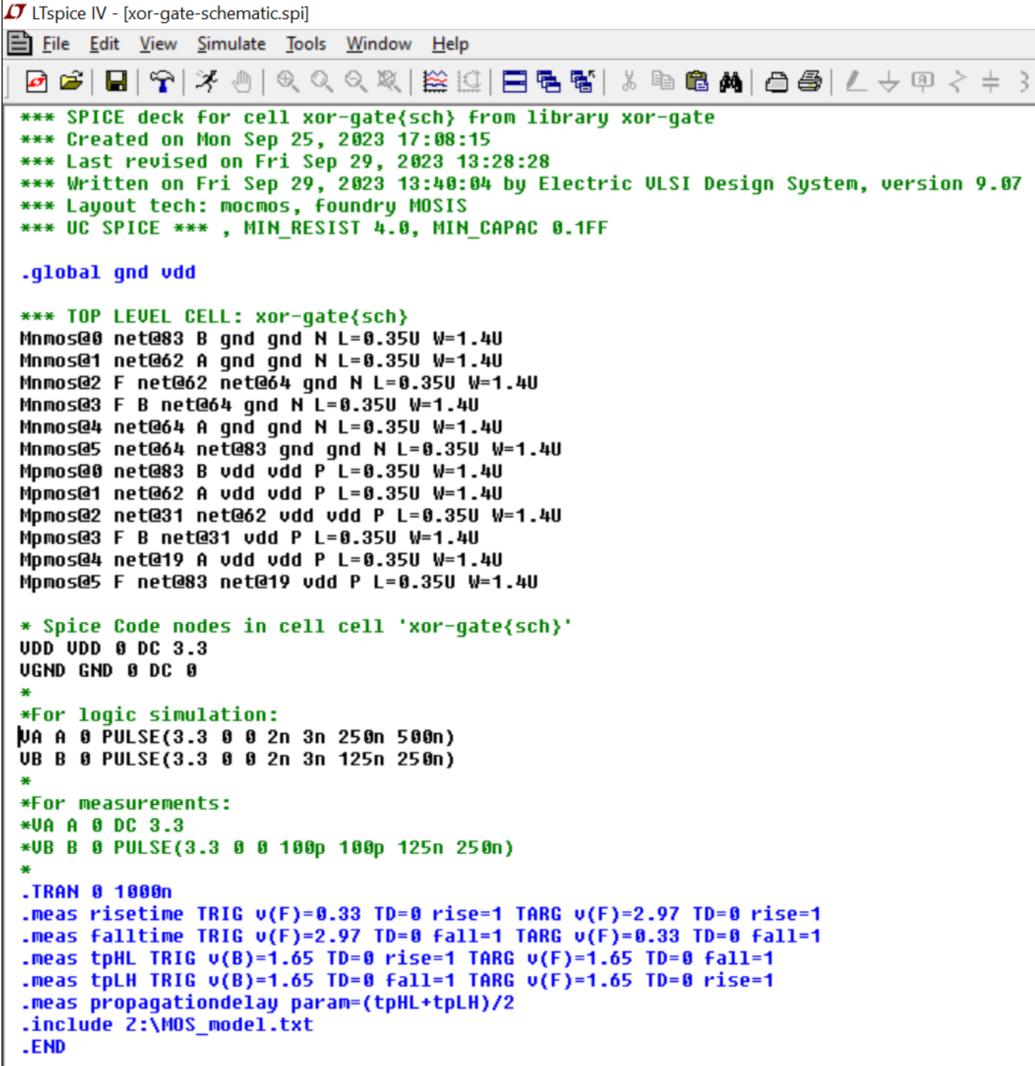
Electric Messages
=====
Checking schematic cell 'xor-gate{sch}'
No errors found
0 errors and 0 warnings found (took 0.0 secs)

```

Figure 5: The DRC for the schematic shows no errors.

5 Schematic Simulation

The spice code for the simulation of the XOR gate schematic is shown in Figure 6. For this simulation, we are required to generate a 2MHz digital signal for input A and a 4MHz digital signal for input B. Both of these signals must have a rise time of 2ns and a fall time of 3ns. This is accomplished with the spice lines `VA A 0 PULSE(3.3 0 0 2n 3n 250n 500n)` for input A and `VB B 0 PULSE(3.3 0 0 2n 3n 125n 250n)` for B. The resulting output signal from these two pulsed input signals can be seen on net F in the simulation graphs.



```

LTspice IV - [xor-gate-schematic.spi]
File Edit View Simulate Tools Window Help
File Edit View Simulate Tools Window Help
*** SPICE deck for cell xor-gate{sch} from library xor-gate
*** Created on Mon Sep 25, 2023 17:08:15
*** Last revised on Fri Sep 29, 2023 13:28:28
*** Written on Fri Sep 29, 2023 13:40:04 by Electric VLSI Design System, version 9.07
*** Layout tech: mocmos, Foundry MOSIS
*** UC SPICE *** , MIN_RESIST 4.0, MIN_CAPAC 0.1FF

.global gnd vdd

*** TOP LEVEL CELL: xor-gate{sch}
Mnmos@0 net@83 B gnd gnd N L=0.35U W=1.4U
Mnmos@1 net@62 A gnd gnd N L=0.35U W=1.4U
Mnmos@2 F net@62 net@64 gnd N L=0.35U W=1.4U
Mnmos@3 F B net@64 gnd N L=0.35U W=1.4U
Mnmos@4 net@64 A gnd gnd N L=0.35U W=1.4U
Mnmos@5 net@64 net@83 gnd gnd N L=0.35U W=1.4U
Mpmos@0 net@83 B vdd vdd P L=0.35U W=1.4U
Mpmos@1 net@62 A vdd vdd P L=0.35U W=1.4U
Mpmos@2 net@31 net@62 vdd vdd P L=0.35U W=1.4U
Mpmos@3 F B net@31 vdd P L=0.35U W=1.4U
Mpmos@4 net@19 A vdd vdd P L=0.35U W=1.4U
Mpmos@5 F net@83 net@19 vdd P L=0.35U W=1.4U

* Spice Code nodes in cell cell 'xor-gate{sch}'
VDD VDD 0 DC 3.3
VGND GND 0 DC 0
*
*For logic simulation:
VA A 0 PULSE(3.3 0 0 2n 3n 250n 500n)
VB B 0 PULSE(3.3 0 0 2n 3n 125n 250n)
*
*For measurements:
*VA A 0 DC 3.3
*VB B 0 PULSE(3.3 0 0 100p 100p 125n 250n)
*
.TRAN 0 1000n
.meas risetime TRIG v(F)=0.33 TD=0 rise=1 TARG v(F)=2.97 TD=0 rise=1
.meas falltime TRIG v(F)=2.97 TD=0 fall=1 TARG v(F)=0.33 TD=0 fall=1
.meas tpHL TRIG v(B)=1.65 TD=0 rise=1 TARG v(F)=1.65 TD=0 fall=1
.meas tpLH TRIG v(B)=1.65 TD=0 fall=1 TARG v(F)=1.65 TD=0 rise=1
.meas propagationdelay param=(tpHL+tpLH)/2
.include Z:\MOS_model.txt
.END

```

Figure 6: The spice code for simulating the schematic of the XOR gate.

The graphs for the spice simulation of the XOR gate schematic are shown in Figure 7. This simulation shows that the schematic is functioning properly since it behaves exactly as we expect an XOR gate to behave. Compare Figure 7 to Table 1 to see that the functionality is identical.

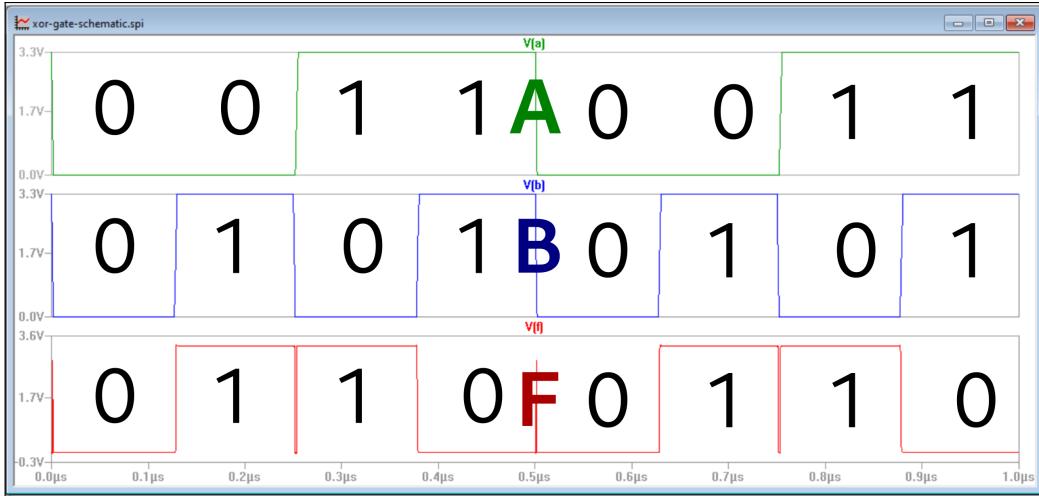


Figure 7: The resulting graphs from the spice simulation of the XOR gate schematic.

IRSIM is different to spice in that its simulation is purely digital. We can use IRSIM to confirm that the behavior of our XOR gate is correct from a purely digital standpoint. IRSIM does not accurately simulate timing like spice does, but is simply another way to validate our design. The rising and falling edges of the inputs must be set manually, and the output at F is automatically shown with each change to the inputs by the user. The resulting graph from the IRSIM simulation of the XOR gate schematic is shown in Figure 8. This simulation shows the correct results that match Figure 7 and Table 1.

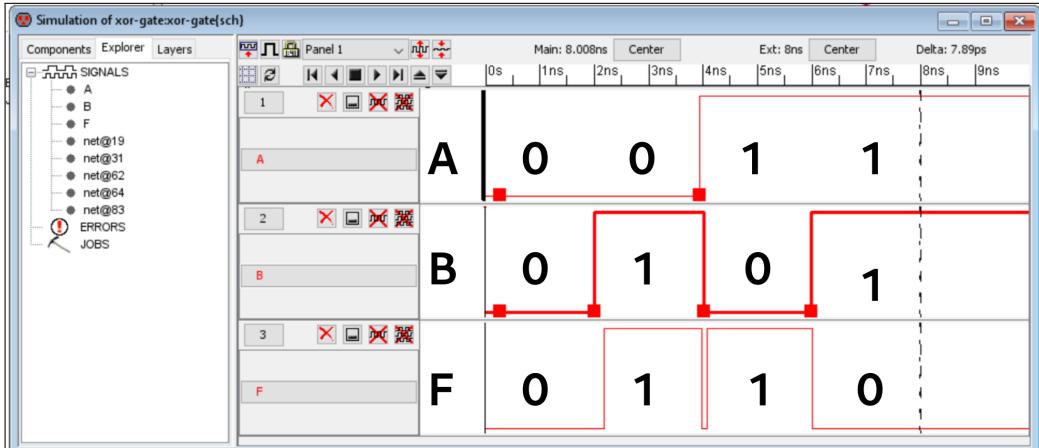


Figure 8: The resulting graphs from the IRSIM simulation of the XOR gate schematic.

6 Schematic Measurements

We are interested in a number of measurements that give us some indication about the performance of our design. The first measurement we are concerned with is the Rise Time of the output signal. The Rise Time of a signal is the amount of time it takes for the signal to go from 10% of VDD to 90% of VDD on a rising edge. A rise time that is too slow can cause issues with the propagation of

the signal through a system. Similarly, the Fall Time is the time it takes for a signal to go from 90% of VDD to 10% of VDD on the falling edge. It is also important that the fall time be fast enough.

Another important metric is the propagation delay. t_{pHl} is a measure of the time between when the rising edge of the input signal hits 50% of VDD and when the falling edge of the output signal hits 50% of VDD. It essentially tells us the time for a rising edge to propagate from input to falling edge of the output. Similarly, t_{pLH} is the time from falling edge of the input to rising edge of the output (also measured from 50% of VDD for each). The propagation delay is then the average of the two, as in $Propagation\ Delay = \frac{t_{pHl} + t_{pLH}}{2}$.

The spice code for measuring these parameters is shown in Figure 9. The first thing to note is that input A is kept at a constant 3.3V so that we can pulse input B and get the inverse waveform at output F. The rise and fall times were also modified from 2ns and 3ns to 100ps. I found that the 2ns and 3ns rise and fall times were too slow, and as a result the output signal would actually reach 50% of VDD before the input signal did. Changing the rise and fall times to 100ps solved this issue and allowed me to take accurate measurements.

LTspice IV - [xor-gate-schematic.spi]

File Edit View Simulate Tools Window Help

```

*** SPICE deck For cell xor-gate{sch} from library xor-gate
*** Created on Mon Sep 25, 2023 17:08:15
*** Last revised on Fri Sep 29, 2023 13:28:28
*** Written on Fri Sep 29, 2023 13:40:04 by Electric VLSI Design System, version 9.07
*** Layout tech: mocmos, Foundry MOSIS
*** UC SPICE *** , MIN_RESIST 4.0, MIN_CAPAC 0.1FF

.global gnd vdd

*** TOP LEVEL CELL: xor-gate{sch}
Mnmos@0 net@83 B gnd gnd N L=0.35U W=1.4U
Mnmos@1 net@62 A gnd gnd N L=0.35U W=1.4U
Mnmos@2 F net@62 net@64 gnd N L=0.35U W=1.4U
Mnmos@3 F B net@64 gnd N L=0.35U W=1.4U
Mnmos@4 net@64 A gnd gnd N L=0.35U W=1.4U
Mnmos@5 net@64 net@83 gnd gnd N L=0.35U W=1.4U
Mpmos@0 net@83 B vdd vdd P L=0.35U W=1.4U
Mpmos@1 net@62 A vdd vdd P L=0.35U W=1.4U
Mpmos@2 net@31 net@62 vdd vdd P L=0.35U W=1.4U
Mpmos@3 F B net@31 vdd vdd P L=0.35U W=1.4U
Mpmos@4 net@19 A vdd vdd P L=0.35U W=1.4U
Mpmos@5 F net@83 net@19 vdd vdd P L=0.35U W=1.4U

* Spice Code nodes in cell cell 'xor-gate{sch}'
VDD VDD 0 DC 3.3
VGND GND 0 DC 0
*
*For logic simulation:
*VA A 0 PULSE(3.3 0 0 2n 3n 250n 500n)
*VB B 0 PULSE(3.3 0 0 2n 3n 125n 250n)
*
*For measurements:
VA A 0 DC 3.3
VB B 0 PULSE(3.3 0 0 100p 100p 125n 250n)
*
.TRAN 0 1000n
.meas risetime TRIG v(F)=0.33 TD=0 rise=1 TARG v(F)=2.97 TD=0 rise=1
.meas falltime TRIG v(F)=2.97 TD=0 Fall=1 TARG v(F)=0.33 TD=0 Fall=1
.meas tpHL TRIG v(B)=1.65 TD=0 rise=1 TARG v(F)=1.65 TD=0 fall=1
.meas tpLH TRIG v(B)=1.65 TD=0 Fall=1 TARG v(F)=1.65 TD=0 rise=1
.meas propagationdelay param=(tpHL+tpLH)/2
.include Z:\MOS_model.txt
.END

```

Figure 9: The spice code that measures the rise time, fall time, and propagation delay of the output signal of the XOR gate schematic.

The lines of spice code that start with `.meas` are the lines that actually take the measurements we are interested in. The line `.meas risetime TRIG v(F)=0.33 TD=0 rise=1 TARG v(F)=2.97 TD=0 rise=1` calculates the rise time by recording the time when output F reaches 10% of VDD and the time when F reaches 90% of VDD and then finding the difference. Similarly, the line `.meas falltime TRIG v(F)=2.97 TD=0 fall=1 TARG v(F)=0.33 TD=0 fall=1` measures the fall time by determining the length of time between F reaching 90% of VDD and it reaching 10% of VDD. The line `.meas tpHL TRIG v(B)=1.65 TD=0 rise=1 TARG v(F)=1.65 TD=0 fall=1` measures t_{pHL} by finding the time between the 50% point of the rising edge of input B and the 50% point of the falling edge of output F. The line `.meas tpLH TRIG v(B)=1.65 TD=0 fall=1 TARG v(F)=1.65 TD=0 rise=1` does the same except it measures from the falling edge of B and the rising edge of F in order to measure t_{pLH} . Finally, the line `.meas propagationdelay param=(tpHL+tpLH)/2` averages t_{pHL} and t_{pLH} in order to calculate the propagation delay.

After running the code in LTSpice, the measurements can be viewed by opening the error log. The results of these measurements are shown in Figure 10. The measurements can be viewed more clearly in Table 2.

```

SPICE Error Log: Z:\xor-gate\xor-gate-schematic.log
Circuit: *** SPICE deck for cell xor-gate{sch} from library xor-gate

Vgnd: both pins shorted together -- ignoring.
Ignoring BSIM parameter XL
Ignoring BSIM parameter XW
Ignoring BSIM parameter XL
Ignoring BSIM parameter XW
Warning: Pd = 0 is less than W.
Warning: Ps = 0 is less than W.
Warning: Pd = 0 is less than W.
Warning: Ps = 0 is less than W.
Direct Newton iteration for .op point succeeded.

risetime=7.62027e-011 FROM 8.45158e-011 TO 1.60718e-010
falltime=3.52785e-011 FROM 1.25145e-007 TO 1.25181e-007
tphl=1.39575e-011 FROM 1.2515e-007 TO 1.25164e-007
tplh=5.62274e-011 FROM 5e-011 TO 1.06227e-010
propagationdelay: (tphl+tplh)/2=3.50925e-011

Date: Sat Sep 30 12:41:58 2023
Total elapsed time: 0.110 seconds.

tnom = 27
temp = 27
method = modified trap
totiter = 3059
traniter = 3030

```

Figure 10: The output from LTSpice showing the measurements done on the output of the XOR gate schematic.

Parameter	Measurement
Rise Time	76.2ps
Fall Time	35.3ps
t_{pHL}	14.0ps
t_{pLH}	56.2ps
Propagation Delay	35.1ps

Table 2: The measurements done on the XOR gate schematic in LTSpice.

7 Layout in Electric

I began designing the layout with a stick diagram, as shown in Figure 11. I started with the active areas and then drew the polysilicon gates. I planned out which gates would take which input signal by looking at the various nodes of the schematic in Figure 4 and determining which transistors from the schematic should be adjacent. Then I routed the metal layer to connect the transistor sources and drains to each other and to VDD and GND. Finally, I added the inverters to the left and routed A , B , \bar{A} , and \bar{B} to the proper transistor pairs on the right.

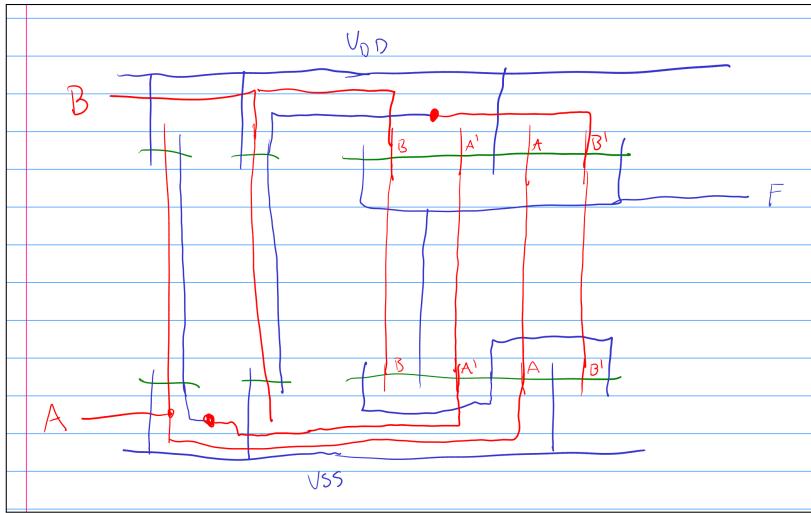


Figure 11: The stick diagram used to plan out the layout of the XOR gate.

I then turned the stick diagram into the layout in Figure 12 with some minor changes to optimize space. For instance, A is now on top on the input side and there is a much more direct connection from B at the input of the inverter to the input to the right of the inverter. Both of these changes save space. The spacing of every part of the design is as close as possible while still passing the DRC. The VDD and GND wells may look like they can be closer, but the metal to polysilicon contacts are in the way and there is nowhere else to place them. It may be noted that the NMOS transistors of the inverters are shifted up slightly - this is to allow me to place GND closer to the rest of the design. I would move the NMOS transistors from the PDN up as well, but that would cause the metal traces to be too close together to pass the DRC. As far as I am aware, every space between design elements has been minimized. The design also conforms to design rules discussed in class that are not built into Electric's design rules, such as the 3λ wide rule for the metal layer.

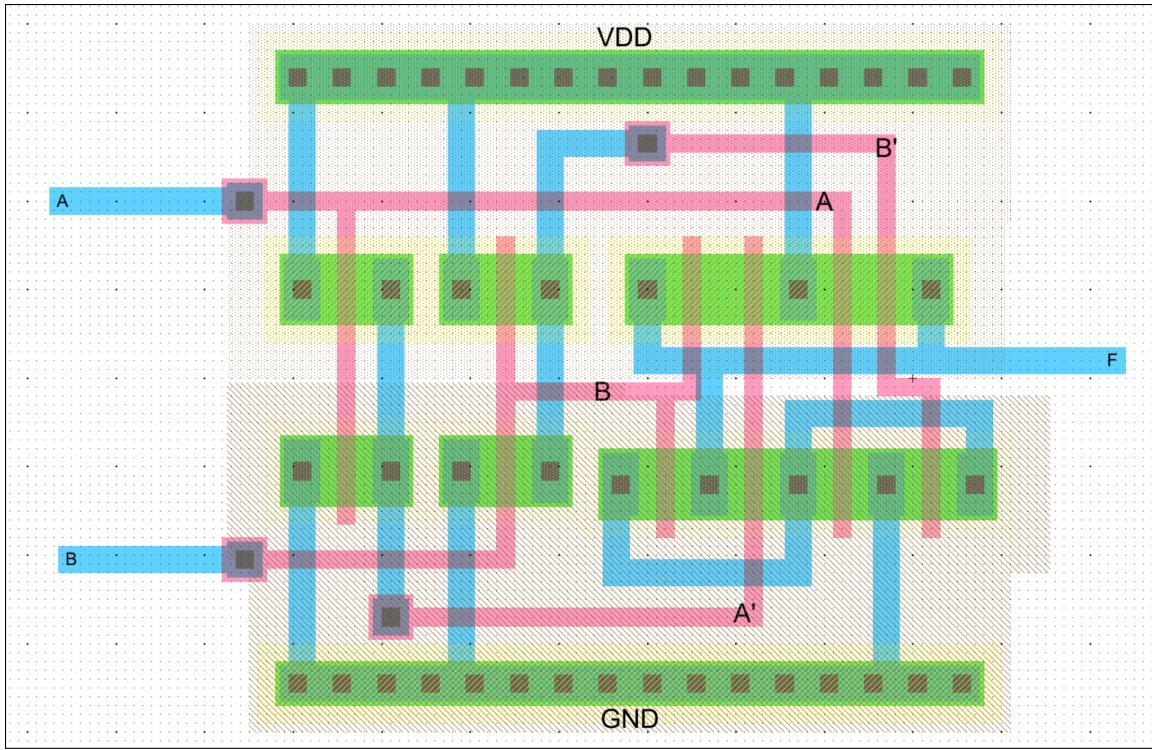
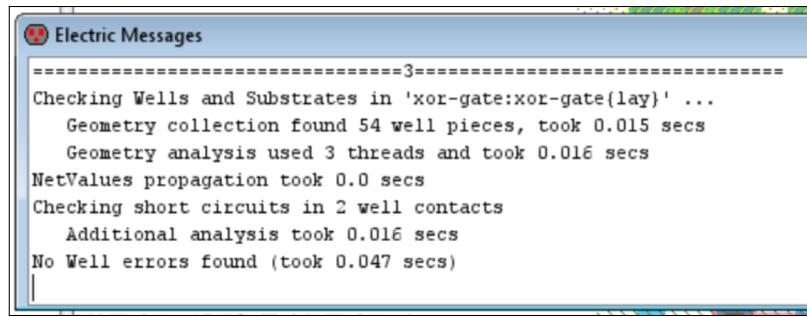


Figure 12: The layout of the XOR gate in Electric.

For the layout, the DRC is very important, since it specifies rules for distances between, widths of, and lengths of parts of the design that must be met. These rules ensure that the design is both functional and able to be manufactured. The results of the DRC check for the XOR gate layout are shown in figure 13. The design passes the DRC check. It is also important to do a well check (which is in the ERC tools in Electric) to ensure that wells that should be connected are. The results of this check are shown in Figure 14, which shows no errors.

```
Electric Messages
=====
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 25 networks
Checking cell 'xor-gate{lay}'
    No errors/warnings found
0 errors and 0 warnings found (took 0.359 secs)
```

Figure 13: The DRC results for the XOR gate layout showing no errors.



```
Electric Messages
=====
Checking Wells and Substrates in 'xor-gate:xor-gate{lay}' ...
    Geometry collection found 54 well pieces, took 0.015 secs
    Geometry analysis used 3 threads and took 0.016 secs
NetValues propagation took 0.0 secs
Checking short circuits in 2 well contacts
    Additional analysis took 0.016 secs
No Well errors found (took 0.047 secs)
```

Figure 14: The well check results for the XOR gate layout showing no errors.

8 Layout Simulation

The process for simulating the layout in LTSpice is essentially the same as for the simulation of the schematic. The spice code for the simulation can be seen in Figure 15.

```

LTspice IV - [xor-gate-layout.spi]
File Edit View Simulate Tools Window Help

*** SPICE deck For cell xor-gate{lay} from library xor-gate
*** Created on Mon Sep 25, 2023 20:41:36
*** Last revised on Fri Sep 29, 2023 14:17:18
*** Written on Fri Sep 29, 2023 14:20:05 by Electric VLSI Design System, version 9.07
*** Layout tech: mocmos, Foundry MOSIS
*** UC SPICE *** , MIN_RESIST 4.0, MIN_CAPAC 0.1FF

*** TOP LEVEL CELL: xor-gate{lay}
Mnmos@0 net@1 A gnd gnd N L=0.35U W=1.4U AS=4.349P AD=1.593P PS=11.375U PD=5.075U
Mnmos@1 net@3 B gnd gnd N L=0.35U W=1.4U AS=4.349P AD=1.593P PS=11.375U PD=5.075U
Mnmos@2 F B net@14 gnd N L=0.35U W=1.4U AS=1.286P AD=1.286P PS=3.937U PD=3.937U
Mnmos@3 net@14 net@1 F gnd N L=0.35U W=1.4U AS=1.286P AD=1.286P PS=3.937U PD=3.937U
Mnmos@4 gnd A net@14 gnd N L=0.35U W=1.4U AS=1.286P AD=4.349P PS=3.937U PD=11.375U
Mnmos@5 net@14 net@3 gnd gnd N L=0.35U W=1.4U AS=4.349P AD=1.286P PS=11.375U PD=3.937U
Mpmos@0 net@5 B F vdd P L=0.35U W=1.4U AS=1.286P AD=0.613P PS=3.937U PD=2.275U
Mpmos@1 vdd net@1 net@5 vdd P L=0.35U W=1.4U AS=0.613P AD=4.961P PS=2.275U PD=11.462U
Mpmos@2 net@8 A vdd vdd P L=0.35U W=1.4U AS=4.961P AD=0.482P PS=11.462U PD=2.363U
Mpmos@3 F net@3 net@8 vdd P L=0.35U W=1.4U AS=0.482P AD=1.286P PS=2.363U PD=3.937U
Mpmos@4 net@3 B vdd vdd P L=0.35U W=1.4U AS=4.961P AD=1.593P PS=11.462U PD=5.075U
Mpmos@5 net@1 A vdd vdd P L=0.35U W=1.4U AS=4.961P AD=1.593P PS=11.462U PD=5.075U

* Spice Code nodes in cell cell 'xor-gate{lay}'
VDD VDD 0 DC 3.3
VGND GND 0 DC 0
*
*For logic simulation:
VA A 0 PULSE(3.3 0 0 2n 3n 250n 500n)
VB B 0 PULSE(3.3 0 0 2n 3n 125n 250n)
*
*For measurements:
*VA A 0 DC 3.3
*VB B 0 PULSE(3.3 0 0 100p 100p 125n 250n)
*
.TRAN 0 1000n
.meas risetime TRIG v(F)=0.33 TD=0 rise=1 TARG v(F)=2.97 TD=0 rise=1
.meas falltime TRIG v(F)=2.97 TD=0 Fall=1 TARG v(F)=0.33 TD=0 Fall=1
.meas tpHL TRIG v(B)=1.65 TD=0 rise=1 TARG v(F)=1.65 TD=0 fall=1
.meas tPLH TRIG v(B)=1.65 TD=0 Fall=1 TARG v(F)=1.65 TD=0 rise=1
.meas propagationdelay param=(tpHL+tPLH)/2
.include Z:\MOS_model.txt
.END

```

Figure 15: The spice code for simulating the layout of the XOR gate.

The resulting waveforms from the spice simulation of the XOR gate layout are shown in Figure 16. This shows the same correct behavior we saw in Table 1 and the simulation of the schematic in Figure ??.

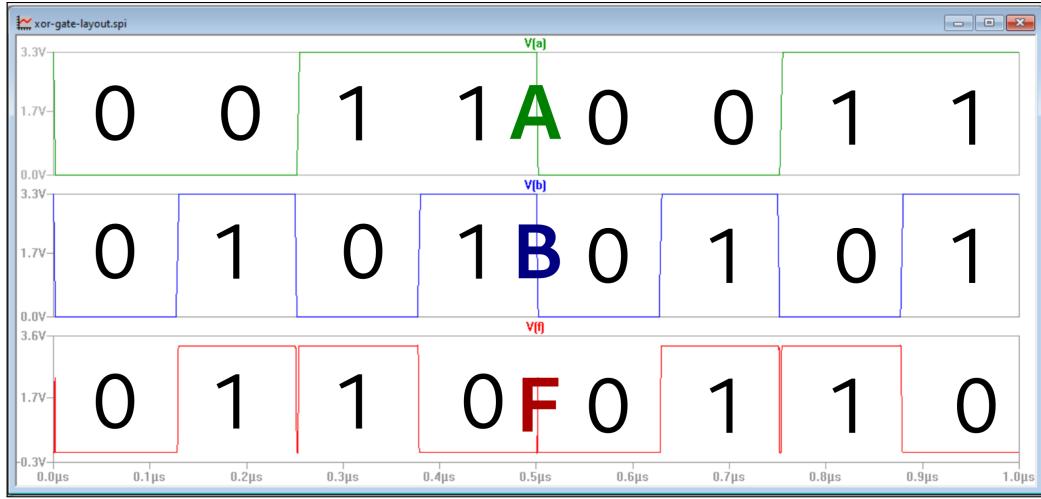


Figure 16: The resulting graphs from the spice simulation of the XOR gate layout.

The IRSIM simulation also follows the same procedure as with the schematic. The results for the IRSIM simulation are shown in Figure 17. The results are correct and match the simulation from LTSpice in Figure 16 and the logic shown in Table 1.

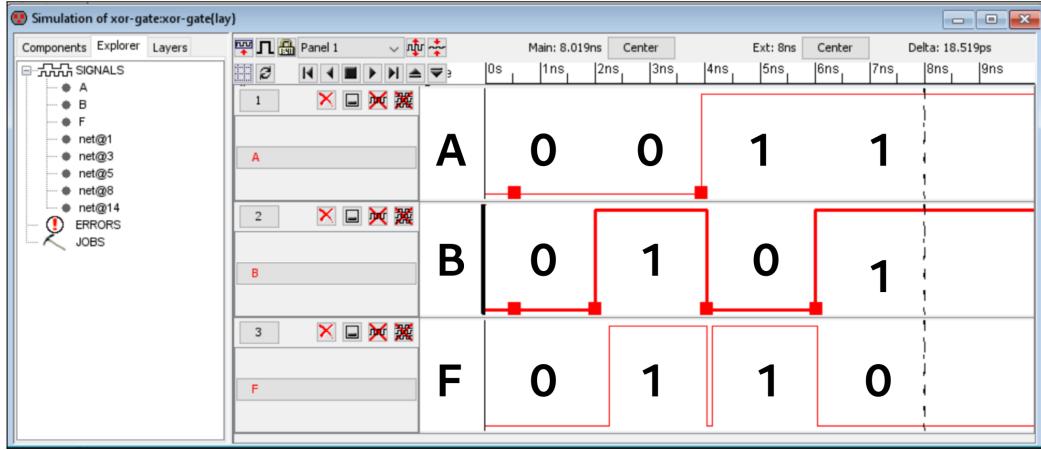


Figure 17: The resulting graphs from the IRSIM simulation of the XOR gate layout.

9 Layout Measurements

The same measurements are taken using LTSpice with the same procedure as detailed for the schematic. The spice code for taking these measurements is shown in Figure ??.

LTspice IV - [xor-gate-layout.spi]

File Edit View Simulate Tools Window Help

```

*** SPICE deck For cell xor-gate{lay} from library xor-gate
*** Created on Mon Sep 25, 2023 20:41:36
*** Last revised on Fri Sep 29, 2023 14:17:18
*** Written on Fri Sep 29, 2023 14:20:05 by Electric VLSI Design System, version 9.07
*** Layout tech: mocmos, Foundry MOSIS
*** UC SPICE *** , MIN_RESIST 4.0, MIN_CAPAC 0.1FF

*** TOP LEVEL CELL: xor-gate{lay}
Mnmos@0 net@1 A gnd gnd N L=0.35U W=1.4U AS=4.349P AD=1.593P PS=11.375U PD=5.075U
Mnmos@1 net@3 B gnd gnd N L=0.35U W=1.4U AS=4.349P AD=1.593P PS=11.375U PD=5.075U
Mnmos@2 F B net@14 gnd N L=0.35U W=1.4U AS=1.286P AD=1.286P PS=3.937U PD=3.937U
Mnmos@3 net@14 net@1 F gnd N L=0.35U W=1.4U AS=1.286P AD=1.286P PS=3.937U PD=3.937U
Mnmos@4 gnd A net@14 gnd N L=0.35U W=1.4U AS=1.286P AD=4.349P PS=3.937U PD=11.375U
Mnmos@5 net@14 net@3 gnd gnd N L=0.35U W=1.4U AS=4.349P AD=1.286P PS=11.375U PD=3.937U
Mpmos@0 net@5 B F vdd P L=0.35U W=1.4U AS=1.286P AD=0.613P PS=3.937U PD=2.275U
Mpmos@1 vdd net@1 net@5 vdd P L=0.35U W=1.4U AS=0.613P AD=4.961P PS=2.275U PD=11.462U
Mpmos@2 net@8 A vdd vdd P L=0.35U W=1.4U AS=4.961P AD=0.482P PS=11.462U PD=2.363U
Mpmos@3 F net@3 net@8 vdd P L=0.35U W=1.4U AS=0.482P AD=1.286P PS=2.363U PD=3.937U
Mpmos@4 net@3 B vdd vdd P L=0.35U W=1.4U AS=4.961P AD=1.593P PS=11.462U PD=5.075U
Mpmos@5 net@1 A vdd vdd P L=0.35U W=1.4U AS=4.961P AD=1.593P PS=11.462U PD=5.075U

* Spice Code nodes in cell cell 'xor-gate{lay}'
VDD VDD 0 DC 3.3
VGND GND 0 DC 0
*
*For logic simulation:
*VA A 0 PULSE(3.3 0 0 2n 3n 250n 500n)
*VB B 0 PULSE(3.3 0 0 2n 3n 125n 250n)
*
*For measurements:
VA A 0 DC 3.3
VB B 0 PULSE(3.3 0 0 100p 100p 125n 250n)
*
.TRAN 0 1000n
.meas risetime TRIG v(F)=0.33 TD=0 rise=1 TARG v(F)=2.97 TD=0 rise=1
.meas falltime TRIG v(F)=2.97 TD=0 Fall=1 TARG v(F)=0.33 TD=0 Fall=1
.meas tpHL TRIG v(B)=1.65 TD=0 rise=1 TARG v(F)=1.65 TD=0 fall=1
.meas tPLH TRIG v(B)=1.65 TD=0 Fall=1 TARG v(F)=1.65 TD=0 rise=1
.meas propagationdelay param=(tpHL+tPLH)/2
.include Z:\MOS_model.txt
.END

```

Figure 18: The spice code that measures the rise time, fall time, and propagation delay of the output signal of the XOR gate layout.