EE 457

Project #1

Due 9/30/2023 by 6PM.

Note: Late Penalty 5%/day, After 5 days, you receive zero on the project.

-2 point rule applies for any violations.

Design a CMOS 2-input exclusive OR gate using Electric to realize Boolean function

F= $A \oplus B$ = A.B'+A'.B = (A+B).(A'+B')

Provide the following:

1. Circuit schematic in Electric (snapshots)
2. Layout in Electric.(snapshots)
3. DRC and Well Check snapshots
4. Generated LTSPICE code snapshot. Use the A input with pulsed input that has period (T) of 2MHz digital pulse and it has 2ns rise and 3ns fall times. The initial delay is zero. Make the input B as the pulsed input that has period (T) of 4MHz digital pulse and it has 2ns rise and 3ns fall times.
5. Print the output waveform of LTSPICE using the pulsed "A" input and pulsed input B.
6. Label all waveforms and provide state as 1 or 0 on the waveforms.
7. Snapshots of IRSIM for digital simulation. Do not use the transient mode.
8. Put waveforms inputs A&B with output in the same plane.
9. DO NOT use TRANS mode which comes in IRSIM.

Note:

1. Do not hand draw schematics. Use only Electric.
2. Do not photograph using your phone.
3. All tables must be labeled and captioned on top of the table (e.g., Table 1: Data from the Schematic.)
4. All Figures must be labeled and captioned below the figure (e.g., Figure 1: Illustration of the Inverter Schematic.)
5. All grammar should be written professionally.
6. Do not use dark backgrounds for waveforms and schematics.

Do the following:

1. Watch appropriate Electric Tutorials. Make sure you have watched Tutorials #1, #2, #3 and #4 before starting this project.
2. Perform design rule checks to see if you violated any design rules (DRC).
3. Put text on inputs, output, VDD and VSS.
4. Make sure you provide a truth table.

What to turn-in: (violations will result in minus 2 points for each violation)

1. A typed report that has the following:
    a. Cover page (print the attached cover page). Type your name.

b. Executive Summary: Summarize your project in about 1/2 –page format.
c. Background: Provide some background and motivations, what your design does, etc.
d. Approach: Put theory of the operation and others. What will you do to accomplish the work? How will you approach this project? Etc.
e. Layout Details: Put layout of the CMOS gate from Electric. Use snapshots and put cropped screen in MSWord. Use the print command and put grid on the paper. Put stick diagram of your layout.
f. Simulate your designed circuit using LTSPICE. Provide output rise and fall times. Measure output delay from the input and compare the two.
g. Run IRSIM and verify your design with the truth table for both.
h. Conclusions: Put what you observed and what you did. Provide some measurement data to conclude your work.
i. **VERY IMPORTANT**: Label all your waveforms clearly using MS Word on LTSpice and IRSIM. Appropriate points will be deducted for not identifying and unclear representation of waveforms.
j. **Not following instructions will have deductions of points**.

EE 457: Digital Integrated Circuits

Project #1 Report Cover Sheet
Due: 9/30/2023 by 6PM

PROJECT TITLE: 2-Input CMOS Exclusive OR Gate

Student Name: Dylan Kirdahy

Your report should follow the following items in sequence. *Do not change the sequence.*	GRADE
Section 1: Executive Summary	/5
Section 2: Background and Approach (Include a truth table)	/5
Section 3: Electric Schematic	/15
Section 4: LTSPICE for Electric schematic	/10
Section 5: IRSIM for Electric schematic	/10
Section 6: Electric Layout	/25
Section 7: LTSPICE for Electric layout (compare with schematic)	/15
Section 8: IRSIM for Electric layout	/10
Section 9: Conclusions and References	/5
TOTAL	**/100**