CUNY The City University of New York

# ***ECE457 Digital IC Design***

## ***Project #2***

### ***Please Read Carefully before beginning work.***

Penalty rules: A) -5pts per day for late submission. After five days, a score of zero will be given, but you are still required to complete the report. B) -2pts for any violations and per hour delays submitted after 8PM. C) If the project does not work, you must mention it and do it again to complete the project. D) You must redo part of the project if you score less than 50%. **E) Please do not request to waive penalty submission after 5 days for any personal problems. You will receive zero after November 2, 2023.**

***Choose only one Project from (A) or (B).***
**Due on 10/28/23 by 8PM on Blackboard.**


**WARNING: This project is estimated to take over 30 hours. Please plan accordingly. I hope you enjoy it.**

Note: ALL reporting work must be done in MS Word. Please pay special attention to presenting your work in Electric layouts. Please make your layout print large so I can see it. Please put figure numbers, table numbers and refer them in your text rather than just have them in your report. All projects have a supply voltage of 3.3V. It is necessary to show all DRC and well checks for error free design. Make sure you set your lambda equal to 175nm.

**Choose from one of the following Projects:**

A) **Design of 8-Bit Binary MUX**
B) **Design 6-Bit CMOS binary divider**

**For Project (A):**
Design of 8-to-1 Multiplexer (MUX) using *both cases* of (1) only transmission gates (TG) and (2) conventional CMOS gates. Compare the TG design with conventional CMOS gate designs by ***performance, power, chip size, number of transistors***, etc. in a tabular form.

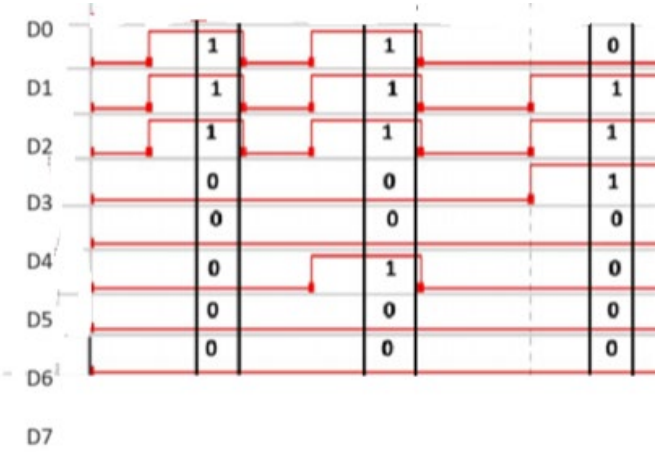
For a report, put the following as a guide for your own design:

1) Draw logic symbol, schematic for simulation.
2) Draw stick diagram and Euler's paths (do not give too many paths)
3) Electric Schematic & Layout
4) LTSPICE and IRSIM where needed to show performance
5) Verify your design by putting pulses to see the outputs.
6) Complete a Truth table for the MUX.
7) Find a Boolean expression for the MUX.

8) Run LTSPICE in Electric to "plot" waveforms of $V_{inputs}$ and $V_{out}$. Use 500ns period, 5ns rise time (tr) and 5ns fall time (tf) for Vin. Use 50% duty cycle which means 50% logic high and 50% logic low levels.

✓ Measure the output waveform by taking measurements for $t_r$, $t_f$, $T_{LH}$ and $T_{HL}$ for the first input, *D0* to the output Y0. You should name the other inputs D0, D1, D2, D3, D4, D5, D6, and D7.

✓ Write some paragraphs for design and measurements and make a project report. Write Figure numbers and captions. Attach the cover page. Follow the IEEE formats for references and use single column with 12 pt Times Roman font for report writing. Use digital waveforms shown below to show the eight inputs and show each output with respect to the switch positions. The input waveforms shown below is only for your reference. You may change the waveform as you would like.



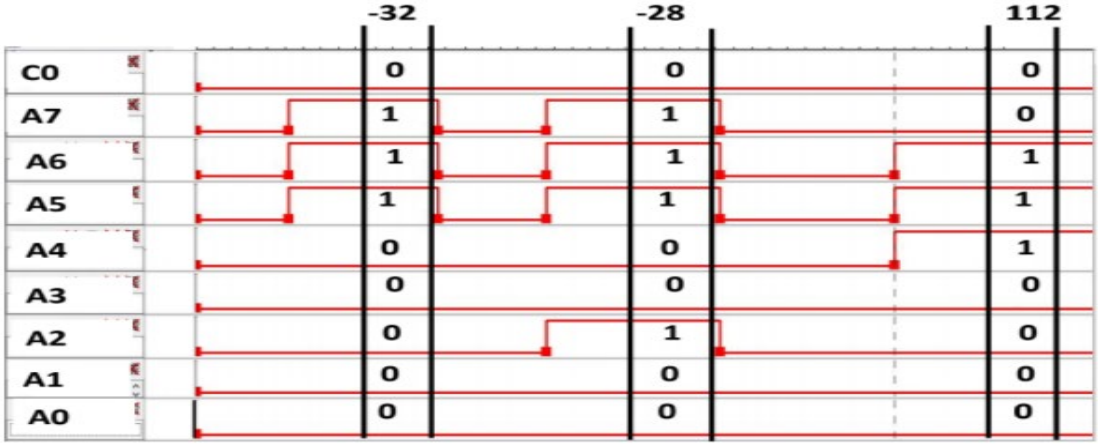

**For Project (B):**

Design a 6-bit CMOS Binary Divider. Show minimum of 3 divisions to show proper operations of your design. You may use transmission gates, static or dynamic CMOS design, but here you are not required to provide all the different cases. You can choose only one design case such as TG. You should work with ***signed two's complement numbers***. All numbers are represented in decimal numbers as examples in the following:

1) Draw a transistor level schematic of the 6-bit divider in Electric and simulate it in LTSpice.
2) Draw stick diagrams and Euler's paths where appropriate to design.
3) Perform the Electric Layout with IRSIM.

Verify your design by dividing the following numbers in signed 2's complement. All numbers are represented in decimal numbers as examples in the following: (A) +16/+2=+8; (B) +28/(-4)=-7; (C) -+4/+2=+2 to verify. **You must provide at least 3 division cases for verifications. Each verification is worth 3 points. You may provide more cases if you desire.**

Provide details of LTSPICE measurements on rise time, fall time and propagation delays. You can use the measurement feature on the LTSPICE tool.
Below waveforms show representation of all inputs A in three different numbers such as -32, -28 and 112 for a 8-bit binary number. Please use this technique to show your numbers for 6 digit binary number.




**What to turn-in: You will be graded for points in the table of the cover sheet.**

1. Follow the Grading cover page for sequence of your sections. Do not reorder them.
2. A typed report that has the following:
    a. Cover page (print the attached cover page)
    b. Executive Summary: Summarize your project in 1/2 –page format.
    c. Introduction: Provide some background and motivations
    d. Approach and calculations: Put schematics and details of the design. Put detailed calculations of all parameters. Put theory of the operation and others. Use schematic or drawing tools to draw schematic.
    e. LTSPICE Simulations: Put the output of the circuit in peace by peace as you need to analyze. Put input and output waveforms on the same panel. Make the waveforms clearly and label them.
    f. IRSIM of the layout. Verify all numbers that I asked.
    g. Perform waveform measurements for rise/fall times and periods. Put them in a table format to compare between the schematic and layout.
    h. Conclusion: Put what you observed and what you did.
    i. **References**: put any papers that are relevant to this project by using the IEEE format. The IEEE format is only for the reference section.
3. Calculate the following parameters:
   Compute the total chip area. Do not simply give me lambda by lambda. I need you to give me micrometer by micrometer, i.e., micrometer squired.
4. Pay attention to Electric layouts. Is it compact? Is the layout in box form? Are signals flowing from left to right? Are signals ready to be tied to next stage of logic gates? Etc.

# EE457: Digital IC Design

# Project #2 FALL SEMESTER 2023

# Report Cover Sheet*

**Due 10/28/2023 by 8PM (-2 pts per hour up to 5 points/day)**

**PROJECT TITLE:** CMOS 8-to-1 MUX

**Student's Name**:_____

| **Topics (Do not change orders of section)** | GRADES |
|---|---|
| Section1: Executive Summary (1/2 page) | Required |
| Section 2: Introduction and Background | /5 |
| Section 3: Electric Circuit Schematics<br>(TG and Conventional CMOS designs) | /10 |
| Section 4: LTSPICE Simulation for Schematic<br>(TG and Conventional CMOS designs) | /10 |
| Section 5: IRSIM for Schematic<br>(TG and Conventional CMOS designs) | /10 |
| Section 6: Electric Layouts (landscape mode and must legible to see gates)<br>(TG and Conventional CMOS designs) | /25 |
| Section 7: LTSPICE Simulation for Layouts<br>(TG and Conventional CMOS designs) | /10 |
| Section 8: IRSIM for Layout<br>(TG and Conventional CMOS designs) | /10 |
| Section 9: Compare LTSPICE Measurements for Schematic and Layout (must provide comparisons between the two in table format)<br>Provide delays, rise and fall times. | /10 |
| Section 10: Measurements of chip area, number of transistors for the layout (provide a table to compare) and write summary for TG and CMOS designs. | /10 |
| Section 11: Conclusions and References | Required |
| Late Penalty | |
| TOTAL | **/100** |

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# EE457: Digital IC Design
# Project #2 FALL SEMESTER 2023
# Report Cover Sheet

**Due 10/28/23 by 8PM (-2 pts per hour up to 5 points/day)**

***PROJECT TITLE:**6-Bit CMOS Binary Divider

*Student's Name:_____

| Sections<br>(**Do not change order of sections**.)* | GRADE Points |
|---|---|
| 1. Executive Summary (1/2-page) | /Required |
| 2. Introduction | /5 |
| 3. Electric Circuit Schematic (transistor level) | /10 |
| 4. LTSpice simulations of Schematic (label waveforms. 3 Verifications) | /10 |
| 5. IRSIM simulations of Schematic (label waveforms. 3 Verifications) | /10 |
| 6. Electric Layout (show all details, Euler, stick) | /25 |
| 7. LTSpice simulation of Layout (3 verifications) | /10 |
| 8. IRSIM Simulations of layout (3 verifications) | /10 |
| 9. Measurements in<br>a) Propagation delays of critical path (I/O)<br>b) Total Chip area in $um^2$ | /5<br>/5 |
| 10. Comparisons of Schematic & Layout in **table form**<br>(Find out any difference of delays, do not use the same waveforms from LTSPICE to IRSIM) | /10 |
| 11. Conclusion and References | /Required |
| Late Penalty: | |
| TOTAL | **/100** |

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