EE457: Digital IC Design

Project #2 FALL SEMESTER 2023

Report Cover Sheet*

Due 10/28/2023 by 8PM (-2 pts per hour up to 5 points/day)

PROJECT TITLE: CMOS 8-to-1 MUX

Student's Name: Dylan Kirdahy

Topics (Do not change orders of section)	GRADES
Section1: Executive Summary (1/2 page)	Required
Section 2: Introduction and Background	/5
Section 3: Electric Circuit Schematics (TG and Conventional CMOS designs)	/10
Section 4: LTSPICE Simulation for Schematic (TG and Conventional CMOS designs)	/10
Section 5: IRSIM for Schematic (TG and Conventional CMOS designs)	/10
Section 6: Electric Layouts (landscape mode and must legible to see gates) (TG and Conventional CMOS designs)	/25
Section 7: LTSPICE Simulation for Layouts (TG and Conventional CMOS designs)	/10
Section 8: IRSIM for Layout (TG and Conventional CMOS designs)	/10
Section 9: Compare LTSPICE Measurements for Schematic and Layout (must provide comparisons between the two in table format) Provide delays, rise and fall times.	/10
Section 10: Measurements of chip area, number of transistors for the layout (provide a table to compare) and write summary for TG and CMOS designs.	/10
Section 11: Conclusions and References	Required
Late Penalty	
TOTAL	**/100**

*Penalty rules: A) -5pts per day for late submission. After five days, a score of zero will be given, but you are still required to complete the report. B) -2pts for any violations and delays submitted after 8PM.