ECE457 Digital IC Design

Project #3 Due 12/07/2023 by 8PM

NOTE: Congratulations on making this far. You must provide any missing projects (#1, #2 or #3) and HW before 12/11/2023.

This project is limited to a single person. This is not a group project.

WARNING: This project is estimated to take over 40 hours. Please plan accordingly.

Note: ALL reporting work must be done in MS Word. Please pay special attention to presenting your work in Electric layouts. Please make your layout print large so I can see it. Please put figure numbers, table numbers and refer them in your text rather than just have them in your report. All projects have a supply voltage of 3.3V. It is necessary to show all DRC and well checks for error free design. Make sure you set your lambda equal to 175nm.

Note: **5 points/day penalty for late submission with notice.**

Project #3: 4-Bit Shift Register

Design of 4-bit binary shift register using D F/F. It has a serial input (Din) and four parallel outputs (Q0, Q1, Q2, Q3). Data changes at a positive edge clock. Provide all output logic timing waveforms and perform measurements in delays with LTSPICE and Pathwave ADS. You may choose to use a combination of TG, static CMOS and dynamic CMOS circuits.

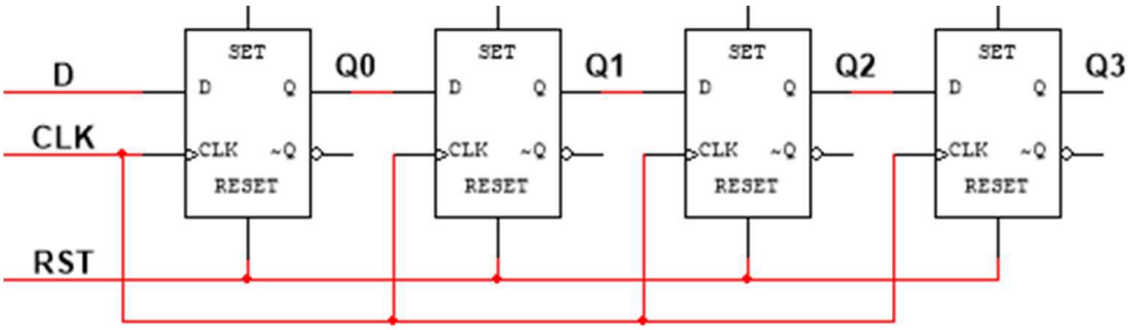

Figure 1. 4-Bit Shift Register using four D-F/Fs.

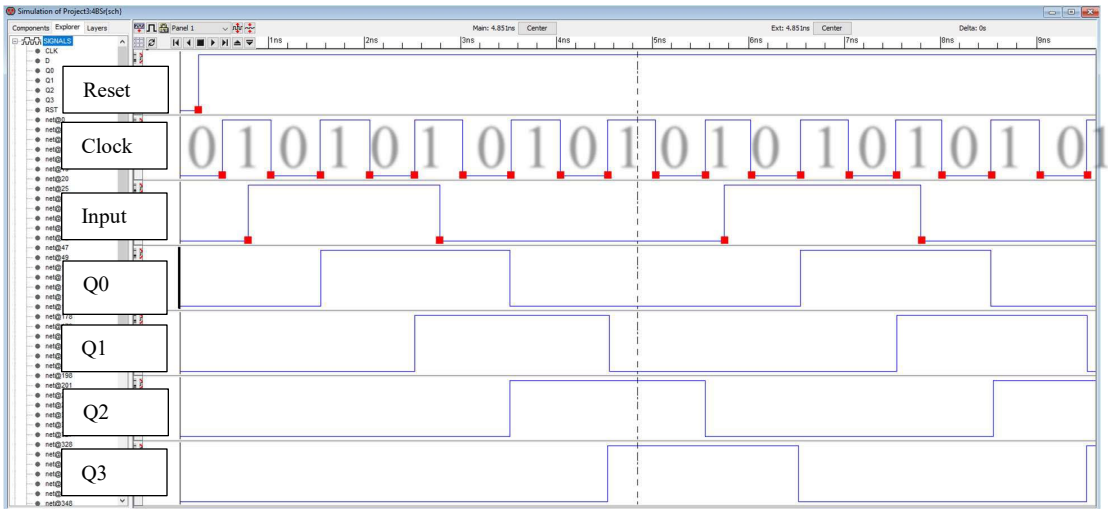

Figure 2. Example of Outputs of 4-Bit shift register.

For a report, put the following as a guide for your own design:

1) Draw logic symbols and transistor schematics for simulation.
2) Draw stick diagram and Euler's paths for D F/F design.
3) Electric Schematic & Layout
4) LTSPICE and IRSIM wherever needed to show performance.
5) Verify your design by putting pulses to see the outputs.
6) Extract Rp, Rn, and C's from your layout using electric. Use the extraction guide I put under the CAD folder.
7) Run LTSPICE in Electric to "plot" waveforms of Vinputs and Vout. Use 100ns period, 5ns rise time (tr) and 5ns fall time (tf) for Vin. Use 50% duty cycle which means 50% logic high and 50% logic low levels.
8) DO NOT use D-Latch
9) Use Positive triggered D-F/F using Master Slave F/F
10) Show the shifting of your input data

This is a hint for LTSPICE: For the parasitic extraction, follow exactly what it says in this link: http://cmosedu.com/cmos1/ltspice/ltspice_electric.htm. Use this extraction for the Pathwave ADS simulations. In the drop-down menu labeled "Parasitics", select the "Conservative RC" option instead of the default "Trans area/Perim only" option. This is what gives you the R and C values when you click Tools -> Simulation (Spice) -> Write Spice Deck. In the tutorial it tells you to save the file C5_models.txt to C:\Electric for SPICE simulations. Then in the LTSPICE code you have to write ".include C:\Electric\C5_models.txt".

1) Measure the output waveform by taking measurements for t_r, t_f, T_{LH} and T_{HL} for the first input, *W0*.

2) Write some paragraphs for design and measurements and make a project report. Write Figure numbers and captions. Attach the cover page.

Pathwave Advanced Design System (Provide circuit simulations)

1. The computers in ST269 are configure to dual-boot to Linux or Windows 10 during a restart of the operation system.

a. In Linux, restart the computer and select from the boot menu "Windows Boot Manager (on /dev/nvme0n1p1)" and press Enter key to boot to Windows 10.

b. In Windows, restart the computer to boot to Linux, no user action is require, as this is the default operation system selected.

For EE457 PathWave Advanced Design System (ADS) software are in ST269

1. **Sign in** using your citymail or ccny email credentials, type in your username and password to authenticate at the computer.
2. Double-click on the **Advanced Design System 2024 Update 0.1 (64-bit Simulations)** shortcut to run the PathWave Advanced Design System (ADS) Software.
3. Select, I want to specify a network license server from the License Setup Wizard for Advance Design System 2024 window.
4. Enter **27009@134.74.17.231** for Network license server name.

NOTE: The PathWave Advanced Design System (ADS) software are installed on 6 computers so far, the first 6 Dell OptiPlex 5090 desktop computers facing the entrance into ST269.

What to turn-in:

A) You will be graded for points in the table of the cover sheet.
B) Use single space with 12 pt font. Do not double space due to page counts.
C) Do not try to make your report long with unnecessary pages that includes non-trivial data such as printing extraction data.

1. A typed report that has the following:
    a. Cover page (print the attached cover page)
    b. Executive Summary: Summarize your project in 1/2 –page format. **Note: Single space format.**
    c. Introduction: Provide some background and motivation
    d. Approach and calculations: Put schematics and details of the design. Put detailed calculations of all parameters. Put theory of the operation and others. Use schematic or drawing tools to draw schematic.
    e. LTSPICE Simulations: Put the output of the circuit in piece by piece as you need to analyze. Put input and output waveforms on the same panel.
    f. Perform waveform measurements for rise/fall times and periods.
    g. Provide transistor counts, power, chip size, trade-offs, etc.
    h. Conclusion: Put what you observed and what you did.
    i. **References**: put any papers that are relevant to this project by using the IEEE format and reference in your text.
2. Calculate the following parameters in a table format:
    a. Calculate transistor sizes (W/L) and delays.

b. Power dissipation of the device. Use hand calculation after the extraction and let LTSpice provide the supply current for power.
c. Total chip area. Provide in units of micrometer square.

3. Turn in your project on Blackboard.
4. ***Five points will be deducted for not following the directions.***
5. ***Five points per day will be deducted for late reports with prior notice by email.***
6. ***Provide section numbers in your report.***

I have summarized how I would grade your report.

Executive Summary: Put at least ½ page of the entire work in single space.
Introduction/Background: Put why you are doing this work. Motivation behind the work and general description of work you have done.
Circuit Schematics/Symbols: put circuit schematics in detail. Put each sub-circuits as well as the entire one. If they are too small, I cannot see them. Make text big enough to see. Put figures with captions and refer them in you text.
Working Electric Layouts: Your layout must be optimized which means make them look good and not wasteful in space. ***It must be working. If it is not working, you cannot get credit.*** Put figures with captions and refer them in your text.
IRSIM Logic Simulations: Put text on waveforms to tell me what is going on. If you just print them out, I don't know what you are giving me. Run all parts of the IRSIM to verify your design. Put figures with captions and refer them in you text.
Measurements of power/delay/chip area/timing: I want all measurements such as power, delays, timing, chip area, number of transistors, etc. Put figures with captions and refer them in you text.
LTSPICE code/extractions: Put your code and tell me how you extracted certain parasitics from your layout. Put figures with captions and refer them in you text.
Measurements in LTSPICE: Make all measurements in the LTSPICE using measurement tool. Put figures with captions and refer them in you text.
Conclusion and References: Put ½ page of conclusion in single space and make sure you put all references for reading and referring them in your text.

EE457: Digital IC Design

Project 3 Report Cover Sheet

Due 12/07/2023

PROJECT TITLE: CMOS 4-bit shift register

Student Name:_____

Topics **(Do Not change order of sections)**	GRADES
Section1: Executive Summary (1/2 page)	Required
Section 2: Introduction and Background	/5
Section 3: Electric Circuit Schematics (transistors only)	/10
Section 4: LTSPICE Simulation for Schematic	/10
Section 5: IRSIM for Schematic	/10
Section 6: Electric Layouts (landscape mode for the final version and others to show all layout details)	/20
Section 7: LTSPICE Simulation for Layouts	/10
Section 8: IRSIM simulations for Layout	/10
Section 9: Compare LTSPICE Measurements for Schematic and Layout (must provide comparisons between the two in table format) Provide some delays, rise and fall times.	/10
Section 10: Measurements of chip area and number of transistors for the layout	/5
Section 11: Pathwave Adanced Design System	/10
Section 12: Conclusions and References	Required
Late Penalty (-5 points per day with prior 24 hour email notice) Max. of 2 days for late submission. Submit on Blackboard. -10 points for no Electric schematic and layout files	
TOTAL	**/100**

Do not erase: *Penalty rules: A) -5pts per day for late submission. After two days (12/9), a score of zero will be given, but you are still required to complete the report. B) -2pts for any violations and delays submitted after 8PM.