EE457: Digital IC Design

Project 3 Report Cover Sheet

Due 12/07/2023

PROJECT TITLE: CMOS 4-bit shift register

Student Name: Dylan Kirdahy

Topics **(Do Not change order of sections)**	GRADES
Section1: Executive Summary (1/2 page)	Required
Section 2: Introduction and Background	/5
Section 3: Electric Circuit Schematics (transistors only)	/10
Section 4: LTSPICE Simulation for Schematic	/10
Section 5: IRSIM for Schematic	/10
Section 6: Electric Layouts (landscape mode for the final version and others to show all layout details)	/20
Section 7: LTSPICE Simulation for Layouts	/10
Section 8: IRSIM simulations for Layout	/10
Section 9: Compare LTSPICE Measurements for Schematic and Layout (must provide comparisons between the two in table format) Provide some delays, rise and fall times.	/10
Section 10: Measurements of chip area and number of transistors for the layout	/5
Section 11: Pathwave Adanced Design System	/10
Section 12: Conclusions and References	Required
Late Penalty (-5 points per day with prior 24 hour email notice) Max. of 2 days for late submission. Submit on Blackboard. -10 points for no Electric schematic and layout files	
TOTAL	**/100**

Do not erase: *Penalty rules: A) -5pts per day for late submission. After two days (12/9), a score of zero will be given, but you are still required to complete the report. B) -2pts for any violations and delays submitted after 8PM.