

## EE 457: Digital Integrated Circuits

### Project #1 Report Cover Sheet

**Due: 9/30/2023 by 6PM**

**PROJECT TITLE: 2-Input CMOS Exclusive OR Gate**

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Your report should follow the following items in sequence. <i><u>Do not change the sequence.</u></i>	GRADE
Section 1: Executive Summary	/5
Section 2: Background and Approach (Include a truth table)	/5
Section 3: Electric Schematic	/15
Section 4: LTSPICE for Electric schematic	/10
Section 5: IRSIM for Electric schematic	/10
Section 6: Electric Layout	/25
Section 7: LTSPICE for Electric layout (compare with schematic)	/15
Section 8: IRSIM for Electric layout	/10
Section 9: Conclusions and References	/5
<b>TOTAL</b>	<b>/100</b>