EE 457: Digital Integrated Circuits

Project #1 Report Cover Sheet
Due: 9/30/2023 by 6PM

PROJECT TITLE: 2-Input CMOS Exclusive OR Gate

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Your report should follow the following items in sequence. *Do not change the sequence.*	GRADE
Section 1: Executive Summary	/5
Section 2: Background and Approach (Include a truth table)	/5
Section 3: Electric Schematic	/15
Section 4: LTSPICE for Electric schematic	/10
Section 5: IRSIM for Electric schematic	/10
Section 6: Electric Layout	/25
Section 7: LTSPICE for Electric layout (compare with schematic)	/15
Section 8: IRSIM for Electric layout	/10
Section 9: Conclusions and References	/5
TOTAL	**/100**

Contents

1 Executive Summary **1**

2 Background **1**

3 Approach **1**

4 Schematic in Electric **3**

5 Schematic Simulation **5**

1 Executive Summary

The goal of this project is to design an XOR gate CMOS integrated circuit using the design software Electric. The process of designing the chip involves starting with the boolean logic that makes up an XOR gate, turning that logic into a functioning schematic using CMOS logic, and then turning that schematic into a finished layout. Then, both the schematic and the layout are simulated in both LTSpice and IRSIM to confirm that they function properly, and finally measurements can be taken in LTSpice to further validate the design. Ultimately, this project is an introduction to the process of turning requirements into a finished design and then validating the design using the tools we have learned from creating the inverter.

2 Background

Designing an IC that performs the function of an XOR gate begins with an understanding of what an XOR gate does. The operation, denoted as $F = A \oplus B$ is a boolean logic function that takes inputs A and B and outputs a 0 if they are the same and 1 if they are dissimilar. This behavior can be seen in Table 1. The symbol for the XOR gate is shown in Figure 1. We can break down this logic into the following boolean expressions: $F = A \oplus B = A\overline{B} + \overline{A}B = (A + B)(\overline{A} + \overline{B})$

Input A	**Input B**	**Output F**
0	0	0
0	1	1
1	0	1
1	1	0

Table 1: Truth Table for the XOR gate.

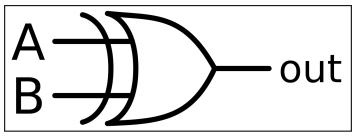

Figure 1: The symbol for the XOR gate.

3 Approach

I chose to start designing the CMOS logic using the function $F = A\overline{B} + \overline{A}B$. The first thing to do is to invert the function, since the output of a CMOS circuit is inverted. Therefore we must invert F and then implement that function in the pull down network. Using De Morgan's Law, we get: $\overline{F} = \overline{A\overline{B} + \overline{A}B} = \overline{A\overline{B}} \cdot \overline{\overline{A}B} = (\overline{A} + B)(A + \overline{B})$ Therefore $(\overline{A} + B)(A + \overline{B})$ will be implemented on the NMOS side. We do this by putting the transistors in parallel for OR and in series for AND. For the pull up network, we put the PMOS transistors in series for OR and in parallel for AND. I sketched out the resulting circuit, as shown in Figure 2.

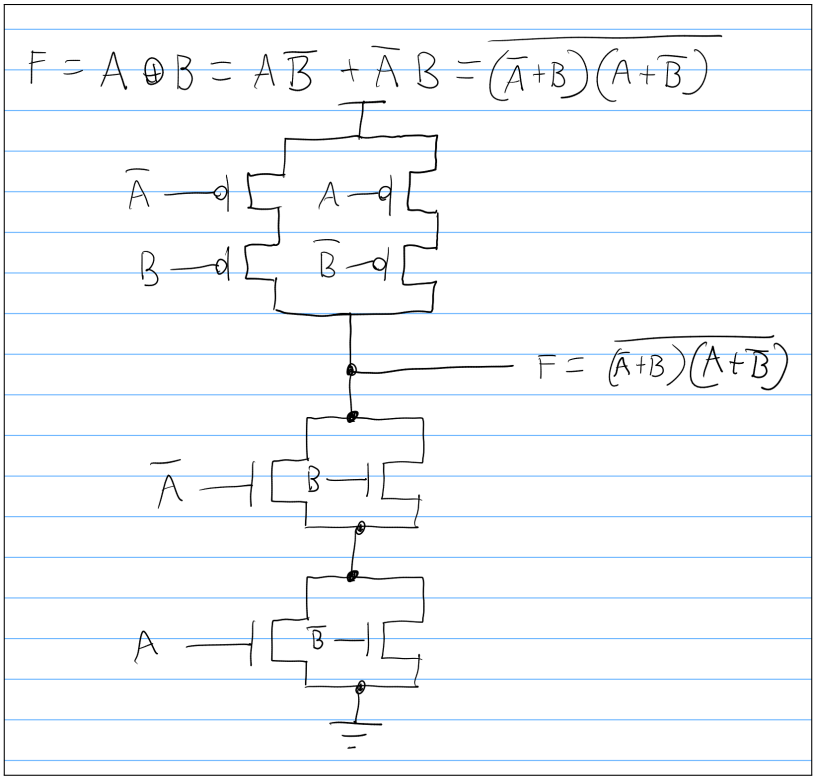

Figure 2: A sketch of the PUN and PDN for implementing the XOR gate.

Since we are only given A and B as inputs and not $\overline{A}$ and $\overline{B}$ as well, we have to invert A and B for the inputs where $\overline{A}$ and $\overline{B}$ are necessary. This requires two inverters at the inputs, as shown in the sketch in Figure 3.

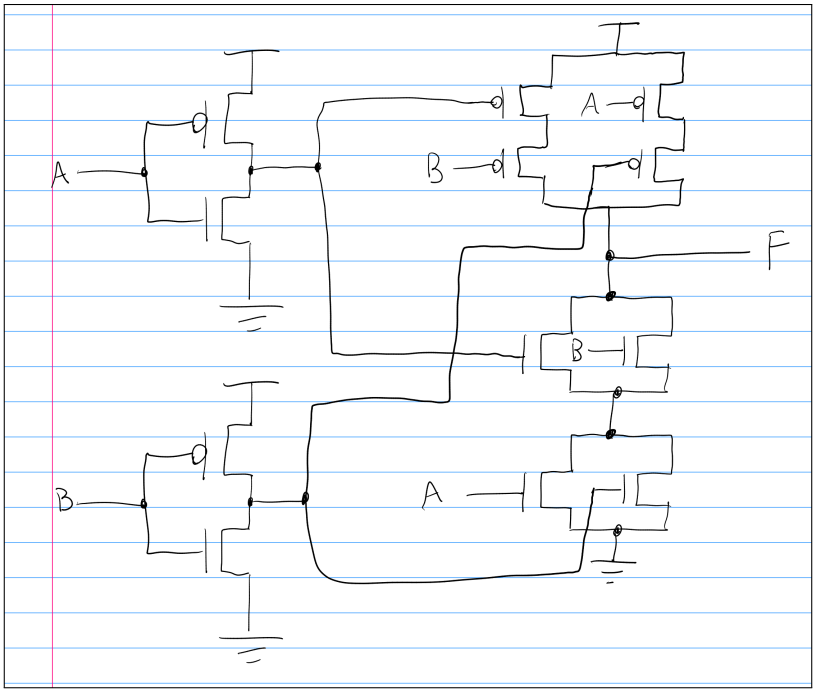

Figure 3: A sketch of the XOR gate in CMOS logic.

4 Schematic in Electric

The sketch of the circuit was then built in the schematic design portion of Electric. The final schematic can be seen in Figure 4. The various nets that feed into the PUN and PDN are labeled to make the schematic easier to read. The transistors were initially chosen to be 8λ wide and 2λ long for PMOS and 4λ wide and 2λ because those are the dimensions that worked best for the inverter that we designed previously. However, we were told to make the PMOS transistors and NMOS transistors the same size, so I made them all 8λ wide and 2λ.

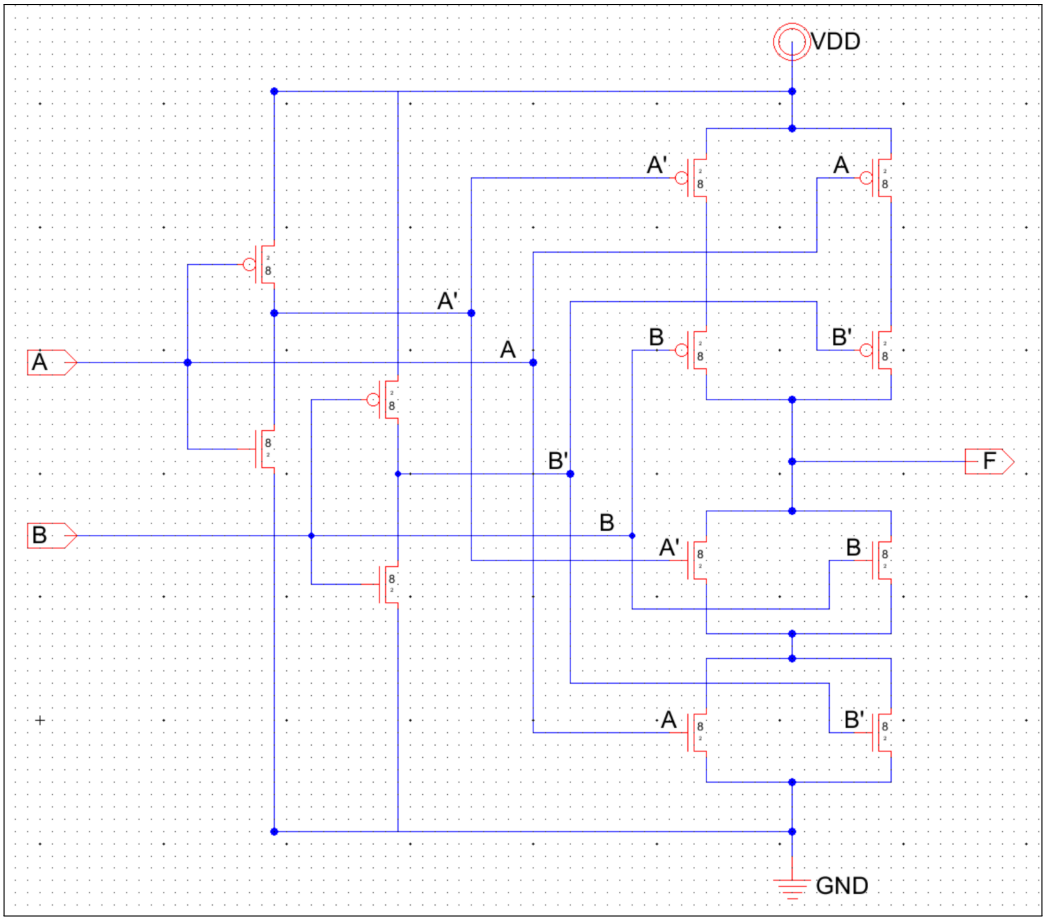

Figure 4: The finished schematic in Electric.

After designing the schematic in electric, it must pass the Design Rule Check (DRC) in order to be simulated properly. The DRC checks to make sure there are no major issues with the schematic. The results of the DRC are shown in Figure 5. The DRC has found no errors and the design can be simulated.

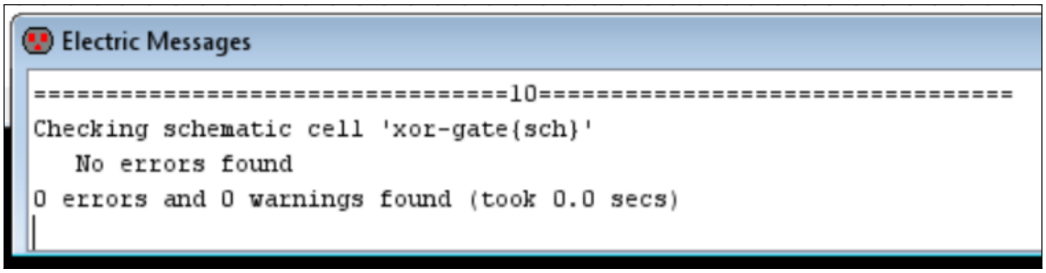

Figure 5: The DRC for the schematic shows no errors.

5 Schematic Simulation

The spice code for the simulation of the XOR gate schematic is shown in Figure 6. For this simulation, we are required to generate a 2MHz digital signal for input A and a 4MHz digital signal for input B. Both of these signals must have a rise time of 2ns and a fall time of 3ns. This is accomplished with the spice lines `VA A 0 PULSE(3.3 0 0 2n 3n 250n 500n)` for input A and `VB B 0 PULSE(3.3 0 0 2n 3n 125n 250n)` for B. The resulting output signal from these two pulsed input signals can be seen on net F in the simulation graphs.

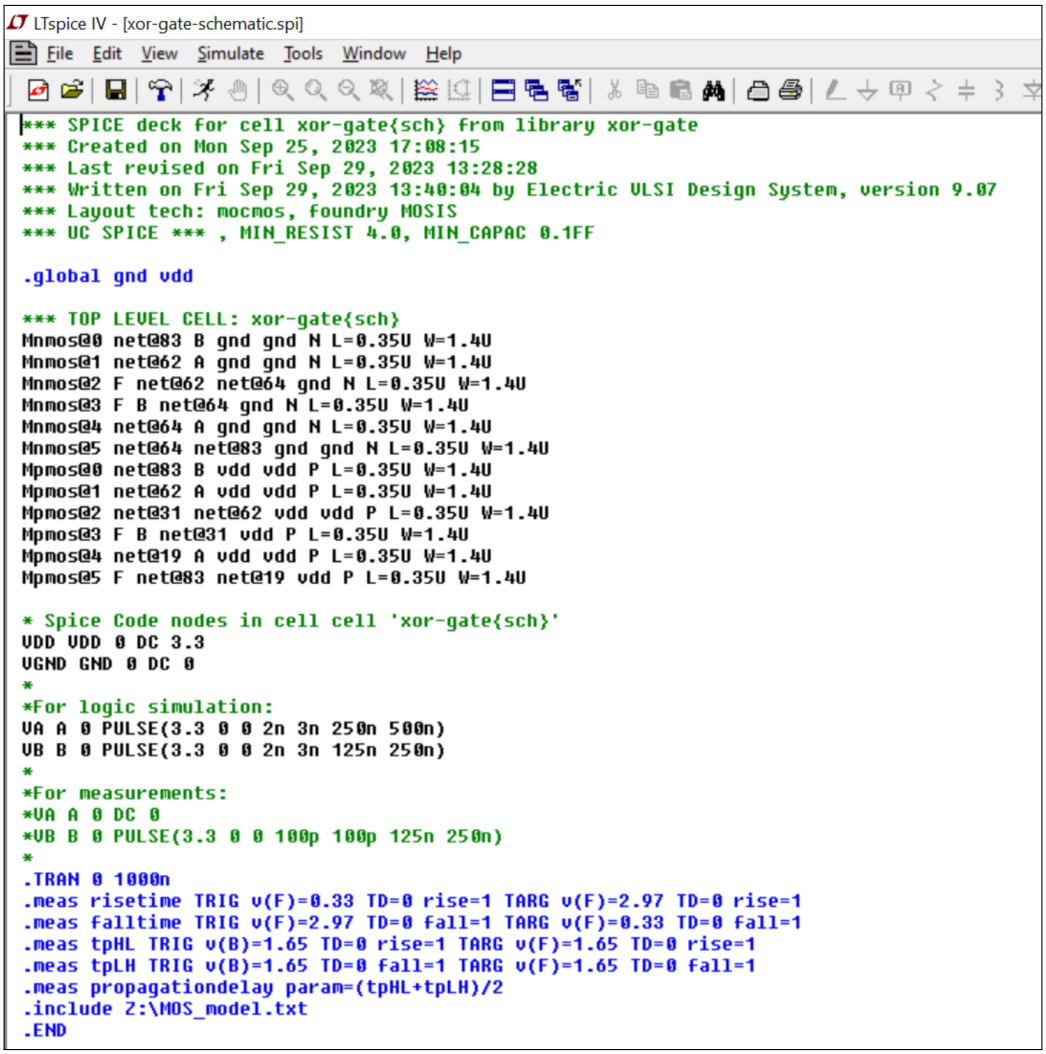

Figure 6: The spice code for simulating the schematic of the XOR gate.

The graphs for the spice simulation of the XOR gate schematic are shown in Figure 7. This simulation shows that the schematic is functioning properly since it behaves exactly as we expect an XOR gate to behave. Compare Figure 7 to Table 1 to see that the functionality is identical.

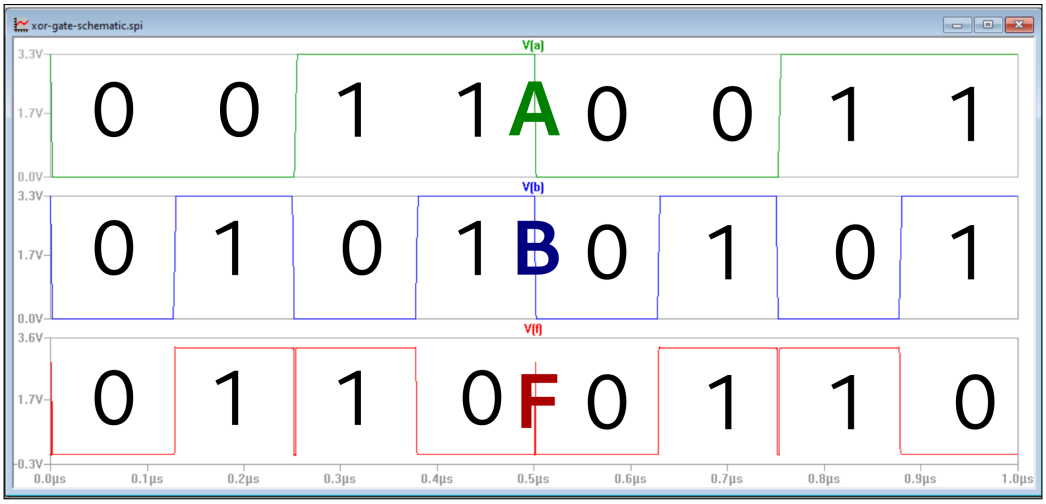

Figure 7: The resulting graphs from the spice simulation of the XOR gate schematic.

IRSIM is different to spice in that its simulation is purely digital. We can use IRSIM to confirm that the behavior of our XOR gate is correct from a purely digital standpoint. IRSIM does not accurately simulate timing like spice does, but is simply another way to validate our design. The rising and falling edges of the inputs must be set manually, and the output at F is automatically shown with each change to the inputs by the user. The resulting graph from the IRSIM simulation of the XOR gate schematic is shown in Figure 8. This simulation shows the correct results that match Figure 7 and Table 1.

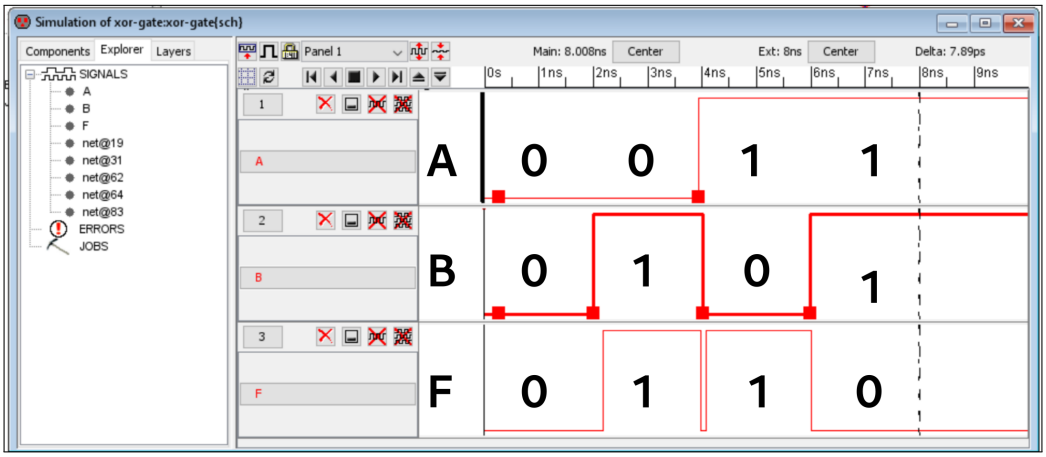

Figure 8: The resulting graphs from the IRSIM simulation of the XOR gate schematic.

6 Schematic Measurements

We are interested in a number of measurements that give us some indication about the performance of our design. The first measurement we are concerned with is the Rise Time of the output signal. The Rise Time of a signal is the amount of time it takes for the signal to go from 10% of VDD to 90% of VDD on a rising edge. A rise time that is too slow can cause issues with the propogation of

the signal through a system. Similarly, the Fall Time is the time it takes for a signal to go from 90% of VDD to 10% of VDD on the falling edge. It is also important that the fall time be fast enough.