EE457: Digital IC Design

Project 3 Report Cover Sheet

Due 12/07/2023

PROJECT TITLE: CMOS 4-bit shift register

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Topics **(Do Not change order of sections)**	GRADES
Section1: Executive Summary (1/2 page)	Required
Section 2: Introduction and Background	/5
Section 3: Electric Circuit Schematics (transistors only)	/10
Section 4: LTSPICE Simulation for Schematic	/10
Section 5: IRSIM for Schematic	/10
Section 6: Electric Layouts (landscape mode for the final version and others to show all layout details)	/20
Section 7: LTSPICE Simulation for Layouts	/10
Section 8: IRSIM simulations for Layout	/10
Section 9: Compare LTSPICE Measurements for Schematic and Layout (must provide comparisons between the two in table format) Provide some delays, rise and fall times.	/10
Section 10: Measurements of chip area and number of transistors for the layout	/5
Section 11: Pathwave Adanced Design System	/10
Section 12: Conclusions and References	Required
Late Penalty (-5 points per day with prior 24 hour email notice) Max. of 2 days for late submission. Submit on Blackboard. -10 points for no Electric schematic and layout files	
TOTAL	**/100**

Do not erase: *Penalty rules: A) -5pts per day for late submission. After two days (12/9), a score of zero will be given, but you are still required to complete the report. B) -2pts for any violations and delays submitted after 8PM.

Contents

1 Executive Summary

The goal of this project was to build a 4-bit shift register in Electric. A shift register is a digital device which can shift bits across a number of outputs. In our case, there are 4 outputs, Q0 through Q3. Every clock cycle, the value of the bit stored at Q2 is shifted to Q3, the value of Q1 is shifted to Q2, Q0 is shifted to Q1, and the state of input D is stored in Q0. This is a very useful circuit for a number of applications, as we can control four outputs with only two inputs: A clock pin and a data pin. Moreover, multiple shift registers can be chained together to create a larger shift register with more outputs. For example, I once worked on a project in which 8-bit shift registers were chained together to control 64 LEDs with just two pins on a microcontroller.

For this project, the shift register shifts data on the positive clock edge. This is done by making the shift register out of four postive edge-triggered D flip-flops, each flip-flop representing one bit. The shift register also has a reset pin, which is active low. When the reset pin is pulled low, all four outputs are reset to logic low.

The project involves designing the shift register as both a schematic and a layout in Electric. Both the schematic and layout are simulated in LTspice and IRSIM to confirm that the shift register design works properly. Measurements are also taken using LTspice to determine the rise times, fall times, propagation delay, and power draw of the designs. For this project specifically, the layout is simulated with parasitic resistances and capacitances. This makes the simulation much more realistic, since more of the physical properties of the design are taken into account.

2 Introduction and Background

The design for the shift register consists of a couple of layers of designs. In order to build the shift register, we must first build a positive-edge-triggered master slave D flip-flop, and in order to build the flip-flop, we must first build a 2-input NAND gate and a 3-input NAND gate. The design for the positive-edge-triggered master-slave D flip-flop is shown in Figure 1. The design consists of two 2-input NAND gates and four 3-input NAND gates. The flip-flop has inputs for the clock signal, data signal, and reset line. It outputs Q and Q prime, however we will only be using Q for the shift register. The flip-flop works like a set of latches; while the clock is low, the "master" latch is set and the "slave" latch is held, and while the clock is high, the "master" latch is held while the "slave" latch is set. Because of this setup, the output of the flip-flop only changes to reflect the input on the positive clock edge.

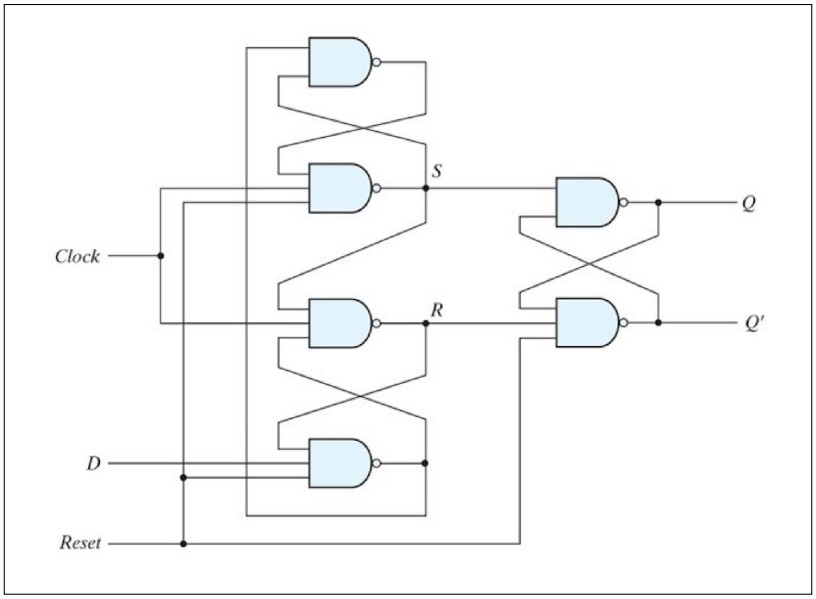

Figure 1: The design for the positive-edge-triggered master-slave flip-flop.

Now that we understand how the flip-flop works, we can understand how the shift register works. As shown in Figure 2, the 4-bit shift register is simply four positive-edge-triggered master-slave D flip-flops chained together. All of the reset pins of the flip-flops are connected together to create the reset line for the shift register. This reset line will reset all outputs to low when it is pulled low. The clock inputs are also tied together so that all of the flip-flops are triggered simultaneously at the positive clock-edge. The D input of the shift register is connected to the D input of the first flip-flop, and then the D input of each successive flip-flop is connected to the output of the previous flip-flop. This way, the data is shifted from left to right each positive clock edge.

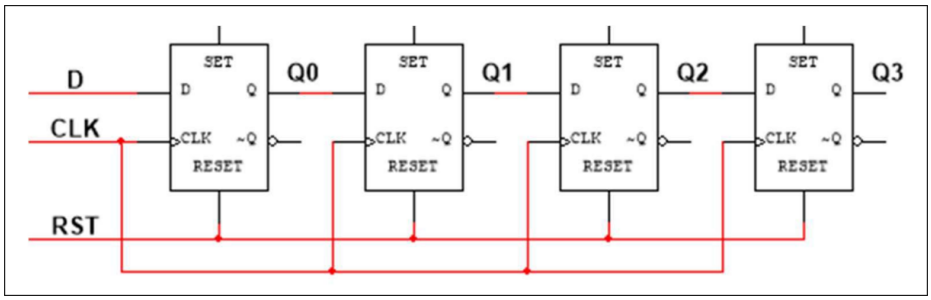

Figure 2: The design for the 4-bit shift register consisting of four positive-edge-triggered master-slave D flip-flops.

To give an example of how the shift register works, let us consider the following scenario. First, we pulse the reset pin low temporarily and then keep it high again. Now all outputs Q0, Q1, Q2, and Q3 are low. We will set D high for the first positive-edge of the clock. After the positive-edge of the clock pulse, Q0 is now high. After another positive-edge of the clock, the 1 stored at Q0 is shifted to Q1. Then after another positive clock edge, Q2 is high. Next positive clock edge, Q3 is high. And then after another positive clock edge, the signal from D going low again has been shifted through the whole shift register and all of the outputs are low again. This example demonstrates

how the high pulse on D "shifts" through the shift register, making the jump every positive clock edge.

3 Electric Circuit Schematics

The basic building blocks for the shift register, as discussed in the previous section, are the 2-input and 3-input NAND gates. The schematic for the 2-input NAND gate is shown in Figure 3. It is a very simple static CMOS design with two PMOS transistors in parallel and two NMOS transistors in series to create the NAND logic. The schematic for the 3-input NAND gate is shown in Figure 4. The design is the same as for the 2-input NAND gate, except that there are three NMOS transistors and three PMOS transistors to support three inputs.

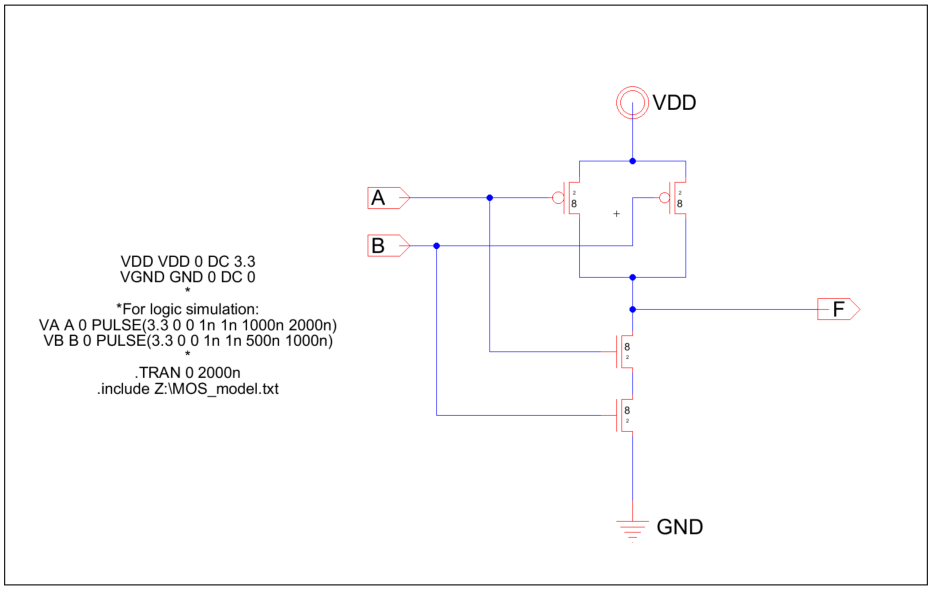

Figure 3: The schematic for the 2-input NAND gates, one component of the D flip-flops that make up the shift register.

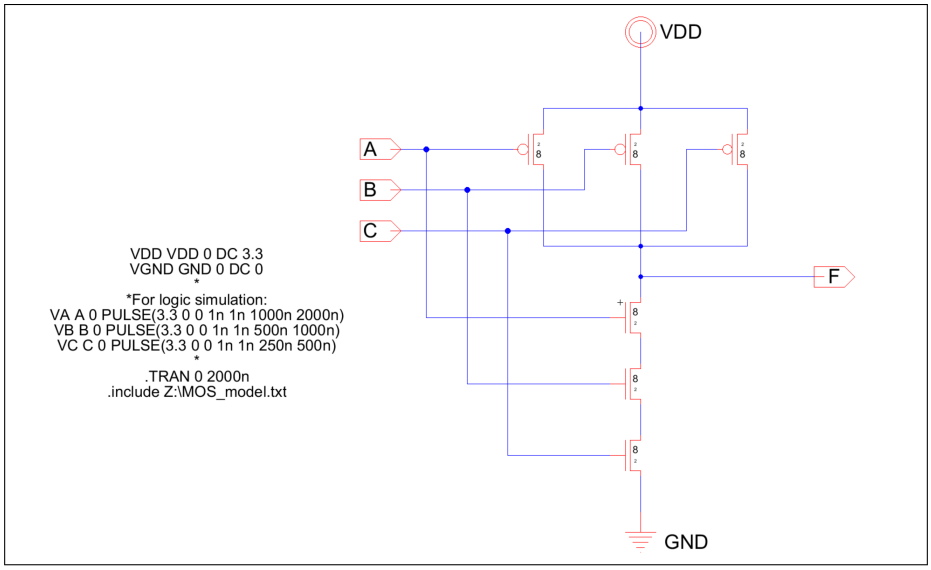

Figure 4: The schematic for the 3-input NAND gates, one component of the D flip-flops that make up the shift register.

Two 2-input NAND gates and four 3-input NAND gates are combined in the configuration shown in Figure 1 to create the schematic for the positive-edge-triggered master-slave D flip-flop that the shift register is based on. The schematic for the flip-flop is shown in Figure 5. The NAND gates can be4 clearly seen in the design. As described previously, the flip-flop design has inputs for the clock signal, data signal, and reset line and has outputs Q and Q prime. Crucially, the flip-flop is positive-edge-triggered due to the master-slave design that acts like two latches chained together.

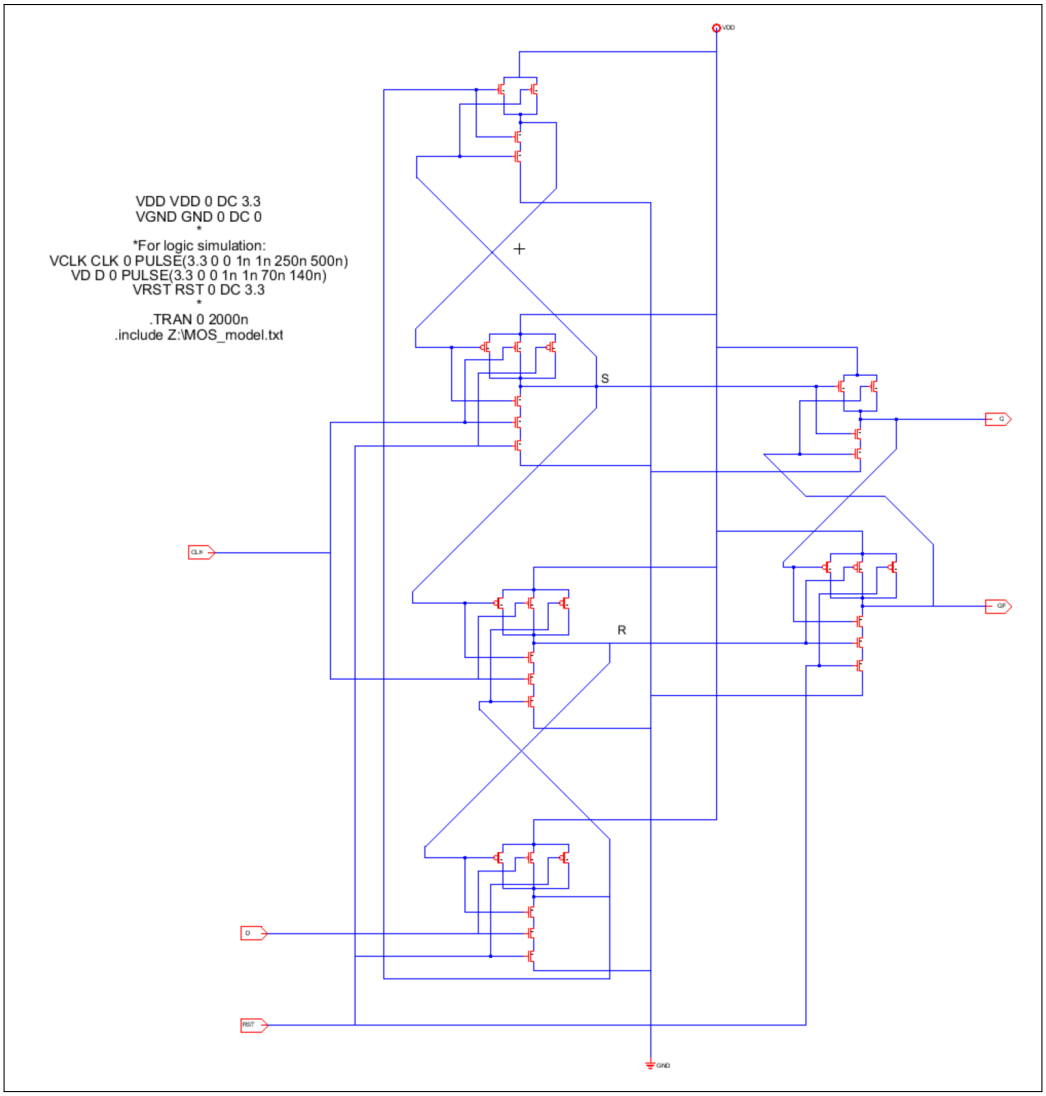

Figure 5: The schematic for the postive-edge-triggered master-slave D flip-flop.

4 References

[1] EE 457 Lectures 1, 2, 3, and 4h
[2] https://cmosedu.com/videos/electric/tutorial3/electric_tutorial_3.htm
[3] https://cmosedu.com/videos/electric/tutorial4/electric_tutorial_4.htm
[4] https://en.wikipedia.org/wiki/Multiplexer
[5] https://vlsiuniverse.blogspot.com/search/label/8%3A1%20mux
[6] https://cmosedu.com/videos/electric/tutorial5/electric_tutorial_5.htm