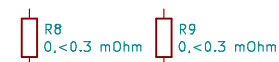


Pin configuration diagram for the 10B\_SAR ADC. The chip is shown with pins 1 through 33. Pin 1 is VDD, Pin 2 is VREF, Pin 3 is VIN+, Pin 4 is VIN-, Pin 5 is VREF, Pin 6 is VREF, Pin 7 is VREF, Pin 8 is VDD, Pin 9 is AVSS2, Pin 10 is VDDPST1, Pin 11 is VDD, Pin 12 is VDD, Pin 13 is RST, Pin 14 is D9, Pin 15 is D8, Pin 16 is VDDPST1, Pin 17 is D7, Pin 18 is D6, Pin 19 is D5, Pin 20 is D4, Pin 21 is D3, Pin 22 is D2, Pin 23 is D1, Pin 24 is D0, Pin 25 is VDDPST1, Pin 26 is CLK\_C, Pin 27 is CLK\_S, Pin 28 is CLK, Pin 29 is VREF, Pin 30 is VDD, Pin 31 is VDD, Pin 32 is AVSS1, Pin 33 is CLK\_FILT. A separate VREFM pin is shown with a 0.3 mOhm resistor connected to GND. The chip is labeled 10B\_SAR.

### CLK TERMINATIONS

The diagram illustrates the termination for two clock signals, CLK- and CLK+. Each signal line is terminated with a series resistor (R3 for CLK-, R5 for CLK+) and a shunt network consisting of a resistor (R2 for CLK-, R4 for CLK+) and an inductor (L1 for CLK-, L2 for CLK+) connected to ground. The component values are: R3 = 26.1, R2 = 49.9, L1 = 1 nH, R5 = 10, R4 = 49.9, and L2 = 2.2 nH.



Conn\_02x10\_Top\_Bottom

-  H1 MountingHole
-  H2 MountingHole
-  H3 MountingHole
-  H4 MountingHole