10-bit SAR ADC

Final Presentation - April 30, 2020

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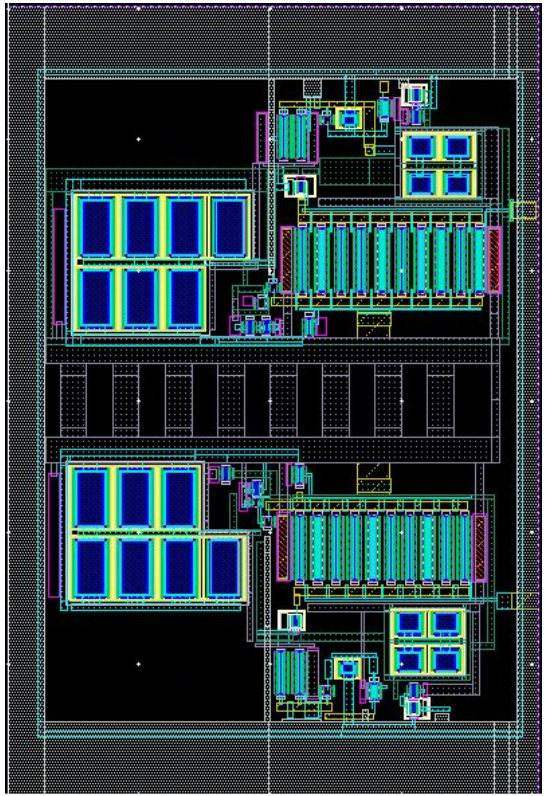
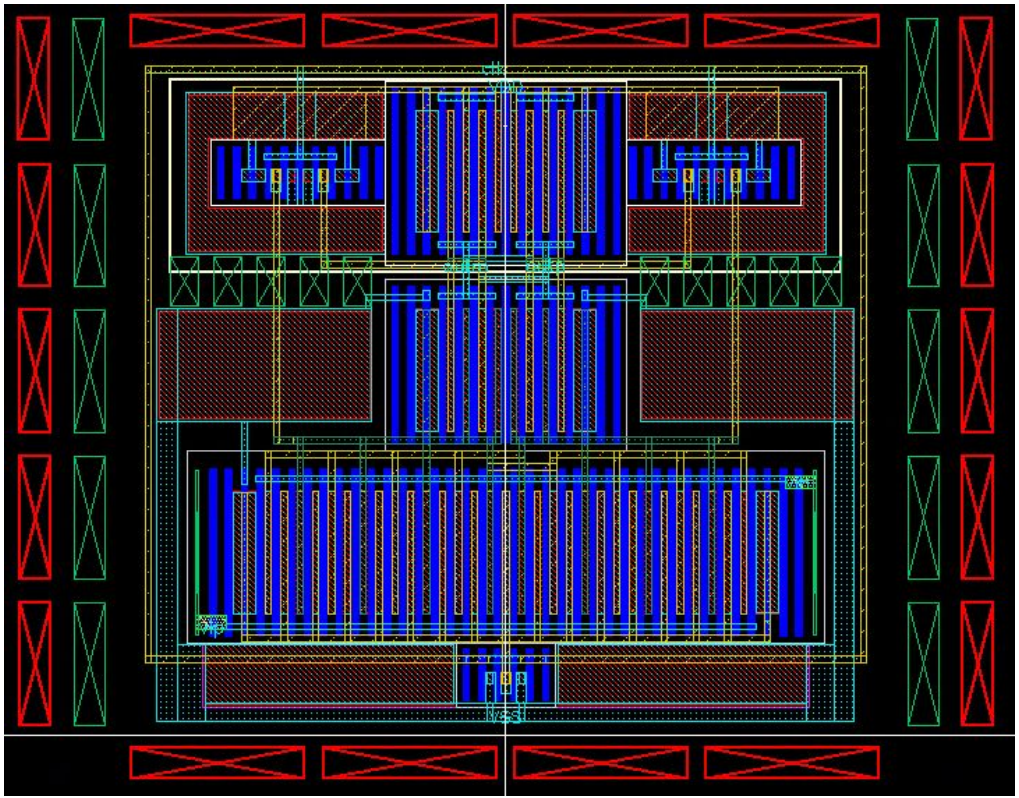
T/H Layout Issues



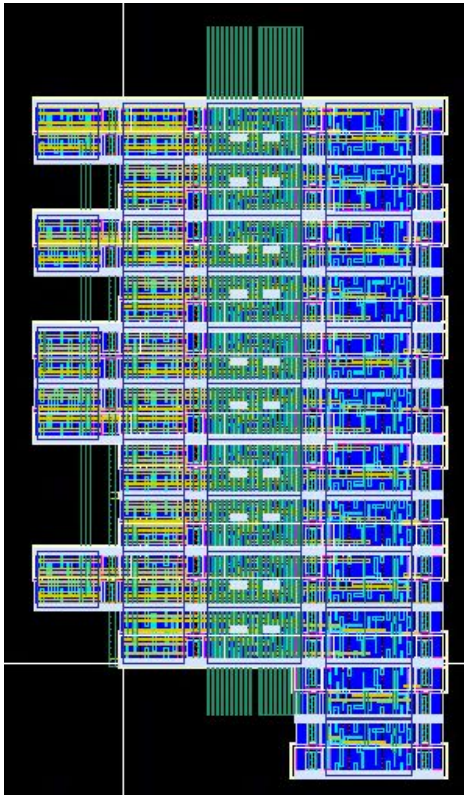
- "Generate connectivity"
- Autogenerated vias from PO to M1
- Angle brackets for LVS (and "Generate")
- PSUB2 "error"

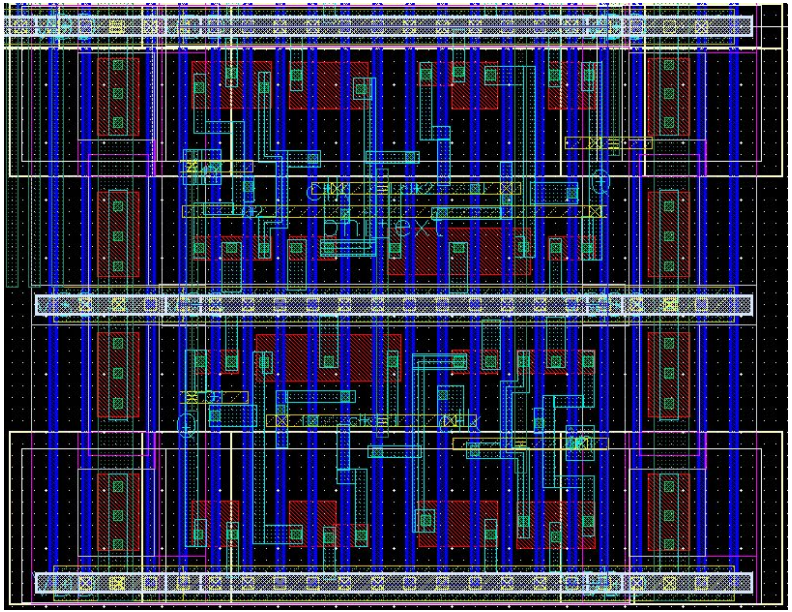
Comparator Layout Issues



- Symmetry
- Dummy devices
- Inter-digitated gates

Logic Cell Layout





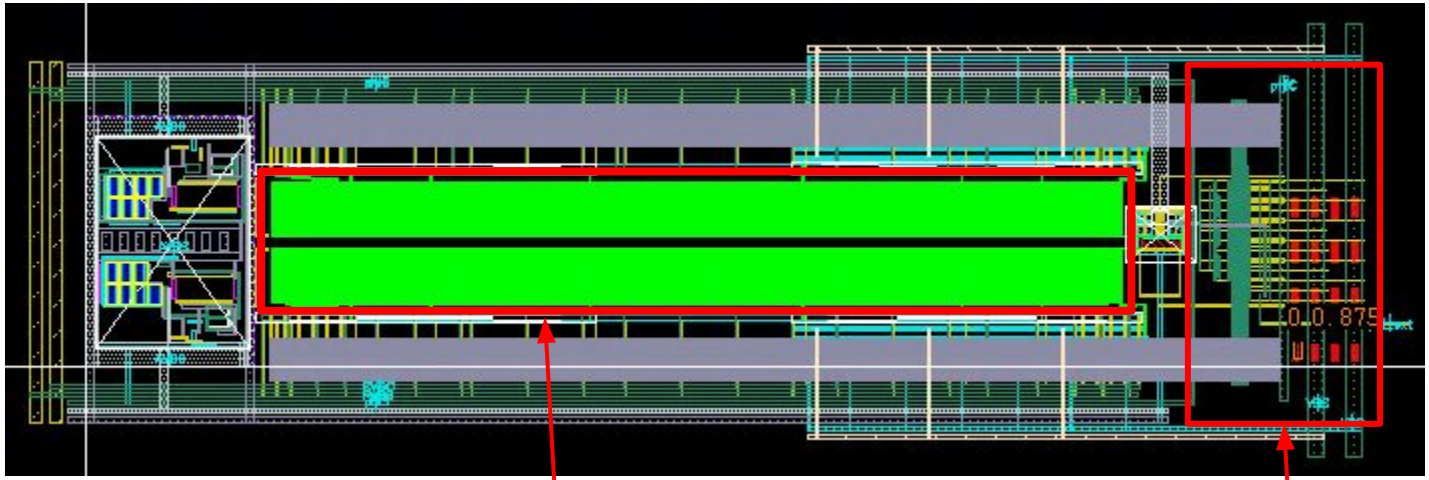
Std cell C/P

Layer1 dr2: Gates (Poly spacing)

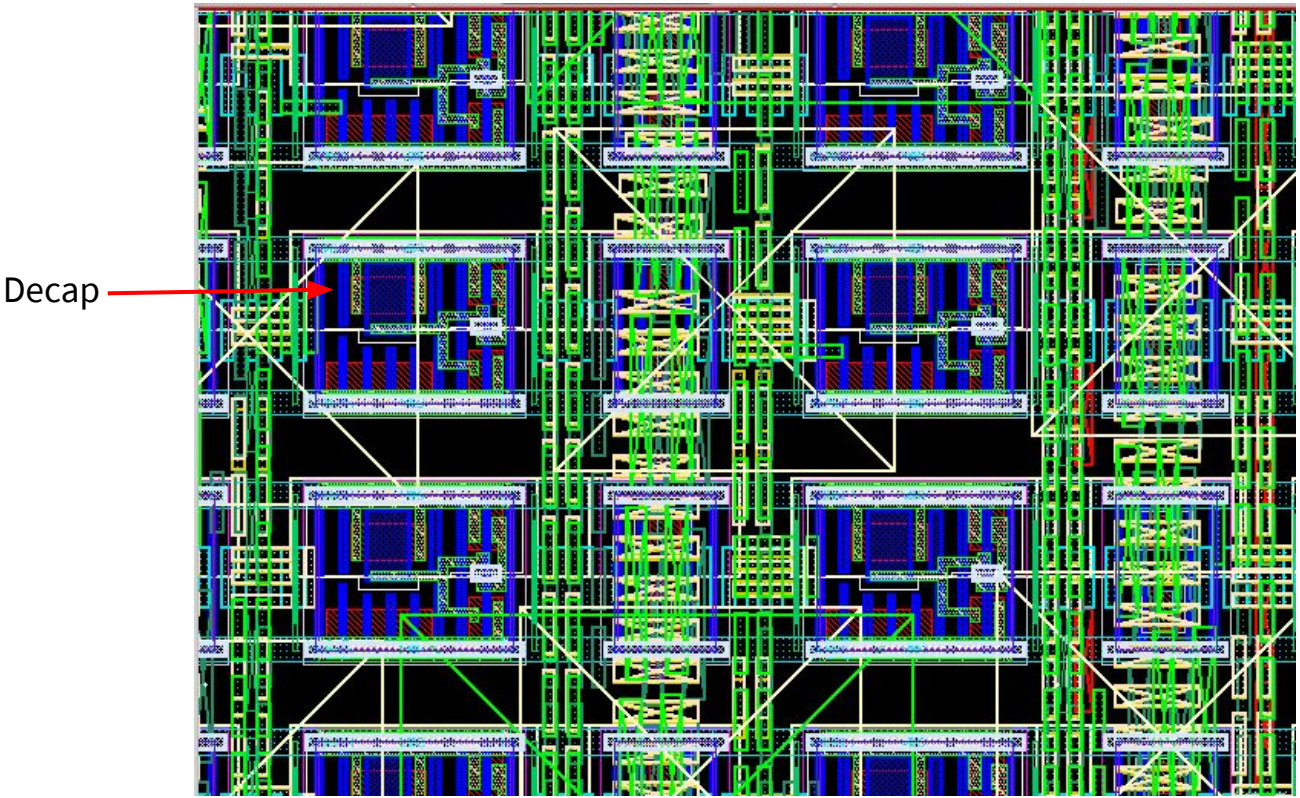
Schematic ambiguity and layout "shortcuts"
Schematic: logic - FFs/latches
Layout: logic - pairs - FFs/latches

Labeling: naming the nets does not work

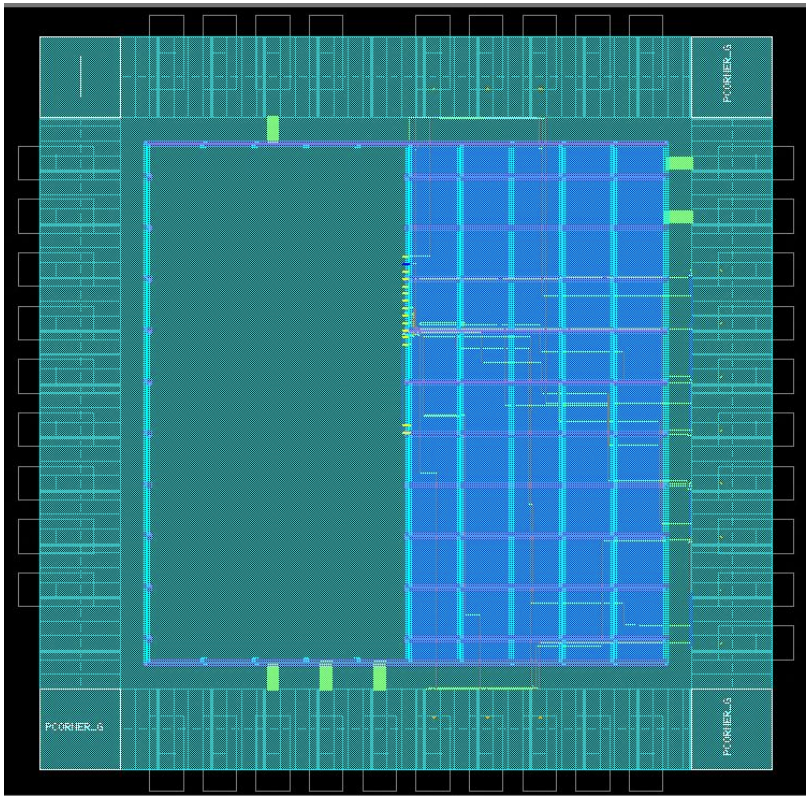
Density Violations



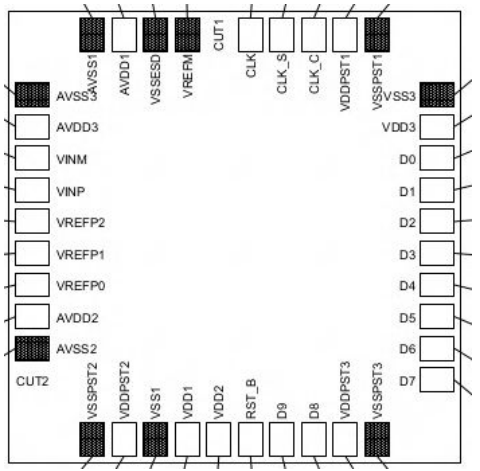
Density Violations



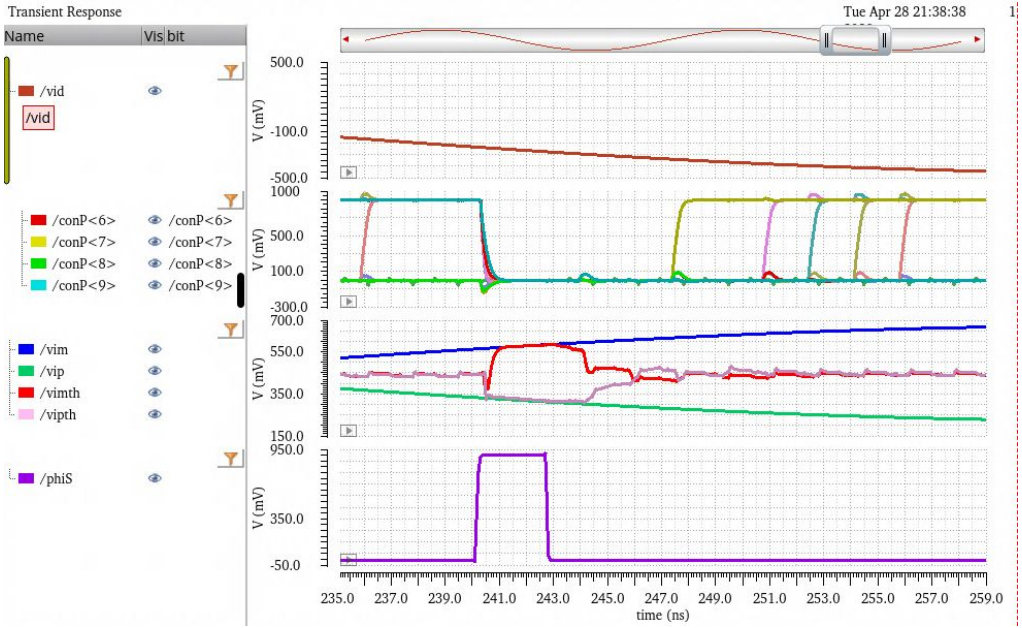
Digital Cell Synthesis and P&R Issues



- Missing bond pad
- Padring appnote recommendations
  - Clamp cells
  - Impact on size
  - VSS pads near corner cells
  - 3 VDD pads
  - Analog IO Filler and Analog Corners needed

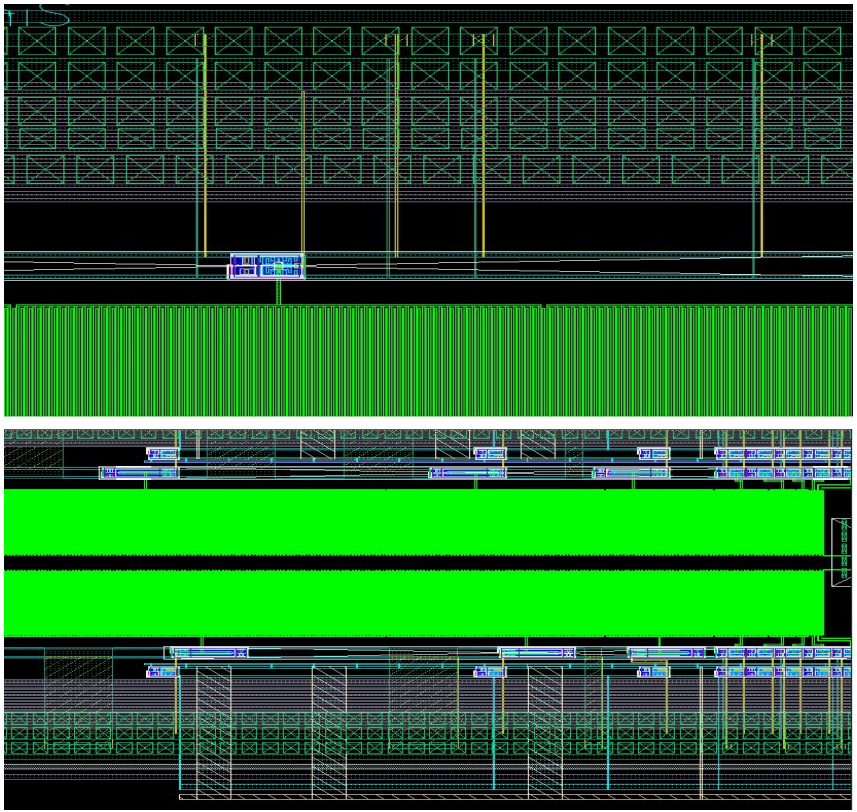


Post-Layout Simulation Results

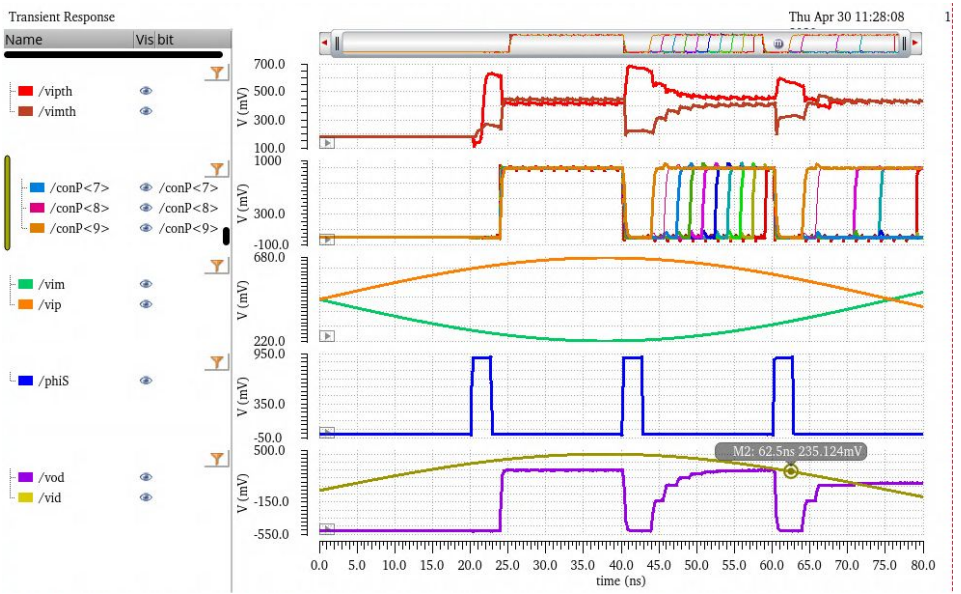


Time	Sampled Differential Voltage	ADC Output Code	Vref	Converted ADC Output
240ns	-250 mV	0010111100	450 mV	-284 mV

Post-Layout Simulation Takeaways



- Focus on impacts of parasitics
- Increase the size of DAC switches
- Improve power routing
- Do as much verification as possible



Final output code: 1100101001 (261 mV if Vfs = 900 mV, adjusted Vfs = 868 mV)