A Double-balanced Down-conversion Mixer in 65-nm CMOS for 2.4-GHz applications

Dylan Rosser
Dept. of Electrical and Computer Engineering
Carnegie Mellon University
Pittsburgh, PA
drosser@andrew.cmu.edu

Abstract-The design of a 2.4-GHz double-balanced down-conversion active mixer is presented. The mixer's functionality is verified in simulations, and the resulting performance is reported. The mixer topology is a Gilbert cell with a resistive load. The mixer consumes 9.2mW while providing a conversion gain of 9.8dB at an intermediate frequency (IF) of 80MHz.

INTRODUCTION

Mixers are essential building blocks of radio frequency communications circuits, as demonstrated by the typical superheterodyne receiver front-end shown in figure I. Mixers perform frequency translation by multiplying two signals [1]. A down-conversion mixer translates a high frequency input to a lower frequency output by means of a local oscillator. The three typical ports on a down-conversion mixer are the input, or RF port, the local oscillator (LO) port, and the intermediate frequency (IF) output port. In a down-conversion mixer, the IF signal can be viewed as multiplication of the RF signal with a square wave toggling between 0 and 1. Defining f_{RF} as the frequency of the RF signal, and f_{LO} as the frequency of the local oscillator, the intermediate frequency is given by

$$f_{IF} = f_{RF} - f_{LO} \quad (1)$$

Design of down-conversion mixers provide a direct tradeoff between linearity and noise. In the receive path, both the mixer's noise and IP3 are divided by the gain of the preceding low noise amplifier (LNA). Operating with low supply voltages

	Target Specifications	This Design
Power (mW)	< 10	9.177
IIP3 (dBm)	> -5	-2.008
DSB NF (dB)	< 8	5.796
Gain (dB)	> 6	9.832
Port Isolation (dB)	<-50	< -180

TABLE I. TARGET SPECIFICATIONS AND SIMULATION RESULTS

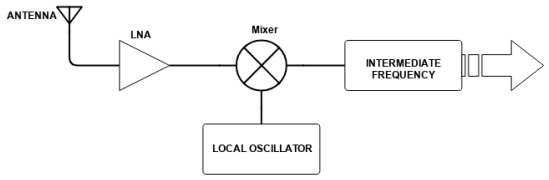

Figure 1. Typical superheterodyne receiver front-end

makes the presented mixer compatible with submicron CMOS technologies, but decreases the maximum achievable gain. This work demonstrates a mixer with modest performance in each of these areas.

In this paper, we study the design methodology of a well understood and common mixer architecture, and simulate its performance in a 65nm process as an academic exercise. All simulation results exceed target specifications and are reported in table I.

MIXER ARCHITECTURE

The architecture of the mixer presented in this paper is known by RF circuit designers as the Gilbert cell. It's operation is initially described in [2]. The CMOS implementation in this design is shown in figure II. Transistors Q1 & Q2 provide transconductance, converting the RF voltage into current. Transistors Q3-Q6 are referred to as the switching quad. These transistors are used to steer the current to each load based on the phase of the LO waveform that controls them. Coupling capacitors are used to connect the RF and LO voltages to the gates of the MOSFETs, and a shunt capacitor at the output node is used to filter out high frequencies. Transistors Q7 and Q8 are connected in the diode configuration to generate bias voltages for the other transistors. The reference current source M1 is set to 40μA.

The LO waveforms supplied to the mixer are an ideal sinusoid that has been buffered through the circuit shown in figure 2. Inclusion of the buffer in simulation was to model the effect of the buffer's noise on the circuit's noise figure (NF). In the buffer

circuit, transistor Q3 acts as current source to set the bias condition. Q1 and Q2 are a common source difference amplifier.

DESIGN

The design process followed is outlined in [1]. For this project, a total power budget of 10mW was allocated. The mixer consumes 7.2mW while the buffer consumes 2mW. In each leg of the mixer, the load resistance was sized so as to provide the maximum voltage conversion gain while keeping all transistors in saturation.

(2) $$R_{D,max} = \frac{2V_{R,max}}{I_D}$$

Because this mixer uses a double-balanced topology, the load resistance was halved to accommodate the required headroom for this amplification. The derivation for $V_{R,max}$ in the above equation can be in [1]. This voltage is sized to accommodate the overdrive of the transconductance transistors (Q1 or Q2) plus 1.7 times the equilibrium overdrive of the switching quad transistors. The voltage conversion gain of this circuit is then given by

(3) $$Av = \frac{2}{\pi} g_{m1} R_D$$

Due to the time varying and non-linear operation of this circuit, a robust noise analysis would require time consuming transient noise simulations. For the sake of simplicity, the input referred noise is approximated as

(4) $$\overline{V_{n,in}} = \pi^2 kT \left[\frac{\gamma}{g_{m1}} + \frac{2}{g_{m1}^2 R_D}\right]$$

The equation quickly shows the designer that noise can be reduced by increasing the transconductance of Q1 and Q2. For a fixed current, the transconductance can be increased by increasing the width of the device.

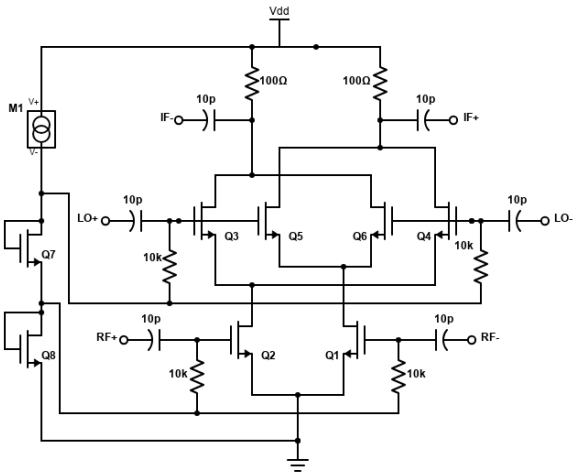

Figure 2. Mixer circuit with biasing shown

Component	Width (um)	Length (um)	Fingers
Q1	2	0.12	30
Q2	2	0.12	30
Q3	1	0.06	30
Q4	1	0.06	30
Q5	1	0.06	30
Q6	1	0.06	30
Q7	1	0.06	1
Q8	2	0.48	1

TABLE II. MIXER COMPONENT SIZES

Component	Width (um)	Length (um)	Fingers
Q1	1	0.06	10
Q2	1	0.06	10
Q3	2	0.24	20
Q4	2	0.48	1
Q5	1	0.06	1

TABLE III. BUFFER COMPONENT SIZES

Component	Width (um)	Length (um)	Value	Quantity
C	70	70	10pF	8
L	592	576	10nH	1
RL	2	13.6	100Ω	2
R	2	25	10kΩ	6

TABLE IV. PASSIVE COMPONENT SIZES

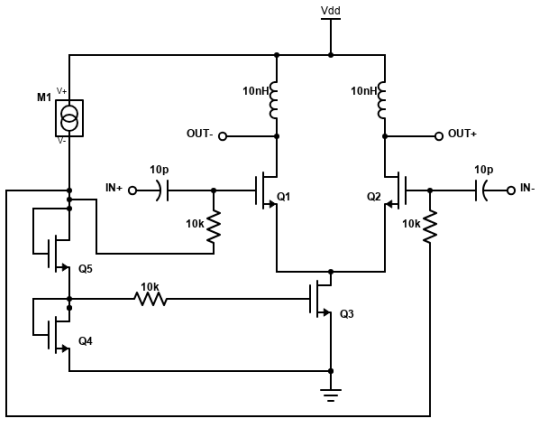

Figure 3. Buffer circuit with biasing shown

SIMULATION & RESULTS

The circuit was built in Cadence virtuoso using a 65nm PDK. The sizes of all devices in the mixer are reported in table 2, while the sizes of the buffer devices are reported in table 3. The pre-layout circuit has a total area of 0.38 mm^2. The circuit was simulated using SpectreRF using the hb, hbac, hbxf, hbnoise, and dc analyses.

The simulation results show the mixer exceeding all specifications. The double side band (DSB) noise figure at 80MHz is 5.79dB as shown in figure 3. The third order interaction point as measured by the simulation results is -2dB, while the conversion gain is 9.8dB. The figure of merit for this design is a function of the input referred third intercept level, the doble side band noise figure, and the power consumed by the circuit, and has been calculated to be -16.98.

(5) $$FOM = IIP3 - dsbNF - Power$$

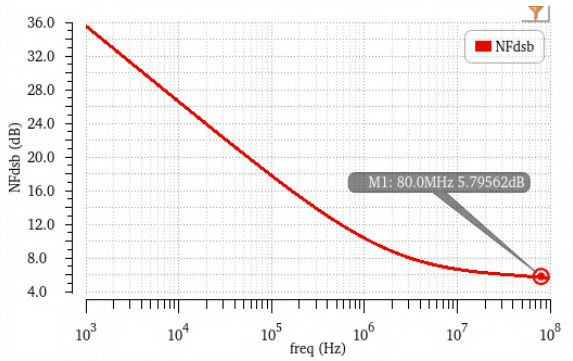

Figure 4. Double side band noise figure

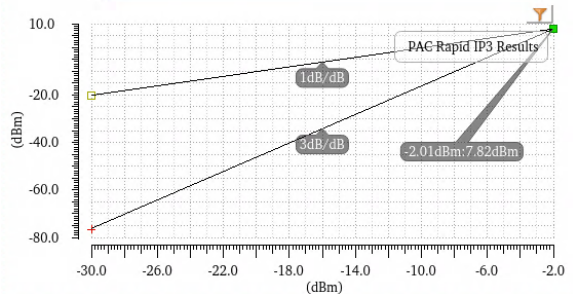

Figure 5. Input referred third intercept point

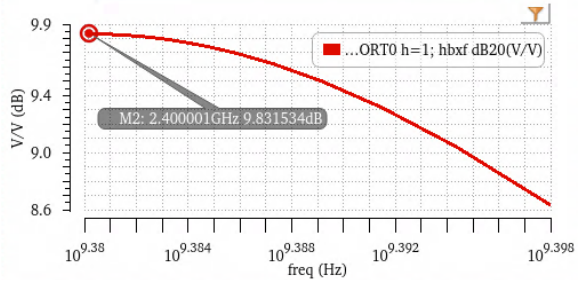

Figure 6. Voltage conversion gain

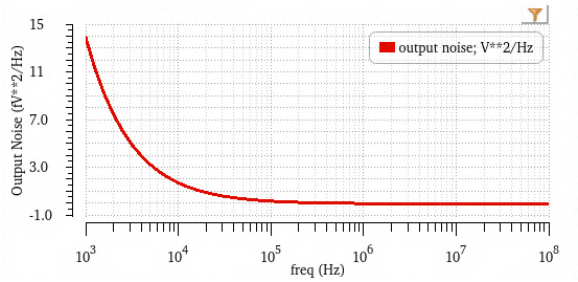

Figure 7. Output noise spectrum

REFERENCES

[1] B. Razavi, "RF Microelectronics", Prentice Hall. 2012

[2] B. Gilbert, "A precision four-quadrant multiplier with subnanosecond response", IEEE J. Solid State Circuits, vol. 3, issue 4, Dec. 1986