A 2.4-GHz Differential Colpitts VCO in 65-nm CMOS

Dylan Rosser
Dept. of Electrical and Computer Engineering
Carnegie Mellon University
Pittsburgh, PA
drosser@andrew.cmu.edu

Abstract – This paper presents the design of a voltage controlled oscillator (VCO) suitable for applications in the 2.4GHz ISM band. The topology is a differential Colpitts oscillator, as first described in [1]. The circuit is realized using a switched capacitor bank for course tuning, while varactors are used for fine tuning. The phase noise is less than -115dBc and -130dBc, measured at offset frequencies of 1MHz, and 3MHz, respectively. The VCO achieves an 18% tuning range and uses 6mW with a 1.2V supply.

INTRODUCTION

VCOs play an important role in the design of phase locked loops. High quality oscillations with low phase noise are a challenging part of the design. To complicate matters, phase noise performance trades-off with power and tuning range. Thus, the design of a VCO low phase noise over a wide tuning range proves difficult. This problem can be overcome with the right topology, and careful selection of the tank components. The tank inductor was chosen to have a near minimum value with a high quality-factor to minimize phase noise while providing enough parallel resistance to meet the startup criteria. The differential Colpitts topology was chosen due to its high output voltage swing and energy transfer efficiency. Furthermore, the MOSFET channel noise is at a maximum when the oscillator is least sensitive to perturbations [1]. Lastly, the differential Colpitts oscillator was designed using PMOS transistors because of their lower 1/f noise compared to their NMOS counterparts.

TUNABILITY

The VCO presented is tuned in two ways. First, it is tuned by a series of switched capacitors for course frequency selection. The design uses 10 unit-capacitors on each side to provide the tuning range desired in the specifications. The capacitors are switched into the tank by NMOS transistors. As more capacitors were added to the design to extend the tuning range, the size of the MOS switches needed to be increased as their on-resistance degraded the phase noise performance. Tuning beyond this point is likely possible with additional unit capacitors, but phase noise performance will probably be sacrificed. Fine tuning was achieved by a NMOS varactor. The width and length of the device was increased, and its gate was biased to VDD/2 to provide a large range of capacitance and larger KVCO. The circuit is capable of being tuned from 2.05GHz to 2.516GHz, putting the center frequency at 2.283GHz.

	Target Specifications	**This Design**
Power (mW)	< 10	5.742
Tuning Range	10%	20%
KVCO	<100MHz/V	66MHz/V
Phase Noise @ 1MHz	< 115 dBc/Hz	< 115 dBc/Hz
Phase Noise @ 3MHz	< 130 dBc/Hz	< 130 dBc/Hz
Min Freq (GHz)	NA	2.05
Max Freq (GHz)	NA	2.516

TABLE I. SPECIFICATIONS FOR THIS DESIGN

SPECIFICATION SUMMARY

As shown in table 1, the VCO meets the specifications for this project. The center frequency of the achieved tuning range is 2.83GHz. Using this center frequency, a tuning range of 20% is reported.

Component	Width (um)	Length (um)	Fingers	Multiplier
Q1	2	0.24	32	1
Q2	2	0.06	24	1
Q3	2	0.06	24	1
Q4	2	0.06	32	1
Q5	2	0.06	32	1
Q6	2	0.24	1	1
Q7	2	0.06	1	1
Cap Switches	2	0.06	20	8
Cap Switches	2	0.06	24	12
Varactors	6	0.15	32	2

TABLE II. ACTIVE DEVICE PARAMETERS

Component	Width (um)	Length (um)	Value	Quantity
C1	29.3	29.3	1.75pF	1
C2&3	51.36	51.36	5.35pF	2
C_unit	4.8	5	131fF	20
C4&5	22.1	22.1	1pF	2
R	2	12.84	5kΩ	4
L	198	194	1.5nH	1

TABLE III. PASSIVE DEVICE PARAMTERS

CONCLUSION

The VCO design provides a 20% tuning range with low phase noise. It consumes 6mW of power and has an area of 0.046 mm^2. The FOM for this design is 120.

REFERENCES

[1] R. Aparicio, A. Hajimiri, "A noise-shifting differential Colpitts VCO", IEEE J. Solid State Circuits, vol. 37, pp. 1728-1736, Dec. 2002.

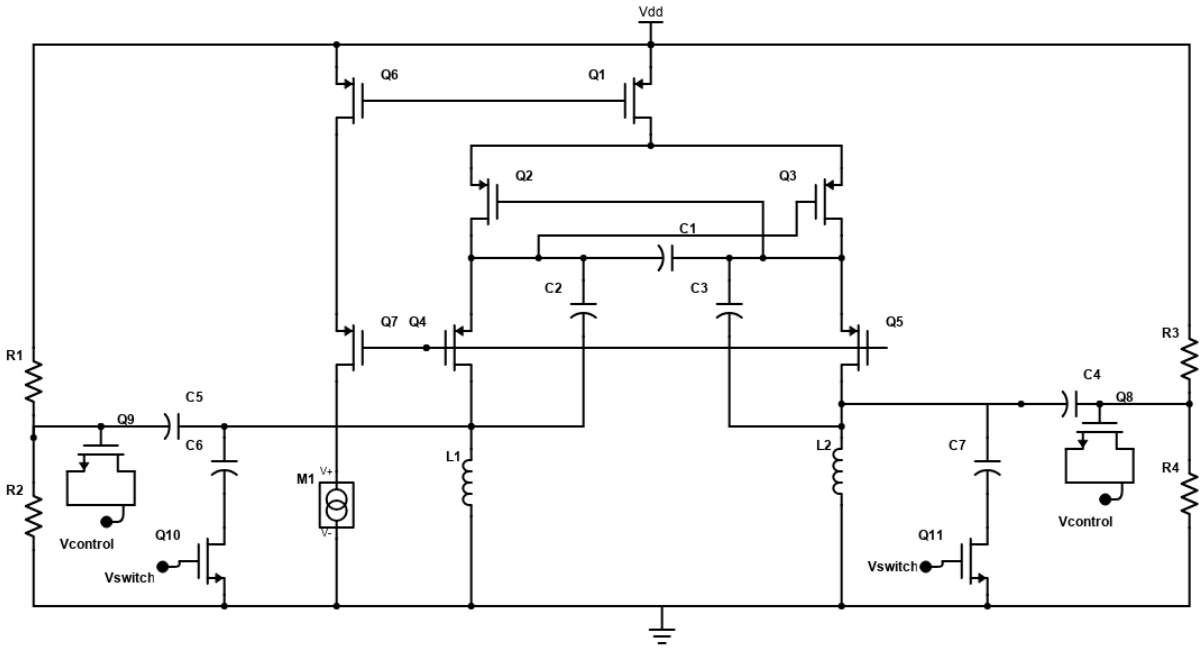

Figure 1. VCO Schematic