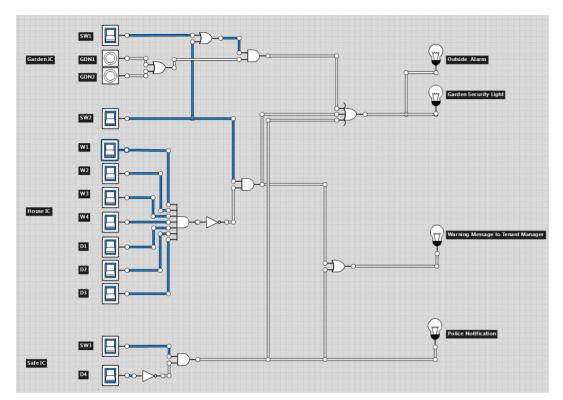
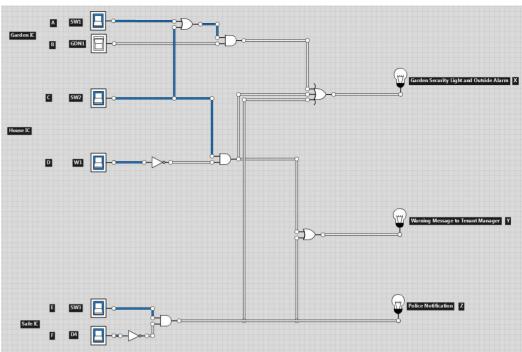
Updating the initial design





Garden Circuit:

Merged the garden sensor PTMs into one switch, in doing so removing the need for an OR gate. The two output lights were merged into one as they were identical.

House Circuit:

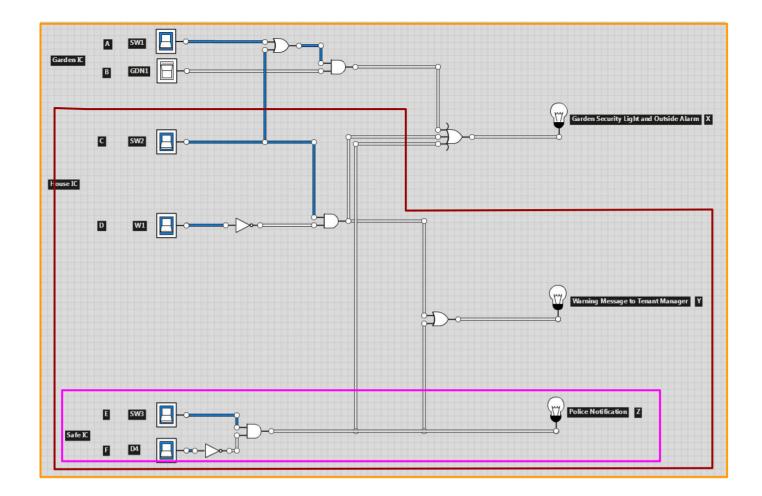
Merged the window switches into one switch, in doing so removing the need for an AND gate.

Safe Circuit:

No changes were made as the initial design only had one door switch.

Each of the inputs and outputs were assigned letters (A-F and X-Z respectively) to allow for the use of boolean algebra.

Primary Optimisation - Boolean Algebra



$$X = B(A+C) + CD' + EF'$$

Y = CD' + EF'

Z = EF'

Using the distributive law

No further simplification

No further simplification

X = AB + BC + CD' + EF'

No further simplification

Secondary Optimisation - Karnaugh Maps

Using the SOP form that we created in the primary optimisation process, we generated Karnaugh maps for each output.

$$X = B(A+C) + CD' + EF'$$

 $X = AB + BC + CD' + EF'$

DEF ABC	000	001	011	111	101	100	110	010
000							1	1
001	1	1	1				1	1
011	1	1	1	1	1	1	1	1
111	1	1	1	1	1	1	1	1
101 _	1	1	1				1	1
100							1	1
110	1	1	1	1	1	1	1	1
010							1	1

$$Y = CD' + EF'$$

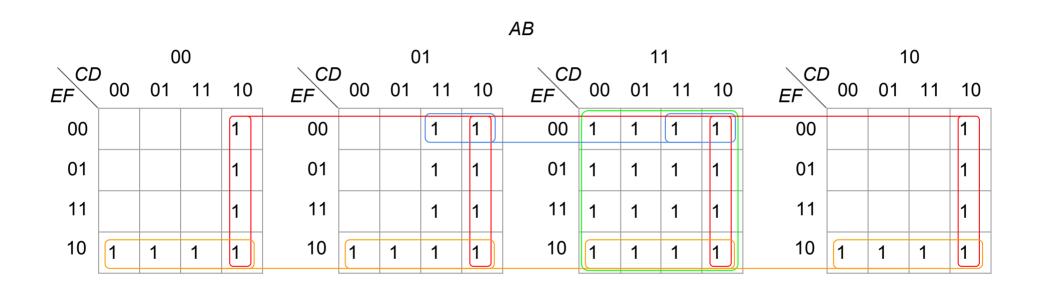
EF CD	00	01	11	10	
00				1	
01				1	
11				1	
10	1	1	1	1	

$$Z = EF'$$

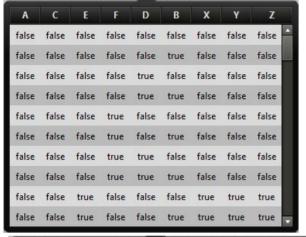
F	0	1
0		
1	1	

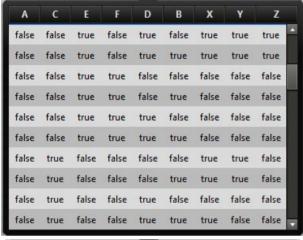
Testing Optimised Circuit Against Updated Circuit

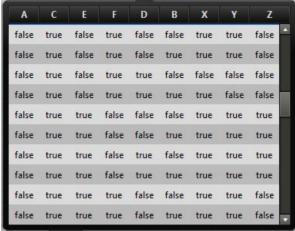
https://docs.google.com/spread sheets/d/1aR111SEPgwN3uUL YRzrOjB2mOmJWx8U3RDdO6 fz7_Nc/edit#gid=862095346&ra nge=A1

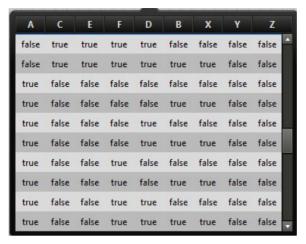


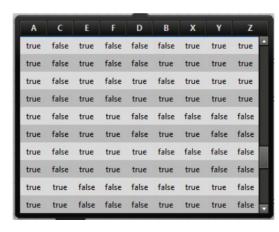
Optimised Circuit LogicLy Truth Tables

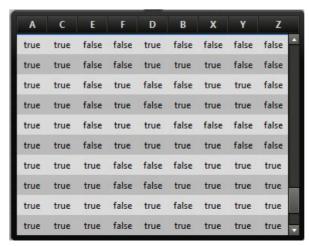


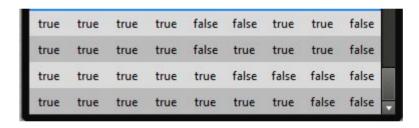




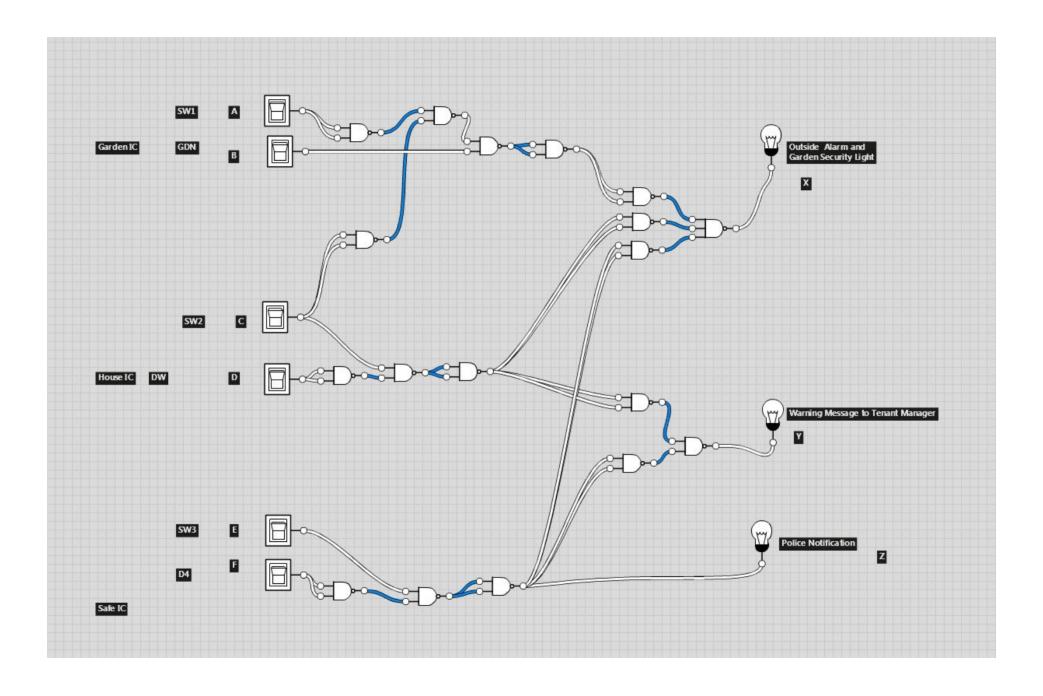








Universal Gate Conversion (NAND)



Universal Gate Truth Table

https://docs.google.com/spreadshee ts/d/1aR111SEPgwN3uULYRzrOjB 2mOmJWx8U3RDdO6fz7_Nc/edit# gid=0&range=A1

Universal Gate LogicLy Truth Tables



