A. Motivation:

The work to be developed aims at giving students the knowledge concerning the limitations of Shockley's model in the characterization of NMOS transistors in nanometric technologies. Mosfet characteristics obtained through simulation in Ltspice will be used.

Case study

For this work, simulation of Mosfets in a Nanometric technology will be considered. A 90nm technology will be studied. Technology files for L=70nm (90nm_NMOS_bulkL70n.pm) and L=700nm (90nm_NMOS_bulkL700n.pm) are to be used.

The Mosfet Schokley's model is considered, where the current flowing through the transistor drain may be obtained with:

$$Id = \begin{cases} 0 & \Leftarrow \quad v_{gs} < v_t \\ 2K\left(\left(v_{gs} - v_t\right)v_{ds} - 0.5{v_{ds}}^2\right)(1 + \lambda v_{ds}) & \Leftarrow \quad v_{gs} \geq v_t \wedge v_{ds} < v_{gs} - v_t \\ K\left(v_{gs} - v_t\right)^2(1 + \lambda v_{ds}) & \Leftarrow \quad v_{gs} \geq v_t \wedge v_{ds} \geq v_{gs} - v_t \end{cases}$$

Methodology

A. For technology file *90nm_NMOS_bulkL700n.pm*, consider a NMOS with *W=L=700nm*
   a. Using Ltspice obtain $I_D(V_{GS},V_{DS})$ for V_{DS}=1.2V and $0 \leq V_{GS} \leq 1.2$ (with a step of 0.01V)
   b. Using Ltspice obtain $I_D(V_{GS},V_{DS})$ for $0 \leq V_{DS} \leq 1.2$ (with a step of 0.01V)and $V_{GS} \in [0.4, 0.6, 0.8, 1.0, 1.2]$
   c. Import Characteristics into Python and plot them
   d. Using $0 \leq V_{GS} \leq 1.2$ use the gm/I_D approach to evaluate values for V_t
   e. Drive conclusions on the accuracy of the results obtained

B. For technology file *90nm_NMOS_bulkL70n.pm*, consider a NMOS with *W=L=70nm* repeat all steps considered in A.