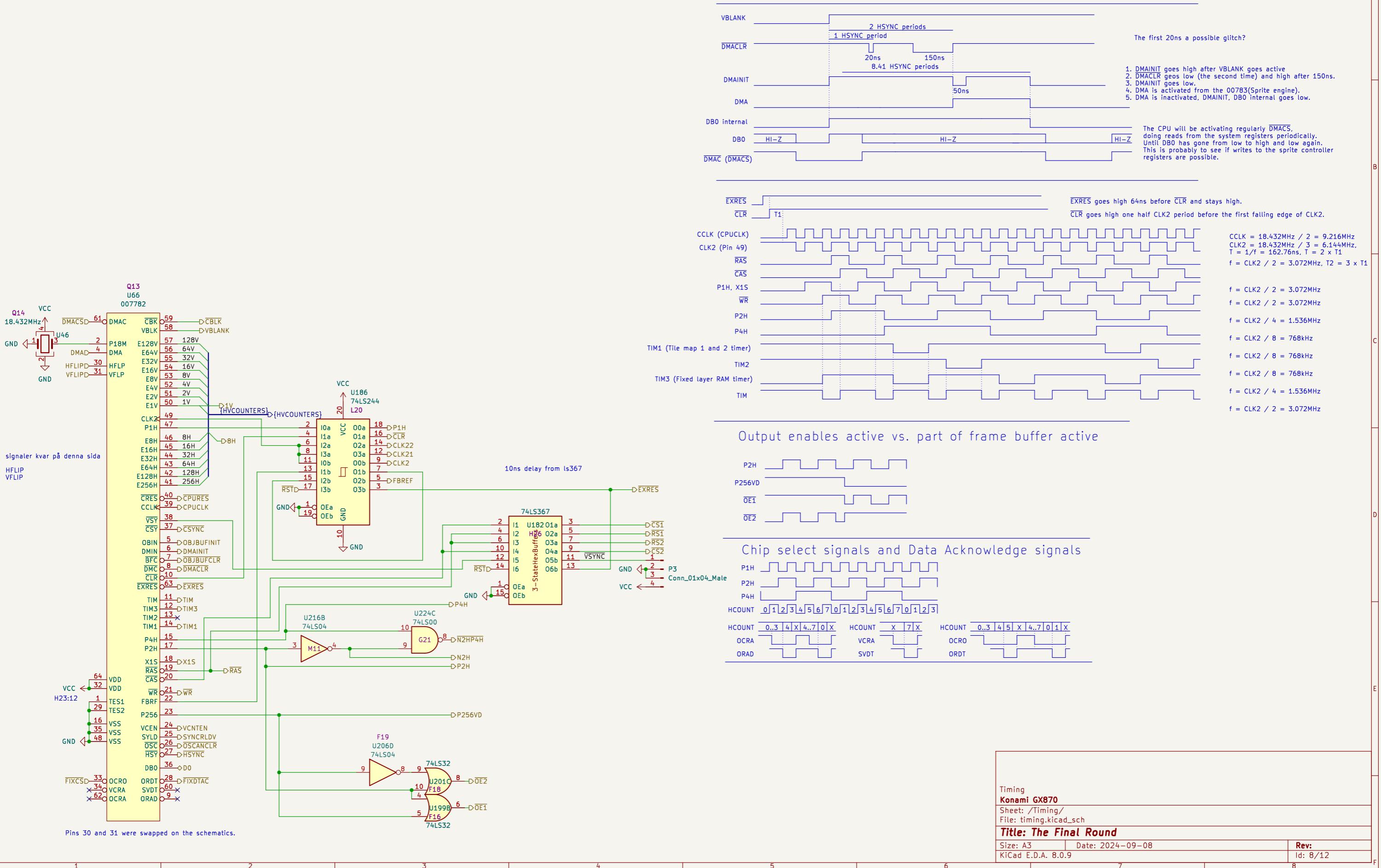
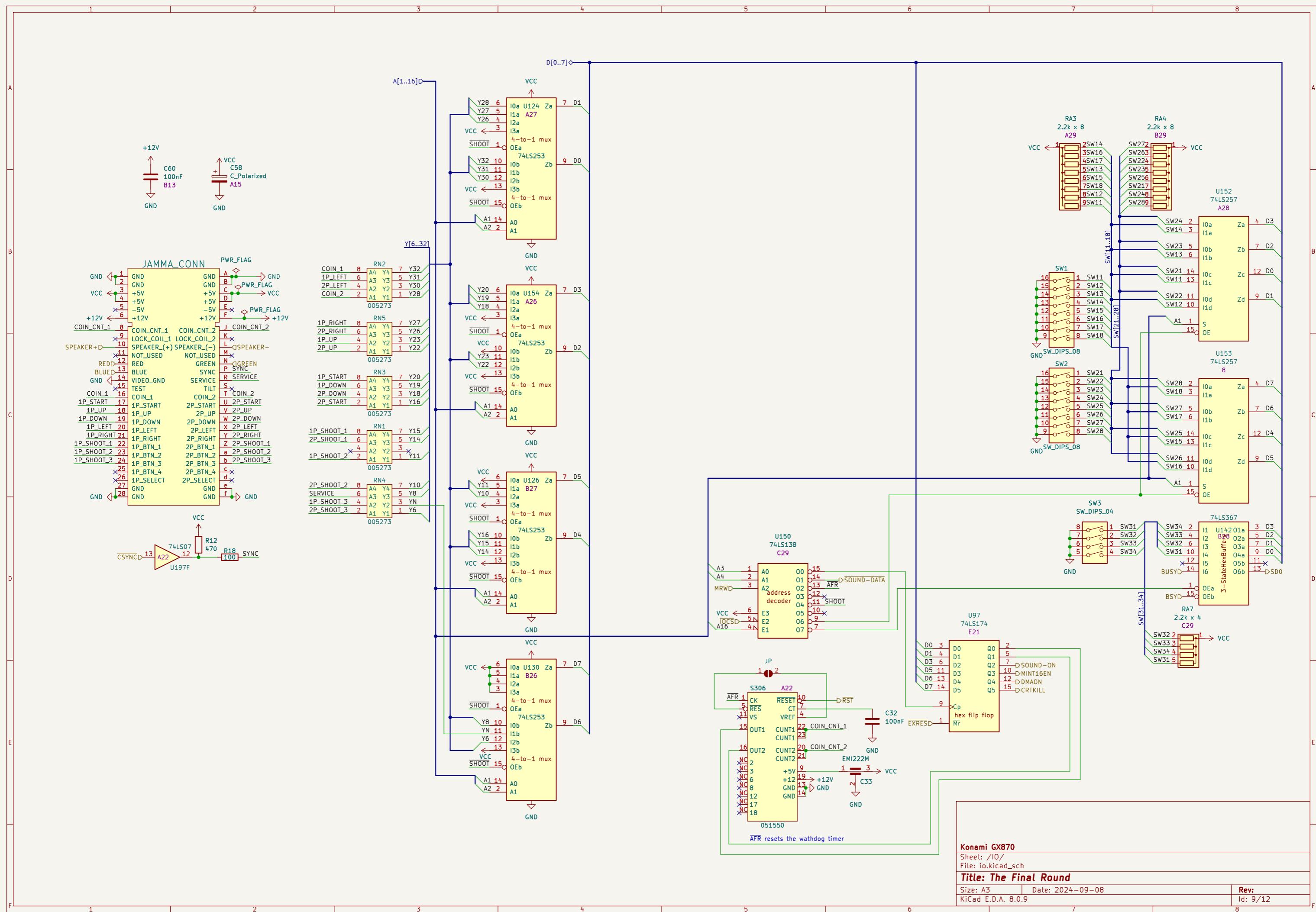
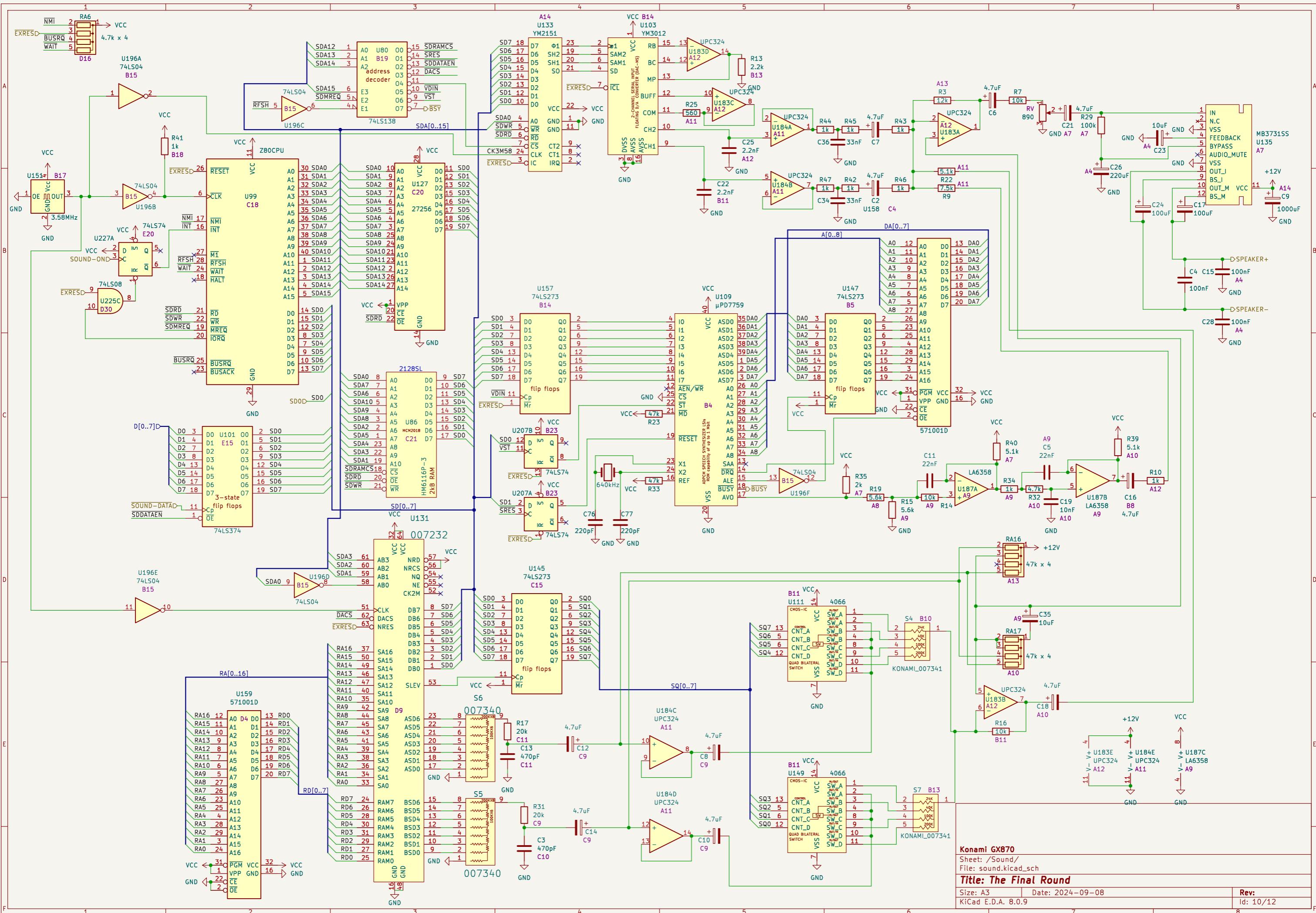


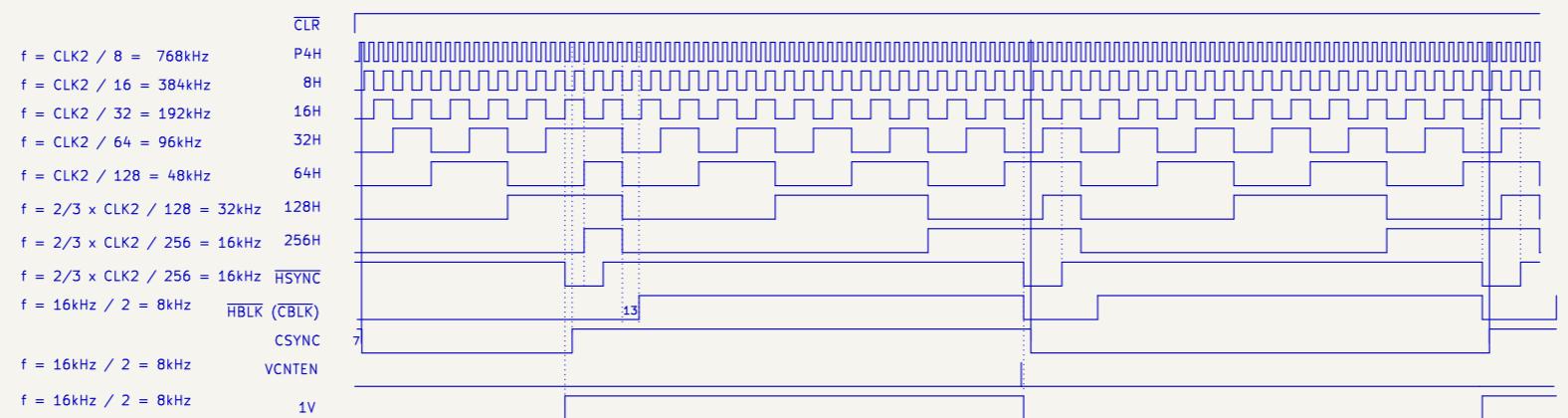
# DMA Synchronization







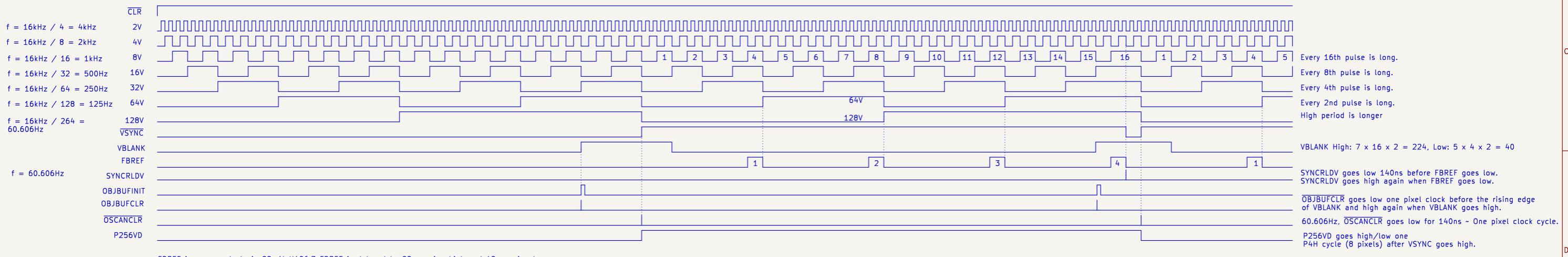
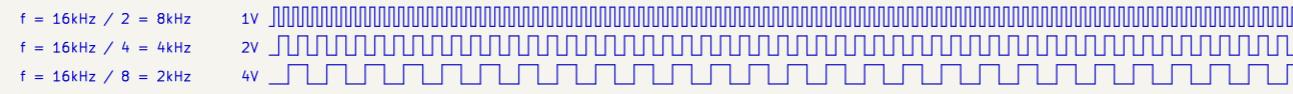
## Horizontal signals



- The first VCNTEN is skipped after reset.  
It goes low 140ns before HSYNC goes low,  
and high again when HSYNC goes low.  
VCNTEN is active right before every second falling edge of  
HSYNC.

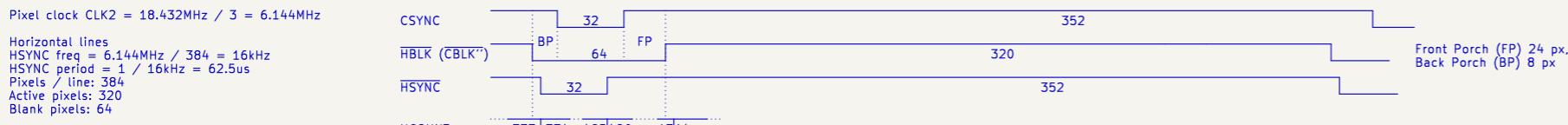
- CPURES goes high, and stays high, on the seventh falling edge  
of HSYNC.

## Vertical signals

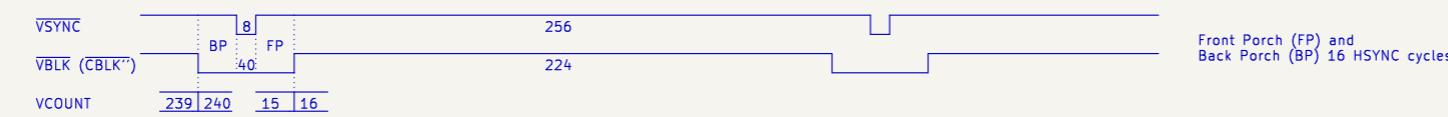


## Horizontal and vertical synch timing diagrams

The numbers in the HSYNC and HBLK diagrams are HSYNC cycles.  
All edges are synchronised to the rising edge of CLK2.



The numbers in the VSYNC and VBLK diagrams are HSYNC cycles.  
All edges are synchronised to the falling edge of HSYNC.



HCOUNT is bits [256H, 128H, 64H, 32H, 16H, 8H, P4H, P2H, P1H]  
VCOUNT is bits [128V, 64V, 32V, 16V, 8V, 4V, 2V, 1V]

CBLK<sup>''</sup> is at the output of color mixer.

### Konami GX870

Sheet: /Timing diagrams/  
File: timing\_diagrams.kicad\_sch

### Title: The Final Round

Size: A3	Date: 2024-09-08
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A

B

C

D

E

F

A

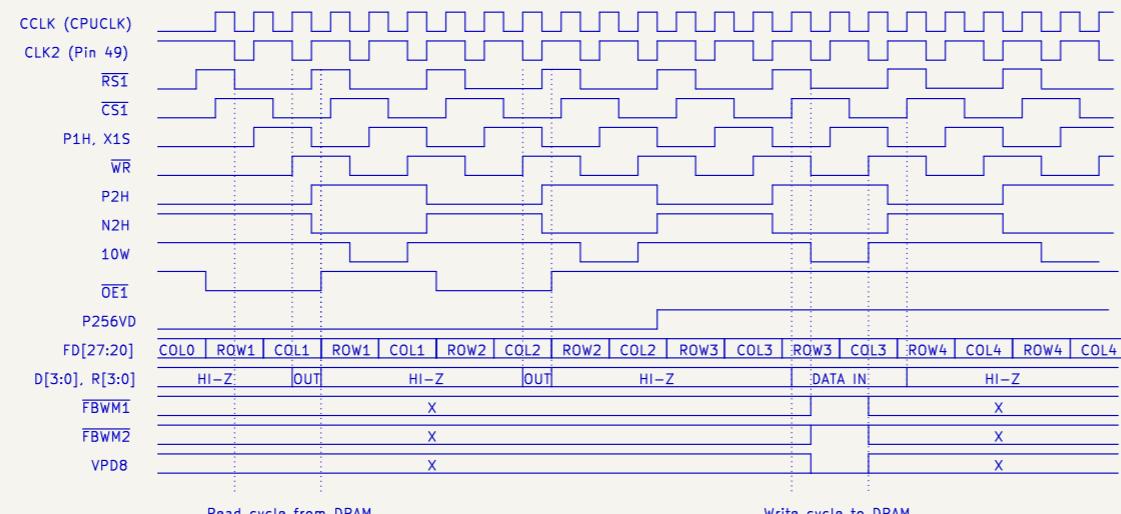
B

C

D

E

F

**Konami GX870**

Sheet: /Sprite timing diagrams/  
File: sprite\_timing\_diagrams.kicad\_sch

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