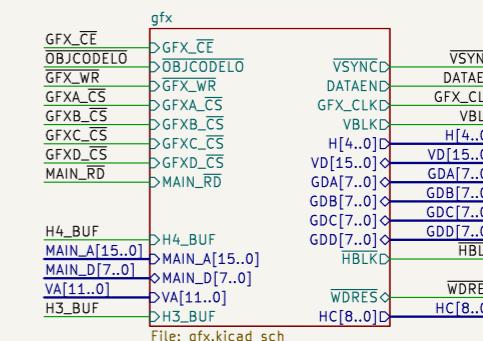
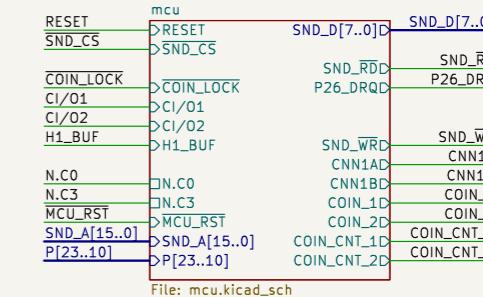
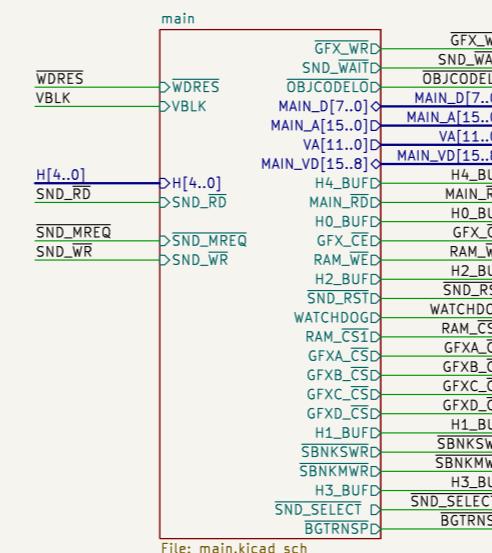
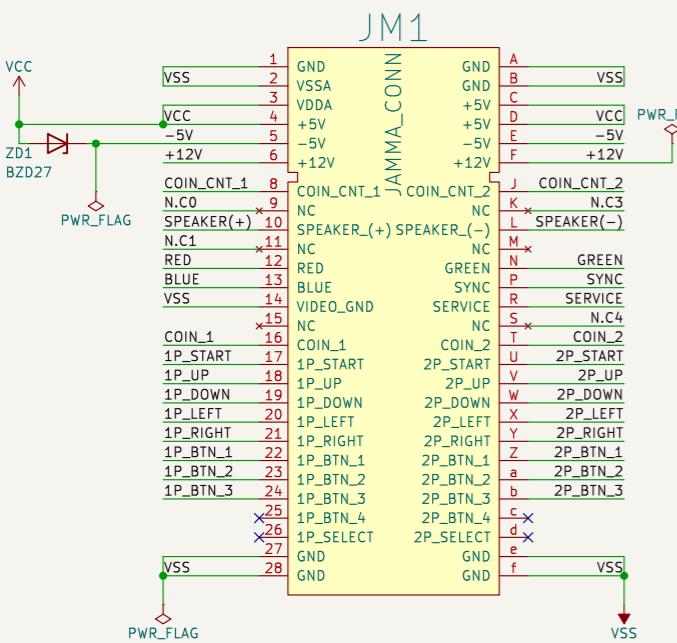
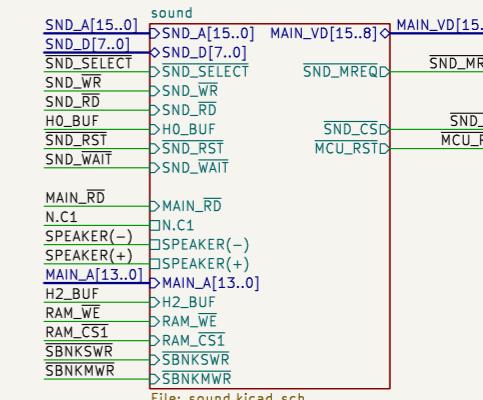
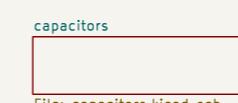
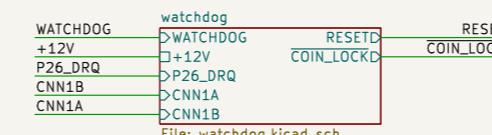
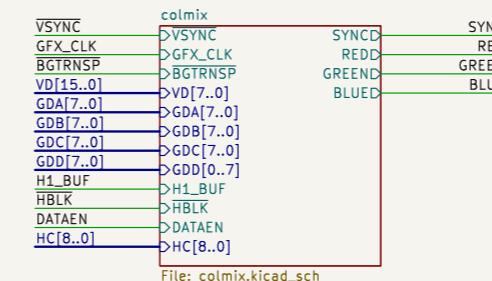
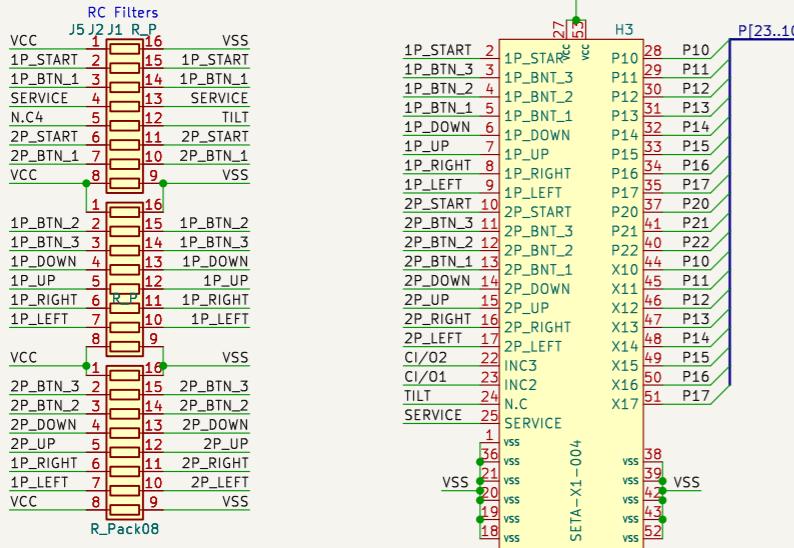


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CABINET I/O



JOTEGO

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Size: A3 | Date: 29/08/2022
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Id: 1/10

1 2 3 4 5 6 7 8

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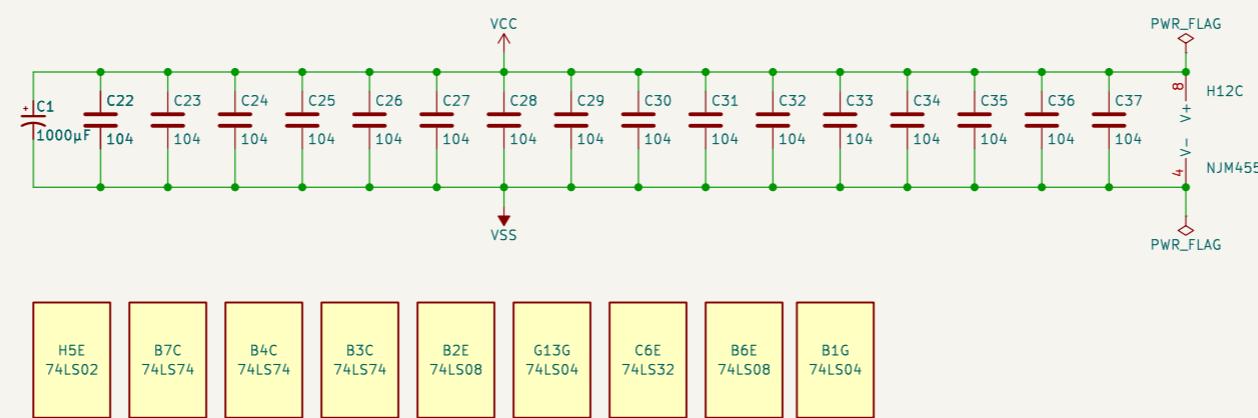
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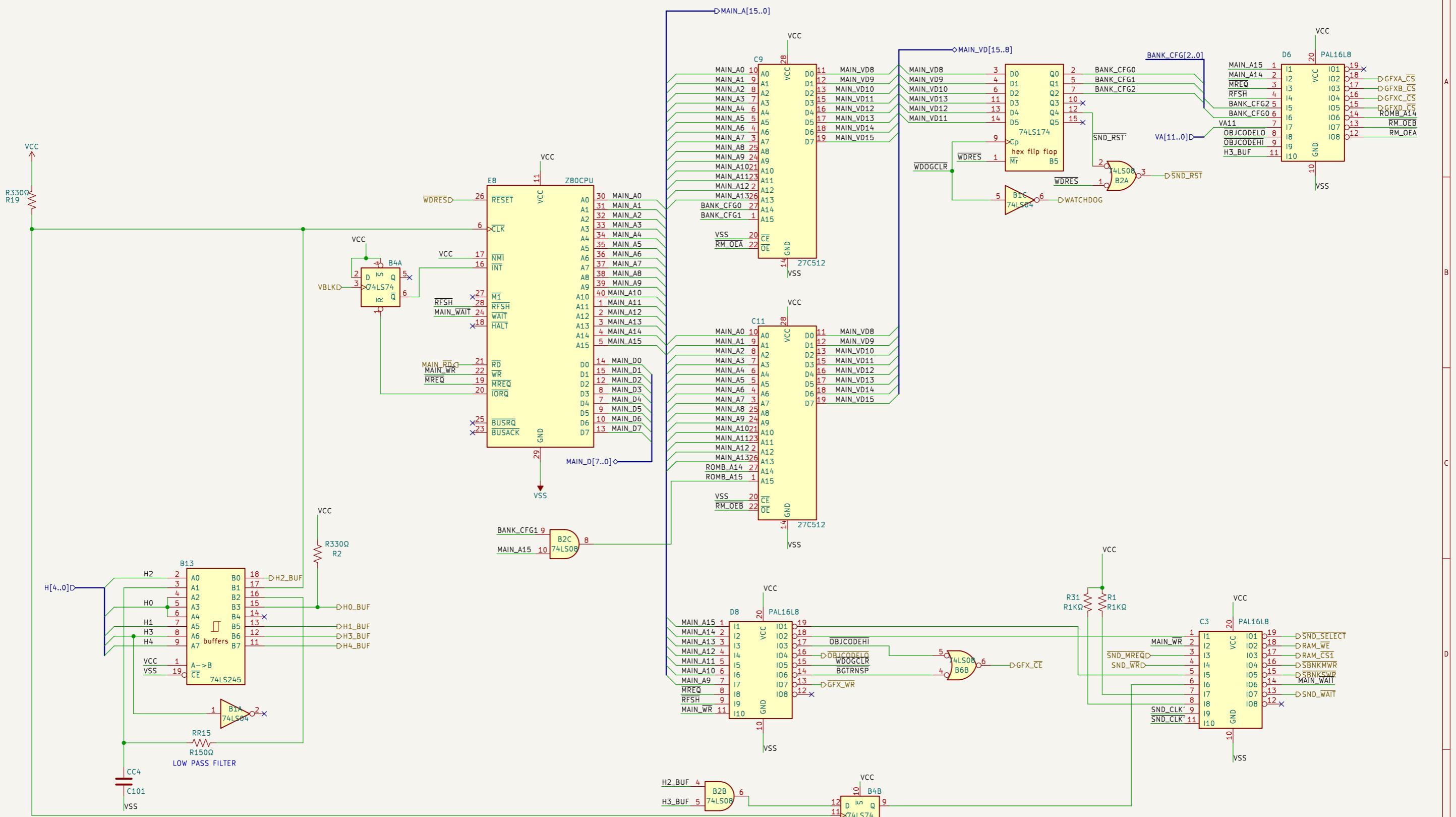
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Id: 3/10

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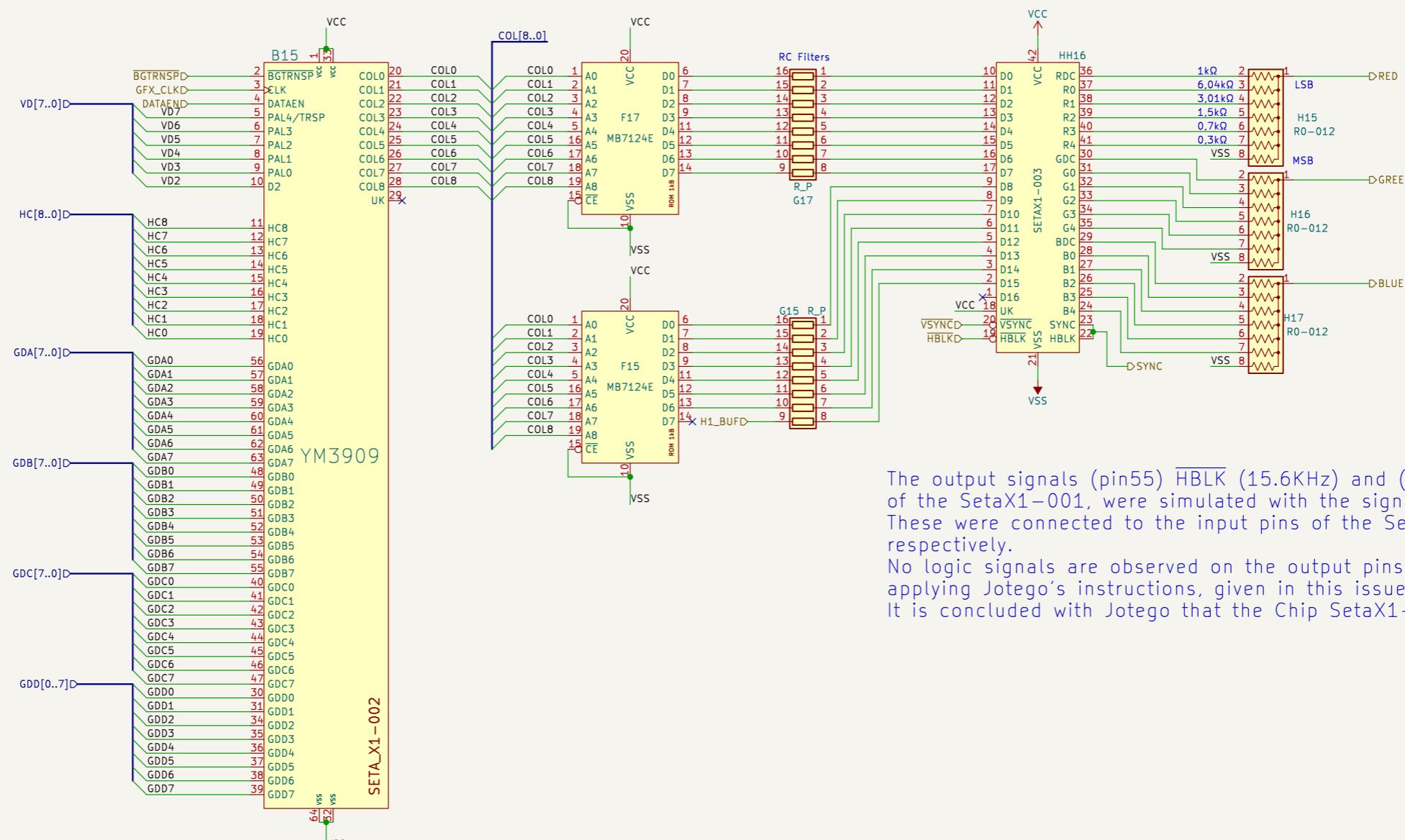
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The output signals (pin 55) **HBLK** (15.6KHz) and (pin 56) **VSYNC** (59.2 Hz) of the **SetaX1-001**, were simulated with the signal generator and an inverter. These were connected to the input pins of the **SetaX01-003** (pin 19 – 20), respectively. No logic signals are observed on the output pins (22–23) **HBLK** – **SYNC**, applying Jotego's instructions, given in this issue. It is concluded with Jotego that the Chip **SetaX1-001** is broken.



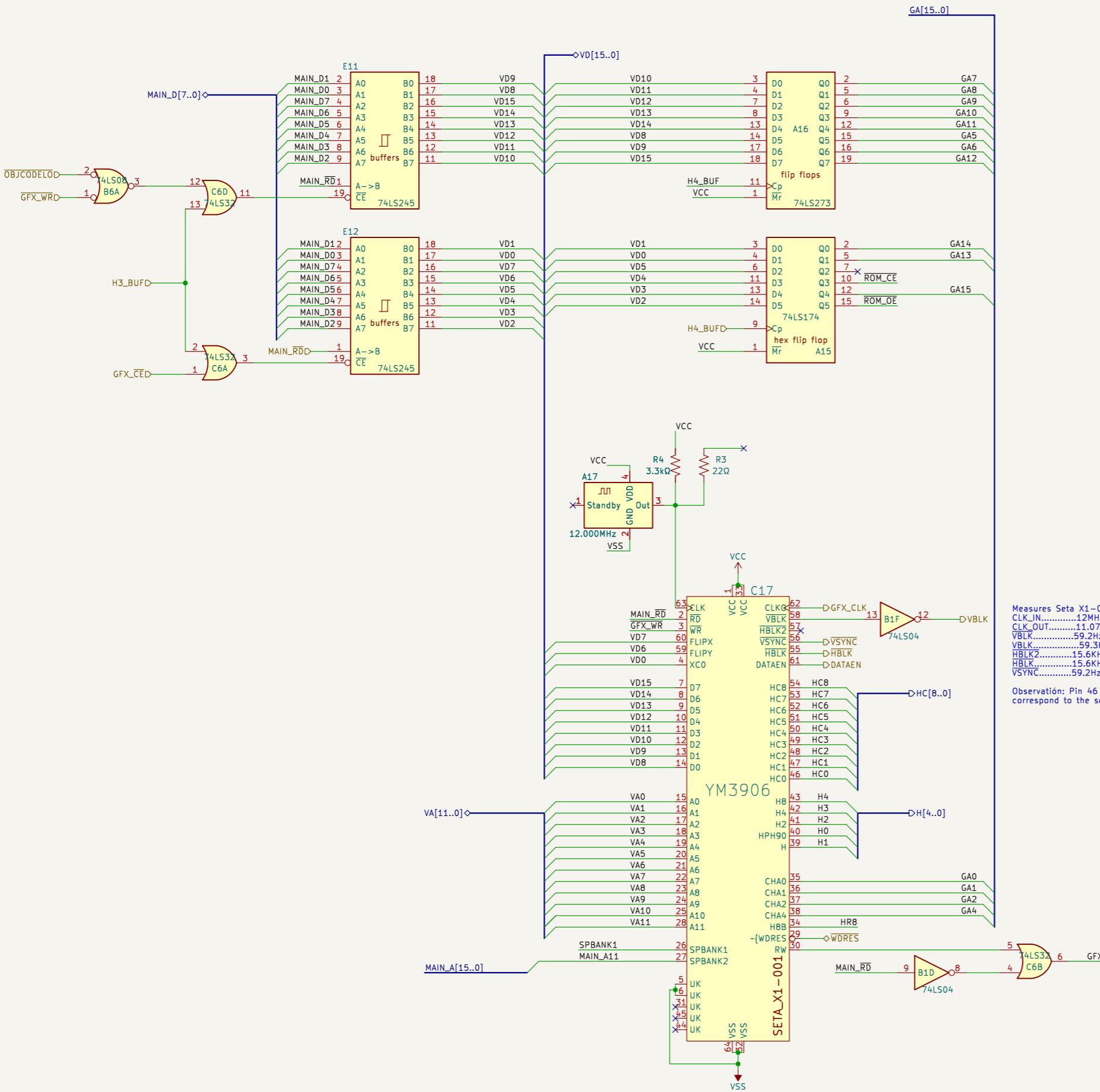
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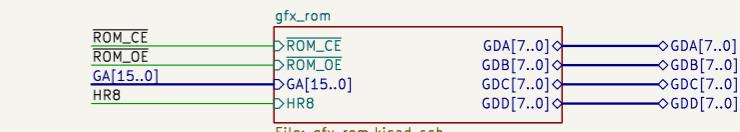
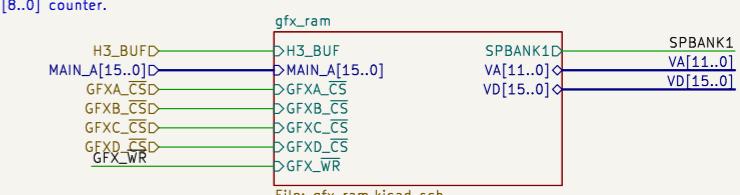
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Measures Seta X1-001:
CLK_IN.....12MHz
CLK_OUT.....11.07-12.01MHz
VBLK.....59.2Hz
VBLK.....59.3Hz
HBLK1.....15.6KHz
HBLK2.....15.6KHz
VGNDVG.....59.3Hz

Observación: Pin 46 (HCO) does not correspond to the sequence of the HC[8..0] counter.



JOTEGO

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File: gfx.kicad_sch

Title: EXTERMINATION

Size: A3 Date: 29/08/2022
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1 2 3 4 5 6 7 8

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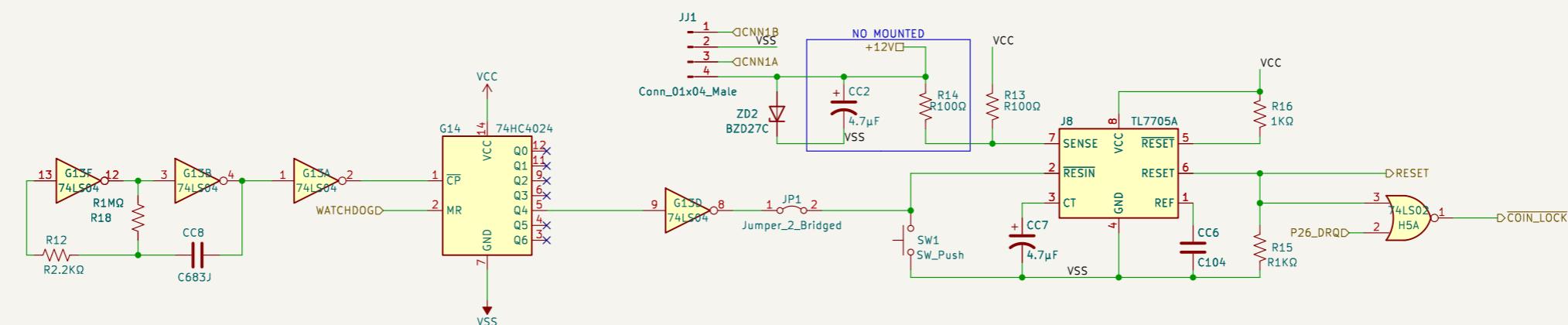
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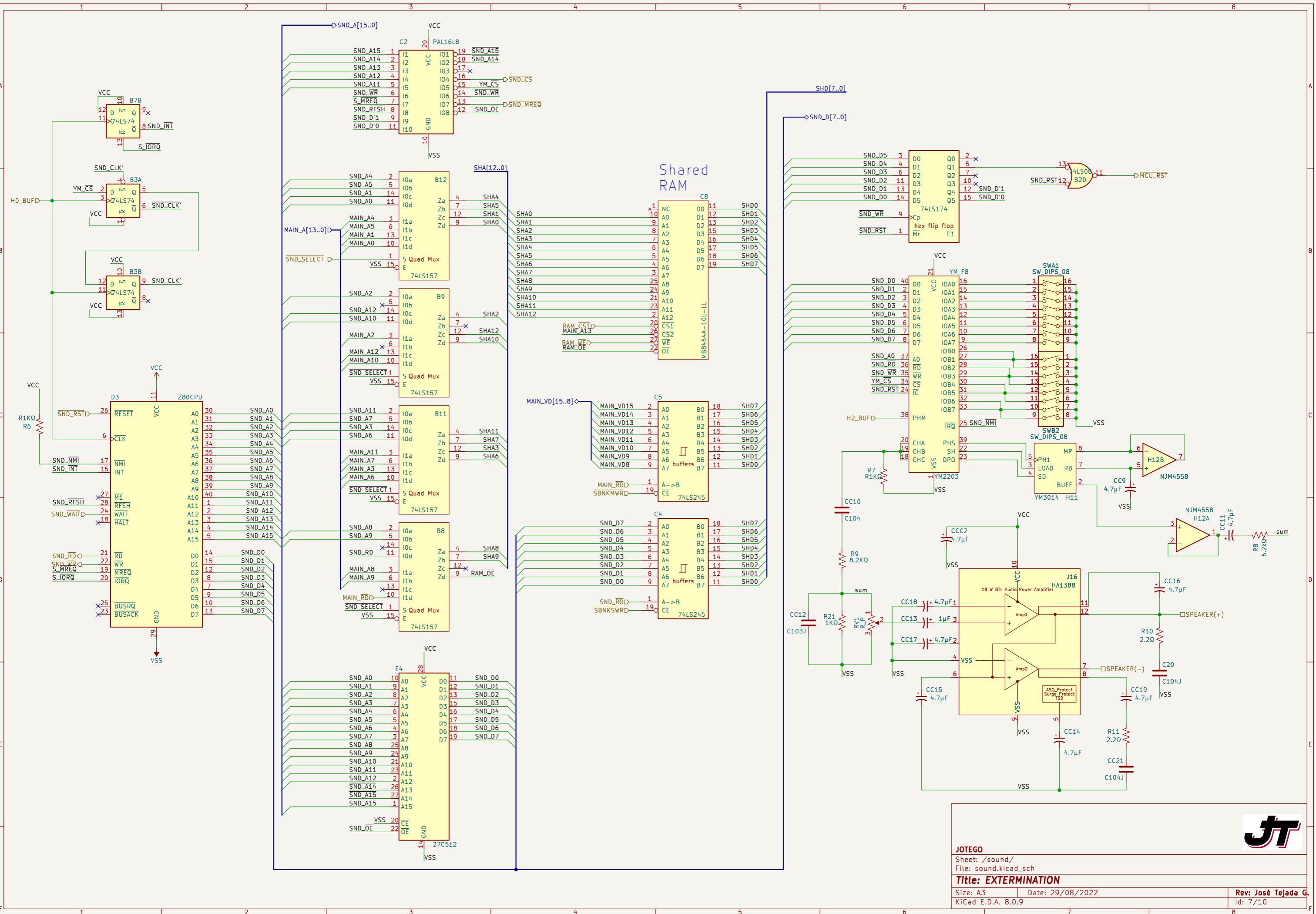
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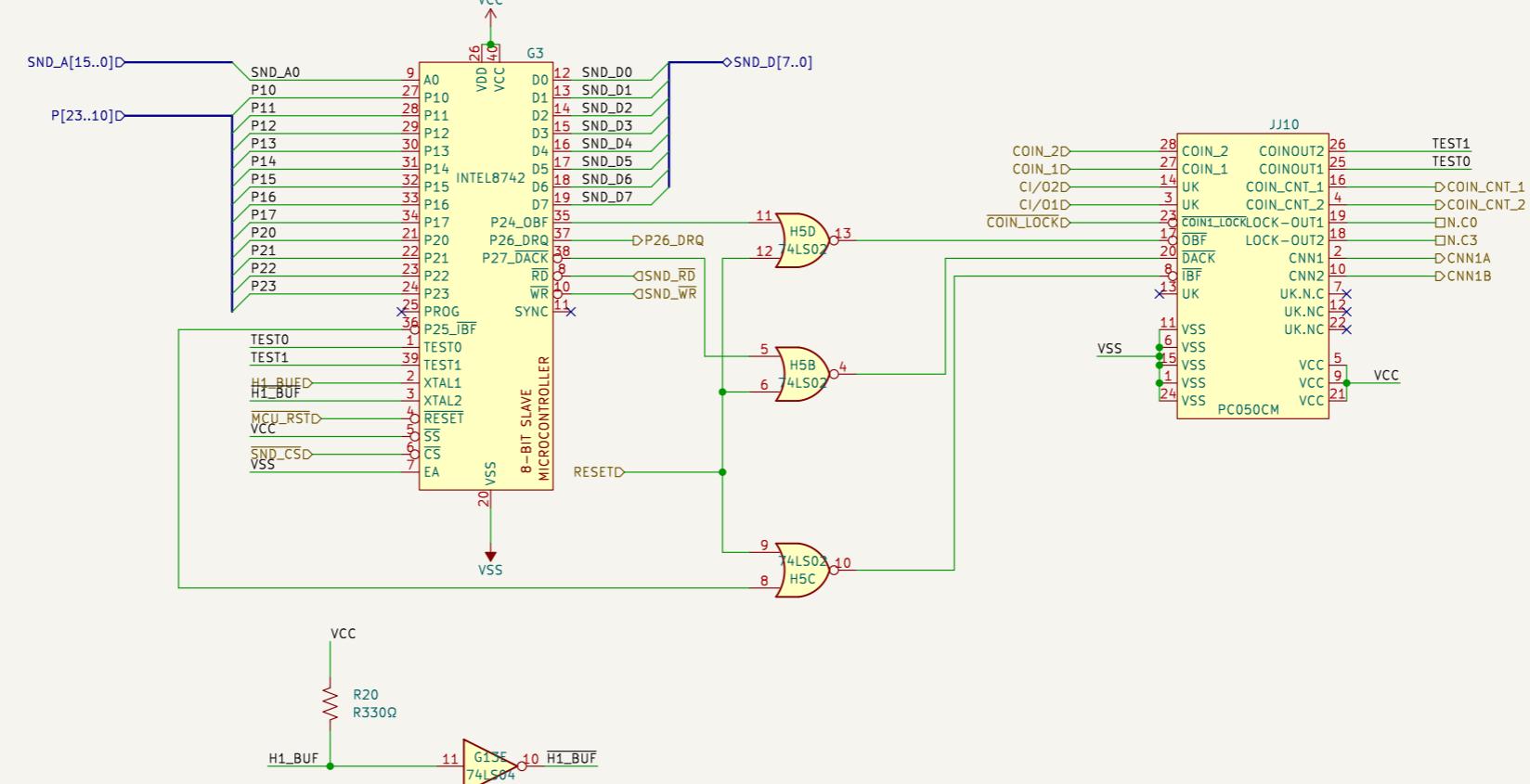
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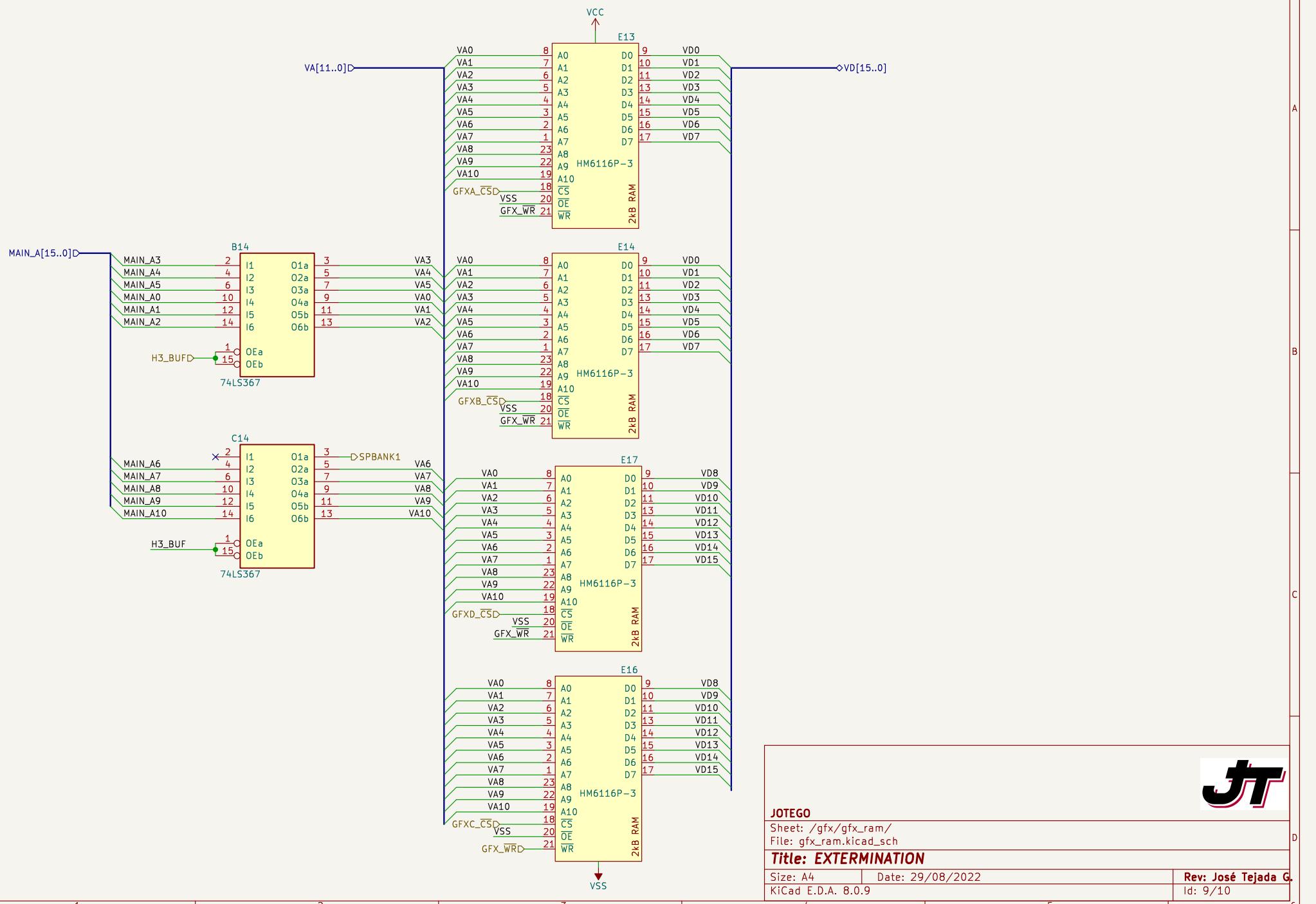
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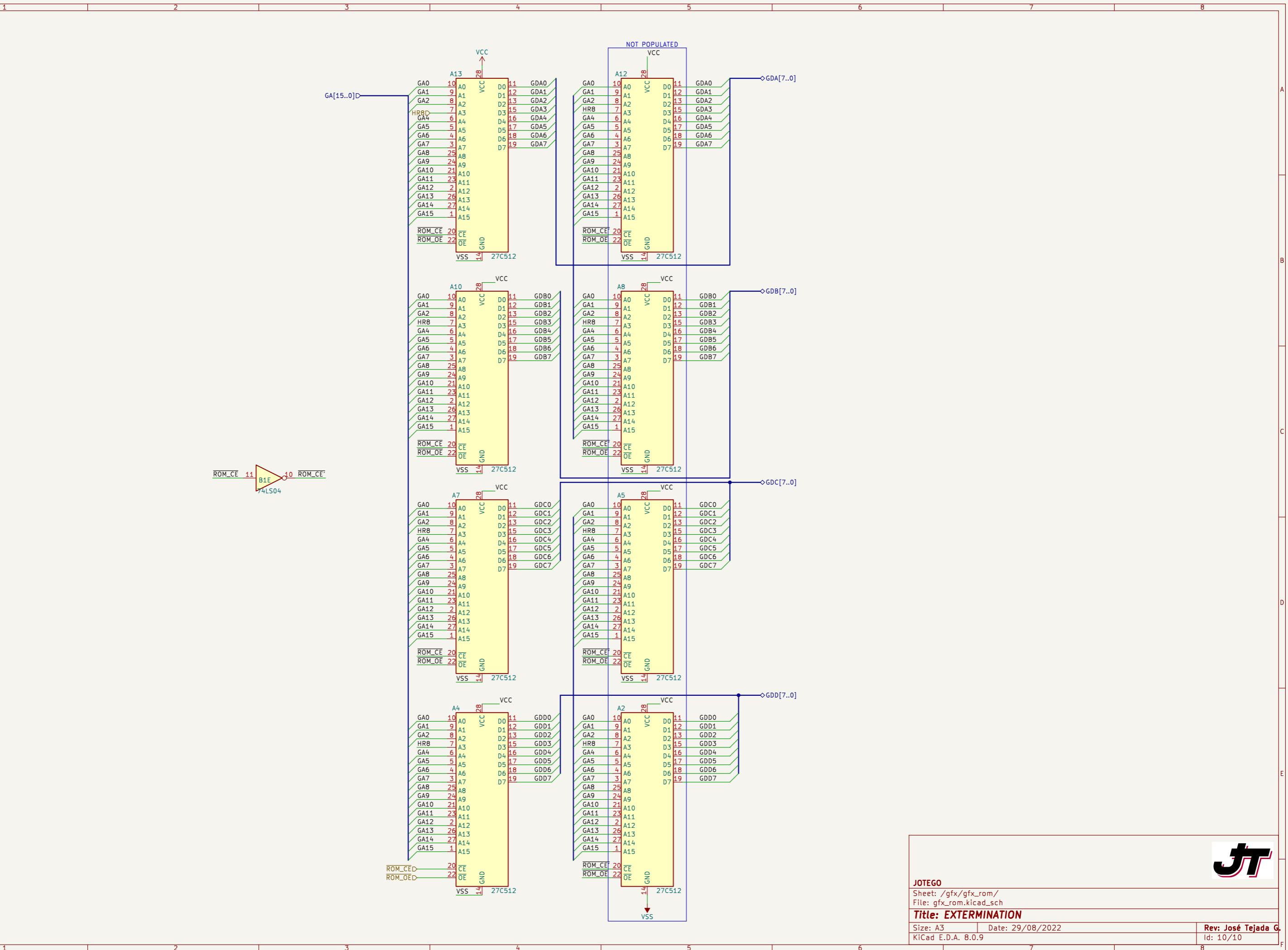
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KiCad E.D.A. 8.0.9



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JOTEGO

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Size: A3 | Date: 29/08/2022
KiCad E.D.A. 8.0.9



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