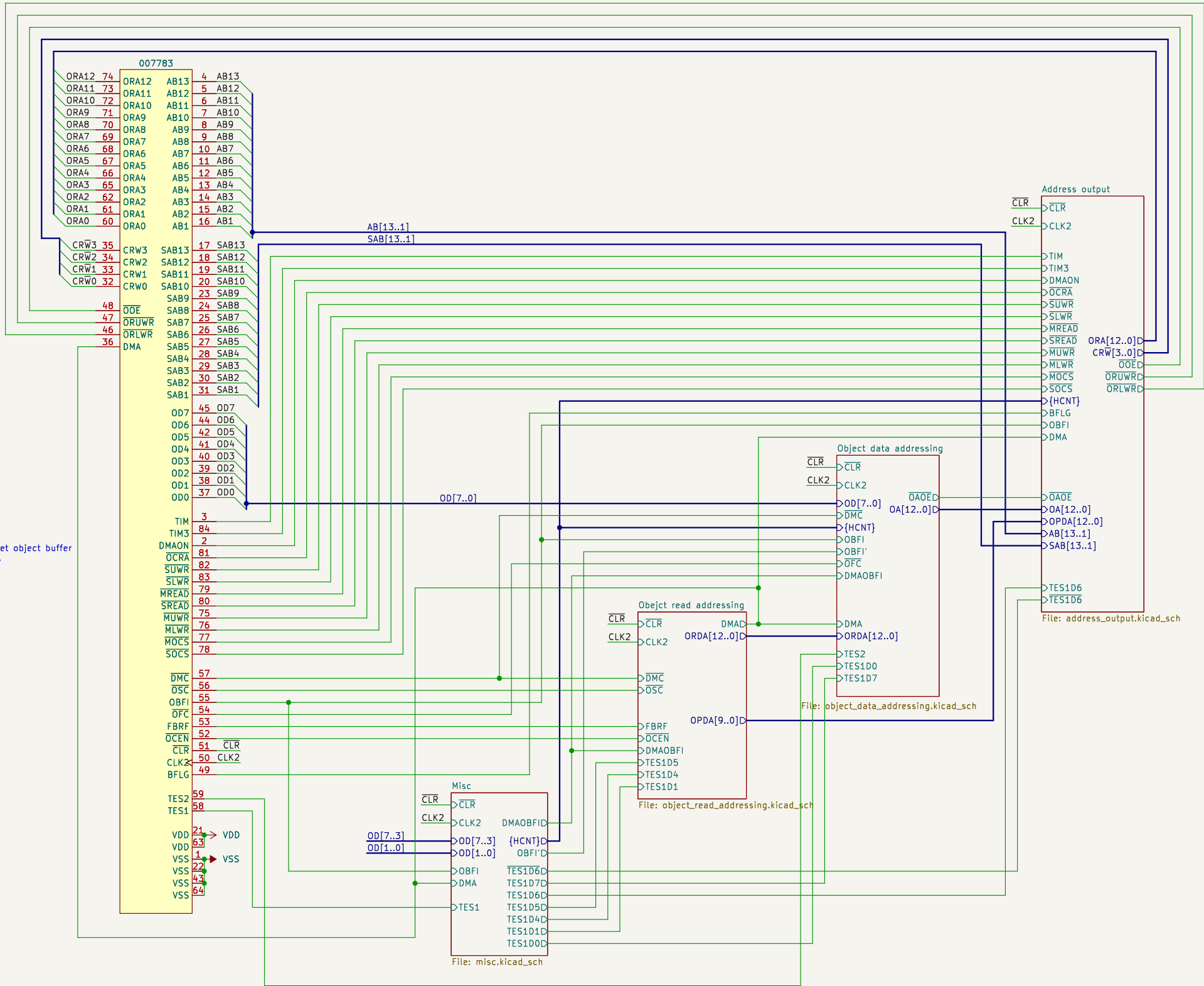# 007783

Notes:

1. OBFI: (OBJBUFINIT) zeros are written to 1800h..1AFFh.
2. DMA: OA[12:0] active.
   a) 8 words are read from addresses 0000h..0007h, 0028h..002Fh,....17E0h..17E7h
      by the sprite data parser 007784 and if the sprite is enabled with BEFLAG
      they are written to the buffer OBJBUF.

OBJRAM

0000h..17E7h	Unprocessed data
1800h..1BFFh	Processed data

WD0	WD1	WD2	WD3	WD4	WD5	WD6	WD7	WD0	WD1	WD2	WD3
0000	0001	0002	0003	0004	0005	0006	0007	BA1	BA2	BA3	BA4

OBJBUF, Buffer Address

BA1 : OA[12:0] = 1800h + OD''[7:0] << 2
BA2 : OA[12:0] = BA1 + 1
BA3 : OA[12:0] = BA1 + 2
BA4 : OA[12:0] = BA1 + 3

OBFI	H8	OA		OAOE	
1	X	{3'b110,OWRA[9:0]}		1	Writes to 1800h..1BFFh, reset object buffer
0	0	ORDA[12:0]		0	Read data from object RAM.
0	1	{3'b110,OD''[7:0],OWRA[2:1]}		1	Writes to 1800h..1BFFh

007783 (main IC)

Pin	Left signal		Right signal	Pin
74	ORA12	AB13	AB13	4
73	ORA11	AB12	AB12	5
72	ORA10	AB11	AB11	6
71	ORA9	AB10	AB10	7
70	ORA8	AB9	AB9	8
69	ORA7	AB8	AB8	9
68	ORA6	AB7	AB7	10
67	ORA5	AB6	AB6	11
66	ORA4	AB5	AB5	12
65	ORA3	AB4	AB4	13
62	ORA2	AB3	AB3	14
61	ORA1	AB2	AB2	15
60	ORA0	AB1	AB1	16
35	CRW3	SAB13	SAB13	17
34	CRW2	SAB12	SAB12	18
33	CRW1	SAB11	SAB11	19
32	CRW0	SAB10	SAB10	20
48	OOE	SAB9	SAB9	23
47	ORUWR	SAB8	SAB8	24
46	ORLWR	SAB7	SAB7	25
36	DMA	SAB6	SAB6	26
		SAB5	SAB5	27
		SAB4	SAB4	28
		SAB3	SAB3	29
		SAB2	SAB2	30
		SAB1	SAB1	31
		OD7	OD7	45
		OD6	OD6	44
		OD5	OD5	42
		OD4	OD4	41
		OD3	OD3	40
		OD2	OD2	39
		OD1	OD1	38
		OD0	OD0	37
3	TIM			
84	TIM3			
2	DMAON			
81	OCRA			
82	SUWR			
83	SLWR			
79	MREAD			
80	SREAD			
75	MUWR			
76	MLWR			
77	MOCS			
78	SOCS			
57	DMC			
56	OSC			
55	OBFI			
54	OFC			
53	FBRF			
52	OCEN			
51	CLR			
50	CLK2			
49	BFLG			
59	TES2			
58	TES1			
21	VDD	VDD		
63	VDD			
1	VSS	VSS		
22	VSS			
43	VSS			
64	VSS			

Address output

CLR
CLK2
TIM
TIM3
DMAON
OCRA
SUWR
SLWR
MREAD
SREAD
MUWR
MLWR
MOCS
SOCS
{HCNT}
BFLG
OBFI
DMA
AB[13..1]
SAB[13..1]

ORA[12..0]
CRW[3..0]
OOE
ORUWRD
ORLWRD

OAOE
OA[12..0]
OPDA[12..0]
AB[13..1]
SAB[13..1]

TES1D6
TES1D6

File: address_output.kicad_sch

Object data addressing

CLR
CLK2
OD[7..0]
DMC
{HCNT}
OBFI
OBFI'
OFC
DMAOBFI
DMA
OAOED
OA[12..0]

File: object_data_addressing.kicad_sch

Objcet read addressing

CLR
CLK2
DMC
OSC
FBRF
OCEN
DMAOBFI
TES1D5
TES1D4
TES1D1
DMAD
ORDA[12..0]
OPDA[9..0]
ORDA[12..0]
TES2
TES1D0
TES1D7

File: object_read_addressing.kicad_sch

Misc

CLR
CLK2
OD[7..3]
OD[1..0]
OBFI
DMA
TES1
DMAOBFID
{HCNT}
OBFI'
TES1D6
TES1D7
TES1D6
TES1D5
TES1D4
TES1D1
TES1D0

File: misc.kicad_sch

AB[13..1]
SAB[13..1]
OD[7..0]
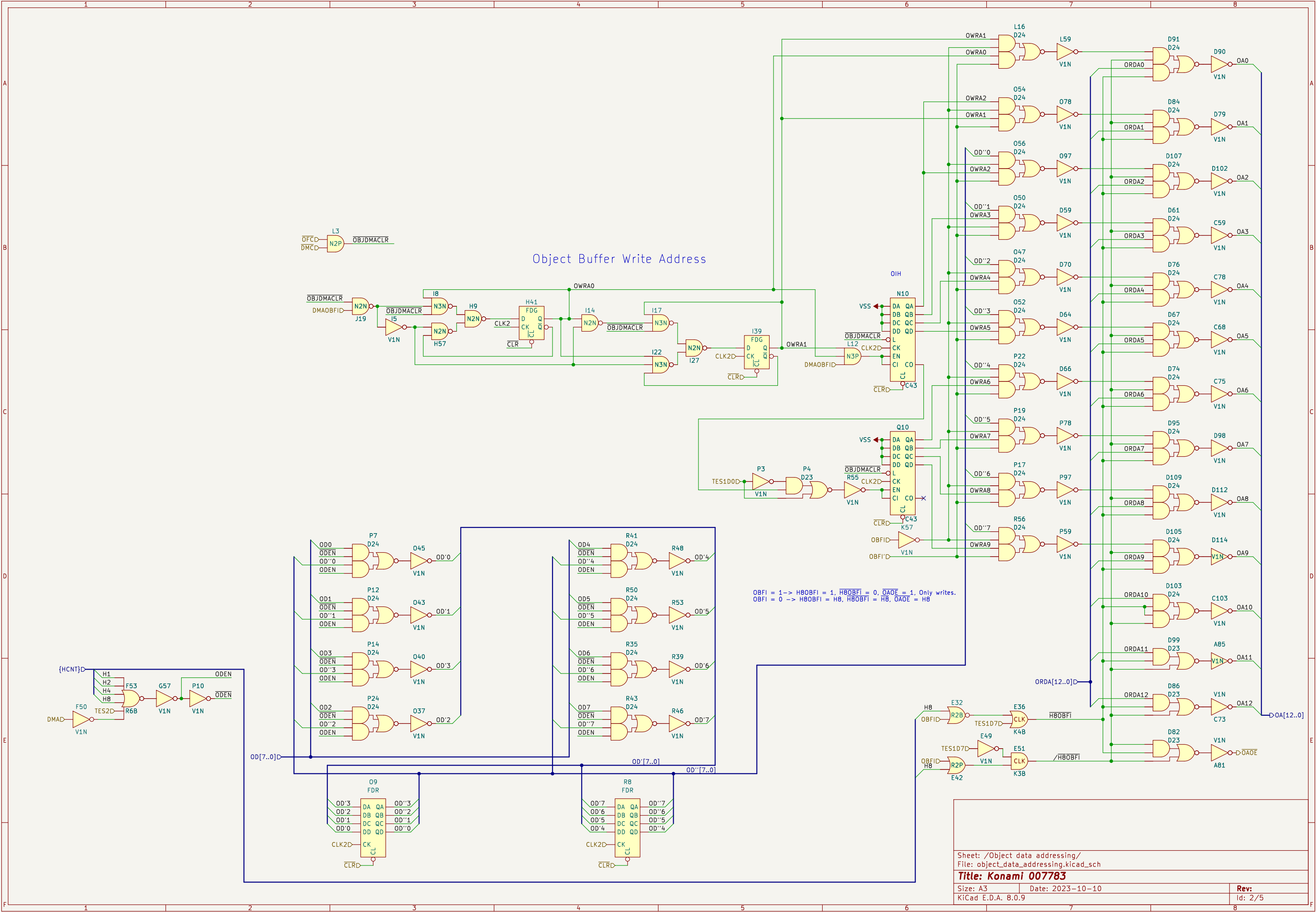
Ulf Skutnabba, twitter: @skutis77

Sheet: /
File: 007783.kicad_sch

Title: Konami 007783

Size: A3	Date: 2023-10-10	Rev:
KiCad E.D.A. 8.0.9		Id: 1/5

Object Buffer Write Address

OBFI = 1-> H8OBFI = 1, H8OBFI = 0, OAOE = 1, Only writes.
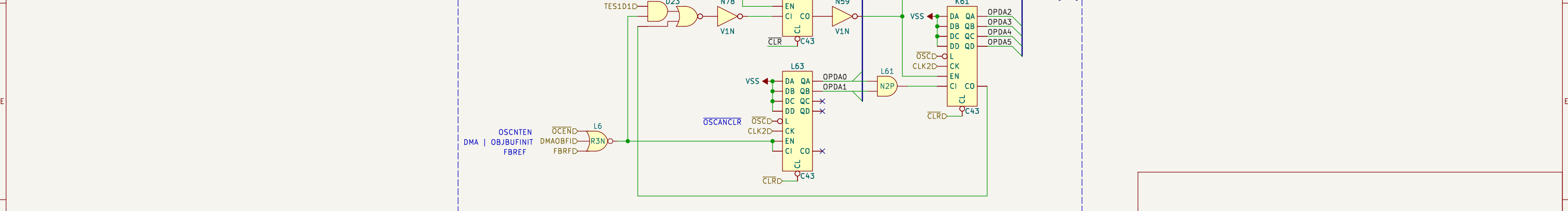OBFI = 0 -> H8OBFI = H8, H8OBFI = H8, OAOE = H8

Object Read Addressing
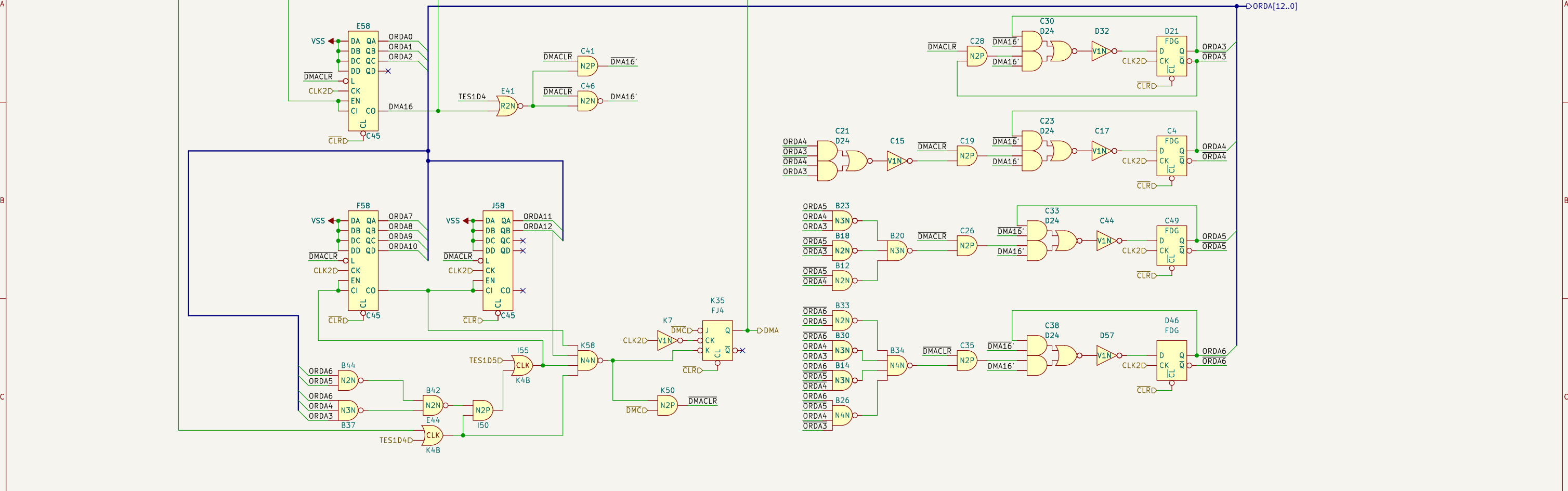
Addressing starts when OSC is activated.
OPDA[12:10] = 110 -> 0x1800..0x1BFF

When DMA, OBJBUFINIT and FBREF are not active the address is
incremented when OCEN is deactivated.

Parsed Object Data Addressing

ORDA[12..0]

OPDA[9..0]

OBFI — J37 / K1B — DMAD — L9 / R2P — OBFI'
DMAOBFI

Test register 1

OD[7..3]
OD7
OD6
OD5
OD4

FDR L32
DA QA — TES1D7
DB QB — TES1D6
DC QC — TES1D5
DD QD — TES1D4
TES1 — CK
CLR — CL

V1N
A30 — TES1D6

FDR P32
OD3 — DA QA — TES1D3
VSS — DB QB — ✕
OD1 — DC QC — TES1D1
OD0 — DD QD — TES1D0
TES1 — CK
CLR — CL

OD[1..0]

O59
V1N

J56
N2P
CLR

F16 C42
CLK2 — CK QA — H1
QB — H2
QC — H4
QD — H8
CL — {HCNT}
CLR

Four time slots available all the time for addressing.
0: – OBJBUFINIT high: Writing zeros to all data in the Object
       Data Buffer.
   – DMA high: Data copying from Object RAM to Object Buffer RAM.
1: Parsed object data copy to the frame buffers.
2: Master CPU access
3: Slave CPU access

OBFI	DMA	OH2	OH2	OH4	OH4
1	X	0	1	0	1
X	1	0	1	0	1

CPU Read/Write logic

Object Character RAM
Read/Write logic

Object RAM Read/Write logic