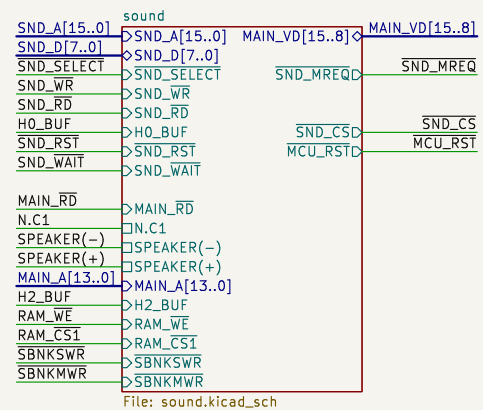
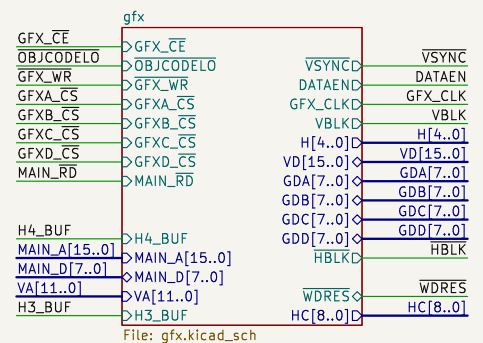
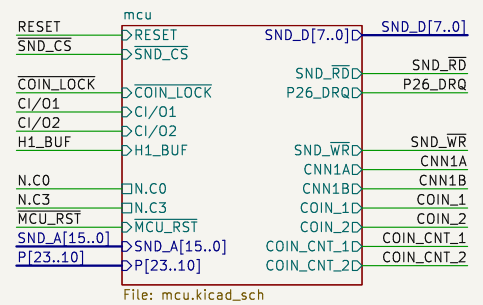
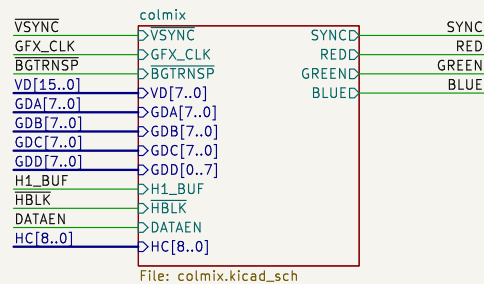
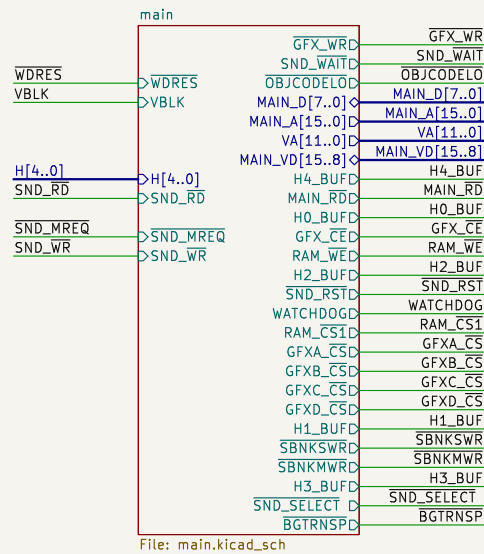
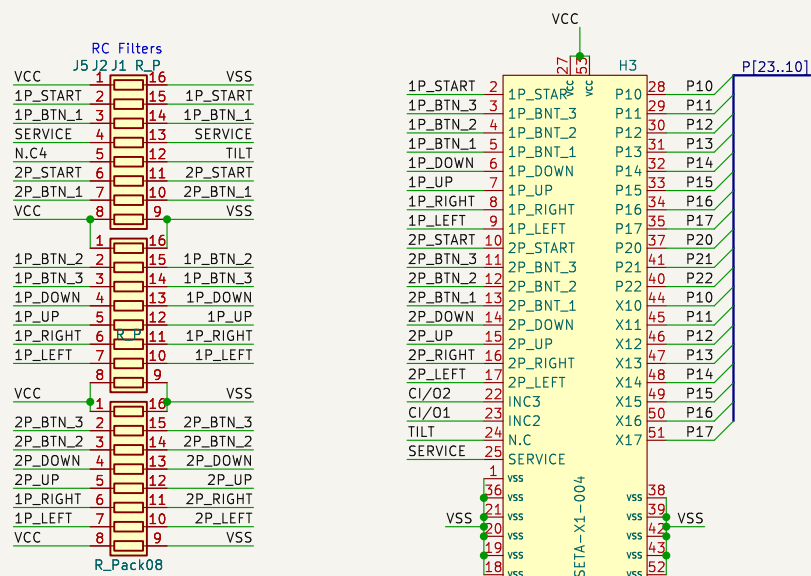


## CABINET I/O



JOTEGO

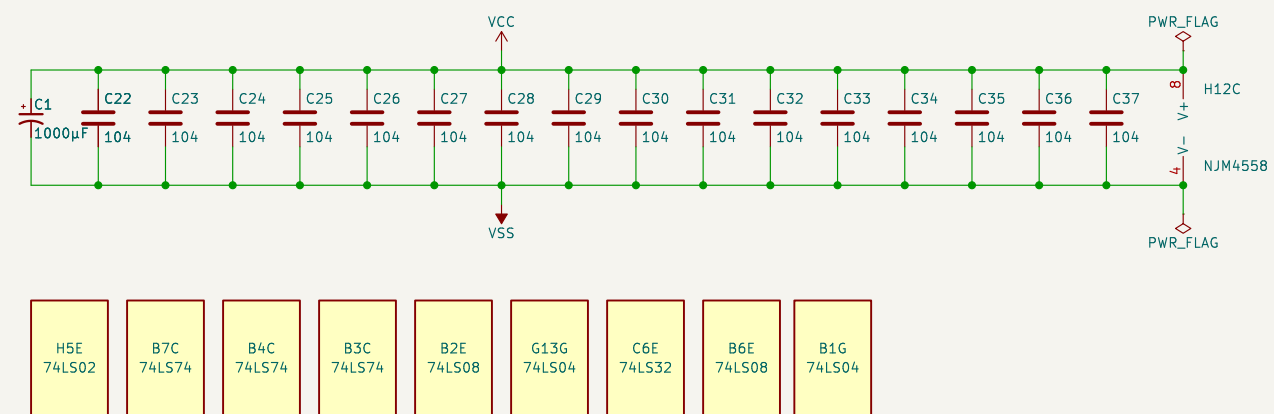
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File: exterm.kicad\_sch

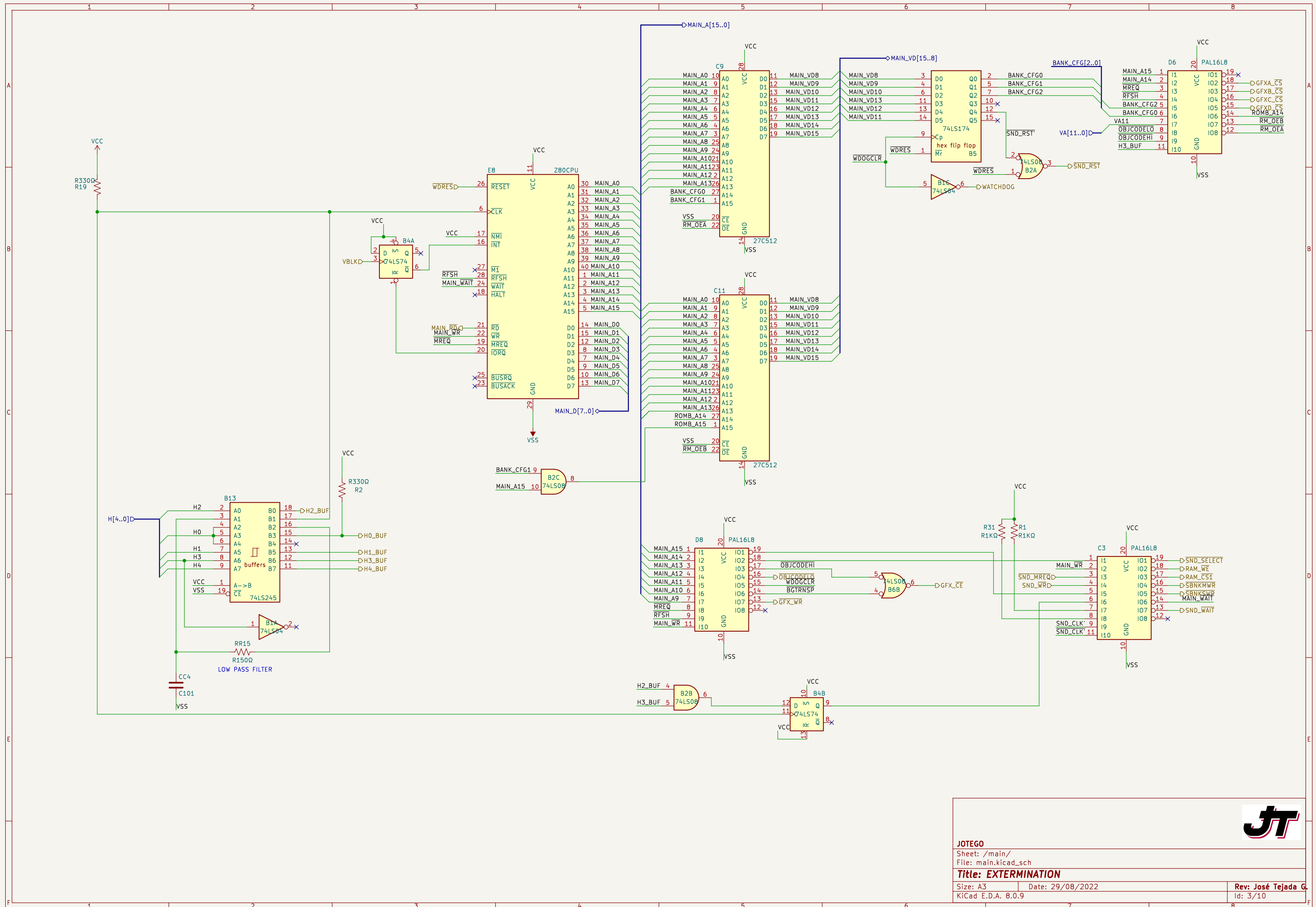
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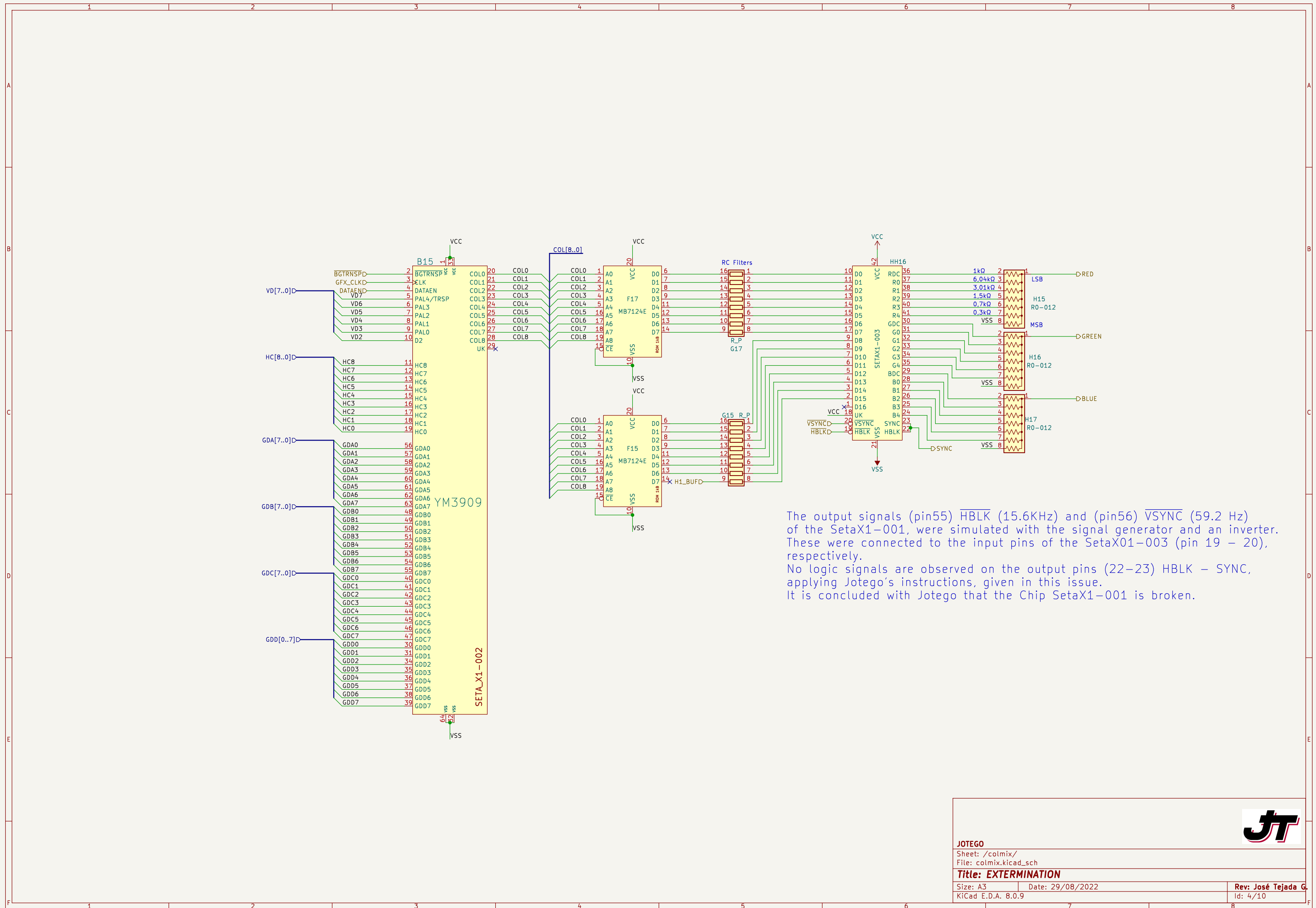
Size: A3  
Date: 29/08/2022

Rev: José Tejada G.  
Id: 1/10









The output signals (pin55)  $\overline{\text{HBLK}}$  (15.6KHz) and (pin56)  $\overline{\text{VSYNC}}$  (59.2 Hz) of the SetaX1-001, were simulated with the signal generator and an inverter. These were connected to the input pins of the SetaX01-003 (pin 19 – 20), respectively.

No logic signals are observed on the output pins (22-23)  $\text{HBLK} - \text{SYNC}$ , applying Jotego's instructions, given in this issue.

It is concluded with Jotego that the Chip SetaX1-001 is broken.



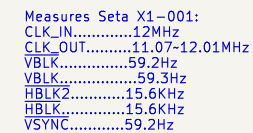
JOTEGO

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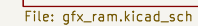
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Size: A3  
Date: 29/08/2022

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Observation: Pin 46 (HC0) does not correspond to the sequence of the HC[8..0] counter.



**JOTEGO**

Sheet: /watchdog/  
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**Title: EXTERMINATION**

Size: A3

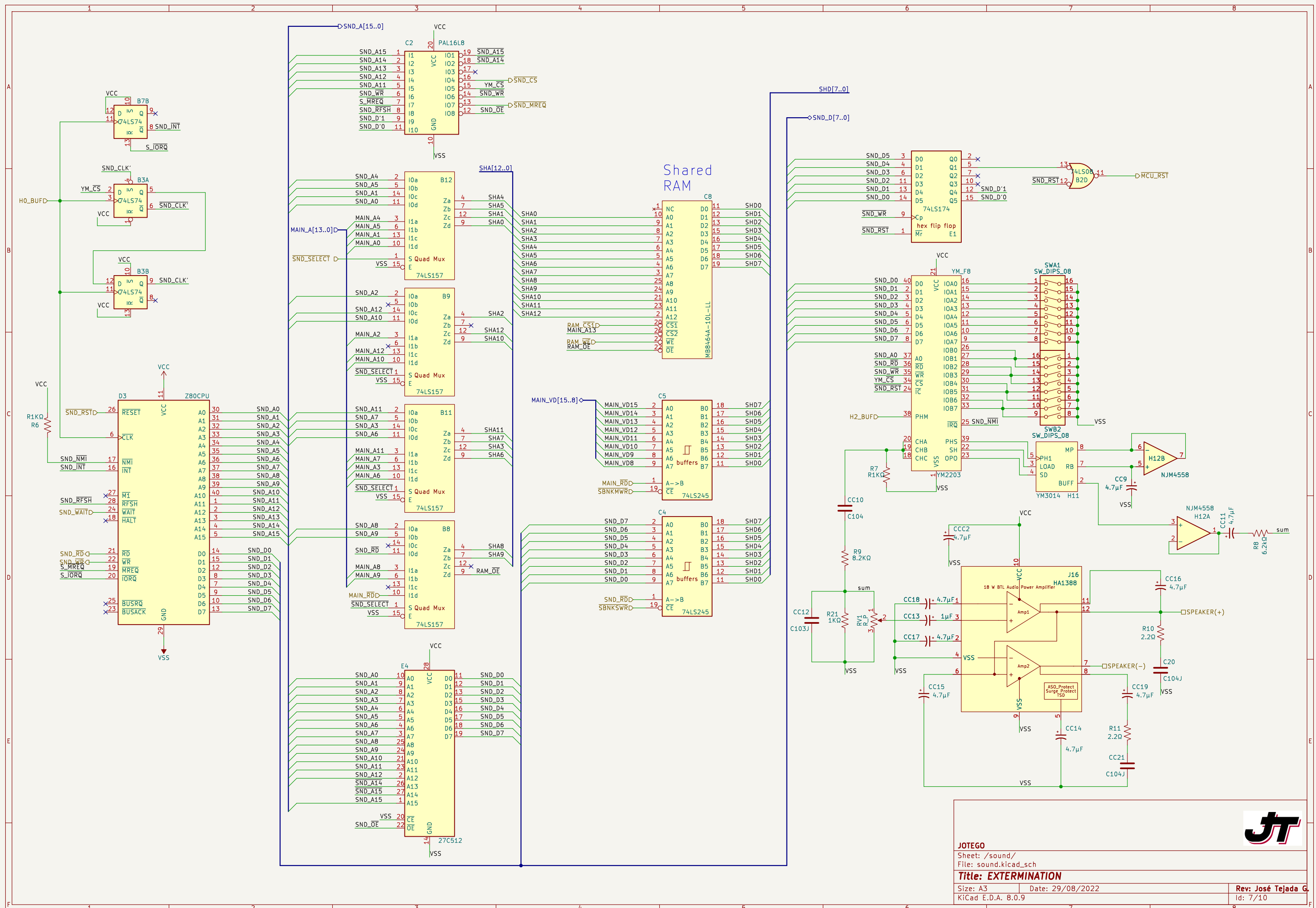
Date: 29/08/2022

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KiCad E.D.A. 8.0.9

Id: 6/10





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Id: 8/10





JOTEGO

Sheet: /gfx/gfx\_ram/  
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**Title: EXTERMINATION**

Size: A4 Date: 29/08/2022  
KiCad E.D.A. 8.0.9

Rev: José Tejada G.  
Id: 9/10



