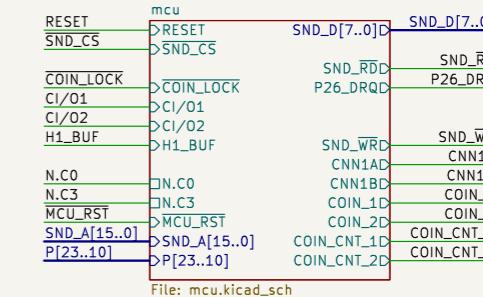
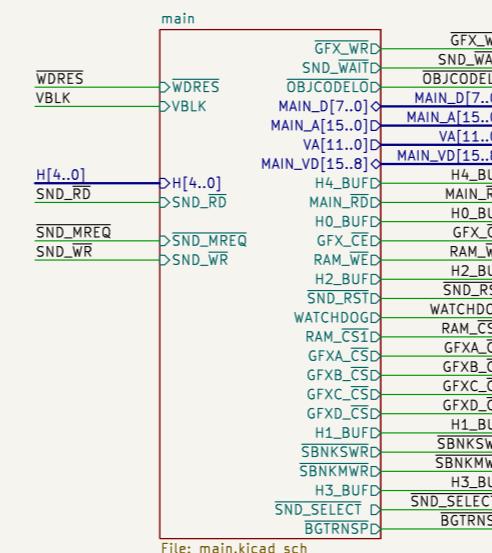
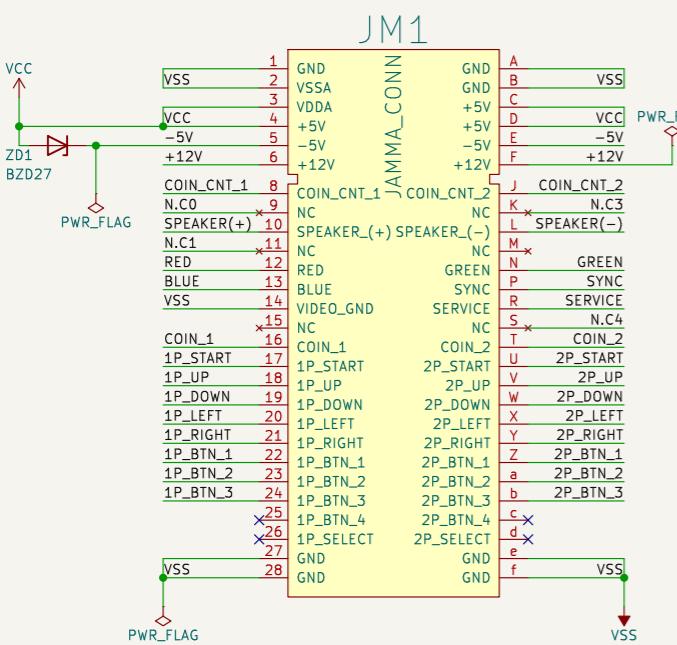
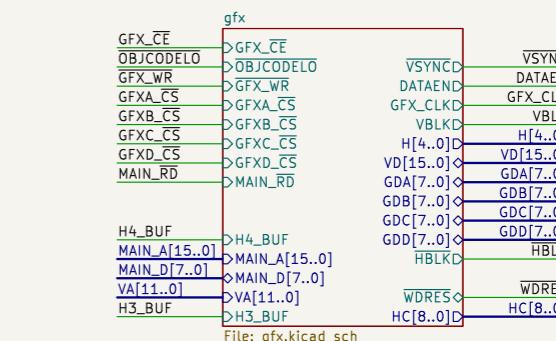


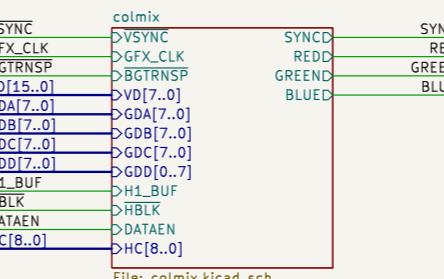
A



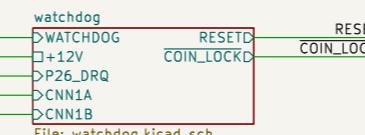
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B



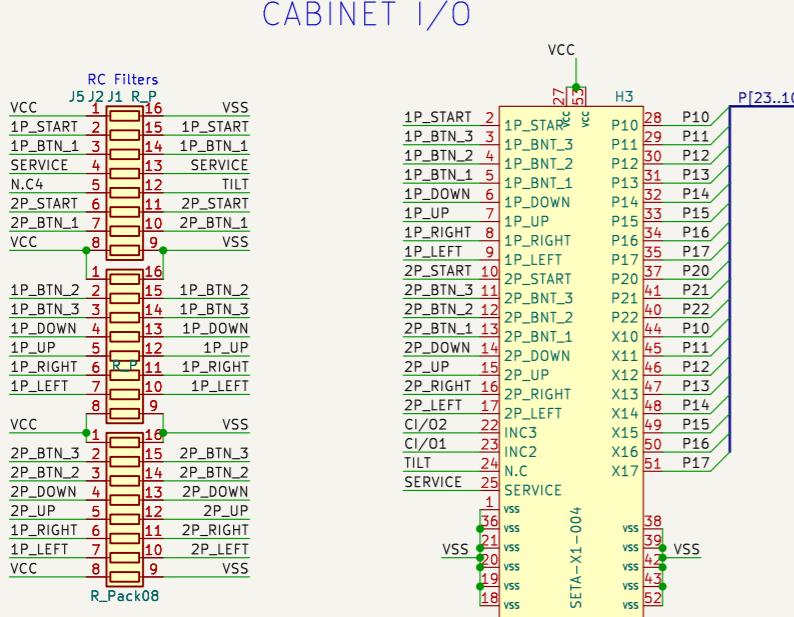
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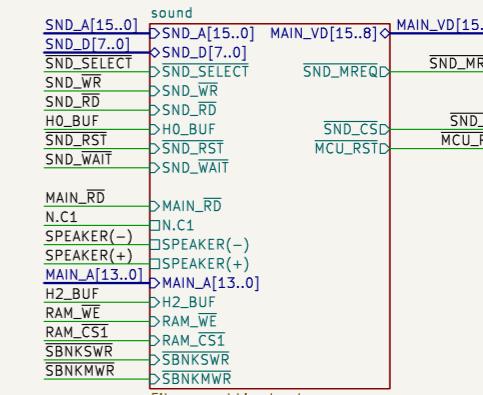
C



E



C



D



JOTEGO

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Title: EXTERMINATION

Size: A3 Date: 29/08/2022

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F

F

1 2 3 4 5 6 7 8

A

B

C

D

E

F



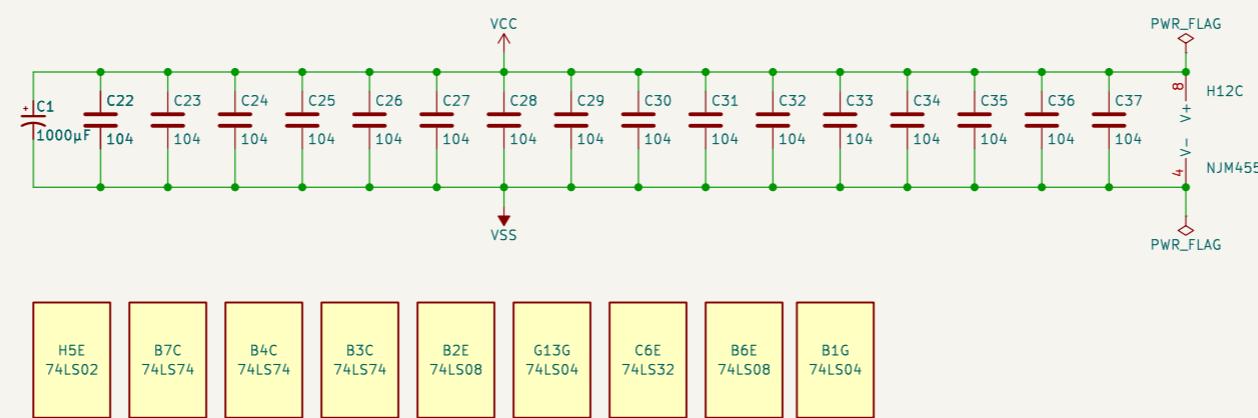
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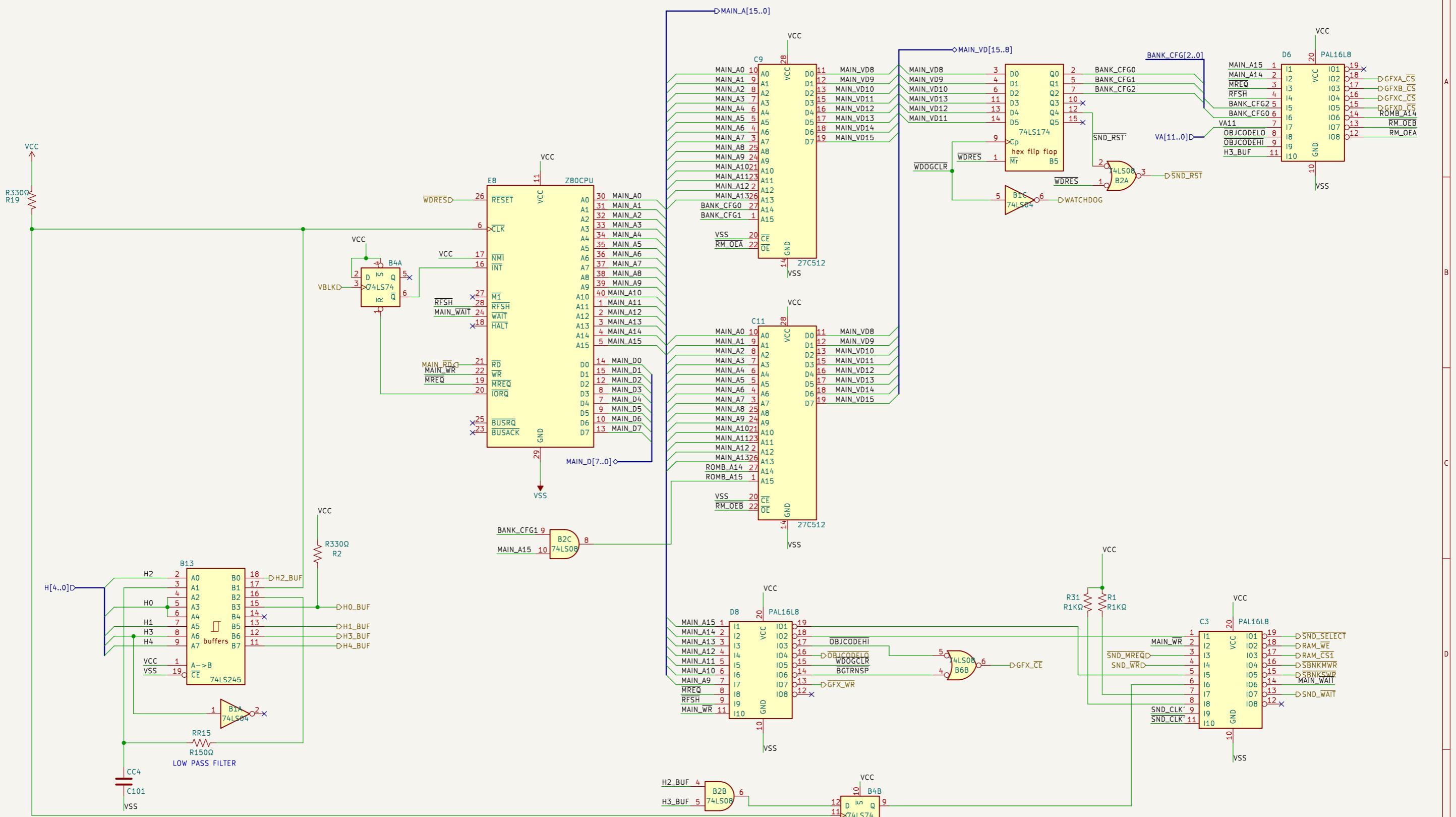
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1 2 3 4 5 6 7 8



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A

A

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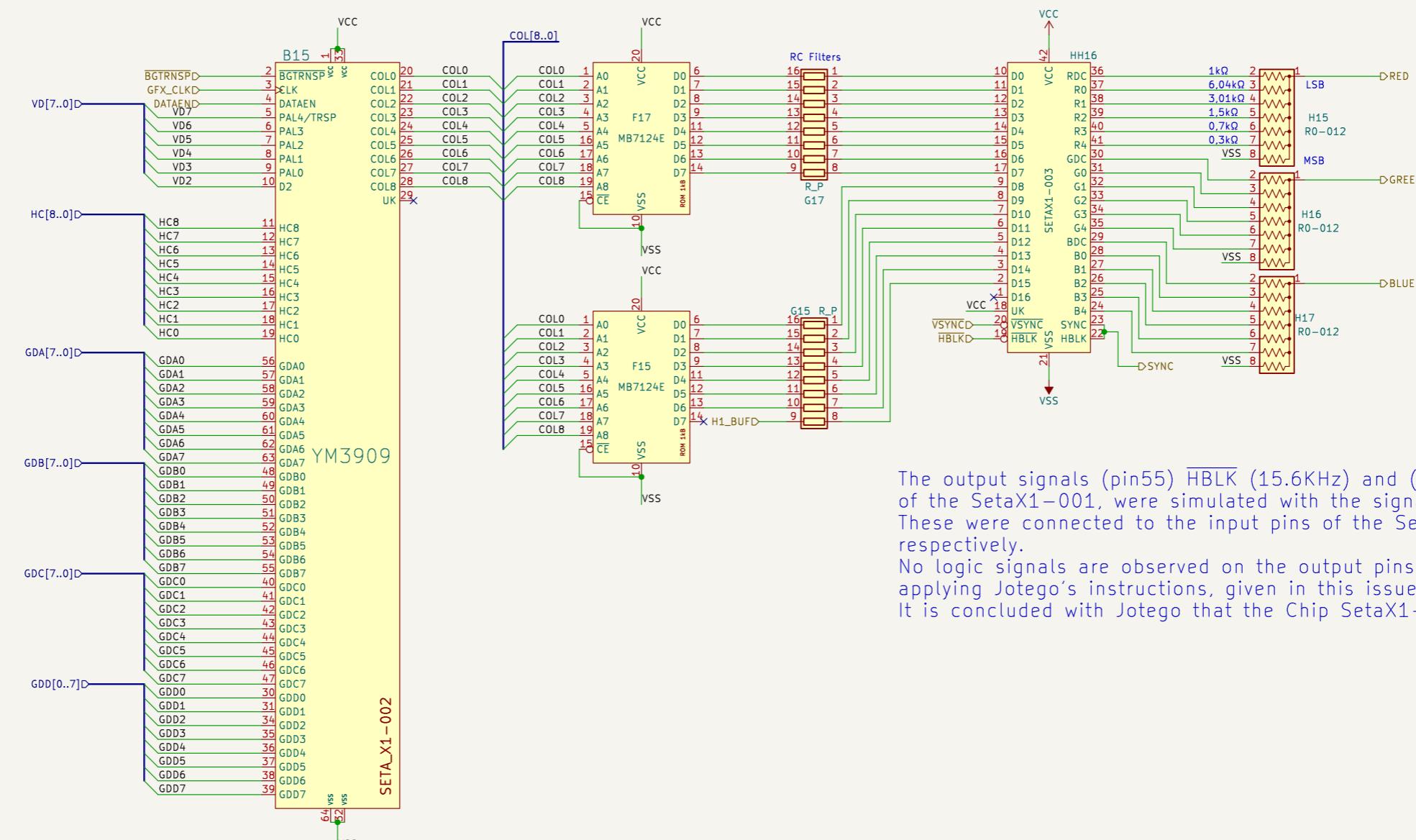
D

E

E

F

F



The output signals (pin 55) HBLK (15.6KHz) and (pin 56) VSYNC (59.2 Hz) of the SetaX1-001, were simulated with the signal generator and an inverter. These were connected to the input pins of the SetaX01-003 (pin 19 – 20), respectively.
 No logic signals are observed on the output pins (22–23) HBLK – SYNC, applying Jotego's instructions, given in this issue.
 It is concluded with Jotego that the Chip SetaX1-001 is broken.



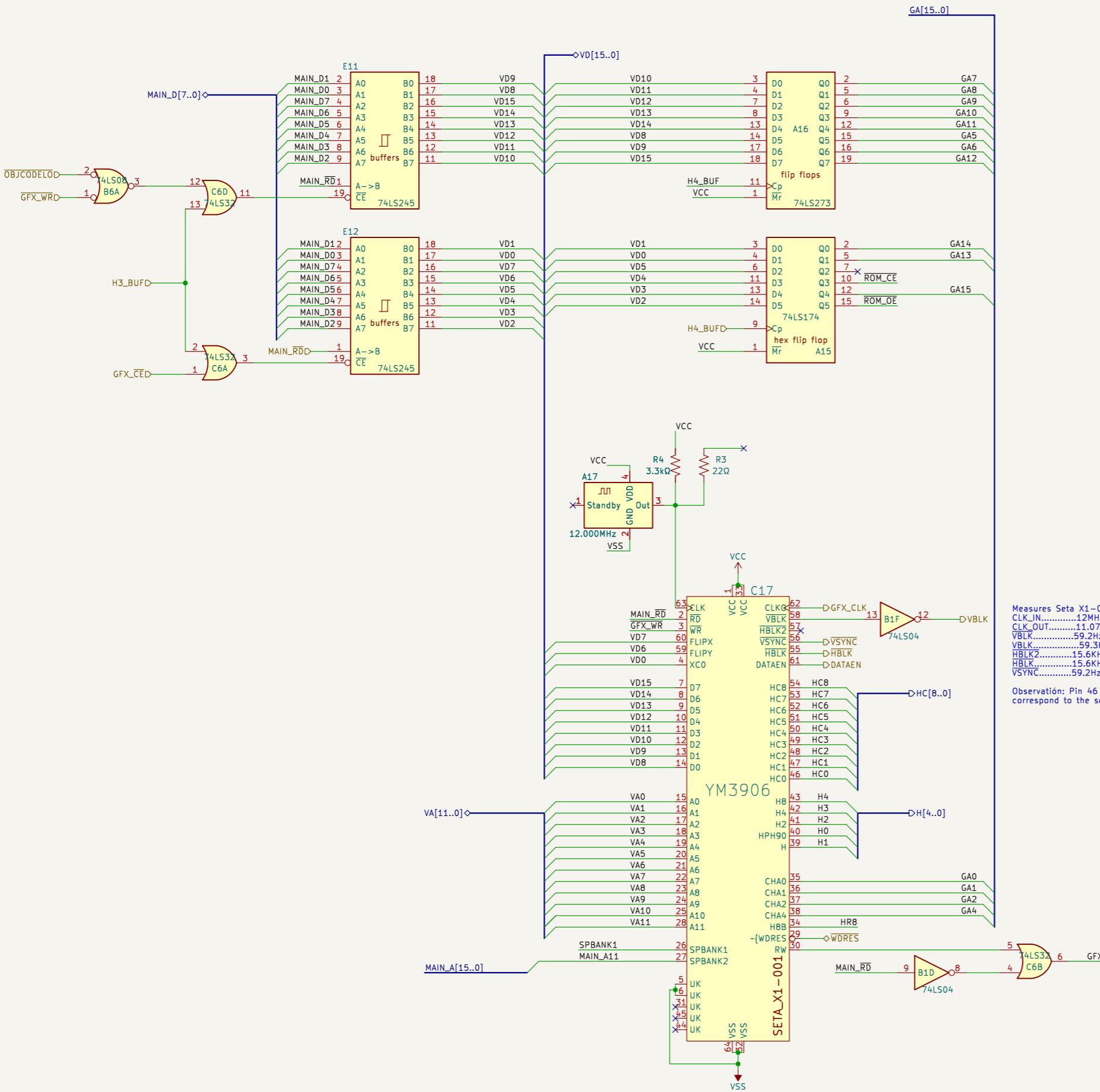
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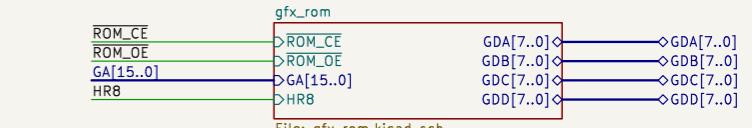


```

Measures Seta X1-001:
CLK_IN.....12MHz
CLK_OUT.....11.07-12.01MHz
VBLK.....59.2Hz
VBLK.....59.3Hz
HBLK2.....15.6KHz
HBLK.....15.6KHz
VSYNC.....50.2Hz

```

Observación: Pin 46 (HCO) does not correspond to the sequence of the HC[8.0] counter.



JOTEGO

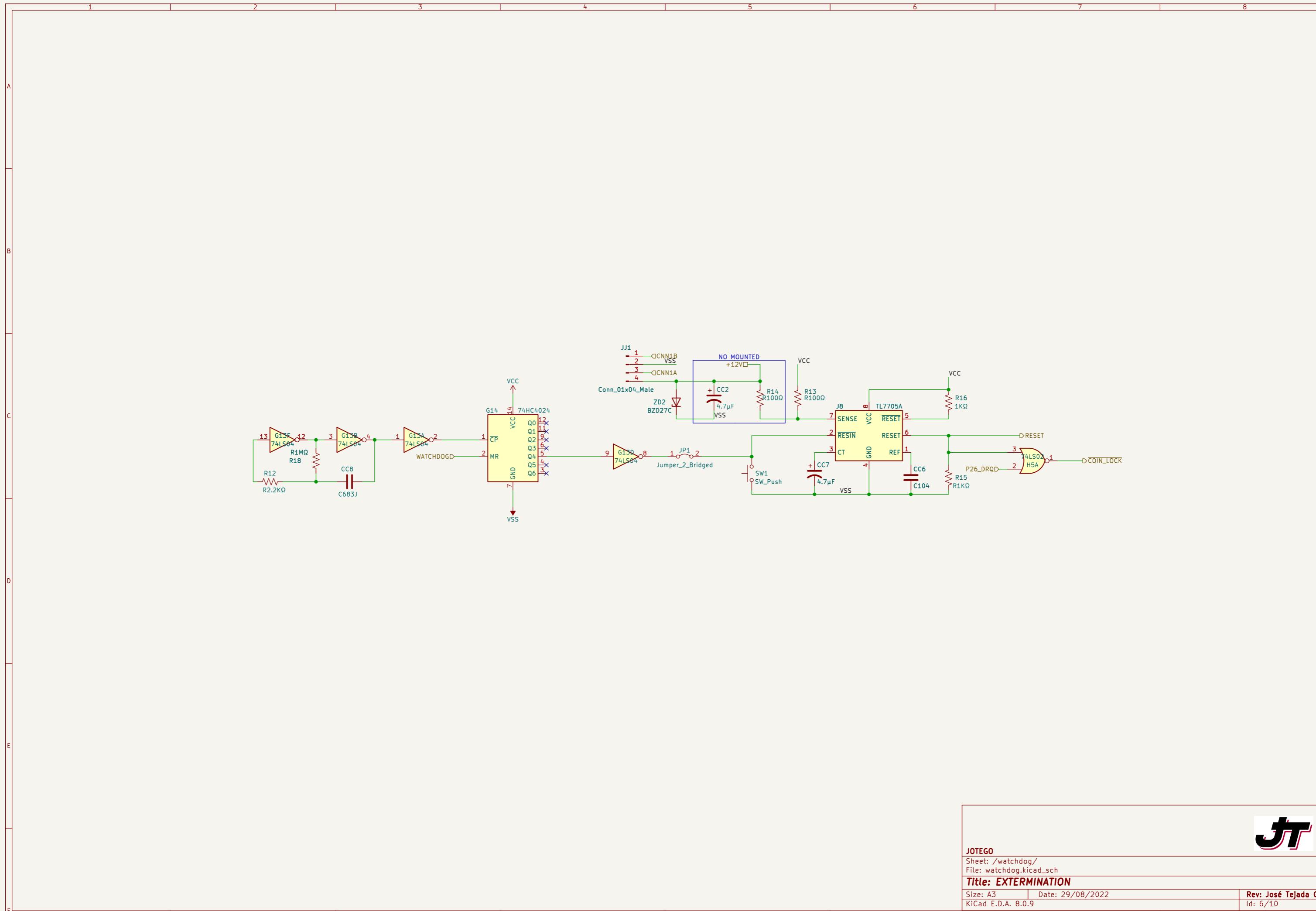
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Title: EXTERMINATION

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The JT logo consists of a stylized lowercase 't' and 'j' in black, with a red outline.

1 2 3 4 5 6 7 8



JOTEGO

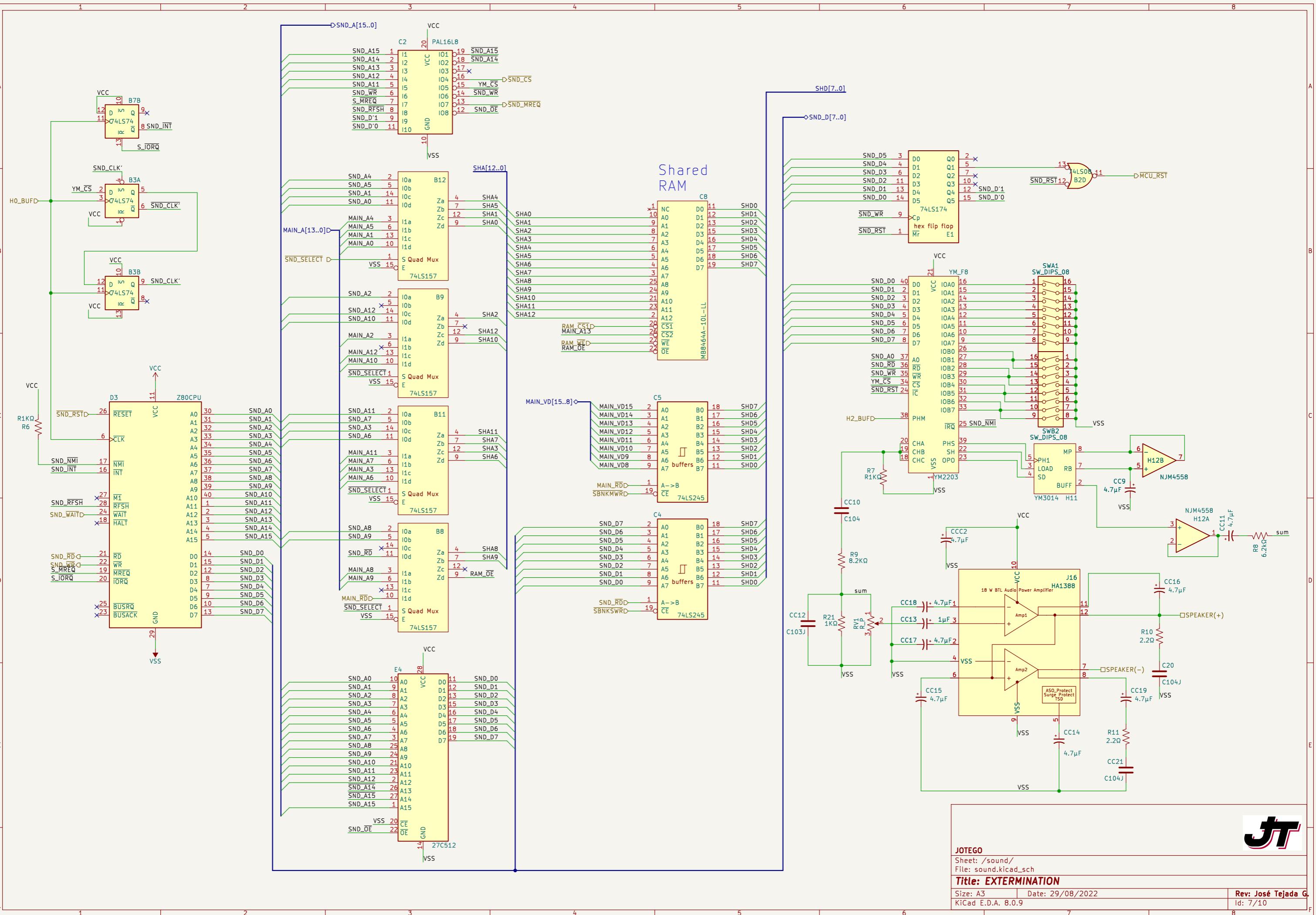
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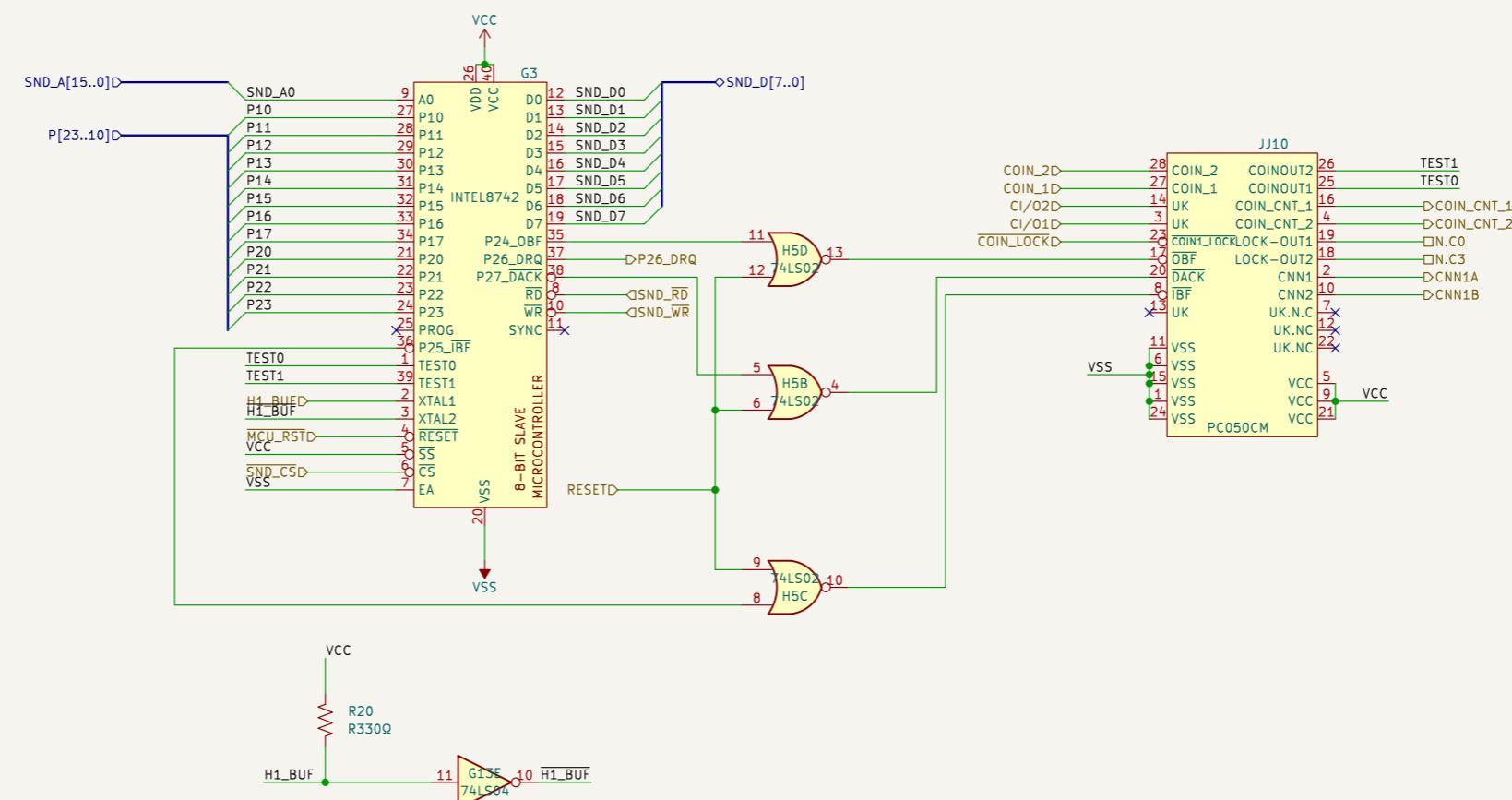
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JOTEGO

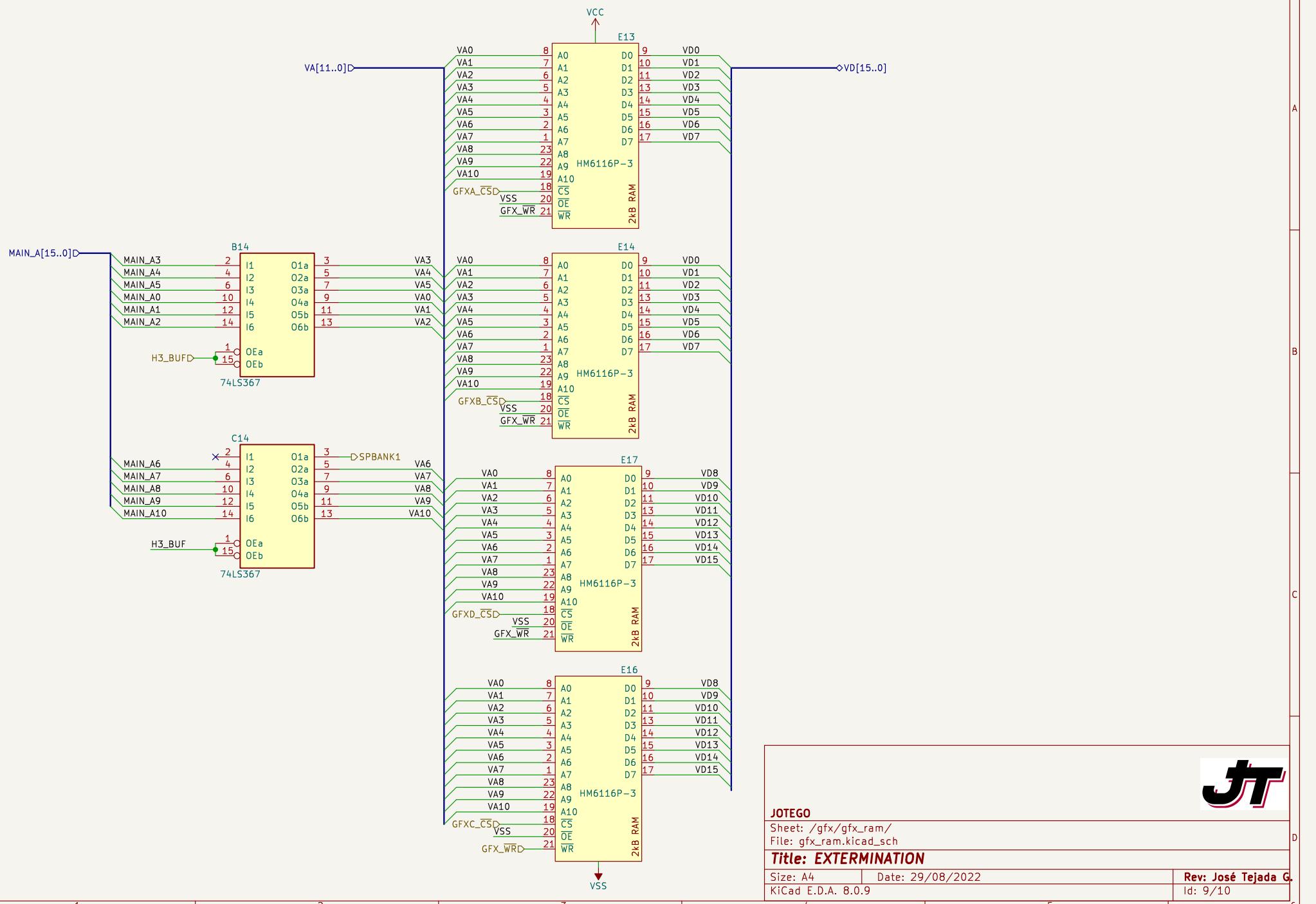
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JOTEGO

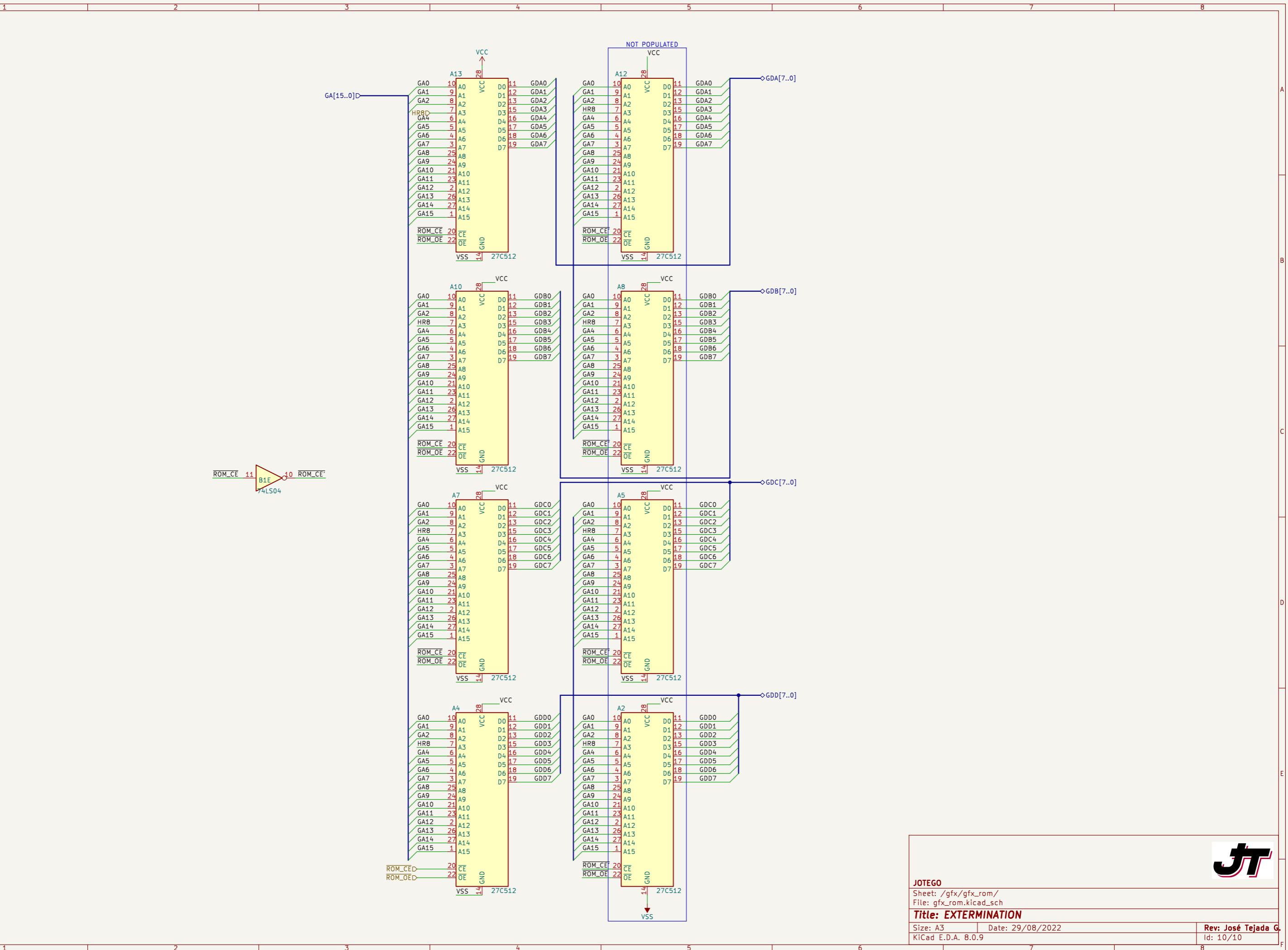
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Size: A4 Date: 29/08/2022
KiCad E.D.A. 8.0.9



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JOTEGO

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Title: EXTERMINATION

Size: A3 | Date: 29/08/2022
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