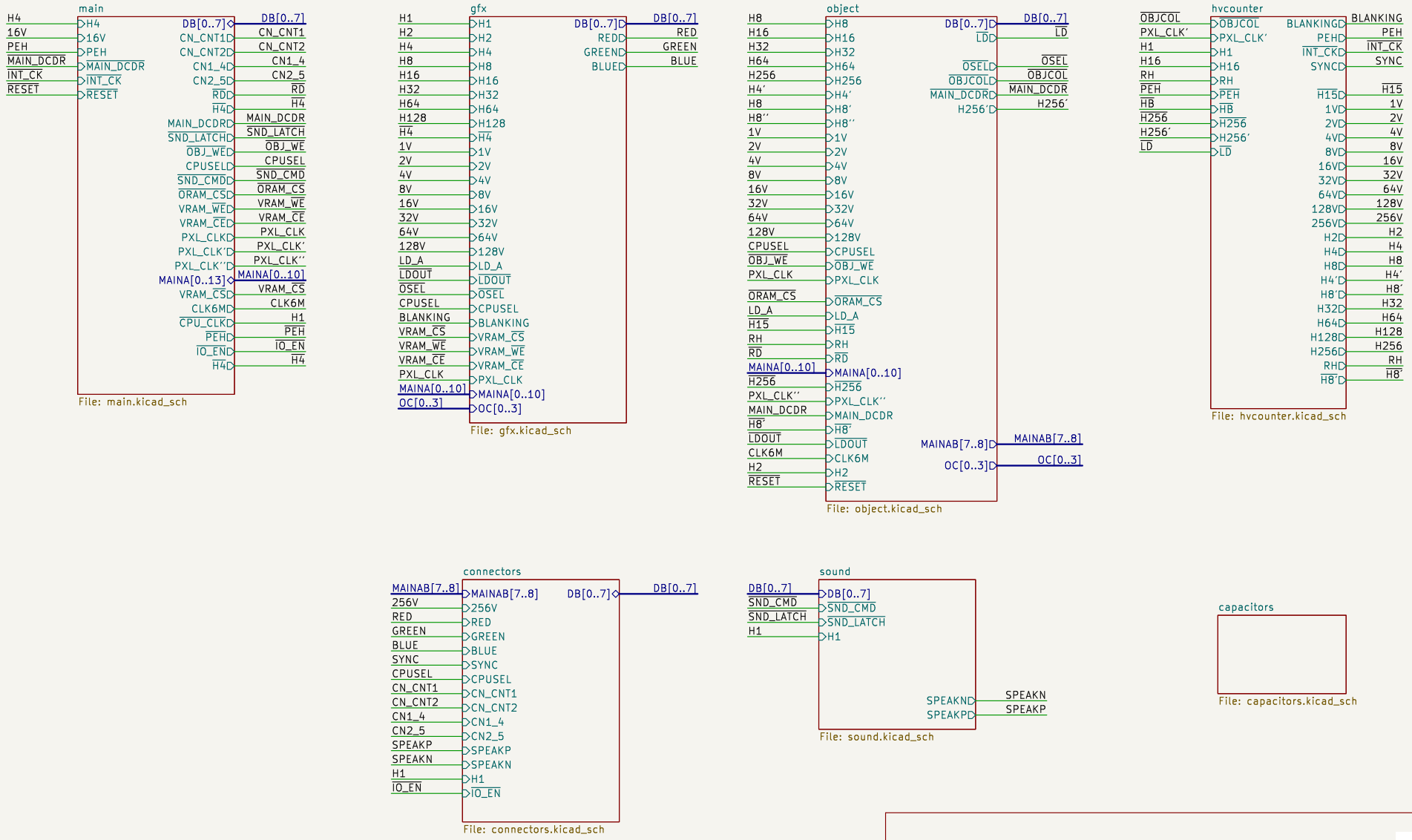

main
H4
16V
PEH
MAIN_DCDR
INT_CK
RESET
H4
16V
PEH
MAIN_DCDR
INT_CK
RESET
DB[0..7]
CN_CNT1
CN_CNT2
CN1_4
CN2_5
RD
H4
MAIN_DCDR
SND_LATCH
OBJ_WE
CPUSEL
SND_CMD
ORAM_CS
VRAM_WE
VRAM_CE
PXL_CLK
PXL_CLK'
PXL_CLK''
MAINA[0..10]
VRAM_CS
CLK6M
H1
PEH
IO_EN
H4
DB[0..7]
CN_CNT1
CN_CNT2
CN1_4
CN2_5
RD
H4
MAIN_DCDR
SND_LATCH
OBJ_WE
CPUSEL
SND_CMD
ORAM_CS
VRAM_WE
VRAM_CE
PXL_CLK
PXL_CLK'
PXL_CLK''
MAINA[0..10]
VRAM_CS
CLK6M
H1
PEH
IO_EN
H4
MAINA[0..13]
File: main.kicad_sch
gfx
H1
H2
H4
H8
H16
H32
H64
H128
H4
1V
2V
4V
8V
16V
32V
64V
128V
LD_A
LDOUT
OSEL
CPUSEL
BLANKING
VRAM_CS
VRAM_WE
VRAM_CE
PXL_CLK
MAINA[0..10]
OC[0..3]
H1
H2
H4
H8
H16
H32
H64
H128
H4
1V
2V
4V
8V
16V
32V
64V
128V
LD_A
LDOUT
OSEL
CPUSEL
BLANKING
VRAM_CS
VRAM_WE
VRAM_CE
PXL_CLK
MAINA[0..10]
OC[0..3]
DB[0..7]
RED
GREEN
BLUE
DB[0..7]
RED
GREEN
BLUE
File: gfx.kicad_sch
object
H8
H16
H32
H64
H256
H4'
H8
H8''
1V
2V
4V
8V
16V
32V
64V
128V
CPUSEL
OBJ_WE
PXL_CLK
ORAM_CS
LD_A
H15
RH
RD
MAINA[0..10]
H256
PXL_CLK''
MAIN_DCDR
H8'
LDOUT
CLK6M
H2
RESET
H8
H16
H32
H64
H256
H4'
H8
H8''
1V
2V
4V
8V
16V
32V
64V
128V
CPUSEL
OBJ_WE
PXL_CLK
ORAM_CS
LD_A
H15
RH
RD
MAINA[0..10]
H256
PXL_CLK''
MAIN_DCDR
H8'
LDOUT
CLK6M
H2
RESET
DB[0..7]
LD
OSEL
OBJCOL
MAIN_DCDR
H256'
MAINAB[7..8]
OC[0..3]
DB[0..7]
LD
OSEL
OBJCOL
MAIN_DCDR
H256'
MAINAB[7..8]
OC[0..3]
File: object.kicad_sch
hvcounter
OBJCOL
PXL_CLK'
H1
H16
RH
PEH
HB
H256
H256'
LD
OBJCOL
PXL_CLK'
H1
H16
RH
PEH
HB
H256
H256'
LD
BLANKING
PEH
INT_CK
SYNC
H15
1V
2V
4V
8V
16V
32V
64V
128V
256V
H2
H4
H8
H4'
H8'
H32
H64
H128
H256
RH
H8'
BLANKING
PEH
INT_CK
SYNC
H15
1V
2V
4V
8V
16V
32V
64V
128V
256V
H2
H4
H8
H4'
H8'
H32
H64
H128
H256
RH
H8'
File: hvcounter.kicad_sch
connectors
MAINAB[7..8]
256V
RED
GREEN
BLUE
SYNC
CPUSEL
CN_CNT1
CN_CNT2
CN1_4
CN2_5
SPEAKP
SPEAKN
H1
IO_EN
MAINAB[7..8]
256V
RED
GREEN
BLUE
SYNC
CPUSEL
CN_CNT1
CN_CNT2
CN1_4
CN2_5
SPEAKP
SPEAKN
H1
IO_EN
DB[0..7]
DB[0..7]
File: connectors.kicad_sch
sound
DB[0..7]
SND_CMD
SND_LATCH
H1
DB[0..7]
SND_CMD
SND_LATCH
H1
SPEAKND
SPEAKPD
SPEAKN
SPEAKP
File: sound.kicad_sch
capacitors
File: capacitors.kicad_sch
JOTEGO
Ping Pong
JOTEGO
Sheet: /
File: pingpong.kicad_sch
GX555
Title: Ping Pong
Size: A4
Date: 2022-03-28
Rev: J. Tejada
KiCad E.D.A. 8.0.9
Id: 1/11

MAIN PROGRAM ROM

VCC
A5 Z80CPU
RESET
3.07MHz
CPU_CLK
NMI
INT
M1
RFSH
WAIT
HALT
RD
WR
MREQ
IORQ
BUSRQ
BUSACK
4.7k R35
4.7k R34
MAINA0 MAINA1 MAINA2 MAINA3 MAINA4 MAINA5 MAINA6 MAINA7 MAINA8 MAINA9 MAINA10 MAINA11 MAINA12 MAINA13 MAINA14 MAINA15
D0 D1 D2 D3 D4 D5 D6 D7
GND
VSS
A6 27128
A7 27128
MAINA[0..13]
D[D0..7]
VPP
CE
OE
PGM
ROM1_CS
ROM0_CS

DB[0..7]
D5 KONAMI_UK
CPU_CLK 6.14MHz
CPUSEL 1.53MHz
CLK6M
A15
RD
WRB
EXT
WAIT
VRAM_CE
VRAM_WE
D8A 74LS32

74LS107
BASE_CLK 18.43MHz
RAW_CLK 6.14MHz
18432.00 KHz
XTA
A3
A_2 A2
BASE_CLK
CPU_CLK 3.07MHz
dual line inv
74LS368

74LS139
D7B decoder
D7A decoder
RFSH
MAINA15
MREQ
MAINA13
MAINA12
EXT
MAIN_DCDR
VRAM_CE
ORAM_CS

74LS174 hex flip flop
C4
IO_WR
RESET
CN2_5
CN1_4
IRQCLR
NMICLR

B4 74xx74
INT_CK
INT Triggers at V=224
NMI
16V

74xx04
PEH from counters
H4
CPUSEL
PEH
PXL_CLK
PXL_CLK'
PXL_CLK''
74LS74
3.06MHz
CPU_CLK

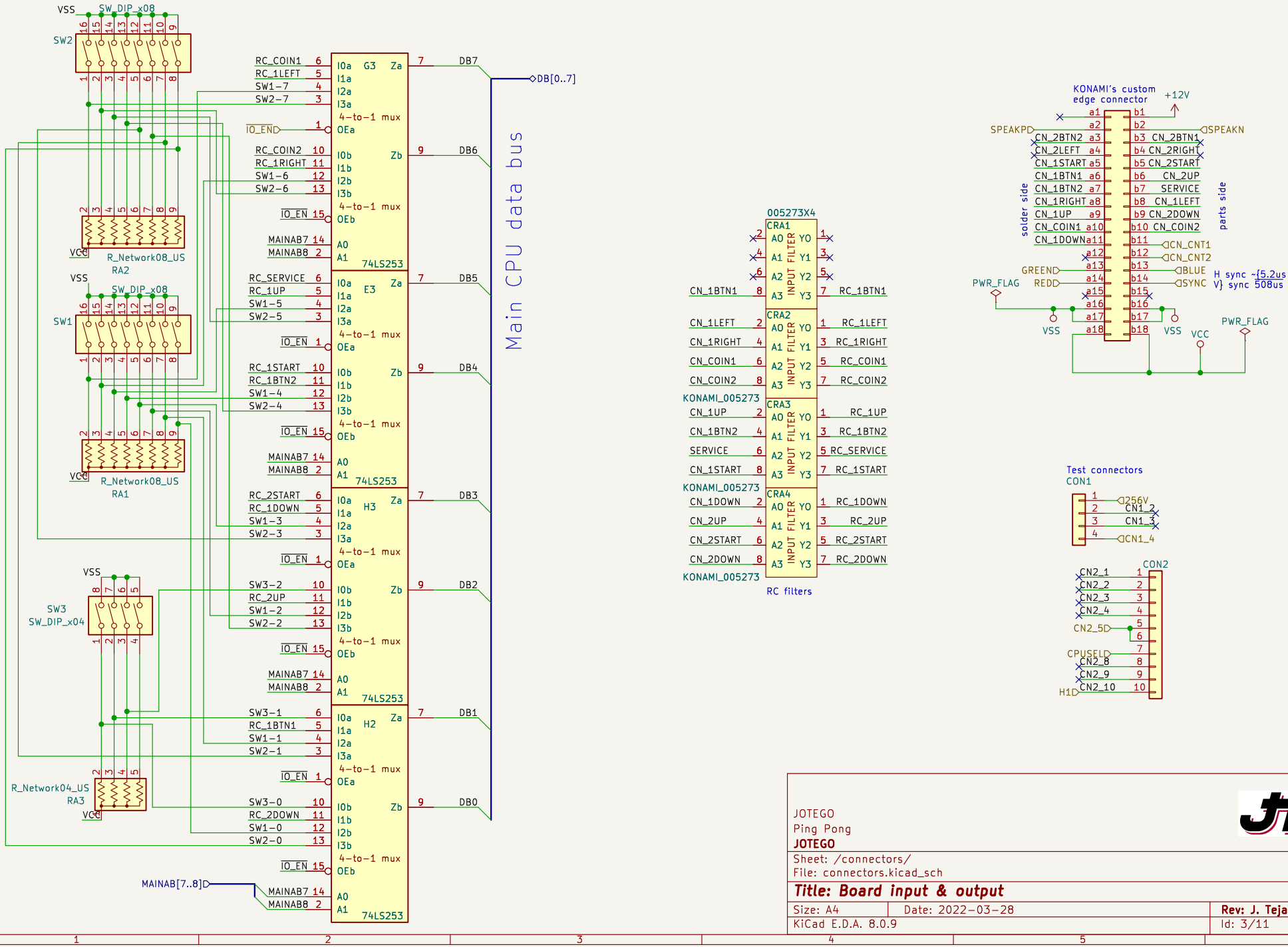
C3 address flip flop 74LS138
MAINA9
MAINA10
WRB
MAINA13
IO_WR
SND_LATCH
SND_CMD
IO_EN

OBJ_WE
ROM0_CS 0000-3FFF
ROM1_CS 4000-7FFF
D9A 74LS00
D8D D8B 74LS32
H8C 74LS08

CA2 47uF
R9 47K
R10 1.2K
CC1 475T
R7 10K
R12 120
R4 6.8K
R2 150
TR2 2SD400
TR1 2SC2330
TR4 2SC2330
TR3 2SD400
R16 120
DD2 10DI
DD1 10DI
CN_CNT2
CN_CNT1
74LS07 B2C
74LS07 B2B

JP1 Jumper
F10B 74LS14
B2F 74LS07
R3 4.7K
R6 30K
R1 100K
R25 51K
CC3 106E_16V
C54 102C
R17 100K
TA7805 BIAS OUT COMP INPUT GND ADJ RESET TC CK

JOTEGO
Ping Pong
JOTEGO
Sheet: /main/
File: main.kicad_sch
Title: CPU & address decoders
Size: A3 | Date: 2022-03-28 | **Rev: J. Tejada**
KiCad E.D.A. 8.0.9 | Id: 2/11

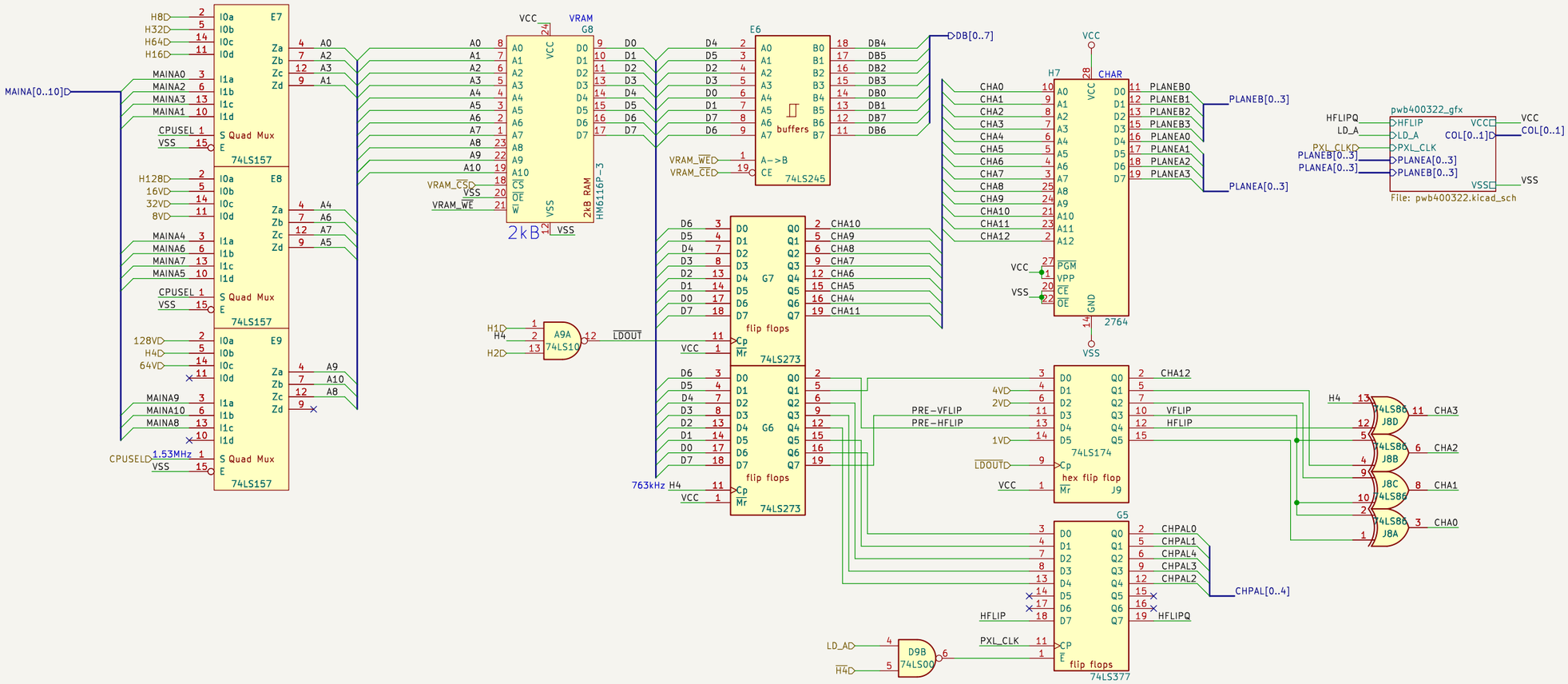


JOTEGO
Ping Ping
JOTEGO

Sheet: /connectors/
File: connectors.kicad_sch

Title: Board input & output

Size: A4	Date: 2022-03-28	**Rev: J. Tejada**
KiCad E.D.A. 8.0.9		Id: 3/11

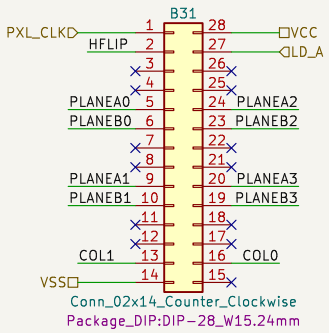


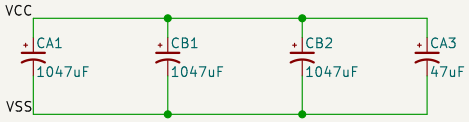
JOTEGO
Ping Pong
JOTEGO

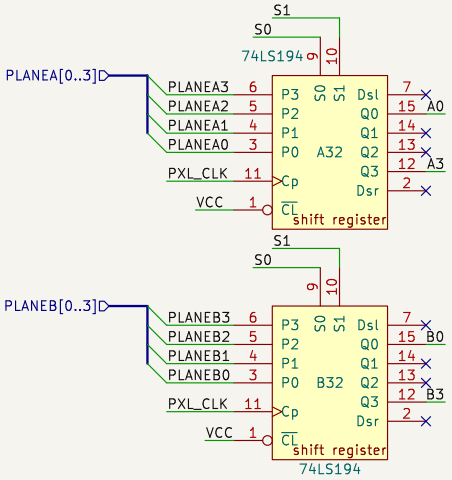
Sheet: /gfx/
File: gfx.kicad_sch

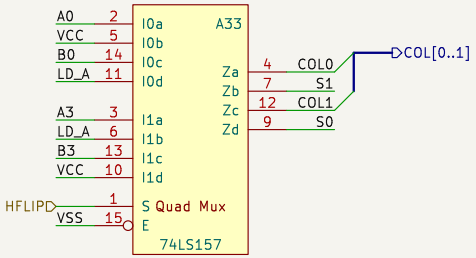
Title: Character generator

Size: A3	Date: 2022-03-28	**Rev: J. Tejada**
KiCad E.D.A. 8.0.9		Id: 4/11









This is a small board soldered to a DIP-28 footprint. It appears twice in the design

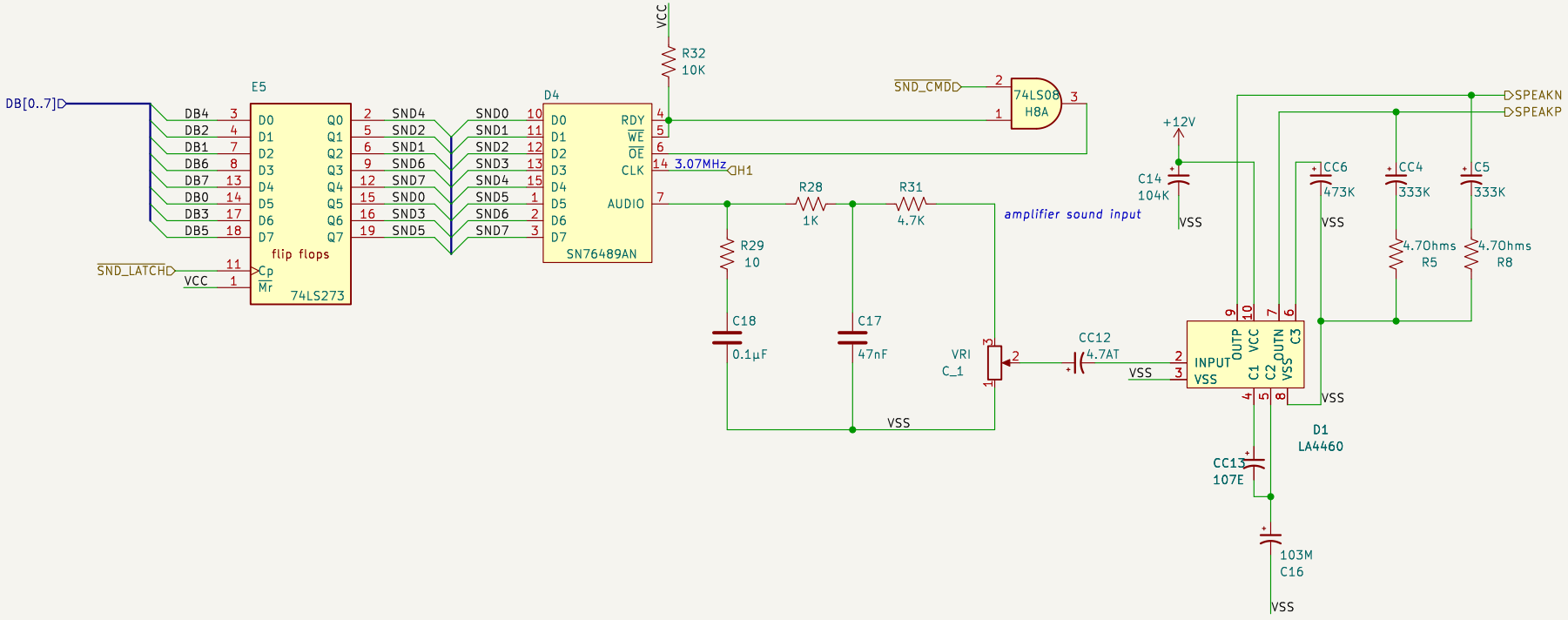
PWB-400322

JOTEGO
Ping Pong
JOTEGO

Sheet: /gfx/pwb400322_gfx/
File: pwb400322.kicad_sch

Title: Pixel shift register

Size: A4	Date: 2022-03-28	**Rev: J. Tejada**
KiCad E.D.A. 8.0.9		Id: 5/11



JOTEGO
Ping Pong
JOTEGO

Sheet: /sound/
File: sound.kicad_sch

Title: Sound generator

Size: A4	Date: 2022-03-28	**Rev: J. Tejada**
KiCad E.D.A. 8.0.9		Id: 6/11

OBJRAM

MAINA[0..10]

192kHz H16
781kHz H4
385kHz H8
96kHz H32
MAINA2 MAINA0 MAINA1 MAINA3
CPUSEL VSS
74LS157 (S Quad Mux)

16.1kHz H256
47.6kHz H64
16.1kHz RHD
MAINA6 MAINA4 MAINA5 MAINA7
CPUSEL VSS
74LS157 (S Quad Mux)

VSS
MAINA10 MAINA9 RDD MAINA8
1.54MHz CPUSEL VSS
74LS157 (S Quad Mux)

VCC
A8 HM6116P-3
AA0 AA1 AA2 AA3 AA4 AA5 AA6 AA7 AA8 AA9 AA10
VSS OEB OBJ_WE
DA0 DA1 DA2 DA3 DA4 DA5 DA6 DA7
2kB RAM OBJECT TABLE

24 objects read
in order from
the first 24x4 bytes

A10 74LS245 buffers
DA0 DA1 DA2 DA3 DA4 DA5 DA6 DA7
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7
DB[0..7]
OBJ_WE1
ORAM_CS

DA1 DA3 DA5 DA7 DA6 DA4 DA2 DA0
H15D VCC
E11 74LS273 flip flops
ATTR1 ATTR3 ATTR5 ATTR7 ATTR6 ATTR4 ATTR2 ATTR0

PRE_LINE HFLIP ATTR4 ATTR0 ATTR1 ATTR2 ATTR3
PXL_CLK OBJCOL
G11 74LS377 flip flops
LINECS HFLIP' PAL4 PAL0 PAL1 PAL2 PAL3

COL[0..1]
COL0 COL1 PAL0 PAL1 PAL2 PAL3 VSS
J11 TBP24S10N Color PROM
A0 A1 A2 A3 A4 A5 A6 A7 G2 G1 Q0 Q1 Q2 Q3
IC3 IC2 IC1 IC0
IC[0..3]

E10 74LS367
ATTR6 ATTR7 MAINA8 MAINA7
H8'D VSS
DN6 (hflip) DN7 (vflip) MAINAB8 MAINAB7
MAINAB[7..8]

DA7 DA5 DA3 DA1 DA0 DA2 DA4 DA6
H8' H8''
A11 74LS374 3-state flip flops
DN7 DN5 DN3 DN1 DN0 DN2 DN4 DN6

A12 KONAMI_503 V/HFLIP XORed
DN7 DN6 DN5 DN4 DN3 DN2 DN1 DN0
128V 64V 32V 16V 8V 4V 2V 1V
OBJV8 OBJH8 OBJH4 OBJV4 OBJV2 OBJV1
128V OBJDATA 64V OBJCOL 32V HFLIP 16V LINE_CS 8V 4V 2V 1V
(input) H8 H4 LD
17383kHz H8' 16766kHz H4'
OBJ5 OBJ4 OBJ3 OBJ2 OBJ1 OBJ0
OBJDATA OBJCOL HFLIP PRE_LINE

C12 2764 8kB
OBJ0 OBJ1 OBJ2 OBJ3 OBJ4 OBJ5 OBJ6 OBJ7 OBJ8 OBJ9 OBJ10 OBJ11 OBJ12
VCC VSS OE_M
PGM VPP CE OE GND
OBJD0 OBJD1 OBJD2 OBJD3 OBJD4 OBJD5 OBJD6 OBJD7
OBJD[0..7]

DA6 DA2 DA3 DA4 DA5 DA0 DA1 DA7
C13 flip flops 74LS273
OBJ12 OBJ8 OBJ9 OBJ10 OBJ11 OBJ6 OBJ7 OBJ13
OBJDATA

H9A 74LS74
ATTR5 OE_OF OE_M

C11 27128 16kB ONLY FOOTPRINT
OBJ0 OBJ1 OBJ2 OBJ3 OBJ4 OBJ5 OBJ6 OBJ7 OBJ8 OBJ9 OBJ10 OBJ11 OBJ12 OBJ13
VCC VSS OE_OF
PGM VPP CE OE GND
OBJD0 OBJD1 OBJD2 OBJD3 OBJD4 OBJD5 OBJD6 OBJD7

OBJD[4..7] OBJD[0..3] PXL_CLK HFLIP LD_A
pwb400322 (PLANEA[0..3] PLANEB[0..3] PXL_CLK HFLIP LD_A VCC COL[0..1] VSS)
File: pwb400322.kicad_sch

PXL_CLK'' DA[0..7] LINECS H2 LD OBJCOL MAIN_DCDR H8' LDOUT H256 CLK6M IC[0..3] RESET
linebuffer (PXL_CLK'' DA[0..7] LINECS H2 LD OBJCOL MAIN_DCDR H8' LDOUT H256 CLK6M IC[0..3] RESET
OC[0..3] OSEL H256 H8'' LD_A H256' MAIN_DCDR)
OC[0..3] OSEL H256 H8'' LD_A H256' MAIN_DCDR
File: linebuffer.kicad_sch

JOTEGO
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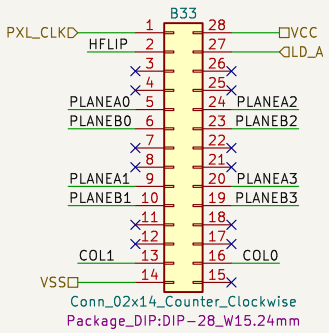
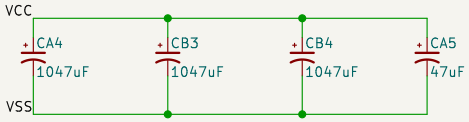
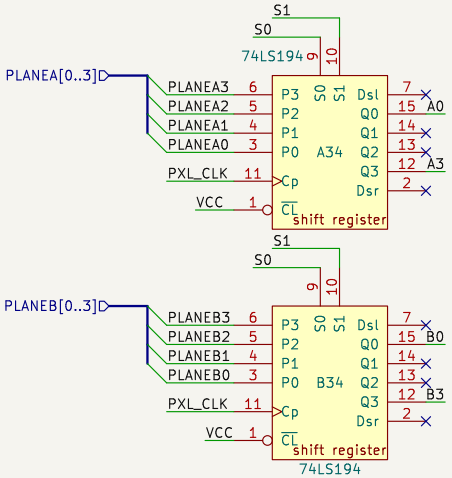
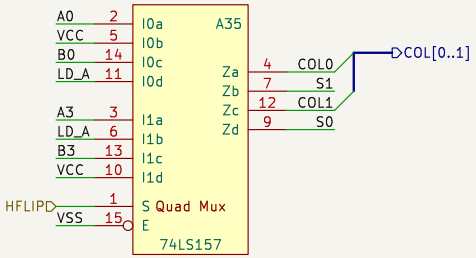
Sheet: /object/		
File: object.kicad_sch		
Title: Object generator		
Size: A3	Date: 2022-03-28	**Rev: J. Tejada**
KiCad E.D.A. 8.0.9		Id: 7/11









This is a small board soldered to a DIP-28 footprint. It appears twice in the design

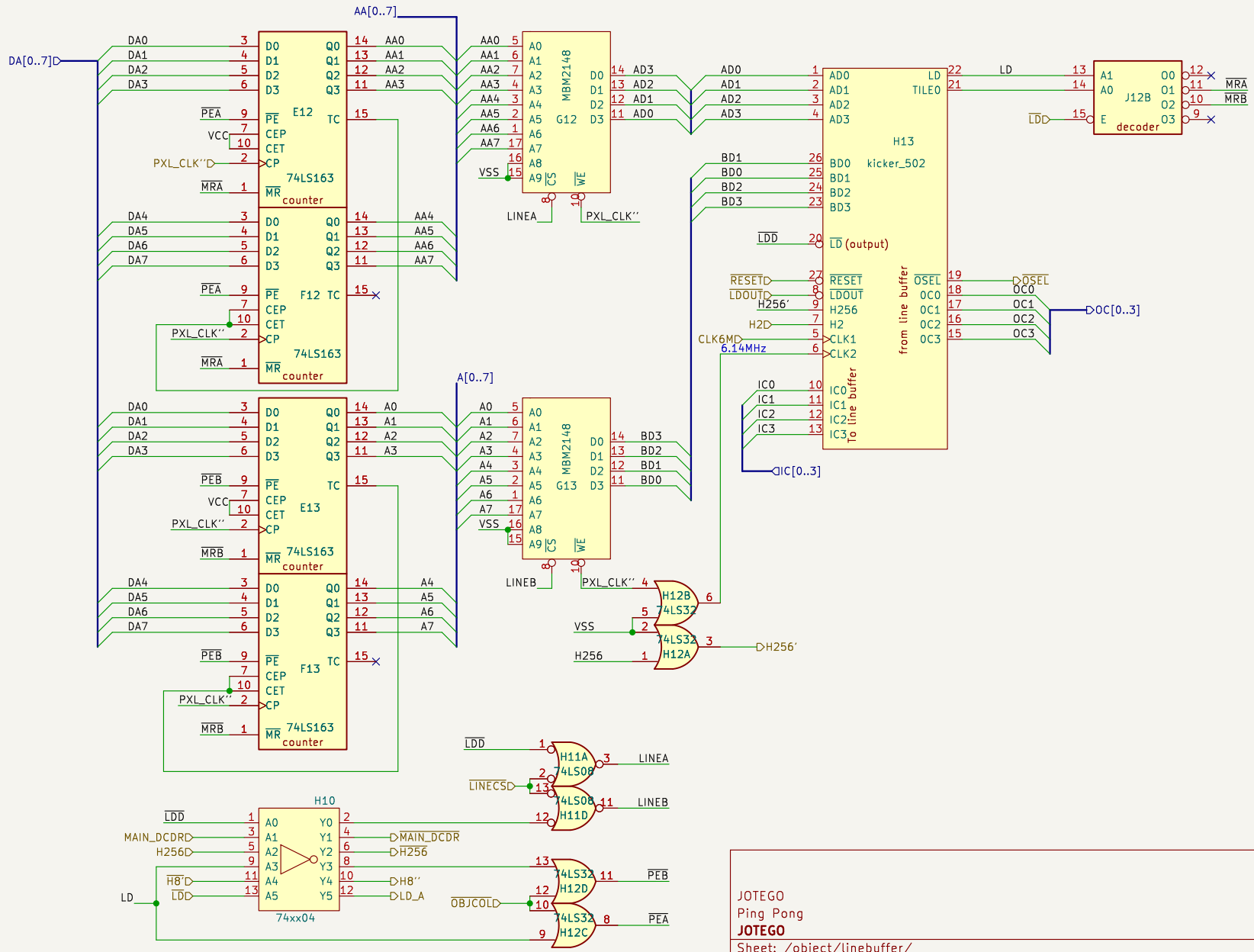
PWB-400322

JOTEGO
Ping Pong
JOTEGO

Sheet: /object/pwb400322/
File: pwb400322.kicad_sch

Title: Pixel shift register

Size: A4	Date: 2022-03-28	**Rev: J. Tejada**
KiCad E.D.A. 8.0.9		Id: 8/11

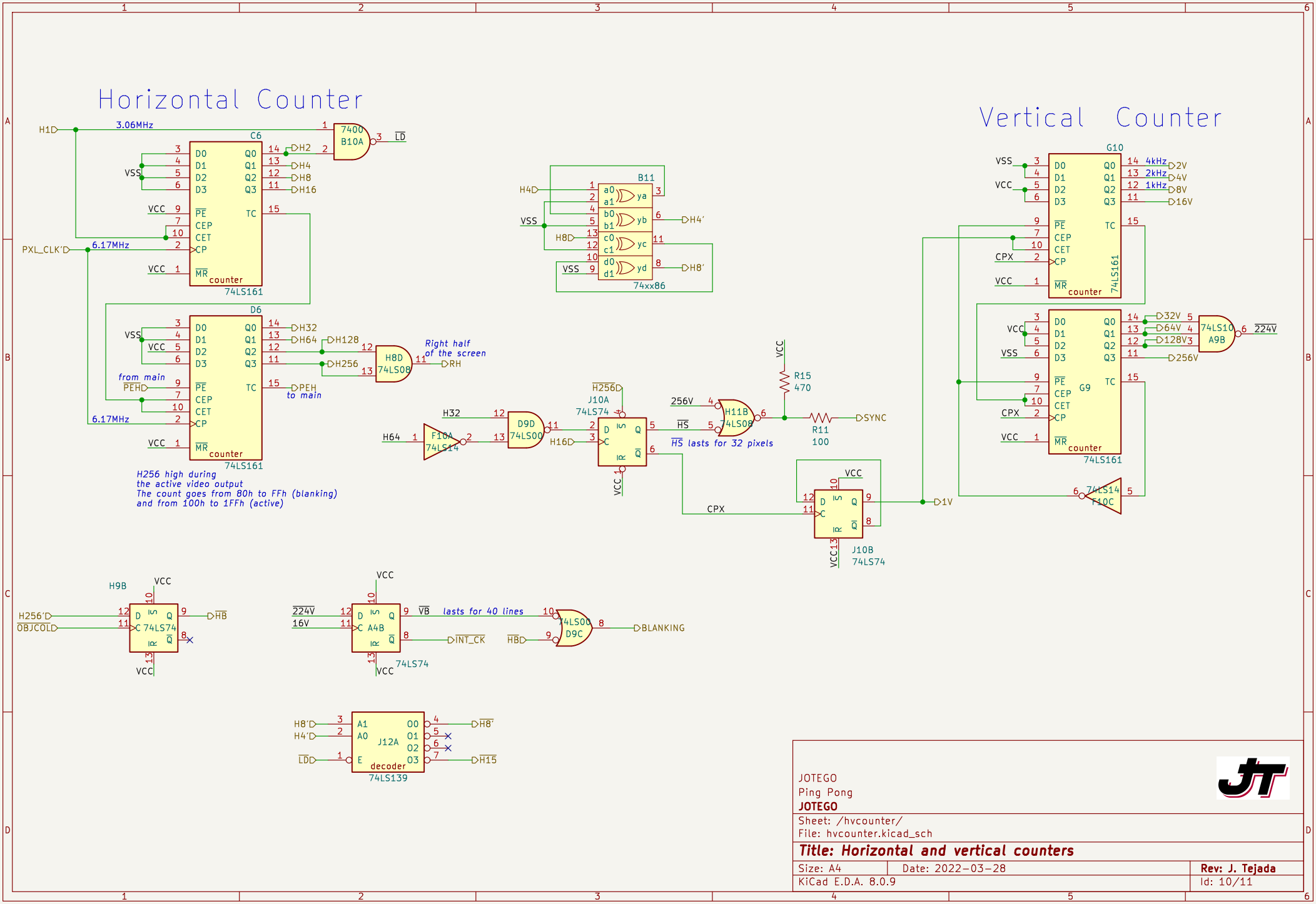


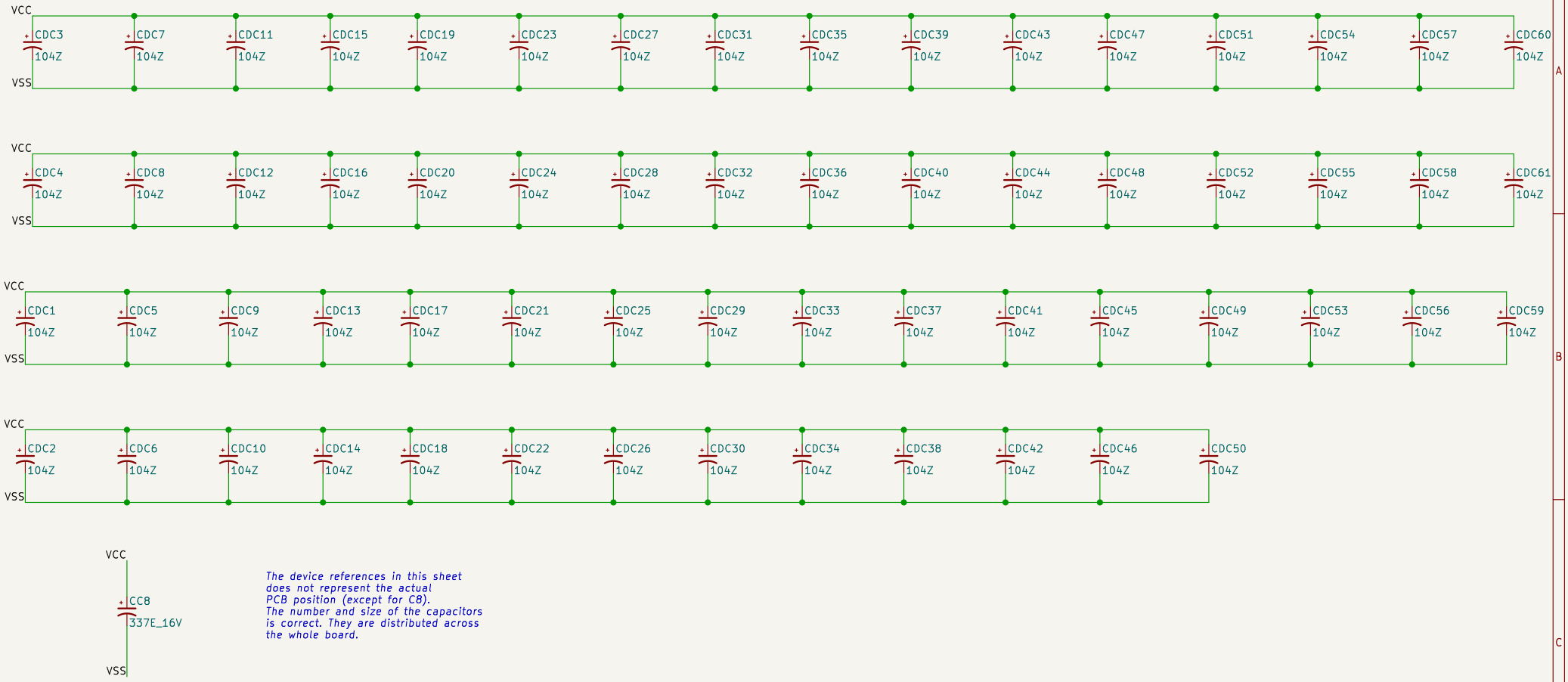
JOTEGO
Ping Pong
JOTEGO

Sheet: /object/linebuffer/
File: linebuffer.kicad_sch

Title: Doube line buffer

Size: A4	Date: 2022-03-28	**Rev: J. Tejada**
KiCad E.D.A. 8.0.9		Id: 9/11


Horizontal Counter
Vertical Counter
H1
3.06MHz
7400
B10A
LD
C6
D0
D1
D2
D3
Q0
Q1
Q2
Q3
H2
H4
H8
H16
VSS
VCC
PE
CEP
CET
CP
TC
MR
counter
74LS161
PXL_CLK'D
6.17MHz
D6
H32
H64
H128
H256
H8D
74LS08
Right half
of the screen
RH
from main
PEH
to main
H256 high during
the active video output
The count goes from 80h to FFh (blanking)
and from 100h to 1FFh (active)
B11
a0
a1
b0
b1
c0
c1
d0
d1
ya
yb
yc
yd
74xx86
H4'
H8'
H32
H64
F10A
74LS14
D9D
74LS00
H16
J10A
74LS74
H256
256V
H11B
HS
HS lasts for 32 pixels
R15
470
R11
100
SYNC
CPX
J10B
1V
G10
2V
4V
8V
16V
4kHz
2kHz
1kHz
G9
74LS10
A9B
224V
32V
64V
128V
256V
F10C
H9B
H256'D
OBJCOLD
HB
A4B
VB
lasts for 40 lines
INT_CK
D9C
BLANKING
J12A
decoder
74LS139
H15
JOTEGO
Ping Pong
JOTEGO
Sheet: /hvcounter/
File: hvcounter.kicad_sch
Title: Horizontal and vertical counters
Size: A4
Date: 2022-03-28
Rev: J. Tejada
KiCad E.D.A. 8.0.9
Id: 10/11



The device references in this sheet does not represent the actual PCB position (except for C8). The number and size of the capacitors is correct. They are distributed across the whole board.

JOTEGO
Ping Pong
JOTEGO

Sheet: /capacitors/
File: capacitors.kicad_sch

Title: Decoupling capacitors

Size: A4	Date: 2022-03-28	**Rev: J. Tejada**
KiCad E.D.A. 8.0.9		Id: 11/11