Kevin Maa

kmaa302@gmail.com | linkedin.com/in/kevinmaa | github.com/dz337

Education

University of Central Florida Orlando, FL

Bachelor of Science in Information Technology with Honors | GPA: 3.70 May 2027

Minor: Secure Comp & Networks | *Honors:* Burnett Honors College – University Honors

Relevant Courses: Computer Science I, Discrete Structures, Operating System Concepts, Security in Computing

Affiliations: IEEE UCF

Projects

2026 SouthEastCon Robotics Competition – *Group Project* Sep 2024 – Present

- Configured Raspberry Pi 5 development environment by flashing Raspberry Pi Desktop OS, setting up Git, Docker Desktop, VSCode Dev Containers extension, and Cloudflare tunneling to access team's Gitea repository for autonomous robot software development.
- Resolved Gazebo simulation compatibility issues on ARM architecture by enabling software rendering through environment variables and modifying initialization scripts to uncomment Linux-specific commands, enabling simulation testing on Raspberry Pi hardware.
- Testing micro-ROS packages and designing automated startup scripts for Docker container deployment to streamline robot development and competition preparation.
- Contributing to PCB design and layout for mini UAV flight controller, focusing on component placement, power distribution, and signal integrity for autonomous navigation systems.

KnightCore – FPGA Integration – 2025 AMD Hardware Competition – *Group Project* Apr 2025 – Aug 2025

- Integrated custom GPU hardware module onto Red Pitaya Zynq FPGA platform using Vivado block design, connecting Zynq processor, AXI interconnect, BRAM controller and memory, configuring address spaces in housekeeping region, and generating bitstreams.
- Debugged memory-mapped I/O communication issues between ARM processor and FPGA programmable logic, identifying and correcting address mapping errors in shared memory regions to enable successful hardware integration.
- Developed and executed shell script and Python-based validation tests on Red Pitaya to verify register read/write operations and confirm successful processor-to-FPGA communication through memory-mapped interfaces.

Custom RISC-V CPU – *Solo Project* Jul 2025 – Present

- Designing a 32-bit single-cycle RISC-V processor from scratch on Red Pitaya FPGA, implementing the RV32I base instruction set with ALU operations, load/store instructions, and control logic using Verilog and SystemVerilog.
- Architecting datapath components including register file, arithmetic logic unit, instruction decoder, and control unit to execute instructions through fetch-decode-execute cycle.
- Developing testbenches to validate instruction execution, register file operations, and memory interface functionality against RISC-V specification requirements.

4 Mini PC Home Lab – *Solo Project* Sep 2025 – Present

- Designing and deploying distributed computing infrastructure using 4 Mini PCs configured in a Proxmox HA cluster with ZFS replication for self-hosted services, network experimentation, and cybersecurity training.
- Implementing containerized services using Docker and Kubernetes for application deployment, alongside network security tools including Wireshark, Security Onion, and Kali Linux for penetration testing and threat detection.
- Configuring network segmentation with VLAN architecture, OPNsense firewall rules, and VPN tunneling through WireGuard to isolate services and implement enterprise-grade security best practices.

IEEE Resume Database – *Group Project* Sep 2025 – Present

- Developed HTML input form structure for IEEE UCF chapter resume database, creating form fields for member information including name, college, education history, work experience, projects, skills, and affiliations.
- Implementing dynamic array input functionality for links and projects sections, enabling members to add multiple entries through interactive form controls.
- Building front-end display components using React to present stored resume data with text fields instead of input forms for viewing member profiles.

Leadership

IEEE UCF

Active Member Sep 2025 – Present

- Contributing to IEEE UCF chapter activities and technical projects, participating in workshops on embedded systems, robotics, and software development to advance technical skills and professional development.
- Collaborating with interdisciplinary teams on hardware competition projects, coordinating between software, electrical, and mechanical engineering members for integrated system design.

Technical Skills

Languages: C, Verilog, SystemVerilog, HTML, CSS, JavaScript, SQL, Python, Bash, Assembly (RISC-V)
Web Development: React, TypeScript
Hardware Design & Verification: AXI Interconnect, Memory-Mapped I/O, BRAM, Functional Verification, RISC-V ISA
Embedded Systems: Raspberry Pi, ESP32, ROS2, micro-ROS
Virtualization & Infrastructure: Proxmox, ZFS Replication, HA Clustering, Network Segmentation
Cybersecurity: Wireshark, Security Onion, Kali Linux, Penetration Testing, OPNsense, WireGuard VPN
Tools & Technologies: Git, GitHub, Linux, Windows, VSCode, Vivado, Docker, Kubernetes, Cloudflare, VLAN, PCB Design