Lab 4: Diode Circuits

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***Abstract*—This is some text to fill up the abstract.**

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I. INTRODUCTION

THIS is some placeholder text to make the formatting less wonky.

A. Purpose

II. THEORY

III. METHODOLOGY

A. Equipment List

1) Breadboard
2) Measuring Equipment:
   a) Digital Oscilloscope
   b) Digital Multi-Meter [x2]
3) Power Sources:
   a) DC Power Supply
   b) Function Generator
4) Resistors:
   a) 1.0 kΩ (1/4 W) [x1]
   b) 10.0 kΩ (1/2 W) [x1]
   c) Variable Resistor Box
5) Diodes:
   a) 1N4002 Diode [x2]
   b) 1N4737 Zener Diode [x1]
6) Capacitors:
   a) 0.1 μF [x1]
   b) 1.0 μF (Electrolytic) [x1]

B. Diodes as Clippers

1) The circuit was built on the protoboard with $R_1 = 10$ kΩ.
2) The oscilloscope was set to DC coupling mode, and Channels 1 and 2 were displayed simultaneously.
3) A **1 kHz triangle wave** was used as the input signal. V_{s1} and $V_{\text{Out }1}$ were monitored on Channels 1 and 2 respectively.
4) The following parameters of the input signal were varied, and the effects recorded:
   a) DC Offset
   b) Frequency
   c) Peak-to-Peak Voltage
5) Screen captures were generated that indicated the clipping behavior of the circuit.
6) The second diode was wired parallel to the first to observe the resulting clipping effects.
7) The following parameters of the input signal were varied, and the effects recorded:
   a) DC Offset
   b) Amplitude
   c) Waveform Type

C. Diode Clamping

1) The circuit was built on the protoboard with $R_2 = 10$ kΩ.
2) A **1kHz sine wave** input signal was used, with the **DC Offset** set to **zero**.
3) The oscilloscope was set to DC coupling mode.
4) The oscilloscope was then wired to monitor V_{s2} and $V_{\text{Out }2}$.
5) The input and output signals were measured on Channels 1 and 2 respectively.
6) The DC Offset of the input signal was varied, and the effects on the output signal were measured and recorded.

D. Voltage Regulator

1) The circuit was built on the protoboard.
2) A 20 V DC power generator was used as the source voltage.
3) The oscilloscope was wired to measure the load variables V_L and i_L.

4) The resistance R_L was varied, and data points were collected for both V_L and i_L.
5) A plot was generated of the data points as the experiment was conducted in order to determine where more data points were needed.

E. AC $\rightarrow$ DC Converter

1) The circuit was built on the protoboard.
2) The function generator was set to produce a **1 kHz sine wave**.
3) The capacitor was tested for its polarization and connected appropriately.
4) The oscilloscope was wired to measure V_s and V_{Out} on Channels 1 and 2 respectively.
5) The oscilloscope was set to DC coupling on both channels.
6) The oscilloscope was zeroed before capturing data.
7) The resistance R_L was varied, and the results were recorded.
8) The voltages were measured with DVMs and recorded.

F. Diode Logic Circuits

1) The circuit for the **AND** gate was built on the protoboard.
2) A **5 V DC** power source was wired into the protoboard.
3) The oscilloscope was wired to measure V_{Out}.
4) Different combinations of voltages were applied to the inputs, and the outputs were recorded.
5) The procedure was repeated for an **OR** gate.

IV. Data and Analysis

A. *Clipping Circuit*

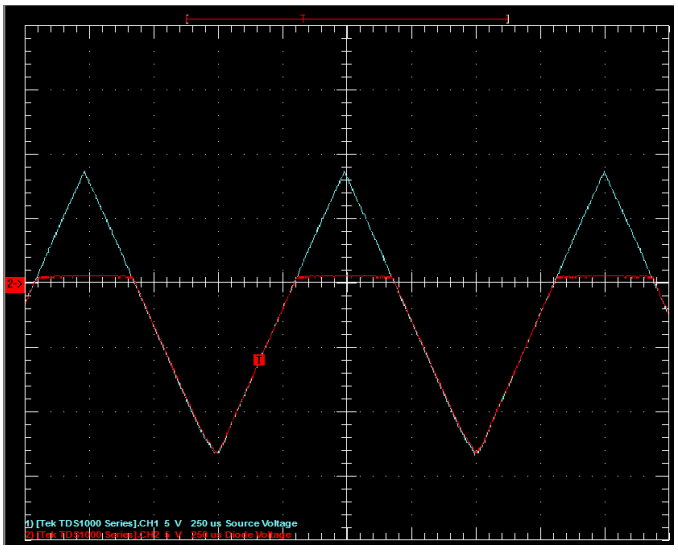

Figure 1. Source and diode voltage overlayed to show clipping behavior. The flat portion waveform just above the x-axis represents the clipped output voltage.

As the parameters outlined in the Methodology section were varied, the following observations were made. See Figure 1

1) *DC Offset*
Changing the DC Offset of the signal generator changes the magnitude of the voltage supplied, but does not have a discernible effect on the output voltage. The diode effectively cut off the signal at approximately zero volts, regardless of what voltage was supplied by the source.

2) *Frequency*
Changing the frequency of the source signal changes the edge behavior of the output voltage slightly. At low frequencies, the waveform of the output signal will mirror the input signal, with all voltages above zero rounded down to zero, which effectively flattens out the peaks. At higher frequencies, the source and output voltages begin to slip out of phase, and the waveform becomes sinusoidal with a peak at zero volts.

3) *Signal Amplitude*
Increasing the amplitude of the source signal increases the steepness of the waveform of the output voltage, but does not have a large effect on the clipping behavior.

It was found that the circuit deviates slightly from an ideal clipping circuit. While the theoretical maximum output voltage should be clipped to zero volts, the actual maximum output voltage was measured to be **552 mV**, which is shown in Figure 2.

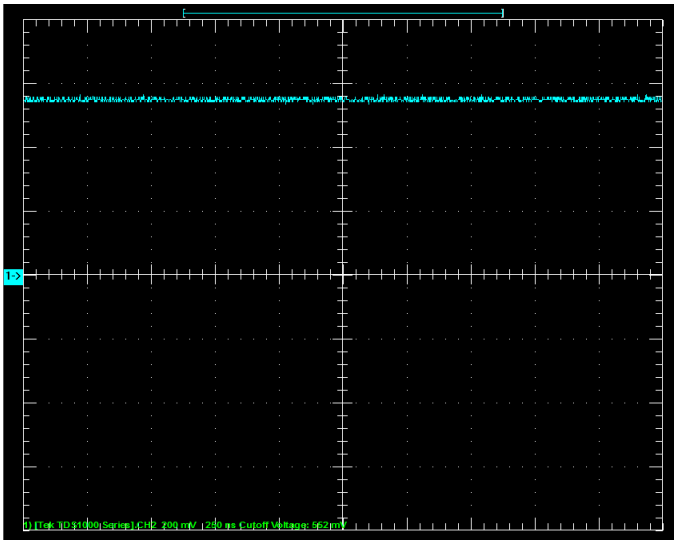

Figure 2. Deviation of cutoff voltage from theoretical ideal of zero volts.

B. *Clamping Circuit*

C. *Voltage Regulator*

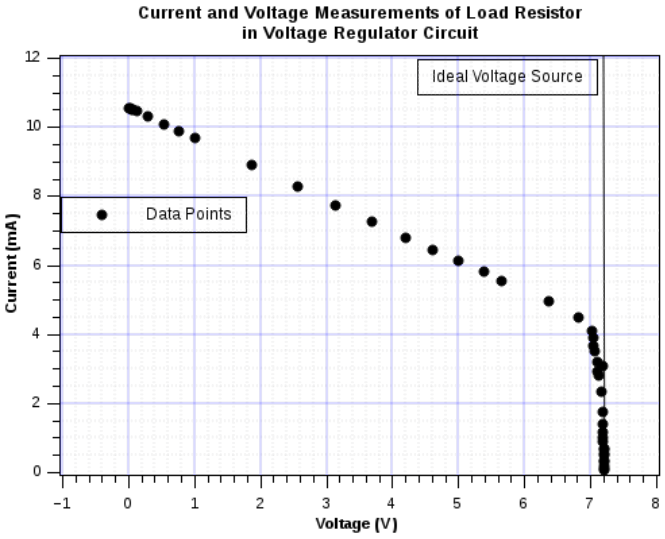

Figure 3. Plots of the load resistor's current and voltage, and its deviation from the behavior of an ideal voltage source.

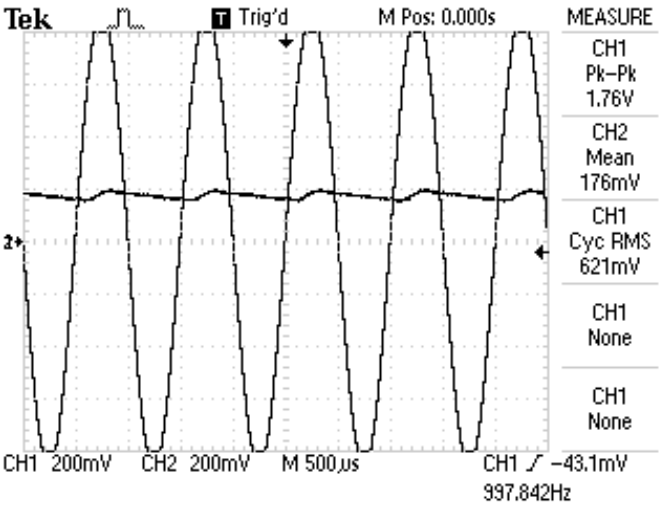

Figure 5. As the frequency increases, the voltage drop between cycles decreases.

D. *AC → DC Converter*

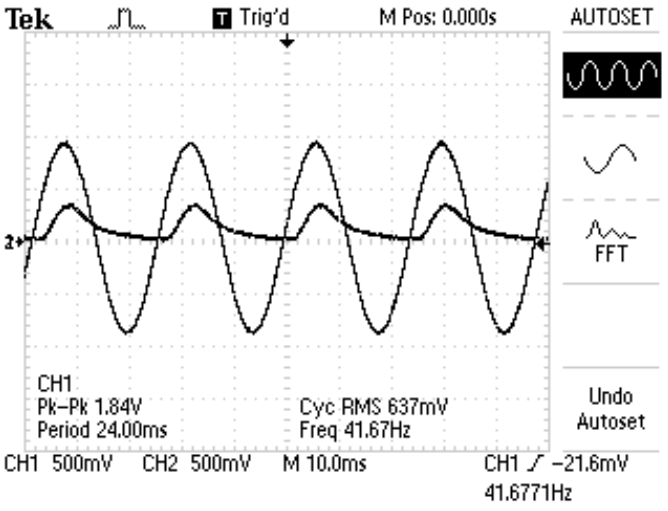

Figure 4. Display of input and output signals. The output voltage is not strictly constant, as it exhibits an exponential voltage decay due to the capacitor.

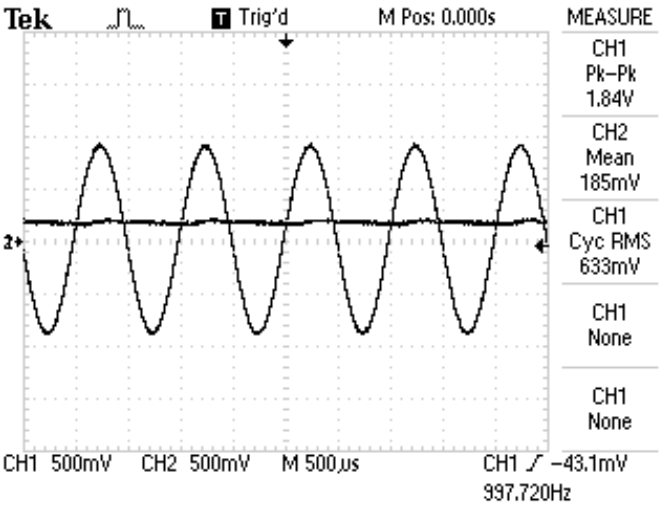

Figure 6. Zooming out at a high frequency shows that the output closely approximates a constant DC voltage.

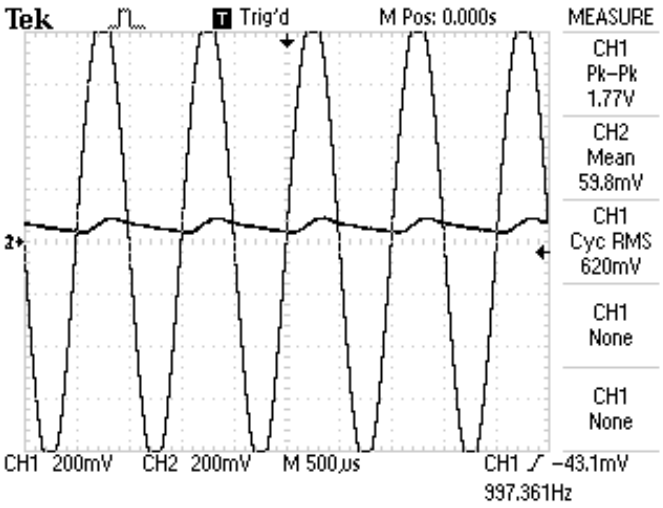

Figure 7. Changing the load resistance directly affects the voltage delivered to it. Decreasing the resistance by a factor of 5 lowered the output voltage by a factor of 3.

E. Logic Gates

Table I
AND GATE TRUTH TABLE

Input 1	Input 2	Output
1	1	1
1	0	0
0	1	0
0	0	0

Table II
OR GATE TRUTH TABLE

Input 1	Input 2	Output
1	1	1
1	0	1
0	1	1
0	0	0