CMOS Hex Schmitt Triggers

Features

- **High Voltage Type (20V Rating)**
- **Schmitt Trigger Action with No External Components**
- **Hysteresis Voltage (Typ.)**
  - **0.9V at VDD = 5V**
  - **2.3V at VDD = 10V**
  - **3.5V at VDD = 15V**
- **Noise Immunity Greater than 50%**
- **No Limit on Input Rise and Fall Times**
- **Low VDD to VSS Current During Slow Input Ramp**
- **100% Tested for Quiescent Current at 20V**
- **5V, 10V and 15V Parametric Ratings**
- **Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C**
- **Standardized Symmetrical Output Characteristics**
- **Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications

- **Wave and Pulse Shapers**
- **High Noise Environment Systems**
- **Monostable Multivibrators**
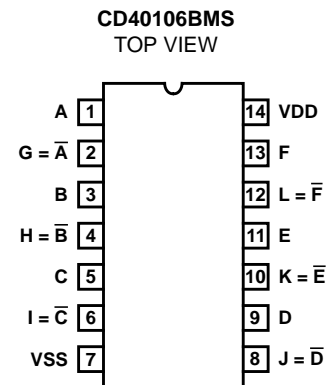- **Astable Multivibrators**

Description

CD40106BMS consists of six Schmitt trigger circuits. Each circuit functions as an inverter with Schmitt trigger action on the input. The trigger switches at different points for positive and negative going signals. The difference between the positive going voltage (VP) and the negative going voltage (VN) is defined as hysteresis voltage (VH) (see Figure 17).
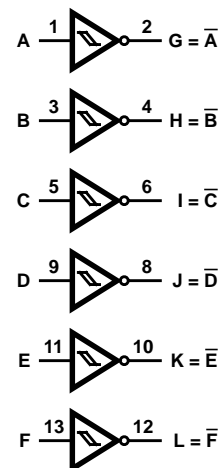
The CD40106BMS is supplied in these 14 lead outline packages:

Braze Seal DIP	H4Q
Frit Seal DIP	H1B
Ceramic Flatpack	H3W

Pinout

CD40106BMS
TOP VIEW

A	1	14	VDD
G = $\overline{A}$	2	13	F
B	3	12	L = $\overline{F}$
H = $\overline{B}$	4	11	E
C	5	10	K = $\overline{E}$
I = $\overline{C}$	6	9	D
VSS	7	8	J = $\overline{D}$

Functional Diagram

A 1 — 2 G = $\overline{A}$

B 3 — 4 H = $\overline{B}$

C 5 — 6 I = $\overline{C}$

D 9 — 8 J = $\overline{D}$

E 11 — 10 K = $\overline{E}$

F 13 — 12 L = $\overline{F}$

Logic Diagram

A 1 (3, 5, 9, 11, 13) — G 2 (4, 6, 8, 10, 12)

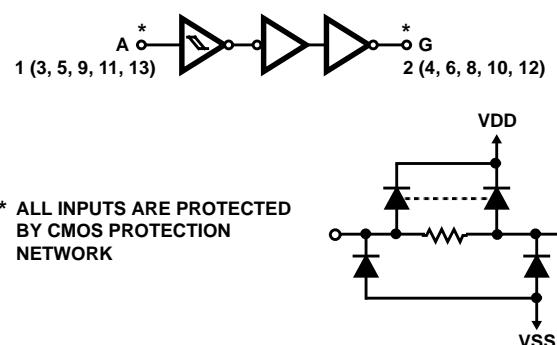VDD

* ALL INPUTS ARE PROTECTED BY CMOS PROTECTION NETWORK

VSS

FIGURE 1. 1 OF 6 SCHMITT TRIGGERS

Specifications CD40106BMS

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) . . . . -0.5V to +20V
   (Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs . . . . -0.5V to VDD +0.5V
DC Input Current, Any One Input . . . . ±10mA
Operating Temperature Range. . . . . -55°C to +125°C
   Package Types D, F, K, H
Storage Temperature Range (TSTG) . . . . -65°C to +150°C
Lead Temperature (During Soldering) . . . . +265°C
   At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for
   10s Maximum

Reliability Information

Thermal Resistance . . . . θ_{ja} θ_{jc}
   Ceramic DIP and FRIT Package . . . . . 80°C/W   20°C/W
   Flatpack Package . . . . 70°C/W   20°C/W
Maximum Package Power Dissipation (PD) at +125°C
   For T$_A$ = -55°C to +100°C (Package Type D, F, K) 500mW
   For T$_A$ = +100°C to +125°C (Package Type D, F, K). . . . . Derate
                 Linearity at 12mW/^{o}C to 200mW
Device Dissipation per Output Transistor 100mW
   For T$_A$ = Full Package Temperature Range (All Package Types)
Junction Temperature . . . . +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	μA
				2	+125°C	-	200	μA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	μA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 2)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10μA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10μA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Positive Trigger Threshold Voltage (See Figure 17)	VP5	VDD = 5V		1, 2, 3	+25°C, +125°C, -55°C	2.2	3.6	V
	VP10	VDD = 10V		1, 2, 3	+25°C, +125°C, -55°C	4.6	7.1	V
	VP15	VDD = 15V		1, 2, 3	+25°C, +125°C, -55°C	6.8	10.8	V
Negative Trigger Threshold Voltage (See Figure 17)	VN5	VDD = 5V		1, 2, 3	+25°C, +125°C, -55°C	0.9	2.8	V
	VN10	VDD = 10V		1, 2, 3	+25°C, +125°C, -55°C	2.5	5.2	V
	VN15	VDD = 15V		1, 2, 3	+25°C, +125°C, -55°C	4	7.4	V
Hysteresis Voltage (See Figure 17)	VH5	VDD = 5V		1, 2, 3	+25°C, +125°C, -55°C	0.3	1.6	V
	VH10	VDD = 10V		1, 2, 3	+25°C, +125°C, -55°C	1.2	3.4	V
	VH15	VDD = 15V		1, 2, 3	+25°C, +125°C, -55°C	1.6	5.0	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
        2. Go/No Go test with limits applied to inputs.
        3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

Specifications CD40106BMS

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	280	ns
			10, 11	+125°C, -55°C	-	378	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns

2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Propagation Delay	TPHL TPLH	VDD = 10V	1, 2, 3	+25°C	-	140	ns
		VDD = 15V	1, 2, 3	+25°C	-	120	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.

2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.

3. CL = 50pF, RL = 200K., Input TR, TF < 20ns

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	∆VTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	∆VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.   3. See Table 2 for +25°C limit.

2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.   4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	
Final Test	100% 5004	2, 3, 8A, 8B, 10, 11	
Group A	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	2, 4, 6, 8, 10, 12	1, 3, 5, 7, 9, 11, 13	14			
Static Burn-In 2 Note 1	2, 4, 6, 8, 10, 12	7	1, 3, 5, 9, 11, 13, 14			
Dynamic Burn-In Note 1	-	7	14	2, 4, 6, 8, 10, 12	1, 3, 5, 9, 11, 13	
Irradiation Note 2	2, 4, 6, 8, 10, 12	7	1, 3, 5, 9, 11, 13, 14			

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V

2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Typical Performance Characteristics
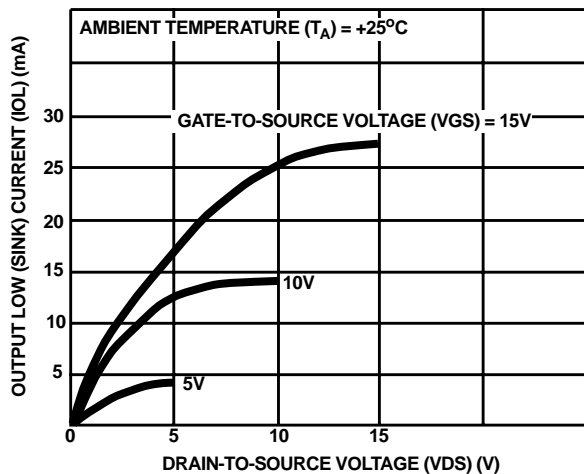
FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS
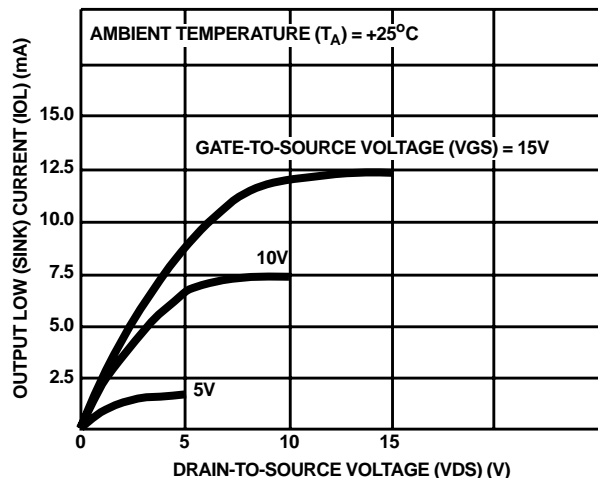
FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)
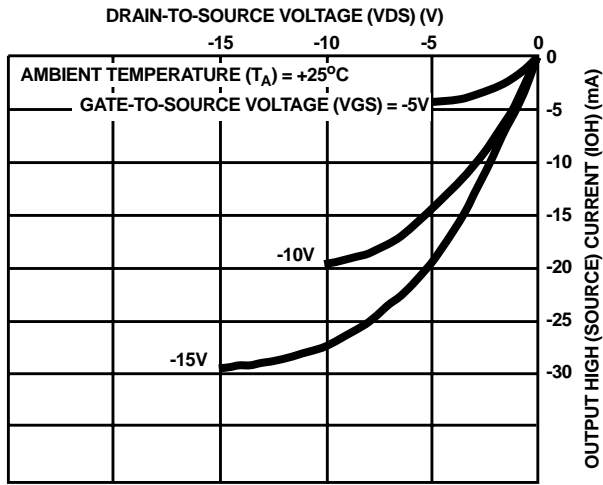
FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS
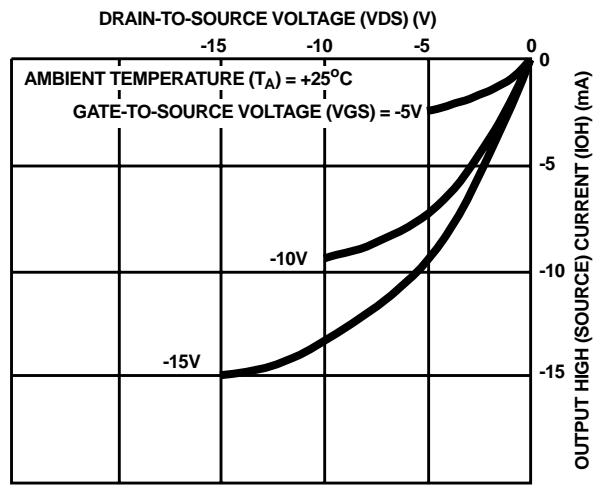
FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS
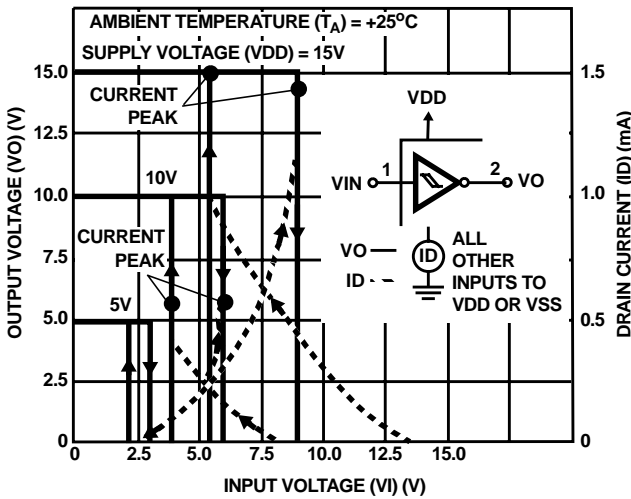
FIGURE 6. TYPICAL CURRENT AND VOLTAGE TRANSFER CHARACTERISTICS
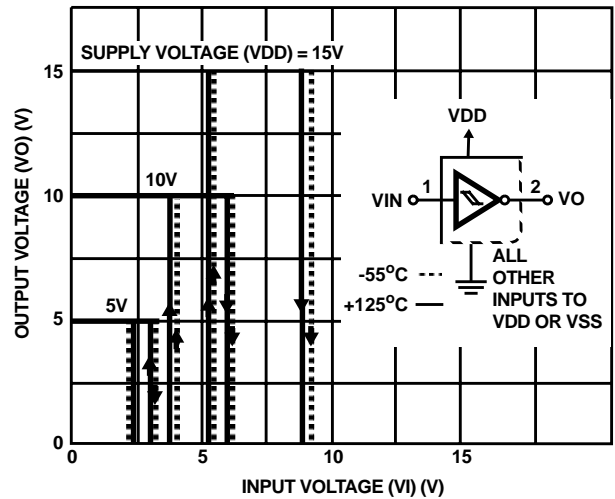

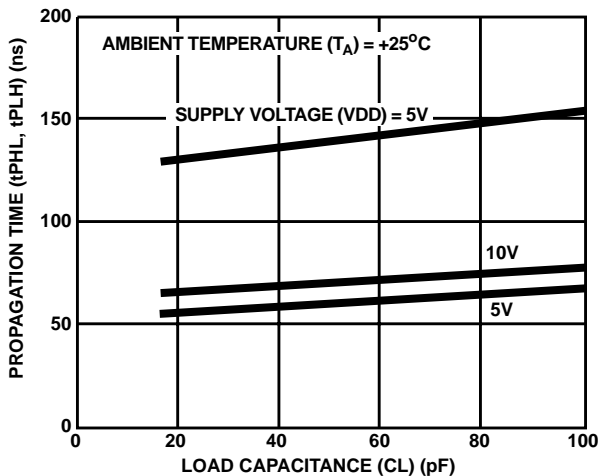**FIGURE 7. TYPICAL VOLTAGE TRANSFER CHARACTERIS-TICS AS A FUNCTION OF TEMPERATURE**

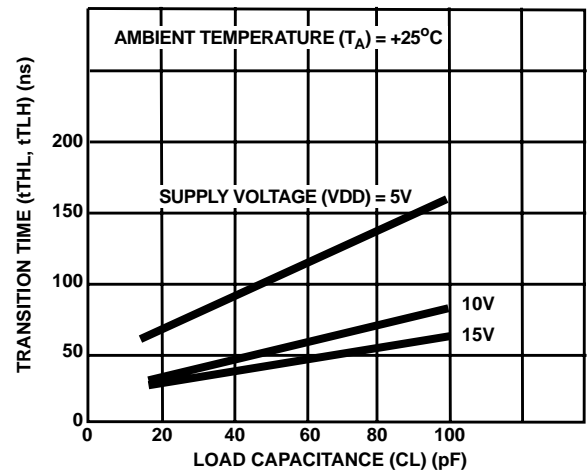**FIGURE 8. TYPICAL PROPAGATION DELAY TIME AS A FUNC-TION OF LOAD CAPACITANCE**

FIGURE 9. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

Typical Performance Characteristics (Continued)
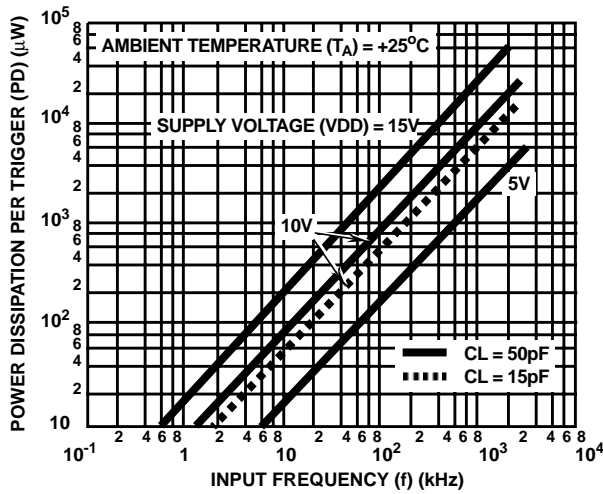
FIGURE 10. TYPICAL POWER DISSIPATION PER TRIGGER AS A FUNCTION OF INPUT FREQUENCY
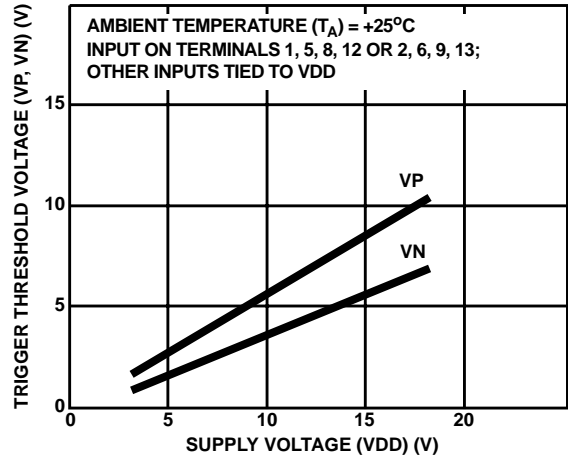
FIGURE 11. TYPICAL TRIGGER THRESHOLD VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE
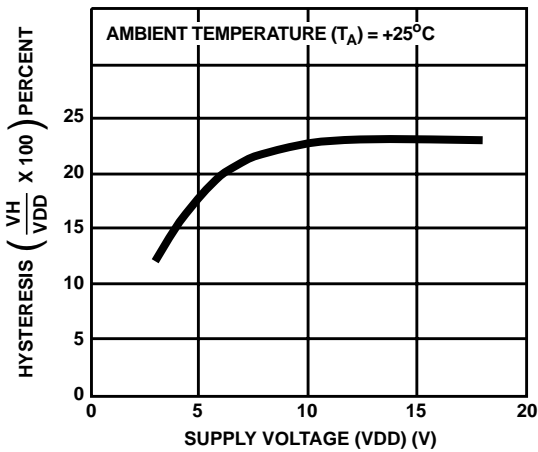
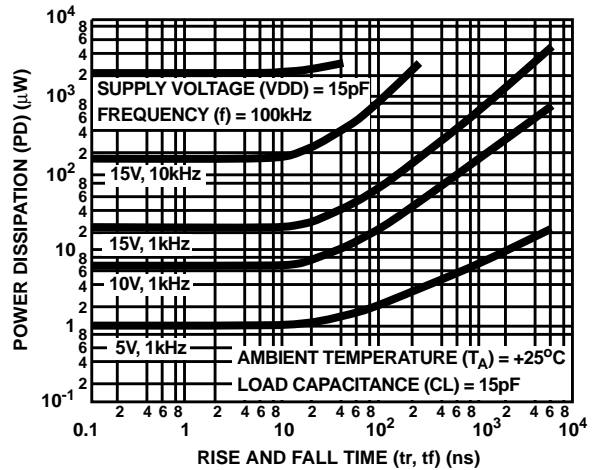**FIGURE 12. TYPICAL PERCENT HYSTERESIS AS A FUNCTION OF SUPPLY VOLTAGE**

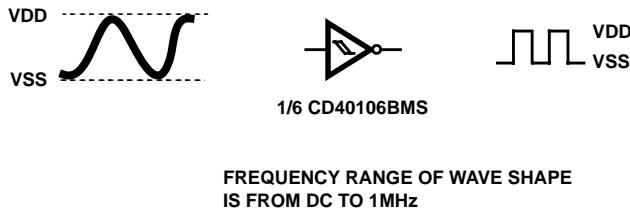**FIGURE 13. TYPICAL POWER DISSIPATION AS A FUNCTION OF RISE AND FALL TIMES**

Applications

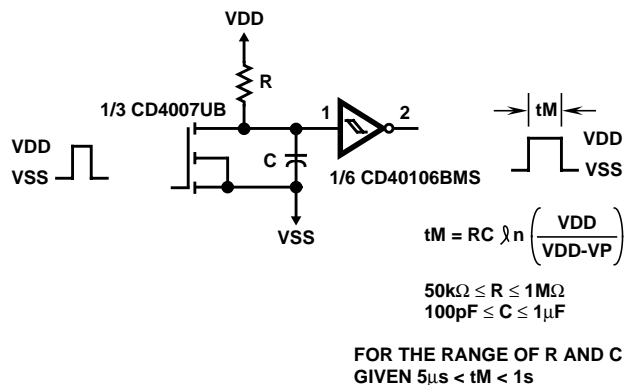**FREQUENCY RANGE OF WAVE SHAPE IS FROM DC TO 1MHz**

FIGURE 14. WAVE SHAPER

$$tM = RC \, \ell n \left(\frac{VDD}{VDD-VP} \right)$$

$50k\Omega \leq R \leq 1M\Omega$
$100pF \leq C \leq 1\mu F$

FOR THE RANGE OF R AND C GIVEN $5\mu s < tM < 1s$

FIGURE 15. MONOSTABLE MULTIVIBRATOR

Applications (Continued)

1/6 CD40106BMS

$$tA = RC \ell n \left[\left(\frac{VP}{VN} \right) \left(\frac{VDD-VN}{VDD-VP} \right) \right]$$

$50k\Omega \leq R \leq 1M\Omega$
$100pF \leq C \leq 1\mu F$

FOR THE RANGE OF R AND C
GIVEN 2μs < tA < 0.4s
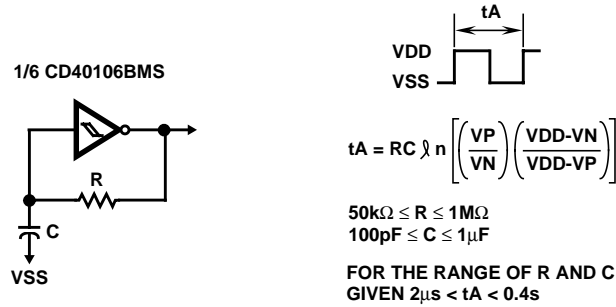
FIGURE 16. ASTABLE MULTIVIBRATOR

(a) DEFINITION OF VP, VN, VH

VH = VP - VN

(b) TRANSFER CHARACTERISTIC OF 1 OF 6 GATES
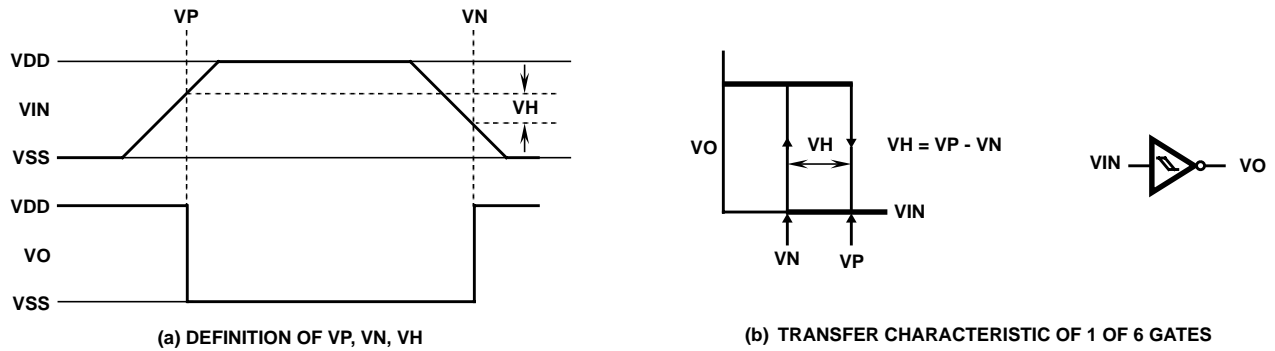
FIGURE 17. HYSTERESIS DEFINITION, CHARACTERISTICS, AND TEST SETUP

OUTPUT CHARACTERISTIC

INPUT CHARACTERISTIC

LOGIC "1" OUTPUT REGION

LOGIC "1" INPUT REGION

LOGIC "0" OUTPUT REGION
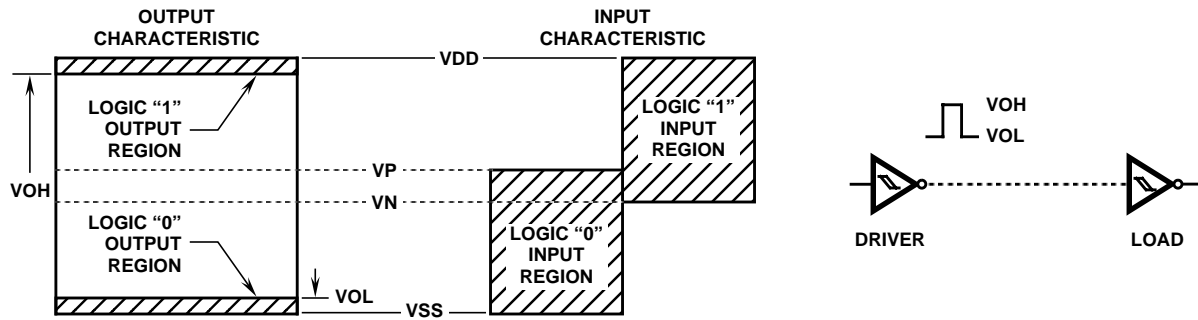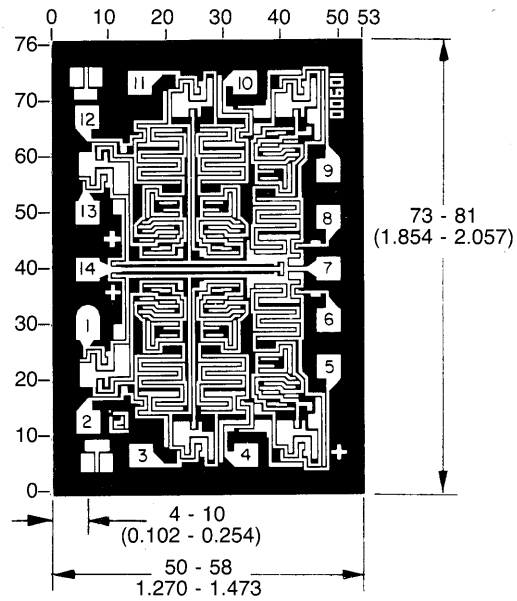
LOGIC "0" INPUT REGION

DRIVER

LOAD

FIGURE 18. INPUT AND OUTPUT CHARACTERISTICS

Chip Dimensions and Pad Layout

Dimensions in parenthesis are in millimeters and are
derived from the basic inch dimensions as indicated.
Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches