

# Analog Engineer's

Circuit Cookbook: Amplifiers



TEXAS INSTRUMENTS

# Analog Engineer's Circuit Cookbook: Amplifiers

**Second Edition**

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# Analog Engineer's Circuit Cookbook: Amplifiers

(Second Edition)

## Message from the editors:

The *Analog Engineer's Circuit Cookbook: Amplifiers* provides amplifier sub-circuit ideas that can be quickly adapted to meet your specific system needs. Each circuit is presented as a “definition-by-example.” They include step-by-step instructions, like a recipe, with formulas enabling you to adapt the circuit to meet your design goals. Additionally, all circuits are verified with SPICE simulations.

We've provided at least one recommended amplifier for each circuit, but you can swap it with another device if you've found one that's a better fit for your design. You can search our large portfolio of amplifiers at [ti.com/amplifiers](https://ti.com/amplifiers).

Our circuits require a basic understanding of amplifier concepts. If you're new to amplifier design, we highly recommend completing our TI Precision Labs (TIPL) training series. TIPL includes courses on introductory topics, such as device architecture, as well as advanced, application-specific problem-solving, using both theory and practical knowledge. Check out our curriculum for operational amplifiers (op amps), analog-to-digital converters (ADCs) and more at: [ti.com/precisionlabs](https://ti.com/precisionlabs).

We hope you find this collection of amplifier circuits helpful in developing your designs. Our goal is to regularly update the cookbook with valuable amplifier circuit building blocks. You can check to see if your version is the latest at [ti.com/circuitcookbooks](https://ti.com/circuitcookbooks). If you have input on any of the existing circuits or would like to request additional amplifier cookbook circuits for the next edition please contact us at: [opampcookbook@list.ti.com](mailto:opampcookbook@list.ti.com).

## Additional resources to explore

### TI Precision Labs

[ti.com/precisionlabs](https://ti.com/precisionlabs)

- On-demand courses and tutorials ranging from introductory to advanced concepts that focus on application-specific problem solving
- Hands-on labs and evaluation modules (EVM) available
  - TIPL Op Amps experimentation platform, [ti.com/TIPL-amp-evm](https://ti.com/TIPL-amp-evm)
  - TIPL SAR ADC experimentation platform, [ti.com/TIPL-Data-Converters-evm](https://ti.com/TIPL-Data-Converters-evm)

### Analog Engineer's Pocket Reference

[ti.com/analogrefguide](https://ti.com/analogrefguide)

- PCB, analog and mixed-signal design formulae; includes conversions, tables and equations
- e-book, iTunes and Android apps and hardcopy available

### The Signal e-book

[ti.com/signalbook](https://ti.com/signalbook)

- Op amp e-book with short, bite-sized lessons on design topics such as offset voltage, input bias current, stability, noise and more

### TI Designs

[ti.com/tidesigns](https://ti.com/tidesigns)

- Ready-to-use reference designs with theory, calculations, simulations schematics, PCB files and bench test results

### TINA-TI™ Simulation Software

[ti.com/tool/tina-ti](https://ti.com/tool/tina-ti)

- Complete SPICE simulator for DC, AC, transient and noise analysis
- Includes schematic entry and post-processor for waveform math

### Analog Engineer's Calculator

[ti.com/analogcalc](https://ti.com/analogcalc)

- ADC and amplifier design tools, noise and stability analysis, PCB and sensor tools

### Analog Wire Blog

[ti.com/analogwire](https://ti.com/analogwire)

- Technical blogs written by analog experts that include tips, tricks and design techniques

### TI E2E™ Community

[ti.com/e2e](https://ti.com/e2e)

- Support forums for all TI products

### Op Amp Circuit Quick Search and Parametric Search

[ti.com/opamp-search](https://ti.com/opamp-search)

- Search our operational amplifier portfolio by entering key parameters or by selecting a circuit function

### Op Amp Parametric Cross-Reference

[ti.com/opampcrossreference](https://ti.com/opampcrossreference)

- Find similar TI Amplifiers using competitive part numbers

### DIY Amplifier Circuit Evaluation Module (DIYAMP-EVM)

[ti.com/DIYAMP-EVM](https://ti.com/DIYAMP-EVM)

- Single-channel circuit evaluation module providing SC70, SOT23 and SOIC package options in 12 popular amplifier configurations

### Dual-Channel DIY Amplifier Circuit Evaluation Module (DUAL-DIYAMP-EVM)

[ti.com/dual-diyamp-evm](https://ti.com/dual-diyamp-evm)

- Dual-channel circuit evaluation module in an SOIC-8 package with 10 popular amplifier configurations

### Want more circuits?

- Download the *Analog Engineer's Circuit Cookbook* for data converters
  - Browse a complete list of amplifier and data converters circuits
- [Visit ti.com/circuitcookbooks](https://ti.com/circuitcookbooks)



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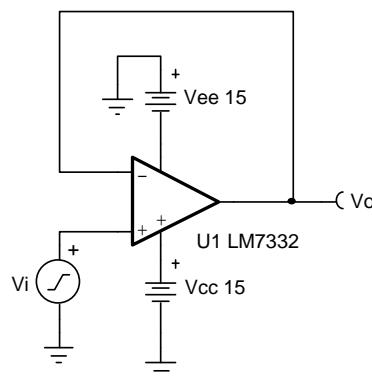
## **Buffer (follower) circuit**

### **Design Goals**

<b>Input</b>		<b>Output</b>		<b>Freq.</b>	<b>Supply</b>	
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	$f$	$V_{cc}$	$V_{ee}$
-10V	10V	-10V	10V	100kHz	15V	-15V

### **Design Description**

This design is used to buffer signals by presenting a high input impedance and a low output impedance. This circuit is commonly used to drive low-impedance loads, analog-to-digital converters (ADC) and buffer reference voltages. The output voltage of this circuit is equal to the input voltage.



### **Design Notes**

1. Use the op-amp linear output operating range, which is usually specified under the  $A_{OL}$  test conditions.
2. The small-signal bandwidth is determined by the unity-gain bandwidth of the amplifier.
3. Check the maximum output voltage swing versus frequency graph in the datasheet to minimize slew-induced distortion.
4. The common mode voltage is equal to the input signal.
5. Do not place capacitive loads directly on the output that are greater than the values recommended in the datasheet.
6. High output current amplifiers may be required if driving low impedance loads.
7. For more information on op-amp linear operating region, stability, slew-induced distortion, capacitive load drive, driving ADCs, and bandwidth, see the Design References section.

## Design Steps

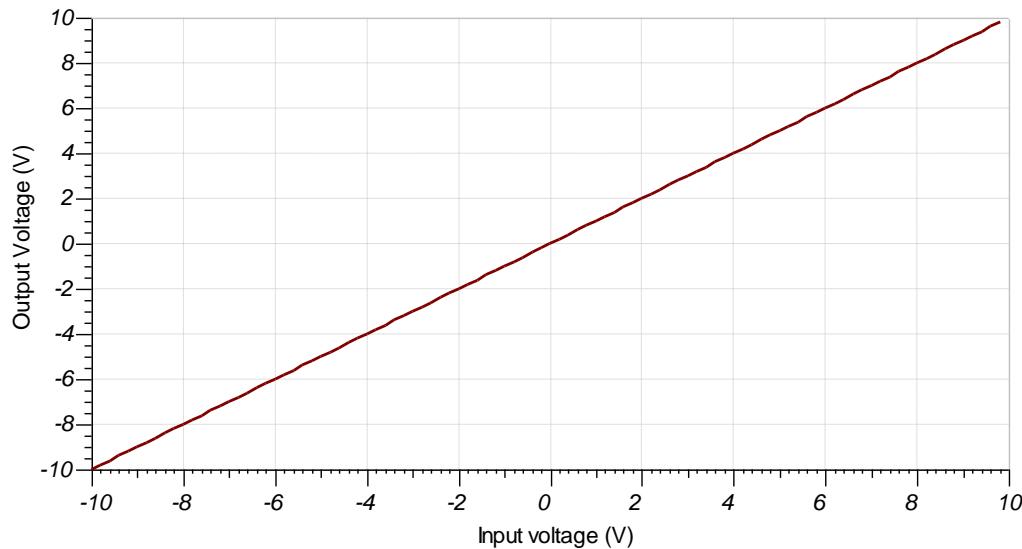
The transfer function for this circuit follows:

$$V_o = V_i$$

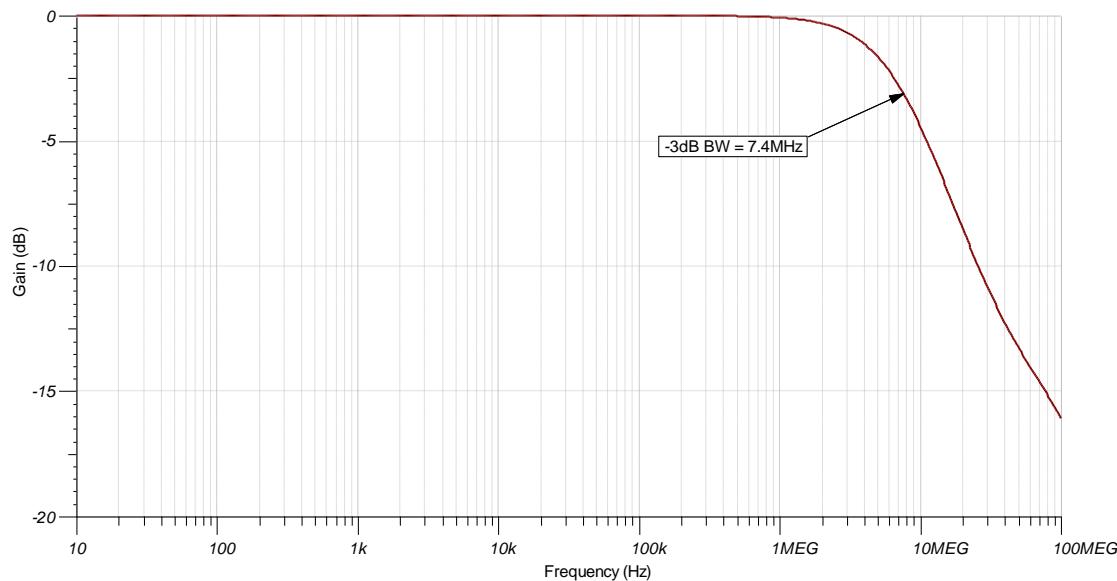
1. Verify that the amplifier can achieve the desired output swing using the supply voltages provided. Use the output swing stated in the  $A_{OL}$  test conditions. The output swing range of the amplifier must be greater than the output swing required for the design.  
 $-14V \leq V_o \leq 14V$ 
  - The output swing of the LM7332 using  $\pm 15$ -V supplies is greater than the required output swing of the design. Therefore, this requirement is met.
  - Review the Output Voltage versus Output Current curves in the product datasheet to verify the desired output voltage can be achieved for the desired output current.
2. Verify the input common mode voltage of the amplifier will not be violated using the supply voltage provided. The input common mode voltage range of the amplifier must be greater than the input signal voltage range.  
 $-15.1V \leq V_{icm} \leq 15.1V$ 
  - The input common-mode range of the LM7332 using  $\pm 15$ -V supplies is greater than the required input common-mode range of the design. Therefore, this requirement is met.
3. Calculate the minimum slew rate required to minimize slew-induced distortion.  
 $SR > 2 \times \pi \times V_p \times f = 2 \times \pi \times 10V \times 100kHz = 6.28V/\mu s$ 
  - The slew rate of the LM7332 is  $15.2V/\mu s$ . Therefore, this requirement is met.
4. Verify the device will have sufficient bandwidth for the desired output signal frequency.  
 $f_{signal} < f_{unity}$   
 $100kHz < 7.5MHz$ 
  - The desired output signal frequency is less than the unity-gain bandwidth of the LM7332. Therefore, this requirement is met.

## Design Simulations

### DC Simulation Results



### AC Simulation Results



### Design References

See the [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

For more information, see the [Capacitive Load Drive Verified Reference Design Using an Isolation Resistor TI Design](#).

See the circuit SPICE simulation file SBOC491 – <http://www.ti.com/lit/zip/sboc491>.

For more information on many op amp topics including common-mode range, output swing, bandwidth, slew rate, and how to drive an ADC, see [TI Precision Labs](#).

## Design Featured Op Amp

LM7332	
$V_{ss}$	2.5V to 32V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	1.6mV
$I_q$	2mA
$I_b$	1 $\mu$ A
<b>UGBW</b>	7.5MHz ( $\pm 5$ -V supply)
<b>SR</b>	15.2V/ $\mu$ s
<b>#Channels</b>	2
<a href="http://www.ti.com/product/LM7332">www.ti.com/product/LM7332</a>	

## Design Alternate Op Amp

OPA192	
$V_{ss}$	4.5V to 36V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	5 $\mu$ V
$I_q$	1mA
$I_b$	5pA
<b>UGBW</b>	10MHz
<b>SR</b>	20V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/opa192">www.ti.com/product/opa192</a>	

The following device is for battery-operated or power-conscious designs outside of the original design goals described earlier, where lowering the total system power is desired.

LPV511	
$V_{ss}$	2.7V to 12V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	0.2mV
$I_q$	1.2 $\mu$ A
$I_b$	0.8nA
<b>UGBW</b>	27KHz
<b>SR</b>	7.5V/ms
<b>#Channels</b>	1
<a href="http://www.ti.com/product/lpv511">www.ti.com/product/lpv511</a>	

## Revision History

Revision	Date	Change
A	January 2019	Downscale title. Added LPV511 table in the Design Alternate Op Amp section.

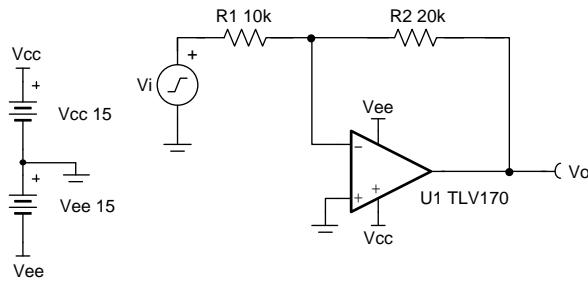
## *Inverting amplifier circuit*

### Design Goals

Input		Output		Freq.	Supply	
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	$f$	$V_{cc}$	$V_{ee}$
-7V	7V	-14V	14V	3kHz	15V	-15V

### Design Description

This design inverts the input signal,  $V_i$ , and applies a signal gain of  $-2V/V$ . The input signal typically comes from a low-impedance source because the input impedance of this circuit is determined by the input resistor,  $R_1$ . The common-mode voltage of an inverting amplifier is equal to the voltage connected to the non-inverting node, which is ground in this design.



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### Design Notes

1. Use the op amp in a linear operating region. Linear output swing is usually specified under the  $A_{OL}$  test conditions. The common-mode voltage in this circuit does not vary with input voltage.
2. The input impedance is determined by the input resistor. Make sure this value is large when compared to the source's output impedance.
3. Using high value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
4. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
5. Small-signal bandwidth is determined by the noise gain (or non-inverting gain) and op amp gain-bandwidth product (GBP). Additional filtering can be accomplished by adding a capacitor in parallel to  $R_2$ . Adding a capacitor in parallel with  $R_2$  will also improve stability of the circuit if high value resistors are used.
6. Large signal performance may be limited by slew rate. Therefore, check the maximum output swing versus frequency plot in the data sheet to minimize slew-induced distortion.
7. For more information on op amp linear operating region, stability, slew-induced distortion, capacitive load drive, driving ADCs, and bandwidth please see the Design References section.

## Design Steps

The transfer function of this circuit is given below.

$$V_o = V_i \times \left( -\frac{R_2}{R_1} \right)$$

1. Determine the starting value of  $R_1$ . The relative size of  $R_1$  to the signal source's impedance affects the gain error. Assuming the signal source's impedance is low (for example,  $100\Omega$ ), set  $R_1=10k\Omega$  for 1% gain error.

$$R_1 = 10k\Omega$$

2. Calculate the gain required for the circuit. Since this is an inverting amplifier use  $V_{iMin}$  and  $V_{oMax}$  for the calculation.

$$G = \frac{V_{oMax}}{V_{iMin}} = \frac{14V}{-7V} = -2V/V$$

3. Calculate  $R_2$  for a desired signal gain of  $-2V/V$ .

$$G = -\frac{R_2}{R_1} \rightarrow R_2 = -G \times R_1 = -(-2V/V) \times 10k\Omega = 20k\Omega$$

4. Calculate the small signal circuit bandwidth to ensure it meets the 3kHz requirement. Be sure to use the noise gain, or non-inverting gain, of the circuit.

$$GBP_{TLV170} = 1.2MHz \quad ($$

$$NG = 1 + \frac{R_2}{R_1} = 3V/V$$

$$BW = \frac{GBP}{NG} = \frac{1.2MHz}{3V/V} = 400kHz$$

5. Calculate the minimum slew rate required to minimize slew-induced distortion.

$$V_p = \frac{SR}{2\pi f} \rightarrow SR > 2 \times \pi \times f \times V_p$$

$$SR > 2 \times \pi \times 3kHz \times 14V = 263.89 \frac{V}{s} = 0.26 \frac{V}{\mu s}$$

- $SR_{TLV170}=0.4V/\mu s$ , therefore it meets this requirement.

6. To avoid stability issues ensure that the zero created by the gain setting resistors and input capacitance of the device is greater than the bandwidth of the circuit.

$$\frac{1}{2\pi \times (C_{cm} + C_{diff}) \times (R_2 \parallel R_1)} > \frac{GBP}{NG}$$

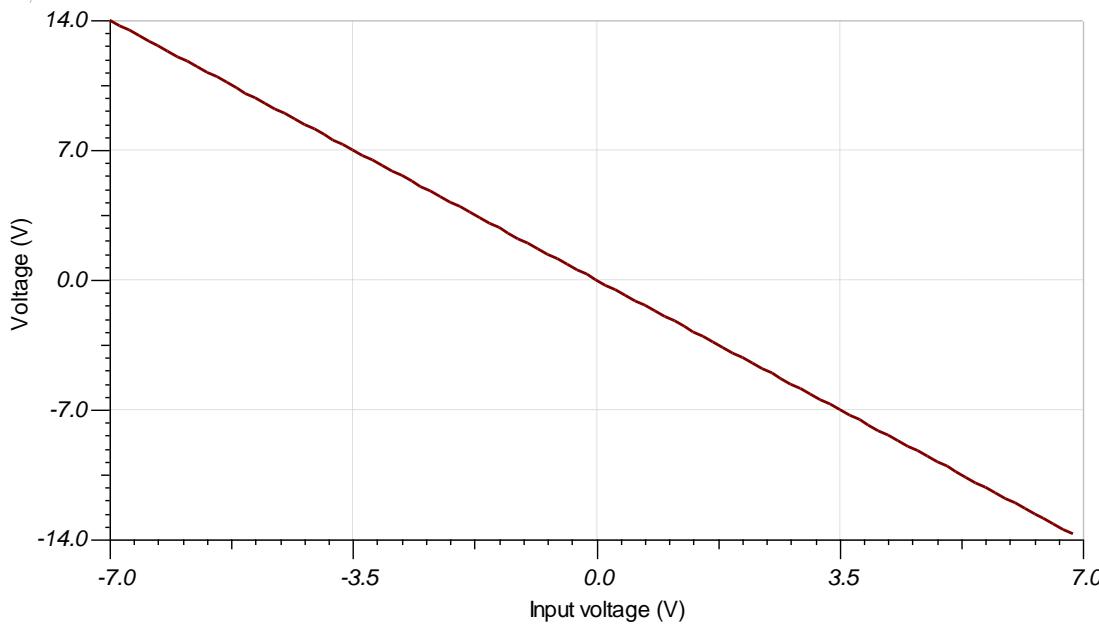
$$\frac{1}{2\pi \times 3pF + 3pF \times \frac{20k\Omega \times 10k\Omega}{20k\Omega + 10k\Omega}} > \frac{1.2MHz}{3V/V}$$

$$43.77MHz > 400kHz$$

- $C_{cm}$  and  $C_{diff}$  are the common-mode and differential input capacitances of the TLV170, respectively.
- Since the zero frequency is greater than the bandwidth of the circuit, this requirement is met.

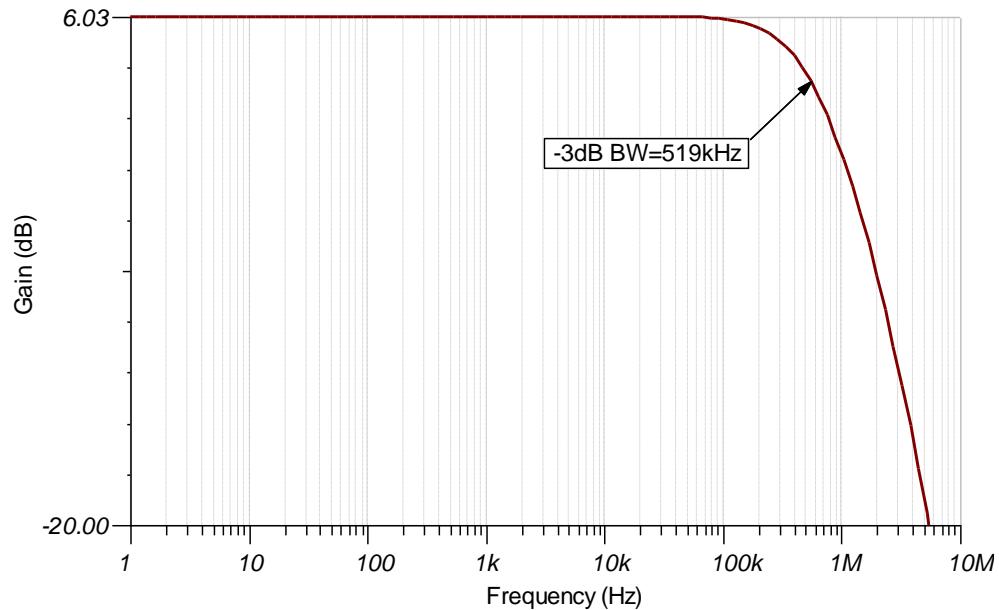
## Design Simulations

### DC Simulation Results



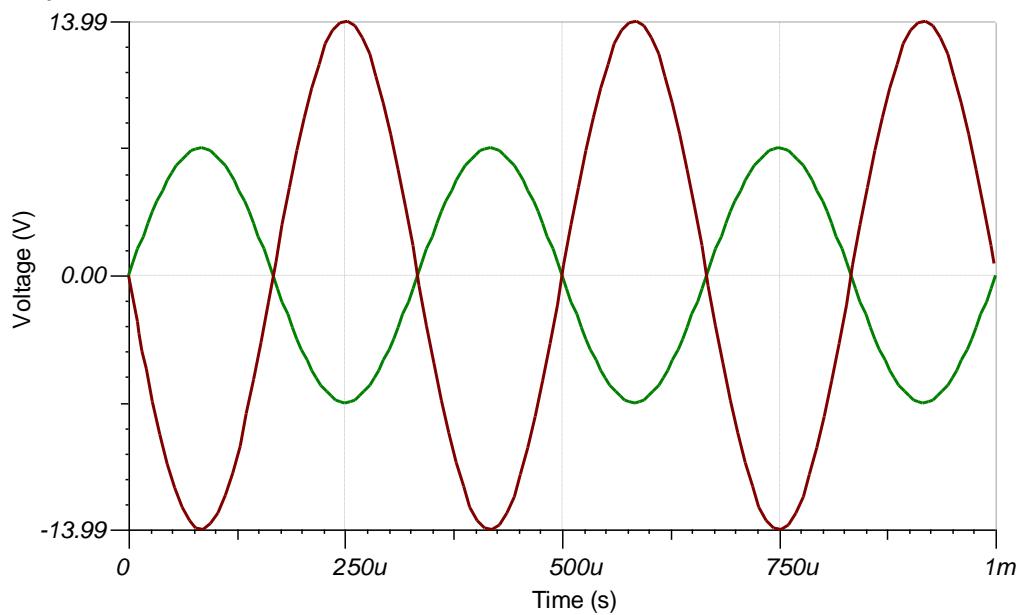
### AC Simulation Results

The bandwidth of the circuit depends on the noise gain, which is  $3V/V$ . The bandwidth is determined by looking at the  $-3\text{dB}$  point, which is located at  $3\text{dB}$  given a signal gain of  $6\text{dB}$ . The simulation sufficiently correlates with the calculated value of  $400\text{kHz}$ .



### Transient Simulation Results

The output is double the magnitude of the input, and inverted.



### Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOC492](#).

For more information on many op amp topics including common-mode range, output swing, bandwidth, and how to drive an ADC please visit [TI Precision Labs](#).

### Design Featured Op Amp

TLV170	
$V_{ss}$	$\pm 18V$ (36V)
$V_{inCM}$	( $V_{ee}-0.1V$ ) to ( $V_{cc}-2V$ )
$V_{out}$	Rail-to-rail
$V_{os}$	0.5mV
$I_q$	125 $\mu$ A
$I_b$	10pA
<b>UGBW</b>	1.2MHz
<b>SR</b>	0.4V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/tlv170">www.ti.com/product/tlv170</a>	

### Design Alternate Op Amp

LMV358	
$V_{ss}$	2.7 to 5.5V
$V_{inCM}$	( $V_{ee}-0.2V$ ) to ( $V_{cc}-0.8V$ )
$V_{out}$	Rail-to-rail
$V_{os}$	1.7mV
$I_q$	210 $\mu$ A
$I_b$	15nA
<b>UGBW</b>	1MHz
<b>SR</b>	1V/ $\mu$ s
<b>#Channels</b>	1 (LMV321), 2 (LMV358), 4 (LMV324)
<a href="http://www.ti.com/product/lmv358">www.ti.com/product/lmv358</a>	

### Revision History

Revision	Date	Change
A	January 2019	Downscale title. Added link to circuit cookbook landing page.

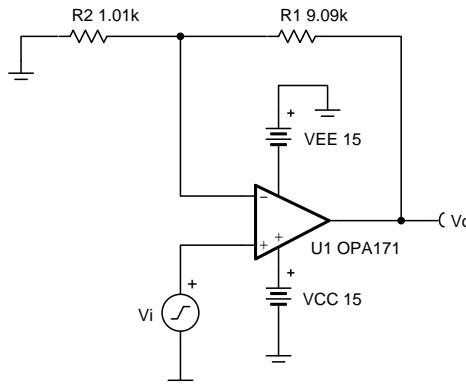
## Non-inverting amplifier circuit

### Design Goals

Input		Output		Supply	
ViMin	ViMax	VoMin	VoMax	Vcc	Vee
-1V	1V	-10V	10	15V	-15V

### Design Description

This design amplifies the input signal,  $V_i$ , with a signal gain of 10V/V. The input signal may come from a high-impedance source (for example,  $M\Omega$ ) because the input impedance of this circuit is determined by the extremely high input impedance of the op amp (for example,  $G\Omega$ ). The common-mode voltage of a non-inverting amplifier is equal to the input signal.



### Design Notes

1. Use the op amp linear output operating range, which is usually specified under the  $A_{OL}$  test conditions. The common-mode voltage is equal to the input signal.
2. The input impedance of this circuit is equal to the input impedance of the amplifier.
3. Using high-value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
4. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
5. The small-signal bandwidth of a non-inverting amplifier depends on the gain of the circuit and the gain bandwidth product (GBP) of the amplifier. Additional filtering can be accomplished by adding a capacitor in parallel to  $R_1$ . Adding a capacitor in parallel with  $R_1$  will also improve stability of the circuit if high-value resistors are used.
6. Large signal performance may be limited by slew rate. Therefore, check the maximum output swing versus frequency plot in the data sheet to minimize slew-induced distortion.
7. For more information on op amp linear operating region, stability, slew-induced distortion, capacitive load drive, driving ADCs, and bandwidth please see the Design References section.

## Design Steps

The transfer function for this circuit is given below.

$$V_o = V_i \times \left(1 + \frac{R_1}{R_2}\right)$$

1. Calculate the gain.

$$G = \frac{V_{o\_max} - V_{o\_min}}{V_{i\_max} - V_{i\_min}} \quad ($$

$$G = \frac{10V - -10V}{1V - -1V} = 10V / V$$

2. Calculate values for  $R_1$  and  $R_2$ .

$$G = 1 + \frac{R_1}{R_2}$$

Choose  $R_1 = 9.09k\Omega$

$$R_2 = \frac{R_1}{G-1} = \frac{9.09k\Omega}{10V/V - 1} = 1.01k\Omega$$

3. Calculate the minimum slew rate required to minimize slew-induced distortion.

$$SR > 2 \times \pi \times V_p \times f = 2 \times \pi \times 10V \times 20kHz = 1.257V / \mu s$$

- The slew rate of the OPA171 is  $1.5V/\mu s$ , therefore it meets this requirement.

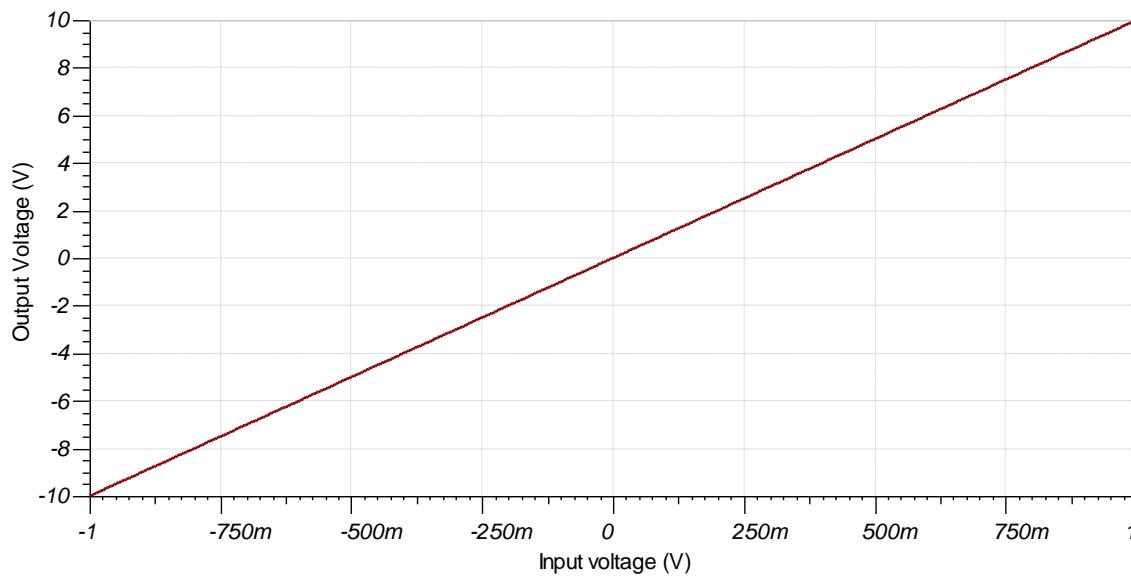
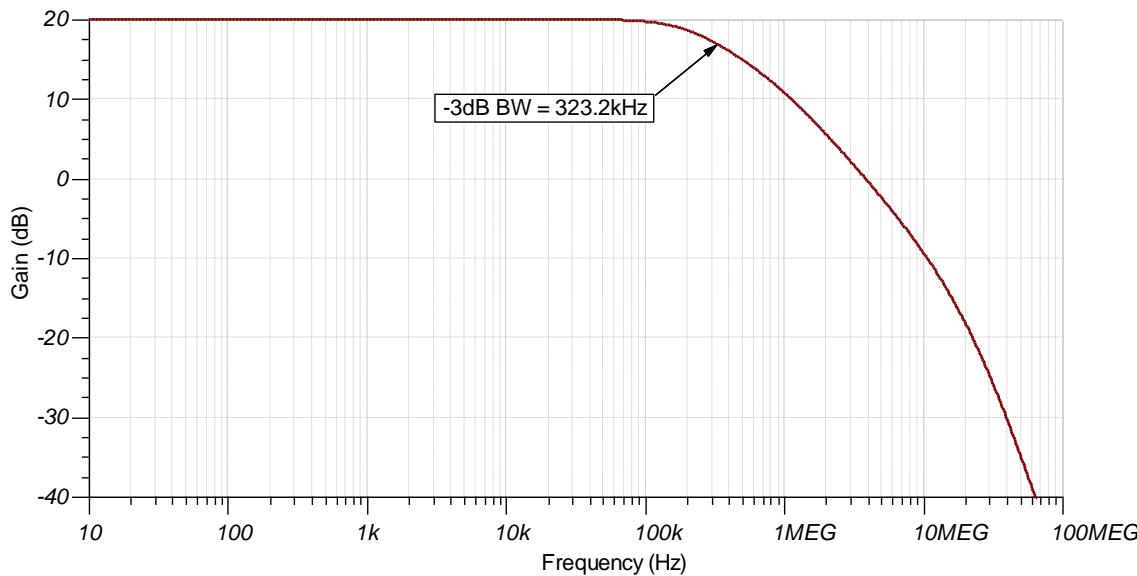
4. To maintain sufficient phase margin, ensure that the zero created by the gain setting resistors and input capacitance of the device is greater than the bandwidth of the circuit.

$$\frac{1}{2 \times \pi \times (C_{cm} + C_{diff}) \times (R_1 \parallel R_2)} > \frac{GBP}{G} \quad ($$

$$\frac{1}{2 \times \pi \times 3pF + 3pF \times \frac{1.01k\Omega \times 9.09k\Omega}{1.01k\Omega + 9.09k\Omega}} > \frac{3MHz}{10V/V}$$

$$29.18MHz > 300kHz$$

- $C_{cm}$  and  $C_{diff}$  are the common-mode and differential input capacitances of the OPA171, respectively.
- Since the zero frequency is greater than the bandwidth of the circuit, this requirement is met.

**Design Simulations****DC Simulation Results****AC Simulation Results**

## Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOC493](#).

For more information on many op amp topics including common-mode range, output swing, and bandwidth please visit [TI Precision Labs](#).

## Design Featured Op Amp

OPA171	
$V_{ss}$	2.7V to 36V
$V_{inCM}$	( $V_{ee}$ -0.1V) to ( $V_{cc}$ -2V)
$V_{out}$	Rail-to-rail
$V_{os}$	250 $\mu$ V
$I_q$	475 $\mu$ A
$I_b$	8pA
<b>UGBW</b>	3MHz
<b>SR</b>	1.5V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/opa171">www.ti.com/product/opa171</a>	

## Design Alternate Op Amp

OPA191	
$V_{ss}$	4.5V to 36V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	5 $\mu$ V
$I_q$	140 $\mu$ A
$I_b$	5pA
<b>UGBW</b>	2.5MHz
<b>SR</b>	7.5V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/OPA191">www.ti.com/product/OPA191</a>	

## Revision History

Revision	Date	Change
A	January 2019	Downscale the title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page.

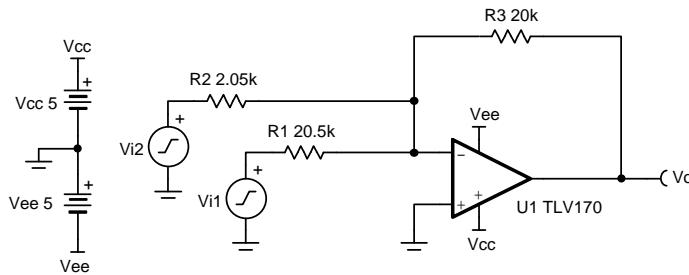
## *Inverting summer circuit*

### Design Goals

Input 1		Input 2		Output		Freq.	Supply	
$V_{i1\text{Min}}$	$V_{i1\text{Max}}$	$V_{i2\text{Min}}$	$V_{i2\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	$f$	$V_{cc}$	$V_{ee}$
-5V	5V	-250mV	250mV	-4.9V	4.9V	10kHz	5V	-5V

### Design Description

This design sums (adds) and inverts two input signals,  $V_{i1}$  and  $V_{i2}$ . The input signals typically come from low-impedance sources because the input impedance of this circuit is determined by the input resistors,  $R_1$  and  $R_2$ . The common-mode voltage of an inverting amplifier is equal to the voltage connected to the non-inverting node, which is ground in this design.



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### Design Notes

1. Use the op amp in a linear operating region. Linear output swing is usually specified under the  $A_{OL}$  test conditions. The common-mode voltage in this circuit does not vary with input voltage.
2. The input impedance is determined by the input resistors. Make sure these values are large when compared to the output impedance of the source.
3. Using high-value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
4. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
5. Small-signal bandwidth is determined by the noise gain (or non-inverting gain) and op amp gain-bandwidth product (GBP). Additional filtering can be accomplished by adding a capacitor in parallel to  $R_3$ . Adding a capacitor in parallel with  $R_3$  will also improve stability of the circuit if high-value resistors are used.
6. Large signal performance may be limited by slew rate. Therefore, check the maximum output swing versus frequency plot in the data sheet to minimize slew-induced distortion.
7. For more information on op amp linear operating region, stability, slew-induced distortion, capacitive load drive, driving ADCs, and bandwidth please see the Design References section.

## Design Steps

The transfer function for this circuit is given below.

$$V_o = V_{i1} \times \left(-\frac{R_3}{R_1}\right) + V_{i2} \times \left(-\frac{R_3}{R_2}\right)$$

1. Select a reasonable resistance value for  $R_3$ .

$$R_3 = 20\text{k}\Omega$$

2. Calculate gain required for  $V_{i1}$ . For this design, half of the output swing is devoted to each input.

$$G_{Vi1} = \frac{\frac{V_{oMax} - V_{oMin}}{2}}{V_{i1\ Max} - V_{i1\ Min}} = \frac{\frac{4.9V - (-4.9V)}{2}}{2.5V - (-2.5V)} = 0.98\frac{V}{V} = -0.175\text{dB}$$

3. Calculate the value of  $R_1$ .

$$|G_{Vi1}| = \frac{R_3}{R_1} \rightarrow R_1 = \frac{R_3}{|G_{Vi1}|} = \frac{20\text{k}\Omega}{0.98\text{V/V}} = 20.4\text{k}\Omega \approx 20.5\text{k}\Omega \text{ (Standard Value)}$$

4. Calculate gain required for  $V_{i2}$ . For this design, half of the output swing is devoted to each input.

$$G_{Vi2} = \frac{\frac{V_{oMax} - V_{oMin}}{2}}{V_{i2\ Max} - V_{i2\ Min}} = \frac{\frac{4.9V - (-4.9V)}{2}}{250\text{mV} - (-250\text{mV})} = 9.8\frac{V}{V} = 19.82\text{dB}$$

5. Calculate the value of  $R_2$ .

$$|G_{Vi2}| = \frac{R_3}{R_2} \rightarrow R_2 = \frac{R_3}{|G_{Vi2}|} = \frac{20\text{k}\Omega}{9.8\text{V/V}} = 2.04\text{k}\Omega \approx 2.05\text{k}\Omega \text{ (Standard Value)}$$

6. Calculate the small signal circuit bandwidth to ensure it meets the 10-kHz requirement. Be sure to use the noise gain (NG), or non-inverting gain, of the circuit. When calculating the noise gain note that  $R_1$  and  $R_2$  are in parallel.

$$GBP_{OPA170} = 1.2\text{MHz} \quad ( \quad ) \quad ( \quad )$$

$$NG = 1 + \frac{R_3}{R_1 \parallel R_2} = 1 + \frac{20\text{k}\Omega}{1.86\text{k}\Omega} = 11.75\frac{V}{V} = 21.4\text{dB}$$

$$BW = \frac{GBP}{NG} = \frac{1.2\text{MHz}}{11.75\text{V/V}} = 102\text{kHz}$$

- This requirement is met because the closed-loop bandwidth is 102kHz and the design goal is 10kHz.

7. Calculate the minimum slew rate to minimize slew-induced distortion.

$$V_p = \frac{SR}{2\pi f} \rightarrow SR > 2 \times \pi \times f \times V_p$$

$$SR > 2 \times \pi \times 10\text{kHz} \times 4.9\text{V} = 307.87\frac{\text{V}}{\mu\text{s}} = 0.31\frac{\text{V}}{\mu\text{s}}$$

- $SR_{OPA170} = 0.4\text{V}/\mu\text{s}$ , therefore it meets this requirement.

8. To avoid stability issues ensure that the zero created by the gain setting resistors and input capacitance of the device is greater than the bandwidth of the circuit.

$$\frac{\frac{1}{2\pi(C_{cm} + C_{diff}) \times (R_1 \parallel R_2 \parallel R_3)}}{\frac{1}{2\pi \times 3\text{pF} + 3\text{pF} \times 1.7\text{k}\Omega}} > \frac{1.2\text{MHz}}{11.75\text{V/V}}$$

$$15.6\text{MHz} > 102\text{kHz}$$

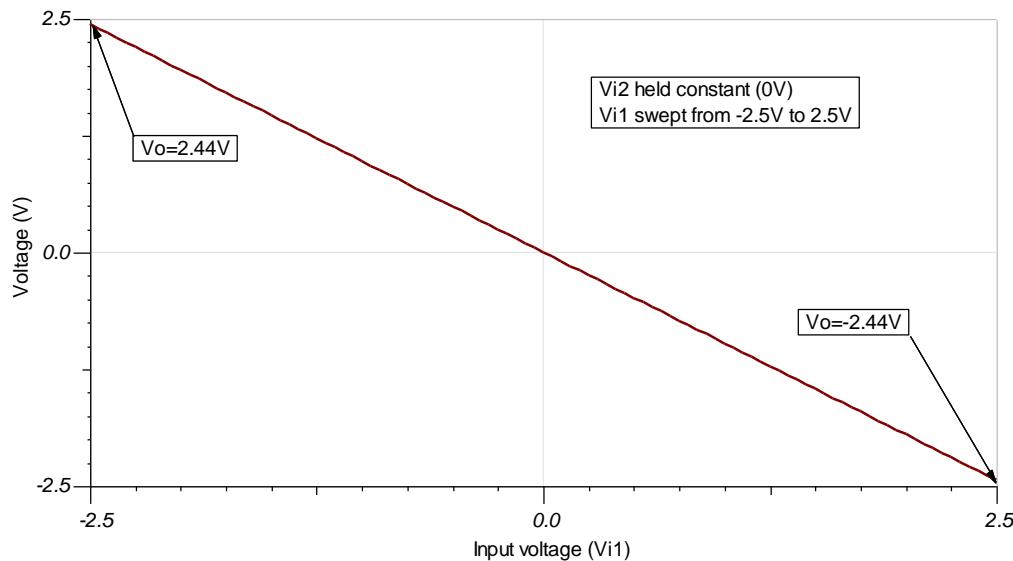
- $C_{cm}$  and  $C_{diff}$  are the common-mode and differential input capacitances.

- Since the zero frequency is greater than the bandwidth of the circuit, this requirement is met.

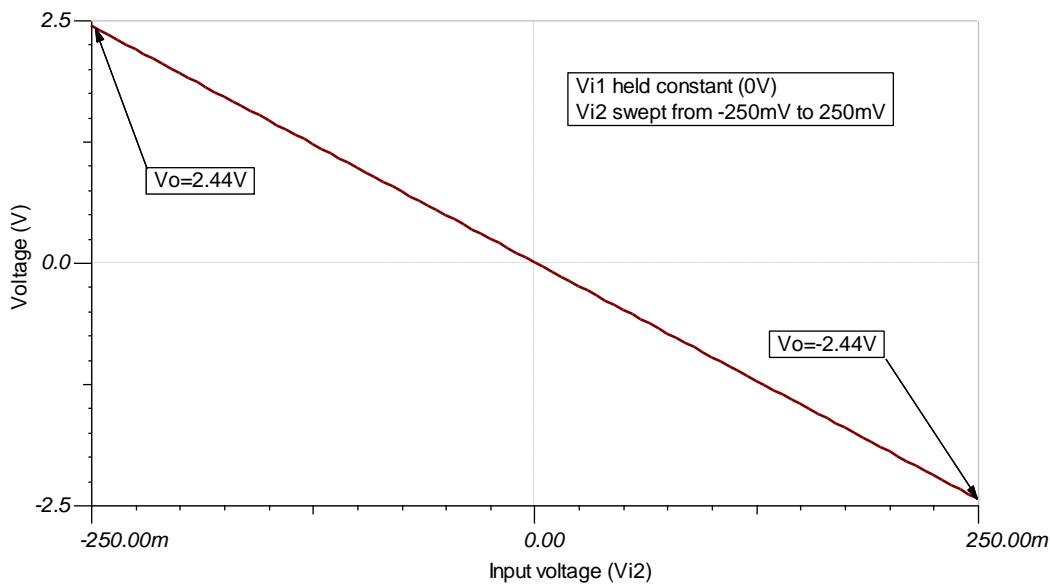
## Design Simulations

### DC Simulation Results

This simulation sweeps  $V_{i1}$  from  $-2.5V$  to  $2.5V$  while  $V_{i2}$  is held constant at  $0V$ . The output is inverted and ranges from  $-2.44V$  to  $2.44V$ .

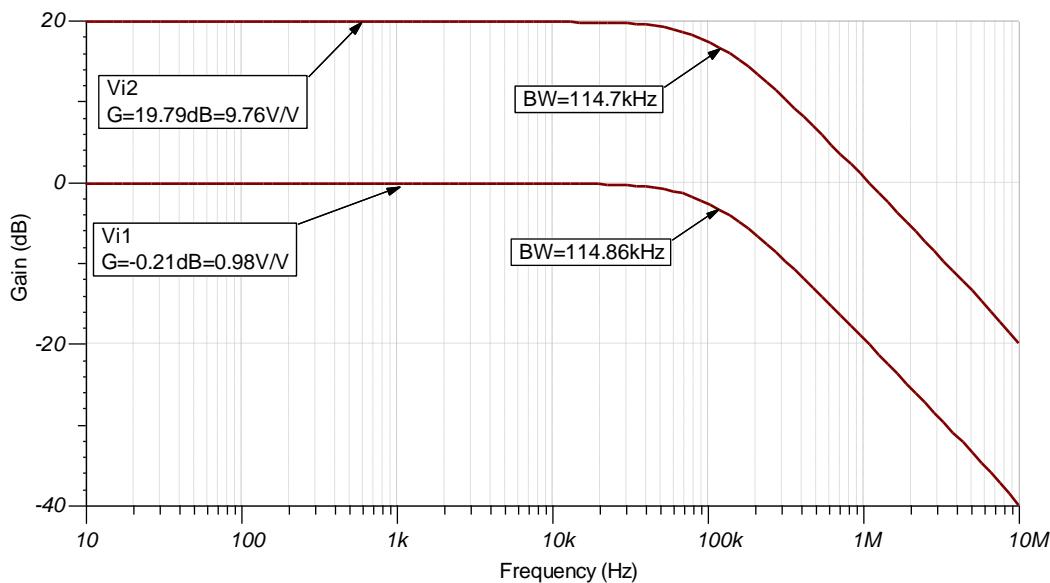


This simulation sweeps  $V_{i2}$  from  $-250mV$  to  $250mV$  while  $V_{i1}$  is held constant at  $0V$ . The output is inverted and ranges from  $-2.44V$  to  $2.44V$ .



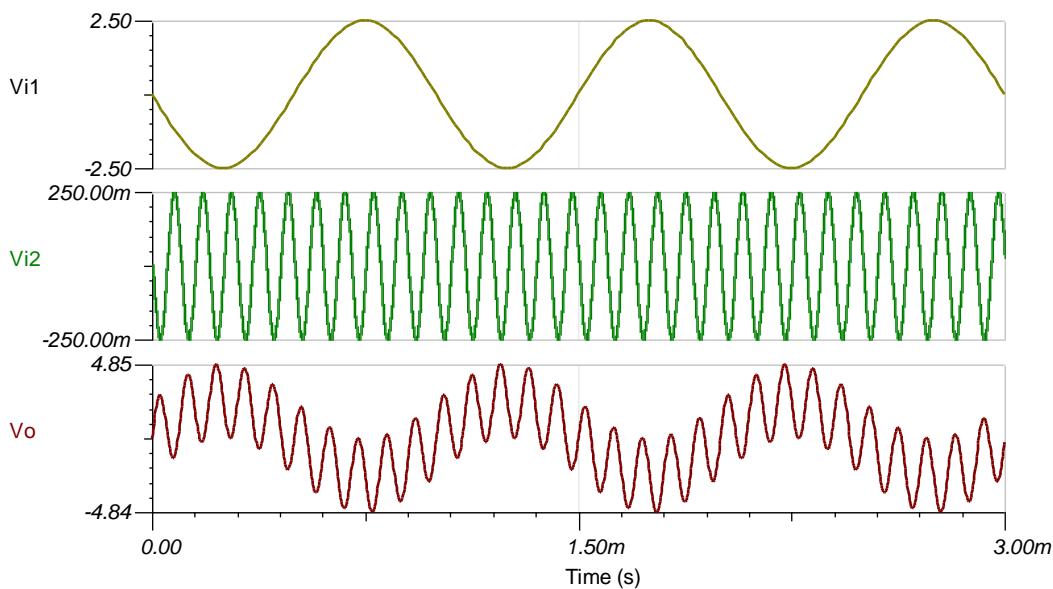
## AC Simulation Results

This simulation shows the bandwidth of the circuit. Note that the bandwidth is the same for either input. This is because the bandwidth depends on the noise gain of the circuit, not the signal gain of each input. These results correlate well with the calculations.



## Transient Simulation Results

This simulation shows the inversion and summing of the two input signals.  $V_{i1}$  is a 1-kHz, 5-V<sub>pp</sub> sine wave and  $V_{i2}$  is a 10-kHz, 500-mV<sub>pp</sub> sine wave. Since both inputs are properly amplified or attenuated, the output is within specification.



### Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOC494](#).

For more information on many op amp topics including common-mode range, output swing, bandwidth, and how to drive an ADC please visit [TI Precision Labs](#).

### Design Featured Op Amp

OPA170	
$V_{ss}$	2.7V to 36V
$V_{inCM}$	(Vee-0.1V) to (Vcc-2V)
$V_{out}$	Rail-to-rail
$V_{os}$	0.25mV
$I_q$	110 $\mu$ A
$I_b$	8pA
<b>UGBW</b>	1.2MHz
<b>SR</b>	0.4V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/opa170">www.ti.com/product/opa170</a>	

### Design Alternate Op Amp

LMC7101	
$V_{ss}$	2.7V to 15.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	110 $\mu$ V
$I_q$	0.8mA
$I_b$	1pA
<b>UGBW</b>	1.1MHz
<b>SR</b>	1.1V/ $\mu$ s
<b>#Channels</b>	1
<a href="http://www.ti.com/product/lmc7101">www.ti.com/product/lmc7101</a>	

### Revision History

Revision	Date	Change
A	January 2019	Downscale title. Updated title role to 'Amplifiers'. Added link to circuit cookbook landing page.

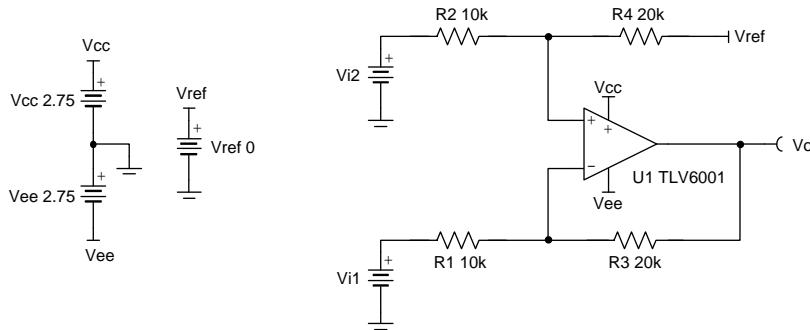
## Difference amplifier (subtractor) circuit

### Design Goals

Input ( $V_{i2}-V_{i1}$ )		Output		CMRR (min)	Supply		
$V_{idiffMin}$	$V_{idiffMax}$	$V_{oMin}$	$V_{oMax}$	dB	$V_{cc}$	$V_{ee}$	$V_{ref}$
-1.25V	1.25V	-2.5V	2.5V	50	2.75V	-2.75V	0V

### Design Description

This design inputs two signals,  $V_{i1}$  and  $V_{i2}$ , and outputs their difference (subtracts). The input signals typically come from low-impedance sources because the input impedance of this circuit is determined by the resistive network. Difference amplifiers are typically used to amplify differential input signals and reject common-mode voltages. A common-mode voltage is the voltage common to both inputs. The effectiveness of the ability of a difference amplifier to reject a common-mode signal is known as common-mode rejection ratio (CMRR). The CMRR of a difference amplifier is dominated by the tolerance of the resistors.



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### Design Notes

1. Use the op amp in a linear operating region. Ensure that the inputs of the op amp do not exceed the common-mode range of the device. Linear output swing is usually specified under the  $A_{OL}$  test conditions.
2. The input impedance is determined by the input resistive network. Make sure these values are large when compared to the output impedance of the sources.
3. Using high-value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
4. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
5. Small-signal bandwidth is determined by the noise gain (or non-inverting gain) and op amp gain-bandwidth product (GBP). Additional filtering can be accomplished by adding a capacitors in parallel to  $R_3$  and  $R_4$ . Adding capacitors in parallel with  $R_3$  and  $R_4$  will also improve stability of the circuit if high-value resistors are used.
6. Large signal performance may be limited by slew rate. Therefore, check the maximum output swing versus frequency plot in the data sheet to minimize slew-induced distortion.
7. For more information on op amp linear operating region, stability, slew-induced distortion, capacitive load drive, driving ADCs, and bandwidth please see the Design References section.

## Design Steps

The complete transfer function for this circuit is shown below.

$$V_o = V_{i1} \times \left( -\frac{R_3}{R_1} \right) + V_{i2} \times \left( \frac{R_4}{R_2+R_4} \right) \times \left( 1 + \frac{R_3}{R_1} \right) + V_{ref} \times \left( \frac{R_2}{R_2+R_4} \right) \times \left( 1 + \frac{R_3}{R_1} \right)$$

If  $R_1 = R_2$  and  $R_3 = R_4$  the transfer function for this circuit simplifies to the following equation.

$$V_o = (V_{i2} - V_{i1}) \times \frac{R_3}{R_1} + V_{ref}$$

- Where the gain,  $G$ , is  $R_3/R_1$ .

1. Determine the starting value of  $R_1$  and  $R_2$ . The relative size of  $R_1$  and  $R_2$  to the signal impedance of the source affects the gain error.

$$R_1 = R_2 = 10k\Omega$$

2. Calculate the gain required for the circuit.

$$G = \frac{V_{oMax} - V_{oMin}}{V_{idiffMax} - V_{idiffMin}} = \frac{2.5V - (-2.5V)}{1.25V - (-1.25V)} = 2 \frac{V}{V} = 6.02dB$$

3. Calculate the values for  $R_3$  and  $R_4$ .

$$G = 2 \frac{V}{V} = \frac{R_3}{R_1} \rightarrow 2 \times R_1 = R_3 = R_4 = 20k\Omega$$

4. Calculate resistor tolerance to meet the minimum common-mode rejection ratio (CMRR). For minimum (worst-case) CMRR,  $\alpha = 4$ . For a more probable, or typical value of CMRR,  $\alpha = 0.33$ .

$$CMRR_{dB} \cong 20\log_{10}\left(\frac{1+G}{\alpha \times \varepsilon}\right) \quad ( ) \quad ( )$$

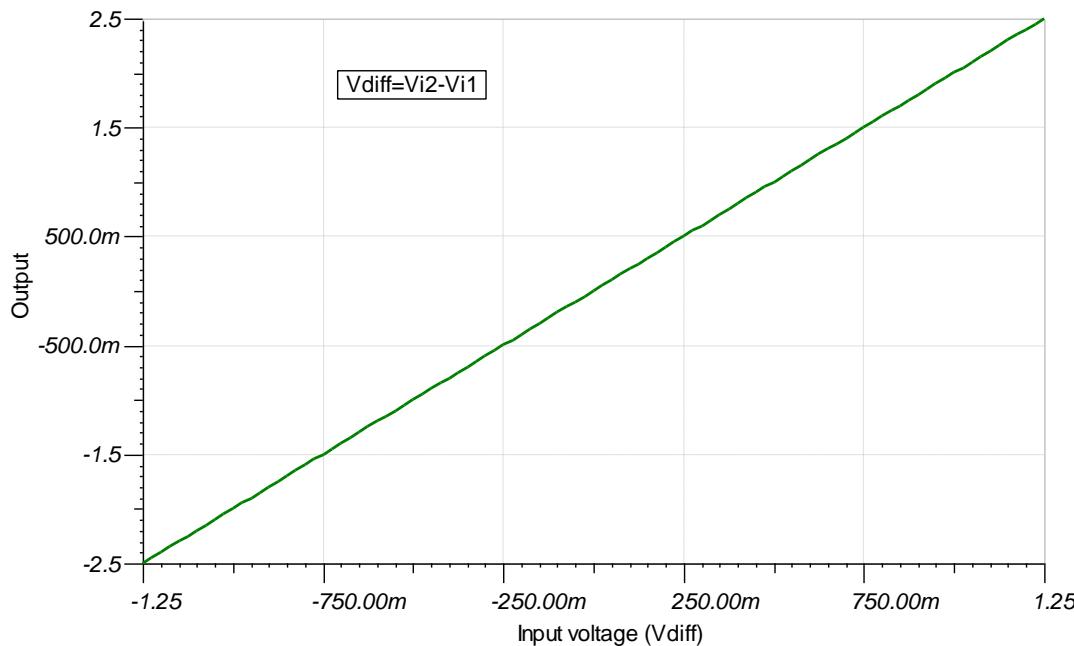
$$\varepsilon = \frac{1+G}{\alpha \times 10^{\frac{CMRR_{dB}}{20}}} = \frac{3}{4 \times 10^{\frac{50}{20}}} = 0.024 = 0.24\% \rightarrow \text{Use } 0.1\% \text{ resistors}$$

5. For quick reference, the following table compares resistor tolerance to minimum and typical CMRR values assuming  $G = 1$  or  $G = 2$ . As shown above, as gain increases so does CMRR.

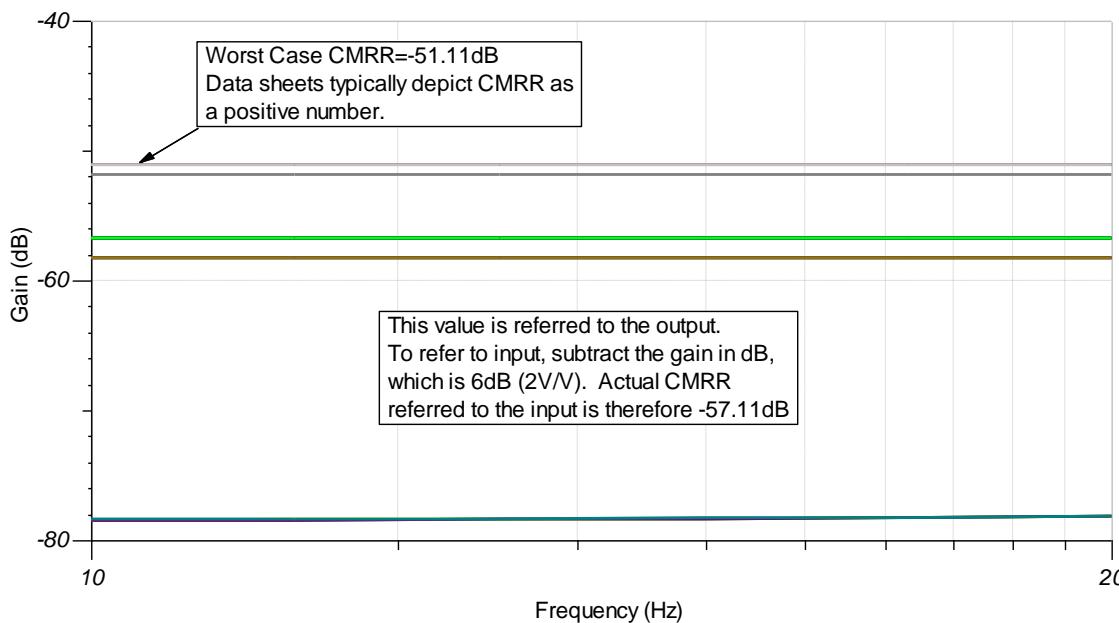
Tolerance	G=1 Minimum (dB)	G=1 Typical (dB)	G=2 Minimum (dB)	G=2 Typical (dB)
0.01% = 0.0001	74	95.6	77.5	99.2
0.1% = 0.001	54	75.6	57.5	79.2
0.5% = 0.005	40	61.6	43.5	65.2
1% = 0.01	34	55.6	37.5	59.2
5% = 0.05	20	41.6	23.5	45.2

## Design Simulations

### DC Simulation Results



### CMRR Simulation Results



## Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOC495](#).

For more information on many op amp topics including common-mode range, output swing, bandwidth, and how to drive an ADC please visit [TI Precision Labs](#). For more information on difference amplifier CMRR, please read [Overlooking the obvious: the input impedance of a difference amplifier](#).

## Design Featured Op Amp

TLV6001	
$V_{ss}$	1.8V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	750 $\mu$ V
$I_q$	75 $\mu$ A
$I_b$	1pA
<b>UGBW</b>	1MHz
<b>SR</b>	0.5V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/tlv6001">www.ti.com/product/tlv6001</a>	

## Design Alternate Op Amp

OPA320	
$V_{ss}$	1.8V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	40 $\mu$ V
$I_q$	1.5mA
$I_b$	0.2pA
<b>UGBW</b>	20MHz
<b>SR</b>	10V/ $\mu$ s
<b>#Channels</b>	1, 2
<a href="http://www.ti.com/product/opa320">www.ti.com/product/opa320</a>	

## Revision History

Revision	Date	Change
A	January 2019	Downscale title. Added link to circuit cookbook landing page.

## Two op amp instrumentation amplifier circuit

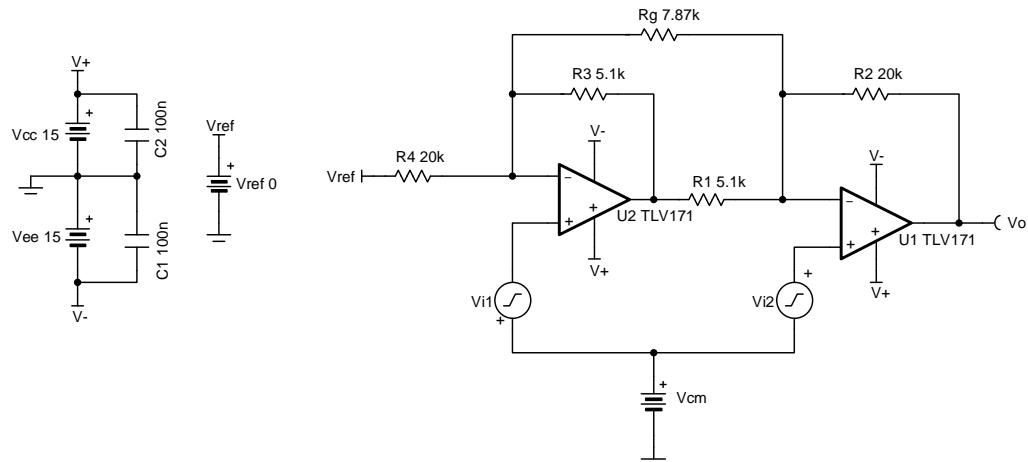
### Design Goals

Input $V_{iDiff}(V_{i2} - V_{i1})$		Output		Supply		
$V_{iDiff\_Min}$	$V_{iDiff\_Max}$	$V_{oMin}$	$V_{oMax}$	$V_{cc}$	$V_{ee}$	$V_{ref}$
+/-1V	+/-2V	-10V	+10V	15V	-15V	0V

$V_{cm}$	Gain Range
+/-10V	5V/V to 10V/V

### Design Description

This design amplifies the difference between  $V_{i1}$  and  $V_{i2}$  and outputs a single ended signal while rejecting the common-mode voltage. Linear operation of an instrumentation amplifier depends upon the linear operation of its primary building block: op amps. An op amp operates linearly when the input and output signals are within the device's input common-mode and output-swing ranges, respectively. The supply voltages used to power the op amps define these ranges.



### Design Notes

1.  $R_g$  sets the gain of the circuit.
2. High-value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
3. The ratio of  $R_4$  and  $R_3$  set the minimum gain when  $R_g$  is removed.
4. Ratios of  $R_2/R_1$  and  $R_4/R_3$  must be matched to avoid degrading the instrumentation amplifier's DC CMRR and ensuring the  $V_{ref}$  gain is 1V/V.
5. Linear operation is contingent upon the input common-mode and the output swing ranges of the discrete op amps used. The linear output swing ranges are specified under the  $A_{ol}$  test conditions in the op amps datasheets.

## Design Steps

1. Transfer function of this circuit.

$$V_o = V_{iDiff} \times G + V_{ref} = (V_{i2} - V_{i1}) \times G + V_{ref}$$

when  $V_{ref} = 0$ , the transfer function simplifies to the following equation:

$$V_o = (V_{i2} - V_{i1}) \times G$$

where  $G$  is the gain of the instrumentation amplifier and  $G = 1 + \frac{R_4}{R_3} + \frac{2R_2}{R_g}$

2. Select  $R_4$  and  $R_3$  to set the minimum gain.

$$G_{min} = 1 + \frac{R_4}{R_3} = 5 \frac{V}{V}$$

Choose  $R_4 = 20k\Omega$

$$G_{min} = 1 + \frac{20k\Omega}{R_3} = 5 \frac{V}{V}$$

$$R_3 = \frac{R_4}{5-1} = \frac{20k\Omega}{4} = 5k\Omega \rightarrow R_3 = 5.1k\Omega \text{ (Standard Value)}$$

3. Select  $R_1$  and  $R_2$ . Ensure that  $R_1/R_2$  and  $R_3/R_4$  ratios are matched to set the gain applied to the reference voltage at 1V/V.

$$\frac{V_{o\_ref}}{V_{ref}} = \left( -\frac{R_3}{R_4} \right) \times \left( -\frac{R_2}{R_1} \right) = \frac{R_3 \times R_2}{R_4 \times R_1} = 1 \frac{V}{V}$$

$$\frac{R_2}{R_1} = \frac{R_4}{R_3} \rightarrow R_1 = R_3 = 5.1k\Omega \text{ and } R_2 = R_4 = 20k\Omega \text{ (Standard Value)}$$

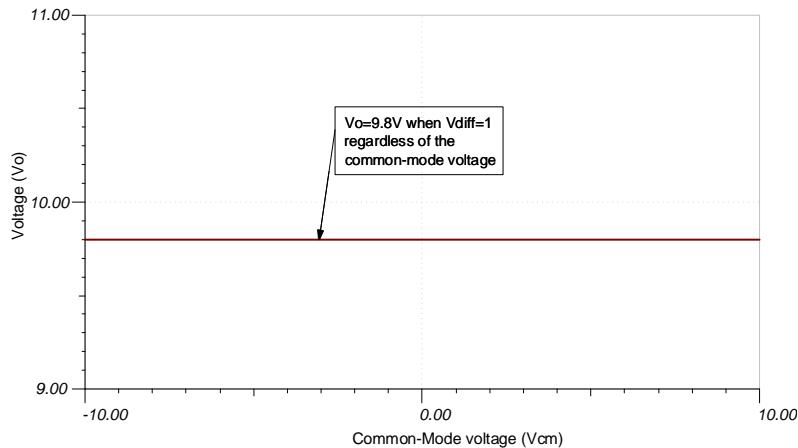
4. Select  $R_g$  to meet the desired maximum gain  $G = 10V/V$ .

$$G = 1 + \frac{R_4}{R_3} + \frac{2R_2}{R_g} = 1 + \frac{20k\Omega}{5.1k\Omega} + \frac{2 \times 20k\Omega}{R_g} = 10 \frac{V}{V}$$

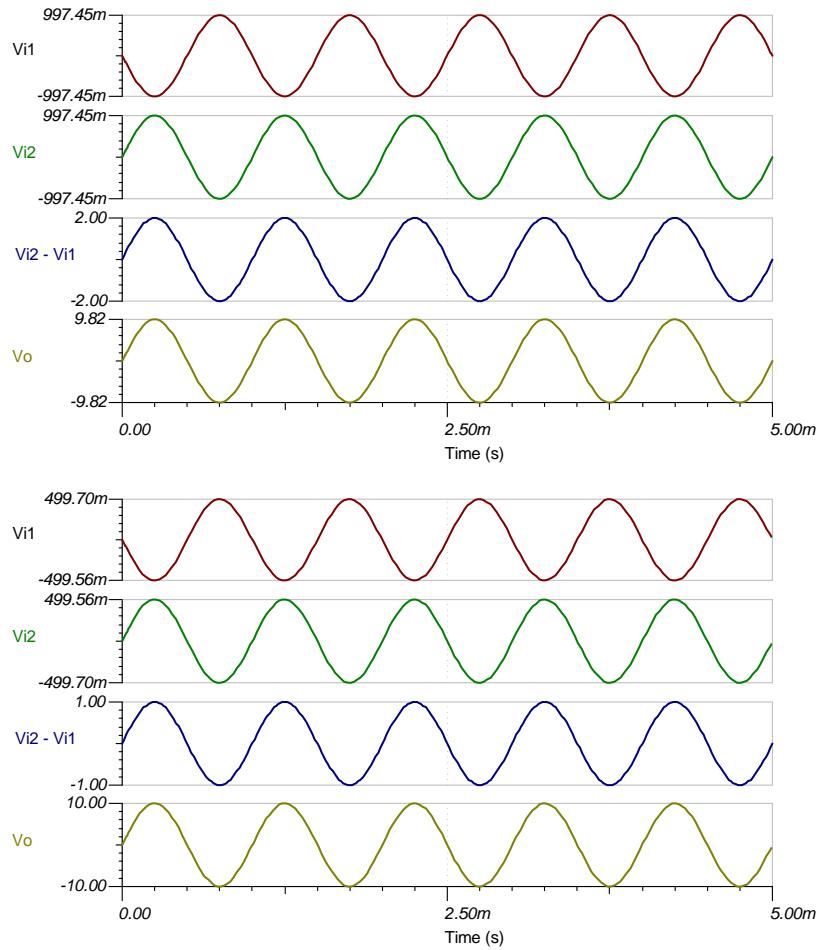
$$R_g = 8k\Omega \rightarrow R_g = 7.87k\Omega \text{ (Standard Value)}$$

## Design Simulations

### DC Simulation Results



### Transient Simulation Results



**References:**

1. [Analog Engineer's Circuit Cookbooks](#)
2. [SPICE Simulation File SBOMAU7](#)
3. [TI Precision Labs](#)
4. [V<sub>CM</sub> vs. V<sub>OUT</sub> plots for instrumentation amplifiers with two op amps](#)
5. [Common-mode Range Calculator for Instrumentation Amplifiers](#)

**Design Featured Op Amp**

TLV171	
<b>V<sub>ss</sub></b>	4.5V to 36V
<b>V<sub>inCM</sub></b>	(V <sub>ee</sub> –0.1V) to (V <sub>cc</sub> –2V)
<b>V<sub>out</sub></b>	Rail-to-rail
<b>V<sub>os</sub></b>	0.25mV
<b>I<sub>q</sub></b>	475 $\mu$ A
<b>I<sub>b</sub></b>	8pA
<b>UGBW</b>	3MHz
<b>SR</b>	1.5V/ $\mu$ s
<b>#Channels</b>	1,2,4
<a href="http://www.ti.com/product/tlv171">www.ti.com/product/tlv171</a>	

**Design Alternate Op Amp**

OPA172	
<b>V<sub>ss</sub></b>	4.5V to 36V
<b>V<sub>inCM</sub></b>	(V <sub>ee</sub> –0.1V) to (V <sub>cc</sub> –2V)
<b>V<sub>out</sub></b>	Rail-to-rail
<b>V<sub>os</sub></b>	0.2mV
<b>I<sub>q</sub></b>	1.6mA
<b>I<sub>b</sub></b>	8pA
<b>UGBW</b>	10MHz
<b>SR</b>	10V/ $\mu$ s
<b>#Channels</b>	1,2,4
<a href="http://www.ti.com/product/opa172">www.ti.com/product/opa172</a>	

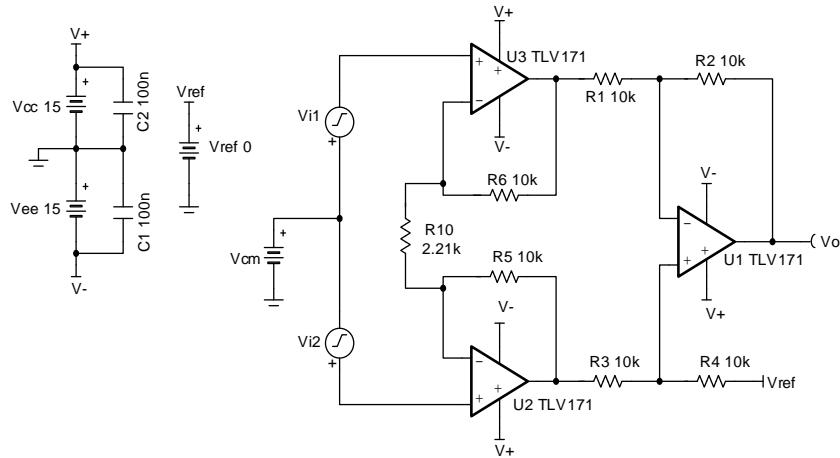
## Three op amp instrumentation amplifier circuit

### Design Goals

Input $V_{idiff}$ ( $V_{i2} - V_{i1}$ )		Common-mode Voltage	Output		Supply		
$V_{i\text{ diff Min}}$	$V_{i\text{ diff Max}}$	$V_{cm}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	$V_{cc}$	$V_{ee}$	$V_{ref}$
-0.5V	+0.5V	$\pm 7V$	-5V	+5V	+15V	-15V	0V

### Design Description

This design uses 3 op amps to build a discrete instrumentation amplifier. The circuit converts a differential signal to a single-ended output signal. Linear operation of an instrumentation amplifier depends upon linear operation of its building block: op amps. An op amp operates linearly when the input and output signals are within the device's input common-mode and output swing ranges, respectively. The supply voltages used to power the op amps define these ranges.



### Design Notes

1. Use precision resistors to achieve high DC CMRR performance
2.  $R_{10}$  sets the gain of the circuit.
3. Add an isolation resistor to the output stage to drive large capacitive loads.
4. High-value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
5. Linear operation is contingent upon the input common-mode and the output swing ranges of the discrete op amps used. The linear output swing ranges are specified under the  $A_{ol}$  test conditions in the op amps datasheets.

## Design Steps

1. Transfer function of this circuit:

$$V_o = (V_{i2} - V_{i1}) \times G + V_{ref}$$

When  $V_{ref} = 0$ , the transfer function simplifies to the following equation:

$$V_o = (V_{i2} - V_{i1}) \times G$$

$$\text{where } G = \frac{R_4}{R_3} \times 1 + \frac{2 \times R_5}{R_{10}}$$

2. Select the feedback loop resistors  $R_5$  and  $R_6$ :

Choose  $R_5 = R_6 = 10 \text{ k}\Omega$  (Standard Value)

3. Select  $R_1$ ,  $R_2$ ,  $R_3$ ,  $R_4$ . To set the Vref gain at 1V/V and avoid degrading the instrumentation amplifier's CMRR, ratios of  $R_4/R_3$  and  $R_2/R_1$  must be equal.

Choose  $R_1 = R_2 = R_3 = R_4 = 10 \text{ k}\Omega$  (Standard Value)

4. Calculate  $R_{10}$  to meet the desired gain:

$$G = \frac{R_4}{R_3} \times \left(1 + \frac{2 \times R_5}{R_{10}}\right) = 10 \frac{V}{V} \quad (1)$$

$$R_4 = R_3 = 10 \text{ k}\Omega$$

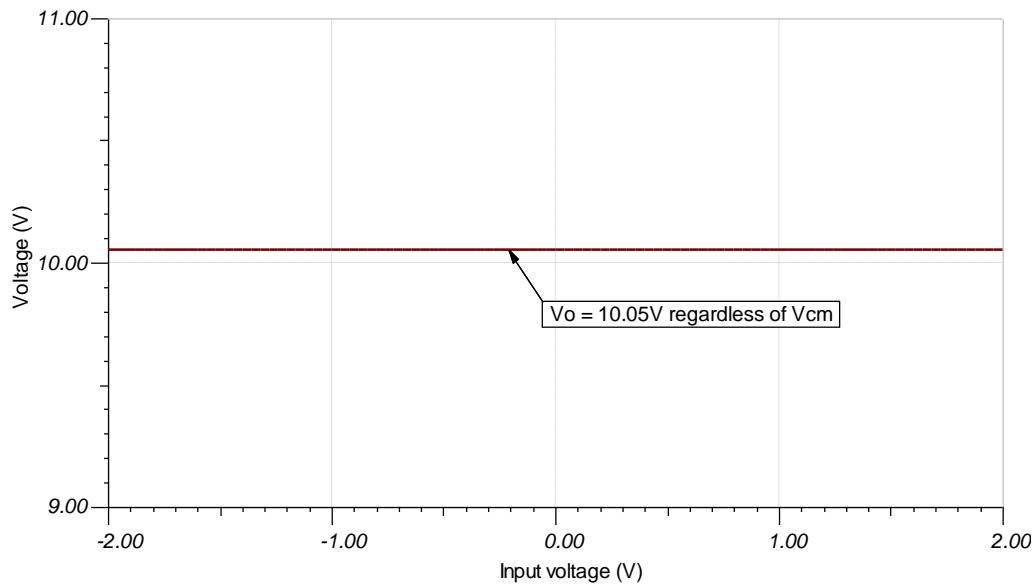
$$\rightarrow G = 1 + \frac{2 \times 10 \text{ k}\Omega}{R_{10}} = 10 \frac{V}{V} \rightarrow 1 + \frac{20 \text{ k}\Omega}{R_{10}} = 10 \frac{V}{V}$$

$$\frac{20 \text{ k}\Omega}{R_{10}} = 9 \frac{V}{V} \rightarrow R_{10} = \frac{20 \text{ k}\Omega}{9} = 2222.2 \Omega \rightarrow R_{10} = 2.21 \text{ k}\Omega \quad (1)$$

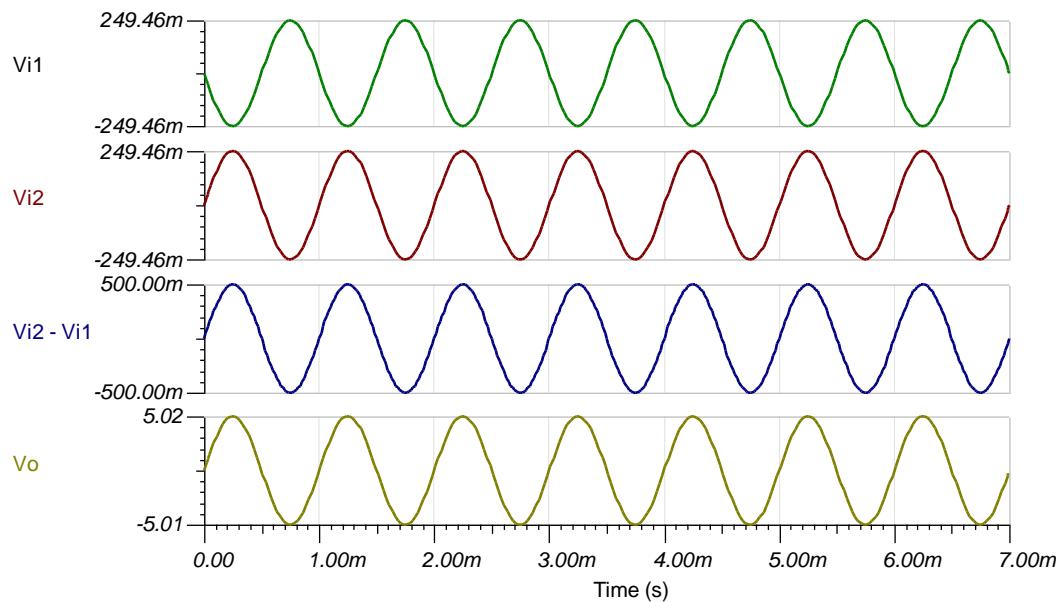
5. To check the common-mode voltage range, download and install the program from reference [5]. Edit the INA\_Data.txt file in the installation directory by adding the code for a 3 op amp INA whose internal amplifiers have the common-mode range, output swing, and supply voltage range as defined by the amplifier of choice (TLV172 in this case). There is no  $V_{be}$  shift in this design and the gain of the output stage difference amplifier is 1 V/V. The default supply voltage and reference voltages are  $\pm 15 \text{ V}$  and  $0 \text{ V}$ , respectively. Run the program and set the gain and reference voltage accordingly. The resulting  $V_{CM}$  vs.  $V_{OUT}$  plot approximates the linear operating region of the discrete INA.

## Design Simulations

### DC Simulation Results



### Transient Simulation Results



**References:**

1. [Analog Engineer's Circuit Cookbooks](#)
2. [SPICE Simulation File SBOMAU8](#)
3. [TI Precision Labs](#)
4. [Instrumentation Amplifier  \$V\_{CM}\$  vs.  \$V\_{OUT}\$  Plots](#)
5. [Common-mode Range Calculator for Instrumentation Amplifiers](#)

**Design Featured Op Amp**

TLV171	
$V_{ss}$	4.5V to 36V
$V_{inCM}$	$(V-) - 0.1V < V_{in} < (V+) - 2V$
$V_{out}$	Rail-to-rail
$V_{os}$	0.25mV
$I_q$	475 $\mu$ A
$I_b$	8pA
<b>UGBW</b>	3MHz
<b>SR</b>	1.5V/ $\mu$ s
<b>#Channels</b>	1,2,4
<a href="http://www.ti.com/product/tlv171">www.ti.com/product/tlv171</a>	

**Design Alternate Op Amp**

	OPA172	OPA192
$V_{ss}$	4.5V to 36V	4.5V to 36V
$V_{inCM}$	$(V-) - 0.1V < V_{in} < (V+) - 2V$	$V_{ee} - 0.1V < V_{cc} < V_{ee} + 0.1V$
$V_{out}$	Rail-to-rail	Rail-to-rail
$V_{os}$	0.2mV	$\pm 5\mu$ V
$I_q$	1.6mA	1mA/Ch
$I_b$	8pA	5pA
<b>UGBW</b>	10MHz	10MHz
<b>SR</b>	10V/ $\mu$ s	20V/ $\mu$ s
<b>#Channels</b>	1,2,4	1, 2, 4
	<a href="http://www.ti.com/product/opa172">www.ti.com/product/opa172</a>	<a href="http://www.ti.com/product/opa192">www.ti.com/product/opa192</a>

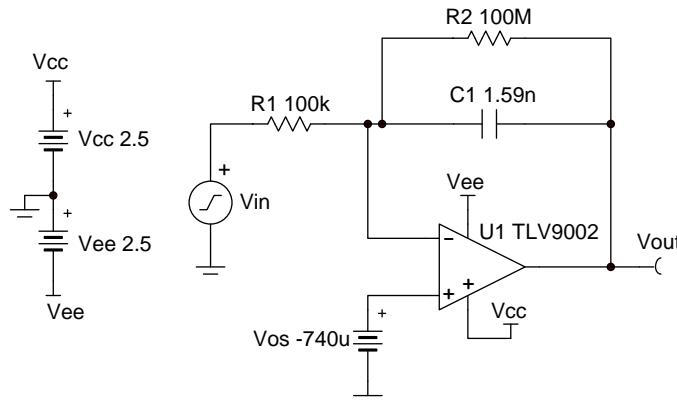
## ***Integrator circuit***

### **Design Goals**

Input			Output		Supply	
$f_{\text{Min}}$	$f_{0\text{dB}}$	$f_{\text{Max}}$	$V_{\text{oMin}}$	$V_{\text{oMax}}$	$V_{\text{cc}}$	$V_{\text{ee}}$
100Hz	1kHz	100kHz	-2.45V	2.45V	2.5V	-2.5V

### **Design Description**

The integrator circuit outputs the integral of the input signal over a frequency range based on the circuit time constant and the bandwidth of the amplifier. The input signal is applied to the inverting input so the output is inverted relative to the polarity of the input signal. The ideal integrator circuit will saturate to the supply rails depending on the polarity of the input offset voltage and requires the addition of a feedback resistor,  $R_2$ , to provide a stable DC operating point. The feedback resistor limits the lower frequency range over which the integration function is performed. This circuit is most commonly used as part of a larger feedback/servo loop which provides the DC feedback path, thus removing the requirement for a feedback resistor.



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### **Design Notes**

1. Use as large of a value as practical for the feedback resistor.
2. Select a CMOS op amp to minimize the errors from the input bias current.
3. The gain bandwidth product (GBP) of the amplifier will set the upper frequency range of the integrator function. The effectiveness of the integration function is usually reduced starting about one decade away from the amplifier bandwidth.
4. An adjustable reference needs to be connected to the non-inverting input of the op amp to cancel the input offset voltage or the large DC noise gain will cause the circuit to saturate. Op amps with very low offset voltage may not require this.

## Design Steps

The ideal circuit transfer function is given below.

$$V_{\text{out}} = -\frac{1}{R_1 \times C_1} \int_0^t V_{\text{in}}(t) dt$$

1. Set  $R_1$  to a standard value.

$$R_1 = 100\text{k}\Omega$$

2. Calculate  $C_1$  to set the unity-gain integration frequency.

$$C_1 = \frac{1}{2 \times \pi \times R_1 \times f_{\text{0dB}}} = \frac{1}{2 \times \pi \times 100\text{k}\Omega \times 1 \text{ kHz}} = 1.59\text{nF}$$

3. Calculate  $R_2$  to set the lower cutoff frequency a decade less than the minimum operating frequency.

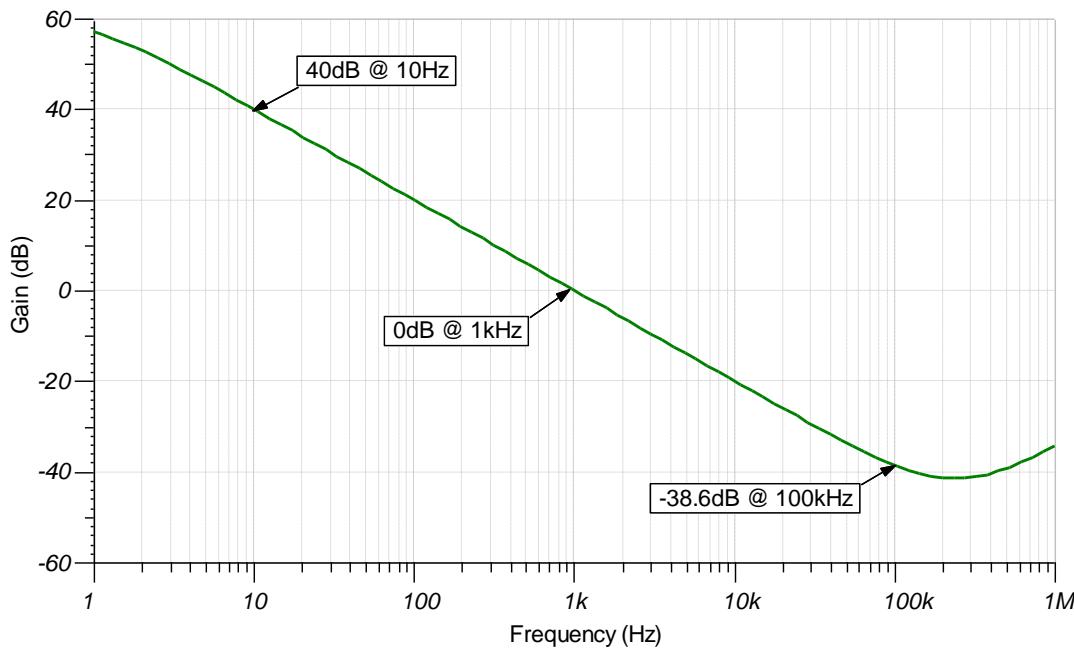
$$R_2 \geq \frac{10}{2 \times \pi \times C_1 \times f_{\text{Min}}} \geq \frac{10}{2 \times \pi \times 1.59\text{nF} \times 10\text{Hz}} \geq 100\text{M}\Omega$$

4. Select an amplifier with a gain bandwidth at least 10 times the desired maximum operating frequency.

$$\text{GBP} \geq 10 \times f_{\text{Max}} \geq 10 \times 100\text{kHz} \geq 1 \text{ MHz}$$

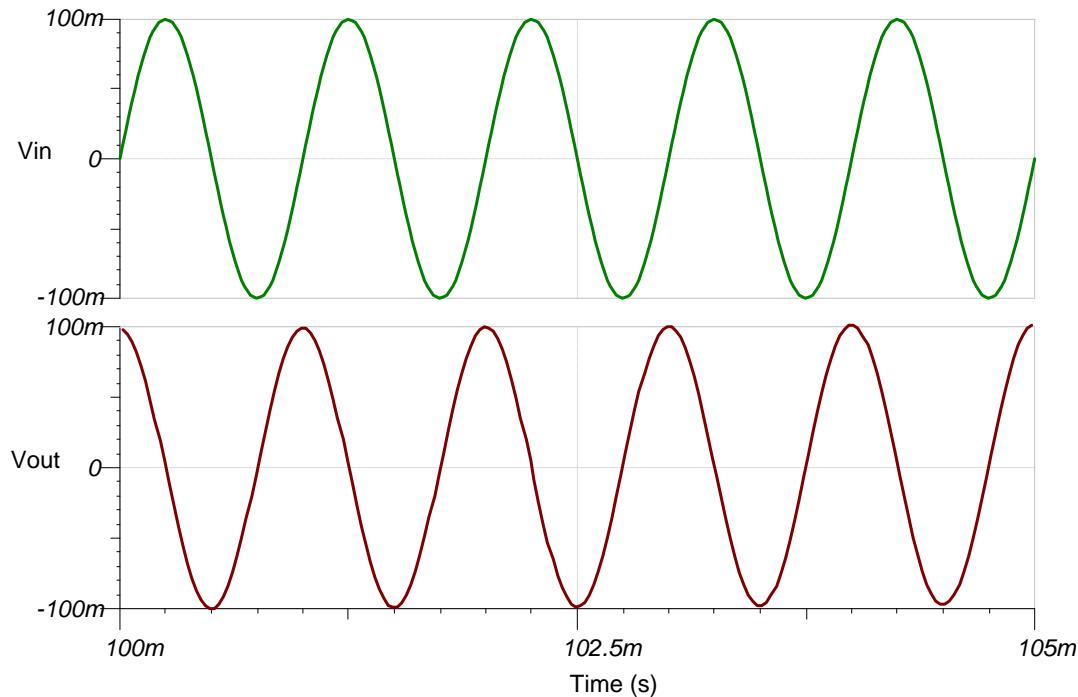
## Design Simulations

### AC Simulation Results

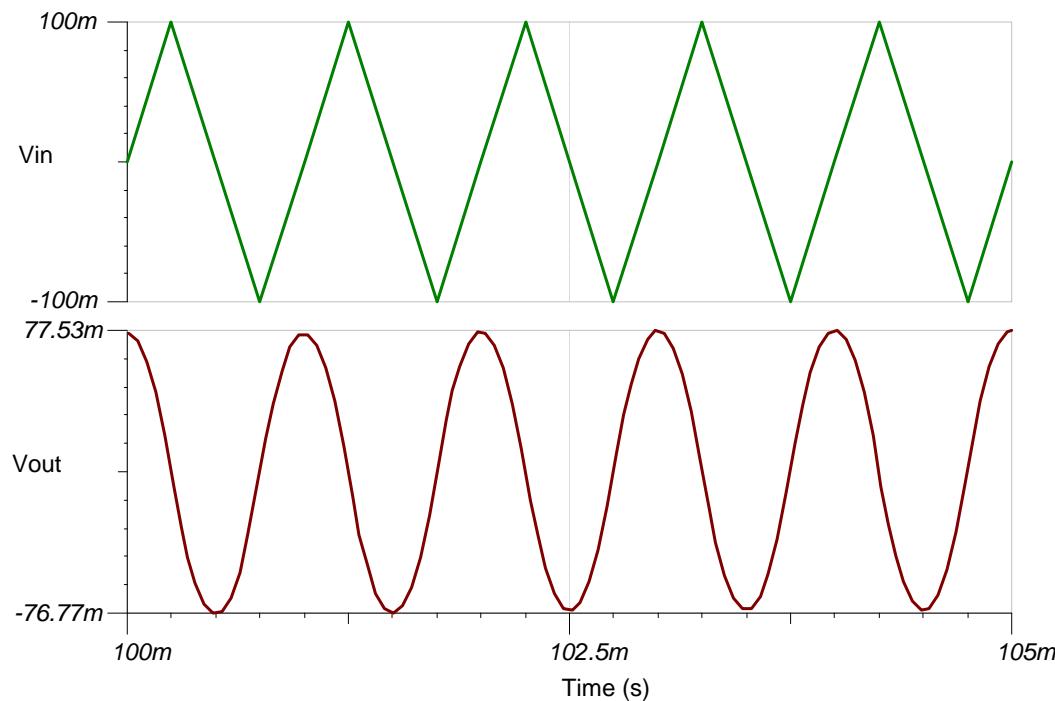


### Transient Simulation Results

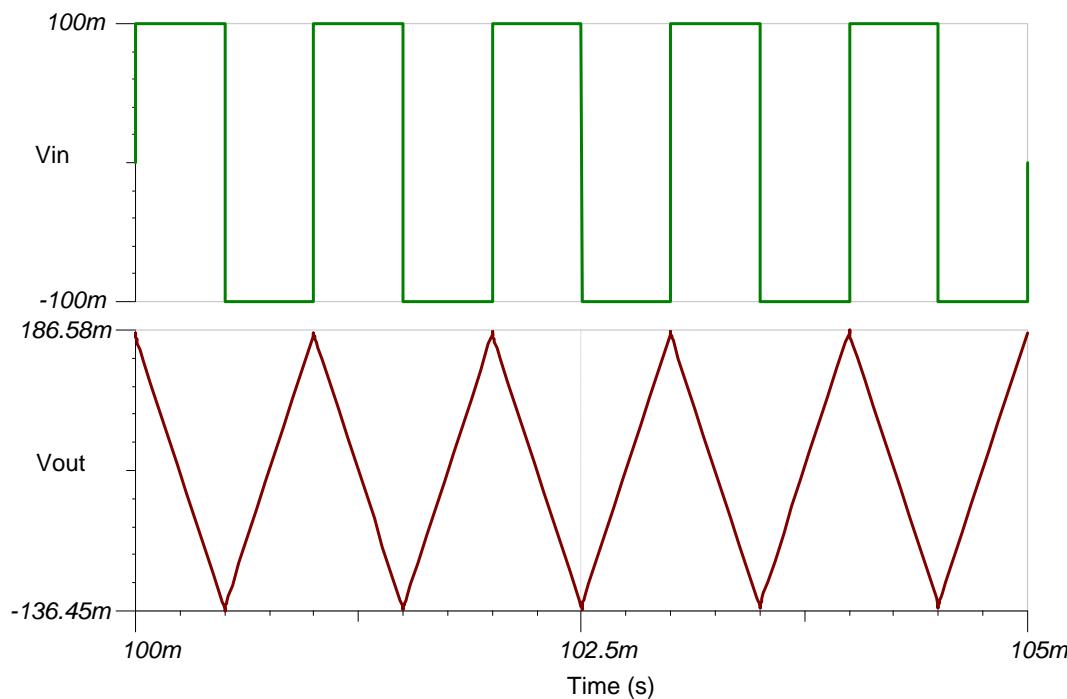
A 1-kHz sine wave input yields a 1-kHz cosine output.



A 1-kHz triangle wave input yields a 1-kHz sine wave output.



A 1-kHz square wave input yields a 1-kHz triangle wave output.



### Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOC496](#).

See TIPD191, [www.ti.com/tool/tipd191](http://www.ti.com/tool/tipd191).

### Design Featured Op Amp

TLV9002	
$V_{cc}$	1.8V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	0.4mV
$I_q$	0.06mA
$I_b$	5pA
<b>UGBW</b>	1MHz
<b>SR</b>	2V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/tlv9002">www.ti.com/product/tlv9002</a>	

### Design Alternate Op Amp

OPA376	
$V_{cc}$	2.2V to 5.5V
$V_{inCM}$	( $V_{ee}$ -0.1V) to ( $V_{cc}$ -1.3V)
$V_{out}$	Rail-to-rail
$V_{os}$	0.005mV
$I_q$	0.76mA
$I_b$	0.2pA
<b>UGBW</b>	5.5MHz
<b>SR</b>	2V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/opa376">www.ti.com/product/opa376</a>	

### Revision History

Revision	Date	Change
A	January 2019	Downscale the title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page.

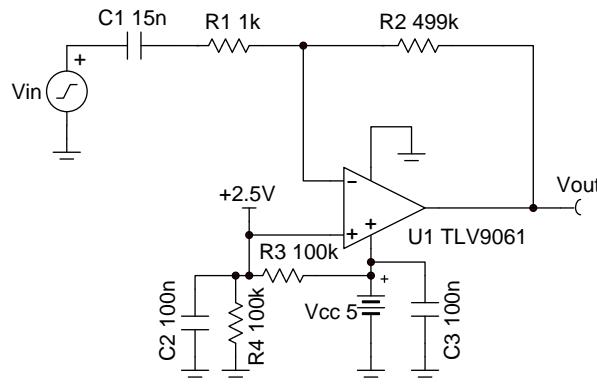
## Differentiator circuit

### Design Goals

Input		Output		Supply		
$f_{\text{Min}}$	$f_{\text{Max}}$	$V_{\text{oMin}}$	$V_{\text{oMax}}$	$V_{\text{cc}}$	$V_{\text{ee}}$	$V_{\text{ref}}$
100Hz	5kHz	0.1V	4.9V	5V	0V	2.5V

### Design Description

The differentiator circuit outputs the derivative of the input signal over a frequency range based on the circuit time constant and the bandwidth of the amplifier. The input signal is applied to the inverting input so the output is inverted relative to the polarity of the input signal. The ideal differentiator circuit is fundamentally unstable and requires the addition of an input resistor, a feedback capacitor, or both, to be stable. The components required for stability limit the bandwidth over which the differentiator function is performed.



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### Design Notes

1. Select a large resistance for  $R_2$  to keep the value of  $C_1$  reasonable.
2. A capacitor can be added in parallel with  $R_2$  to filter the high-frequency noise of the circuit. The capacitor will limit the effectiveness of the differentiator function starting about half a decade (approximately 3.5 times) away from the filter cutoff frequency.
3. A reference voltage can be applied to the non-inverting input to set the DC output voltage which allows the circuit to work single-supply. The reference voltage can be derived from a voltage divider.
4. Operate within the linear output voltage swing (see  $A_{\text{ol}}$  specification) to minimize non-linearity errors.

## Design Steps

The ideal circuit transfer function is given below.

$$V_{out} = -R_2 \times C_1 \times \frac{dV_{in}(t)}{dt}$$

1. Set  $R_2$  to a large standard value.

$$R_2 = 499\text{k}\Omega$$

2. Set the minimum differentiation frequency at least half a decade below the minimum operating frequency.

$$C_1 \geq \frac{3.5}{2 \times \pi \times R_2 \times f_{min}} \geq \frac{3.5}{2 \times \pi \times 499\text{k}\Omega \times 100\text{Hz}} \geq 11.1 \text{ nF} \approx 15\text{nF} \text{ (Standard Value)}$$

3. Set the upper cutoff frequency at least half a decade above the maximum operating frequency.

$$R_1 \leq \frac{1}{3.5 \times 2 \times \pi \times C_1 \times f_{Max}} \leq \frac{1}{7 \times \pi \times 15\text{nF} \times 2.5\text{kHz}} \leq 1.2\text{k}\Omega \approx 1 \text{ k}\Omega \text{ (Standard Value)}$$

4. Calculate the necessary op amp gain bandwidth product (GBP) for the circuit to be stable.

$$GBP > \frac{R_1 + R_2}{2 \times \pi \times R_1^2 \times C_1} > \frac{499\text{k}\Omega + 1 \text{ k}\Omega}{2 \times \pi \times 1 \text{ k}\Omega^2 \times 15\text{nF}} > 5.3\text{MHz}$$

- The bandwidth of the TLV9061 is 10MHz, therefore this requirement is met.

5. If a feedback capacitor,  $C_F$ , is added in parallel with  $R_2$ , the equation to calculate the cutoff frequency follows.

$$f_c = \frac{1}{2 \times \pi \times R_2 \times C_F}$$

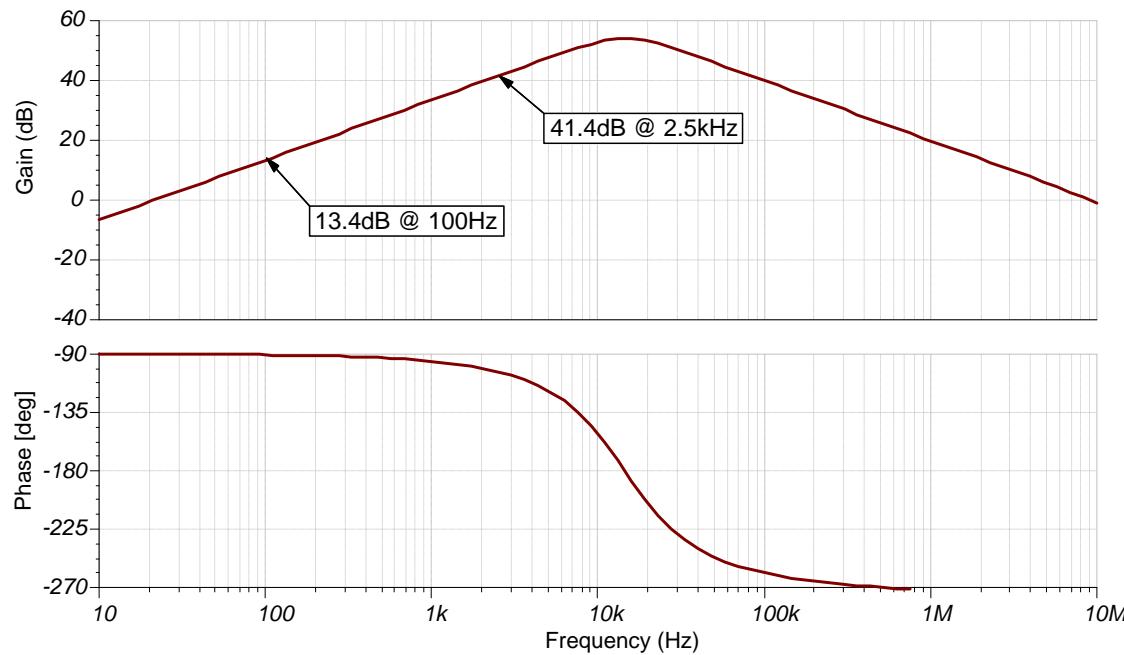
6. Calculate the resistor divider values for a 2.5-V reference voltage.

$$R_3 = \frac{V_{cc} - V_{ref}}{V_{ref}} \times R_4 = \frac{5\text{V} - 2.5\text{V}}{2.5\text{V}} \times R_4 = R_4$$

$$R_3 = R_4 = 100\text{k}\Omega \text{ (Standard Values)}$$

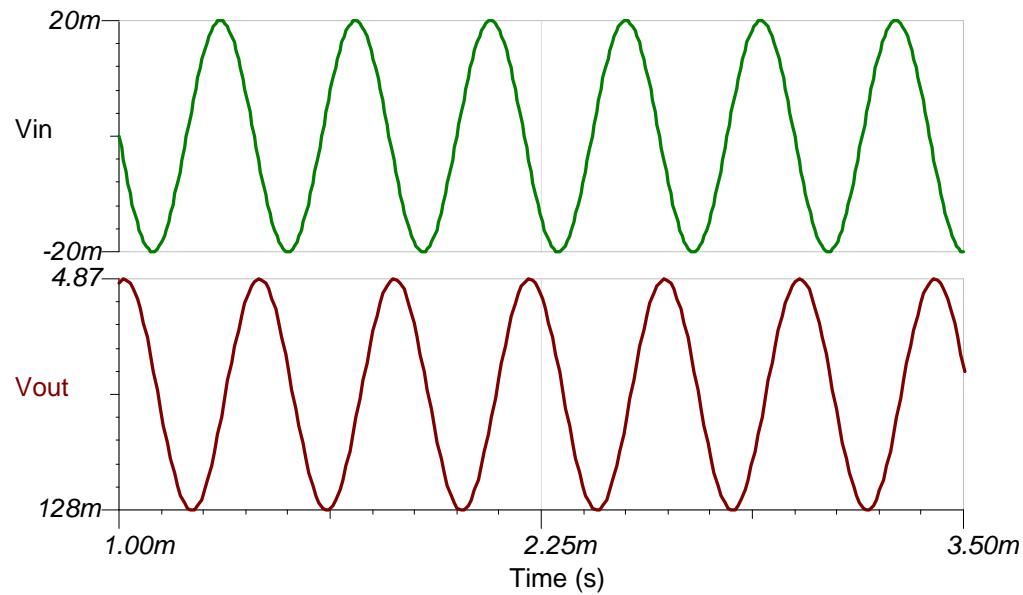
## Design Simulations

### AC Simulation Results

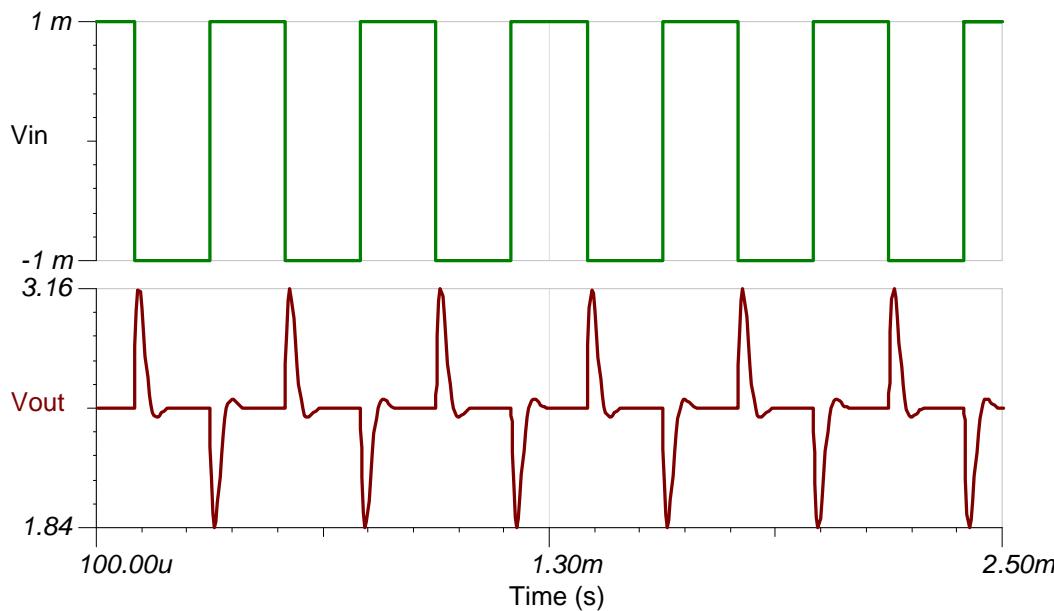


### Transient Simulation Results

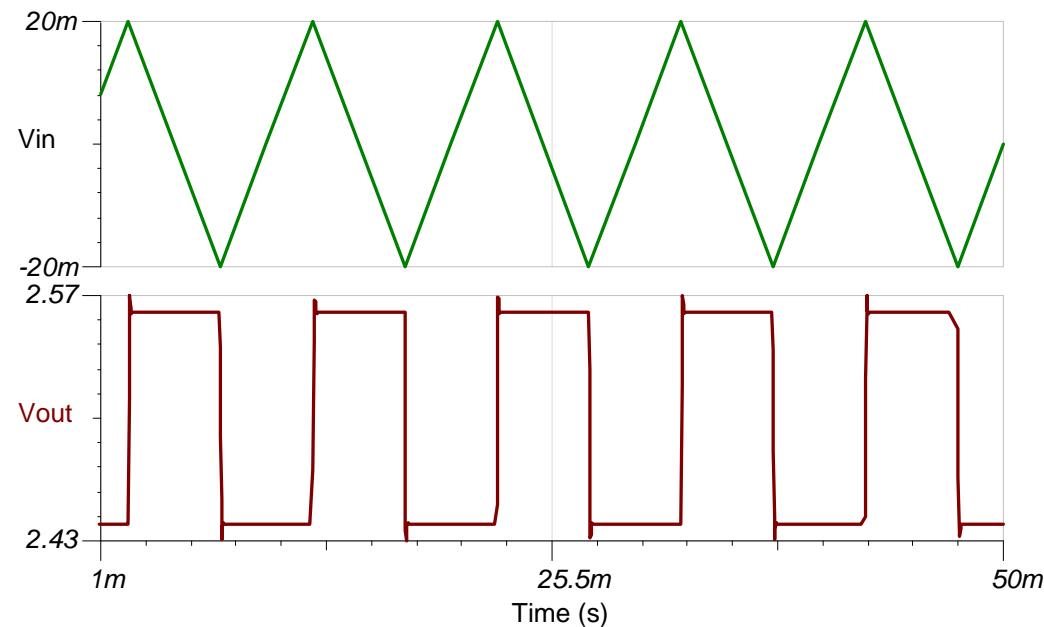
A 2.5-kHz sine wave input yields a 2.5-kHz cosine output.



A 2.5-kHz square wave input produces an impulse output.



A 100-Hz triangle wave input yields a square wave output.



### Design Featured Op Amp

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOC497](#).

TLV9061	
$V_{cc}$	1.8V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	0.3mV
$I_q$	0.538mA
$I_b$	0.5pA
<b>UGBW</b>	10MHz
<b>SR</b>	6.5V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/tlv9061">www.ti.com/product/tlv9061</a>	

### Design Alternate Op Amp

OPA374	
$V_{cc}$	2.3V to 5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	1mV
$I_q$	0.585mA
$I_b$	0.5pA
<b>UGBW</b>	6.5MHz
<b>SR</b>	0.4V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/opa374">www.ti.com/product/opa374</a>	

### Revision History

Revision	Date	Change
A	January 2019	Downscale the title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page.

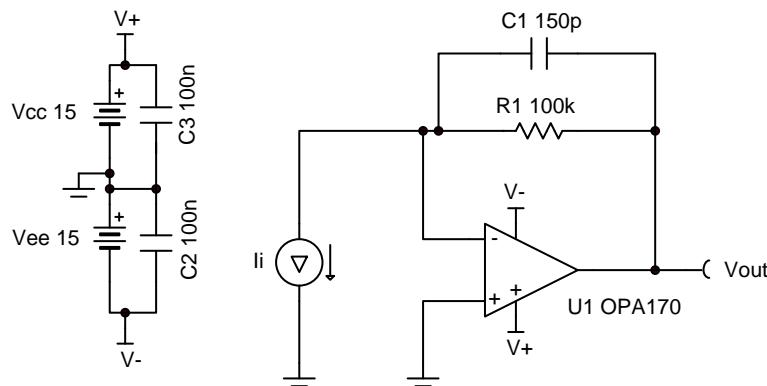
## Transimpedance amplifier circuit

### Design Goals

Input		Output		BW	Supply	
$I_{iMin}$	$I_{iMax}$	$V_{oMin}$	$V_{oMax}$	$f_p$	$V_{cc}$	$V_{ee}$
0A	50 $\mu$ A	0V	5V	10kHz	15V	-15V

### Design Description

The transimpedance op amp circuit configuration converts an input current source into an output voltage. The current to voltage gain is based on the feedback resistance. The circuit is able to maintain a constant voltage bias across the input source as the input current changes which benefits many sensors.



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### Design Notes

1. Use a JFET or CMOS input op amp with low bias current to reduce DC errors.
2. A bias voltage can be added to the non-inverting input to set the output voltage for 0-A input currents.
3. Operate within the linear output voltage swing (see  $A_{oi}$  specification) to minimize non-linearity errors.

## Design Steps

1. Select the gain resistor.

$$R_1 = \frac{V_{oMax} - V_{oMin}}{I_{iMax}} = \frac{5V - 0V}{50\mu A} = 100k\Omega$$

2. Select the feedback capacitor to meet the circuit bandwidth.

$$C_1 \leq \frac{1}{2\pi \times R_1 \times f_p}$$

$$C_1 \leq \frac{1}{2\pi \times 100k\Omega \times 10kHz} \leq 159pF \approx 150pF \text{ (Standard Value)}$$

3. Calculate the necessary op amp gain bandwidth (GBW) for the circuit to be stable.

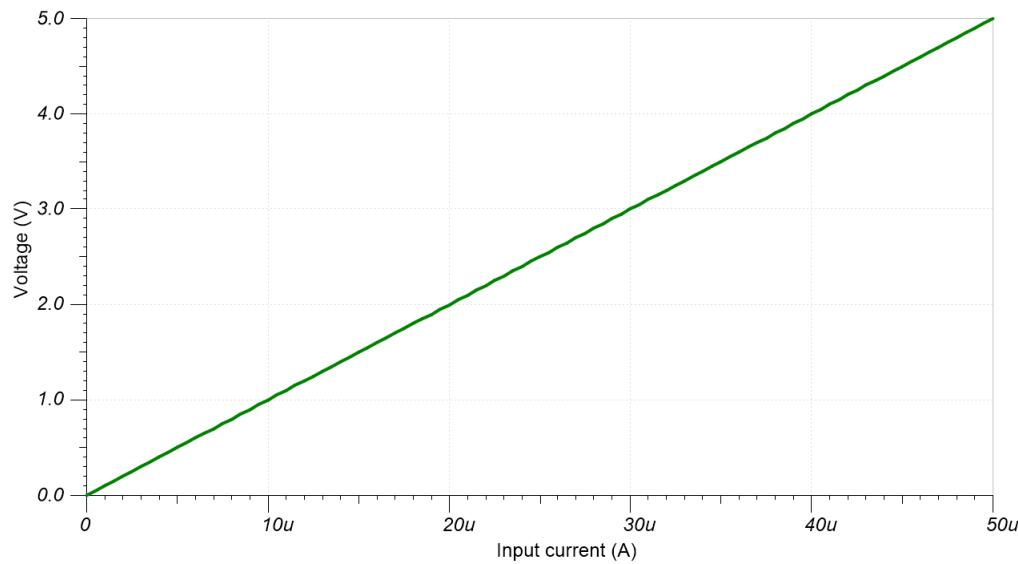
$$GBW > \frac{C_i + C_1}{2\pi \times R_1 \times C_1^2} > \frac{6pF + 150pF}{2\pi \times 100k\Omega \times (150pF)^2} > 11.03kHz$$

where  $C_i = C_s + C_d + C_{cm} = 0pF + 3pF + 3pF = 6pF$  given

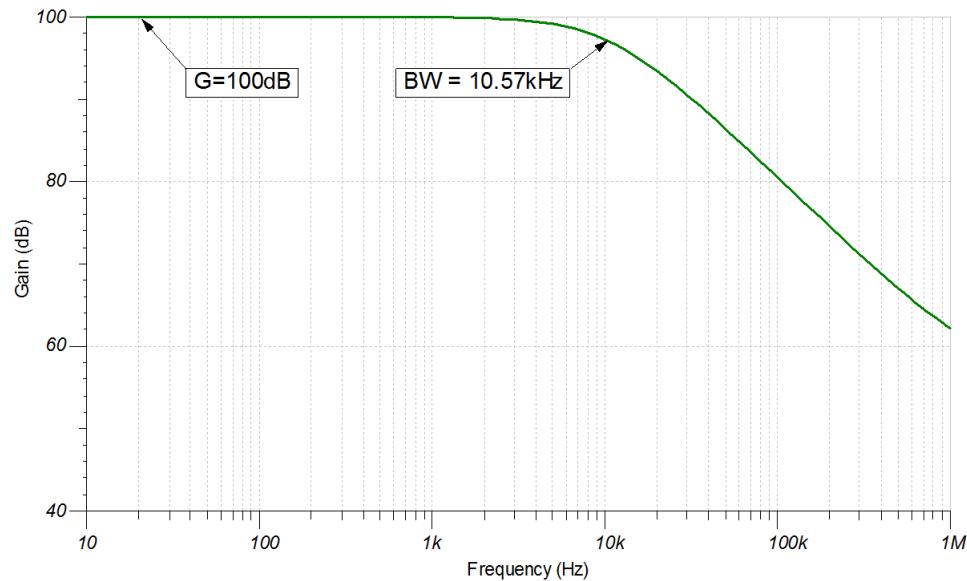
- $C_s$ : Input source capacitance
- $C_d$ : Differential input capacitance of the amplifier
- $C_{cm}$ : Common-mode input capacitance of the inverting input

## Design Simulations

### DC Simulation Results



### AC Simulation Results



## Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOC501](#).

See TIPD176, [www.ti.com/tool/tipd176](http://www.ti.com/tool/tipd176).

## Design Featured Op Amp

OPA170	
$V_{cc}$	2.7V to 36V
$V_{inCM}$	( $V_{ee}$ -0.1V) to ( $V_{cc}$ -2V)
$V_{out}$	Rail-to-rail
$V_{os}$	0.25mV
$I_q$	0.11mA
$I_b$	8pA
<b>UGBW</b>	1.2MHz
<b>SR</b>	0.4V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/opa170">www.ti.com/product/opa170</a>	

## Design Alternate Op Amp

OPA1671	
$V_{cc}$	1.7V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	( $V_{ee}$ +10mV) to ( $V_{cc}$ -10mV) @ 275 $\mu$ A
$V_{os}$	250 $\mu$ V
$I_q$	940 $\mu$ A
$I_b$	1pA
<b>UGBW</b>	12MHz
<b>SR</b>	5V/ $\mu$ s
<b>#Channels</b>	1
<a href="http://www.ti.com/product/opa1671">www.ti.com/product/opa1671</a>	

## Revision History

Revision	Date	Change
A	January 2019	Downscale the title and changed title role to 'Amplifiers'. Updated Design Alternate Op Amp table with OPA1671. Added link to circuit cookbook landing page.

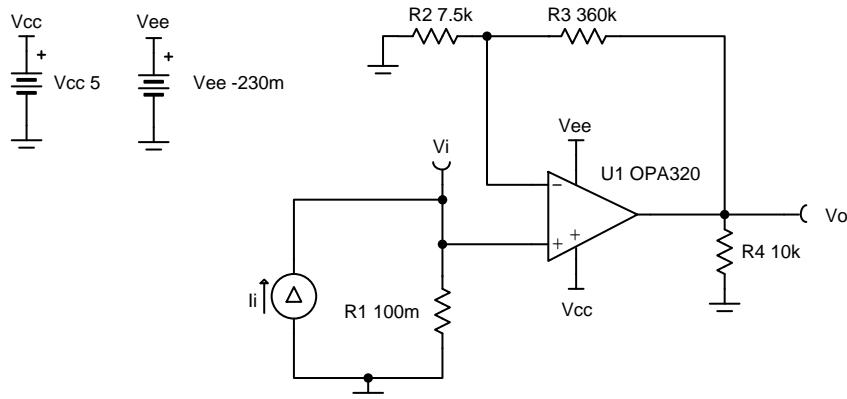
## **Single-supply, low-side, unidirectional current-sensing solution with output swing to GND circuit**

### **Design Goals**

<b>Input</b>		<b>Output</b>		<b>Supply</b>		
$I_{iMin}$	$I_{iMax}$	$V_{oMin}$	$V_{oMax}$	$V_{cc}$	$V_{ee}$	$V_{ref}$
0A	1A	0V	4.9V	5V	0V	0V

### **Design Description**

This single-supply, low-side, current sensing solution accurately detects load current between 0A to 1A and converts it to a voltage between 0V to 4.9V. The input current range and output voltage range can be scaled as necessary and larger supplies can be used to accommodate larger swings. A negative charge pump (such as the LM7705) is used as the negative supply in this design to maintain linearity for output signals near 0V.



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### **Design Notes**

1. Use precision resistors to minimize gain error.
2. For light load accuracy, the negative supply should extend slightly below ground.
3. A capacitor placed in parallel with the feedback resistor will limit bandwidth and help reduce noise.

### Design Steps

1. Determine the transfer function.

$$V_o = I_i \times R_1 \times \left(1 + \frac{R_3}{R_2}\right)$$

2. Define the full-scale shunt voltage and shunt resistance.

$$V_{iMax} = 100mV \text{ at } I_{iMax} = 1A$$

$$R_1 = \frac{V_{iMax}}{I_{iMax}} = \frac{100mV}{1 A} = 100m\Omega$$

3. Select gain resistors to set the output range.

$$V_{iMax} = 100mV \text{ and } V_{oMax} = 4.9V$$

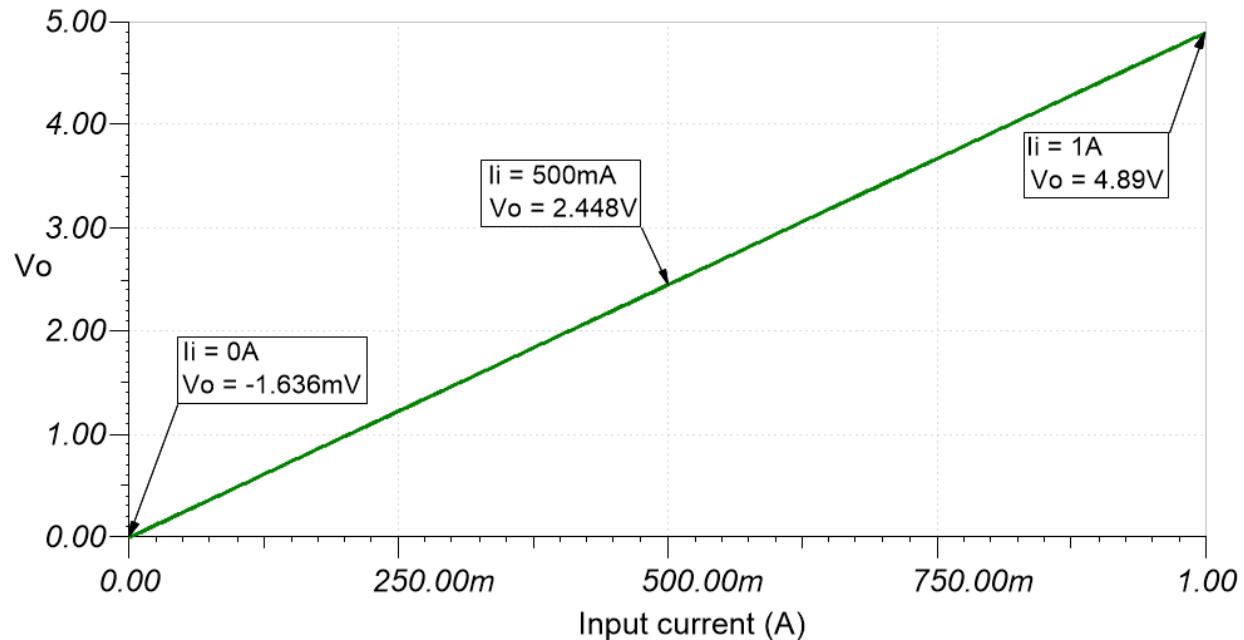
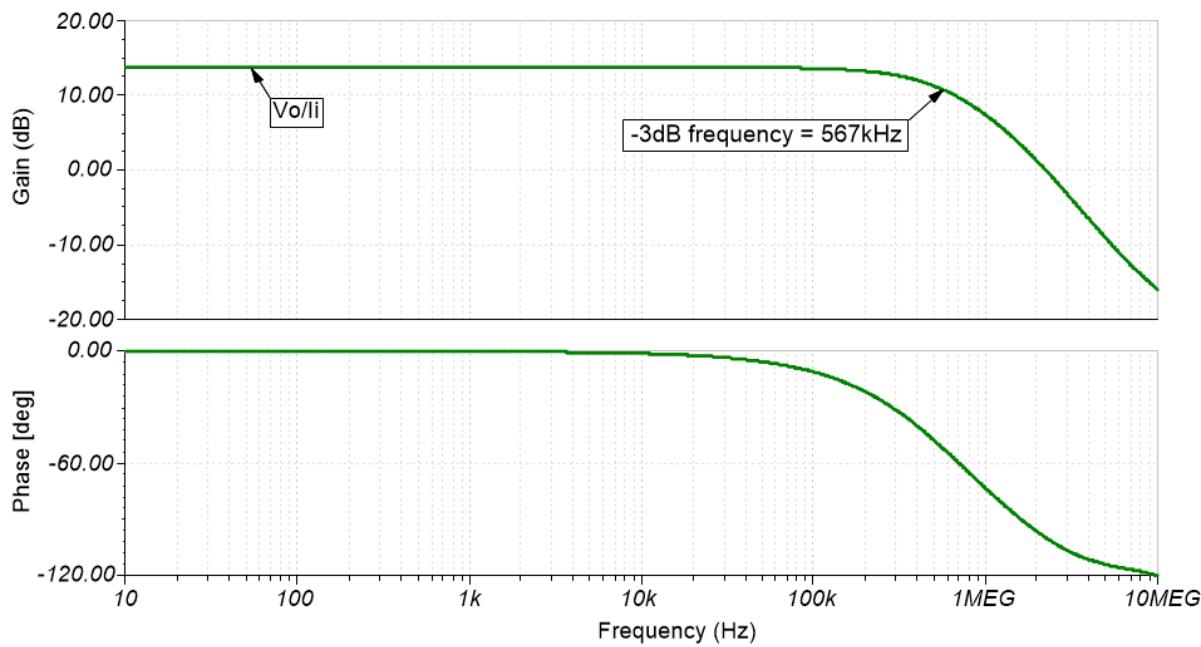
$$\text{Gain} = \frac{V_{oMax}}{V_{iMax}} = \frac{4.9V}{100mV} = 49V/V$$

$$\text{Gain} = 1 + \frac{R_3}{R_2} = 49V/V$$

4. Select a standard value for  $R_2$  and  $R_3$ .

$$R_2 = 7.5k\Omega \text{ (0.05% Standard Value)}$$

$$R_3 = 48 \times R_2 = 360k\Omega \text{ (0.05% Standard Value)}$$

**Design Simulations**
**DC Simulation Results**

**AC Simulation Results**


## Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOC499](#).

See TIPD129, [www.ti.com/tool/tipd129](http://www.ti.com/tool/tipd129).

## Design Featured Op Amp

OPA320	
$V_{cc}$	1.8V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	40 $\mu$ V
$I_q$	1.5mA/Ch
$I_b$	0.2pA
<b>UGBW</b>	10MHz
<b>SR</b>	10V/ $\mu$ s
<b>#Channels</b>	1, 2
<a href="http://www.ti.com/product/opa320">www.ti.com/product/opa320</a>	

## Design Alternate Op Amp

TLV9002	
$V_{cc}$	1.8V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	400 $\mu$ V
$I_q$	60 $\mu$ A
$I_b$	5pA
<b>UGBW</b>	1MHz
<b>SR</b>	2V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/tlv9002">www.ti.com/product/tlv9002</a>	

## Revision History

Revision	Date	Change
A	January 2019	Downscale the title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page.

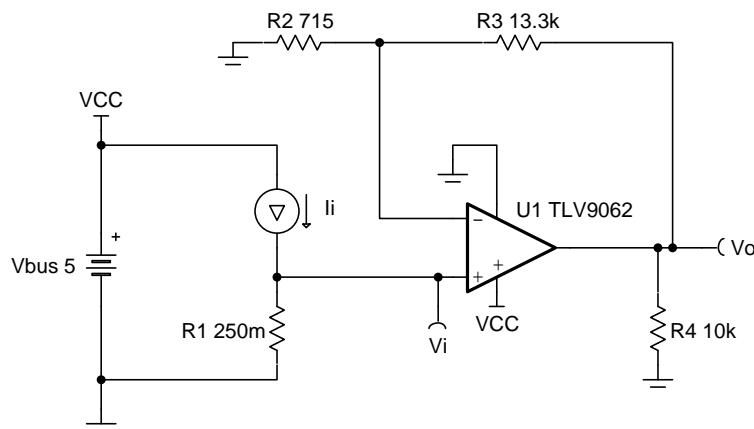
## **Single-supply, low-side, unidirectional current-sensing circuit**

### **Design Goals**

Input		Output		Supply		Full-Scale Range Error
$I_{i\text{Max}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	$V_{cc}$	$V_{ee}$	$\text{FSR}_{\text{Error}}$
1A	250mV	50mV	4.9V	5V	0V	0.2%

### **Design Description**

This single-supply, low-side, current sensing solution accurately detects load current up to 1A and converts it to a voltage between 50mV and 4.9V. The input current range and output voltage range can be scaled as necessary and larger supplies can be used to accommodate larger swings.



### **Design Notes**

1. Use the op amp linear output operating range, which is usually specified under the test conditions.
2. The common-mode voltage is equal to the input voltage.
3. Tolerance of the shunt resistor and feedback resistors will determine the gain error of the circuit.
4. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
5. If trying to detect zero current with output swing to GND, a negative charge pump (such as LM7705) can be used as the negative supply in this design to maintain linearity for output signals near 0V. [5]
6. Using high-value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
7. The small-signal bandwidth of this circuit depends on the gain of the circuit and gain bandwidth product (GBP) of the amplifier.
8. Filtering can be accomplished by adding a capacitor in parallel with  $R_3$ . Adding a capacitor in parallel with  $R_3$  will also improve stability of the circuit if high-value resistors are used.
9. For more information on op amp linear operating region, stability, capacitive load drive, driving ADCs, and bandwidth please see the Design References section.

## Design Steps

The transfer function for this circuit is given below.

$$V_o = I_i \times R_1 \times \left(1 + \frac{R_3}{R_2}\right)$$

1. Define the full-scale shunt voltage and calculate the maximum shunt resistance.

$$V_{iMax} = 250 \text{ mV} \text{ at } I_{iMax} = 1 \text{ A}$$

$$R_1 = \frac{V_{iMax}}{I_{iMax}} = \frac{250 \text{ mV}}{1 \text{ A}} = 250 \text{ m}\Omega$$

2. Calculate the gain required for maximum linear output voltage.

$$V_{iMax} = 250 \text{ mV} \text{ and } V_{oMax} = 4.9 \text{ V}$$

$$\text{Gain} = \frac{V_{oMax}}{V_{iMin}} = \frac{4.9 \text{ V}}{250 \text{ mV}} = 19.6 \frac{\text{V}}{\text{V}}$$

3. Select standard values for  $R_2$  and  $R_3$ .

From [Analog Engineer's calculator](#), use "Find Amplifier Gain" and get resistor values by inputting gain ratio of 19.6.

$$R_2 = 715 \Omega \text{ (0.1\% Standard Value)}$$

$$R_3 = 13.3 \text{ k}\Omega \text{ (0.1\% Standard Value)}$$

4. Calculate minimum input current before hitting output swing-to-rail limit.  $I_{iMin}$  represents the minimum accurately detectable input current.

$$V_{oMin} = 50 \text{ mV}; \quad R_1 = 250 \text{ m}\Omega$$

$$V_{iMin} = \frac{V_{oMin}}{\text{Gain}} = \frac{50 \text{ mV}}{19.6 \frac{\text{V}}{\text{V}}} = 2.55 \text{ mV}$$

$$I_{iMin} = \frac{V_{iMin}}{R_1} = \frac{2.55 \text{ mV}}{250 \text{ m}\Omega} = 10.2 \text{ mA}$$

5. Calculate Full scale range error and relative error.  $V_{os}$  is the typical offset voltage found in datasheet.

$$\text{FSR}_{\text{error}} = \left( \frac{V_{os}}{V_{iMax} - V_{iMin}} \right) \times 100 = \left( \frac{0.3 \text{ mV}}{247.45 \text{ mV}} \right) \times 100 = 0.121 \%$$

$$\text{Relative Error at } I_{iMax} = \left( \frac{V_{os}}{V_{iMax}} \right) \times 100 = \left( \frac{0.3 \text{ mV}}{250 \text{ mV}} \right) \times 100 = 0.12 \%$$

$$\text{Relative Error at } I_{iMin} = \left( \frac{V_{os}}{V_{iMin}} \right) \times 100 = \left( \frac{0.3 \text{ mV}}{2.5 \text{ mV}} \right) \times 100 = 12 \%$$

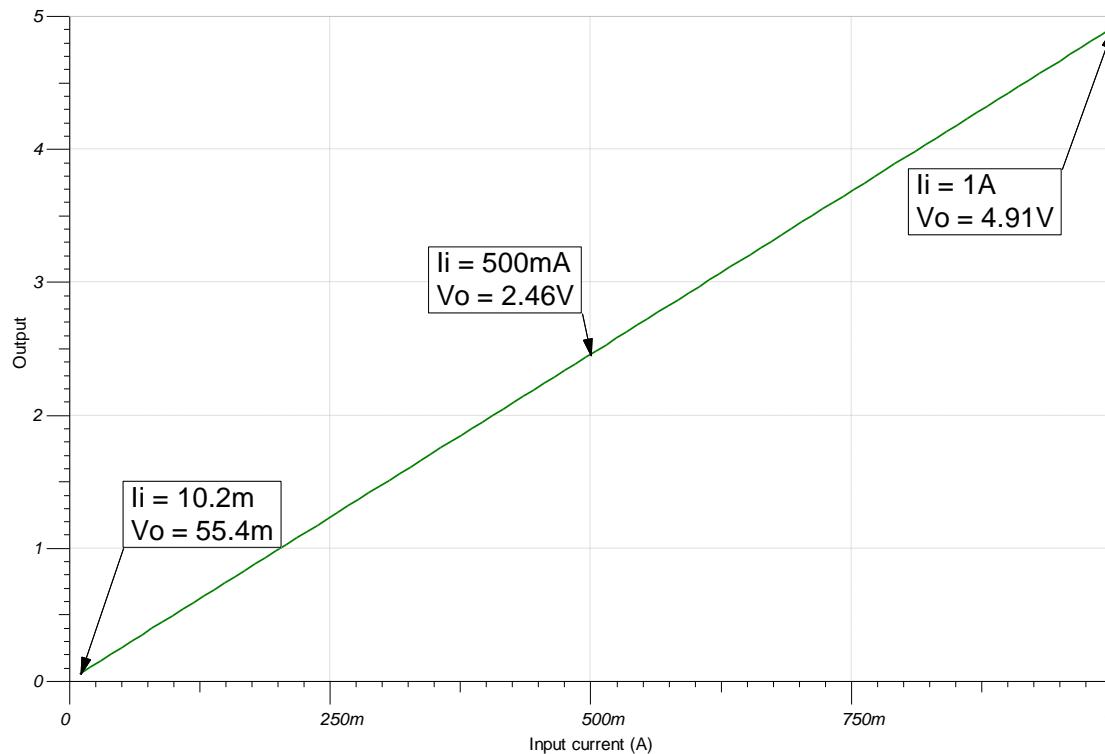
6. To maintain sufficient phase margin, ensure that the zero created by the gain setting resistors and input capacitance of the device is greater than the bandwidth of the circuit

$$\frac{1}{2\pi \times (C_{cm} + C_{diff}) \times (R_2 || R_3)} > \frac{\text{GBP}}{G}$$

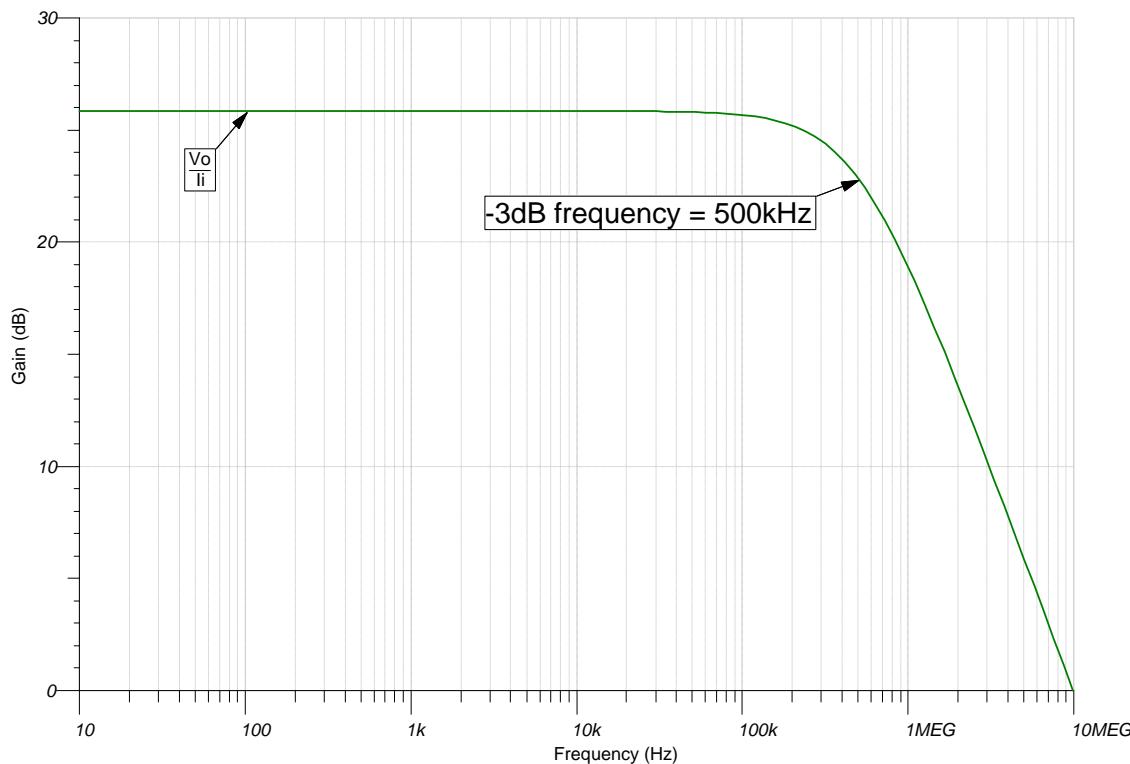
$$\frac{1}{2\pi \times (3pF + 3pF) \times \left( \frac{715 \Omega \times 13.3 \text{ k}\Omega}{715 \Omega + 13.3 \text{ k}\Omega} \right)} > \frac{10 \text{ MHz}}{19.6 \frac{\text{V}}{\text{V}}} = 39.1 \text{ MHz} > 510 \text{ kHz}$$

## Design Simulations

### DC Simulation Results



### AC Simulation Results



**References:**

1. [Analog Engineer's Circuit Cookbooks](#)
2. [SPICE Simulation File SBOC523](#)
3. [TI Precision Designs TIPD129, TIPD104](#)
4. [TI Precision Labs](#)
5. [Single-Supply, Low-Side, Unidirectional Current-Sensing Solution with Output Swing to GND Circuit](#)

**Design Featured Op Amp**

TLV9061	
$V_{ss}$	1.8V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	0.3mV
$I_q$	538 $\mu$ A
$I_b$	0.5pA
<b>UGBW</b>	10MHz
<b>SR</b>	6.5V/ $\mu$ s
<b>#Channels</b>	1,2,4
<a href="http://www.ti.com/product/tlv9061">www.ti.com/product/tlv9061</a>	

**Design Alternate Op Amp**

OPA375	
$V_{cc}$	2.25V to 5.5V
$V_{inCM}$	(V-) to ((V+)−1.2V)
$V_{out}$	Rail-to-rail
$V_{os}$	0.15mV
$I_q$	890 $\mu$ A
$I_b$	10pA
<b>UGBW</b>	10MHz
<b>SR</b>	4.75V/ $\mu$ s
<b>#Channels</b>	1
<a href="http://www.ti.com/product/OPA375">www.ti.com/product/OPA375</a>	

For battery operated or power conscious designs, outside of the original design goals described earlier, where lowering total system power is desired.

LPV821	
$V_{cc}$	1.7V to 3.6V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	1.5 $\mu$ V
$I_q$	650nA/Ch
$I_b$	7pA
<b>UGBW</b>	8kHz
<b>SR</b>	3.3V/ms
<b>#Channels</b>	1
<a href="http://www.ti.com/product/LPV821">www.ti.com/product/LPV821</a>	

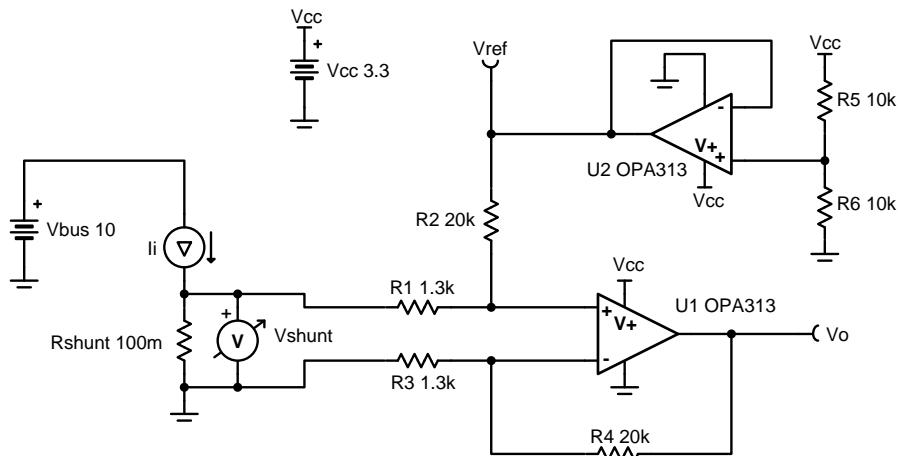
## Low-side, bidirectional current sensing circuit

### Design Goals

Input		Output		Supply		
$I_{iMin}$	$I_{iMax}$	$V_{oMin}$	$V_{oMax}$	$V_{cc}$	$V_{ee}$	$V_{ref}$
-1A	1A	110mV	3.19V	3.3V	0V	1.65V

### Design Description

This single-supply low-side, bidirectional current sensing solution can accurately detect load currents from -1A to 1A. The linear range of the output is from 110mV to 3.19V. Low-side current sensing keeps the common-mode voltage near ground, and is thus most useful in applications with large bus voltages.



### Design Notes

1. To minimize errors, set  $R_3 = R_1$  and  $R_4 = R_2$ .
2. Use precision resistors for higher accuracy.
3. Set output range based on linear output swing (see  $A_{ol}$  specification).
4. Low-side sensing should not be used in applications where the system load cannot withstand small ground disturbances or in applications that need to detect load shorts.

### Design Steps

1. Determine the transfer equation given  $R_4 = R_2$  and  $R_1 = R_3$ .

$$V_o = (I_i \times R_{\text{shunt}} \times \frac{R_4}{R_3}) + V_{\text{ref}}$$

$$V_{\text{ref}} = V_{\text{cc}} \times \left( \frac{R_6}{R_5 + R_6} \right)$$

2. Determine the maximum shunt resistance.

$$R_{\text{shunt}} = \frac{V_{\text{shunt}}}{I_{\text{imax}}} = \frac{100\text{mV}}{1 \text{ A}} = 100\text{m}\Omega$$

3. Set reference voltage.

- Since the input current range is symmetric, the reference should be set to mid supply. Therefore, make  $R_5$  and  $R_6$  equal.

$$R_5 = R_6 = 10\text{k}\Omega$$

4. Set the difference amplifier gain based on the op amp output swing. The op amp output can swing from 100mV to 3.2V, given a 3.3-V supply.

$$\text{Gain} = \frac{V_{o\text{Max}} - V_{o\text{Min}}}{R_{\text{shunt}} \times (I_{i\text{Max}} - I_{i\text{Min}})} = \frac{3.2\text{V} - 100\text{mV}}{100\text{m}\Omega \times (1 \text{ A} - (-1 \text{ A}))} = 15.5 \frac{\text{V}}{\text{V}}$$

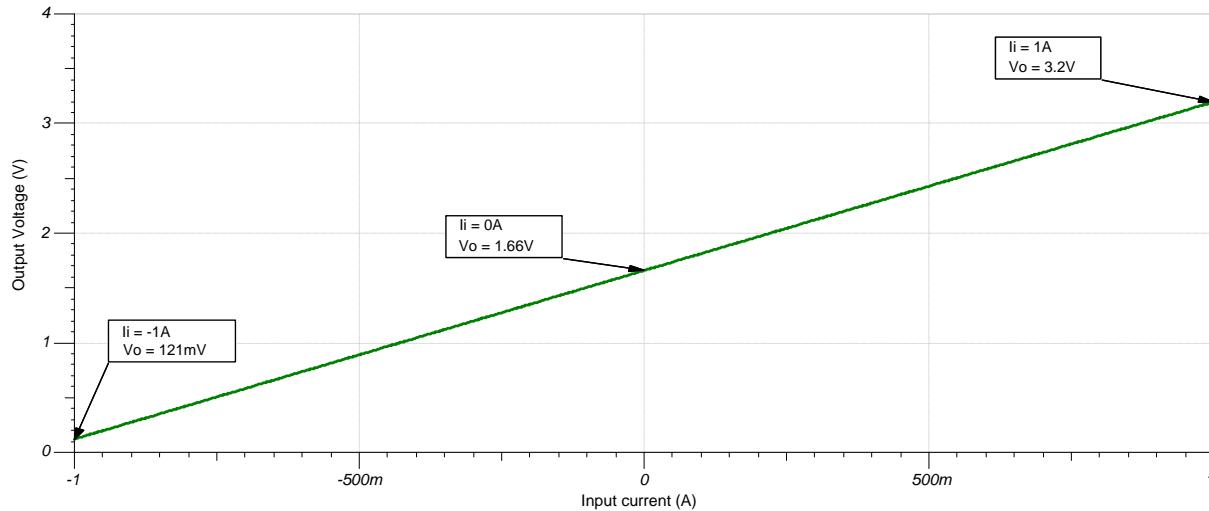
$$\text{Gain} = \frac{R_4}{R_3} = 15.5 \frac{\text{V}}{\text{V}}$$

Choose  $R_1 = R_3 = 1.3\text{k}\Omega$  (Standard Value)

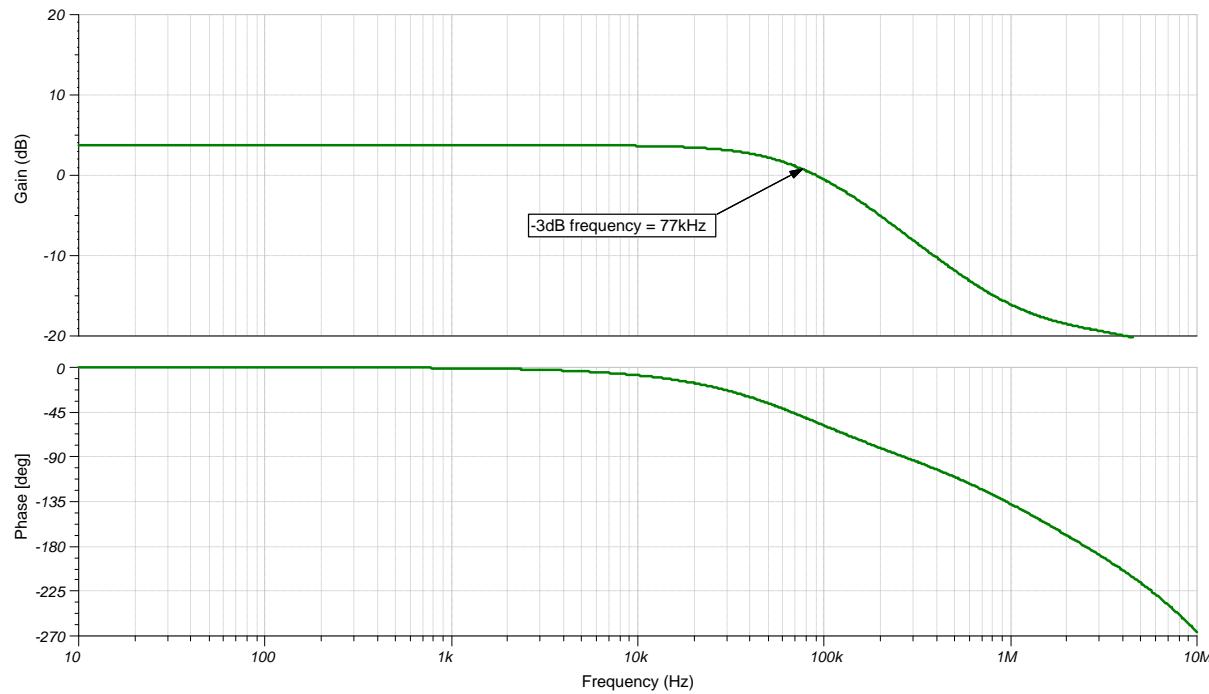
$$R_2 = R_4 = 15.5 \frac{\text{V}}{\text{V}} \times 1.3\text{k}\Omega = 20.15 \text{ k}\Omega \approx 20\text{k}\Omega \text{ (Standard Value)}$$

## Design Simulations

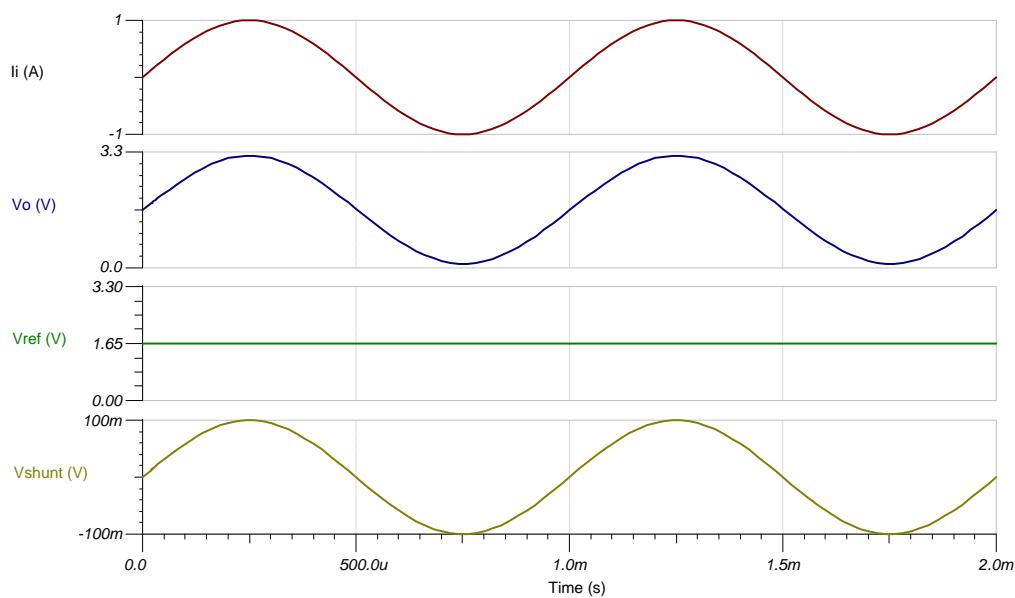
### DC Simulation Results



### Closed Loop AC Simulation Results



### Transient Simulation Results



### Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOC500](#).

See TIPD175, [www.ti.com/tipd175](http://www.ti.com/tipd175).

### Design Featured Op Amp

OPA313	
$V_{cc}$	1.8V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	500 $\mu$ V
$I_q$	50 $\mu$ A/Ch
$I_b$	0.2pA
<b>UGBW</b>	1MHz
<b>SR</b>	0.5V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/opa313">www.ti.com/product/opa313</a>	

### Design Alternate Op Amp

	TLV9062	OPA376
$V_{cc}$	1.8V to 5.5V	2.2V to 5.5V
$V_{inCM}$	Rail-to-rail	Rail-to-rail
$V_{out}$	Rail-to-rail	Rail-to-rail
$V_{os}$	300 $\mu$ V	5 $\mu$ V
$I_q$	538 $\mu$ A/Ch	760 $\mu$ A/Ch
$I_b$	0.5pA	0.2pA
<b>UGBW</b>	10MHz	5.5MHz
<b>SR</b>	6.5V/ $\mu$ s	2V/ $\mu$ s
<b>#Channels</b>	1, 2, 4	1, 2, 4
	<a href="http://www.ti.com/product/tlv9062">www.ti.com/product/tlv9062</a>	<a href="http://www.ti.com/product/opa376">www.ti.com/product/opa376</a>

For battery-operated or power-conscious designs, outside of the original design goals described earlier, where lowering total system power is desired.

LPV821	
$V_{cc}$	1.7V to 3.6V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	1.5 $\mu$ V
$I_q$	650nA/Ch
$I_b$	7pA
<b>UGBW</b>	8KHz
<b>SR</b>	3.3V/ms
<b>#Channels</b>	1
<a href="http://www.ti.com/product/lpv821">www.ti.com/product/lpv821</a>	

**Revision History**

Revision	Date	Change
B	January 2019	Downscale the title. Added link to circuit cookbook landing page.
A	May 2018	Changed title role to 'Amplifiers'. Added SPICE simulation file link. Added LPV821 as a Design Alternate Op Amp for battery-operated or power-conscious designs.

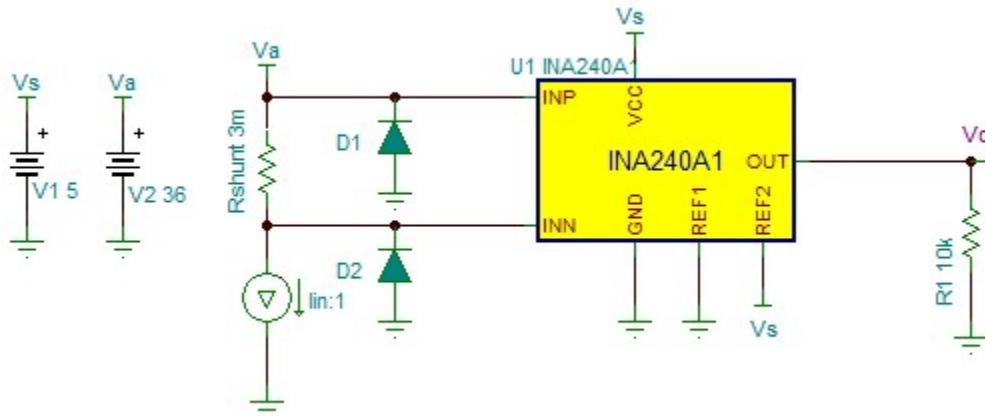
## **High-side, bidirectional current-sensing circuit with transient protection**

### **Design Goals**

Input		Output		Supply			Standoff and Clamp Voltages		EFT Level
$I_{inMin}$	$I_{inMax}$	$V_{oMin}$	$V_{oMax}$	$V_s$	GND	$V_{ref}$	$V_{wm}$	$V_c$	$V_{pp}$
-40A	40A	100mV	4.9V	5V	0V	2.5V	36V	80V	2kV 8/20 $\mu$ s

### **Design Description**

This high-side, bidirectional current sensing solution can accurately measure current in the range of -40A to 40A for a 36-V voltage bus. The linear voltage output is 100mV to 4.90V. This solution is also designed to survive IEC61000-4-4 level 4 EFT stress ( $V_{oc} = 2kV$ ;  $I_{sc} = 40A$ ; 8/20 $\mu$ s).



### **Design Notes**

1. This solution is targeted toward high-side current sensing.
2. The sense resistor value is determined by minimum and maximum load currents, power dissipation and Current Shunt Amplifier (CSA) gain.
3. Bidirectional current sensing requires an output reference voltage ( $V_{ref}$ ). Device gain is achieved through internal precision matched resistor network.
4. The expected maximum and minimum output voltage must be within the device linear range.
5. The TVS diode must be selected based on bus voltage, the CSA common-mode voltage specification, and EFT pulse characteristics.

## Design Steps

1. Determine the maximum output swing:

$$V_{swN} = V_{ref} - V_{oMin} = 2.5V - 0.1V = 2.4V$$

$$V_{swP} = V_{oMax} - V_{ref} = 4.9V - 2.5V = 2.4V$$

2. Determine the maximum value of the sense resistor based on maximum load current, swing and device gain. In this example, a gain of 20 was chosen to illustrate the calculation, alternative gain versions may be selected as well:

$$R_{shunt} \leq \frac{V_{swP}}{I_{in\_max} \times \text{Gain}} = \frac{2.4V}{40A \times 20} = 3m\Omega$$

3. Calculate the peak power rating of the sense resistor:

$$P_{shunt} = I_{in\_max}^2 \times R_{shunt} = 40A^2 \times 3m\Omega = 5W$$

4. Determine TVS standoff voltage and clamp voltage:

$$V_{wm} = 36V \text{ and } V_c \leq 80V$$

5. Select a TVS diode.

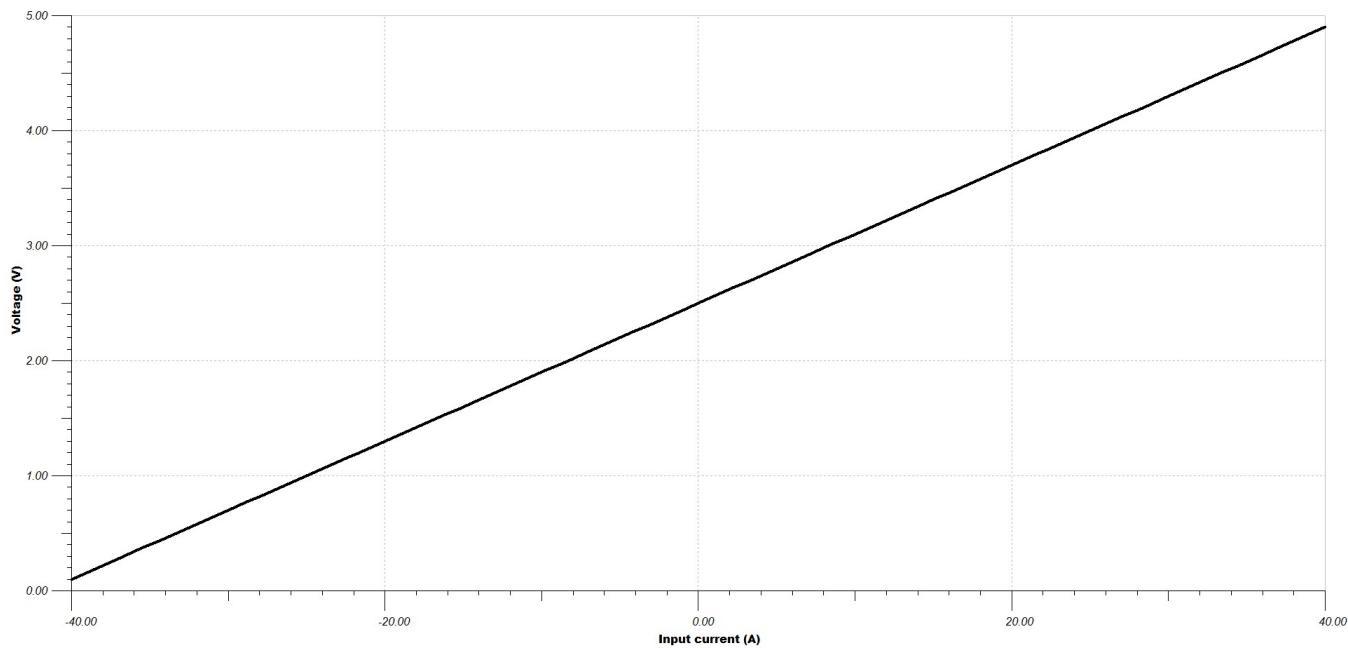
For example, SMBJ36A from Littelfuse™ satisfies the previous requirement, with peak pulse power of 600W (10/1000μs) and current of 10.4A.

6. Make sure the TVS diode satisfies the design requirement based on the TVS operating curve.

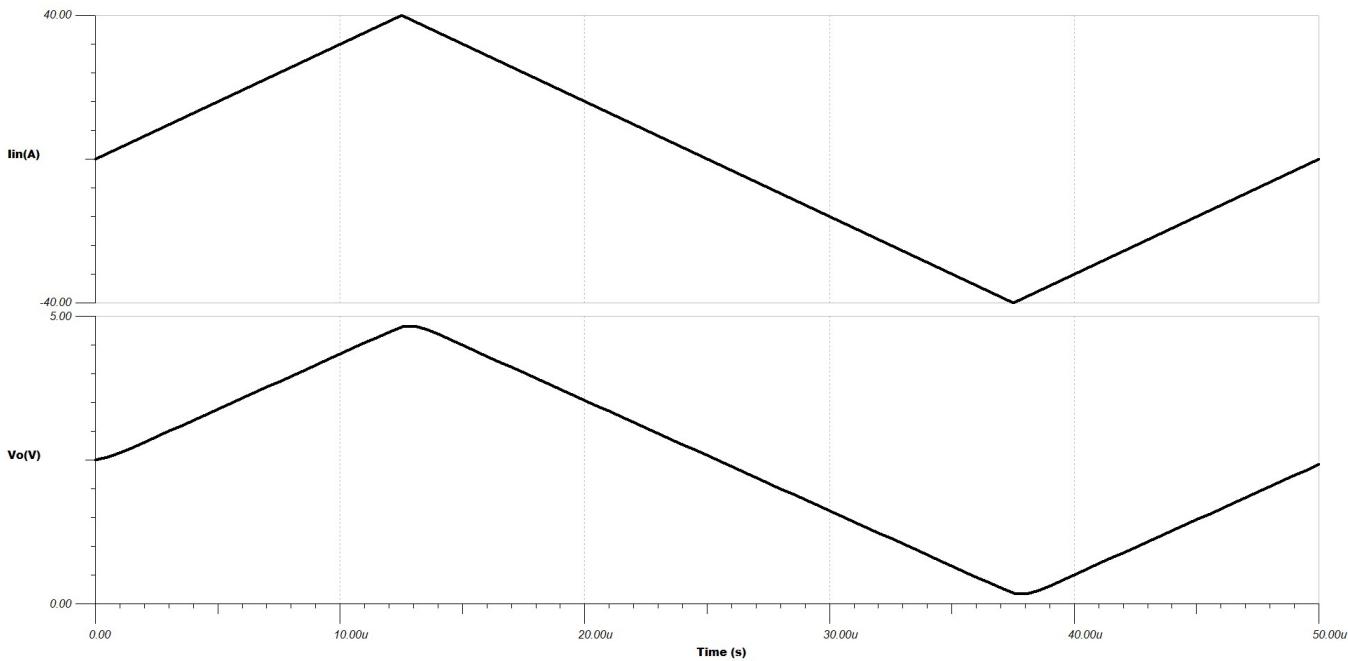
Peak pulse power at given excitation (8/20μs) is estimated to be around 3.5kW, which translates to peak pulse current:

$$I_{pp} = \frac{3.5kW}{600W} \times 10.4A = 60A$$

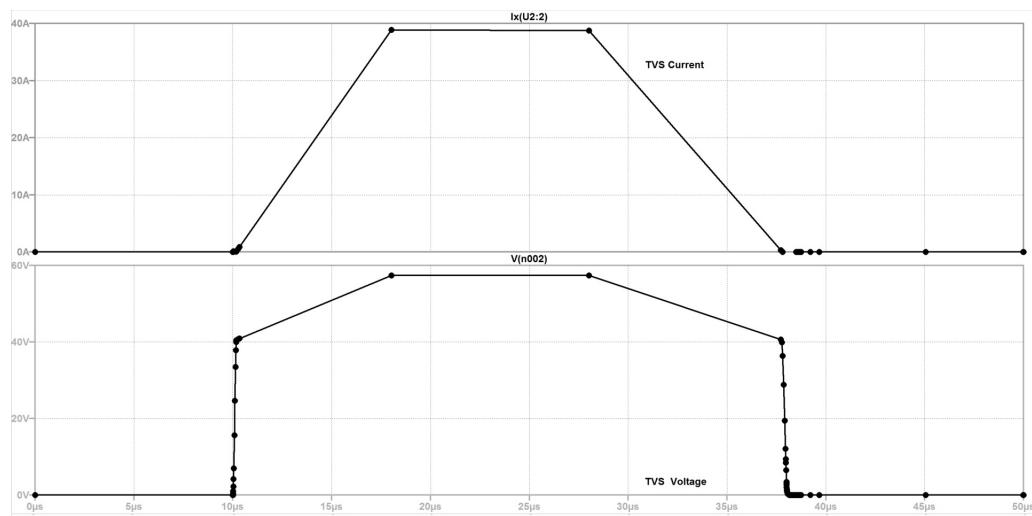
This is above the maximum excitation (short circuit) current of 40A. The select TVS effectively protects the circuit against the specified EFT strike.

**Design Simulations****DC Transfer Characteristics****Transient Simulation Results**

The output is a scaled version of the input.



### TVS Diode Transient Response Under EFT Excitation



## Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

For more information on transient protection of the current sense amplifiers, see [TIDA-00302](#) and the [Current Sense Amplifier Training Videos](#).

## Design Featured Current Sense Amplifier

INA240A1	
$V_s$	2.7V to 5.5V
$V_{CM}$	-4V to 80V
$V_{os}$	Rail-to-rail
$V_{os}$	5 $\mu$ V
$I_B$	80 $\mu$ A
<b>BW</b>	400kHz
<b>Vos Drift</b>	50nV/ $^{\circ}$ C
<a href="http://www.ti.com/product/INA240">http://www.ti.com/product/INA240</a>	

## Design Alternate

INA282	
$V_s$	2.7V to 18V
$V_{CM}$	-14V to 80V
$V_{os}$	20 $\mu$ V
$I_B$	25 $\mu$ A
<b>BW</b>	10kHz
<b>Vos Drift</b>	0.3 $\mu$ V/ $^{\circ}$ C
<a href="http://www.ti.com/product/INA193">http://www.ti.com/product/INA193</a>	

## Revision History

Revision	Date	Change
A	February 2019	Changed VinMin and VinMax in the Design Goals table to linMin and linMax, respectively.

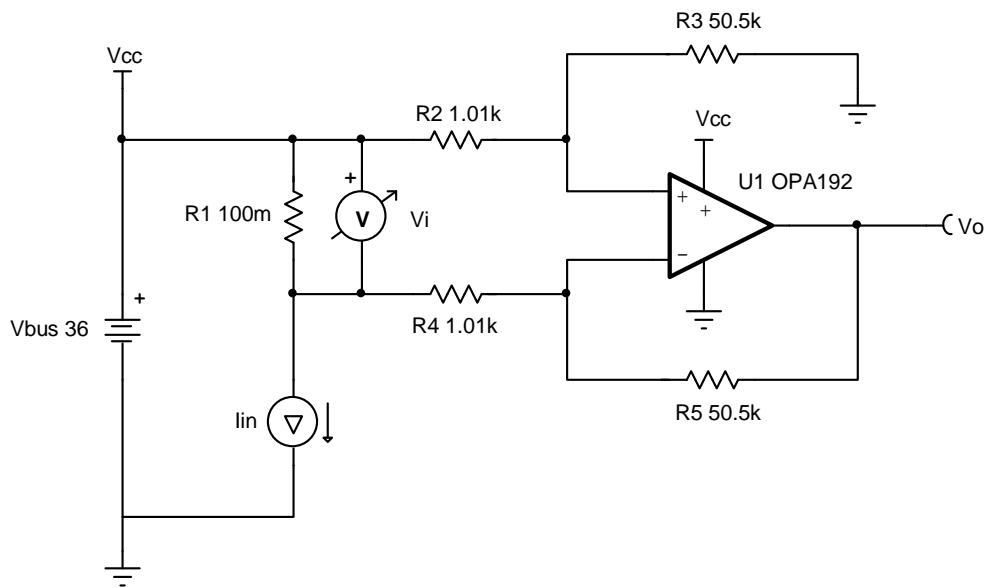
## High-side current-sensing circuit design

### Design Goals

Input		Output		Supply	
$I_{i\text{Min}}$	$I_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	$V_{cc}$	$V_{ee}$
50mA	1A	0.25V	5V	36V	0V

### Design Description

This single-supply, high-side, low-cost current sensing solution detects load current between 50mA and 1A and converts it to an output voltage from 0.25V to 5V. High-side sensing allows for the system to identify ground shorts and does not create a ground disturbance on the load.



### Design Notes

1. DC common mode rejection ratio (CMRR) performance is dependent on the matching of the gain setting resistors,  $R_2$ - $R_5$ .
2. Increasing the shunt resistor increases power dissipation.
3. Ensure that the common-mode voltage is within the linear input operating region of the amplifier. The common mode voltage is set by the resistor divider formed by  $R_2$ ,  $R_3$ , and the bus voltage. Depending on the common-mode voltage determined by the resistor divider a rail-to-rail input (RRI) amplifier may not be required for this application.
4. An op amp that does not have a common-mode voltage range that extends to  $V_{cc}$  may be used in low-gain or an attenuating configuration.
5. A capacitor placed in parallel with the feedback resistor will limit bandwidth, improve stability, and help reduce noise.
6. Use the op amp in a linear output operating region. Linear output swing is usually specified under the  $A_{OL}$  test conditions.

### Design Steps

1. The full transfer function of the circuit is provided below.

$$V_o = I_{in} \times R_1 \times \frac{R_5}{R_4}$$

Given  $R_2 = R_4$  and  $R_3 = R_5$

2. Calculate the maximum shunt resistance. Set the maximum voltage across the shunt to 100mV.

$$R_1 = \frac{V_{oMax}}{I_{iMax}} = \frac{100mV}{1A} = 100m\Omega$$

3. Calculate the gain to set the maximum output swing range.

$$\text{Gain} = \frac{V_{oMax} - V_{oMin}}{(I_{iMax} - I_{iMin}) \times R_1} = \frac{5V - 0.25V}{(1A - 0.05A) \times 100m\Omega} = 50 \frac{V}{V}$$

4. Calculate the gain setting resistors to set the gain calculated in step 3.

Choose  $R_2 = R_4 = 1.01k\Omega$  (Standard value)

$$R_3 = R_5 = R_2 \times \text{Gain} = 1.01k\Omega \times 50 \frac{V}{V} = 50.5k\Omega \text{ (Standard value)}$$

5. Calculate the common-mode voltage of the amplifier to ensure linear operation.

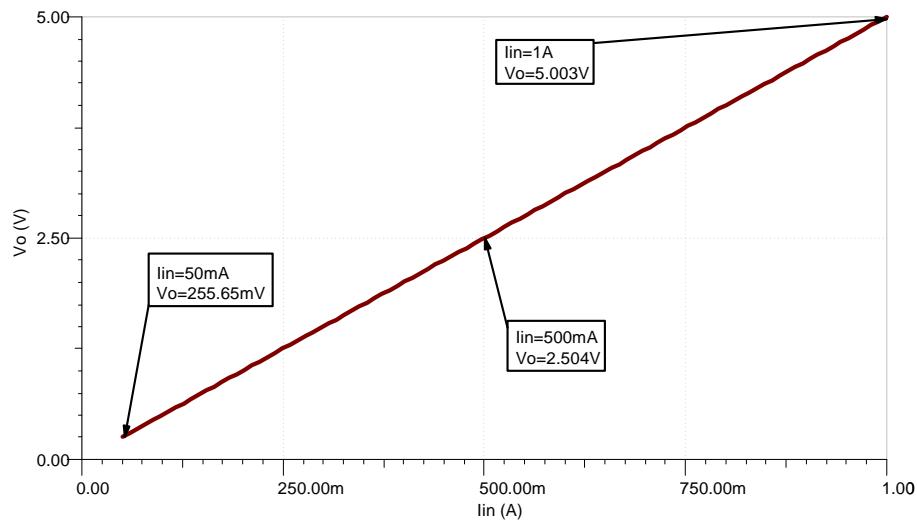
$$V_{cm} = V_{CC} \times \frac{R_3}{R_2 + R_3} = 36V \times \frac{50.5k}{1.01k + 50.5k} = 35.294V$$

6. The upper cutoff frequency ( $f_H$ ) is set by the non-inverting gain (noise gain) of the circuit and the gain bandwidth (GBW) of the op amp.

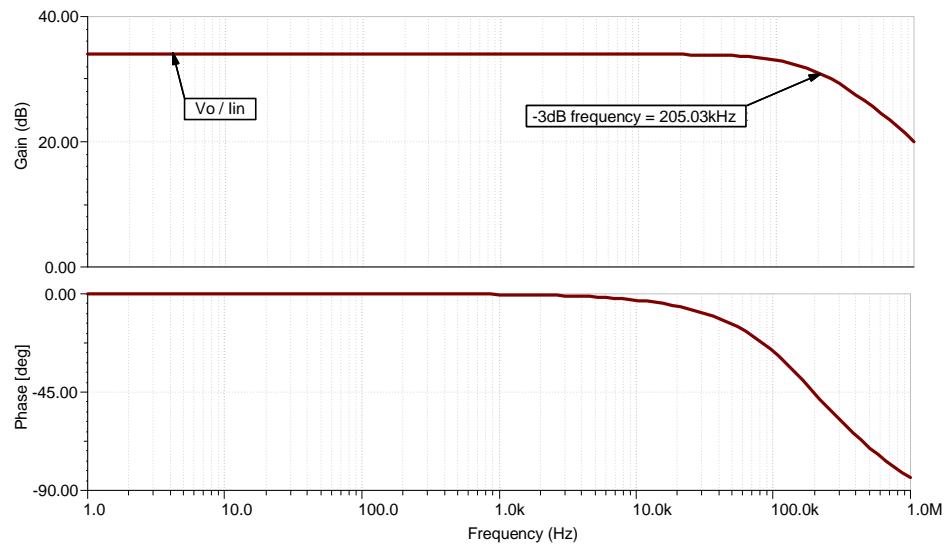
$$f_H = \frac{\text{GBW}}{\text{Noise Gain}} = \frac{10\text{MHz}}{51 \frac{V}{V}} = 196.1 \text{ kHz}$$

## Design Simulations

### DC Simulation Results



### AC Simulation Results



**References:**

1. [Analog Engineer's Circuit Cookbooks](#)
2. [SPICE Simulation File SBOMAV4](#)
3. [TI Precision Labs](#)

**Design Featured Op Amp**

OPA192	
$V_{cc}$	4.5V to 36V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	5 $\mu$ V
$I_q$	1mA
$I_b$	5pA
<b>UGBW</b>	10MHz
<b>SR</b>	20V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/OPA192">www.ti.com/product/OPA192</a>	

**Design Alternate Op Amp**

OPA2990	
$V_{cc}$	2.7V to 40V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	250 $\mu$ V
$I_q$	120 $\mu$ A
$I_b$	10pA
<b>UGBW</b>	1.25MHz
<b>SR</b>	5V/ $\mu$ s
<b>#Channels</b>	2
<a href="http://www.ti.com/product/OPA2990">www.ti.com/product/OPA2990</a>	

**Revision History**

Revision	Date	Change
A	February 2019	Downstyle title. Added Design Alternate Op Amp table.

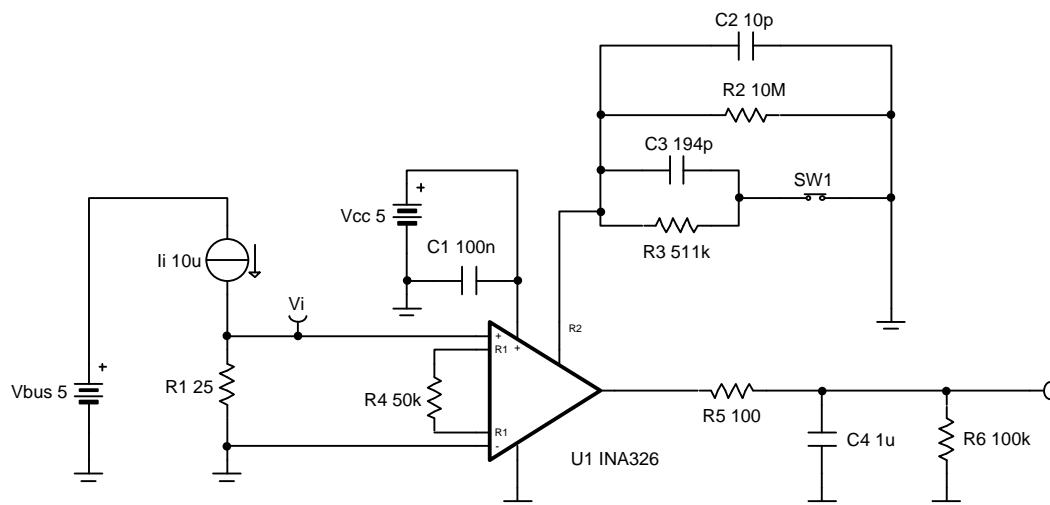
### **3-decade, load-current sensing circuit**

## Design Goals

Input		Output		Supply		
$I_{iMin}$	$I_{iMax}$	$V_{oMin}$	$V_{oMax}$	$V_{cc}$	$V_{ee}$	$V_{ref}$
10 $\mu$ A	10mA	100mV	4.9V	5.0V	0V	0V

## Design Description

This single-supply, low-side, current-sensing solution accurately detects load current between 10 $\mu$ A and 10mA. A unique yet simple gain switching network was implemented to accurately measure the three-decade load current range.



## Design Notes

1. Use a maximum shunt resistance to minimize relative error at minimum load current.
  2. Select 0.1% tolerance resistors for  $R_1$ ,  $R_2$ ,  $R_3$ , and  $R_4$  in order to achieve approximately 0.1% FSR gain error.
  3. Use a switch with low on-resistance ( $R_{on}$ ) to minimize interaction with feedback resistances, preserving gain accuracy.
  4. Minimize capacitance on INA326 gain setting pins.
  5. Scale the linear output swing based on the gain error specification.

## Design Steps

1. Define full-scale shunt resistance.

$$R_1 = \frac{V_{iMax}}{I_{iMax}} = \frac{250mV}{10mA} = 25\Omega$$

2. Select gain resistors to set output range.

$$G_{iMax} = \frac{V_{oMax}}{V_{iMax}} = \frac{V_{oMax}}{R_1 \times I_{iMax}} = \frac{4.9V}{25\Omega \times 10mA} = 19.6V$$

$$G_{iMin} = \frac{V_{oMin}}{V_{iMin}} = \frac{V_{oMin}}{R_1 \times I_{iMin}} = \frac{100mV}{25\Omega \times 10\mu A} = 400V$$

$$R_2 = \frac{R_4 \times G_{iMin}}{2} = \frac{50k\Omega \times 400V}{2} = 10M\Omega$$

$$R_2 \parallel R_3 = \frac{R_4 \times G_{iMax}}{2} = \frac{50k\Omega \times 19.6V}{2} = 490k\Omega$$

$$R_3 = \frac{490k\Omega \times R_2}{R_2 - 490k\Omega} = 515.25k\Omega \approx 511k\Omega \text{ (Standard Value)}$$

3. Select a capacitor for the output filter.

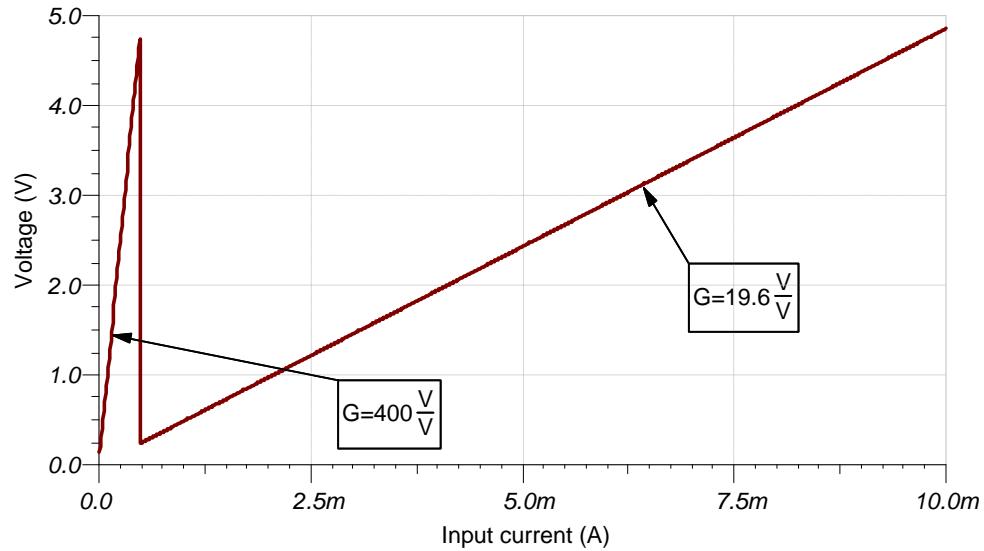
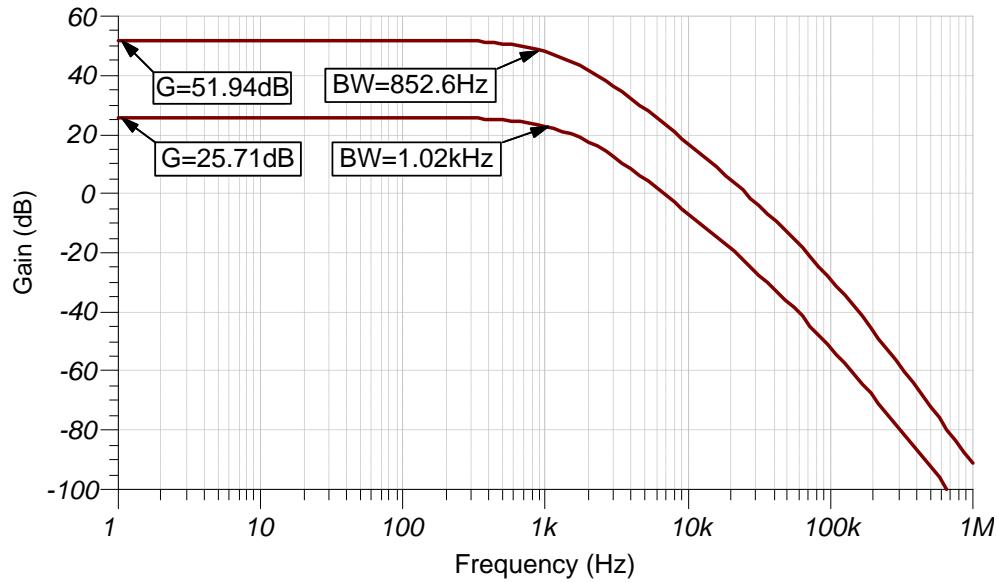
$$f_p = \frac{1}{2\pi R_5 C_4} = \frac{1}{2\pi \times 100\Omega \times 1\mu F} = 1.59kHz$$

4. Select a capacitor for gain and filtering network.

$$C_2 = \frac{1}{2\pi R_2 f_p} = \frac{1}{2\pi \times 10M\Omega \times 1.59kHz} = 10pF$$

$$C_3 = \frac{1}{2\pi (R_2 \parallel R_3) f_p} - C_2 = \frac{1}{2\pi \times (10M\Omega \parallel 511k\Omega) \times 1.59kHz} - 10pF$$

$$C_3 = 196pF \approx 194pF \text{ (Standard Value)}$$

**Design Simulations**
**DC Simulation Results**

**AC Simulation Results**


## Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOC498](#).

See TIPD104, [www.ti.com/tool/tipd104](http://www.ti.com/tool/tipd104).

## Design Featured Op Amp

INA326	
$V_{ss}$	1.8V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	0.1mV
$I_q$	3.4mA
$I_b$	2nA
<b>UGBW</b>	1kHz
<b>SR</b>	Filter limited
<b>#Channels</b>	1
<a href="http://www.ti.com/product/ina326">www.ti.com/product/ina326</a>	

## Revision History

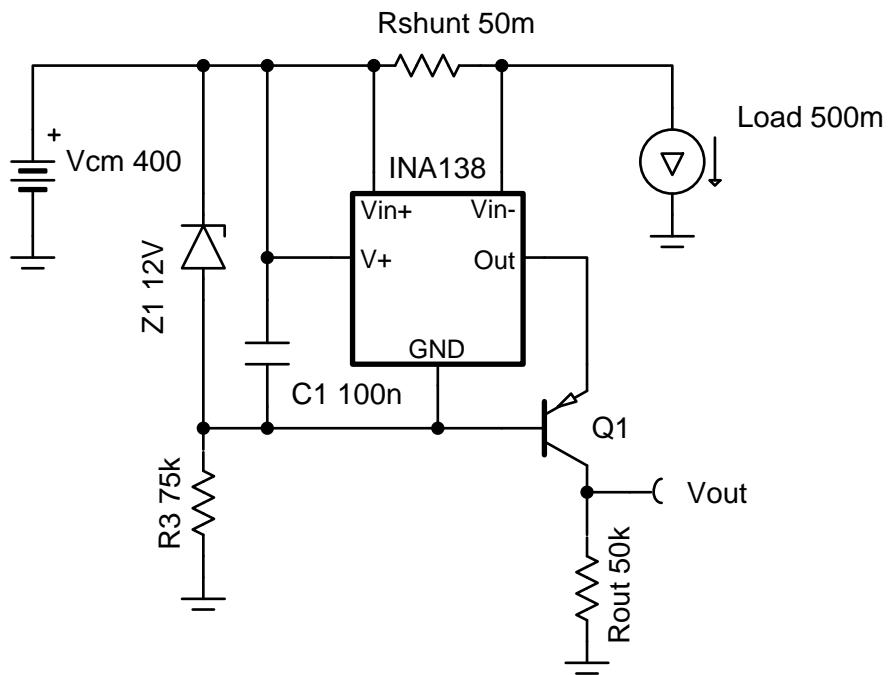
Revision	Date	Change
A	January 2019	Downscale the title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page.

## High-voltage, high-side floating current sensing circuit using current output, current sense amplifier

Input		Output		Supply		
I <sub>load</sub> Min	I <sub>load</sub> Max	V <sub>out</sub> Min	V <sub>out</sub> Max	V <sub>cm</sub> Min	V <sub>cm</sub> Max	V <sub>ee</sub>
0.5A	9.9A	250mV	4.95V	12V	400V	GND (0V)

### Design Description

This cookbook is intended to demonstrate a method of designing an accurate current sensing solution for systems with high common mode voltages. The principle aspect of this design uses a unidirectional circuit to monitor a system with  $V_{cm} = 400V$  by floating the supplies of the device across a Zener diode from the supply bus ( $V_{cm}$ ). This cookbook is based on the [High Voltage 12 V – 400 V DC Current Sense Reference Design](#).



## Design Notes

1. The [Getting Started with Current Sense Amplifiers](#) video series introduces implementation, error sources, and advanced topics for using current sense amplifiers.
2. This example is for high  $V_{CM}$ , high-side, unidirectional, DC sensing.
3. To minimize error, make the shunt voltage as large as the design will allow. For the INA138 device, keep  $V_{sense} \gg 15mV$ .
4. The relative error due to input offset increases as shunt voltage decreases, so use a current sense amplifier with low offset voltage. A precision resistor for  $R_{shunt}$  is necessary because  $R_{shunt}$  is a major source of error.
5. The INA138 is a current-output device, so voltages referenced to ground are achieved with a high voltage bipolar junction transistor (BJT).
  - Ensure the transistor chosen for Q1 can withstand the maximum voltage across the collector and emitter (for example, need 400V, but select > 450V for margin).
  - Multiple BJTs can be stacked and biased in series to achieve higher voltages
  - High beta of this transistor reduces gain error from current that leaks out of the base

## Design Steps

1. Determine the operating load current and calculate  $R_{shunt}$ :
  - Recommended  $V_{sense}$  is 100mV and maximum recommended is 500mV, so the following equation can be used to calculate  $R_{shunt}$  where  $V_{sense} \leq 500mV$ :
 
$$R_{shunt} = \frac{V_{sense\ max}}{I_{load\ max}} \rightarrow \frac{0.5V}{10A} = 50m\Omega$$
  - For more accurate and precise measurements over the operating temperature range, a current monitor with integrated shunt resistor can be used in some systems. The benefits of using these devices are explained in [Getting Started with Current Sense Amplifiers, Session 16: Benefits of Integrated Precision Shunt Resistor](#).
2. Choose a Zener diode to create an appropriate voltage drop for the INA138 supply:
  - The Zener voltage of the diode should fall in the INA138 supply voltage range of 2.7V to 36V and needs to be larger than the maximum output voltage required.
  - The Zener diode voltage regulates the INA138 supply and protects from transients.
  - Data sheet parameters are defined for 12-V  $V_{int}$  to the GND pin so a 12-V Zener is chosen.
3. Determine the series resistance with the Zener diode:
  - This resistor (R3) is the main power consumer due to its voltage drop (up to 388V in this case). If R3 is too low, it will dissipate more power, but if it is too high R3 will not allow the Zener diode to avalanche properly. Since the data sheet specifies  $I_Q$  for  $V_S = 5V$ , estimate the max quiescent current of the INA138 device at  $V_S = 12V$  to be  $108\mu A$  and calculate R3 using the bias current of the Zener diode, 5mA, as shown:

$$R_3 = \frac{V_{CM} - V_{zener}}{I_{zener} + I_{INA138}} = \frac{400V - 12V}{5mA + 108\mu A} \approx 75.96k\Omega$$

standard value  $\rightarrow 75k\Omega$

- The power consumption of this resistor is calculated using the following equation:

$$\text{Power}_{R3} = \frac{(V_{cm} - V_{Zener})^2}{R3} \rightarrow \frac{(400V - 12V)^2}{75k\Omega} \approx 2.007W$$

4. Calculate  $R_{out}$  using the equation for output current in the INA138 data sheet.

- This system is designed for 10V/V gain where  $V_{out} = 1V$  if  $V_{sense} = 100mV$ :

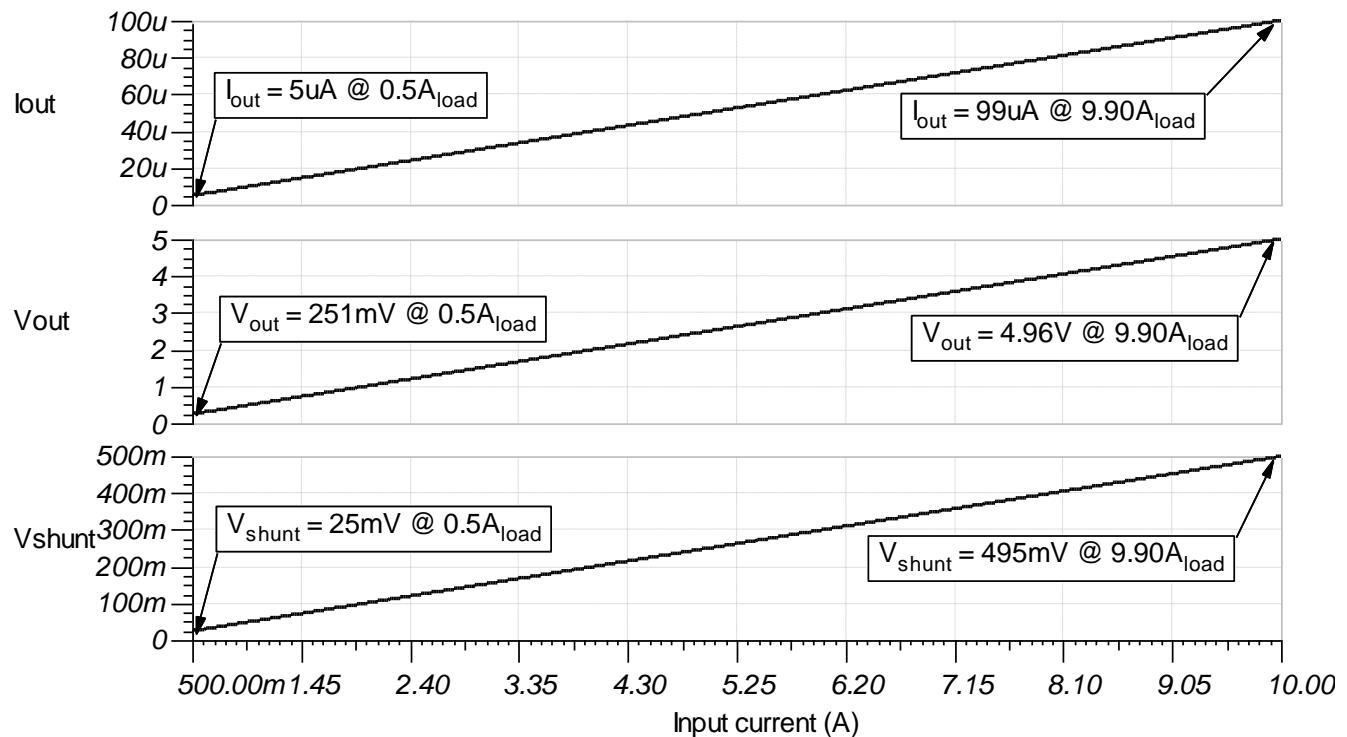
$$I_{out \text{ INA138}} = 200 \frac{\mu A}{V} \times (V_{sense \text{ max}}) \rightarrow 200 \frac{\mu A}{V} \times (0.5V) = 100\mu A$$

$$R_{out} = \frac{V_{out \text{ max}}}{I_{out \text{ INA138}}} \rightarrow \frac{5V}{100\mu A} = 50k\Omega$$

## Design Simulations

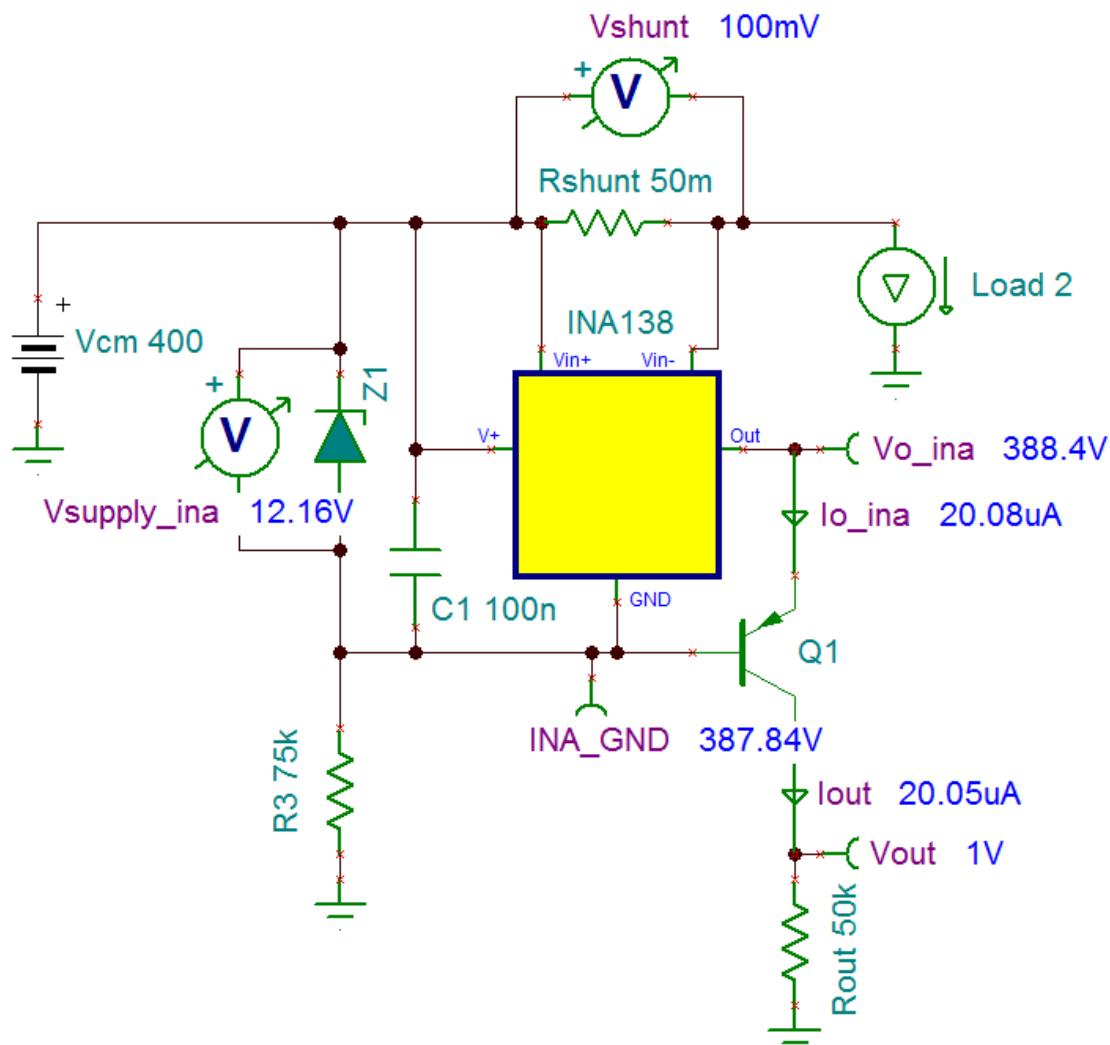
### DC Simulation Results

The following graph shows a linear output response for load currents from 0.5A to 10A and  $12V \leq V_{cm} \leq 400V$ .  $I_{out}$  and  $V_{out}$  remain constant over a varying  $V_{cm}$  once the Zener diode is reverse biased.



### Steady State Simulation Results

The following image shows this system in DC steady state with a 2-A load current. The output voltage is 10x greater than the measured voltage across  $R_{\text{shunt}}$ .



### Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SGLC001](#).

**Getting Started with Current Sense Amplifiers video series:**

<https://training.ti.com/getting-started-current-sense-amplifiers>

**Abstract on Extending Voltage Range of Current Shunt Monitor:**

<http://www.ti.com/lit/an/slla190/slla190.pdf>

**High Voltage 12V – 400V DC Current Sense Reference Design:**

<http://www.ti.com/tool/TIDA-00332>

**Cookbook Design Files:**

<http://proddms.itg.ti.com/stage/lit/sw/sglc001a/sglc001a.zip>

**Current Sense Amplifiers on TI.com:**

<http://www.ti.com/amplifier-circuit/current-sense/products.html>

**For direct support from TI Engineers use the E2E community:**

<http://e2e.ti.com>

### Design Featured Current Shunt Monitor

INA138	
$V_{ss}$	2.7V to 36V
$V_{in\ cm}$	2.7V to 36V
$V_{out}$	Up to (V+) - 0.8V
$V_{os}$	$\pm 0.2\text{mV}$ to $\pm 1\text{mV}$
$I_q$	25 $\mu\text{A}$ to 45 $\mu\text{A}$
$I_b$	2 $\mu\text{A}$
UGBW	800kHz
# of Channels	1
<a href="http://www.ti.com/product/ina138">http://www.ti.com/product/ina138</a>	

### Design Alternate Current Shunt Monitor

INA168	
$V_{ss}$	2.7V to 60V
$V_{in\ cm}$	2.7V to 60V
$V_{out}$	Up to (V+) - 0.8V
$V_{os}$	$\pm 0.2\text{mV}$ to $\pm 1\text{mV}$
$I_q$	25 $\mu\text{A}$ to 45 $\mu\text{A}$
$I_b$	2 $\mu\text{A}$
UGBW	800kHz
# of Channels	1
<a href="http://www.ti.com/product/ina168">http://www.ti.com/product/ina168</a>	

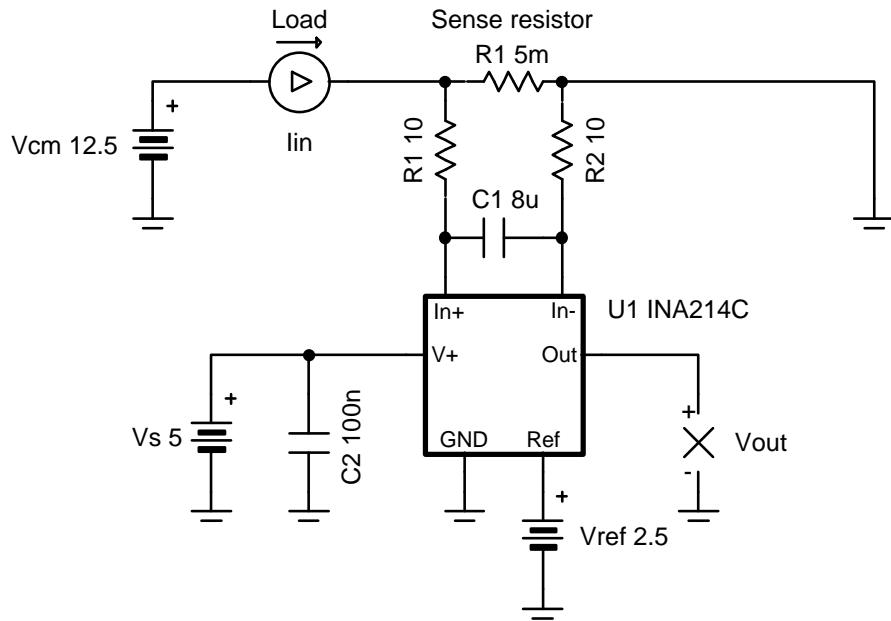
## Low-drift, low-side, bidirectional current sensing circuit with integrated precision gain resistors

### Design Goals

Input			Output		Supply	
$I_{inMin}$	$I_{inMax}$	$V_{cm}$	$V_{outMin}$	$V_{outMax}$	$V_s$	$V_{ref}$
-4A	4A	12.5V	0.5V	4.5V	5V	2.5V

### Design Description

The low-side bidirectional current-shunt monitor solution illustrated in the following image can accurately measure currents from -4A to 4A, and the design parameters can easily be changed for different current measurement ranges. Current-shunt monitors from the INA21x family have integrated precision gain resistors and a zero-drift architecture that enables current sensing with maximum drops across the shunt as low as 10mV full-scale.



### Design Notes

- To avoid additional error, use  $R_1 = R_2$  and keep the resistance as small as possible (no more than 10Ω, as stated in [INA21x Voltage Output, Low- or High-Side Measurement, Bidirectional, Zero-Drift Series, Current-Shunt Monitors](#)).
- Low-side sensing should not be used in applications where the system load cannot withstand small ground disturbances or in applications that need to detect load shorts.
- The [Getting Started with Current Sense Amplifiers](#) video series introduces implementation, error sources, and advanced topics that are good to know when using current sense amplifiers.

## Design Steps

1. Determine  $V_{ref}$  based on the desired current range:

With a current range of -4A to 4A, then half of the range is below 0V, so set:

$$V_{ref} = \frac{1}{2}V_s = \frac{5}{2} = 2.5V$$

2. Determine the desired shunt resistance based on the maximum current and maximum output voltage:

To not exceed the swing-to-rail and to allow for some margin, use  $V_{outMax} = 4.5V$ . This, combined with maximum current of 4A and the  $V_{ref}$  calculated in step 1, can be used to determine the shunt resistance using the equation:

$$R_1 = \frac{V_{outMax} - V_{ref}}{\text{Gain} \times I_{loadMax}} = \frac{4.5 - 2.5}{100 \times 4} = 5m\Omega$$

3. Confirm  $V_{out}$  will be within the desired range:

At the maximum current of 4A, with Gain = 100V/V,  $R_1 = 5m\Omega$ , and  $V_{ref} = 2.5V$ :

$$V_{out} = I_{load} \times \text{Gain} \times R_1 + V_{ref} = 4 \times 100 \times 0.005 + 2.5 = 4.5V$$

At the minimum current of 4A, with Gain = 100V/V,  $R_1 = 5m\Omega$ , and  $V_{ref} = 2.5V$ :

$$V_{out} = I_{load} \times \text{Gain} \times R_1 + V_{ref} = -4 \times 100 \times 0.005 + 2.5 = 0.5V$$

4. Filter cap selection:

To filter the input signal at 1kHz, using  $R_1 = R_2 = 10\Omega$ :

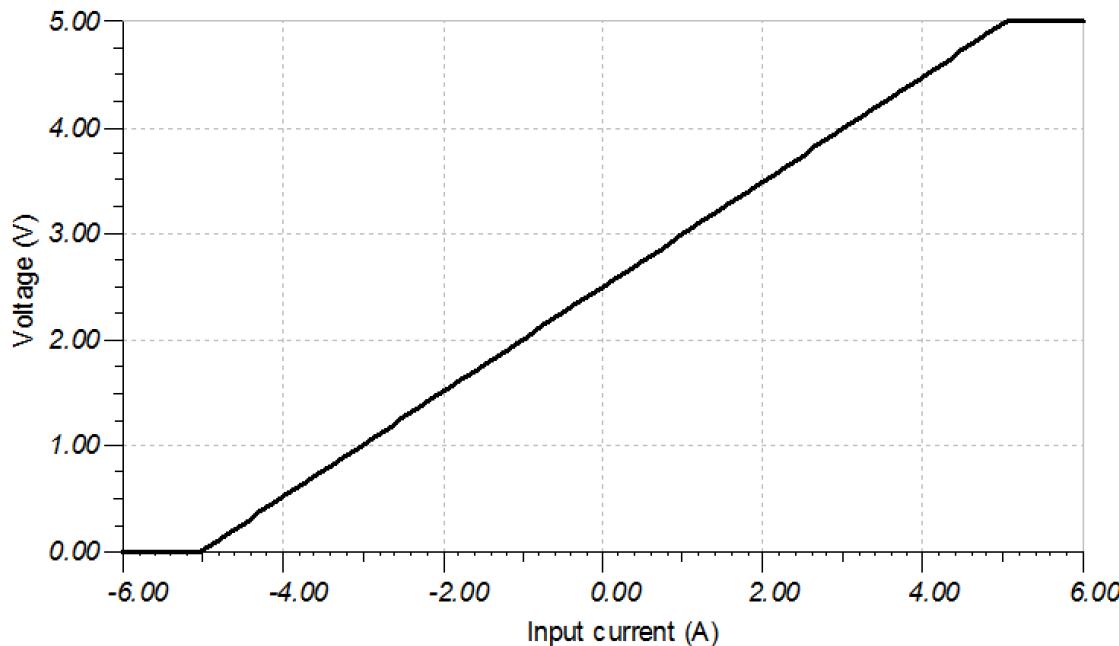
$$C_1 = \frac{1}{2\pi(R_1 + R_2)F_{-3dB}} = \frac{1}{2\pi(10 + 10)1000} = 7.958 \times 10^{-6} \approx 8\mu\text{F}$$

For more information on signal filtering and the associated gain error, see [INA21x Voltage Output, Low- or High-Side Measurement, Bidirectional, Zero-Drift Series, Current-Shunt Monitors](#).

## Design Simulations

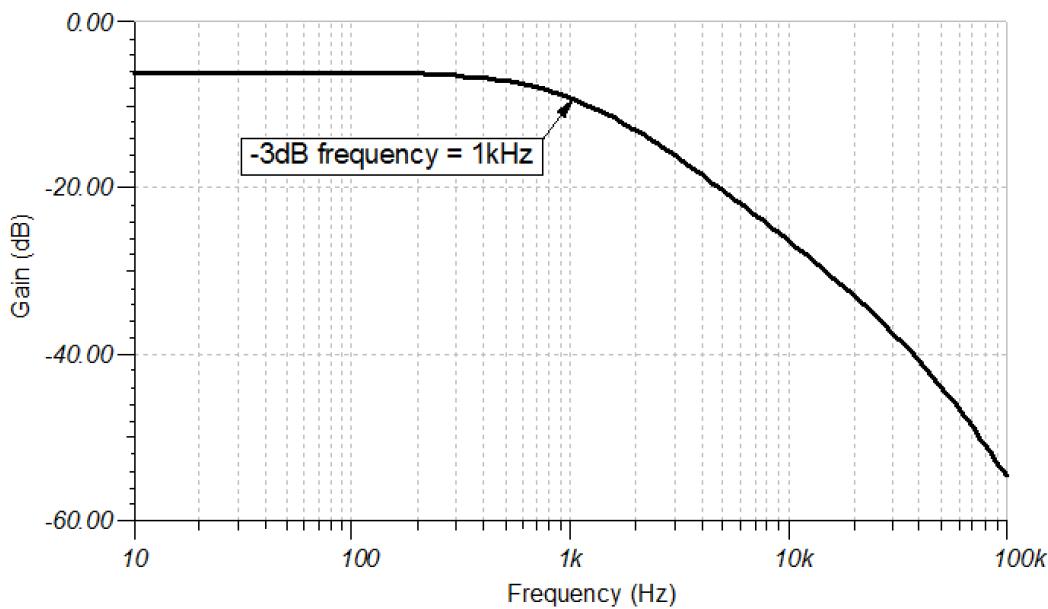
### DC Analysis Simulation Results

The following plot shows the simulated output voltage  $V_{out}$  for the given input current  $I_{in}$ .



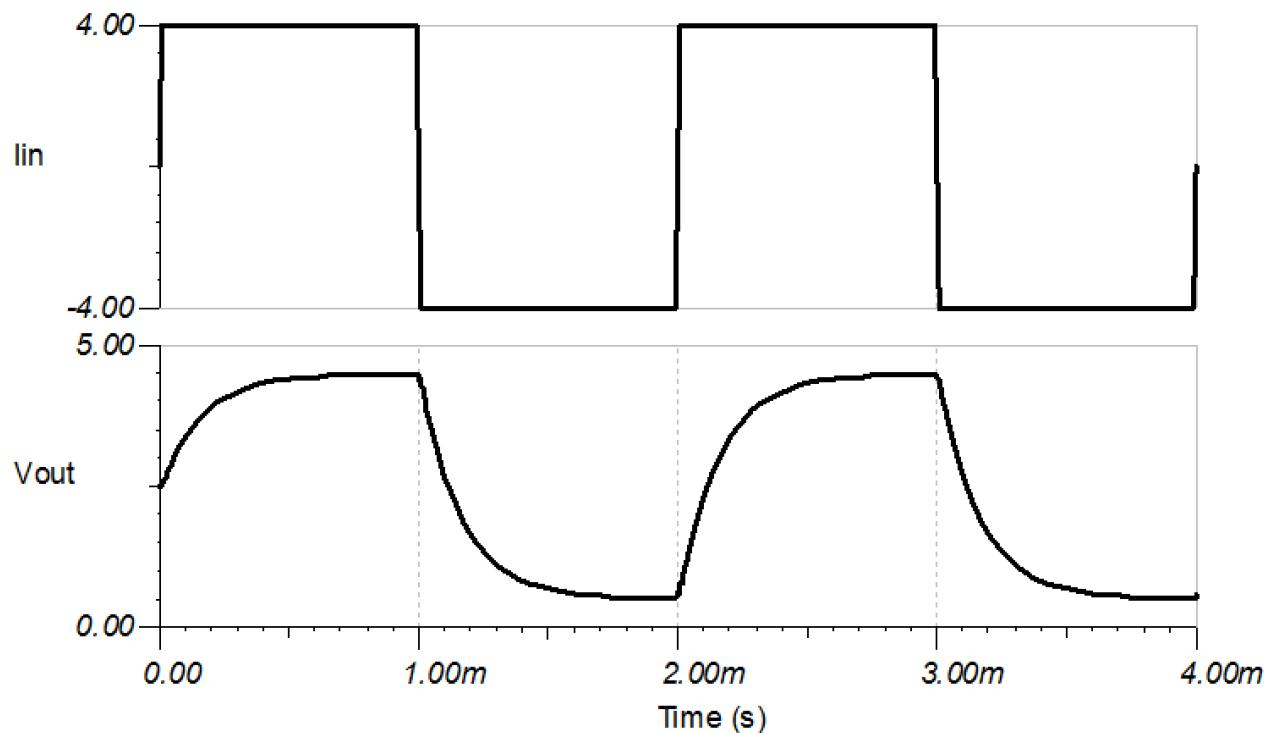
### AC Analysis Simulation Results

The following plot shows the simulated gain vs frequency, as designed for in the design steps.



### Transient Analysis Simulation Results

The following plot shows the simulated delay and settling time of the output  $V_{out}$  for a step response in  $I_{in}$  from  $-4A$  to  $4A$ .



## Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

Circuit SPICE simulation File: <http://proddms.itg.ti.com/fnview/sboc518>

Getting Started with Current Sense Amplifiers video series: <https://training.ti.com/getting-started-current-sense-amplifiers>

Current Sense Amplifiers on TI.com: <http://www.ti.com/amplifier-circuit/current-sense/products.html>

For direct support from TI Engineers use the E2E community: <http://e2e.ti.com>

## Design Featured Current Sense Amplifier

INA214C	
$V_s$	2.7V to 26V
$V_{cm}$	GND-0.1V to 26V
$V_{out}$	GND-0.3V to $V_s+0.3V$
$V_{os}$	$\pm 1\mu V$ typical
$I_q$	65 $\mu A$ typical
$I_b$	28 $\mu A$ typical
<a href="http://www.ti.com/product/INA214">http://www.ti.com/product/INA214</a>	

## Design Alternate Current Sense Amplifiers

INA199C	
$V_s$	2.7V to 26V
$V_{cm}$	GND-0.1V to 26V
$V_{out}$	GND-0.3V to $V_s+0.3V$
$V_{os}$	$\pm 5\mu V$ typical
$I_q$	65 $\mu A$ typical
$I_b$	28 $\mu A$ typical
<a href="http://www.ti.com/product/INA199">http://www.ti.com/product/INA199</a>	

INA181	
$V_s$	2.7V to 5.5V
$V_{cm}$	GND-0.2V to 26V
$V_{out}$	GND-0.3V to $V_s+0.3V$
$V_{os}$	$\pm 100\mu V$ typical
$I_q$	65 $\mu A$ typical
$I_b$	195 $\mu A$ typical
<a href="http://www.ti.com/product/INA181">http://www.ti.com/product/INA181</a>	

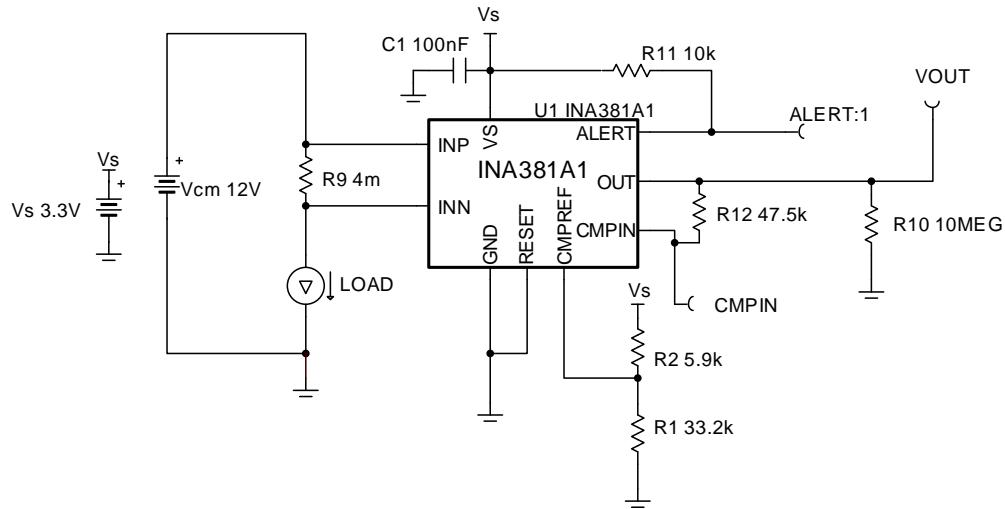
## Overcurrent event detection circuit

### Design Goals

Input		Overcurrent Conditions		Output		Supply	
$I_{load\ Min}$	$I_{load\ Max}$	$I_{OC\_TH}$	$I_{Release\_TH}$	$V_{out\_OC}$	$V_{out\_release}$	$V_S$	$V_{REF}$
1.5A	40A	35A	32A	2.8V	2.61V	3.3V	2.8V

### Design Description

This is a unidirectional current sensing solution generally referred to as overcurrent protection (OCP) that can provide an overcurrent alert signal to shut off a system for a threshold current and re-engage the system once the output drops below a desired voltage ( $V_{out\_release}$ ) lower than the overcurrent output threshold voltage ( $V_{out\_OC}$ ). In this particular setup, the sensing range is from 1.5A to 40A, with the overcurrent threshold defined at 35A ( $I_{OC\_TH}$ ). The system re-asserts the ALERT to high once the current has dropped below 32A ( $I_{Release\_TH}$ ). The current shunt monitor is powered from a 3.3-V supply rail. OCP can be applied to both high-side and low-side topologies. The solution presented in this article is a high-side implementation.



### Design Notes

1. Use low-tolerance, high-precision resistors if using a voltage divider for CMPREF and consider buffering the voltage. Otherwise consider using a low-dropout regulator (LDO), reference or buffered reference voltage circuit to supply the CMPREF.
2. Use decoupling capacitors to ensure the device supply is stable, such as  $C_1$ . Also place the decoupling capacitor as close to the device supply pin as possible.

### Design Steps

1. Calculate the  $R_{\text{shunt}}$  value given 20V/V gain. Use the nearest standard value shunt, preferably lower than the calculated shunt to avoid rail the output prematurely .

$$R_{\text{shunt}} = \frac{V_{\text{out max}}}{\text{gain} \times I_{\text{max}}} = \frac{V_S - 0.02V}{\text{gain} \times I_{\text{max}}} = \frac{3.3V - 0.02V}{20V/V \times 40A} = 0.0041\Omega$$

$R_{\text{standard shunt}} = 4m\Omega$  (standard 1% value)

2. Determine the voltage at the current shunt monitor output for the overcurrent threshold.

$$V_{\text{out\_35A}} = I_{\text{OC\_TH}} \times R_{\text{standard shunt}} \times \text{gain} = 35A \times 4m\Omega \times 20V/V = 2.8V$$

3. Choose a standard resistor value for  $R_1$  and solve for  $R_2$ .

A resistor with kilo-ohm resistance or higher is desired to minimize power loss. Through calculation, 33.2k $\Omega$  and 5.9k $\Omega$  were chosen for resistances  $R_1$  and  $R_2$ .

$$R_2 = \left( \frac{V_S}{V_{\text{out\_35A}}} - 1 \right) \times R_1 = \left( \frac{3.3V}{2.8V} - 1 \right) \times 33.2k\Omega = 5.9k\Omega$$

4. Calculate the resistance ( $R_{\text{Hyst}}$ ) required for the proper hysteresis.

$$R_{\text{Hyst}} = \frac{V_{\text{out\_35A}} - (I_{\text{Release\_TH}} \times R_{\text{standard shunt}} \times \text{gain} + V_{\text{Hyst\_def}})}{I_{\text{Hyst}}}$$

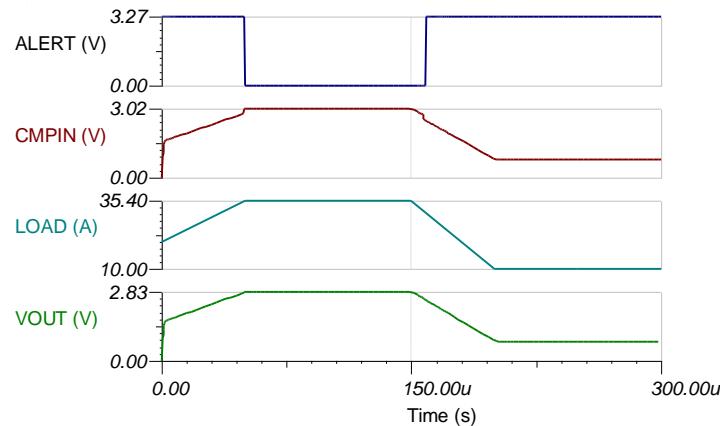
$$R_{\text{Hyst}} = \frac{2.8V - (32A \times 4m\Omega \times 20V/V + 50mV)}{4\mu A} = 47.5k\Omega$$

## Design Simulations

### Transient Simulation Results

Considering [error](#),  $V_{out\_OC}$  is expected to be approximately 2.8V, while  $V_{out\_release}$  is expected to be approximately 2.61V.

### High-Side OCP Simulation Results



The device exhibits an active low on the Alert pin when the load reaches 35A and re-asserts Alert to high when the load drops below 32A. If the user zooms in and looks at the VOUT voltage, and accounts for an expected propagation delay of 0.4 $\mu$ s, the device output is 2.69V at  $I_{OC\_TH}$ , which only has an error of 0.39% with respect to the ideal output of 2.8V. At  $I_{release\_TH}$ , the alert re-asserts to high when the output dropped to 2.58V, which only has an error of 1.15% with respect to the ideal output of 2.61V.

## Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

### Key files for Overcurrent Protection Circuit:

Source files for this design:

[High-Side OCP Tina Model](#)

[Low-Side OCP Tina Model](#)

### Getting Started with Current Sense Amplifiers video series:

<https://training.ti.com/getting-started-current-sense-amplifiers>

### Design Featured Current Sense Amplifier

INA381	
$V_S$	2.7V to 5.5V
$V_{CM}$	GND-0.3V to 26V
$V_{OUT}$	GND+5 $\mu$ V to $V_S$ -0.02V
$V_{OS}$	$\pm$ 100 typical
$I_q$	250 $\mu$ A typical
$I_B$	80 $\mu$ A typical
<a href="http://www.ti.com/product/INA381">http://www.ti.com/product/INA381</a>	

### Design Alternate Current Sense Monitor

	INA301	INA302	INA303
$V_S$	2.7V to 5.5V	2.7V to 5.5V	2.7V to 5.5V
$V_{CM}$	GND-0.3V to 40V	-0.1V to 36V	-0.1V to 36V
$V_{OUT}$	GND+0.02 to $V_S$ -0.05V	GND+0.015 to $V_S$ -0.05V	GND+0.015 to $V_S$ -0.05V
$V_{OS}$	Gain Dependent	Gain Dependent	Gain Dependent
$I_q$	500 $\mu$ A typical	850 $\mu$ A typical	850 $\mu$ A typical
$I_B$	120 $\mu$ A typical	115 $\mu$ A typical	115 $\mu$ A typical
Comparator	Single Comparators	Dual Comparators	Window Comparators
	<a href="http://www.ti.com/product/INA301">http://www.ti.com/product/INA301</a>	<a href="http://www.ti.com/product/INA302">http://www.ti.com/product/INA302</a>	<a href="http://www.ti.com/product/INA303">http://www.ti.com/product/INA303</a>

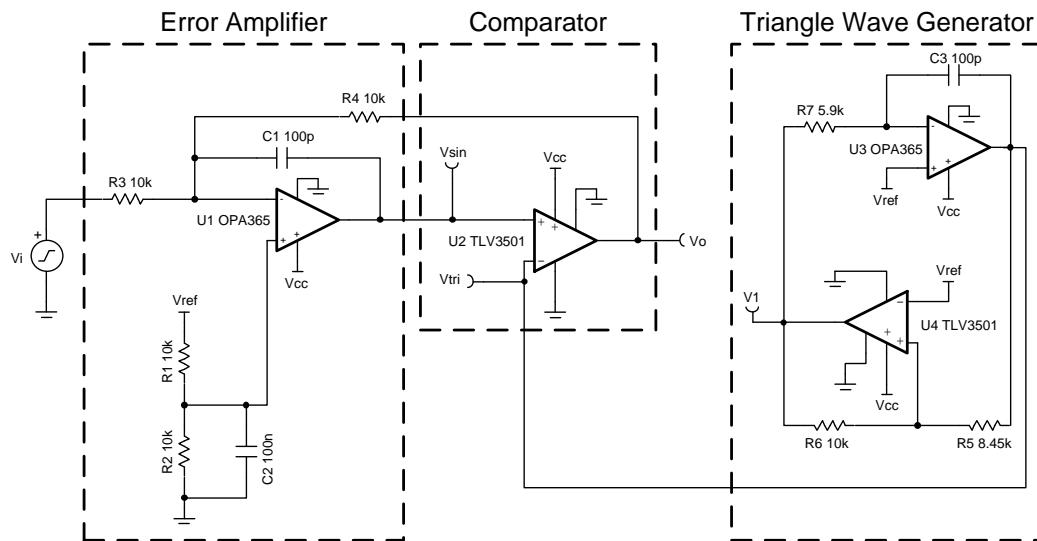
## ***PWM generator circuit***

### **Design Goals**

<b>Input</b>		<b>Output</b>		<b>Supply</b>		
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	$V_{cc}$	$V_{ee}$	$V_{ref}$
-2.0V	2.0V	0V	5V	5V	0V	2.5V

### **Design Description**

This circuit utilizes a triangle wave generator and comparator to generate a 500 kHz pulse-width-modulated (PWM) waveform with a duty cycle that is inversely proportional to the input voltage. An op amp and comparator ( $U_3$  and  $U_4$ ) generate a triangle waveform which is applied to the inverting input of a second comparator ( $U_2$ ). The input voltage is applied to the non-inverting input of  $U_2$ . By comparing the input waveform to the triangle wave, a PWM waveform is produced.  $U_2$  is placed in the feedback loop of an error amplifier ( $U_1$ ) to improve the accuracy and linearity of the output waveform.



### **Design Notes**

1. Use a comparator with push-pull output and minimal propagation delay.
2. Use an op amp with sufficient slew rate, GBW, and voltage output swing.
3. Place the pole created by  $C_1$  below the switching frequency and well above the audio range.
4.  $V_{ref}$  must be low impedance (for example, output of an op amp).

## Design Steps

1. Set the error amplifier inverting signal gain.

$$\text{Gain} = -\frac{R_4}{R_3} = -1 \frac{V}{V}$$

Select  $R_3 = R_4 = 10\text{k}\Omega$

2. Determine  $R_1$  and  $R_2$  to divide  $V_{\text{ref}}$  to cancel the non-inverting gain.

$$V_{o\_dc} = \left(1 + \frac{R_4}{R_3}\right) \left(\frac{R_2}{R_1 + R_2}\right) \times V_{\text{ref}}$$

$R_1 = R_2 = R_3 = R_4 = 10\text{k}\Omega$ ,  $V_{o\_dc} = 2.5\text{V}$

3. The amplitude of  $V_{\text{tri}}$  must be chosen such that it is greater than the maximum amplitude of  $V_i$  (2.0V) to avoid 0% or 100% duty cycle in the PWM output signal. Select  $V_{\text{tri}}$  to be 2.1V. The amplitude of  $V_1 = 2.5\text{V}$ .

$$V_{\text{tri}}(\text{Amplitude}) = \frac{R_5}{R_6} \times V_1(\text{Amplitude})$$

Select  $R_6$  to be  $10\text{k}\Omega$ , then compute  $R_5$

$$R_5 = \frac{V_{\text{tri}}(\text{Amplitude}) \times R_6}{V_1(\text{Amplitude})} = 8.4\text{k}\Omega \approx 8.45\text{k}\Omega \text{ (Standard Value)}$$

4. Set the oscillation frequency to 500kHz.

$$f_t = \frac{R_6}{4 \times R_7 \times R_5 \times C_3}$$

Set  $C_3 = 100\text{pF}$ , then compute  $R_7$

$$R_7 = \frac{R_6}{4 \times f_t \times R_5 \times C_3} = 5.92\text{k}\Omega \approx 5.90\text{k}\Omega \text{ (Standard Value)}$$

5. Choose  $C_1$  to limit amplifier bandwidth to below switching frequency.

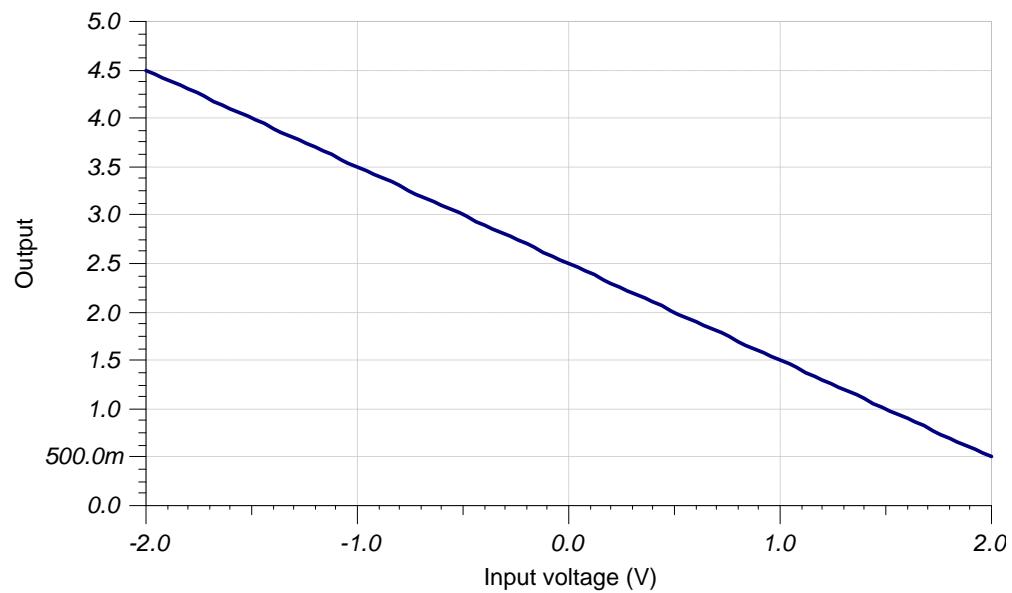
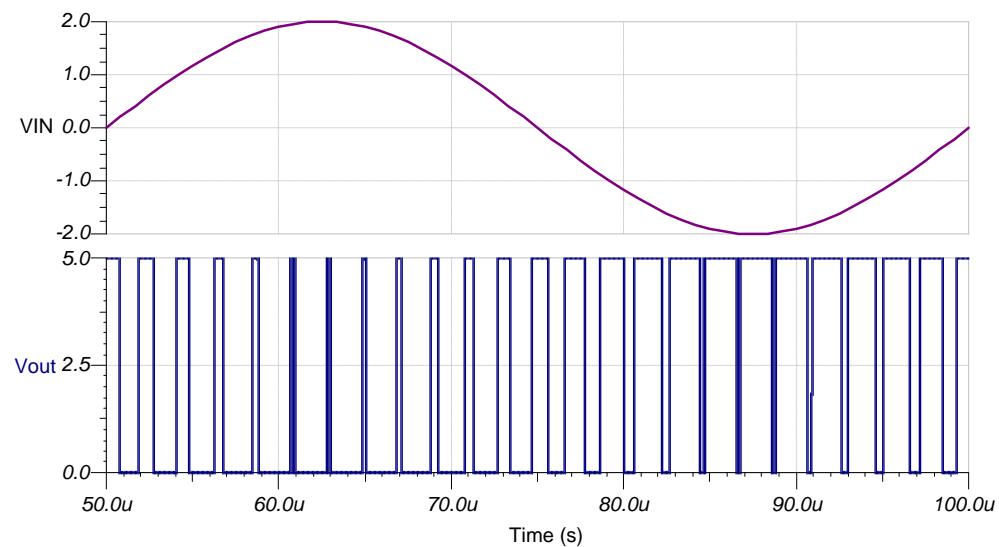
$$f_p = \frac{1}{2 \times \pi \times R_4 \times C_1}$$

$$C_1 = 100\text{pF} \rightarrow f_p = 159\text{kHz}$$

6. Select  $C_2$  to filter noise from  $V_{\text{ref}}$ .

$$C_2 = 100\text{nF} \text{ (Standard Value)}$$

$$f_{\text{div}} = \frac{1}{2 \times \pi \times C_2 \times \frac{R_1 \times R_2}{R_1 + R_2}} = 320\text{Hz}$$

**Design Simulations****DC Simulation Results****Transient Simulation Results**

## Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOC502](#).

See TIPD108, [www.ti.com/tool/tipd108](http://www.ti.com/tool/tipd108)

## Design Featured Op Amp

OPA2365	
$V_{ss}$	2.2V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	100 $\mu$ V
$I_q$	4.6mA
$I_b$	2pA
<b>UGBW</b>	50MHz
<b>SR</b>	25V/ $\mu$ s
<b>#Channels</b>	2
<a href="http://www.ti.com/product/opa2365">www.ti.com/product/opa2365</a>	

## Design Comparator

TLV3502	
$V_{ss}$	2.2V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	1mV
$I_q$	3.2mA
$I_b$	2pA
<b>UGBW</b>	-
<b>SR</b>	-
<b>#Channels</b>	2
<a href="http://www.ti.com/product/tlv3502">www.ti.com/product/tlv3502</a>	

## Design Alternate Op Amp

OPA2353	
$V_{ss}$	2.7V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	3mV
$I_q$	5.2mA
$I_b$	0.5pA
<b>UGBW</b>	44MHz
<b>SR</b>	22V/ $\mu$ s
<b>#Channels</b>	2
<a href="http://www.ti.com/product/opa2353">www.ti.com/product/opa2353</a>	

## Revision History

Revision	Date	Change
A	January 2019	Downscale the title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page.

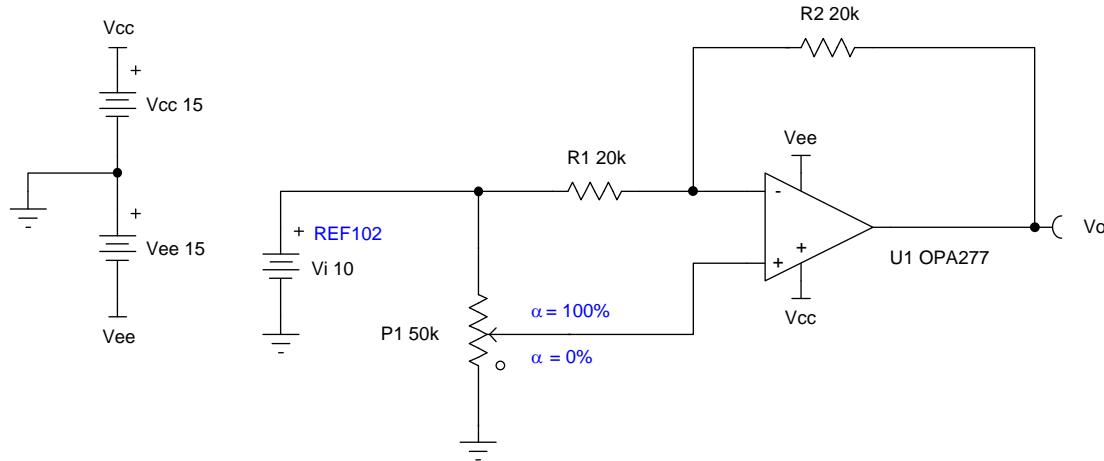
## Adjustable reference voltage circuit

### Design Goals

Input	Output		Supply	
$V_i$	$V_{oMin}$	$V_{oMax}$	$V_{cc}$	$V_{ee}$
10V	-10V	10V	15V	-15V

### Design Description

This circuit combines an inverting and non-inverting amplifier to make a reference voltage adjustable from the negative of the input voltage up to the input voltage. Gain can be added to increase the maximum negative reference level.

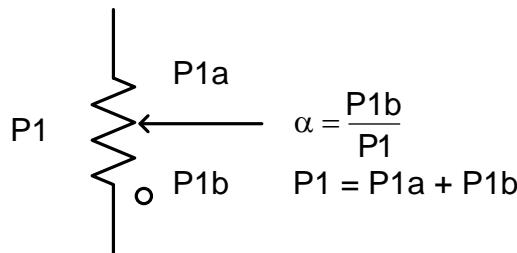


### Design Notes

1. Observe the common-mode and output swing limitations of the op amp.
2. Mismatch in  $R_1$  and  $R_2$  results in a gain error. Selecting  $R_2 > R_1$  increases the maximum negative voltage, and selecting  $R_2 < R_1$  decreases the maximum negative voltage. In either case, the maximum positive voltage is always equal to the input voltage. This relationship is inverted if a negative input reference voltage is used.
3. Select the potentiometer based on the desired resolution of the reference. Generally, the potentiometers can be set accurately to within one-eighth of a turn. For a 10-turn pot this means alpha ( $\alpha$ ) may be off by as much as 1.25%.

## Design Steps

Alpha represents the potentiometer setting relative to ground. This is the fraction of the input voltage that will be applied to the non-inverting terminal of the op amp and amplified by the non-inverting gain.



The transfer function of this circuit follows:

$$\frac{V_o}{V_i} = -\frac{R_2}{R_1} + \alpha(1 + \frac{R_2}{R_1})$$

1. If  $R_2 = R_1 = 20k\Omega$ , then the equation for  $V_o$  simplifies as the following shows:

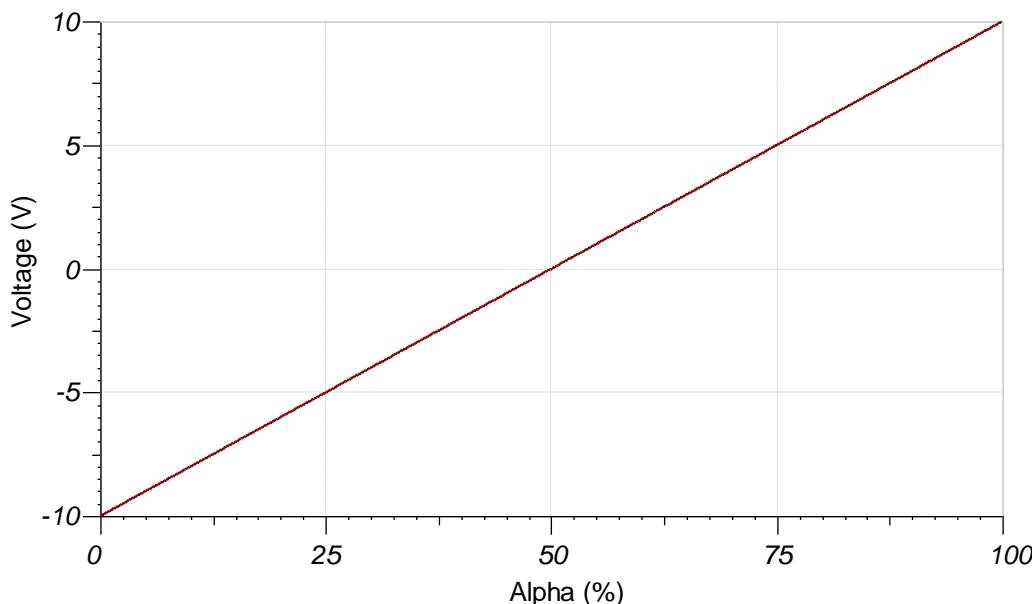
$$V_o = (2\alpha - 1) \times V_i$$

2. If  $V_i = 10V$  and  $\alpha = 0.75$ , the value of  $V_o$  can be determined.

$$V_o = (2 \times 0.75 - 1) \times 10 = 5V$$

## Design Simulations

### DC Simulation Results



### Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See the TINA-TI™ circuit simulation file, [SBOMAU2](#).

See [TI Precision Labs - Op Amps](#).

### Design Featured Op Amp

OPA277	
<b>V<sub>ss</sub></b>	4V to 36V
<b>V<sub>inCM</sub></b>	V <sub>ee</sub> +2V to V <sub>cc</sub> -2V
<b>V<sub>out</sub></b>	V <sub>ee</sub> +0.5V to V <sub>cc</sub> -1.2V
<b>V<sub>os</sub></b>	10µV
<b>I<sub>q</sub></b>	790µA/Ch
<b>I<sub>b</sub></b>	500pA
<b>UGBW</b>	1MHz
<b>SR</b>	0.8V/µs
<b>#Channels</b>	1,2,4
<a href="http://www.ti.com/product/opa277">http://www.ti.com/product/opa277</a>	

### Design Alternate Op Amp

OPA172	
<b>V<sub>ss</sub></b>	4.5V to 36V
<b>V<sub>inCM</sub></b>	V <sub>ee</sub> -0.1V to V <sub>cc</sub> -2V
<b>V<sub>out</sub></b>	Rail-to-rail
<b>V<sub>os</sub></b>	200µV
<b>I<sub>q</sub></b>	1.6mA/Ch
<b>I<sub>b</sub></b>	8pA
<b>UGBW</b>	10MHz
<b>SR</b>	10V/µs
<b>#Channels</b>	1,2,4
<a href="http://www.ti.com/product/opa172">http://www.ti.com/product/opa172</a>	

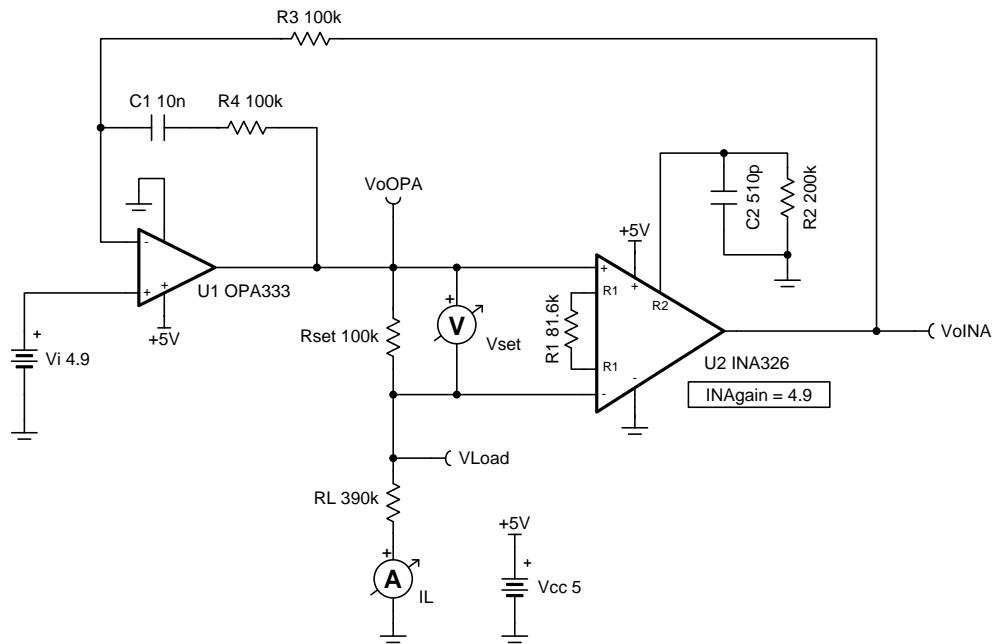
## Low-level voltage-to-current converter circuit

### Design Goals

Input		Output		Supply		Load Resistance ( $R_L$ )	
$V_{iMin}$	$V_{iMax}$	$I_{LMin}$	$I_{LMax}$	$V_{cc}$	$V_{ee}$	$R_{LMin}$	$R_{LMax}$
0.49V	4.9V	1 $\mu$ A	10 $\mu$ A	5V	0V	0 $\Omega$	390k $\Omega$

### Design Description

This circuit delivers a precise low-level current,  $I_L$ , to a load,  $R_L$ . The design operates on a single 5-V supply and uses one precision low-drift op amp and one instrumentation amplifier. Simple modifications can change the range and accuracy of the voltage-to-current (V-I) converter.



### Design Notes

1. Voltage compliance is dominated by op amp linear output swing (see data sheet  $A_{OL}$  test conditions) and instrumentation amplifier linear output swing. See the [Common-Mode Input Range Calculator for Instrumentation Amplifiers](#) for more information.
2. Voltage compliance, along with  $R_{LMin}$ ,  $R_{LMax}$ , and  $R_{set}$  bound the  $I_L$  range.
3. Check op amp and instrumentation amplifier input common-mode voltage range.
4. Stability analysis must be done to choose  $R_4$  and  $C_1$  for stable operation.
5. Loop stability analysis to select  $R_4$  and  $C_1$  will be different for each design. The compensation shown is only valid for the resistive load ranges used in this design. Other types of loads, op amps, or instrumentation amplifiers, or both will require different compensation. See the [Design References](#) section for more op amp stability resources.

## Design Steps

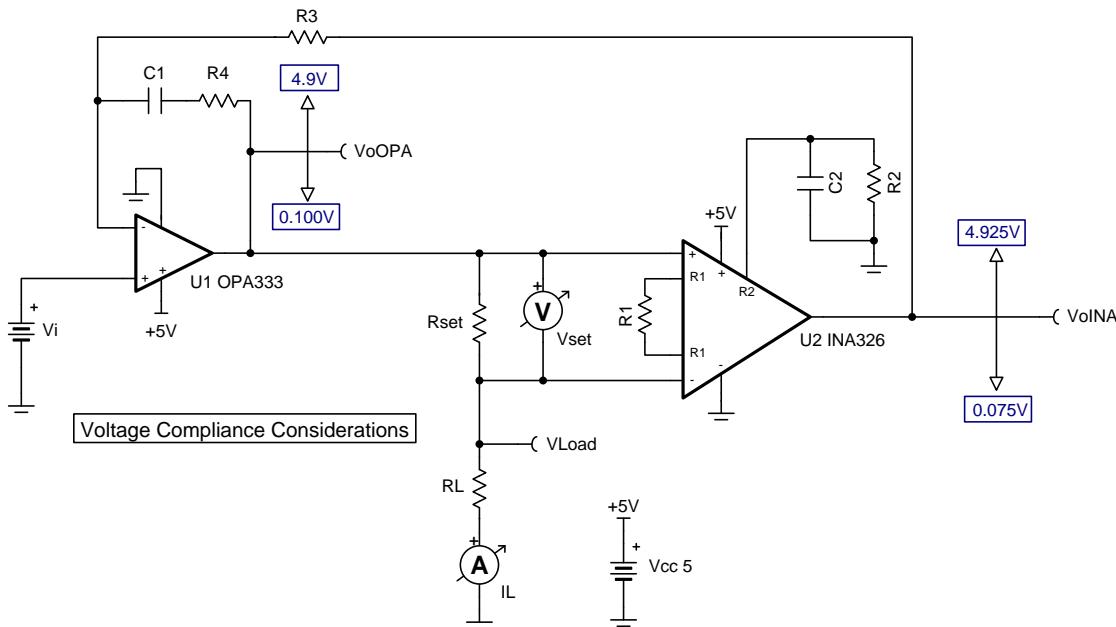
1. Select  $R_{set}$  and check  $I_{LMin}$  based on voltage compliance.

$$I_{LMax} = \frac{V_{oOPAMax}}{R_{set} + R_{LMax}}$$

$$10\mu A = \frac{4.9V}{R_{set} + 390k\Omega} \rightarrow R_{set} = 100k\Omega$$

$$I_{LMin} = \frac{V_{oOPAMin}}{R_{set} + R_{LMin}}$$

$$I_{LMin} = \frac{0.1V}{100k\Omega + 0\Omega} = 1\mu A$$



2. Compute instrumentation amplifier gain, G.

$$V_{setMin} = I_{LMin} \times R_{set} = 1\mu A \times 100k\Omega = 0.1V$$

$$V_{setMax} = I_{LMax} \times R_{set} = 10\mu A \times 100k\Omega = 1V$$

$$G = \frac{V_{setMax} - V_{setMin}}{V_{setMax} - V_{setMin}}$$

$$G = \frac{4.9V - 0.49V}{1V - 0.1V} = 4.9$$

3. Choose  $R_1$  for INA326 instrumentation amplifier gain, G. Use data sheet recommended  $R_2 = 200k\Omega$  and  $C_2 = 510pF$ .

$$G = 2 \times \left( \frac{R_2}{R_1} \right)$$

$$R_1 = \frac{2 \times R_2}{G}$$

$$R_1 = \left( \frac{2 \times 200k\Omega}{4.9} \right) = 81.6327k\Omega \approx 81.6k\Omega$$

4. The final transfer function of the circuit follows:

$$I_L = \frac{V_i}{G \times R_{set}}$$

$$I_L = \frac{V_i}{4.9 \times 100k\Omega} = \frac{V_i}{490k\Omega}$$

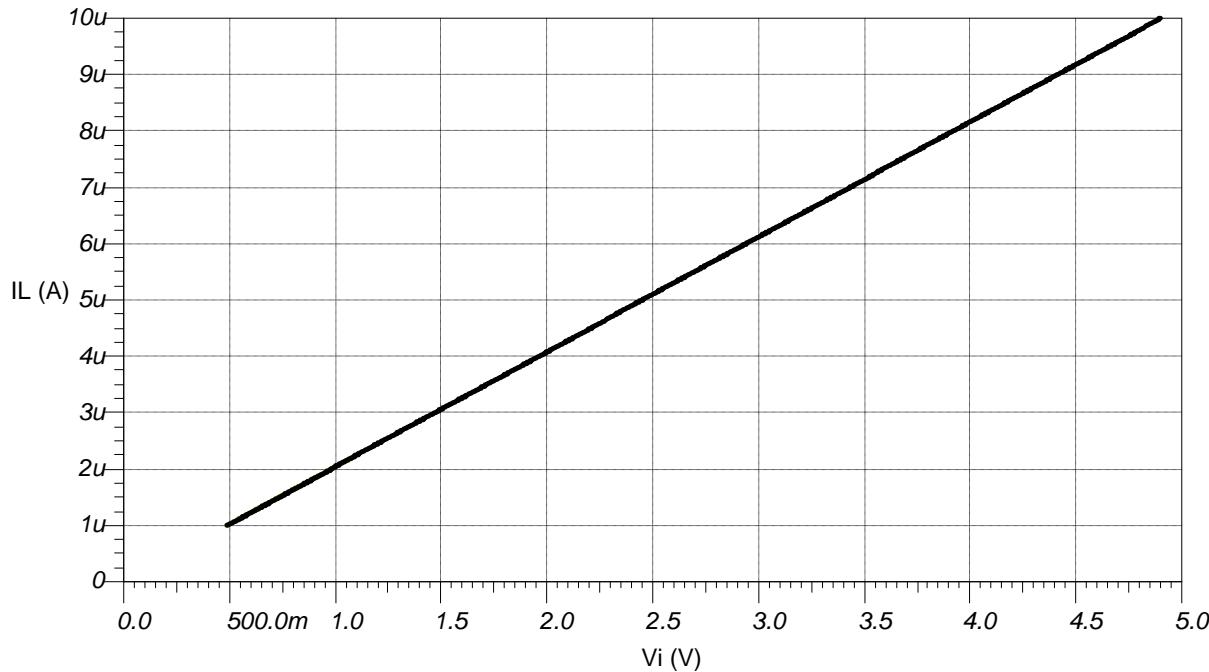
$$V_i = 0.49V \rightarrow I_L = 1\mu A$$

$$V_i = 4.9V \rightarrow I_L = 10\mu A$$

## Design Simulations

### DC Simulation Results

$V_i$	$R_L$	$I_L$	$V_{oOPA}$	$V_{oOPA}$ Compliance	$V_{oINA}$	$V_{oINA}$ Compliance
0.49V	0Ω	0.999627μA	99.982723mV	100mV to 4.9V	490.013346mV	75mV to 4.925V
0.49V	390kΩ	0.999627μA	489.837228mV	100mV to 4.9V	490.013233mV	75mV to 4.925V
4.9V	0Ω	9.996034μA	999.623352mV	100mV to 4.9V	4.900016V	75mV to 4.925V
4.9V	390kΩ	9.996031μA	4.898075V	100mV to 4.9V	4.900015V	75mV to 4.925V



## Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See the TINA-TI™ circuit simulation file, [SBOMAT8](#).

See TIPD107, <http://www.ti.com/tool/TIPD107>.

See [Solving Op Amp Stability Issues - E2E FAQ](#).

See [TI Precision Labs - Op Amps](#).

## Design Featured Op Amp

OPA333	
$V_{ss}$	1.8V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	2 $\mu$ V
$I_q$	17 $\mu$ A/Ch
$I_b$	70pA
<b>UGBW</b>	350kHz
<b>SR</b>	0.16V/ $\mu$ s
<b>#Channels</b>	1,2
<a href="http://www.ti.com/product/opa333">http://www.ti.com/product/opa333</a>	

## Design Featured Instrumentation Amplifier

INA326	
$V_{ss}$	2.7V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	20 $\mu$ V
$I_q$	2.4mA
$I_b$	0.2nA
<b>UGBW</b>	1kHz (set by 1kHz filter)
<b>SR</b>	0.012V/ $\mu$ s (set by 1kHz filter)
<b>#Channels</b>	1
<a href="http://www.ti.com/product/INA326">http://www.ti.com/product/INA326</a>	

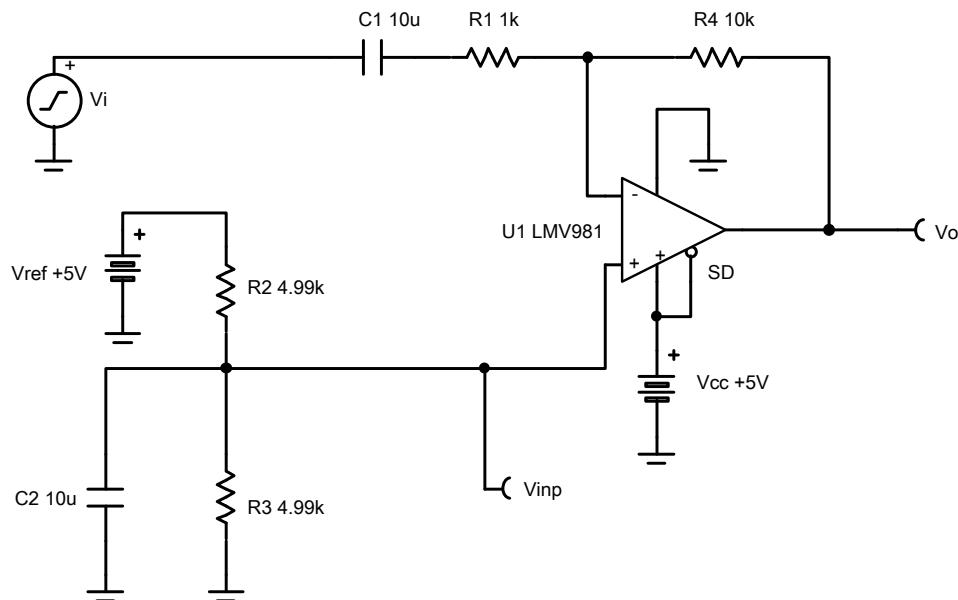
## AC coupled (HPF) inverting amplifier circuit

### Design Goals

Input		Output		Supply		
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	$V_{cc}$	$V_{ee}$	$V_{ref}$
-240mV	240mV	0.1V	4.9V	5V	0V	5V

### Design Description

This circuit amplifies an AC signal and shifts the output signal so that it is centered at half the power supply voltage. Note that the input signal has zero DC offset so it swings above and below ground. The key benefit of this circuit is that it accepts signals which swing below ground even though the amplifier does not have a negative power supply.



### Design Notes

1.  $R_1$  sets the AC input impedance.  $R_4$  loads the op amp output.
2. Use low feedback resistances to reduce noise and minimize stability concerns.
3. Set the output range based on linear output swing (see  $A_{ol}$  specification).
4. The cutoff frequency of the circuit is dependent on the gain bandwidth product (GBP) of the amplifier. Additional filtering can be accomplished by adding a capacitor in parallel to  $R_4$ . Adding a capacitor in parallel with  $R_4$  will also improve stability of the circuit if high-value resistors are used.

### Design Steps

1. Select  $R_1$  and  $R_4$  to set the AC voltage gain.

$$R_1 = 1 \text{ k}\Omega \text{ (Standard Value)}$$

$$R_4 = R_1 \times |G_{ac}| = 1 \text{ k}\Omega \times |-10\frac{V}{V}| = 10\text{k}\Omega \text{ (Standard Value)}$$

2. Select  $R_2$  and  $R_3$  to set the DC output voltage to 2.5V.

$$R_3 = 4.99\text{k}\Omega \text{ (Standard Value)}$$

$$R_2 = \frac{R_3 \times V_{ref}}{V_{DC}} - R_3 = \frac{4.99\text{k}\Omega \times 5\text{V}}{2.5\text{V}} - 4.99\text{k}\Omega = 4.99\text{k}\Omega$$

3. Choose a value for the lower cutoff frequency,  $f_l$ , then calculate  $C_1$ .

$$f_l = 16\text{Hz}$$

$$C_1 = \frac{1}{2\pi \times R_1 \times f_l} = \frac{1}{2\pi \times 1 \text{ k}\Omega \times 16\text{Hz}} = 9.94\mu\text{F} \approx 10\mu\text{F} \text{ (Standard Value)}$$

4. Choose a value for  $f_{div}$ , then calculate  $C_2$ .

$$f_{div} = 6.4\text{Hz}$$

$$R_{div} = \frac{R_2 \times R_3}{R_2 + R_3} = \frac{4.99\text{k}\Omega \times 4.99\text{k}\Omega}{4.99\text{k}\Omega + 4.99\text{k}\Omega} = 2.495\text{k}\Omega$$

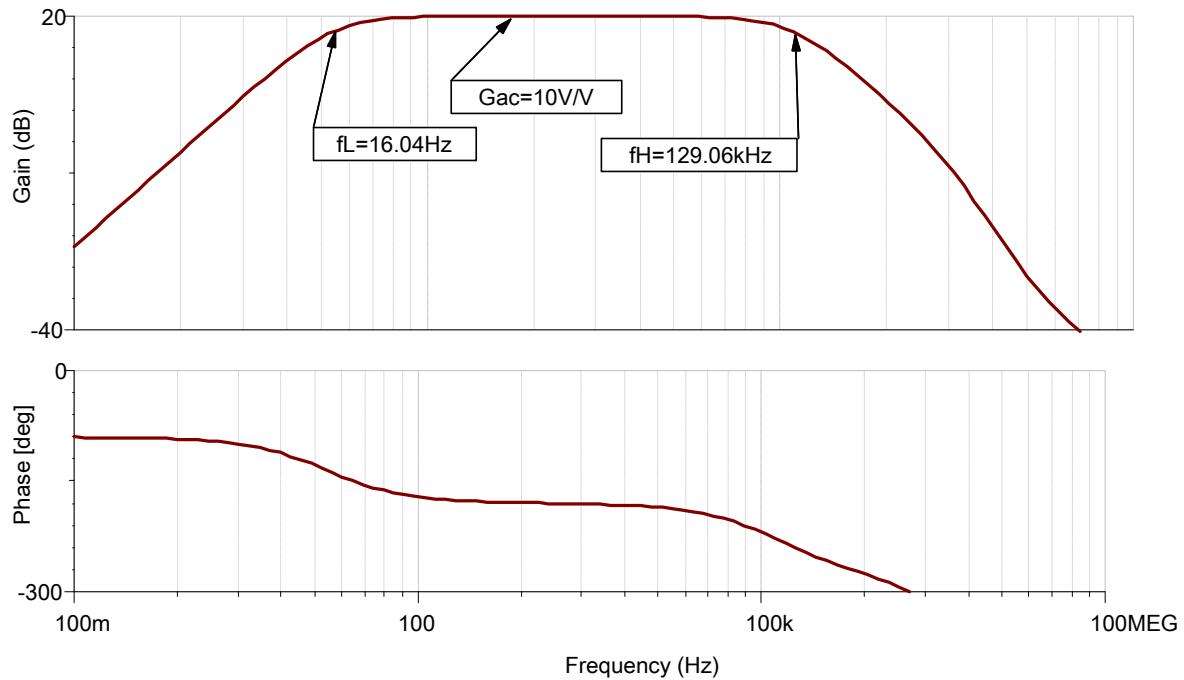
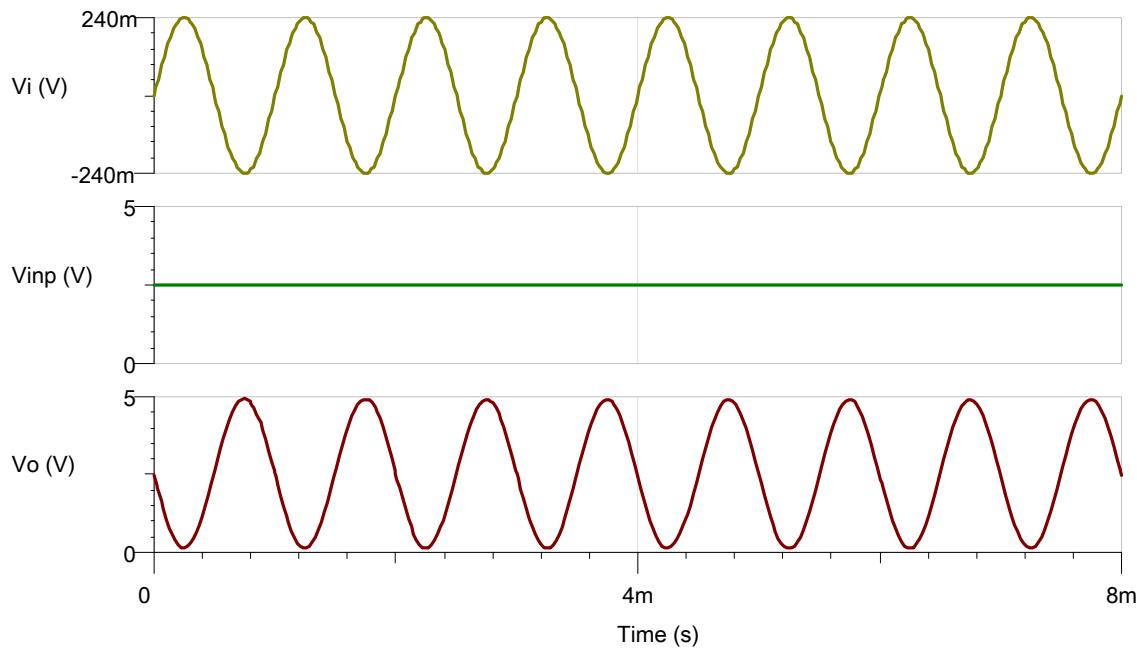
$$C_2 = \frac{1}{2\pi \times R_{div} \times f_{div}} = \frac{1}{2\pi \times 2.495\text{k}\Omega \times 6.4\text{Hz}} = 9.96\mu\text{F} \approx 10\mu\text{F} \text{ (Standard Value)}$$

5. The upper cutoff frequency,  $f_h$ , is set by the noise gain of this circuit and the gain bandwidth (GBW) of the device (LMV981).

$$\text{GBW} = 1.5\text{MHz}$$

$$G_{noise} = 1 + \frac{R_4}{R_1} = 1 + \frac{10\text{k}\Omega}{1 \text{ k}\Omega} = 11\frac{V}{V}$$

$$f_h = \frac{\text{GBW}}{G_{noise}} = \frac{1.5\text{MHz}}{11\frac{V}{V}} = 136.3\text{kHz}$$

**Design Simulations**
**AC Simulation Results**

**Transient Simulation Results**


## Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOC504](#).

See TIPD185, [www.ti.com/tool/tipd185](http://www.ti.com/tool/tipd185).

## Design Featured Op Amp

LMV981	
$V_{cc}$	1.8V to 5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	1mV
$I_q$	116 $\mu$ A
$I_b$	14nA
<b>UGBW</b>	1.5MHz
<b>SR</b>	0.42V/ $\mu$ s
<b>#Channels</b>	1, 2
<a href="http://www.ti.com/product/lmv981-n">www.ti.com/product/lmv981-n</a>	

## Design Alternate Op Amp

LMV771	
$V_{cc}$	2.7V to 5V
$V_{inCM}$	$V_{ee}$ to ( $V_{cc}$ –0.9V)
$V_{out}$	Rail-to-rail
$V_{os}$	0.25mV
$I_q$	600 $\mu$ A
$I_b$	–0.23pA
<b>UGBW</b>	3.5MHz
<b>SR</b>	1.5V/ $\mu$ s
<b>#Channels</b>	1, 2
<a href="http://www.ti.com/product/lmv771">www.ti.com/product/lmv771</a>	

## Revision History

Revision	Date	Change
A	January 2019	Downscale the title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page.

## AC coupled (HPF) non-inverting amplifier circuit

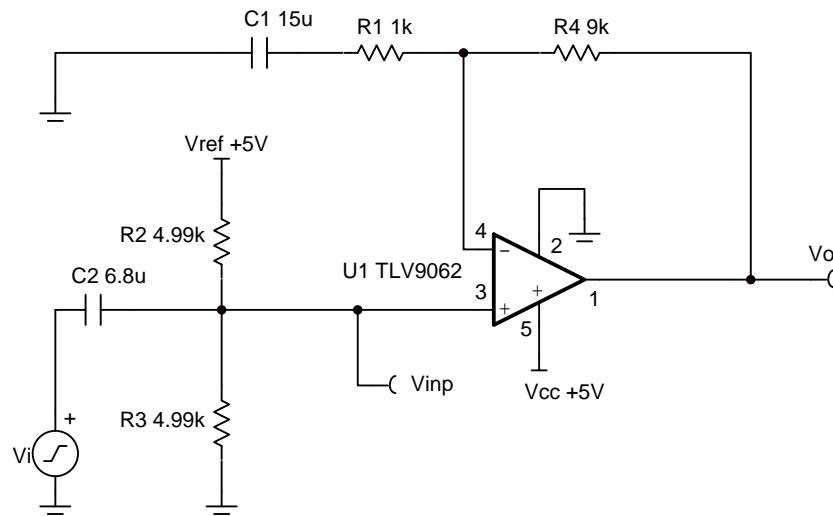
### Design Goals

Input		Output		Supply		
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	$V_{cc}$	$V_{ee}$	$V_{ref}$
-240mV	240mV	0.1V	4.9V	5V	0V	5V

Lower Cutoff Freq. ( $f_L$ )	Upper Cutoff Freq. ( $f_H$ )	AC Gain ( $G_{ac}$ )
16Hz	$\geq 1\text{MHz}$	10V/V

### Design Description

This circuit amplifies an AC signal, and shifts the output signal so that it is centered at one-half the power supply voltage. Note that the input signal has zero DC offset so it swings above and below ground. The key benefit of this circuit is that it accepts signals which swing below ground even though the amplifier does not have a negative power supply.



### Design Notes

1. The voltage at  $V_{inp}$  sets the input common-mode voltage.
2.  $R_2$  and  $R_3$  load the input signal for AC frequencies.
3. Use low feedback resistance for low noise.
4. Set the output range based on linear output swing (see  $A_{ol}$  specification of op amp).
5. The circuit has two real poles that determine the high-pass filter  $-3\text{dB}$  frequency. Set them both to  $f_L/1.557$  to achieve  $-3\text{dB}$  at the lower cutoff frequency ( $f_L$ ).

## Design Steps

1. Select  $R_1$  and  $R_4$  to set the AC voltage gain.

$$R_1 = 1 \text{ k}\Omega \text{ (Standard Value)}$$

$$R_4 = R_1 \times (G_{ac} - 1) = 1 \text{ k}\Omega \times (10\frac{V}{V} - 1) = 9\text{k}\Omega \text{ (Standard Value)}$$

2. Select  $R_2$  and  $R_3$  to set the DC output voltage ( $V_{DC}$ ) to 2.5V, or mid-supply.

$$R_3 = 4.99\text{k}\Omega \text{ (Standard Value)}$$

$$R_2 = \frac{R_3 \times V_{ref}}{V_{DC}} - R_3 = \frac{4.99\text{k}\Omega \times 5\text{V}}{2.5\text{V}} - 4.99\text{k}\Omega = 4.99\text{k}\Omega$$

3. Select  $C_1$  based on  $f_L$  and  $R_1$ .

$$f_L = 16\text{Hz}$$

$$C_1 = \frac{1}{2 \times \pi \times R_1 \times \left( \frac{f_L}{1.557} \right)} = \frac{1}{2 \times \pi \times 1 \text{ k}\Omega \times 10.3\text{Hz}} = 15.5\mu\text{F} \approx 15\mu\text{F} \text{ (Standard Value)}$$

4. Select  $C_2$  based on  $f_L$ ,  $R_2$ , and  $R_3$ .

$$R_{div} = \frac{R_2 \times R_3}{R_2 + R_3} = \frac{4.99\text{k}\Omega \times 4.99\text{k}\Omega}{4.99\text{k}\Omega + 4.99\text{k}\Omega} = 2.495\text{k}\Omega$$

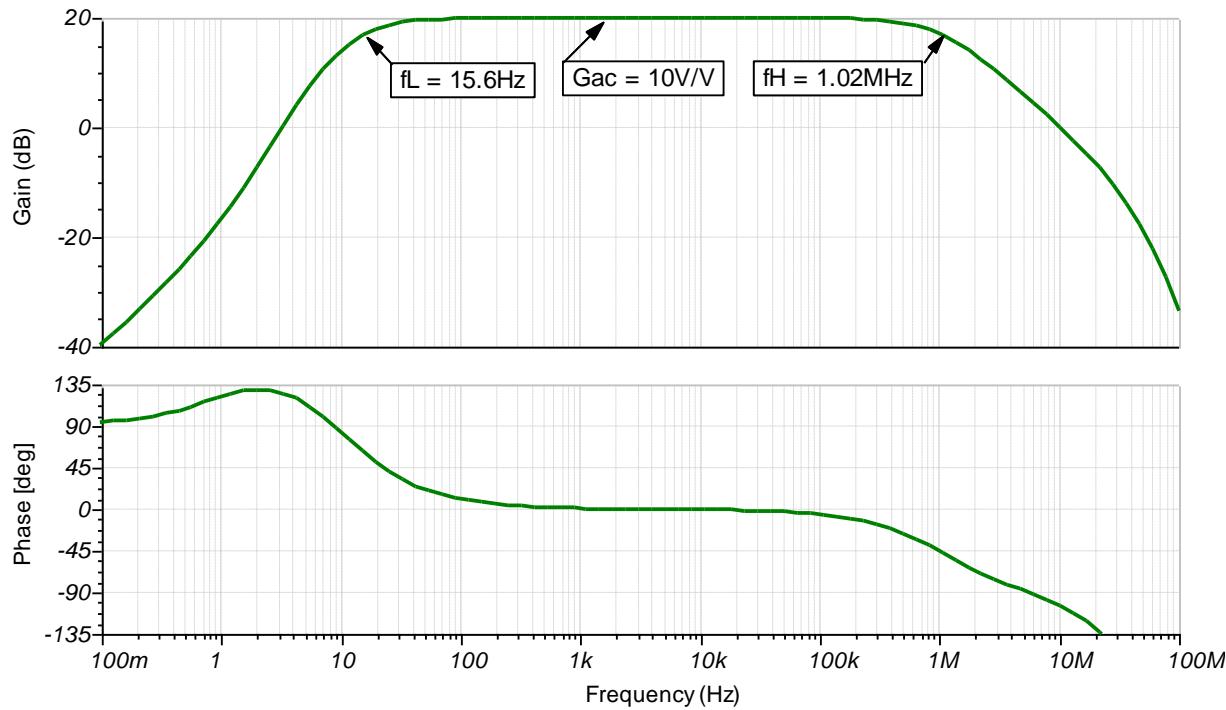
$$C_2 = \frac{1}{2 \times \pi \times R_{div} \times \left( \frac{f_L}{1.557} \right)} = \frac{1}{2 \times \pi \times 2.495\text{k}\Omega \times 10.3\text{Hz}} = 6.4\mu\text{F} \rightarrow 6.8\mu\text{F} \text{ (Standard Value)}$$

5. The upper cutoff frequency ( $f_H$ ) is set by the non-inverting gain of this circuit and the gain bandwidth (GBW) of the device (TLV9062).

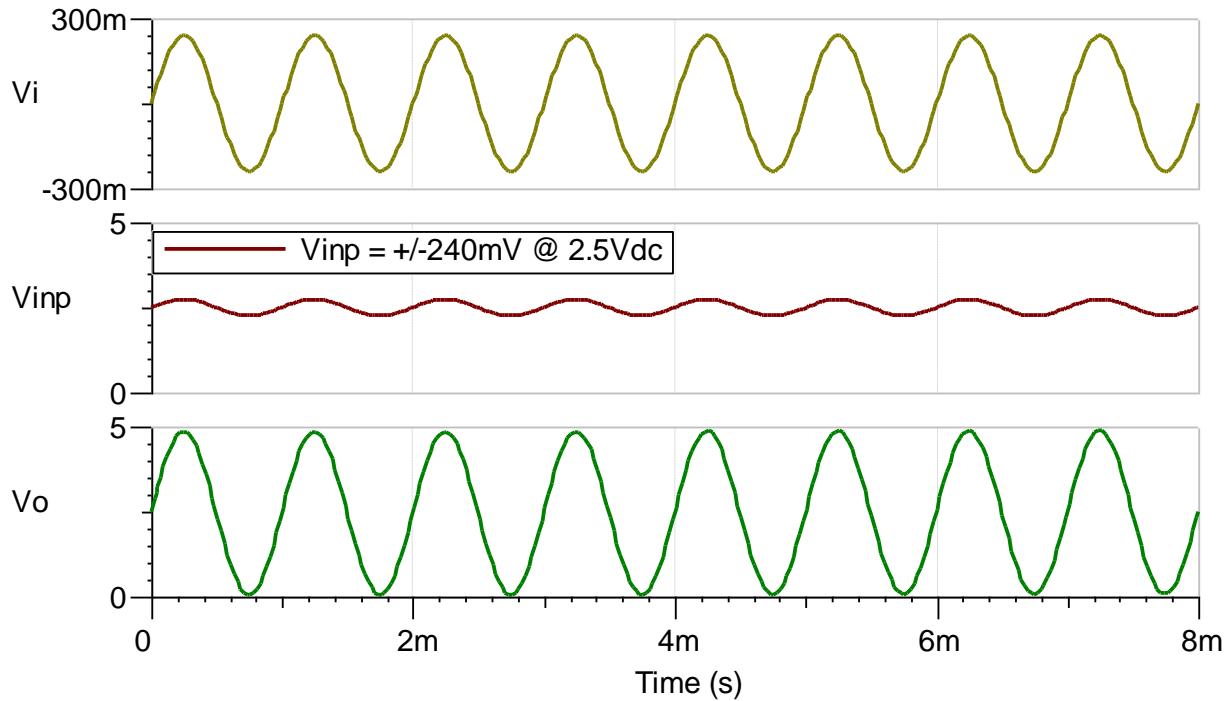
$$f_H = \frac{\text{GBW of TLV9062}}{G_{ac}} = \frac{10\text{MHz}}{10\frac{V}{V}} = 1 \text{ MHz}$$

### Design Simulations

#### AC Simulation Results



#### Transient Simulation Results



## Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOC505](#).

See TIPD185, [www.ti.com/tool/tipd185](http://www.ti.com/tool/tipd185).

## Design Featured Op Amp

TLV9062	
$V_{cc}$	1.8V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	300 $\mu$ V
$I_q$	538 $\mu$ A
$I_b$	0.5pA
UGBW	10MHz
SR	6.5V/ $\mu$ s
#Channels	1, 2, 4
<a href="http://www.ti.com/product/tlv9062">www.ti.com/product/tlv9062</a>	

## Design Alternate Op Amp

OPA192	
$V_{cc}$	4.5V to 36V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	5 $\mu$ V
$I_q$	1mA/Ch
$I_b$	5pA
UGBW	10MHz
SR	20V/ $\mu$ s
#Channels	1, 2, 4
<a href="http://www.ti.com/product/opa192">www.ti.com/product/opa192</a>	

## Revision History

Revision	Date	Change
A	January 2019	Downscale the title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page.

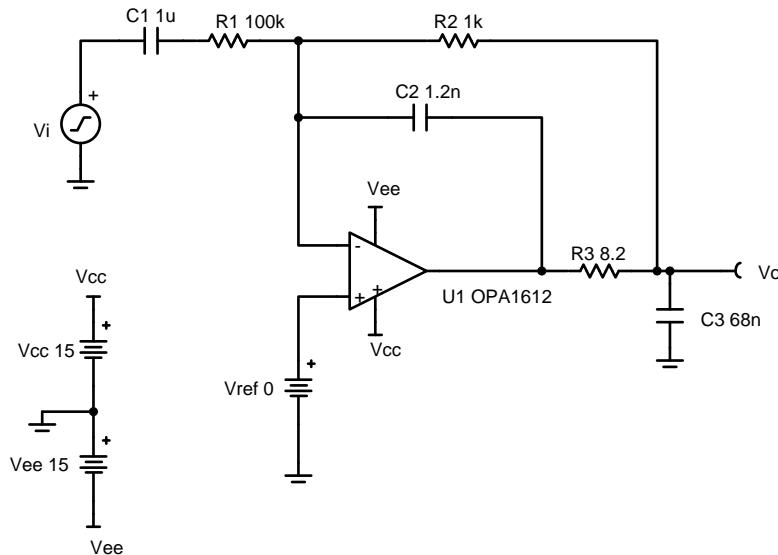
## Band pass filtered inverting attenuator circuit

### Design Goals

Input		Output		Supply		
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	$V_{cc}$	$V_{ee}$	$V_{ref}$
100mV <sub>pp</sub>	50V <sub>pp</sub>	1mV <sub>pp</sub>	500mV <sub>pp</sub>	15V	-15V	0V

### Design Description

This tunable band-pass attenuator reduces signal level by  $-40\text{dB}$  over the frequency range from  $10\text{Hz}$  to  $100\text{kHz}$ . It also allows for independent control of the DC output level. For this design, the pole frequencies were selected outside the pass band to minimize attenuation within the specified bandwidth range.



### Design Notes

1. If a DC voltage is applied to  $V_{ref}$  be sure to check common mode limitations.
2. Keep  $R_3$  as small as possible to avoid loading issues while maintaining stability.
3. Keep the frequency of the second pole in the low-pass filter ( $f_{p3}$ ) at least twice the frequency of the first low-pass filter pole ( $f_{p2}$ ).

### Design Steps

1. Set the passband gain.

$$\text{Gain} = -\frac{R_2}{R_1} = -0.01 \frac{V}{V} (-40\text{dB})$$

$$R_1 = 100\text{k}\Omega$$

$$R_2 = 0.01 \times R_1 = 1 \text{ k}\Omega$$

2. Set high-pass filter pole frequency ( $f_{p1}$ ) below  $f_i$ .

$$f_i = 10\text{Hz}, f_{p1} = 2.5 \text{ Hz}$$

3. Set low-pass filter pole frequency ( $f_{p2}$  and  $f_{p3}$ ) above  $f_h$ .

$$f_h = 100\text{kHz}$$

$$f_{p2} = 150\text{kHz}$$

$$f_{p3} \geq 2 \times f_{p2} = 300\text{kHz}$$

$$f_{p3} = 300\text{kHz}$$

4. Calculate  $C_1$  to set the location of  $f_{p1}$ .

$$C_1 = \frac{1}{2\pi \times R_1 \times f_{p1}} = \frac{1}{2\pi \times 100\text{k}\Omega \times 2.5\text{Hz}} = 0.636 \mu\text{F} \approx 1 \mu\text{F} \text{ (Standard Value)}$$

5. Select components to set  $f_{p2}$  and  $f_{p3}$ .

$$R_3 = 8.2\Omega \text{ (provides stability for cap loads up to 100nF)}$$

$$C_2 = \frac{1}{2\pi \times (R_2 + R_3) \times f_{p2}} = \frac{1}{2\pi \times 1008.2\Omega \times 150\text{kHz}} \\ = 1052\text{pF} \approx 1200\text{pF} \text{ (Standard Value)}$$

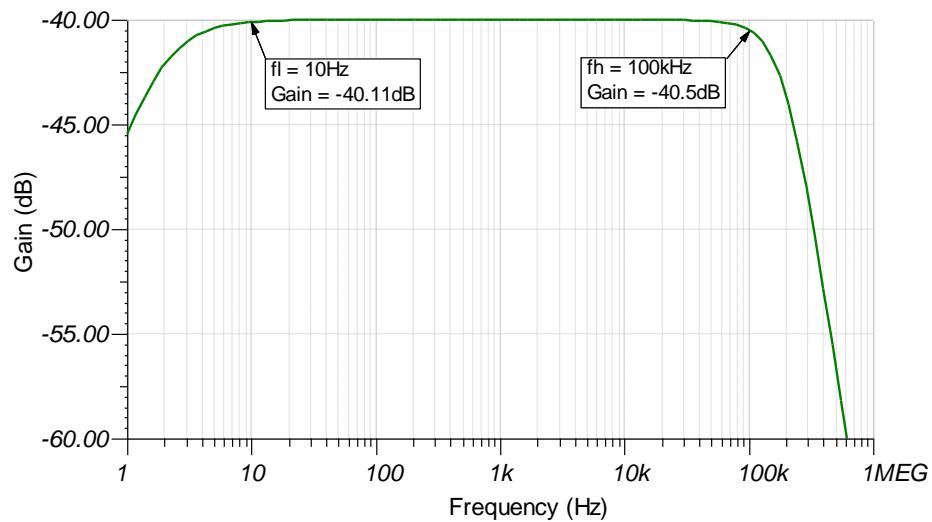
$$C_3 = \frac{1}{2\pi \times R_3 \times f_{p3}} = \frac{1}{2\pi \times 8.2\Omega \times 300\text{kHz}} = 64.7 \text{ nF} \approx 68\text{nF} \text{ (Standard Value)}$$

## Design Simulations

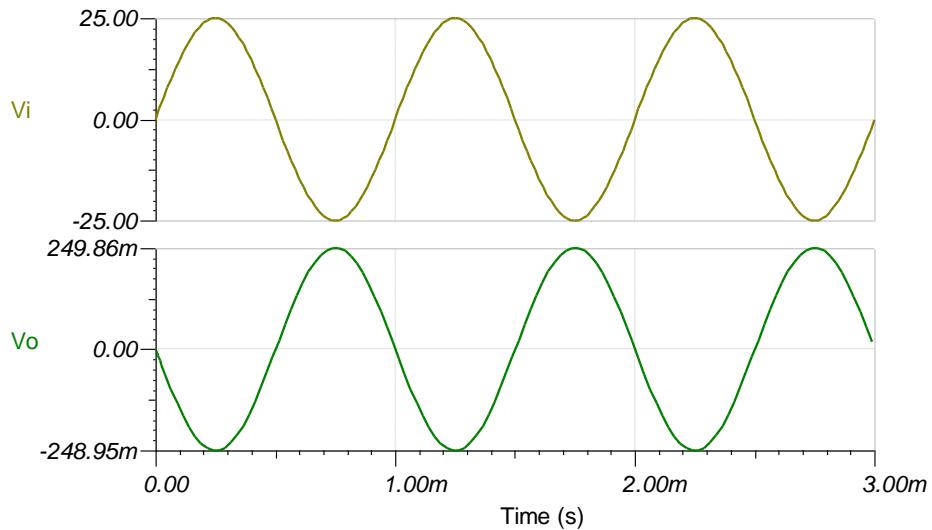
### DC Simulation Results

The amplifier will pass DC voltages applied to the noninverting pin up to the common mode limitations of the op amp ( $\pm 13V$  in this design)

### AC Simulation Results



### Transient Simulation Results



## Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOC503](#).

See TIPD118, [www.ti.com/tool/tipd118](http://www.ti.com/tool/tipd118).

## Design Featured Op Amp

OPA1612	
$V_{ss}$	4.5V to 36V
$V_{inCM}$	$V_{ee}+2V$ to $V_{cc}-2V$
$V_{out}$	$V_{ee}+0.2V$ to $V_{cc}-0.2V$
$V_{os}$	100 $\mu$ V
$I_q$	3.6mA/Ch
$I_b$	60nA
<b>UGBW</b>	40MHz
<b>SR</b>	27V/ $\mu$ s
<b>#Channels</b>	1, 2
<a href="http://www.ti.com/product/opa1612">www.ti.com/product/opa1612</a>	

## Design Alternate Op Amp

OPA172	
$V_{ss}$	4.5V to 36V
$V_{inCM}$	$V_{ee}-100mV$ to $V_{cc}-2V$
$V_{out}$	Rail-to-rail
$V_{os}$	200 $\mu$ V
$I_q$	1.6mA/Ch
$I_b$	8pA
<b>UGBW</b>	10MHz
<b>SR</b>	10V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/opa172">www.ti.com/product/opa172</a>	

## Revision History

Revision	Date	Change
A	January 2019	Downscale the title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page.

## Fast-settling low-pass filter circuit

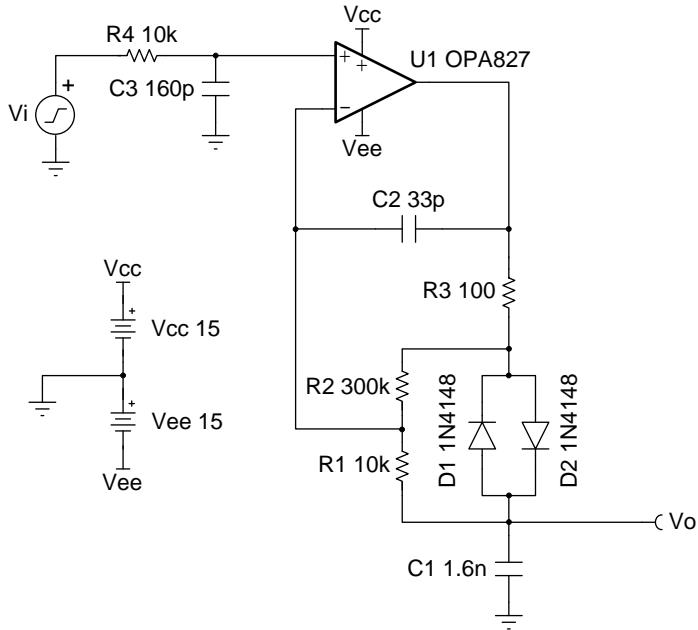
### Design Goals

Input		Output		Supply	
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	$V_{cc}$	$V_{ee}$
-12V	12V	-12V	12V	15V	-15V

Cutoff Frequency ( $f_c$ )	Diode Threshold Voltage ( $V_t$ )
10kHz	20mV

### Design Description

This low-pass filter topology offers a significant improvement in settling time over the conventional single-pole RC filter. This is achieved through the use of diodes  $D_1$  and  $D_2$ , that allow the filter capacitor to charge and discharge much faster when there is a large enough difference between the input and output voltages.



### Design Notes

1. Observe the common-mode input limitations of the op amp.
2. Keeping  $C_1$  small will ensure the op amp does not struggle to drive the capacitive load.
3. For the fastest settling time, use fast switching diodes.
4. The selected op amp should have sufficient output drive capability to charge  $C_1$ .  $R_3$  limits the maximum charge current.

### Design Steps

1. Select standard values for  $R_1$  and  $C_1$  based on  $f_C = 10\text{kHz}$ .

$$R_1 = 10\text{k}\Omega$$

$$C_1 = \frac{1}{2\pi \times f_C \times R_1} = \frac{1}{2\pi \times 10\text{kHz} \times 10\text{k}\Omega} = 1.6\text{nF}$$

2. Set the diode threshold voltage ( $V_t$ ). This threshold is the minimum difference in voltage between the input and output that will result in diode conduction (fast capacitor charging and discharging).

$$V_t = \frac{V_f}{1 + \frac{R_2}{R_1}} \approx \frac{0.6V}{1 + \frac{R_2}{R_1}} = 20\text{mV}$$

$$R_2 = \left( \frac{0.6V}{20\text{mV}} - 1 \right) \times R_1 = 290\text{k}\Omega \approx 300\text{k}\Omega \text{ (standard 5% value)}$$

3. Select components for noise pre-filtering.

$$f_{c2} = 10 \times f_c = 100\text{kHz}$$

$$f_{c2} = \frac{1}{2\pi \times R_4 \times C_3}$$

$$\text{Select } R_4 = R_1 = 10\text{k}\Omega$$

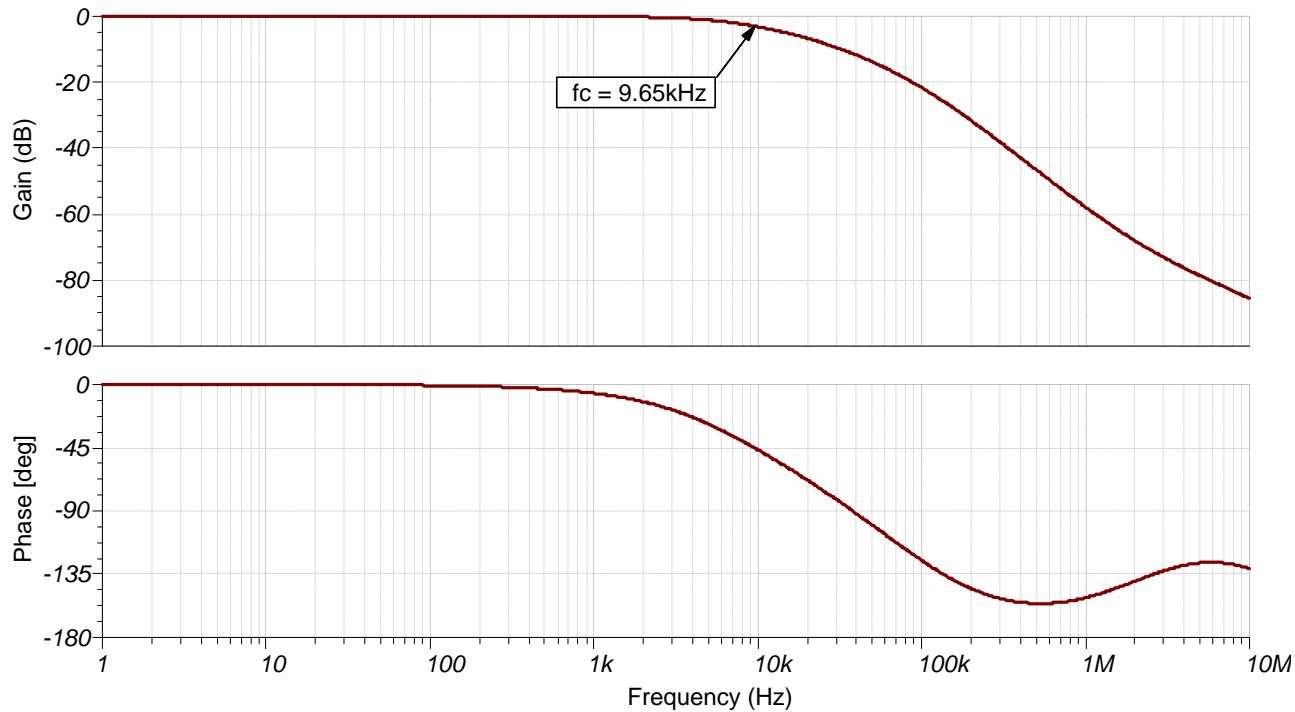
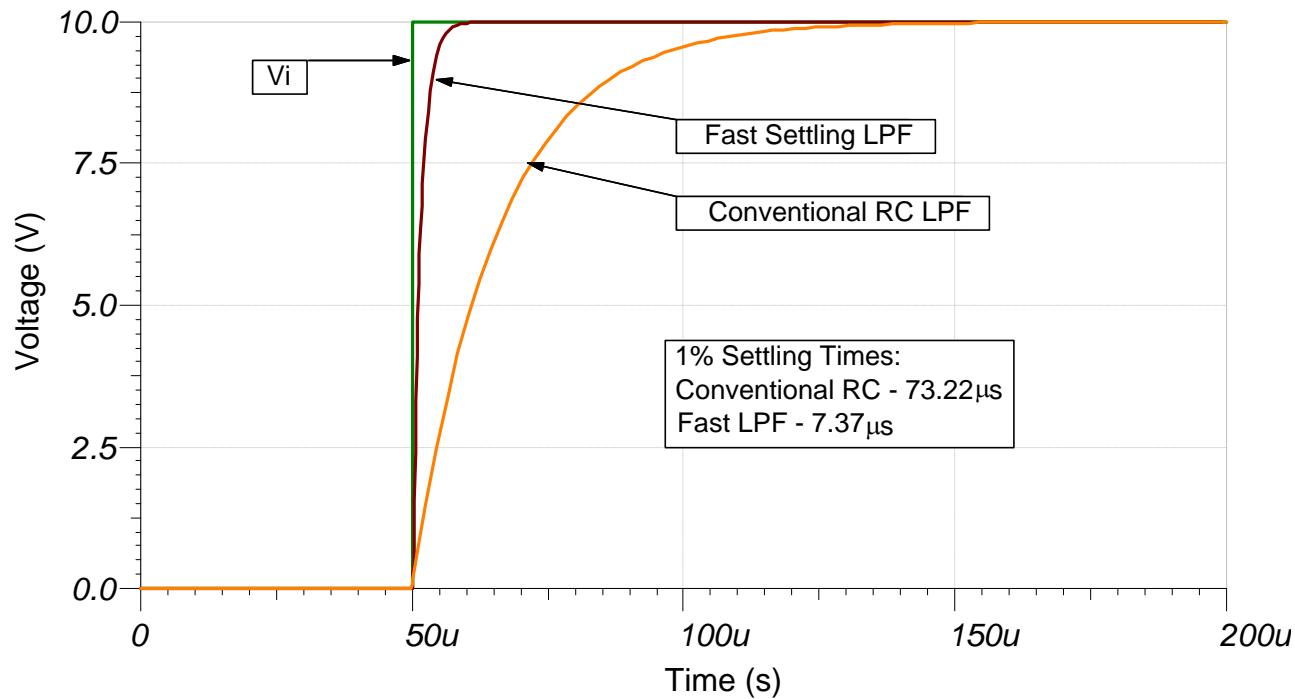
$$C_3 = \frac{C_1}{10} = 160\text{pF}$$

4. Add compensation components to stabilize  $U_1$ .  $R_3$  limits the charge current into  $C_1$  and also serves to isolate the capacitance from the op amp output when the diodes are conducting. Larger values will improve stability but increase  $C_1$  charge time.

$$\text{Select } R_3 = 100\Omega$$

5.  $C_2$  provides local high frequency feedback to counteract the interaction between the input capacitance with the parallel combination of  $R_1$  and  $R_2$ . To prevent interaction with  $C_1$ , select  $C_2$  as the following shows:

$$\text{Select } C_2 = \frac{C_1}{50} = 32\text{pF} \approx 33\text{pF} \text{ (standard value)}$$

**Design Simulations**
**AC Simulation Results**

**Transient Simulation Results**


## Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See TINA-TI™ circuit simulation file, [SBOMAU1](#).

For more information on many op amp topics including common-mode range, output swing, bandwidth, and how to drive an ADC, see [TI Precision Labs](#).

## Design Featured Op Amp

OPA827	
<b>V<sub>ss</sub></b>	8V to 36V
<b>V<sub>inCM</sub></b>	V <sub>ee</sub> +3V to V <sub>cc</sub> -3V
<b>V<sub>out</sub></b>	V <sub>ee</sub> +3V to V <sub>cc</sub> -3V
<b>V<sub>os</sub></b>	75µV
<b>I<sub>q</sub></b>	4.8mA
<b>I<sub>b</sub></b>	3pA
<b>UGBW</b>	22MHz
<b>SR</b>	28V/µs
<b>#Channels</b>	1
<a href="http://www.ti.com/product/opa827">http://www.ti.com/product/opa827</a>	

## Design Alternate Op Amp

TLC072	
<b>V<sub>ss</sub></b>	4.5V to 16V
<b>V<sub>inCM</sub></b>	V <sub>ee</sub> +0.5V to V <sub>cc</sub> -0.8V
<b>V<sub>out</sub></b>	V <sub>ee</sub> +350mV to V <sub>cc</sub> -1V
<b>V<sub>os</sub></b>	390µV
<b>I<sub>q</sub></b>	2.1mA/Ch
<b>I<sub>b</sub></b>	1.5pA
<b>UGBW</b>	10MHz
<b>SR</b>	16V/µs
<b>#Channels</b>	1,2,4
<a href="http://www.ti.com/product/tlc072">http://www.ti.com/product/tlc072</a>	

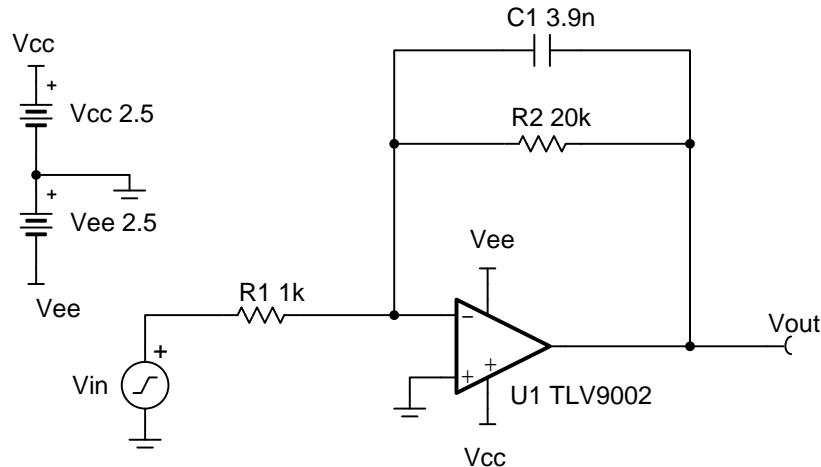
## Low-pass *filtered*, inverting amplifier circuit

### Design Goals

Input		Output		BW	Supply	
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	$f_p$	$V_{ee}$	$V_{cc}$
-0.1V	0.1V	-2V	2V	2kHz	-2.5V	2.5V

### Design Description

This tunable low-pass inverting amplifier circuit amplifies the signal level by 26dB or 20V/V.  $R_2$  and  $C_1$  set the cutoff frequency for this circuit. The frequency response of this circuit is the same as that of a passive RC filter, except that the output is amplified by the pass-band gain of the amplifier. Low-pass filters are often used in audio signal chains and are sometimes called bass-boost filters.



### Design Notes

1.  $C_1$  and  $R_2$  set the low-pass filter cutoff frequency
2. The common-mode voltage is set by the non-inverting input of the op amp, which in this case is mid-supply.
3. Using high value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
4.  $R_2$  and  $R_1$  set the gain of the circuit.
5. The pole frequency  $f_p$  of 2kHz is selected for an audio bass-boost application.
6. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
7. Large signal performance may be limited by slew rate. Therefore, check the maximum output swing versus frequency plot in the data sheet to minimize slew-induced distortion.
8. For more information on op amp linear operation region, stability, slew-induced distortion, capacitive load drive, driving ADCs and bandwidth please see the design references section.

## Design Steps

The DC transfer function of this circuit is given below.

$$V_o = V_i \times \left( -\frac{R_2}{R_1} \right)$$

1. Pick resistor values for given passband gain.

$$\text{Gain} = \frac{R_2}{R_1} = 20 \frac{V}{V} \text{ (26 dB)}$$

$$R_1 = 1 \text{ k}\Omega$$

$$R_2 = \text{Gain} \times (R_1) = 20 \frac{V}{V} \times 1 \text{ k}\Omega = 20 \text{ k}\Omega$$

2. Select low-pass filter pole frequency  $f_p$

$$f_p = 2 \text{ kHz}$$

3. Calculate  $C_1$  using  $R_2$  to set the location of  $f_p$ .

$$f_p = \frac{1}{2\pi \times R_2 \times C_1} = 2 \text{ kHz}$$

$$C_1 = \frac{1}{2\pi \times R_2 \times f_p} = \frac{1}{2\pi \times 20 \text{ k}\Omega \times 2 \text{ kHz}} = 3.98 \text{nF} \approx 3.9 \text{nF} \text{ (Standard Value)}$$

4. Calculate the minimum slew rate required to minimize slew-induced distortion.

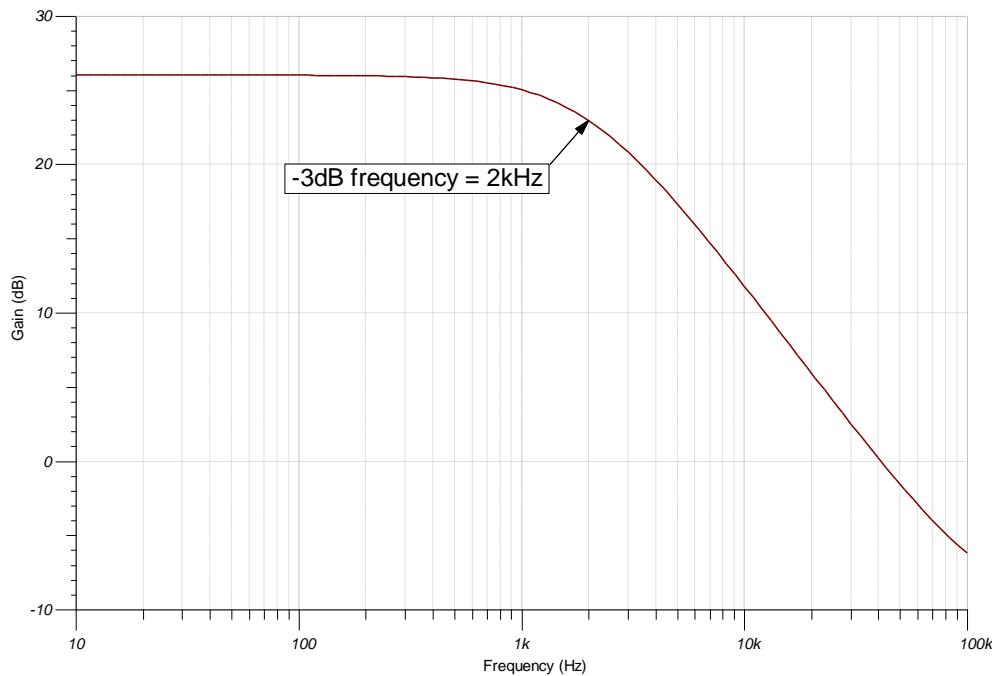
$$V_p = \frac{SR}{2 \times \pi \times f} \rightarrow SR > 2 \times \pi \times f \times V_p$$

$$SR > 2 \times \pi \times 2 \text{ kHz} \times 2 \text{ V} = 0.25 \frac{\text{V}}{\mu\text{s}}$$

5.  $SR_{TLV9002} = 2 \text{ V}/\mu\text{s}$ , therefore it meets this requirement

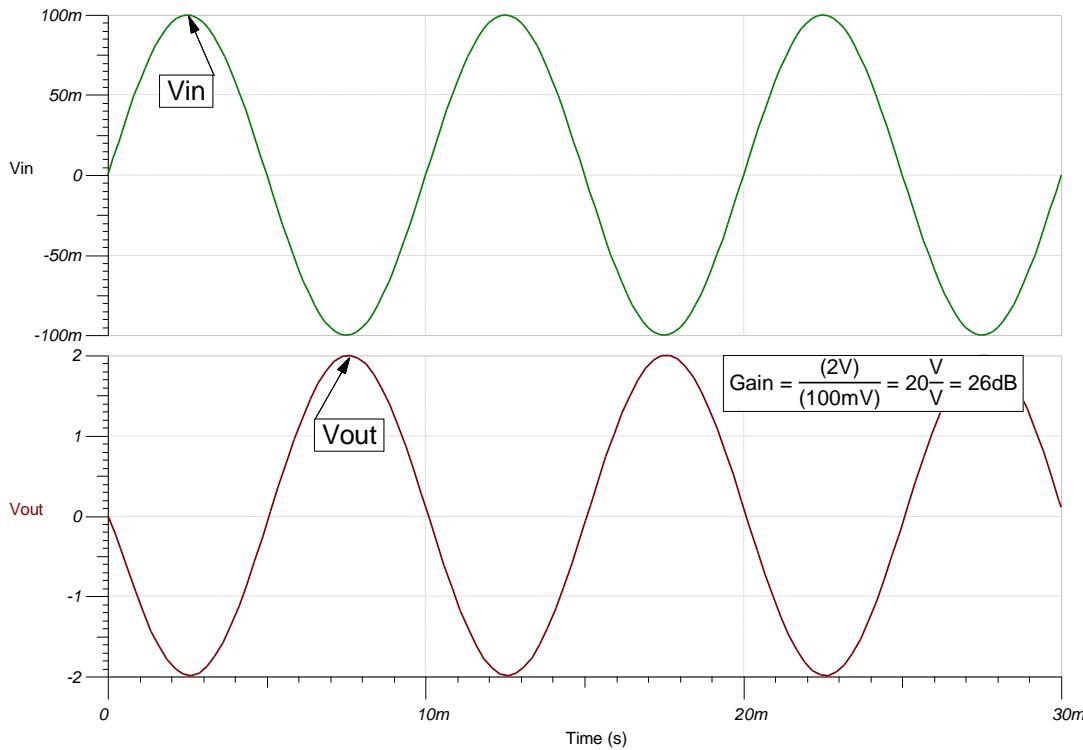
## Design Simulations

### AC Simulation Results

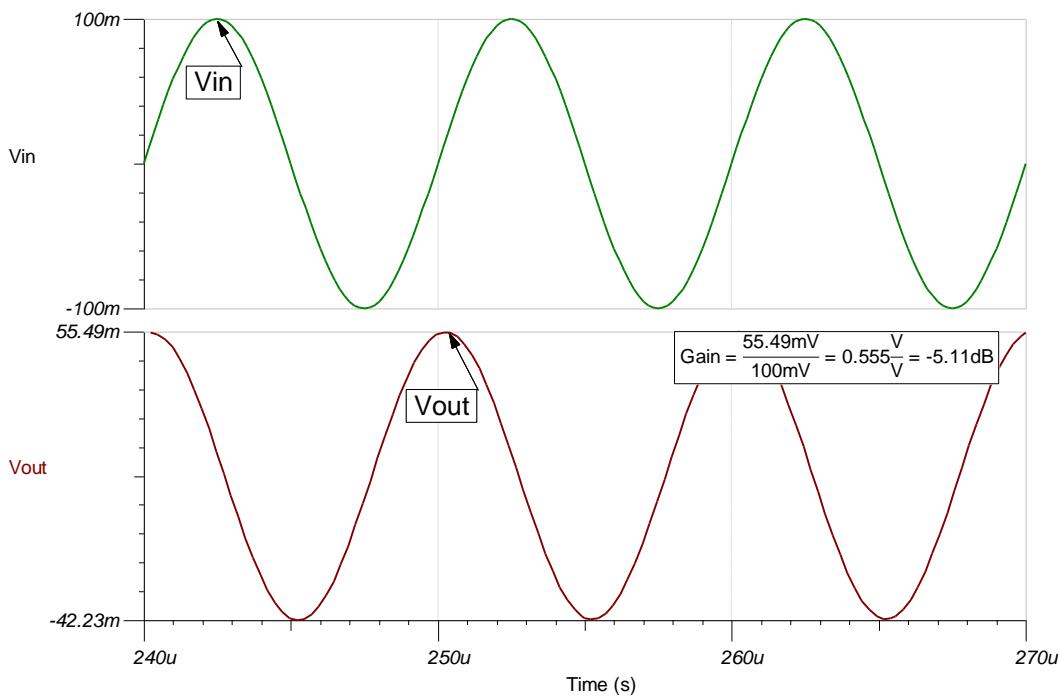


### Transient Simulation Results

A 100 Hz, 0.2 V<sub>pp</sub> sine wave yields a 4 V<sub>pp</sub> output sine wave.



A 100 kHz, 0.2 V<sub>pp</sub> sine wave yields a 0.1 V<sub>pp</sub> output sine wave.



**References:**

1. [Analog Engineer's Circuit Cookbooks](#)
2. [SPICE Simulation File SBOC523](#)
3. [TI Precision Designs TIPD185](#)
4. [TI Precision Labs](#)

**Design Featured Op Amp**

TLV9002	
$V_{ss}$	1.8V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	0.4mV
$I_q$	60 $\mu$ A
$I_b$	5pA
<b>UGBW</b>	1MHz
<b>SR</b>	2V/ $\mu$ s
<b>#Channels</b>	1,2,4
<a href="http://www.ti.com/product/tlv9002">www.ti.com/product/tlv9002</a>	

**Design Alternate Op Amp**

OPA375	
$V_{ss}$	2.25V to 5.5V
$V_{inCM}$	$V_{ee}$ to $V_{cc}$ -1.2V
$V_{out}$	Rail-to-rail
$V_{os}$	0.15mV
$I_q$	890 $\mu$ A
$I_b$	10pA
<b>UGBW</b>	10MHz
<b>SR</b>	4.75V/ $\mu$ s
<b>#Channels</b>	1
<a href="http://www.ti.com/product/opa375">www.ti.com/product/opa375</a>	

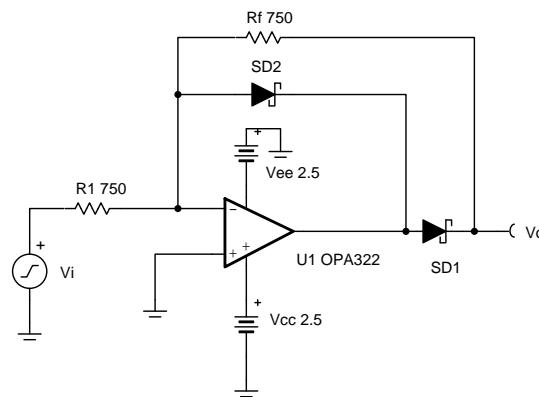
## Half-wave rectifier circuit

### Design Goals

Input		Output		Supply	
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	$V_{cc}$	$V_{ee}$
$\pm 0.2\text{mV}_{\text{pp}}$	$\pm 4\text{V}_{\text{pp}}$	$0.1V_p$	$2V_p$	2.5V	-2.5V

### Design Description

The precision half-wave rectifier inverts and transfers only the negative-half input of a time varying input signal (preferably sinusoidal) to its output. By appropriately selecting the feedback resistor values, different gains can be achieved. Precision half-wave rectifiers are commonly used with other op amp circuits such as a peak-detector or bandwidth limited non-inverting amplifier to produce a DC output voltage. This configuration has been designed to work for sinusoidal input signals between  $0.2\text{mV}_{\text{pp}}$  and  $4\text{V}_{\text{pp}}$  at frequencies up to 50kHz.



### Design Notes

1. Select an op amp with a high slew rate. When the input signal changes polarities, the amplifier output must slew two diode voltage drops.
2. Set output range based on linear output swing (see  $A_{ol}$  specification).
3. Use fast switching diodes. High-frequency input signals will be distorted depending on the speed by which the diodes can transition from blocking to forward conducting mode. Schottky diodes might be a preferable choice, since these have faster transitions than pn-junction diodes at the expense of higher reverse leakage.
4. The resistor tolerance sets the circuit gain error.
5. Minimize noise errors by selecting low-value resistors.

## Design Steps

1. Set the desired gain of the half-wave rectifier to select the feedback resistors.

$$V_o = \text{Gain} \times V_i$$

$$\text{Gain} = -\frac{R_f}{R_1} = -1$$

$$R_f = R_1 = 2 \times R_{eq}$$

- Where  $R_{eq}$  is the parallel combination of  $R_1$  and  $R_f$

2. Select the resistors such that the resistor noise is negligible compared to the voltage broadband noise of the op amp.

$$E_{nr} = \sqrt{4 \times k_b \times T \times R_{eq}}$$

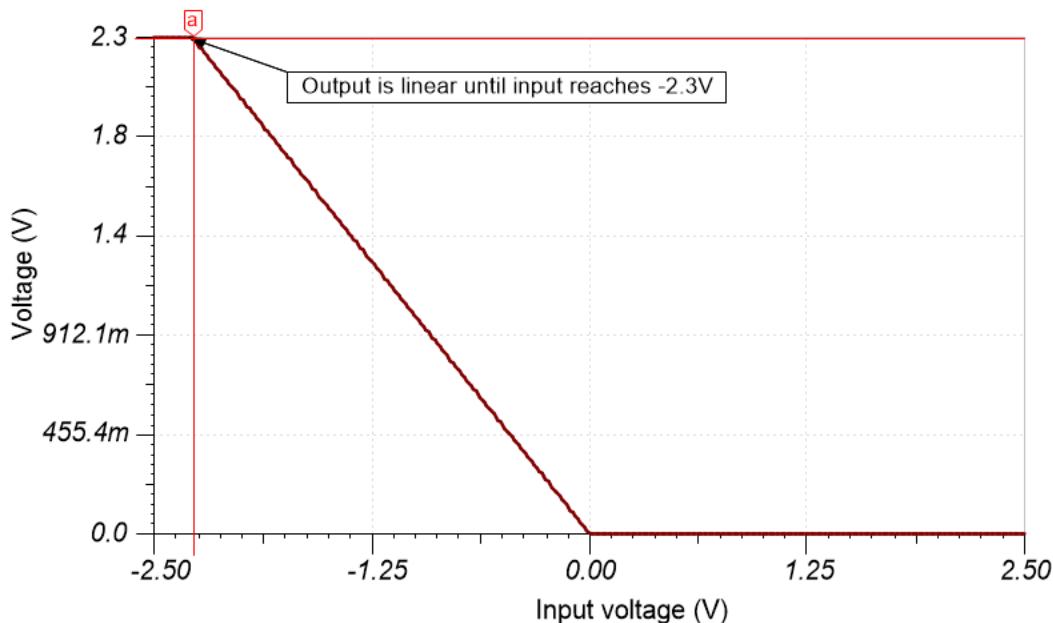
$$R_{eq} \leq \frac{E_{nbb}^2}{4 \times k_b \times T \times 3^2} = (E_{nbb})$$

$$= 7.5 \frac{nV}{\sqrt{Hz}} = \frac{(7.5 \times 10^{-9})^2}{4 \times 1.381 \times 10^{-23} \times 298 \times 3^2} = 380\Omega$$

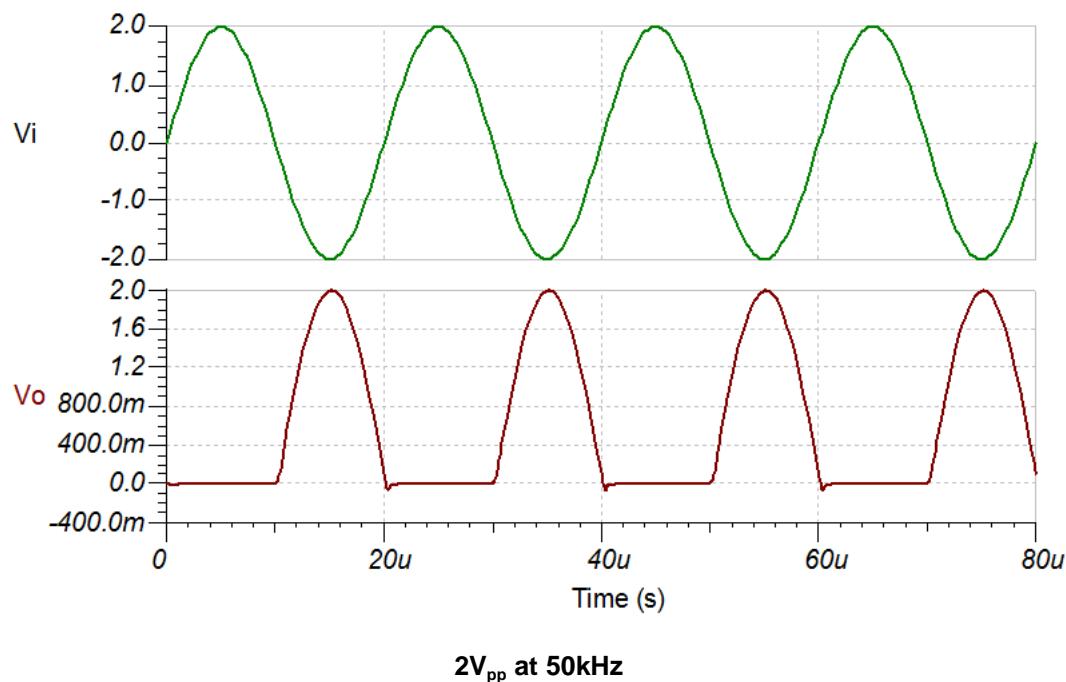
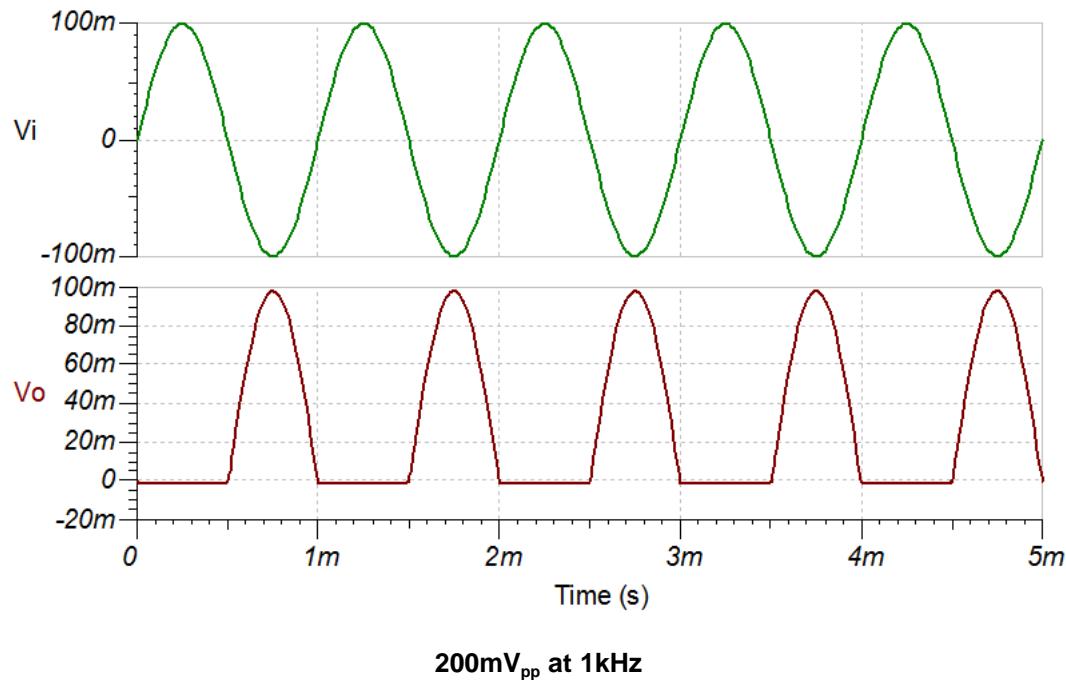
$$R_f = R_1 \leq 760\Omega \rightarrow 750\Omega \text{ (Standard Value)}$$

## Design Simulations

### DC Simulation Results



### Transient Simulation Results



## Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOC509](#).

## Design Featured Op Amp

OPA322	
$V_{ss}$	1.8V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	500 $\mu$ V
$I_q$	1.6mA/Ch
$I_b$	0.2pA
<b>UGBW</b>	20MHz
<b>SR</b>	10V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/opa322">www.ti.com/product/opa322</a>	

## Design Alternate Op Amp

OPA2325	
$V_{ss}$	2.2V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	40 $\mu$ V
$I_q$	0.65mA/Ch
$I_b$	0.2pA
<b>UGBW</b>	10MHz
<b>SR</b>	5V/ $\mu$ s
<b>#Channels</b>	2 $\mu$
<a href="http://www.ti.com/product/opa2325">www.ti.com/product/opa2325</a>	

## Revision History

Revision	Date	Change
A	January 2019	Downscale the title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page and link to Spice simulation file.

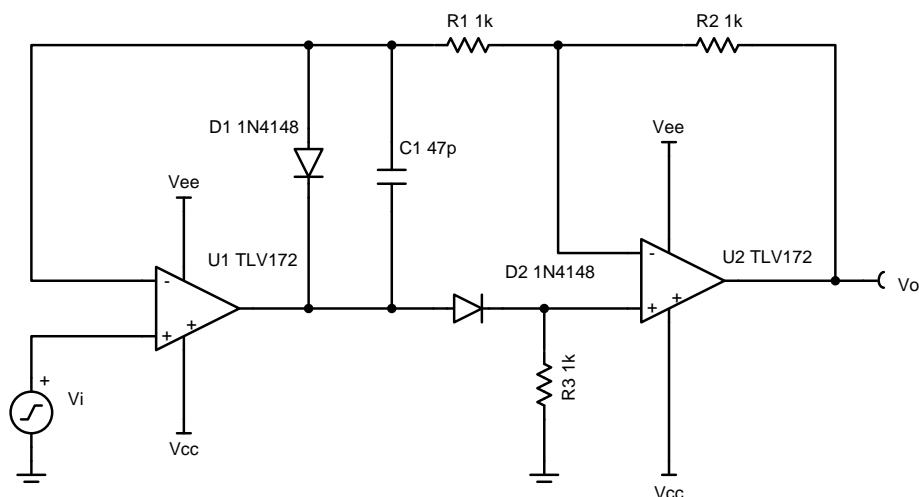
## Full-wave rectifier circuit

### Design Goals

Input		Output		Supply		
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	$V_{cc}$	$V_{ee}$	$V_{ref}$
$\pm 25\text{mV}$	$\pm 10\text{V}$	25mV	10V	15V	-15V	0V

### Design Description

This absolute value circuit can turn alternating current (AC) signals to single polarity signals. This circuit functions with limited distortion for  $\pm 10\text{-V}$  input signals at frequencies up to 50kHz and for signals as small as  $\pm 25\text{mV}$  at frequencies up to 1kHz.



### Design Notes

1. Be sure to select an op amp with sufficient bandwidth and a high slew rate.
2. For greater precision look for an op amp with low offset voltage, low noise, and low total harmonic distortion (THD).
3. The resistors were selected to be 0.1% tolerance to reduce gain error.
4. Selecting too large of a capacitor  $C_1$  will cause large distortion on the transition edges when the input signal changes polarity.  $C_1$  may not be required for all op amps.
5. Use a fast switching diode.

### Design Steps

1. Select gain resistors.

- a. Gain for positive input signals.

$$\frac{V_o}{V_i} = 1 \frac{V}{V}$$

- b. Gain for negative input signals.

$$\frac{V_o}{V_i} = - \frac{R_2}{R_1} = - 1 \frac{V}{V}$$

2. Select  $R_1$  and  $R_2$  to reduce thermal noise and to minimize voltage drops due to the reverse leakage current of the diode. These resistors will appear as loads to  $U_1$  and  $U_2$  during negative input signals.

$$R_1 = R_2 = 1 \text{ k}\Omega$$

3.  $R_3$  biases the non-inverting node of  $U_2$  to GND during negative input signals. Select  $R_3$  to be the same value as  $R_1$  and  $R_2$ .  $U_1$  must be able to drive the  $R_3$  load during positive input signals.

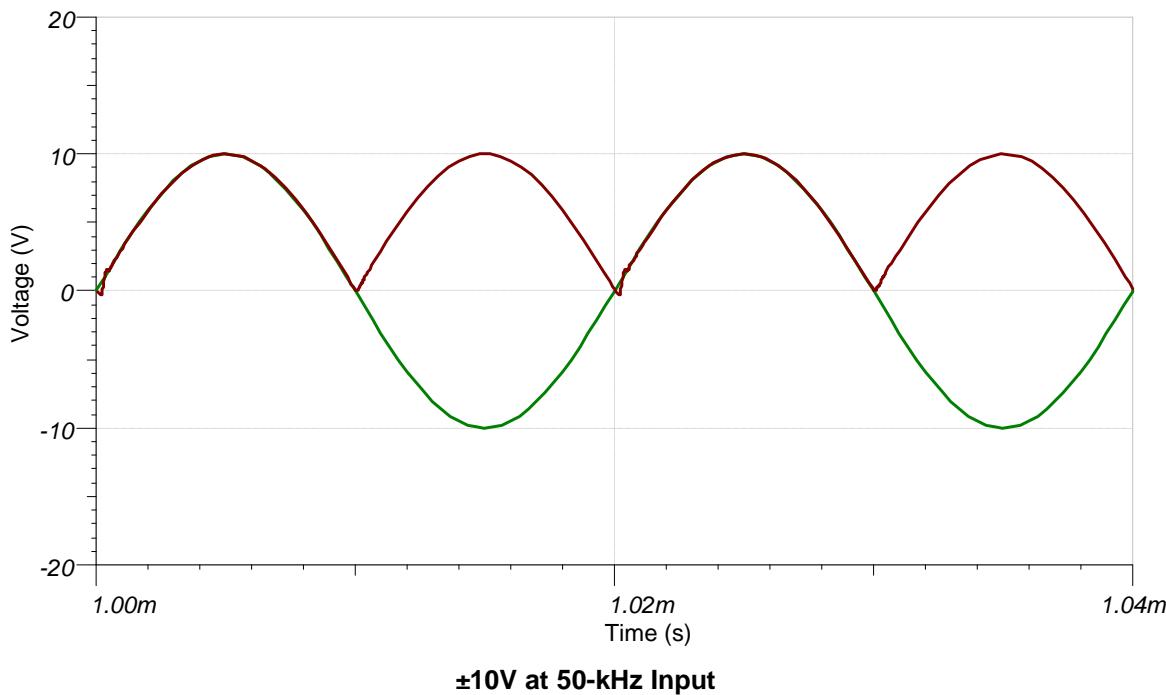
$$R_3 = 1 \text{ k}\Omega$$

4. Select  $C_1$  based on the desired transient response. See the Design Reference section for more information.

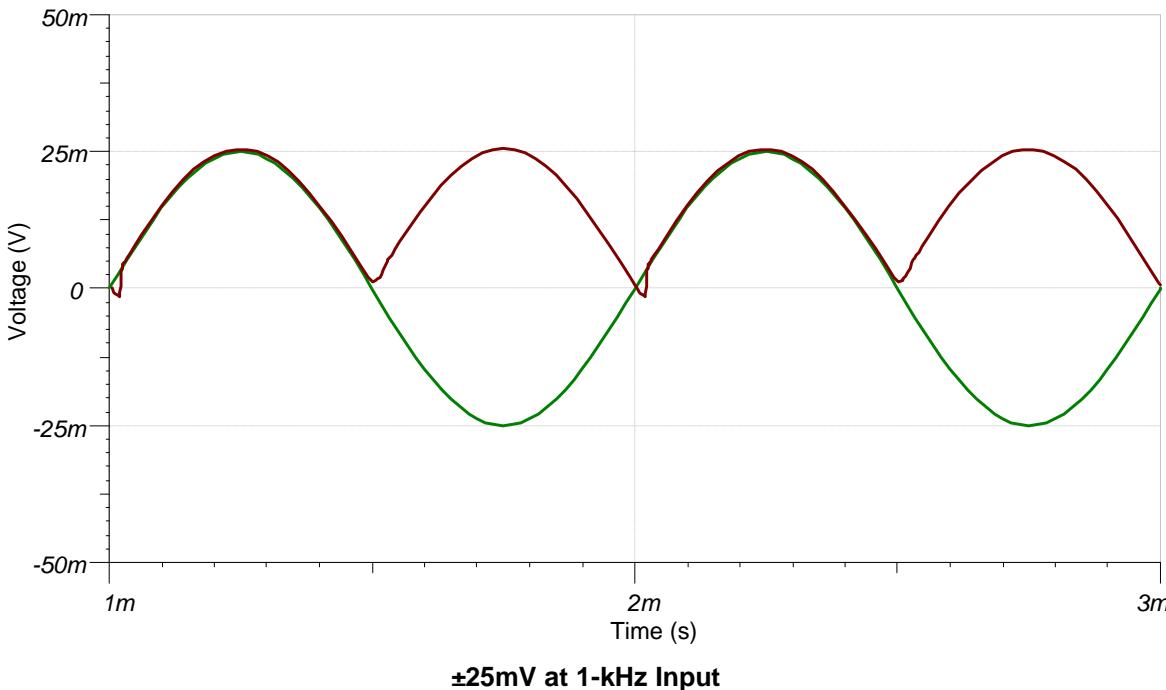
$$C_1 = 47\text{pF}$$

## Design Simulations

### Transient Simulation Results



$\pm 10V$  at 50-kHz Input



$\pm 25mV$  at 1-kHz Input

## Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOC517](#).

See TIPD139, [www.ti.com/tool/tipd139](http://www.ti.com/tool/tipd139).

## Design Featured Op Amp

TLV172	
$V_{cc}$	4.5V to 36V
$V_{inCM}$	Vee to ( $V_{cc}$ –2V)
$V_{out}$	Rail-to-rail
$V_{os}$	0.5mV
$I_q$	1.6mA/Ch
$I_b$	10pA
<b>UGBW</b>	10MHz
<b>SR</b>	10V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/tlv172">www.ti.com/product/tlv172</a>	

## Design Alternate Op Amp

OPA197	
$V_{cc}$	4.5V to 36V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	25 $\mu$ V
$I_q$	1mA/Ch
$I_b$	5pA
<b>UGBW</b>	10MHz
<b>SR</b>	20V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/opa197">www.ti.com/product/opa197</a>	

## Revision History

Revision	Date	Change
A	January 2019	Downscale the title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page and Spice simulation file.

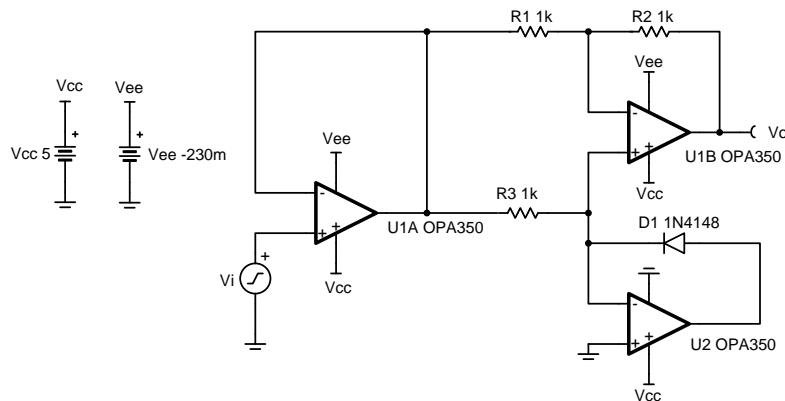
## **Single-supply, low-input voltage, full-wave rectifier circuit**

### **Design Goals**

<b>Input</b>		<b>Output</b>		<b>Supply</b>		
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	$V_{cc}$	$V_{ee}$	$V_{ref}$
5mVpp	400mVpp	2.5mVpp	200mVpp	5V	-0.23V	0V

### **Design Description**

This single-supply precision absolute value circuit is optimized for low-input voltages. It is designed to function up to 50kHz and has excellent linearity at signal levels as low as 5mVpp. The design uses a negative charge pump (such as LM7705) on the negative op amp supply rails to maintain linearity with signal levels near 0V.

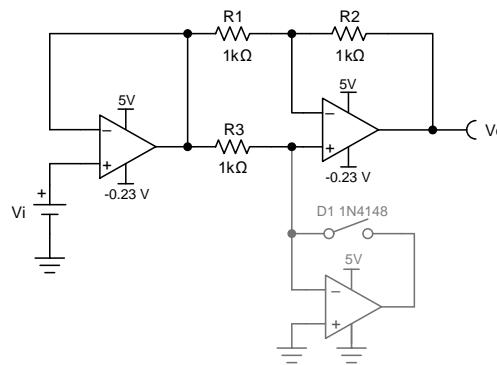


### **Design Notes**

1. Observe common-mode and output swing limitations of op amps.
2.  $R_3$  should be sized small enough that the leakage current from  $D_1$  does not cause errors in positive input cycles while ensuring the op amp can drive the load.
3. Use a fast switching diode for  $D_1$ .
4. Removing the input buffer will allow for input signals with peak-to-peak values twice as large as the supply voltage at the expense of lower input impedance and slight gain error.
5. Use precision resistors to minimize gain error.

### Design Steps

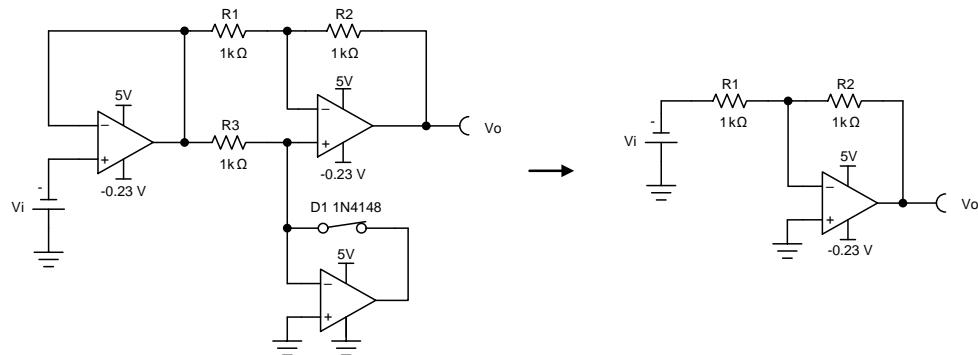
1. Circuit analysis for positive input signals.



$$\frac{V_o}{V_i} = \left( -\frac{R_2}{R_1} \right) + \left( 1 + \frac{R_2}{R_1} \right) = 1$$

$$V_o = V_i$$

2. Circuit analysis for negative input signals.



$$\frac{V_o}{V_i} = \left( -\frac{R_2}{R_1} \right) = -1$$

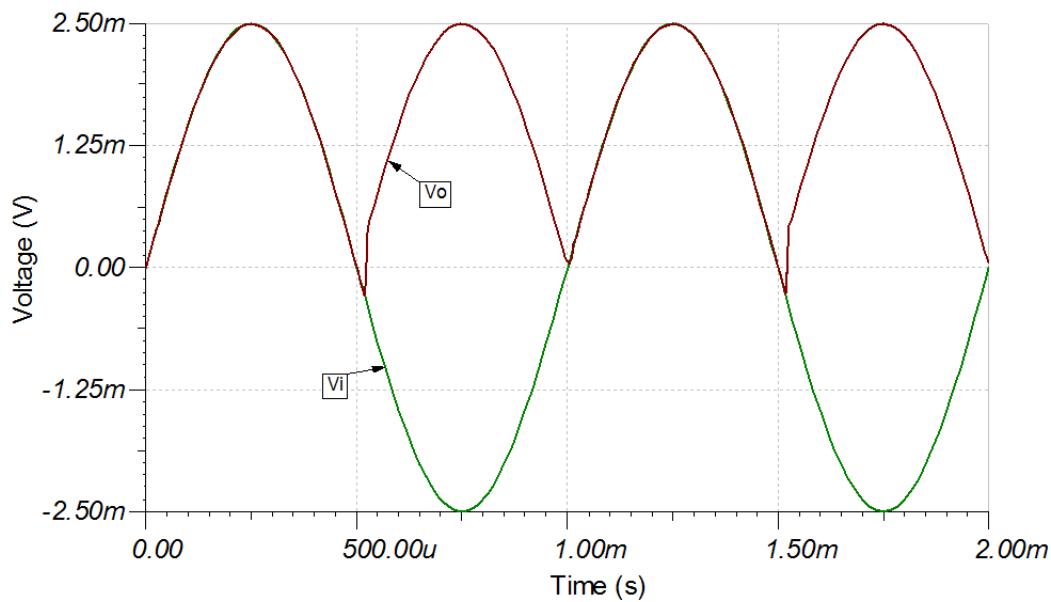
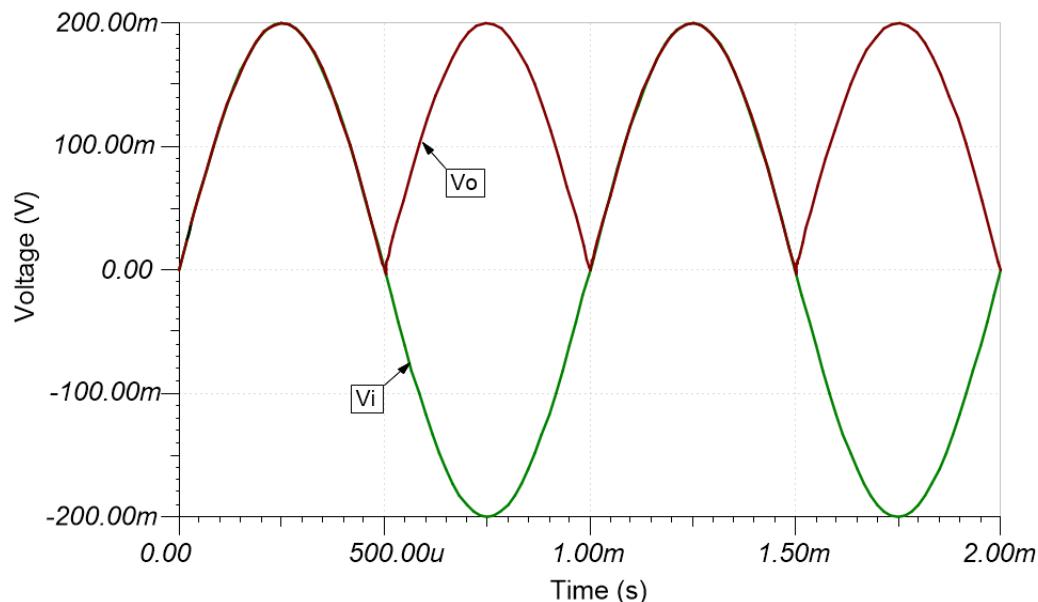
$$V_o = -V_i$$

3. Select  $R_1$ ,  $R_2$ , and  $R_3$ .

$$\frac{V_o}{V_i} = -\frac{R_2}{R_1}$$

If  $R_2 = R_1$  then  $V_o = -V_i$

Set  $R_1 = R_2 = R_3 = 1\text{ k}\Omega$

**Design Simulations**
**Transient Simulation Results**

**5mVpp at 1-kHz Input**

**400mVpp at 1-kHz Input**

## Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOC506](#).

See TIPD124, [www.ti.com/tool/tipd124](http://www.ti.com/tool/tipd124).

## Design Featured Op Amp

OPA350	
$V_{ss}$	2.7V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	150 $\mu$ V
$I_q$	5.2mA/Ch
$I_b$	0.5pA
<b>UGBW</b>	38MHz
<b>SR</b>	22V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/opa350">www.ti.com/product/opa350</a>	

## Design Alternate Op Amp

OPA353	
$V_{ss}$	2.7V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	3mV
$I_q$	5.2mA
$I_b$	0.5pA
<b>UGBW</b>	44MHz
<b>SR</b>	22V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/opa353">www.ti.com/product/opa353</a>	

## Revision History

Revision	Date	Change
A	January 2019	Downscale the title and changed title role to 'Amplifiers'. Added links to circuit cookbook landing page and SPICE simulation file.

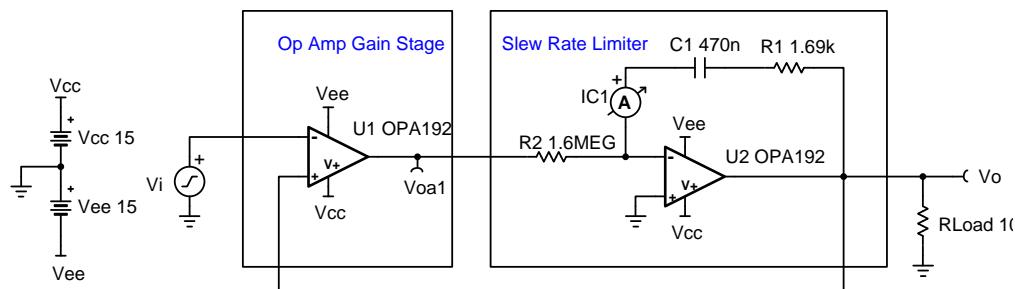
## Slew rate limiter circuit

### Design Goals

Input		Output		Supply		
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	$V_{cc}$	$V_{ee}$	$V_{ref}$
-10V	10V	-10V	10V	15V	-15V	0V

### Design Description

This circuit controls the slew rate of an analog gain stage. This circuit is intended for symmetrical slew rate applications. The desired slew rate must be slower than that of the op amp chosen to implement the slew rate limiter.



### Design Notes

1. The gain stage op-amp and slew rate limiting op amp should both be checked for stability.
2. Verify that the current demands for charging or discharging  $C_1$  plus any load current out of  $U_2$  will not limit the voltage swing of  $U_2$ .

### Design Steps

1. Set slew rate and choose a standard value for the feedback capacitor,  $C_1$ .  
 $C_1 = 470\text{nF}$   
 $SR = 20\frac{\text{V}}{\text{s}}$
2. Choose the value of  $R_2$  to set the capacitor current necessary for the desired slew rate.

$$SR = \frac{I_{C_1}}{C_1}$$

$$20\frac{\text{V}}{\text{s}} = \frac{I_{C_1}}{470\text{nF}} \text{ where } I_{C_1} = 9.4 \mu\text{A}$$

Gain stage op amp  $V_{\text{sat}} = \pm 14.995$  (typical)

$$I_{C_1} = \frac{V_{\text{sat}}}{R_2}$$

$$9.4 \mu\text{A} = \frac{14.995\text{V}}{R_2}, \text{ so } R_2 = 1.595 \text{ M}\Omega \approx 1.6 \text{ M}\Omega \text{ (Standard Value)}$$

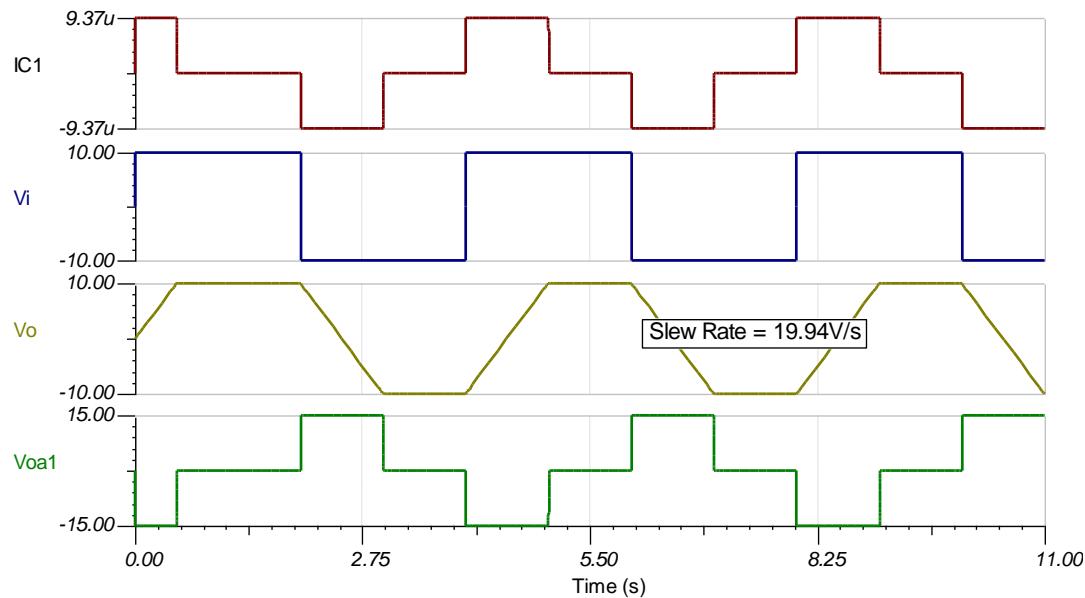
3. Compensate feedback network for stability.  $R_1$  adds a pole to the  $1/\beta$  network. This pole should be placed so that the  $1/\beta$  curve levels off a decade before it intersects the open loop gain curve (200Hz, for this example).

$$f_p = \frac{1}{2\pi \times R_1 \times C_1} = 200\text{Hz}$$

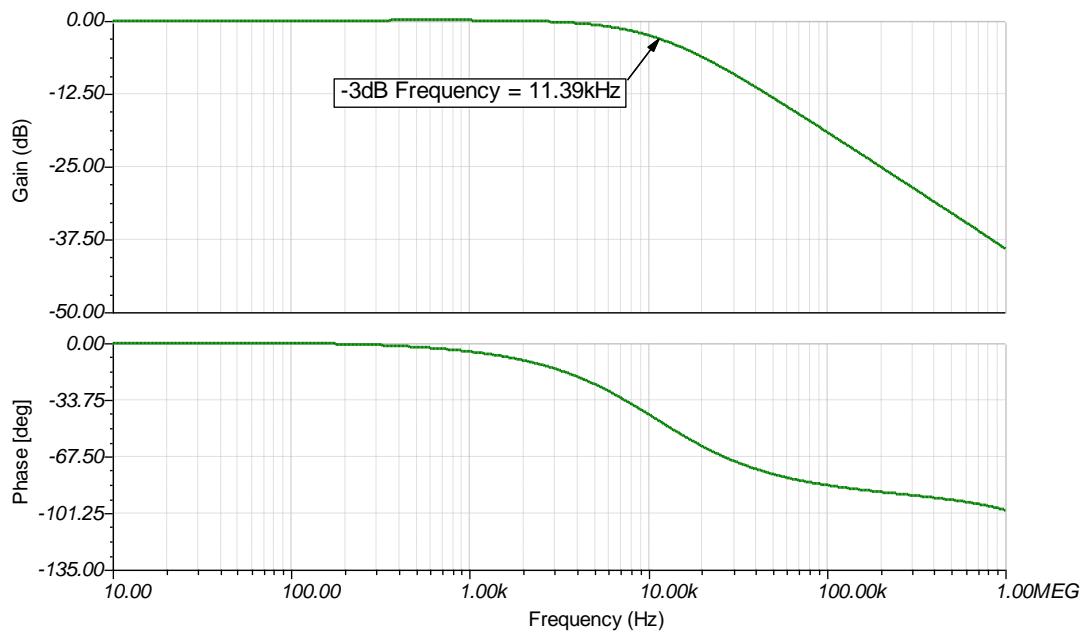
$$200\text{Hz} = \frac{1}{2\pi \times R_1 \times 470\text{nF}}, \text{ so } R_1 = 1.693 \text{ k}\Omega \approx 1.69 \text{ k}\Omega \text{ (Standard Value)}$$

## Design Simulations

### Transient Simulation Results



### AC Simulation Results



## Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See the circuit SPICE simulation file [SBOC508](#).

See TIPD140, [www.ti.com/tool/tipd140](http://www.ti.com/tool/tipd140).

## Design Featured Op Amp

OPA192	
$V_{cc}$	4.5V to 36V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	5 $\mu$ V
$I_q$	1mA/Ch
$I_b$	5pA
UGBW	10MHz
SR	20V/ $\mu$ s
#Channels	1, 2, 4
<a href="http://www.ti.com/product/opa192">www.ti.com/product/opa192</a>	

## Design Alternate Op Amp

TLV2372	
$V_{cc}$	2.7V to 16V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	2mV
$I_q$	750 $\mu$ A/Ch
$I_b$	1pA
UGBW	3MHz
SR	2.1V/ $\mu$ s
#Channels	1, 2, 4
<a href="http://www.ti.com/product/tlv2372">www.ti.com/product/tlv2372</a>	

## Revision History

Revision	Date	Change
A	February 2019	Downscale the title and changed title role to 'Amplifiers'. Added links to circuit cookbook landing page and SPICE simulation file.

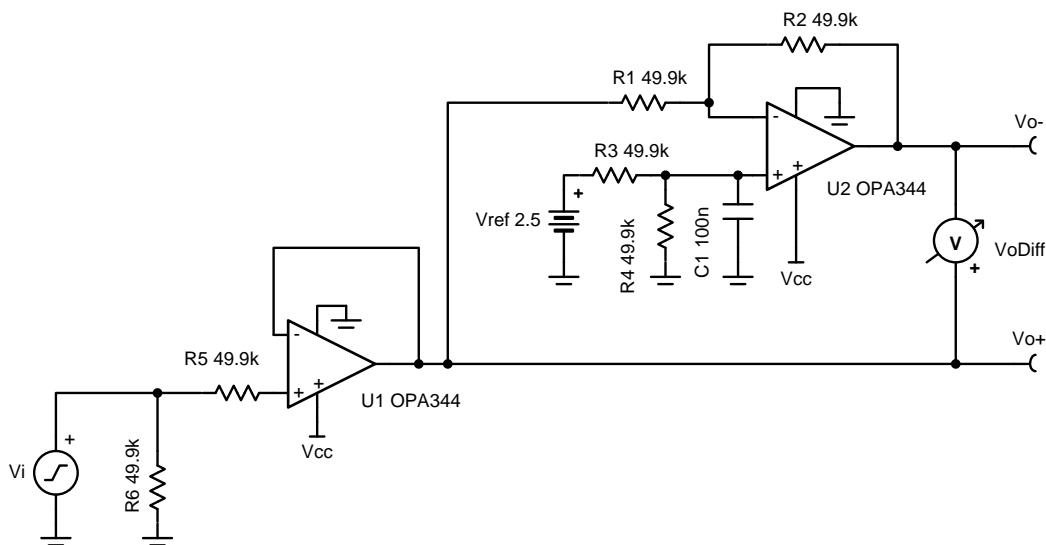
## ***Single-ended input to differential output circuit***

### **Design Goals**

Input		Output		Supply		
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{DiffMin}}$	$V_{o\text{DiffMax}}$	$V_{cc}$	$V_{ee}$	$V_{ref}$
0.1V	2.4V	-2.3V	2.3V	2.7V	0V	2.5V

### **Design Description**

This circuit converts a single ended input of 0.1V to 2.4V into a differential output of  $\pm 2.3V$  on a single 2.7-V supply. The input and output ranges can be scaled as necessary as long as the op amp input common-mode range and output swing limits are met.



### **Design Notes**

1. Op amps with rail-to-rail input and output will maximize the input and output range of the circuit.
2. Op amps with low  $V_{os}$  and offset drift will reduce DC errors.
3. Use low tolerance resistors to minimize gain error.
4. Set output range based on linear output swing (see  $A_{ol}$  specification).
5. Keep feedback resistors low or add capacitor in parallel with  $R_2$  for stability.

### Design Steps

1. Buffer  $V_i$  signal to generate  $V_{o+}$ .

$$V_{o+} = V_i$$

2. Invert and level shift  $V_{o+}$  using a difference amplifier to create  $V_{o-}$ .

$$V_{o-} = (V_{ref} - V_{o+}) \times \left(\frac{R_2}{R_1}\right)$$

3. Select resistances so that the resistor noise is smaller than the amplifier broadband noise.

$$E_{nv} = 30 \frac{nV}{\sqrt{Hz}} \text{ (Voltage noise from op amp)}$$

If  $R_1 = R_2 = R_3 = R_4 = 49.9k\Omega$  then

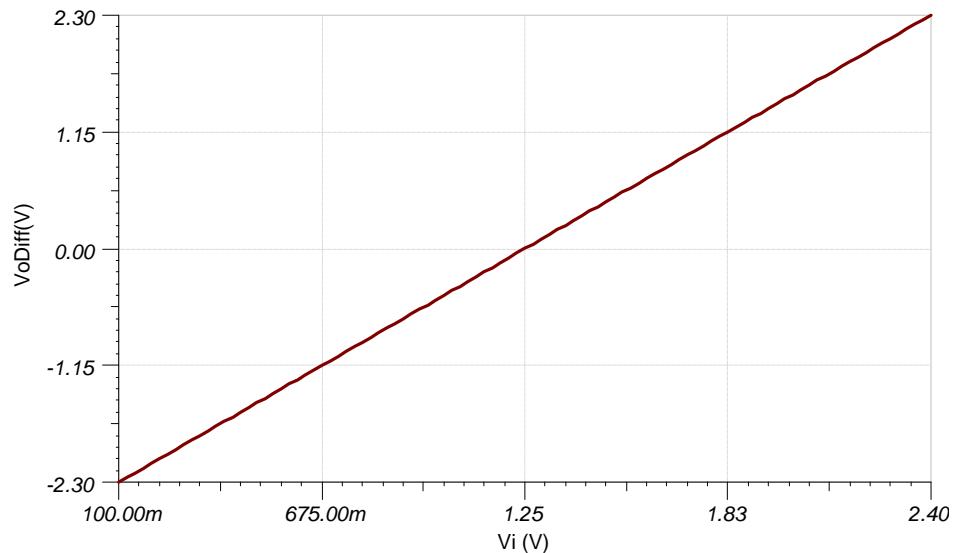
$$E_{nr} = \sqrt{(\sqrt{4 \times kB \times T \times (R_1|R_2)})^2 + (\sqrt{4 \times kB \times T \times (R_3|R_4)})^2} = 28.7 \frac{nV}{\sqrt{Hz}} (< E_{nv})$$

4. Select resistances that protect the input of the amplifier and prevents floating inputs. To simplify the bill of materials (BOM), select  $R_5 = R_6$ .

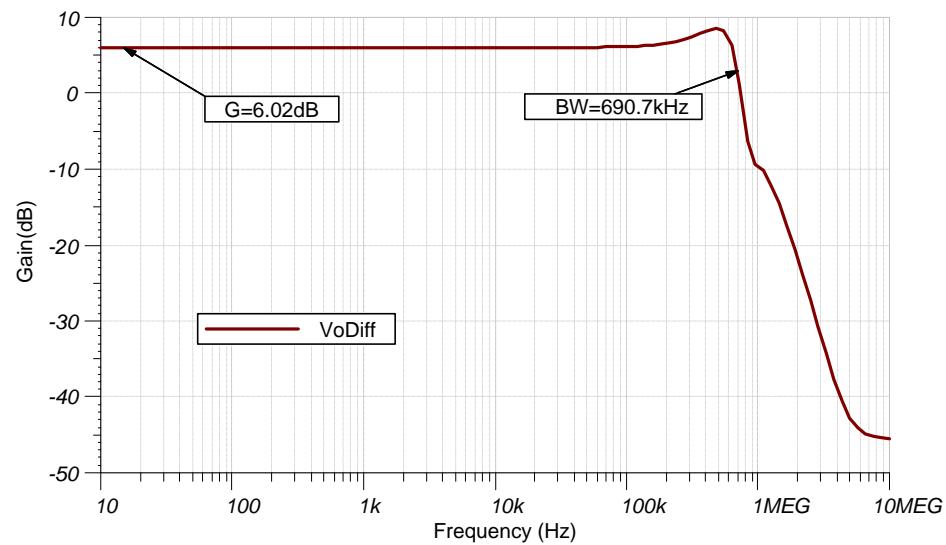
$$R_5 = R_6 = 49.9k\Omega$$

## Design Simulations

### DC Simulation Results



### AC Simulation Results



## Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See the circuit SPICE simulation file [SBOC510](#).

See TIPD131, [www.ti.com/tool/tipd131](http://www.ti.com/tool/tipd131).

## Design Featured Op Amp

OPA344	
$V_{ss}$	1.8V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	0.2mV
$I_q$	150 $\mu$ A
$I_b$	0.2pA
<b>UGBW</b>	1MHz
<b>SR</b>	0.8V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/opa344">www.ti.com/product/opa344</a>	

## Design Alternate Op Amp

OPA335	
$V_{ss}$	2.7V to 5.5V
$V_{inCM}$	$V_{ee}$ -0.1V to $V_{cc}$ -1.5V
$V_{out}$	Rail-to-rail
$V_{os}$	1 $\mu$ V
$I_q$	285 $\mu$ A/Ch
$I_b$	70pA
<b>UGBW</b>	2MHz
<b>SR</b>	1.6V/ $\mu$ s
<b>#Channels</b>	1, 2
<a href="http://www.ti.com/product/opa335">www.ti.com/product/opa335</a>	

## Revision History

Revision	Date	Change
A	February 2019	Downscale the title and changed title role to 'Amplifiers'. Added links to circuit cookbook landing page and SPICE simulation file.

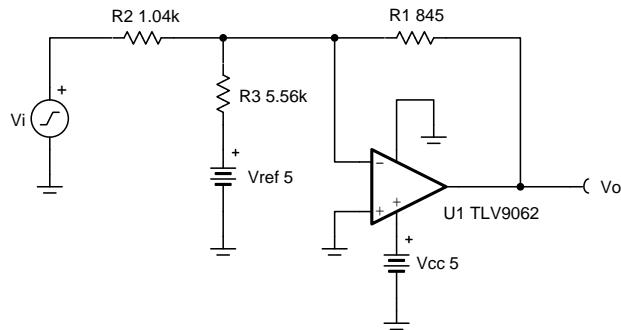
## ***Inverting op amp with inverting positive reference voltage circuit***

### **Design Goals**

<b>Input</b>		<b>Output</b>		<b>Supply</b>		
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	$V_{cc}$	$V_{ee}$	$V_{ref}$
-5V	-1V	0.05V	3.3V	5V	0V	5V

### **Design Description**

This design uses an inverting amplifier with an inverting positive reference to translate an input signal of -5V to -1V to an output voltage of 3.3V to 0.05V. This circuit can be used to translate a negative sensor output voltage to a usable ADC input voltage range.



### **Design Notes**

1. Use op amp linear output operating range. Usually specified under  $A_{OL}$  test conditions.
2. Common mode range must extend down to or below ground.
3.  $V_{ref}$  output must be low impedance.
4. Input impedance of the circuit is equal to  $R_2$ .
5. Choose low-value resistors to use in the feedback. It is recommended to use resistor values less than 100kΩ. Using high-value resistors can degrade the phase margin of the amplifier and introduce additional noise in the circuit.
6. The cutoff frequency of the circuit is dependent on the gain bandwidth product (GBP) of the amplifier. Additional filtering can be accomplished by adding a capacitor in parallel to  $R_1$ . Adding a capacitor in parallel with  $R_1$  will also improve stability of the circuit if high-value resistors are used.

### Design Steps

$$V_o = -V_i \times \left( \frac{R_1}{R_2} \right) - V_{ref} \times \left( \frac{R_1}{R_3} \right)$$

1. Calculate the gain of the input signal.

$$G_{input} = \frac{V_{o\_max} - V_{o\_min}}{V_{i\_max} - V_{i\_min}} = \frac{3.3V - 0.05V}{-1V - (-5V)} = 0.8125 \frac{V}{V}$$

2. Calculate  $R_1$  and  $R_2$ .

Choose  $R_1 = 845\Omega$

$$R_2 = \frac{R_1}{G_{input}} = \frac{R_1}{0.8125 \frac{V}{V}} = 1.04 \text{ k}\Omega$$

3. Calculate the gain of the reference voltage required to offset the output.

$$G_{ref} = \frac{R_1}{R_3} \quad ( ) \quad ( )$$

$$-V_{i\_min} \times \frac{R_1}{R_2} - V_{ref} \times \frac{R_1}{R_3} = V_{o\_min}$$

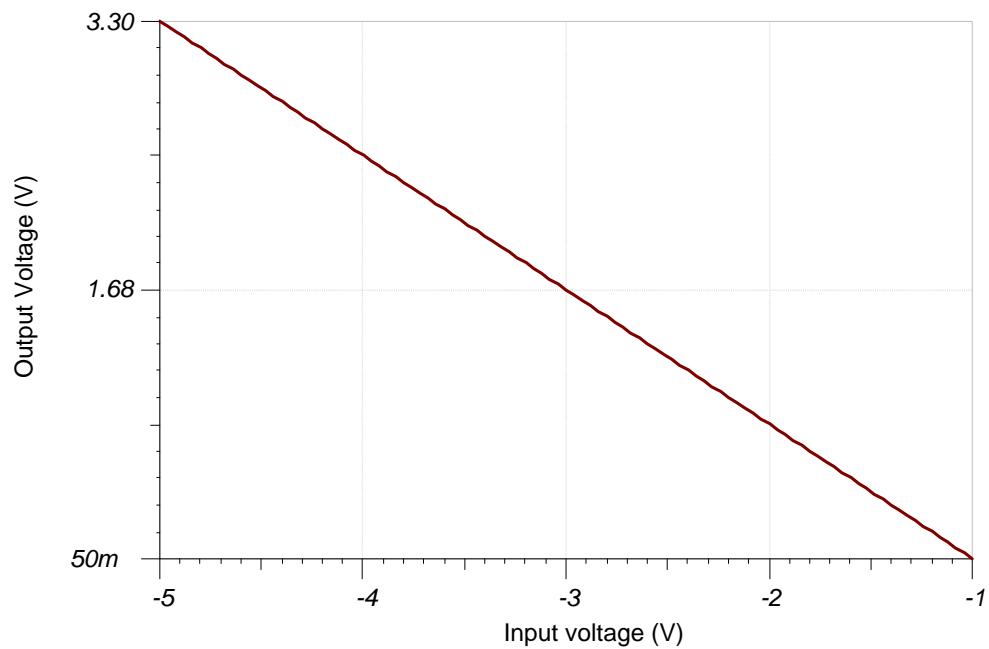
$$\frac{R_1}{R_3} = \frac{V_{o\_min} + V_{i\_min} \times \frac{R_1}{R_2}}{-V_{ref}} = \frac{0.05V + -1V}{-5} \times \frac{845\Omega}{1.04\text{k}\Omega} = 0.1525 \frac{V}{V}$$

4. Calculate  $R_3$ .

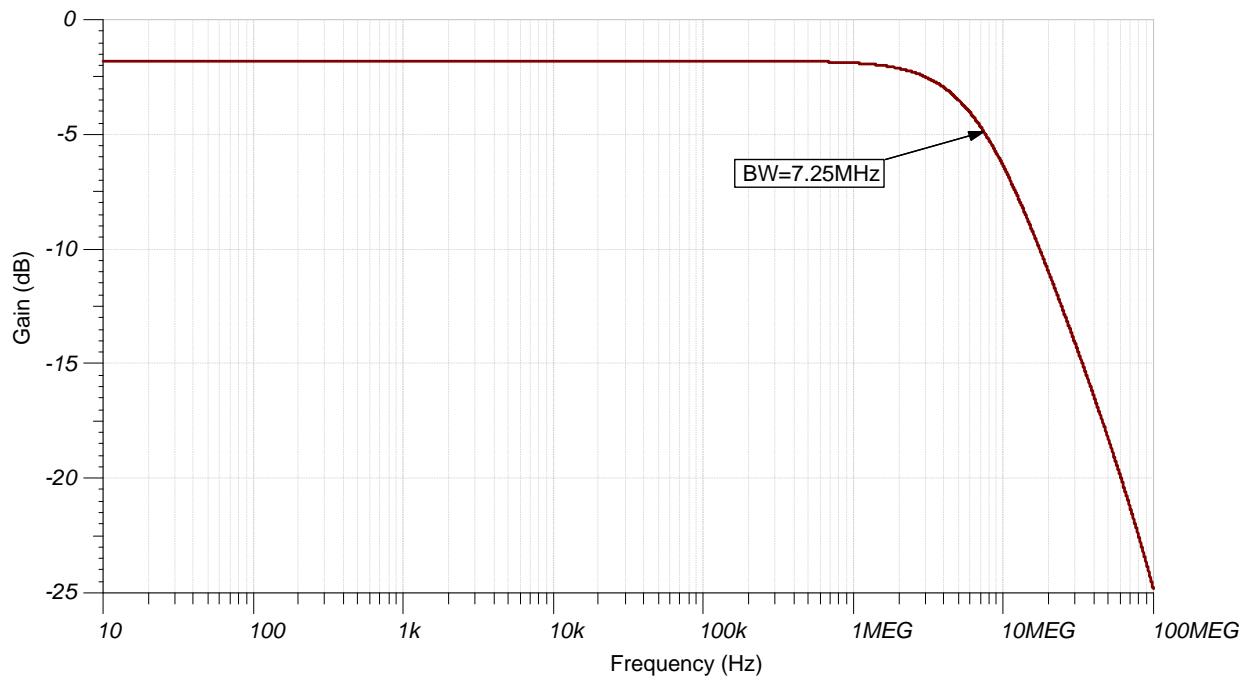
$$R_3 = \frac{R_1}{G_{ref}} = \frac{845\Omega}{0.1525 \frac{V}{V}} = 5.54 \text{ k}\Omega \approx 5.56 \text{ k}\Omega$$

## Design Simulations

### DC Simulation Results



### AC Simulation Results



## Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See the circuit SPICE simulation file [SBOC511](#).

See [Designing Gain and Offset in Thirty Seconds](#).

## Design Featured Op Amp

TLV9062	
$V_{ss}$	1.8V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	0.3mV
$I_q$	538 $\mu$ A
$I_b$	0.5pA
<b>UGBW</b>	10MHz
<b>SR</b>	6.5V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/tlv9062">www.ti.com/product/tlv9062</a>	

## Design Alternate Op Amp

OPA197	
$V_{ss}$	4.5V to 36V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	25 $\mu$ V
$I_q$	1mA
$I_b$	5pA
<b>UGBW</b>	10MHz
<b>SR</b>	20V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/opa197">www.ti.com/product/opa197</a>	

## Revision History

Revision	Date	Change
A	February 2019	Downscale the title and changed title role to 'Amplifiers'. Added links to circuit cookbook landing page and SPICE simulation file.

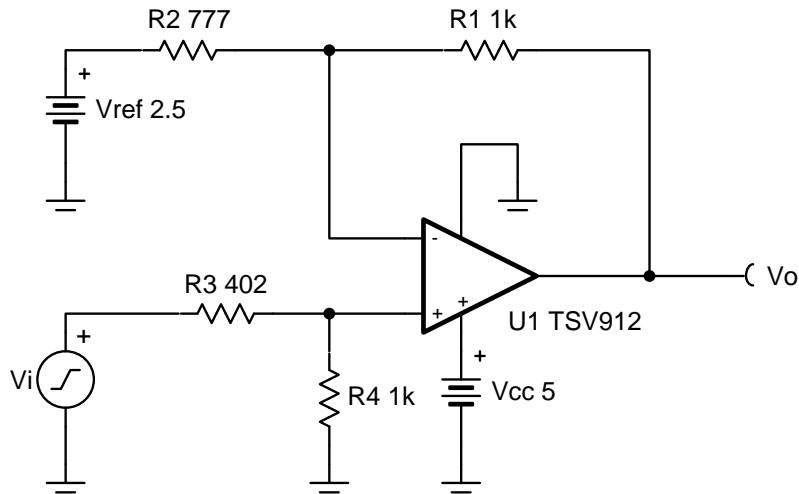
## ***Non-inverting op amp with inverting positive reference voltage circuit***

### **Design Goals**

<b>Input</b>		<b>Output</b>		<b>Supply</b>		
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	$V_{cc}$	$V_{ee}$	$V_{ref}$
2V	5V	0.05V	4.95V	5V	0V	2.5V

### **Design Description**

This design uses a non-inverting amplifier with an inverting positive reference to translate an input signal of 2V to 5V to an output voltage of 0.05V to 4.95V. This circuit can be used to translate a sensor output voltage with a positive slope and offset to a usable ADC input voltage range.



### **Design Notes**

1. Use op amp linear output operating range. Usually specified under  $A_{OL}$  test conditions.
2. Check op amp input common mode voltage range. The common mode voltage varies with the input voltage.
3.  $V_{ref}$  must be low impedance.
4. Input impedance of the circuit is equal to the sum of  $R_3$  and  $R_4$ .
5. Choose low-value resistors to use in the feedback. It is recommended to use resistor values less than 100k $\Omega$ . Using high-value resistors can degrade the phase margin of the amplifier and introduce additional noise in the circuit.
6. The cutoff frequency of the circuit is dependent on the gain bandwidth product (GBP) of the amplifier.
7. Adding a capacitor in parallel with  $R_1$  will improve stability of the circuit if high-value resistors are used.

### Design Steps

$$V_o = V_i \times \left( \frac{R_4}{R_3 + R_4} \right) \left( \frac{R_1 + R_2}{R_2} \right) - V_{ref} \times \left( \frac{R_1}{R_2} \right)$$

1. Calculate the gain of the input to produce the largest output swing.

$$V_{o\_max} - V_{o\_min} = (V_{i\_max} - V_{i\_min}) \left( \frac{R_4}{R_3 + R_4} \right) \left( \frac{R_1 + R_2}{R_2} \right)$$

$$\frac{V_{o\_max} - V_{o\_min}}{V_{i\_max} - V_{i\_min}} = \frac{R_4}{R_3 + R_4} \frac{R_1 + R_2}{R_2}$$

$$\frac{4.95V - 0.05V}{5V - 2V} = \frac{R_4}{R_3 + R_4} \frac{R_1 + R_2}{R_2}$$

$$1.633 \frac{V}{V} = \frac{R_4}{R_3 + R_4} \frac{R_1 + R_2}{R_2}$$

2. Select a value for  $R_1$  and  $R_4$  and insert the values into the previous equation. The other two resistor values must be solved using a system of equations. The proper output swing and offset voltage cannot be calculated if more than two variables are selected.

$$R_1 = R_4 = 1 \text{ k}\Omega \quad (1)$$

$$1.633 \frac{V}{V} = \frac{1 \text{ k}\Omega}{R_3 + 1 \text{ k}\Omega} \frac{1 \text{ k}\Omega + R_2}{R_2}$$

3. Solve the previous equation for  $R_3$  in terms of  $R_2$ .

$$R_3 = \frac{1 \text{ M}\Omega + (1 \text{ k}\Omega \times R_2)}{1.633 \times R_2} - 1 \text{ k}\Omega$$

4. Select any point along the transfer function within the linear output range of the amplifier to set the proper offset voltage at the output (for example, the minimum input and output voltage).

$$V_{o\_min} = V_{i\_min} \times \left( \frac{R_4}{R_3 + R_4} \right) \left( \frac{R_1 + R_2}{R_2} \right) - V_{ref} \times \left( \frac{R_1}{R_2} \right)$$

$$0.05V = 2V \times \frac{1 \text{ k}\Omega}{R_3 + 1 \text{ k}\Omega} \frac{1 \text{ k}\Omega + R_2}{R_2} - V_{ref} \times \frac{1 \text{ k}\Omega}{R_2}$$

5. Insert  $R_3$  from step 3 into the equation from step 4 and solve for  $R_2$ .

$$0.05V = 2V \times \left( \frac{1 \text{ k}\Omega}{\frac{1 \text{ M}\Omega + 1 \text{ k}\Omega \times R_2}{1.633 \times R_2} - 1 \text{ k}\Omega + 1 \text{ k}\Omega} \right) \left( \frac{1 \text{ k}\Omega + R_2}{R_2} \right) - V_{ref} \times \left( \frac{1 \text{ k}\Omega}{R_2} \right)$$

$$R_2 = 777.2 \Omega \approx 777 \Omega$$

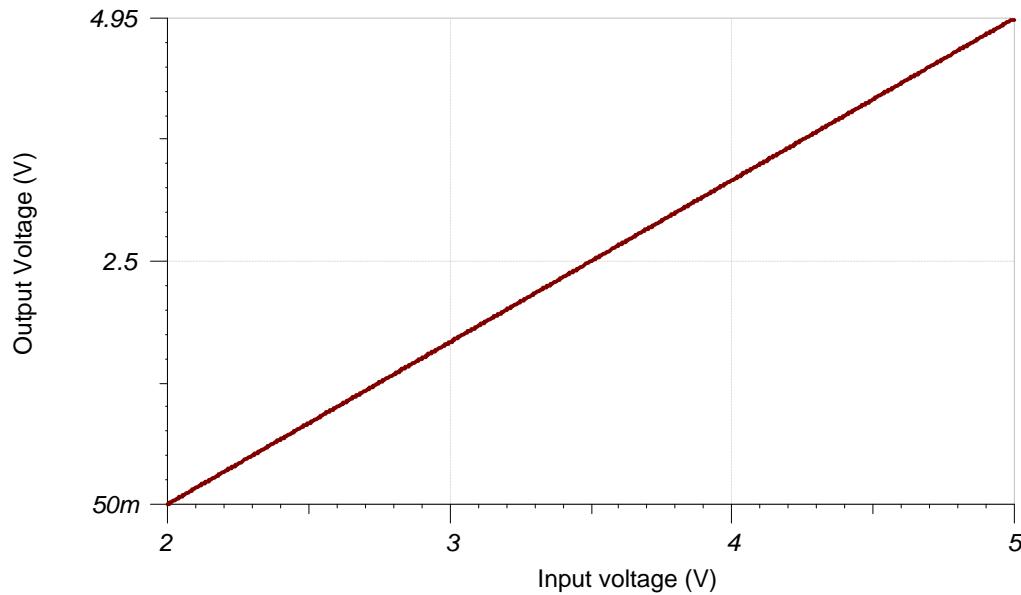
6. Insert  $R_2$  calculation from step 5, and solve for  $R_3$ .

$$R_3 = \frac{1 \text{ M}\Omega + (1 \text{ k}\Omega \times R_2)}{1.633 \times R_2} - 1 \text{ k}\Omega \quad (2)$$

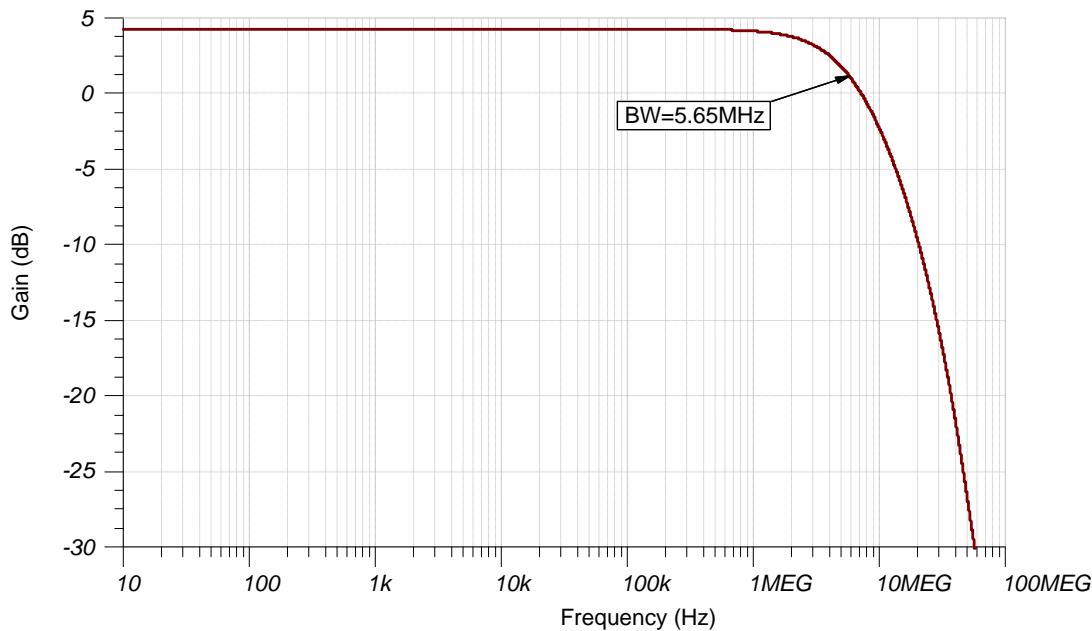
$$R_3 = \frac{1 \text{ M}\Omega + 1 \text{ k}\Omega \times 777 \Omega}{1.633 \times 777 \Omega} - 1 \text{ k}\Omega = 400.49 \Omega \approx 402 \Omega$$

## Design Simulations

### DC Simulation Results



### AC Simulation Results



## Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOC512](#).

See [TI Precision Lab Videos on Input and Output Limitations](#).

## Design Featured Op Amp

TSV912	
$V_{ss}$	2.5V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	0.3mV
$I_q$	550 $\mu$ A
$I_b$	1pA
<b>UGBW</b>	8MHz
<b>SR</b>	4.5V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/tsv912">www.ti.com/product/tsv912</a>	

## Design Alternate Op Amp

OPA191	
$V_{ss}$	4.5V to 36V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	5 $\mu$ V
$I_q$	140 $\mu$ A/Ch
$I_b$	5pA
<b>UGBW</b>	2.5MHz
<b>SR</b>	5.5V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/opa191">www.ti.com/product/opa191</a>	

## Revision History

Revision	Date	Change
A	February 2019	Downscale the title and changed title role to 'Amplifiers'. Added links to circuit cookbook landing page and SPICE simulation file.

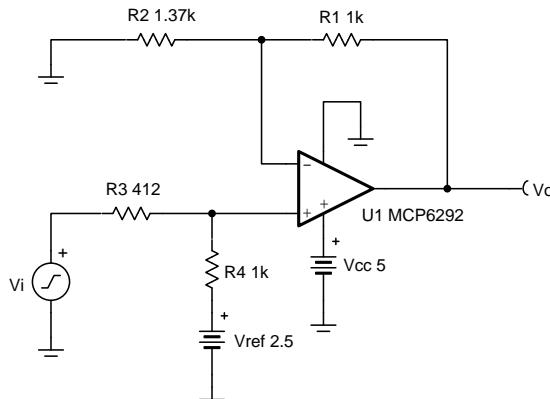
## ***Non-inverting op amp with non-inverting positive reference voltage circuit***

### **Design Goals**

<b>Input</b>		<b>Output</b>		<b>Supply</b>		
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	$V_{cc}$	$V_{ee}$	$V_{ref}$
-1V	3V	0.05V	4.95V	5V	0V	2.5V

### **Design Description**

This design uses a non-inverting amplifier with a non-inverting positive reference to translate an input signal of -1V to 3V to an output voltage of 0.05V to 4.95V. This circuit can be used to translate a sensor output voltage with a positive slope and negative offset to a usable ADC input voltage range.



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### **Design Notes**

1. Use op amp linear output operating range. Usually specified under  $A_{OL}$  test conditions.
2. Check op amp input common mode voltage range.
3.  $V_{ref}$  output must be low impedance.
4. Input impedance of the circuit is equal to the sum of  $R_3$  and  $R_4$ .
5. Choose low-value resistors to use in the feedback. It is recommended to use resistor values less than 100k $\Omega$ . Using high-value resistors can degrade the phase margin of the amplifier and introduce additional noise in the circuit.
6. The cutoff frequency of the circuit is dependent on the gain bandwidth product (GBP) of the amplifier.
7. Adding a capacitor in parallel with  $R_1$  will improve stability of the circuit if high-value resistors are used.

### Design Steps

$$V_o = V_i \times \left( \frac{R_4}{R_3 + R_4} \right) \left( \frac{R_1 + R_2}{R_2} \right) + V_{ref} \times \left( \frac{R_3}{R_3 + R_4} \right) \left( \frac{R_1 + R_2}{R_2} \right)$$

1. Calculate the gain of the input voltage to produce the desired output swing.

$$G_{input} = \left( \frac{R_4}{R_3 + R_4} \right) \left( \frac{R_1 + R_2}{R_2} \right) \quad (1)$$

$$V_{o\_max} - V_{o\_min} = V_{i\_max} - V_{i\_min} \quad \frac{R_4}{R_3 + R_4} = \frac{R_1 + R_2}{R_2}$$

$$\frac{V_{o\_max} - V_{o\_min}}{V_{i\_max} - V_{i\_min}} = \frac{R_4}{R_3 + R_4} = \frac{R_1 + R_2}{R_2}$$

$$\frac{4.95V - 0.05V}{3V - 1V} = \frac{R_4}{R_3 + R_4} = \frac{R_1 + R_2}{R_2}$$

$$1.225V = \frac{R_4}{R_3 + R_4} = \frac{R_1 + R_2}{R_2}$$

2. Select a value for  $R_1$  and  $R_4$  and insert the values into the previous equation. The other two resistor values must be solved using a system of equations. The proper output swing and offset voltage cannot be calculated if more than two variables are selected.

$$R_1 = R_4 = 1 \text{ k}\Omega \quad (1)$$

$$1.225V = \frac{1 \text{ k}\Omega}{R_3 + 1 \text{ k}\Omega} = \frac{1 \text{ k}\Omega + R_2}{R_2}$$

3. Solve the previous equation for  $R_3$  in terms of  $R_2$ .

$$R_3 = \frac{1 \text{ M}\Omega + (1 \text{ k}\Omega \times R_2)}{1.225 \times R_2} - 1 \text{ k}\Omega$$

4. Select any point along the transfer function within the linear output range of the amplifier to set the proper offset voltage at the output (for example, the minimum input and output voltage).

$$V_{o\_min} = V_{i\_min} \times \left( \frac{R_4}{R_3 + R_4} \right) \left( \frac{R_1 + R_2}{R_2} \right) + V_{ref} \times \left( \frac{R_3}{R_3 + R_4} \right) \left( \frac{R_1 + R_2}{R_2} \right)$$

$$0.05V = -1 \text{ V} \times \frac{1 \text{ k}\Omega}{R_3 + 1 \text{ k}\Omega} = \frac{1 \text{ k}\Omega + R_2}{R_2} + 2.5V \times \frac{R_3}{R_3 + 1 \text{ k}\Omega} = \frac{1 \text{ k}\Omega + R_2}{R_2}$$

5. Insert  $R_3$  into the equation from step 1 and solve for  $R_2$ .

$$0.05V = -1 \text{ V} \times \left( \frac{1 \text{ k}\Omega}{\frac{1 \text{ M}\Omega + 1 \text{ k}\Omega \times R_2}{1.225 \times R_2} - 1 \text{ k}\Omega + 1 \text{ k}\Omega} \right) \left( \frac{1 \text{ k}\Omega + R_2}{R_2} \right) + 2.5V \times \left( \frac{\frac{1 \text{ M}\Omega + 1 \text{ k}\Omega \times R_2 - 1 \text{ k}\Omega}{1.225 \times R_2}}{\frac{1 \text{ M}\Omega + 1 \text{ k}\Omega \times R_2 - 1 \text{ k}\Omega + 1 \text{ k}\Omega}{1.225 \times R_2}} \right) \left( \frac{1 \text{ k}\Omega + R_2}{R_2} \right)$$

$$R_2 = 1360.5\Omega \approx 1370\Omega$$

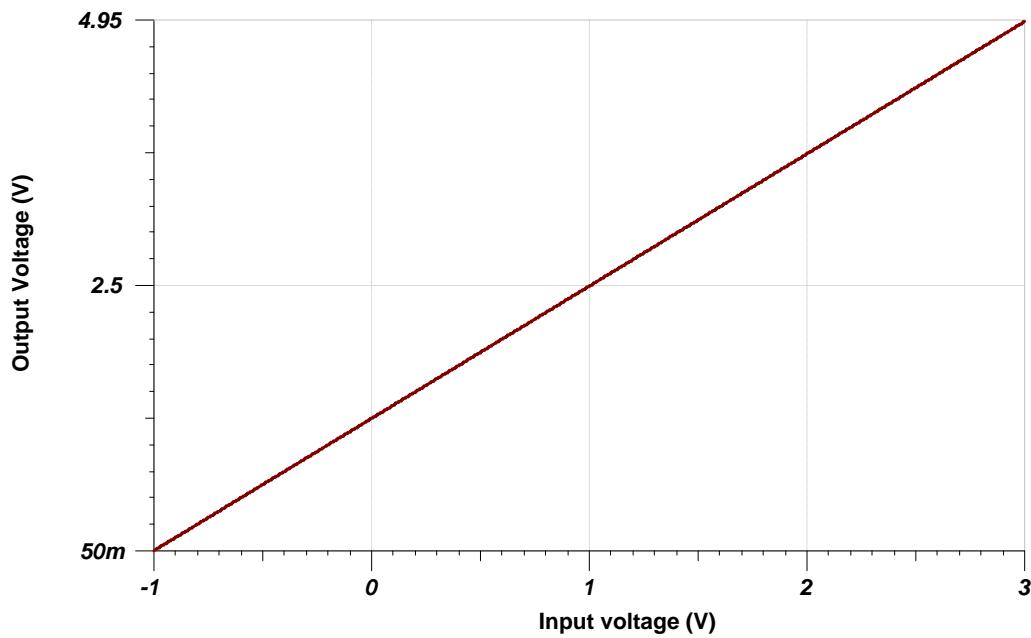
6. Insert  $R_2$  into the equation from step 1 to solve for  $R_3$ .

$$R_3 = \frac{1 \text{ M}\Omega + 1 \text{ k}\Omega \times (1370\Omega)}{1.225 \times (1370\Omega)} - 1 \text{ k}\Omega$$

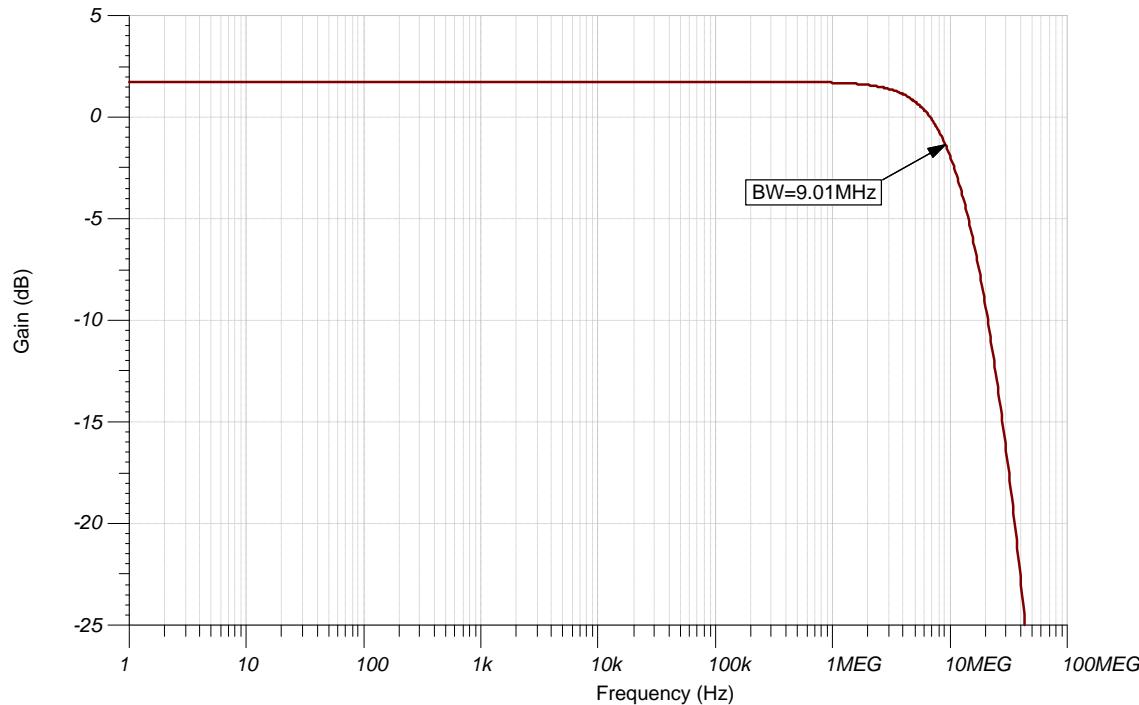
$$R_3 = 412.18\Omega \approx 412\Omega$$

## Design Simulations

### DC Simulation Results



### AC Simulation Results



## Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See the circuit SPICE simulation file [SBOC513](#).

See [Designing Gain and Offset in Thirty Seconds](#).

## Design Featured Op Amp

MCP6292	
$V_{ss}$	2.4V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	0.3mV
$I_q$	600 $\mu$ A
$I_b$	1pA
<b>UGBW</b>	10MHz
<b>SR</b>	6.5V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/MCP6292">www.ti.com/product/MCP6292</a>	

## Design Alternate Op Amp

OPA388	
$V_{ss}$	2.5V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	0.25 $\mu$ V
$I_q$	1.9mA
$I_b$	30pA
<b>UGBW</b>	10MHz
<b>SR</b>	5V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/opa388">www.ti.com/product/opa388</a>	

## Revision History

Revision	Date	Change
A	January 2019	Downscale the title and changed title role to 'Amplifiers'. Added links to circuit cookbook landing page and SPICE simulation file.

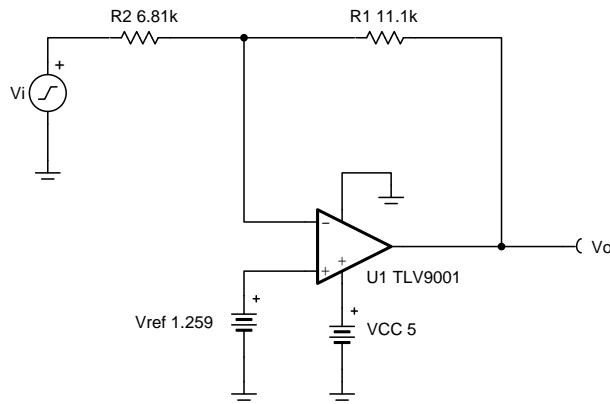
## ***Inverting op amp with non-inverting positive reference voltage circuit***

### **Design Goals**

<b>Input</b>		<b>Output</b>		<b>Supply</b>		
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	$V_{cc}$	$V_{ee}$	$V_{ref}$
-1V	2V	0.05V	4.95V	5V	0V	1.259V

### **Design Description**

This design uses an inverting amplifier with a non-inverting positive reference voltage to translate an input signal of -1V to 2V to an output voltage of 0.05V to 4.95V. This circuit can be used to translate a sensor output voltage with a positive slope and negative offset to a usable ADC input voltage range.



### **Design Notes**

1. Use op amp linear output operating range. Usually specified under  $A_{OL}$  test conditions.
2. Amplifier common mode voltage is equal to the reference voltage.
3.  $V_{ref}$  can be created with a voltage divider.
4. Input impedance of the circuit is equal to  $R_2$ .
5. Choose low-value resistors to use in the feedback. It is recommended to use resistor values less than 100kΩ. Using high-value resistors can degrade the phase margin of the amplifier and introduce additional noise in the circuit.
6. The cutoff frequency of the circuit is dependent on the gain bandwidth product (GBP) of the amplifier. Additional filtering can be accomplished by adding a capacitor in parallel to  $R_1$ . Adding a capacitor in parallel with  $R_1$  will also improve stability of the circuit, if high-value resistors are used.

### Design Steps

$$V_o = - V_i \times \left( \frac{R_1}{R_2} \right) + V_{ref} \times \left( 1 + \frac{R_1}{R_2} \right)$$

1. Calculate the gain of the input signal.

$$G_{input} = - \frac{R_1}{R_2} \quad (1)$$

$$V_{o\_max} - V_{o\_min} = V_{i\_max} - V_{i\_min} - \frac{R_1}{R_2}$$

$$- \frac{R_1}{R_2} = - \frac{V_{o\_max} - V_{o\_min}}{V_{i\_max} - V_{i\_min}} = - \frac{4.95V - 0.05V}{2V - 1V} = - 1.633 \frac{V}{V}$$

2. Select  $R_2$  and calculate  $R_1$ .

$$R_2 = 6.81 \text{ k}\Omega$$

$$R_1 = G_{input} \times R_2 = 1.633 \frac{V}{V} \times 6.81 \text{ k}\Omega = 11.123 \text{ k}\Omega \approx 11.1 \text{ k}\Omega \text{ (Standard Value)}$$

3. Calculate the reference voltage.

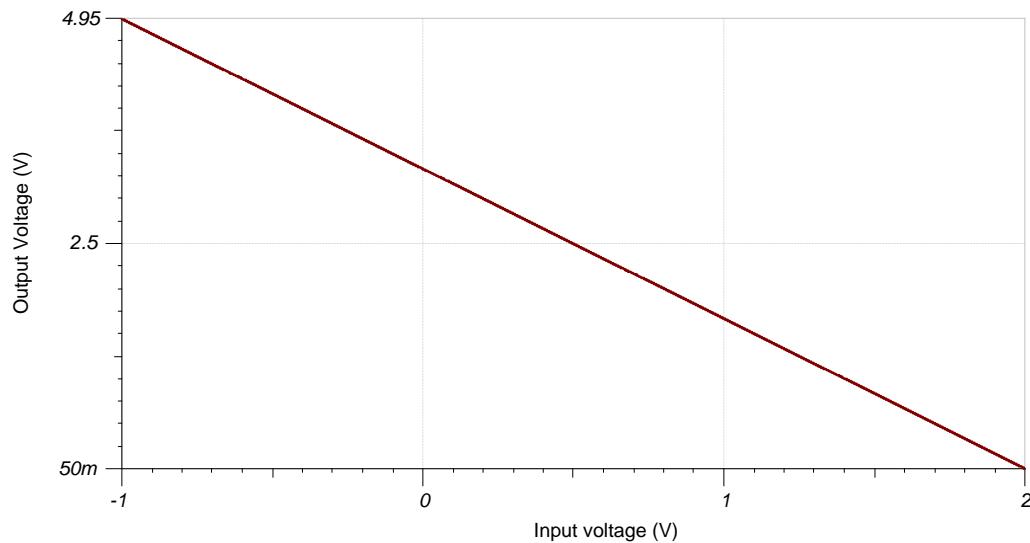
$$V_{o\_min} = - V_{i\_max} \times \left( \frac{R_1}{R_2} \right) + V_{ref} \times \left( 1 + \frac{R_1}{R_2} \right)$$

$$0.05V = - 2V \times \frac{11.11 \text{ k}\Omega}{6.81 \text{ k}\Omega} + V_{ref} \times 1 + \frac{11.11 \text{ k}\Omega}{6.81 \text{ k}\Omega}$$

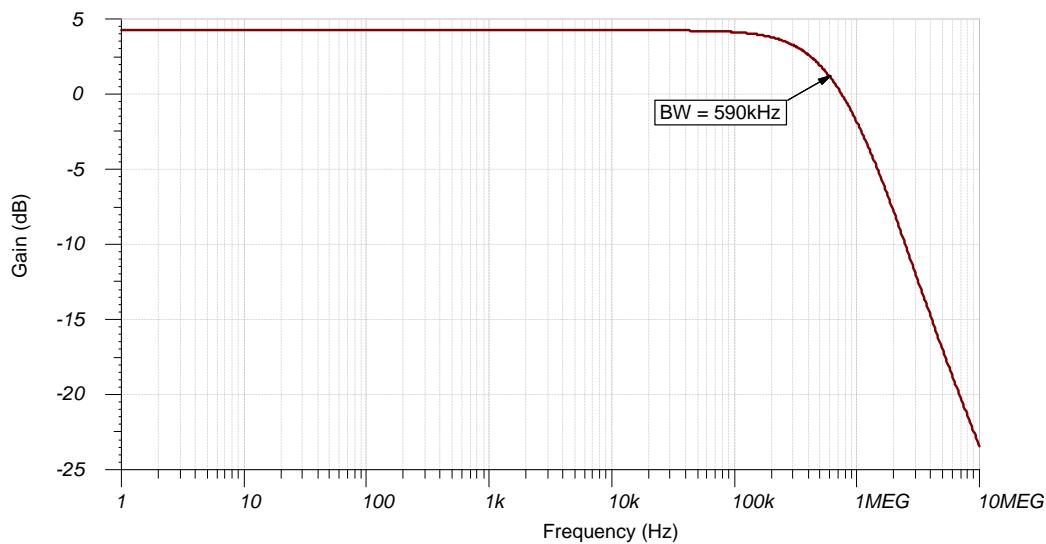
$$V_{ref} = \frac{V_{o\_min} + V_{i\_max} \times \frac{R_1}{R_2}}{1 + \frac{R_1}{R_2}} \frac{0.05V + 2V \times \frac{11.11 \text{ k}\Omega}{6.81 \text{ k}\Omega}}{1 + \frac{11.11 \text{ k}\Omega}{6.81 \text{ k}\Omega}} = 1.259V$$

## Design Simulations

### DC Simulation Results



### AC Simulation Results



## Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See the circuit SPICE simulation file [SBOC514](#).

See the [Designing gain and offset in thirty seconds](#) application report.

## Design Featured Op Amp

TLV9001	
$V_{ss}$	1.8V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	0.4mV
$I_q$	60 $\mu$ A
$I_b$	5pA
<b>UGBW</b>	1MHz
<b>SR</b>	2V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/tlv9002">www.ti.com/product/tlv9002</a>	

## Design Alternate Op Amp

OPA376	
$V_{ss}$	2.2V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	5 $\mu$ V
$I_q$	760 $\mu$ A
$I_b$	0.2pA
<b>UGBW</b>	5.5MHz
<b>SR</b>	2V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/opa376">www.ti.com/product/opa376</a>	

## Revision History

Revision	Date	Change
A	February 2019	Downscale the title and changed title role to 'Amplifiers'. Added links to circuit cookbook landing page and SPICE simulation file.

## Single-supply diff-in to diff-out AC amplifier circuit

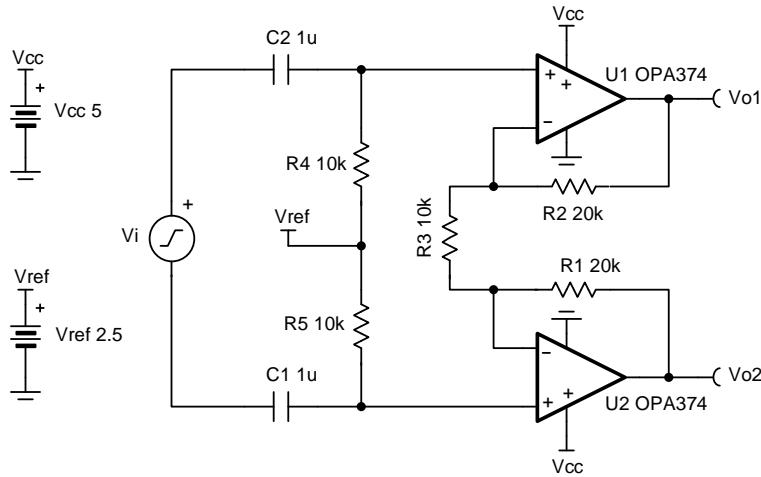
### Design Goals

Diff. Input $V_i$		Diff. Output ( $V_{o1} - V_{o2}$ )		Supply		
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	$V_{cc}$	$V_{ee}$	$V_{ref}$
-500mV	+500mV	-2.5V	+2.5V	+5	0V	+2.5V

Lower Cutoff Freq.	Upper Cutoff Freq.
16Hz	> 1MHz

### Design Description

This circuit uses 2 op amps to build a discrete, single-supply diff-in diff-out amplifier. The circuit converts a differential signal to a differential output signal.



### Design Notes

1. Ensure that  $R_1$  and  $R_2$  are well matched with high accuracy resistors to maintain high DC common-mode rejection performance.
2. Increase  $R_4$  and  $R_5$  to match the necessary input impedance at the expense of thermal noise performance.
3. Bias for single-supply operation can also be created by a voltage divider from  $V_{cc}$  to ground.
4.  $V_{ref}$  sets the output voltage of the instrumentation amplifier bias at mid-supply to allow the output to swing to both supply rails.
5. Choose  $C_1$  and  $C_2$  to select the lower cutoff frequency.
6. Linear operation is contingent upon the input common-mode and the output swing ranges of the discrete op amps used. The linear output swing ranges are specified under the Aol test conditions in the op amps data sheets

## Design Steps

1. The transfer function of the circuit is shown below.

$$V_{oDiff} = V_i \times G + V_{ref}$$

where  $V_i$  = the differential input voltage

$V_{ref}$  = the reference voltage provided to the amplifier

$$G = 1 + 2 \times \left(\frac{R_1}{R_3}\right)$$

2. Choose resistors  $R_1 = R_2$  to maintain common-mode rejection performance.

Choose  $R_1 = R_2 = 20 \text{ k}\Omega$  (Standard value)

3. Choose resistors  $R_4$  and  $R_5$  to meet the desired input impedance.

Choose  $R_4 = R_5 = 10 \text{ k}\Omega$  (Standard value)

4. Calculate  $R_3$  to set the differential gain.

$$\text{Gain} = 1 + \left(\frac{2 \times R_1}{R_3}\right) = 5 \frac{V}{V}$$

$$R_1 = R_2 = 20 \text{ k}\Omega$$

$$G = 1 + \frac{2 \times 20 \text{ k}\Omega}{R_3} = 5 \frac{V}{V} \rightarrow 5 \frac{V}{V} - 1 = \frac{40 \text{ k}\Omega}{R_3} = 4 \rightarrow R_3 = \frac{40 \text{ k}\Omega}{4} = 10 \text{ k}\Omega \text{ (Standard value)}$$

5. Set the reference voltage  $V_{ref}$  at mid-supply.

$$V_{ref} = \frac{V_{cc}}{2} = \frac{5V}{2} \rightarrow V_{ref} = 2.5V$$

6. Calculate  $C_1$  and  $C_2$  to set the lower cutoff frequency.

$$f_c = \frac{1}{2 \times \pi \times R_4 \times C_1} = 16 \text{ Hz}$$

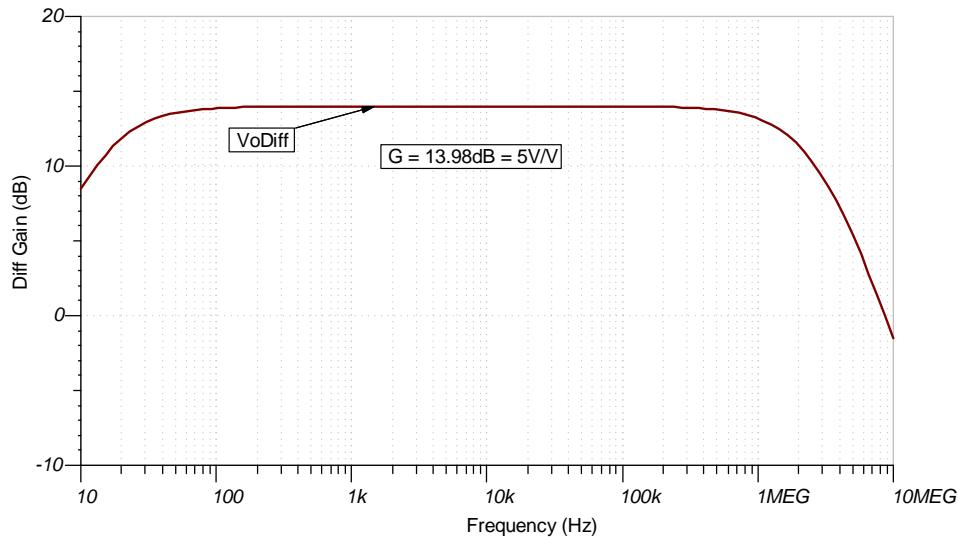
$$R_4 = R_5 = 10 \text{ k}\Omega$$

$$f_c = \frac{1}{2 \times \pi \times 10 \text{ k}\Omega \times C_1} = 16 \text{ Hz} \rightarrow C_1 = \frac{1}{2 \times \pi \times 10 \text{ k}\Omega \times 16 \text{ Hz}} = 0.99 \mu\text{F} \rightarrow C_1 = C_2 = 1 \mu\text{F} \text{ (Standard value)}$$

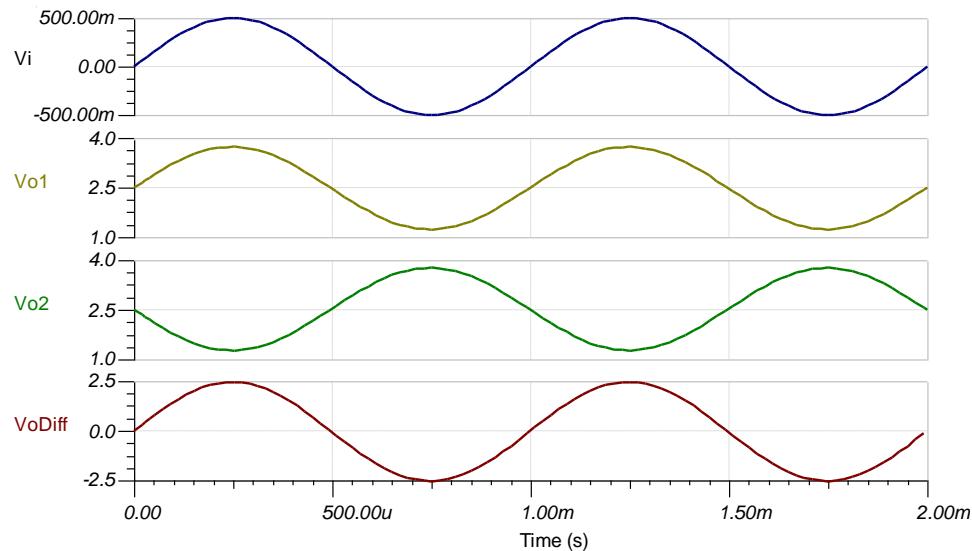
## Design Simulations

### AC Simulation Results

In the following figure, notice the lower  $-3\text{-dB}$  cutoff frequency is approximately 16Hz and the upper cutoff frequency is  $> 1\text{MHz}$  as required for this design.



### Transient Simulation Results



## References

1. [Analog Engineer's Circuit Cookbooks](#)
2. SPICE Simulation File [SBOMAU5](#).
3. [TI Precision Labs](#)

## Design Featured Op Amp

OPA374	
$V_{ss}$	2.3V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	1mV
$I_q$	585 $\mu$ A/Ch
$I_b$	0.5pA
<b>UGBW</b>	6.5MHz
<b>SR</b>	5V/ $\mu$ s
<b>#Channels</b>	1,2,4
<a href="http://www.ti.com/product/opa374">www.ti.com/product/opa374</a>	

## Design Alternate Op Amp

TLV9061	
$V_{ss}$	1.8V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	0.3mV
$I_q$	0.538mA
$I_b$	0.5pA
<b>UGBW</b>	10MHz
<b>SR</b>	6.5V/ $\mu$ s
<b>#Channels</b>	1,2,4
<a href="http://www.ti.com/product/tlv9061">www.ti.com/product/tlv9061</a>	

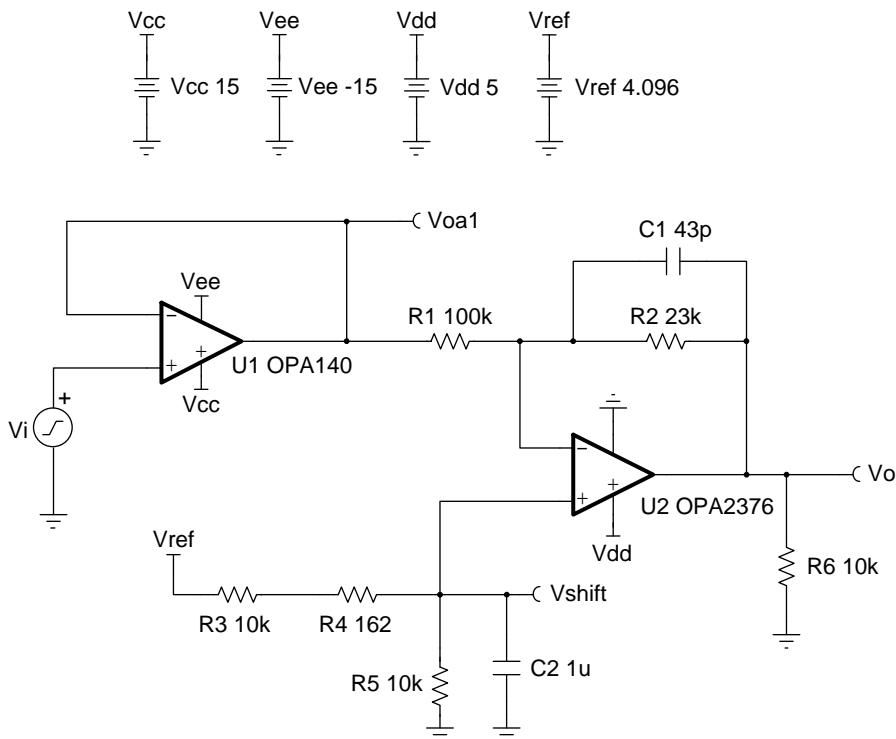
## Inverting dual-supply to single-supply amplifier circuit

### Design Goals

Input		Output		Supply			
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	$V_{cc}$	$V_{ee}$	$V_{dd}$	$V_{ref}$
-10V	+10V	+0.2V	+4.8V	+15V	-15V	+5V	+4.096V

### Design Description

This inverting dual-supply to single-supply amplifier translates a  $\pm 10\text{-V}$  signal to a  $0\text{-V}$  to  $5\text{-V}$  signal for use with an ADC. Levels can easily be adjusted using the given equations. The buffer can be replaced with other  $\pm 15\text{-V}$  configurations to accommodate the desired input signal, as long as the output of the first stage is low impedance.



### Design Notes

1. Observe common-mode limitations of the input buffer.
2. A high-impedance source will alter the gain characteristics of  $U_2$  if buffer amplifier  $U_1$  is not used.
3.  $R_6$  provides a path to ground for the output of  $U_1$  if the  $\pm 15\text{-V}$  supplies come up before the  $5\text{-V}$  supply. This limits the voltage at the inverting pin of  $U_2$  through the voltage divider created by  $R_1$ ,  $R_2$ , and  $R_6$  and prevents damage to  $U_2$  as well as to any converter that may be connected to its output. To best protect the devices a transient voltage suppressor (TVS) should be used at the power pins of  $U_2$ .
4. A capacitor across  $R_5$  will help filter  $V_{ref}$  and provide a cleaner  $V_{shift}$ .

## Design Steps

The transfer function for this circuit follows:

$$V_o = -\frac{R_2}{R_1} \times V_i + (1 + \frac{R_2}{R_1}) \times V_{shift}$$

1. Set the gain of the amplifier.

$$\frac{\Delta V_o}{\Delta V_i} = \frac{V_{oMax} - V_{oMin}}{V_{iMax} - V_{iMin}} = \frac{4.8V - 0.2V}{10V - (-10V)} = 0.23$$

$$\frac{\Delta V_o}{\Delta V_i} = \frac{R_2}{R_1}$$

$$R_2 = 0.23 \times R_1$$

Choose  $R_1 = 100\text{k}\Omega$  (standard value)

$R_2 = 23\text{k}\Omega$  (for standard values use  $22\text{k}\Omega$  and  $1\text{k}\Omega$  in series)

2. Set  $V_{shift}$  to translate the signal to single supply.

At midscale,  $V_{in} = 0V$

$$\text{Then } V_o = (1 + \frac{R_2}{R_1}) \times V_{shift}$$

$$V_{shift} = \frac{V_o}{(1 + \frac{R_2}{R_1})} = \frac{2.5V}{1.23} = 2.033V$$

3. Select resistors for reference voltage divider to achieve  $V_{shift}$ .

$$V_{ref} = 4.096V$$

$$V_{shift} = V_{ref} \times \frac{R_5}{(R_3 + R_4) + R_5}$$

$$\frac{V_{shift}}{V_{ref}} = \frac{2.033V}{4.096V} = \frac{R_5}{(R_3 + R_4) + R_5}$$

$$R_3 + R_4 = 1.0161 \times R_5$$

Select a standard value for  $R_5$

$$R_5 = 10\text{k}\Omega$$

$$R_3 + R_4 = 10.161\text{k}\Omega$$

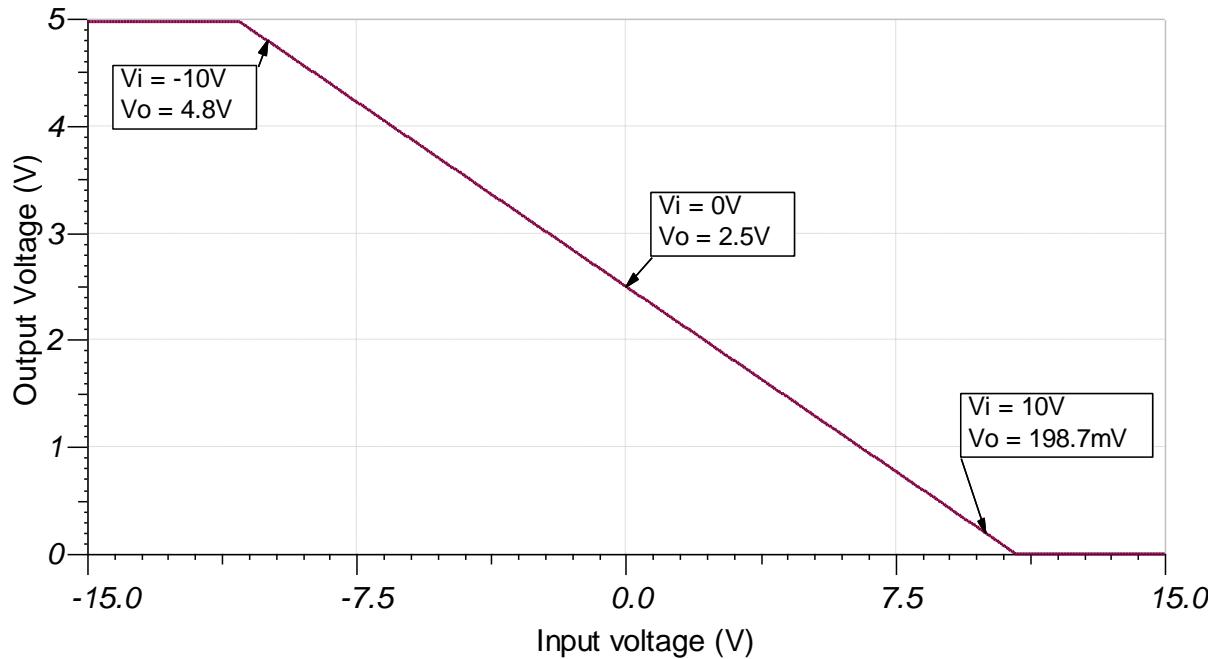
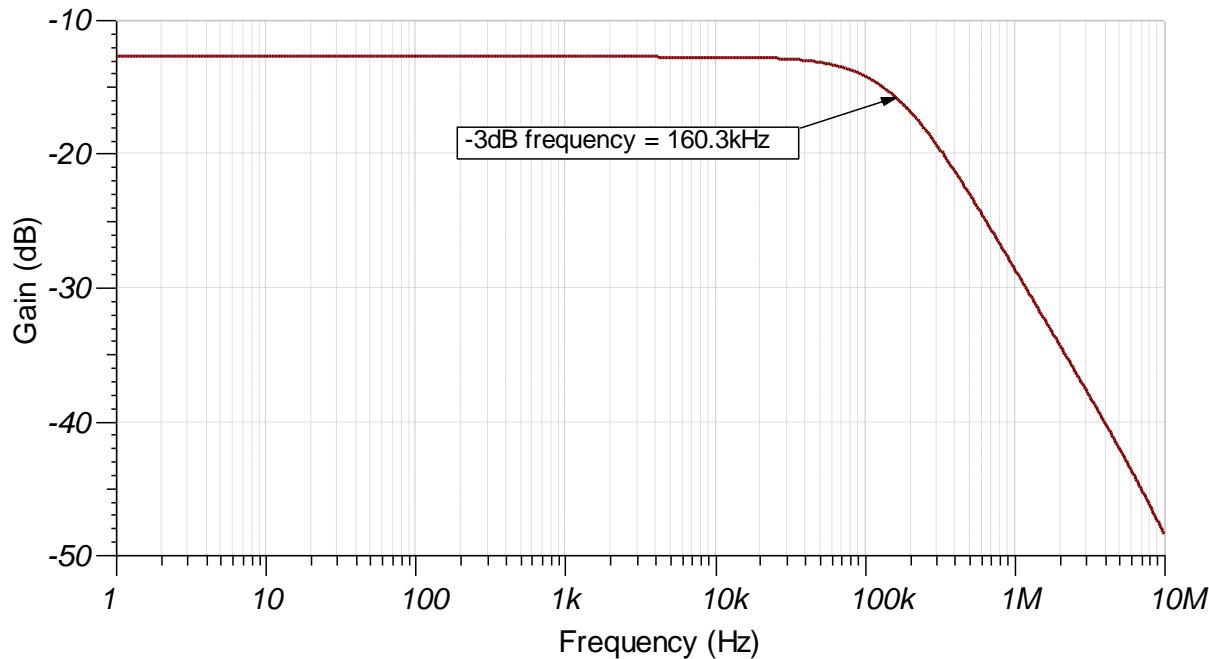
$$R_3 = 10\text{k}\Omega$$

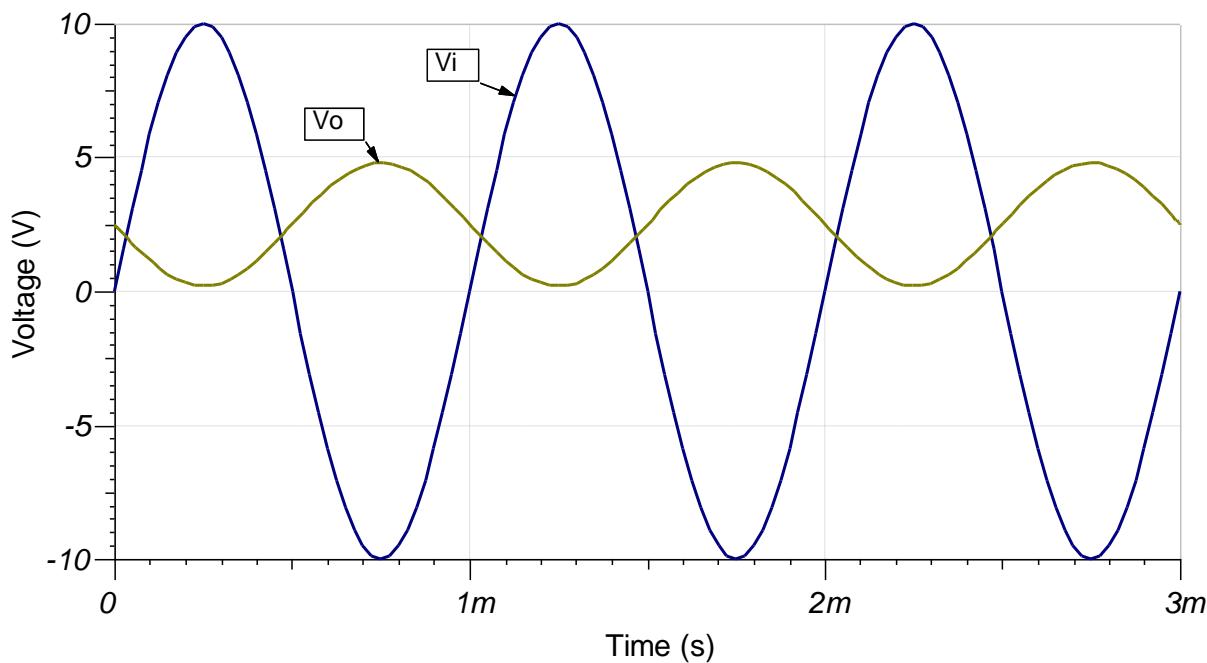
$$R_4 = 162\Omega \text{ (standard 1% value)}$$

4. Large feedback resistors can interact with the input capacitance and cause instability. Choose  $C_1$  to add a pole to the transfer function to counteract this. The pole must be lower in frequency than the effective bandwidth of the op amp.

$$C_1 = 43\text{pF}$$

$$f_p = \frac{1}{2\pi \times R_2 \times C_1} = 160.3\text{kHz}$$

**Design Simulations**
**DC Simulation Results**

**AC Simulation Results**


**Transient Simulation Results**

### Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See TINA-TI™ circuit simulation file, [SBOMAT9](#).

See TIPD148, <http://www.ti.com/tool/TIPD148>.

### Design Featured Op Amp

OPA376	
<b>V<sub>ss</sub></b>	2.2V to 5.5V
<b>V<sub>inCM</sub></b>	Vee to Vcc-1.3V
<b>V<sub>out</sub></b>	Rail-to-rail
<b>V<sub>os</sub></b>	5µV
<b>I<sub>q</sub></b>	760µA/Ch
<b>I<sub>b</sub></b>	0.2pA
<b>UGBW</b>	5.5MHz
<b>SR</b>	2V/µs
<b>#Channels</b>	1,2,4
<a href="http://www.ti.com/product/opa376">http://www.ti.com/product/opa376</a>	

### Design Featured Op Amp

OPA140	
<b>V<sub>ss</sub></b>	4.5V to 36V
<b>V<sub>inCM</sub></b>	Vee-0.1V to Vcc-3.5V
<b>V<sub>out</sub></b>	Rail-to-rail
<b>V<sub>os</sub></b>	30µV
<b>I<sub>q</sub></b>	1.8mA/Ch
<b>I<sub>b</sub></b>	±0.5pA
<b>UGBW</b>	11MHz
<b>SR</b>	20V/µs
<b>#Channels</b>	1,2,4
<a href="http://www.ti.com/product/opa375">http://www.ti.com/product/opa375</a>	

## Dual-supply, discrete, programmable gain amplifier circuit

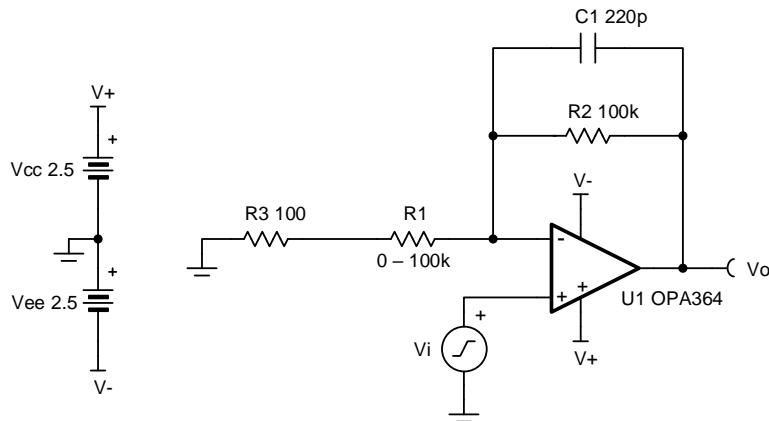
### Design Goals

Input		Output		Supply	
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	$V_{cc}$	$V_{ee}$
-1.25V	+1.25V	-2.4V	+2.4V	+2.5V	-2.5V

Gain	Cutoff Frequency
6dB (2V/V) to 60dB (1000 V/V)	7kHz

### Design Description

This circuit provides programmable, non-inverting gains ranging from 6dB (2V/V) to 60dB (1000V/V) using a variable input resistance. The design maintains the same cutoff frequency over the gain range.



### Design Notes

1. Choose a digital potentiometer, such as TPL0102 for  $R_1$  to design a low-cost digital programmable gain amplifier.
2.  $R_3$  sets the maximum gain when  $R_1$  approaches  $0\Omega$ .
3. A feedback capacitor limits the bandwidth and prevent stability issues.
4. Stability should be evaluated across the selected gain range. The minimum gain setting will likely be most sensitive to stability issues.
5. Some digital potentiometers can vary in absolute value by as much as  $\pm 20\%$  so gain calibration may be necessary.

### Design Steps

1. Choose  $R_2$  and  $R_3$ , to set the maximum gain when  $R_1$  approaches 0:

$$G_{\max} = 1 + \frac{R_2}{R_3}$$

$$G_{\max} - 1 = \frac{R_2}{R_3} \rightarrow R_2 = (G_{\max} - 1) \times R_3$$

Set  $R_3 = 100 \Omega$

$$R_2 = (1000 \frac{V}{V} - 1) \times 100 = 99 \text{ k}\Omega \rightarrow R_2 = 100 \text{ k}\Omega \text{ (Standard value)}$$

2. Choose the potentiometer maximum value to set the minimum gain:

$$G_{\min} = 1 + \frac{R_2}{R_{1,\max} + R_3}$$

$$G_{\min} - 1 = \frac{R_2}{R_{1,\max} + R_3}$$

$$R_{1,\max} + R_3 = \frac{R_2}{G_{\min} - 1}$$

$$R_{1,\max} = \frac{R_2}{G_{\min} - 1} - R_3 = \frac{100\text{k}\Omega}{2-1} - 100\Omega = 99.9\text{k}\Omega \rightarrow R_{1,\max} = 100\text{k}\Omega \text{ (Standard value)}$$

$R_{1,\min} = 0\Omega$  (Wiper resistance, typically  $25\Omega$ , will introduce some error)

3. Choose the bandwidth with a feedback capacitor:

$$f_c = \frac{GBW}{G_{\max}} = \frac{7\text{MHz}}{1000\frac{V}{V}} = 7\text{kHz}$$

$$f_c = 7\text{kHz} \rightarrow C_1 = \frac{1}{2\pi \times R_2 \times f_c} = 227\text{pF} \rightarrow C_1 = 220\text{pF} \text{ (Standard Value)}$$

4. Check for stability at minimum gain ( $2V/V$ ), which is when  $R_1=100\text{k}\Omega$ . To satisfy the requirement  $f_c$  (circuit bandwidth) must be less than  $f_{\text{zero}}$  (zero created by the resistive feedback network and the differential and common-mode input capacitances).

$$f_c = \frac{1}{2\pi \times C_1 \times R_2} = 7 \text{ kHz}$$

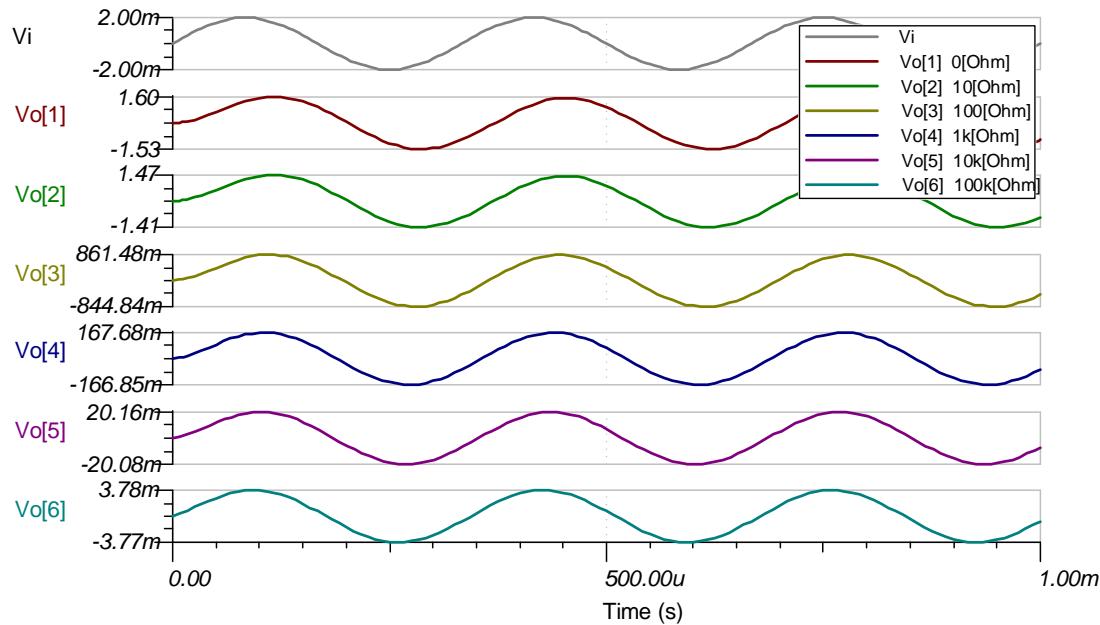
$$f_{\text{zero}} = \frac{1}{2\pi \times (C_{\text{cm}} + C_{\text{diff}}) \times (R_2 \parallel R_1)} = \frac{1}{2 \times \pi \times (3 \text{ pF} + 2 \text{ pF}) \times \left( \frac{100 \text{ k}\Omega \times 100 \text{ k}\Omega}{100 \text{ k}\Omega + 100 \text{ k}\Omega} \right)}$$

$$f_{\text{zero}} = 637 \text{ kHz}$$

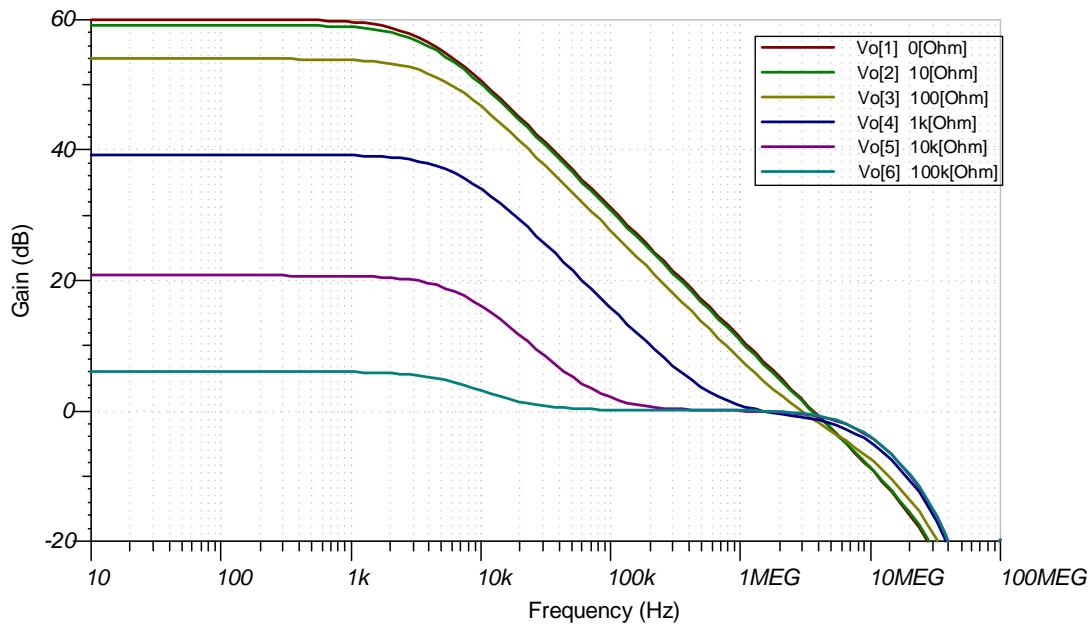
$$7 \text{ kHz} < 637 \text{ kHz} \rightarrow f_c < f_{\text{zero}}$$

## Design Simulations

### Transient Simulation Results



### AC Simulation Results



**References:**

1. [Analog Engineer's Circuit Cookbooks](#)
2. [SPICE Simulation File SBOC521](#)
3. [TI Precision Designs TIPD204](#)
4. [TI Precision Labs](#)

**Design Featured Op Amp**

OPA364	
$V_{ss}$	1.8V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	1mV
$I_q$	1.1mA
$I_b$	1pA
<b>UGBW</b>	7MHz
<b>SR</b>	5V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/opa364">www.ti.com/product/opa364</a>	

**Design Alternate Op Amp**

OPA376	
$V_{ss}$	2.2V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	5 $\mu$ V
$I_q$	760 $\mu$ A
$I_b$	0.2pA
<b>UGBW</b>	5.5MHz
<b>SR</b>	2V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/opa376">www.ti.com/product/opa376</a>	

## AC coupled instrumentation amplifier circuit

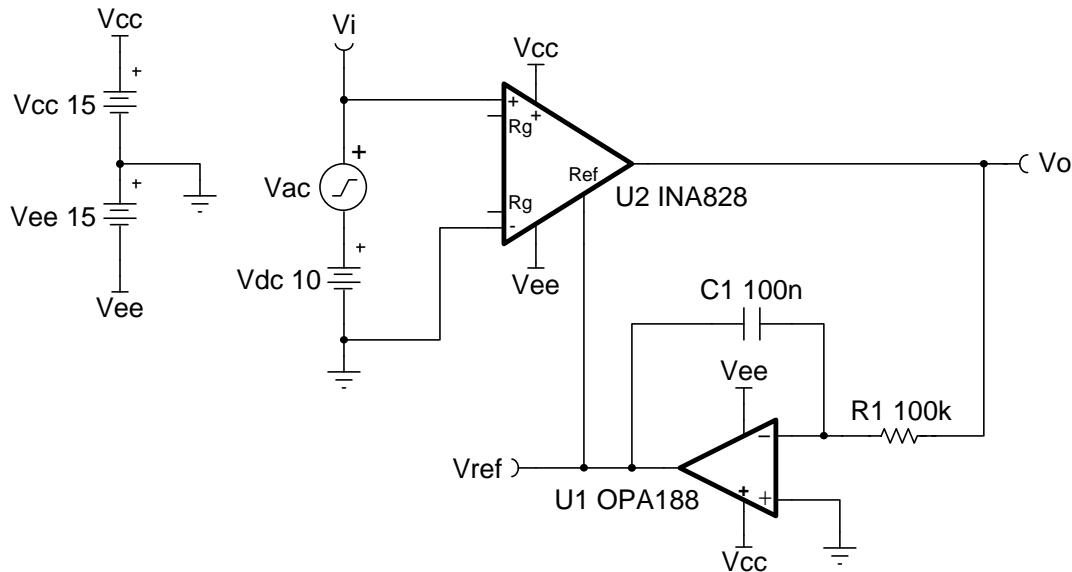
### Design Goals

Input		Output		Supply	
$V_{iMin}$	$V_{iMax}$	$V_{oMin}$	$V_{oMax}$	$V_{cc}$	$V_{ee}$
-13V	13V	-14.85V	14.85	15	-15

Lower Cutoff Frequency ( $f_L$ )	Gain	Input
16Hz	1	$\pm 2\text{VAC}$ ; +10VDC

### Design Description

This circuit produces an AC-coupled output from a DC-coupled input to an instrumentation amplifier. The output is fed back through an integrator, and the output of the integrator is used to modulate the reference voltage of the amplifier. This creates a high-pass filter and effectively cancels the output offset. This circuit avoids the need for large capacitors and resistors on the input, which can significantly degrade CMRR due to component mismatch.



### Design Notes

1. The DC correction from output to reference is unity-gain.  $U_1$  can only correct for a signal within its input/output limitations, thus the magnitude of DC voltage that can be corrected for will degrade with increasing instrumentation amplifier gain. See the table in Design Steps for more information.
2. Large values of  $R_1$  and  $C_1$  will lower the cutoff frequency, but increase startup transient response time. Startup behavior can be observed in the Transient Simulation Results.
3. When AC-coupling this way, the total input voltage must remain within the common-mode input range of the instrumentation amplifier.

### Design Steps

1. Set the lower cutoff frequency for circuit (integrator cutoff frequency). The upper cutoff frequency will be dictated by the gain and instrumentation amplifier bandwidth.

$$f_L = \frac{1}{2\pi \times R_1 \times C_1} = 16 \text{ Hz}$$

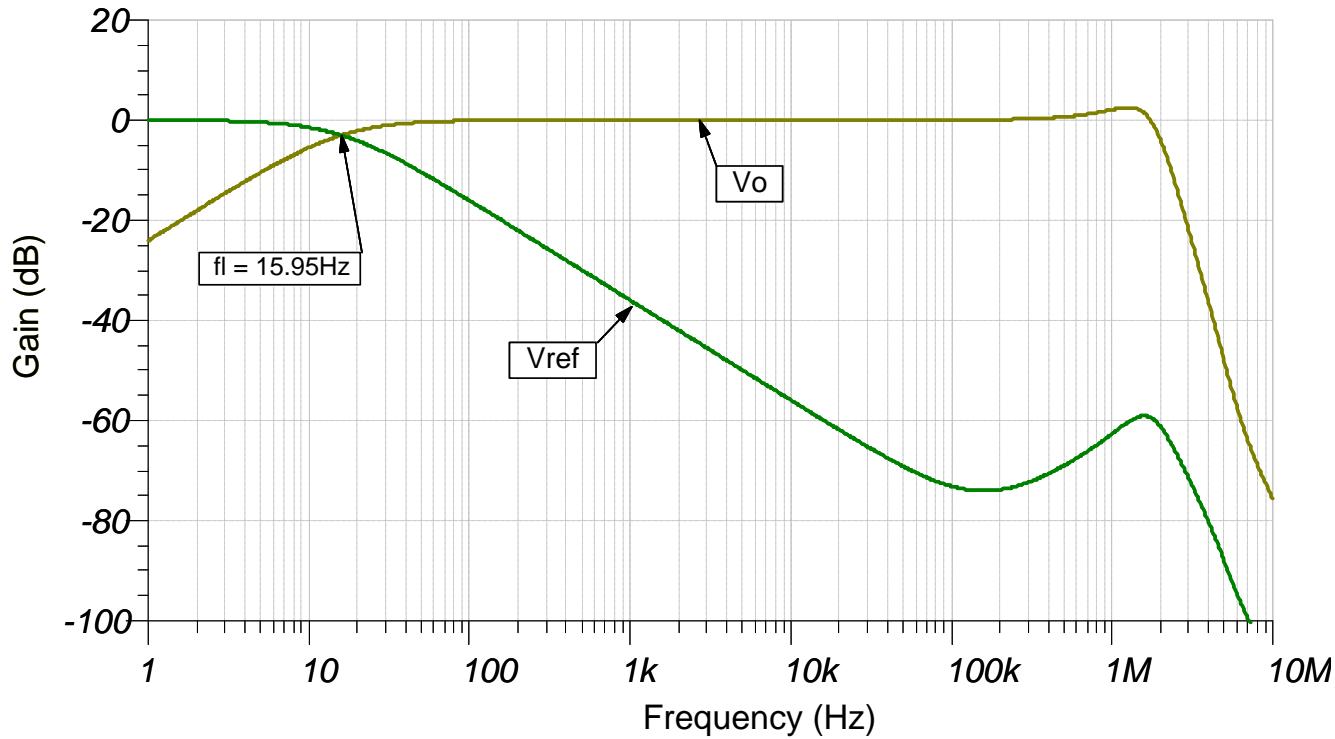
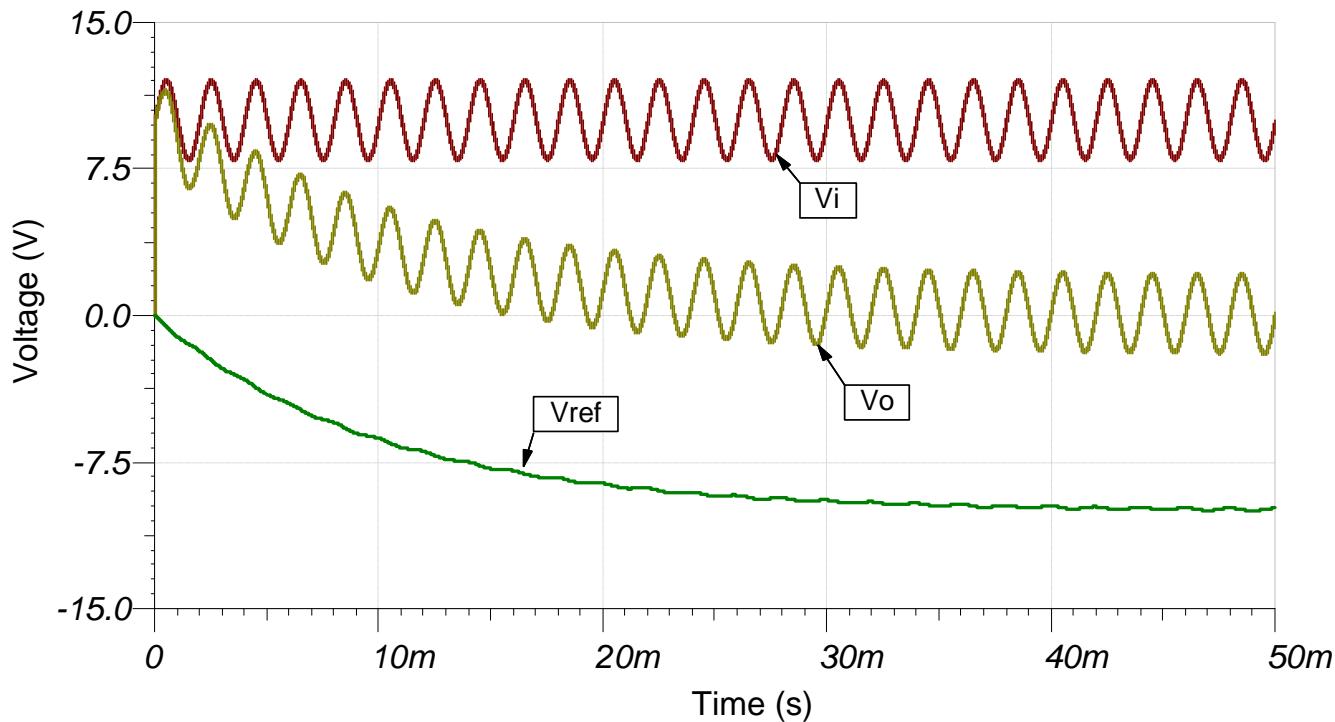
2. Choose a standard value for  $R_1$  and  $C_1$ .

$$C_1 = 100 \text{ nF}$$

$$R_1 = \frac{1}{2\pi \times 100 \text{ nF} \times 16 \text{ Hz}} = 99.47 \text{ k}\Omega \approx 100 \text{ k}\Omega \text{ (standard value)}$$

3. The DC rejection capabilities of the circuit will degrade with gain. The following table provides a good estimate of the DC correction range for higher gains.

Gain	DC Correction Range
1V/V	$\pm 10V$
10V/V	$\pm 1V$
100V/V	$\pm 0.1V$
1000V/V	$\pm 0.01V$

**Design Simulations**
**AC Simulation Results**

**Transient Simulation Results**


## Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See TINA-TI™ circuit simulation file, [SBOMAU0](#).

See TIPD191, <http://www.ti.com/tool/tipd191>.

## Design Featured Instrumentation Amplifier

INA828	
$V_{ss}$	4.5V to 36V
$V_{inCM}$	$V_{ee}+2V$ to $V_{cc}-2V$
$V_{out}$	$V_{ee}+150mV$ to $V_{cc}-150mV$
$V_{os}$	20 $\mu$ V
$I_q$	600 $\mu$ A
$I_b$	150pA
<b>UGBW</b>	2MHz
<b>SR</b>	1.2V/ $\mu$ s
<b>#Channels</b>	1
<a href="http://www.ti.com/product/INA828">www.ti.com/product/INA828</a>	

## Design Featured Op Amp

OPA188	
$V_{ss}$	8V to 36V
$V_{inCM}$	$V_{ee}$ to $V_{cc}-1.5V$
$V_{out}$	Rail-to-rail
$V_{os}$	6 $\mu$ V
$I_q$	450 $\mu$ A
$I_b$	$\pm 160pA$
<b>UGBW</b>	2MHz
<b>SR</b>	0.8V/ $\mu$ s
<b>#Channels</b>	1,2,4
<a href="http://www.ti.com/product/OPA188">www.ti.com/product/OPA188</a>	

## Design Alternate Op Amp

TLV171	
$V_{ss}$	2.7V to 36V
$V_{inCM}$	$V_{ee}-0.1V$ to $V_{cc}-2V$
$V_{out}$	Rail-to-rail
$V_{os}$	750 $\mu$ V
$I_q$	525 $\mu$ A
$I_b$	$\pm 10pA$
<b>UGBW</b>	3MHz
<b>SR</b>	1.5V/ $\mu$ s
<b>#Channels</b>	1,2,4
<a href="http://www.ti.com/product/OPA188">www.ti.com/product/OPA188</a>	

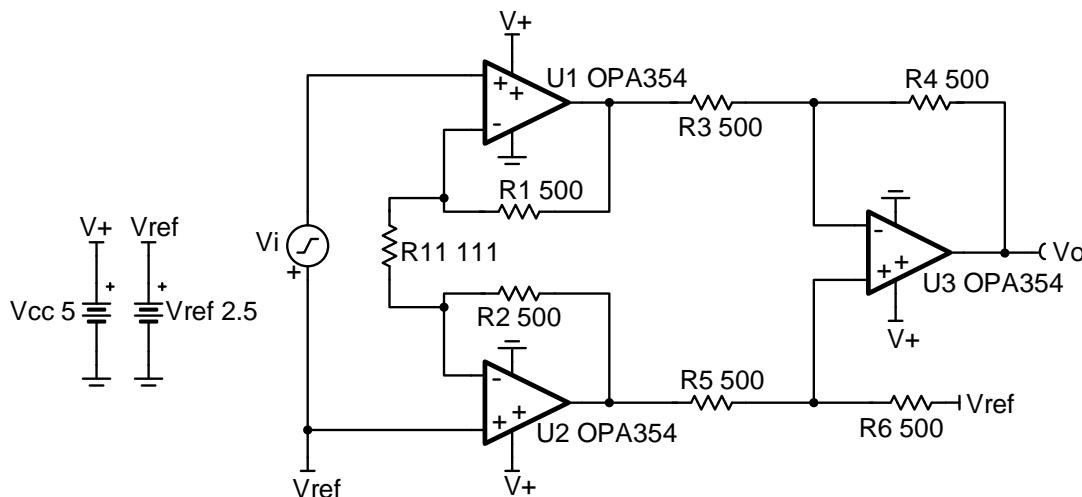
## Discrete wide bandwidth INA circuit

### Design Goals

Input		Output		Bandwidth	Supply		
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	BW	$V_{cc}$	$V_{ee}$	$V_{ref}$
-0.24V	+0.24V	+0.1V	+4.9V	10MHz	+2.5V	0V	2.5V

### Design Description

This design uses 3 op-amps to build a discrete wide bandwidth instrumentation amplifier. The circuit converts a differential, high frequency signal to a single-ended output.



### Design Notes

1. Reduce the capacitance on the output of each op amp to avoid stability issues.
2. Use low gain configurations to maximize the bandwidth of the circuit.
3. Use precision resistors to achieve high DC CMRR performance.
4. Use small resistors in op-amp feedback to maintain stability.
5. Set the reference voltage,  $V_{ref}$ , at mid-supply to allow the output to swing to both supply rails.
6. Phase margin of 45° or greater is required for stable operation.
7.  $R_{11}$  sets the gain of the instrumentation amplifier.
8. Linear operation depends upon the input common-mode and the output swing ranges of the discrete op amps used. The linear output swing ranges are specified under the  $A_{ol}$  test conditions in the op amps datasheets.
9.  $V_{ref}$  also sets the common-mode voltage of the input,  $V_i$ , to ensure linear operation.

### Design Steps

1. The transfer function of the circuit is given below.

$$V_o = V_i \times \left(1 + \frac{2 \times R_1}{R_{11}}\right) \times \left(\frac{R_6}{R_5}\right) + V_{ref}$$

where  $V_i$  = the differential input voltage

$V_{ref}$  = the reference voltage provided to the amplifier

$$\text{Gain} = \left(1 + \frac{2 \times R_1}{R_{11}}\right) \times \frac{R_6}{R_5}$$

2. To maximize the usable bandwidth of design, set the gain of the diff amp stage to 1V/V. Use smaller value resistors to minimize noise.

Choose  $R_3 = R_4 = R_5 = R_6 = 500\Omega$  (Standard value)

3. Choose values for resistors  $R_1$  and  $R_2$ . Keep these values low to minimize noise.

$R_1 = R_2 = 500\Omega$  (Standard value)

4. Calculate resistor  $R_{11}$  to set the gain of the circuit to 10V/V

$$G = \left(1 + \frac{2 \times R_1}{R_{11}}\right) = 10 \frac{V}{V} \rightarrow 1 + \frac{2 \times 500\Omega}{R_{11}} = 10 \frac{V}{V} \rightarrow \frac{2 \times 500\Omega}{R_{11}} = 9 \frac{V}{V}$$

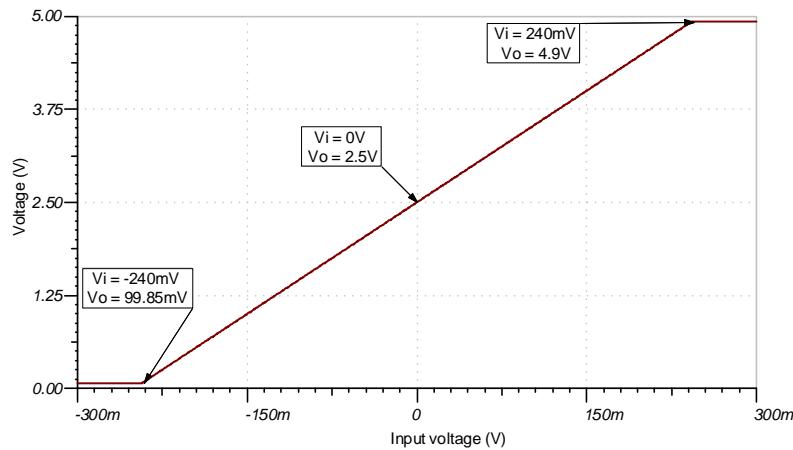
$$R_{11} = \frac{1000\Omega}{9 \frac{V}{V}} = 111.11\Omega \rightarrow R_{11} = 111\Omega \text{ (Standard value)}$$

5. Calculate the reference voltage to bias the input to mid-supply. This will maximize the linear output swing of the instrumentation amplifier. See References for more information on the linear operating region of instrumentation amplifiers.

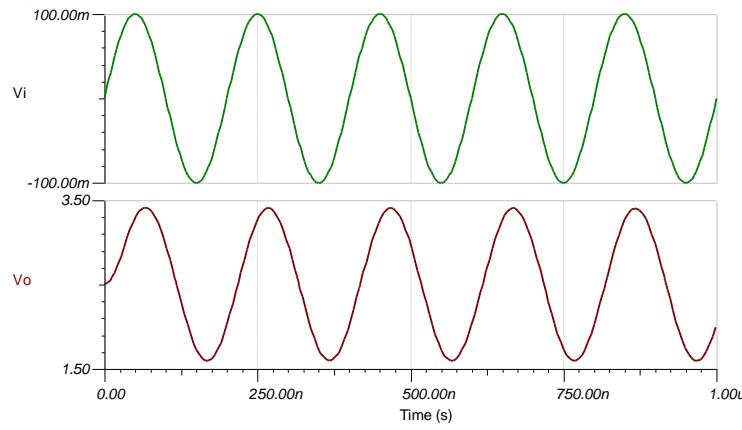
$$V_{ref} = \frac{V_s}{2} = \frac{5V}{2} = 2.5V$$

## Design Simulations

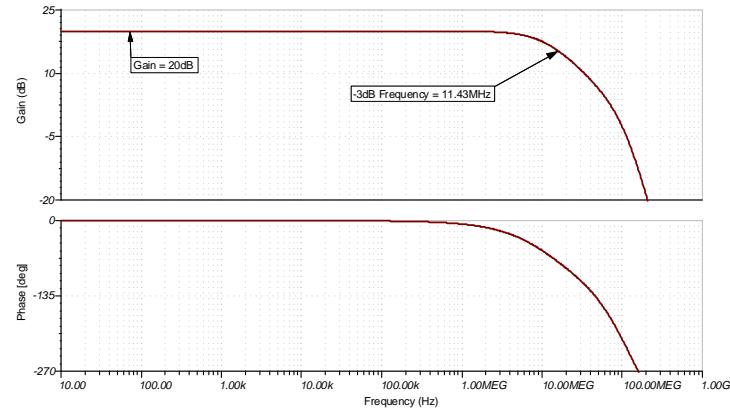
### DC Simulation Results



### Transient Simulation Results



### AC Simulation Results



## References

1. [Analog Engineer's Circuit Cookbooks](#)
2. [SPICE Simulation File SBOMAU6](#)
3. [TI Precision Labs](#)
4. [Instrumentation Amplifier  \$V\_{CM}\$  vs.  \$V\_{OUT}\$  Plots](#)
5. [Common-mode Range Calculator for Instrumentation Amplifiers](#)

## Design Featured Op Amp

OPA354	
$V_{ss}$	2.5V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	2mV
$I_q$	4.9mA/Ch
$I_b$	3pA
<b>UGBW</b>	250MHz
<b>SR</b>	150V/ $\mu$ s
<b>#Channels</b>	1,2,4
<a href="http://www.ti.com/product/opa354">www.ti.com/product/opa354</a>	

## Design Alternate Op Amp

OPA322	
$V_{ss}$	1.8V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	500 $\mu$ V
$I_q$	1.6mA/Ch
$I_b$	0.2pA
<b>UGBW</b>	20MHz
<b>SR</b>	10V/ $\mu$ s
<b>#Channels</b>	1,2,4
<a href="http://www.ti.com/product/opa322">www.ti.com/product/opa322</a>	

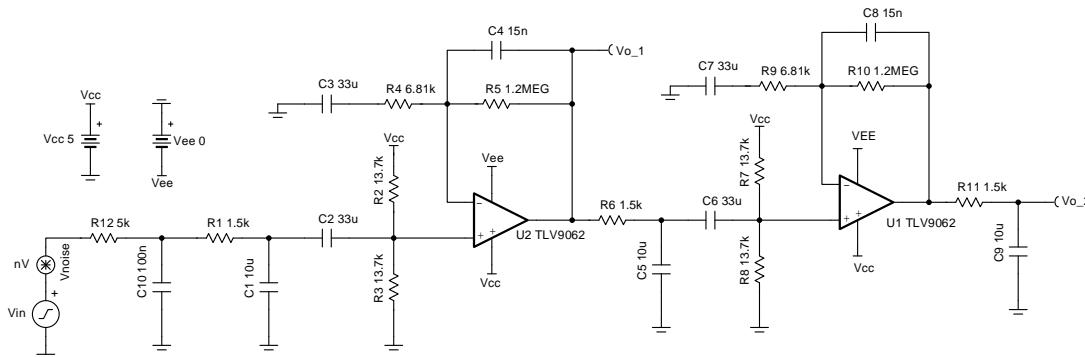
## Low-noise and long-range PIR sensor conditioner circuit

### Design Goals

AC Gain	Filter Cut Off Frequency		Supply	
90dB	$f_L$	$f_H$	$V_{cc}$	$V_{ee}$
	0.7Hz	10Hz	5V	0V

### Design Description

This two stage amplifier design amplifies and filters the signal from a passive infrared (PIR) sensor. The circuit includes multiple low-pass and high-pass filters to reduce noise at the output of the circuit to be able to detect motion at long distances and reduce false triggers. This circuit can be followed by a window comparator circuit to create a digital output or connect directly to an analog-to-digital converter (ADC) input.



### Design Notes

1. The common mode voltage and output bias voltage are set using the resistor dividers between  $R_2$  and  $R_3$  (and  $R_7$  and  $R_8$ ).
2. Two or more amplifier stages must be used to allow for sufficient loop gain.
3. Additional low-pass and high-pass filters can be added to further reduce noise.
4. Capacitors  $C_4$  and  $C_8$  filter noise by decreasing the bandwidth of the circuit and help stabilize the amplifiers.
5. RC filters on the output of the amplifiers (for example,  $R_6$  and  $C_5$ ) are required to reduce the total integrated noise of the amplifier.
6. The maximum gain of the circuit can be affected by the cutoff frequencies of the filters. The cutoff frequencies may need to be adjusted to achieve the desired gain.

### Design Steps

1. Choose large-valued capacitors  $C_1$ ,  $C_5$ , and  $C_9$  for the low-pass filters. These capacitors should be selected first since large-valued capacitors have limited standard values to select from compared to standard resistor values.

$$C_1 = C_5 = C_9 = 10\mu F$$

2. Calculate resistor values for  $R_1$ ,  $R_6$ , and  $R_{11}$  to form the low-pass filters.

$$R_1 = R_6 = R_{11} = \frac{1}{2\pi \times f_L \times C_1} = \frac{1}{2\pi \times 0.7\text{Hz} \times 10\mu F} = 1.592k\Omega$$

Choose  $R_1 = R_6 = R_{11} = 1.5k\Omega$  (Standard value)

3. Select capacitor values for  $C_2$ ,  $C_3$ ,  $C_6$ , and  $C_7$  for the high-pass filters.

$$C_2 = C_3 = C_6 = C_7 = 33\mu F$$

4. Calculate the resistor values for  $R_4$  and  $R_9$  for the high-pass filters.

$$R_4 = R_9 = \frac{1}{2\pi \times f_H \times C_2} = \frac{1}{2\pi \times 10\text{Hz} \times 33\mu F} = 6.89k\Omega$$

Choose  $R_4 = R_9 = 6.81k\Omega$  (Standard value)

5. Set the common-mode voltage of the amplifier to mid-supply using a voltage divider. The equivalent resistance of the voltage divider should be equal to  $R_4$  to properly set the corner frequency of the high-pass filter.

$$R_2 = R_3 = R_7 = R_8 = 2 \times R_4 = 2 \times 6.81k\Omega = 13.62k\Omega$$

Choose  $R_2 = R_3 = R_7 = R_8 = 13.7k\Omega$  (Standard value)

6. Calculate the gain required by each gain stage to achieve the total gain requirement. Distribute the total gain target of the circuit evenly between both gain stages.

$$\text{Gain} = \frac{90\text{dB}}{2} = 45\text{dB} = 177.828\frac{\text{V}}{\text{V}}$$

7. Calculate  $R_5$  to set the gain of the first stage.

$$R_5 = (\text{Gain} - 1) \times R_4 = (177.828\frac{\text{V}}{\text{V}} - 1) \times 6.81k\Omega = 1.204M\Omega$$

Choose  $1.2M\Omega$

8. Calculate  $C_4$  to set the low-pass filter cut off frequency.

$$C_4 = \frac{1}{2\pi \times R_5 \times f_L} = \frac{1}{2\pi \times 1.2M\Omega \times 10\text{Hz}} = 13.263nF$$

Choose  $C_4 = 15nF$

9. Since the gain and cut off frequency of the first gain stage is equal to the second gain stage, set all component values of both stages equal to each other.

$$R_1 = R_6 = 5k\Omega$$

$$R_7 = R_8 = 13.7k\Omega$$

$$R_9 = R_4 = 6.81k\Omega$$

$$R_{10} = R_5 = 1.2M\Omega$$

$$C_8 = C_4 = 15nF$$

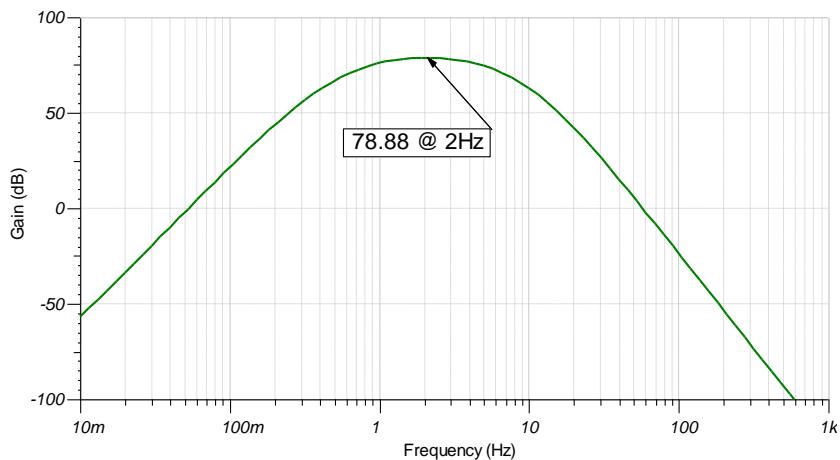
10. Calculate  $R_{11}$  to set the cut off frequency of the low-pass filter at the output of the circuit.

$$R_{11} = \frac{1}{2\pi \times C_9 \times f_L} = \frac{1}{2\pi \times 10\mu F \times 10\text{Hz}} = 1.592k\Omega$$

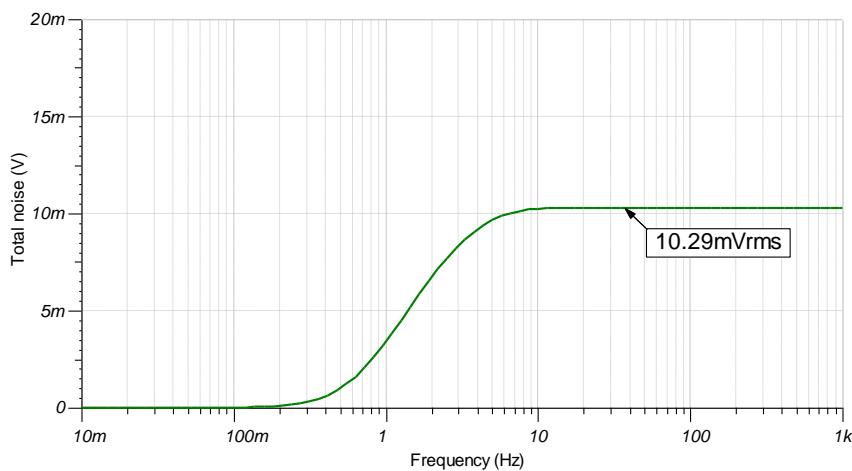
Choose  $R_{11} = 1.5k\Omega$

## Design Simulations

### AC Simulation Results



### Noise Simulation Results



**References:**

1. [Analog Engineer's Circuit Cookbooks](#)
2. [SPICE Simulation File SBOC524](#)
3. [TI Precision Labs](#)

**Design Featured Op Amp**

TLV9062	
$V_{ss}$	1.8V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	0.3mV
$I_q$	538 $\mu$ A
$I_b$	0.5pA
<b>UGBW</b>	10MHz
<b>SR</b>	6.5V/ $\mu$ s
<b>#Channels</b>	1,2,4
<a href="http://www.ti.com/product/tlv9062">www.ti.com/product/tlv9062</a>	

**Design Alternate Op Amp**

OPA376	
$V_{ss}$	2.2V to 5.5V
$V_{inCM}$	$V_{ee}$ to $V_{cc}$ -1.3V
$V_{out}$	Rail-to-rail
$V_{os}$	5 $\mu$ V
$I_q$	760 $\mu$ A/Ch
$I_b$	0.2pA
<b>UGBW</b>	5.5MHz
<b>SR</b>	2V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/opa376">http://www.ti.com/product/opa376</a>	

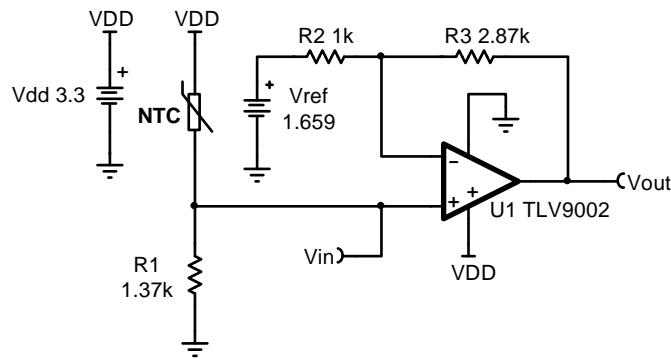
## Temperature sensing with NTC circuit

### Design Goals

Temperature		Output Voltage		Supply		
T <sub>Min</sub>	T <sub>Max</sub>	V <sub>outMin</sub>	V <sub>outMax</sub>	V <sub>dd</sub>	V <sub>ee</sub>	V <sub>ref</sub>
25 °C	50 °C	0.05V	3.25V	3.3V	0V	1.659V

### Design Description

This temperature sensing circuit uses a resistor in series with a negative-temperature-coefficient (NTC) thermistor to form a voltage divider, which has the effect of producing an output voltage that is linear over temperature. The circuit uses an op amp in a non-inverting configuration with inverting reference to offset and gain the signal, which helps to utilize the full ADC resolution and increase measurement accuracy.



### Design Notes

1. Use the op amp in a linear operating region. Linear output swing is usually specified under the A<sub>OL</sub> test conditions.
2. The connection, Vin, is a positive temperature coefficient output voltage. To correct an NTC output voltage, switch the position of R<sub>1</sub> and the NTC thermistor.
3. R<sub>1</sub> is chosen based on the temperature range and the NTC's value.
4. V<sub>ref</sub> can be created using a DAC or voltage divider. If a voltage divider is used the equivalent resistance of the voltage divider will influence the gain of the circuit.
5. Using high value resistors can degrade the phase margin of the amplifier and introduce additional noise in the circuit. It is recommended to use resistor values around 10 kΩ or less.
6. A capacitor placed in parallel with the feedback resistor will limit bandwidth, improve stability and help reduce noise.

## Design Steps

$$V_{out} = V_{dd} \times \frac{R_1}{R_{NTC} + R_1} \times \frac{R_2 + R_3}{R_2} - \frac{R_3}{R_2} \times V_{ref}$$

1. Calculate the value of  $R_1$  to produce a linear output voltage. Use the minimum and maximum values of the PTC to obtain a range of values for  $R_1$ .

$$R_{NTC\_max} = R_{NTC @ 25^\circ C} = 2.252 \text{ k}\Omega, \quad R_{NTC\_min} = R_{NTC @ 50^\circ C} = 819.7 \text{ }\Omega$$

$$R_1 = \sqrt{R_{NTC @ 25^\circ C} \times R_{NTC @ 50^\circ C}} = \sqrt{2.252 \text{ k}\Omega \times 819.7 \text{ }\Omega} = 1.359 \text{ k}\Omega \approx 1.37 \text{ k}\Omega$$

2. Calculate the input voltage range.

$$V_{inMin} = V_{dd} \times \frac{R_1}{R_{NTC\_max} + R_1} = 3.3 \text{ V} \times \frac{1.37 \text{ k}\Omega}{2.252 \text{ k}\Omega + 1.37 \text{ k}\Omega} = 1.248 \text{ V}$$

$$V_{inMax} = V_{dd} \times \frac{R_1}{R_{NTC\_min} + R_1} = 3.3 \text{ V} \times \frac{1.37 \text{ k}\Omega}{819.7 \text{ }\Omega + 1.37 \text{ k}\Omega} = 2.065 \text{ V}$$

3. Calculate the gain required to produce the maximum output swing.

$$G_{ideal} = \frac{V_{outMax} - V_{outMin}}{V_{inMax} - V_{inMin}} = \frac{3.25 \text{ V} - 0.05 \text{ V}}{2.065 \text{ V} - 1.248 \text{ V}} = 3.917 \frac{\text{V}}{\text{V}}$$

4. Select  $R_2$  and calculate  $R_3$  to set the gain in Step 3.

$$\text{Gain} = \frac{R_2 + R_3}{R_2}$$

$$R_2 = 1 \text{ k}\Omega \text{ (Standard value)}$$

$$R_3 = R_2 \times (G_{ideal} - 1) = 1 \text{ k}\Omega \times (3.917 \frac{\text{V}}{\text{V}} - 1) = 2.917 \text{ k}\Omega$$

$$\text{Choose } R_3 = 2.87 \text{ k}\Omega \text{ (Standard value)}$$

5. Calculate the actual gain based on standard values of  $R_2$  and  $R_3$ .

$$G_{actual} = \frac{R_2 + R_3}{R_2} = \frac{1 \text{ k}\Omega + 2.87 \text{ k}\Omega}{1 \text{ k}\Omega} = 3.87 \frac{\text{V}}{\text{V}}$$

6. Calculate the output voltage swing based on the actual gain.

$$V_{out\_swing} = (V_{inMax} - V_{inMin}) \times G_{actual} = (2.065 \text{ V} - 1.248 \text{ V}) \times 3.87 \frac{\text{V}}{\text{V}} = 3.162 \text{ V}$$

7. Calculate the maximum output voltage when the output voltage is symmetrical around mid-supply.

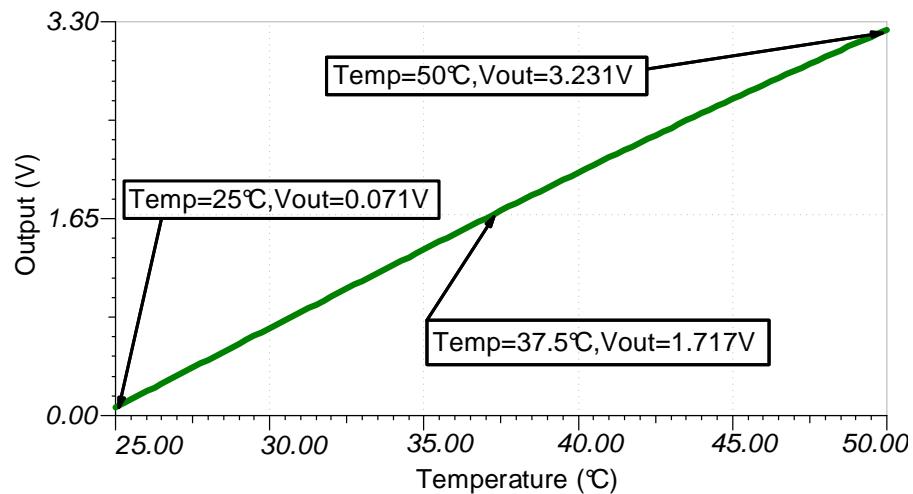
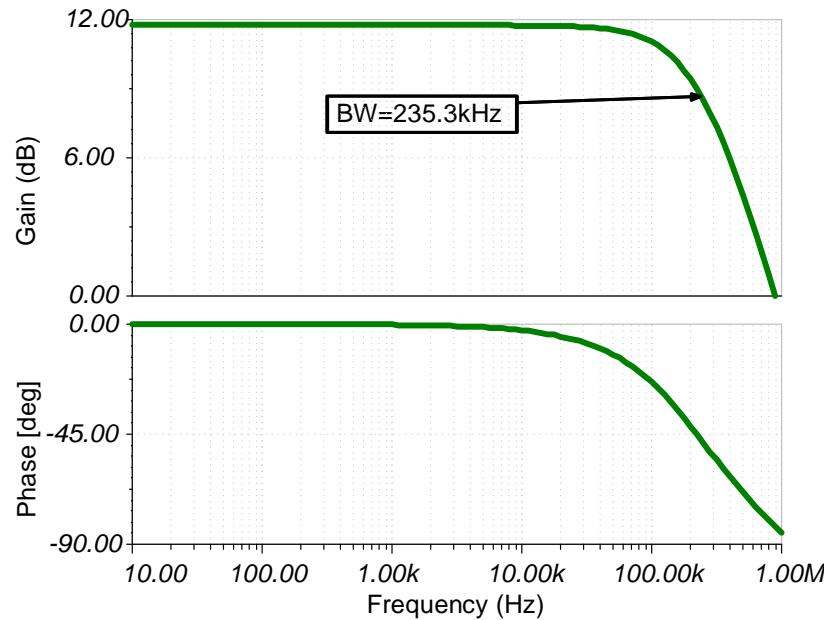
$$V_{outMax} = V_{mid-supply} + \frac{V_{out\_swing}}{2} = \frac{V_{dd} - V_{ee}}{2} + \frac{V_{out\_swing}}{2} = \frac{3.3 \text{ V} - 0 \text{ V}}{2} + \frac{3.162 \text{ V}}{2} = 3.231 \text{ V}$$

8. Calculate the reference voltage.

$$V_{outMax} = V_{inMax} \times G_{actual} - \frac{R_3}{R_2} \times V_{ref}$$

$$3.231 \text{ V} = 2.065 \text{ V} \times 3.87 \frac{\text{V}}{\text{V}} - \frac{2.87 \text{ k}\Omega}{1 \text{ k}\Omega} \times V_{ref}$$

$$V_{ref} = \frac{2.065 \text{ V} \times 3.87 \frac{\text{V}}{\text{V}} - 3.231 \text{ V}}{\frac{2.87 \text{ k}\Omega}{1 \text{ k}\Omega}} = 1.659 \text{ V}$$

**Design Simulations****DC Transfer Results****AC Simulation Results**

**References:**

1. [Analog Engineer's Circuit Cookbooks](#)
2. [SPICE Simulation File SBOMAV6](#)
3. [TI Precision Labs](#)

**Design Featured Op Amp:**

TLV9002	
$V_{cc}$	1.8 V to 5.5 V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	1.5mV
$I_q$	0.06mA
$I_b$	5pA
<b>UGBW</b>	1MHz
<b>SR</b>	2V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/TLV9002">http://www.ti.com/product/TLV9002</a>	

**Design Alternate Op Amp:**

OPA333	
$V_{cc}$	1.8 V to 5.5 V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	2 $\mu$ V
$I_q$	17 $\mu$ A
$I_b$	70pA
<b>UGBW</b>	350kHz
<b>SR</b>	0.16V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/OPA333">http://www.ti.com/product/OPA333</a>	

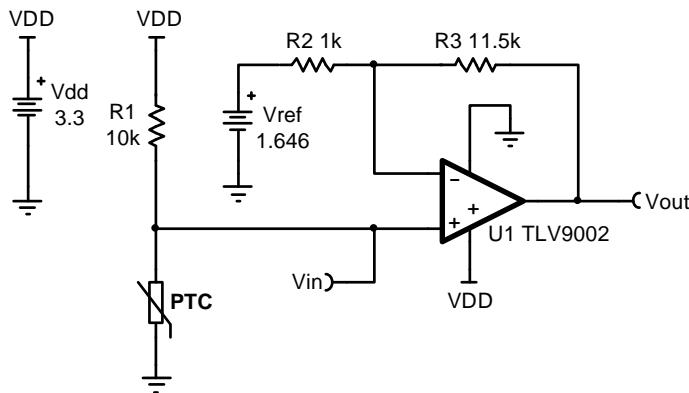
## Temperature sensing with PTC circuit

### Design Goals

Temperature		Output voltage		Supply		
T <sub>Min</sub>	T <sub>Max</sub>	V <sub>outMin</sub>	V <sub>outMax</sub>	V <sub>dd</sub>	V <sub>ee</sub>	V <sub>ref</sub>
0 °C	50 °C	0.05V	3.25V	3.3V	0V	1.646V

### Design Description

This temperature sensing circuit uses a resistor in series with a positive-temperature-coefficient (PTC) thermistor to form a voltage-divider, which has the effect of producing an output voltage that is linear over temperature. The circuit uses an op amp in a non-inverting configuration with inverting reference to offset and amplify the signal, which helps to utilize the full ADC resolution and increase measurement accuracy.



### Design Notes

1. Use the op amp in a linear operating region. Linear output swing is usually specified under the  $A_{OL}$  test conditions.
2. The connection,  $V_{in}$ , is a positive temperature coefficient output voltage. To correct a negative-temperature-coefficient (NTC) output voltage, switch the position of  $R_1$  and PTC resistor.
3. Choose  $R_1$  based on the temperature range and the PTC's value.
4.  $V_{ref}$  can be created using a DAC or voltage divider. If a voltage divider is used the equivalent resistance of the voltage divider will alter the gain of the circuit and should be accounted for.
5. Using high-value resistors can degrade the phase margin of the amplifier and introduce additional noise in the circuit. It is recommended to use resistor values around  $10k\Omega$  or less.
6. A capacitor placed in parallel with the feedback resistor will limit bandwidth, improve stability and help reduce noise.

## Design Steps

$$V_{out} = V_{dd} \times \frac{R_{PTC}}{R_{PTC} + R_1} \times \frac{R_2 + R_3}{R_2} - \frac{R_3}{R_2} \times V_{ref}$$

1. Calculate the value of  $R_1$  to produce a linear output voltage. Use the minimum and maximum values of the PTC to obtain a range of values for  $R_1$ .

$$R_{PTC\_Max} = R_{PTC} @ 50^\circ C = 11.611 \text{ k}\Omega$$

$$R_{PTC\_Min} = R_{PTC} @ 0^\circ C = 8.525 \text{ k}\Omega$$

$$R_1 = \sqrt{R_{PTC} @ 0^\circ C \times R_{PTC} @ 50^\circ C} = \sqrt{8.525 \text{ k}\Omega \times 11.611 \text{ k}\Omega} = 9.95 \text{ k}\Omega \approx 10 \text{ k}\Omega$$

2. Calculate the input voltage range.

$$V_{inMin} = V_{dd} \times \frac{R_{PTC\_Min}}{R_{PTC\_Min} + R_1} = 3.3 \text{ V} \times \frac{8.525 \text{ k}\Omega}{8.525 \text{ k}\Omega + 10 \text{ k}\Omega} = 1.519 \text{ V}$$

$$V_{inMax} = V_{dd} \times \frac{R_{PTC\_Max}}{R_{PTC\_Max} + R_1} = 3.3 \text{ V} \times \frac{11.611 \text{ k}\Omega}{11.611 \text{ k}\Omega + 10 \text{ k}\Omega} = 1.773 \text{ V}$$

3. Calculate the gain required to produce the maximum output swing.

$$G_{ideal} = \frac{V_{outMax} - V_{outMin}}{V_{inMax} - V_{inMin}} = \frac{3.25 \text{ V} - 0.05 \text{ V}}{1.773 \text{ V} - 1.519 \text{ V}} = 12.598 \frac{\text{V}}{\text{V}}$$

4. Select  $R_2$  and calculate  $R_3$  to set the gain calculated in Step 3.

$$\text{Gain} = \frac{R_2 + R_3}{R_2}$$

$$R_2 = 1 \text{ k}\Omega$$

$$R_3 = R_2 \times (G_{ideal} - 1) = 1 \text{ k}\Omega \times (12.598 - 1) = 11.598 \text{ k}\Omega$$

Choose  $R_3 = 11.5 \text{ k}\Omega$  (Standard value)

5. Calculate the actual gain based on standard values of  $R_2$  and  $R_3$ .

$$G_{actual} = \frac{R_2 + R_3}{R_2} = \frac{1 \text{ k}\Omega + 11.5 \text{ k}\Omega}{1 \text{ k}\Omega} = 12.5 \frac{\text{V}}{\text{V}}$$

6. Calculate the output voltage swing based on the actual gain.

$$V_{out\_swing} = (V_{inMax} - V_{inMin}) \times G_{actual} = (1.773 \text{ V} - 1.519 \text{ V}) \times 12.5 \frac{\text{V}}{\text{V}} = 3.175 \text{ V}$$

7. Calculate the maximum output voltage when the output voltage is symmetrical around mid-supply.

$$V_{outMax} = V_{mid-supply} + \frac{V_{out\_swing}}{2} = \frac{V_{dd} - V_{ee}}{2} + \frac{V_{out\_swing}}{2} = \frac{3.3 \text{ V} - 0 \text{ V}}{2} + \frac{3.175 \text{ V}}{2} = 3.238 \text{ V}$$

8. Calculate the reference voltage.

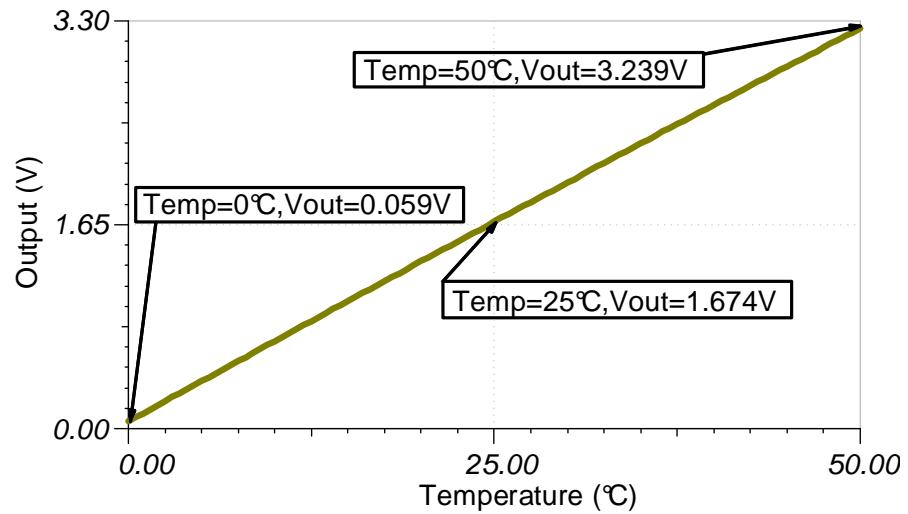
$$V_{outMax} = V_{inMax} \times G_{actual} - \frac{R_3}{R_2} \times V_{ref}$$

$$3.238 \text{ V} = 1.773 \text{ V} \times 12.5 \frac{\text{V}}{\text{V}} - \frac{11.5 \text{ k}\Omega}{1 \text{ k}\Omega} \times V_{ref}$$

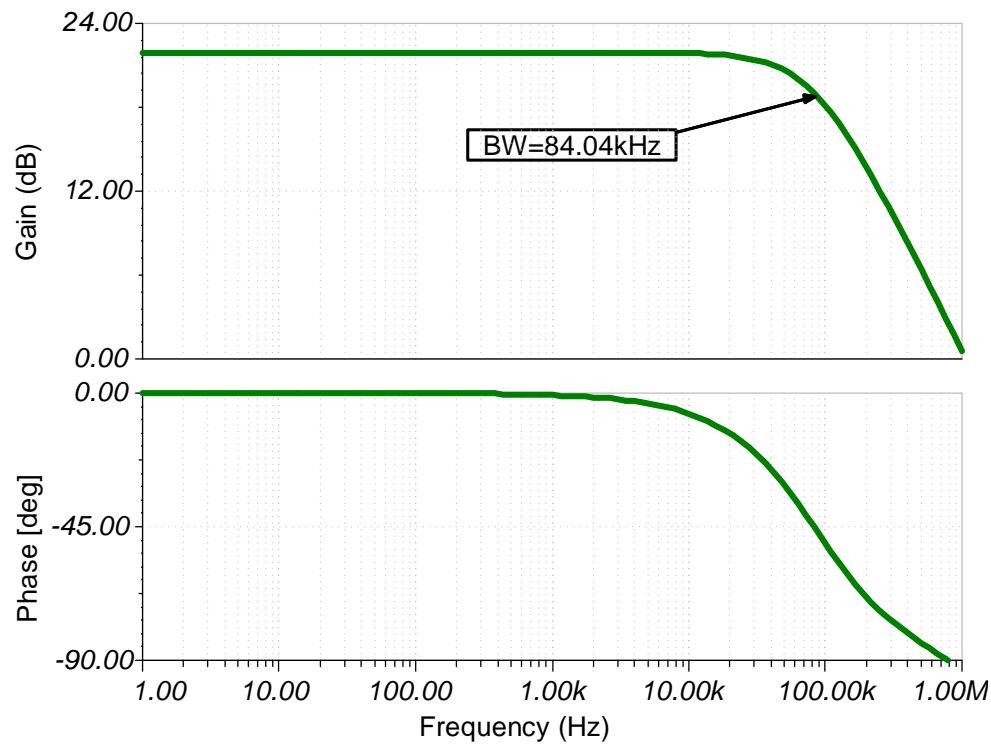
$$V_{ref} = \frac{1.773 \text{ V} \times 12.5 \frac{\text{V}}{\text{V}} - 3.238 \text{ V}}{\frac{11.5 \text{ k}\Omega}{1 \text{ k}\Omega}} = 1.646 \text{ V}$$

**Design Simulations**

**DC Transfer Results**



**AC Simulation Results**



**References:**

1. [Analog Engineer's Circuit Cookbooks](#)
2. SPICE Simulation File [SBOMAV5](#)
3. [TI Precision Labs](#)

**Design Featured Op Amp**

TLV9002	
$V_{cc}$	1.8 V to 5.5 V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	1.5mV
$I_q$	0.06mA
$I_b$	5pA
<b>UGBW</b>	1MHz
<b>SR</b>	2V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/TLV9002">http://www.ti.com/product/TLV9002</a>	

**Design Alternate Op Amp**

OPA333	
$V_{cc}$	1.8 V to 5.5 V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	2 $\mu$ V
$I_q$	17 $\mu$ A
$I_b$	70pA
<b>UGBW</b>	350kHz
<b>SR</b>	0.16V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/OPA333">http://www.ti.com/product/OPA333</a>	

## ***Differential input to differential output circuit using a fully-differential amplifier***

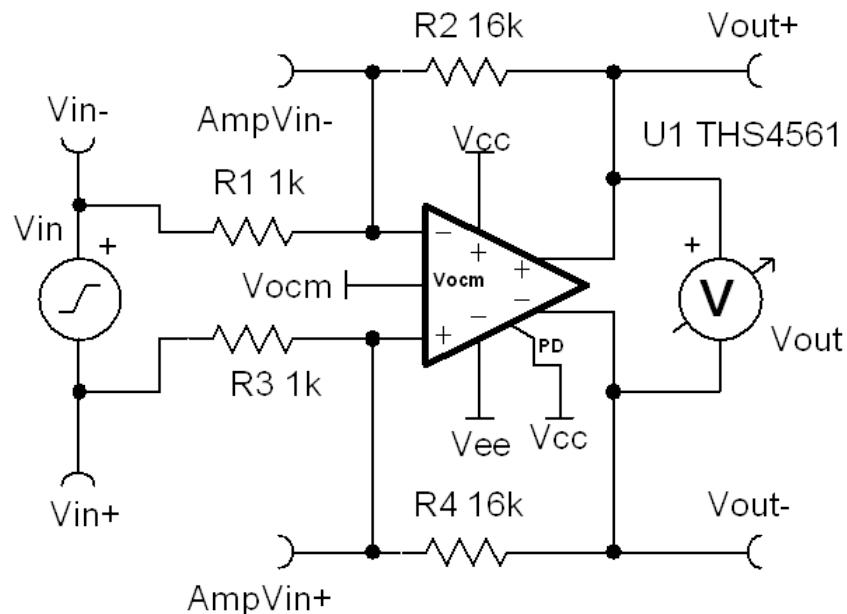
### **Design Goals**

Input	Output	Supply	
Differential	Differential	$V_{cc}$	$V_{ee}$
1Vpp	16Vpp	10V	0V

Output Common-Mode	3dB Bandwidth	AC Gain (Gac)
5V	3MHz	16V/V

### **Design Description**

This design uses a fully differential amplifier (FDA) as a differential input to differential output amplifier.



**Design Notes**

1. The ratio  $R_2/R_1$ , equal to  $R_4/R_3$ , sets the gain of the amplifier.
2. For a given supply, the output swing for a FDA is twice that of a single ended amplifier. This is because a fully differential amplifier swings both terminals of the output, instead of swinging one and fixing the other to either ground or a  $V_{ref}$ . The minimum voltage of an FDA is therefore achieved when  $V_{out+}$  is held at the negative rail and  $V_{out-}$  is held at the positive rail, and the maximum is achieved when  $V_{out+}$  is held at the positive rail and  $V_{out-}$  is held at the negative rail.
3. FDAs are useful for noise sensitive signals, since noise coupling equally into both inputs will not be amplified, as is the case in a single ended signal referenced to ground.
4. The output voltages will be centered about the output common-mode voltage set by  $V_{ocm}$ .
5. Both feedback paths should be kept symmetrical in layout.

### Design Steps

- Set the ratio  $R_2/R_1$  to select the AC voltage gain. To keep the feedback paths balanced,  
 $R_1 = R_3 = 1\text{k}\Omega$  (Standard Value)
- $R_2 = R_4 = R_1 \cdot (G_{AC}) = 1\text{k}\Omega \cdot \left(16 \frac{V}{V}\right) = 16\text{k}\Omega$  (Standard Value)
- Given the output rails of 9.8V and 0.2V for  $V_s = 10\text{V}$ , verify that 16Vpp falls within the output range available for  $V_{ocm} = 5\text{V}$ .

In normal operation:

$$\text{Amp}V_{IN+} = \text{Amp}V_{IN-}$$

$$V_{OUT+} - V_{ocm} = V_{ocm} - V_{OUT-}$$

$$V_{OUT} = V_{OUT+} - V_{OUT-}$$

- Rearrange to solve for each output voltage in edge conditions

$$V_{OUT-} = 2V_{ocm} - V_{OUT+}$$

$$V_{OUT-} = V_{OUT+} - V_{OUT}$$

$$2V_{OUT+} = 2V_{ocm} + V_{OUT}$$

$$V_{OUT+} = V_{ocm} + \frac{V_{OUT}}{2}$$

$$V_{OUT-} = V_{ocm} - \frac{V_{OUT}}{2}$$

- Verifying for  $V_{OUT} = +8\text{V}$  and  $V_{ocm} = +5\text{V}$ ,

$$V_{OUT+} = 5 + \frac{8}{2} = 9\text{V} < 9.8\text{V}$$

$$V_{OUT-} = 5 - \frac{8}{2} = 1\text{V} > 0.2\text{V}$$

- Verifying for  $V_{OUT} = -8\text{V}$  and  $V_{ocm} = +5\text{V}$ ,

$$V_{OUT+} = 5 + \frac{-8}{2} = 1\text{V} > 0.2\text{V}$$

$$V_{OUT-} = 5 - \frac{-8}{2} = 9\text{V} > 9.8\text{V}$$

Note that the maximum swing possible is:

$$(9.8V - 0.2V) - (0.2V - 9.8V) = 18.4V_{DD}, \text{ or } \pm 9.4V$$

- Use the input common mode voltage range of the amplifier and the feedback resistor divider to find the signal input range when the output range is 1V to 9V. Due to symmetry, calculation of one side is sufficient.

$$\text{Min}(\text{Amp}V_{IN+}) = \text{Min}(\text{Amp}V_{IN-}) = V_{ee} - 0.1V = -0.1V$$

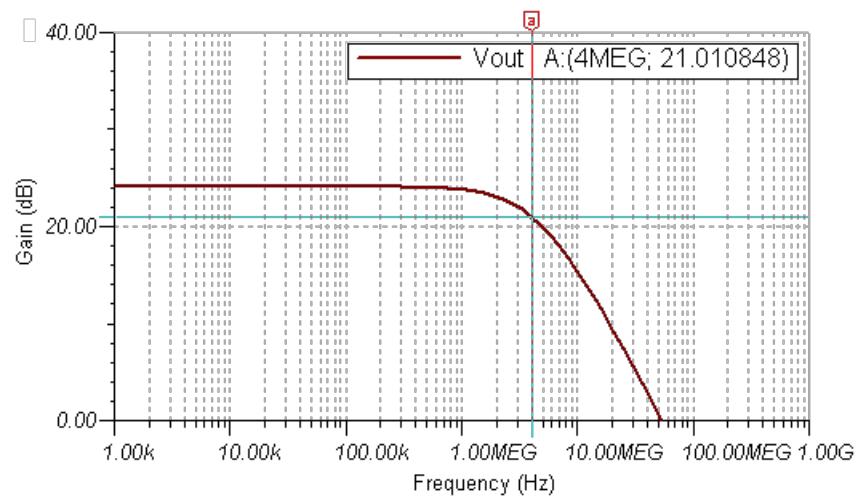
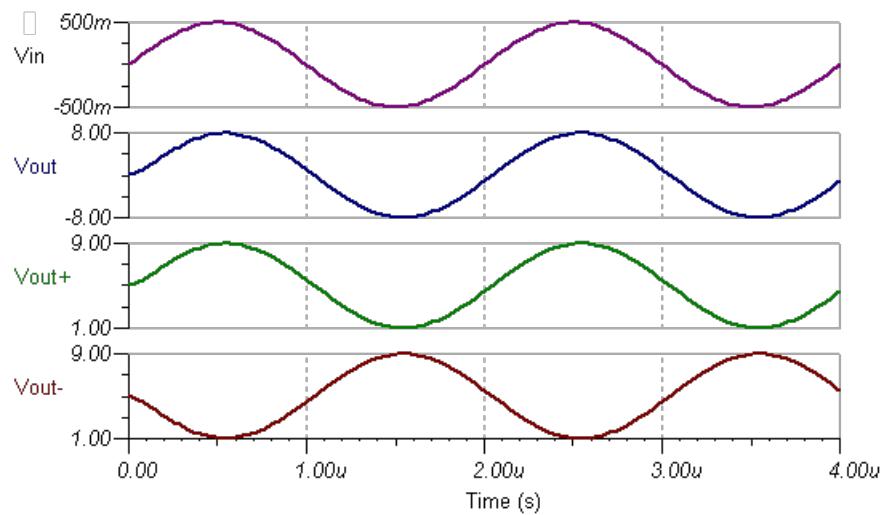
$$\text{Max}(\text{Amp}V_{IN+}) = \text{Max}(\text{Amp}V_{IN-}) = V_{cc} - 1.1V = 8.9V$$

$$\frac{\text{Amp}V_{IN-} - V_{IN-}}{R_1} = \frac{V_{OUT+} - \text{Amp}V_{IN-}}{R_2}$$

$$V_{IN-} = \text{Amp}V_{IN-} - \frac{V_{OUT+} - \text{Amp}V_{IN-}}{\frac{R_2}{R_1}}$$

$$\text{Min}(V_{IN-}) = -0.1V - \frac{9V - (-0.1V)}{16 \frac{V}{V}} = -0.65V$$

$$\text{Max}(V_{IN-}) = 8.9V + \frac{8.9V - 1V}{16 \frac{V}{V}} = 9.4V$$

**Design Simulations****AC Simulation Results****Transient Simulation Results**

## Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See the [TIDA-01036](#) tool folder for more information.

## Design Featured Op Amp

THS4561	
$V_{ss}$	3V to 13.5V
$V_{inCM}$	Vee-0.1V to Vcc-1.1V
$V_{out}$	Vee+0.2V to Vcc-0.2
$V_{os}$	TBD
$I_q$	TBD
$I_b$	TBD
<b>UGBW</b>	70MHz
<b>SR</b>	4.4V/ $\mu$ s
<b>#Channels</b>	1
<a href="http://www.ti.com/product/THS4561">http://www.ti.com/product/THS4561</a>	

## Design Alternate Op Amp

THS4131	
$V_{ss}$	5V to 33V
$V_{inCM}$	Vee+1.3V to Vcc-0.1V
$V_{out}$	Varies
$V_{os}$	2mV
$I_q$	14mA
$I_b$	2uA
<b>UGBW</b>	80MHz
<b>SR</b>	52V/ $\mu$ s
<b>#Channels</b>	1
<a href="http://www.ti.com/product/THS4131">http://www.ti.com/product/THS4131</a>	

## ***Single-ended input to differential output circuit using a fully-differential amplifier***

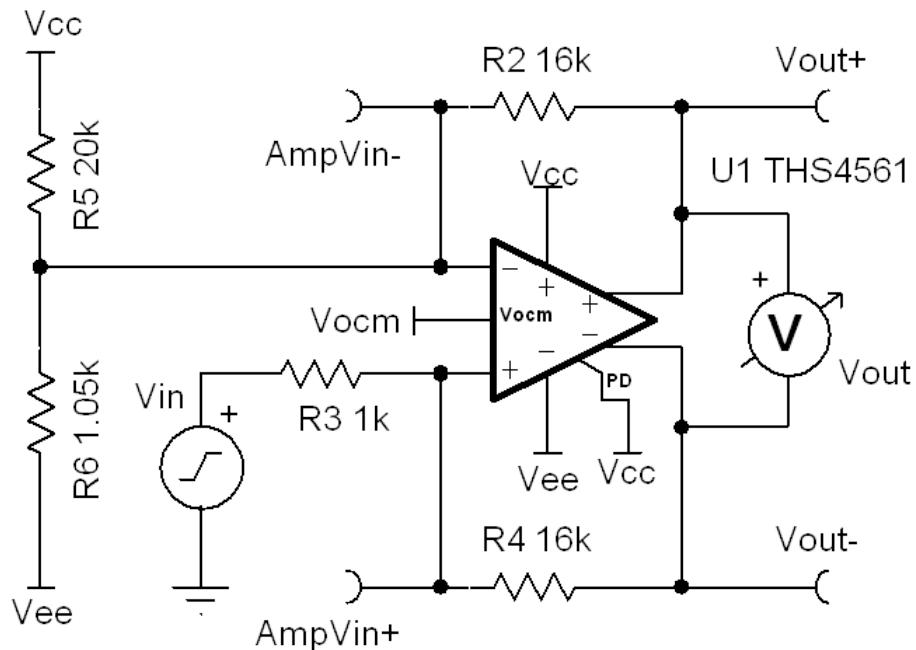
### **Design Goals**

Input	Output	Supply	
Single-Ended	Differential	$V_{cc}$	$V_{ee}$
0V to 1V	16Vpp	10V	0V

Output Common-Mode	3dB Bandwidth	AC Gain (Gac)
5V	3MHz	16V/V

### **Design Description**

This design uses a fully-differential amplifier (FDA) as a single-ended input to differential output amplifier.



### Design Notes

1. The ratio  $R_4/R_3$ , equal to  $R_2/(R_5||R_6)$ , sets the gain of the amplifier.
2. The main difference between a single-ended input and a differential input is that the available input swing is only half. This is because one of the input voltages is fixed at a reference.
3. It is recommended to set this reference to mid-input signal range, rather than the min-input, to induce polarity reversal in the measured differential input. This preserves the ability of the outputs to crossover, which provides the doubling of output swing possible with an FDA.
4. The impedance of the reference voltage must be equal to the signal input resistor. This can be done by creating a resistor divider with a Thevenin equivalent of the correct reference voltage and impedance.

### Design Steps

- Find the resistor divider with that produces a 0.5V, 1-kΩ reference from  $V_s = 10V$ .

$$\frac{R_6}{R_5 + R_6} = F \quad \frac{0.5V}{10V} \quad \frac{R_5 \cdot R_6}{R_5 + R_6} = E = 1k\Omega$$

$$R_6 = FR_5 + FR_6$$

$$R_6(1-F) = FR_5$$

$$R_5 = \frac{R_6(1-F)}{F}$$

$$\frac{R_6(1-F)/F \cdot R_6}{R_6(1-F)/F + R_6} = E$$

$$\frac{R_6^2 \cdot (1-F)/F}{(R_6/F - R_6) + R_6} = E$$

$$\frac{R_6^2 \cdot (1-F)/F}{R_6/F} = E$$

$$R_6 \cdot (1-F) = E$$

$$R_6 = \frac{E}{1-F} = \frac{1k\Omega}{1-0.05} = 1.05k\Omega$$

$$R_5 = \frac{1.05\Omega(1-0.05)}{0.05} = 20k\Omega$$

- Verify that the minimum input of 0V and the maximum input of 1-V result in an output within the 9.4-V range available for  $V_{ocm} = 5V$ .

Since the resistor divider acts like a 0.5V reference, the measured differential input for a 0-V  $V_{IN}$  is:

$$V_{IN} = 0V - 0.5V = -0.5V$$

- The output is:

$$-0.5V \cdot \frac{16V}{V} = -8V > -9.8V$$

- Likewise, for a 1-V input:

$$V_{IN} = 1V - 0.5V = 0.5V$$

$$0.5V \cdot \frac{16V}{V} = 8V < 9.8V$$

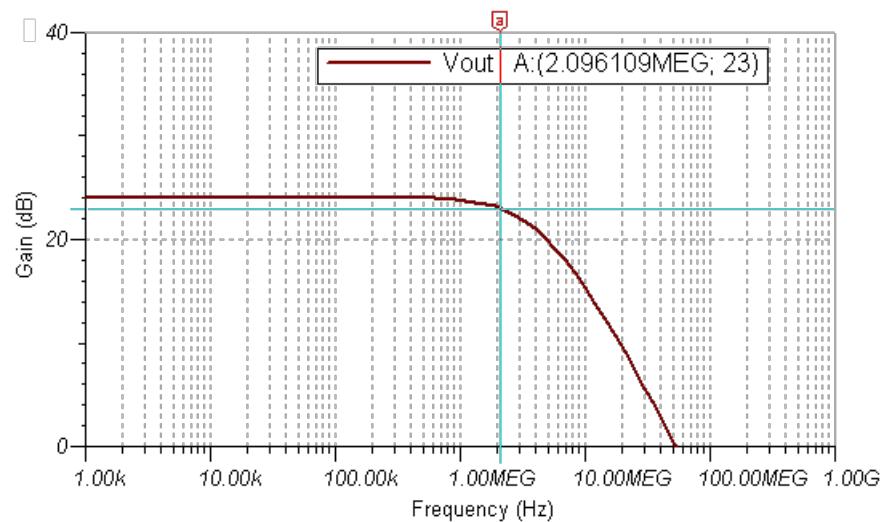
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**NOTE:** With a reference voltage of 0V, a 1-V input results in an output voltage greater than the maximum output range of the amplifier.

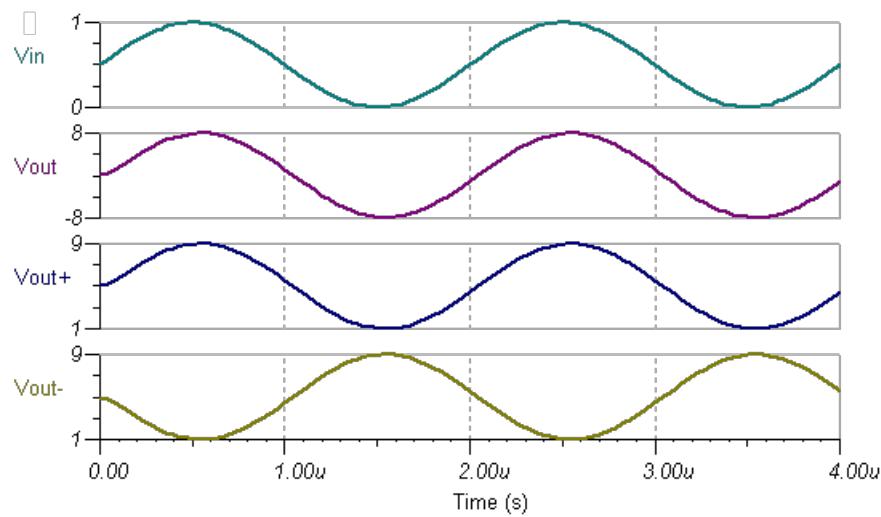
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## Design Simulations

### AC Simulation Results



### Transient Simulation Results



## Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See the TI Precision Labs video – [Op Amps: Fully Differential Amplifiers – Designing a Front-End Circuit for Driving a Differential Input ADC](#), for more information.

## Design Featured Op Amp

THS4561	
$V_{ss}$	3V to 13.5V
$V_{inCM}$	Vee-0.1V to Vcc-1.1V
$V_{out}$	Vee+0.2V to Vcc-0.2
$V_{os}$	TBD
$I_q$	TBD
$I_b$	TBD
<b>UGBW</b>	70MHz
<b>SR</b>	4.4V/ $\mu$ s
<b>#Channels</b>	1
<a href="http://www.ti.com/product/THS4561">http://www.ti.com/product/THS4561</a>	

## Design Alternate Op Amp

THS4131	
$V_{ss}$	5V to 33V
$V_{inCM}$	Vee+1.3V to Vcc-0.1V
$V_{out}$	Varies
$V_{os}$	2mV
$I_q$	14mA
$I_b$	2uA
<b>UGBW</b>	80MHz
<b>SR</b>	52V/ $\mu$ s
<b>#Channels</b>	1
<a href="http://www.ti.com/product/THS4131">http://www.ti.com/product/THS4131</a>	

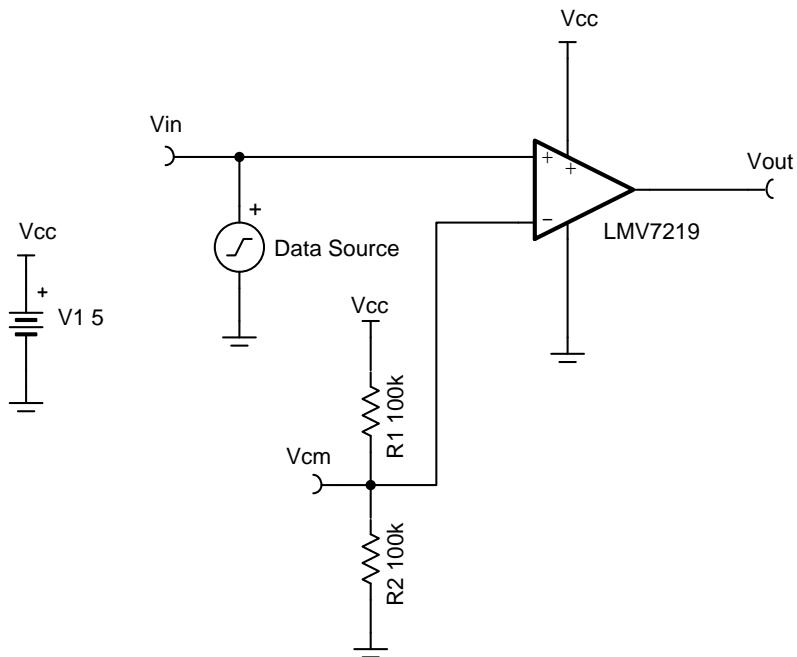
## Signal and clock restoration circuit

### Design Goals

Supply		Attenuated Input Signal		
$V_{cc}$	$V_{ee}$	$V_i$	$V_{cm}$	$f$
5V	0V	200mV <sub>p-p</sub>	2.5V	20MHz

### Design Description

The signal restoration circuit is used in digital systems to retrieve distorted clock or data waveforms. These clock and data signals can be attenuated and distorted on long traces due to stray capacitance, stray inductance, or reflections on transmission lines. The comparator is used to sense the attenuated and distorted input signal and convert it to a full scale digital output signal.



### Design Notes

1. Select a comparator with low input offset voltage and fast propagation delay.
2. A comparator with a toggle frequency larger than the input signal frequency should be used in order to properly process the incoming digital signal. A margin of 30% is sufficient.
3. If level translation is also required, use a comparator with separate input and output supplies.
4. If a differential output is required, use a comparator with a compatible output stage such as the LVDS compatible output on the LMH7220.

**Design Steps**

1. Calculate the maximum toggle frequency of the comparator to ensure it can process the 20MHz input signal.

$$f_{\max} = (t_{\text{rise}} + t_{\text{fall}} + t_{\text{pd\_hl}} + t_{\text{pd\_lh}})^{-1}$$

$$f_{\max} = (1.3\text{ns} + 1.25\text{ns} + 7\text{ns} + 7\text{ns})^{-1} = 35.4 \text{ MHz}$$

2. Set the inverting input of the comparator to the common mode voltage of 2.5V through the resistor divider  $R_1, R_2$ .

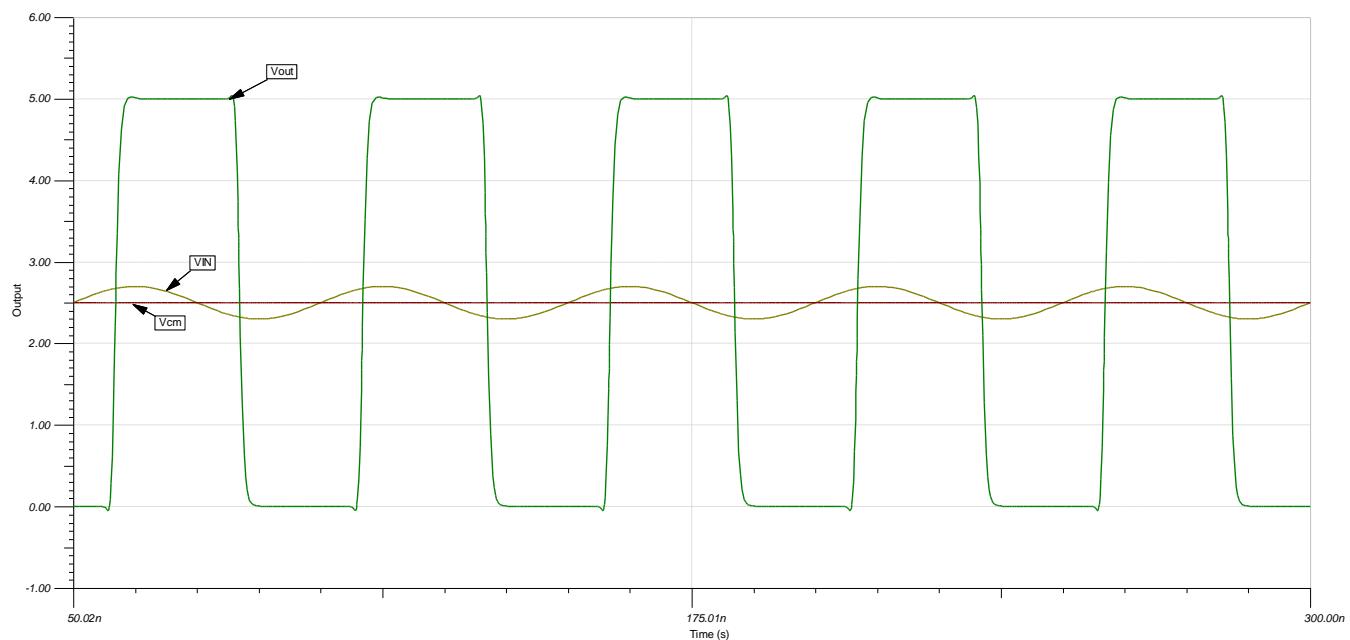
$$V_{\text{cm}} = (V_{\text{cc}}) \times \left(\frac{R_2}{R_1+R_2}\right) = 2.5\text{V}$$

$$\left(\frac{R_2}{R_1+R_2}\right) = \frac{1}{2}$$

3. Set  $R_1 = R_2 = 100\text{k}$ .
4. Set the noninverting input of the comparator to the input data signal.

## Design Simulations

### Transient Simulation Results



## Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit spice simulation file, [SNOM661](#).

For more information on many comparator topics including hysteresis, propagation delay and input common mode range please see, [TI Precision Labs](#).

## Design Featured Comparator

LMV7219	
$V_{ss}$	2.7V to 5V
$V_{inCM}$	Rail-to-rail
$t_{pd}$	7ns
$V_{os}$	1mV
$V_{HYS}$	7mV
$I_q$	0.9mA
<b>Output Type</b>	Push-Pull
<b>#Channels</b>	1
<a href="http://www.ti.com/product/lmv7219">www.ti.com/product/lmv7219</a>	

## Design Alternate Comparator

	TLV3501	LMH7220
$V_{ss}$	2.7 to 5.5V	2.7V to 12V
$V_{inCM}$	Rail-to-rail	Rail-to-rail
$t_{pd}$	4.5ns	2.9ns
$V_{os}$	1mV	9.5mV
$V_{HYS}$	6mV	na
$I_q$	3.2mA	6.8
<b>Output Type</b>	Push-Pull	LVDS
<b>#Channels</b>	1	1
	<a href="http://www.ti.com/product/tlv3501">www.ti.com/product/tlv3501</a>	<a href="http://www.ti.com/product/lmh7220">www.ti.com/product/lmh7220</a>

## Comparator with and without hysteresis circuit

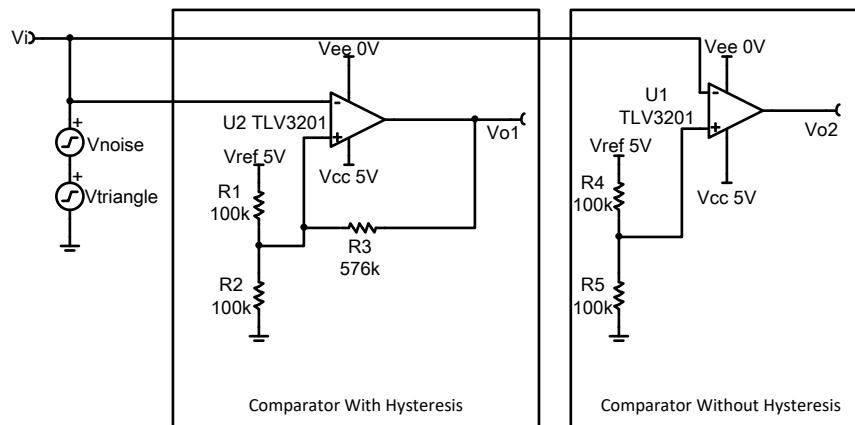
### Design Goals

Input		Output		Supply		
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	$V_{cc}$	$V_{ee}$	$V_{ref}$
0V	5V	0V	5V	5V	0V	5V

$V_L$ (Lower Threshold)	$V_H$ (Upper Threshold)	$V_H - V_L$
2.3V	2.7V	0.4V

### Design Description

Comparators are used to compare two different signal levels and create an output based on the input with the higher input voltage. Noise or signal variation at the comparison threshold will cause the comparator output to have multiple output transitions. Hysteresis sets upper- and lower-threshold voltages to eliminate the multiple transitions caused by noise.



### Design Notes

1. Use a comparator with low quiescent current to reduce power consumption.
2. The accuracy of the hysteresis threshold voltages are related to the tolerance of the resistors used in the circuit.
3. The propagation delay is based on the specifications of the selected comparator.

### Design Steps

1. Select components for the comparator with hysteresis.

- a. Select  $V_L$ ,  $V_H$ , and  $R_1$ .

$$V_L = 2.3V$$

$$V_H = 2.7V$$

$$R_1 = 100k\Omega \text{ (Standard Value)}$$

- b. Calculate  $R_2$ .

$$R_2 = \frac{V_L}{V_{cc} - V_H} \times R_1 = \frac{2.3V}{5V - 2.7V} \times 100k\Omega = 100k\Omega \text{ (Standard Value)}$$

- c. Calculate  $R_3$ .

$$R_3 = \frac{V_L}{V_H - V_L} \times R_1 = \frac{2.3V}{2.7V - 2.3V} \times 100k\Omega = 575k\Omega \approx 576k\Omega \text{ (Standard Value)}$$

- d. Verify hysteresis width.

$$V_H - V_L = \frac{R_1 \times R_2}{(R_3 \times R_1) + (R_3 \times R_2) + (R_1 \times R_2)} \times V_{cc}$$

$$= \frac{100k\Omega \times 100k\Omega}{(576k\Omega \times 100k\Omega) + (576k\Omega \times 100k\Omega) + (100k\Omega \times 100k\Omega)} \times 5V = 0.399V$$

2. Select components for comparator without hysteresis.

- a. Select  $V_{th}$  and  $R_4$ .

$$V_{th} = 2.5V$$

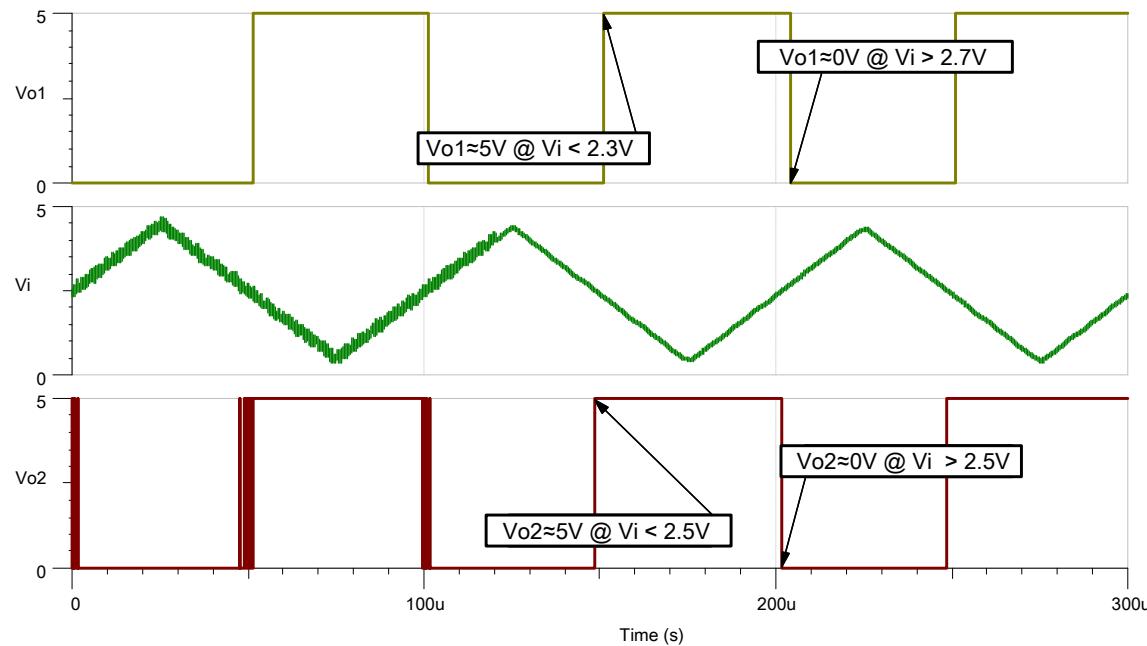
$$R_4 = 100k\Omega \text{ (Standard Value)}$$

- b. Calculate  $R_5$ .

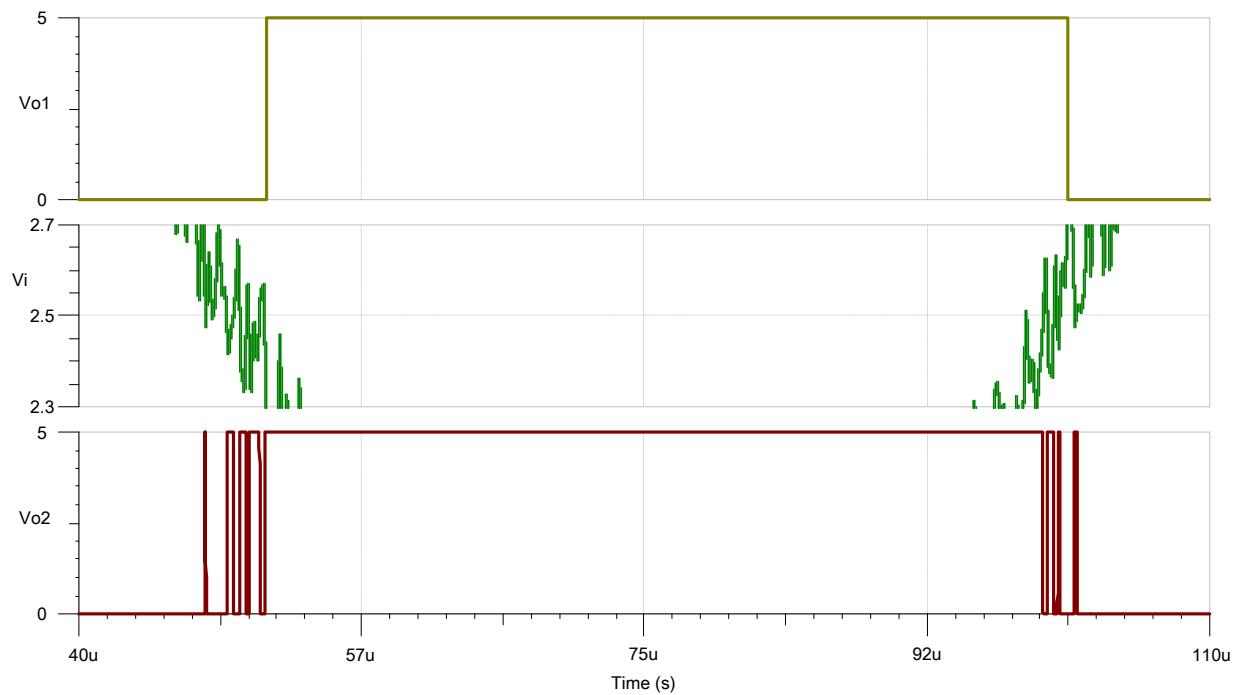
$$R_5 = \frac{V_{th}}{V_{cc} - V_{th}} \times R_4 = \frac{2.5V}{5V - 2.5V} \times 100k\Omega = 100k\Omega \text{ (Standard Value)}$$

## Design Simulations

### Transient Simulation Results



**Noise Only Present From 0s to 120 $\mu$ s**



**Zoomed in From 40 $\mu$ s to 110 $\mu$ s**

## Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See the circuit SPICE simulation file [SBOC515](#).

See TIPD144, [www.ti.com/tool/tipd144](http://www.ti.com/tool/tipd144).

## Design Featured Comparator

TLV3201	
<b>V<sub>cc</sub></b>	2.7V to 5.5V
<b>V<sub>inCM</sub></b>	Extends 200mV beyond either rail
<b>V<sub>out</sub></b>	(V <sub>ee</sub> +230mV) to (V <sub>cc</sub> -210mV) @ 4mA
<b>V<sub>os</sub></b>	1mV
<b>I<sub>q</sub></b>	40µA
<b>I<sub>b</sub></b>	1pA
<b>UGBW</b>	-
<b>SR</b>	-
<b>#Channels</b>	1, 2
<a href="http://www.ti.com/product/tlv3201">www.ti.com/product/tlv3201</a>	

## Revision History

Revision	Date	Change
A	February 2019	Downscale the title and changed title role to 'Amplifiers'. Added links to circuit cookbook landing page and SPICE simulation file.

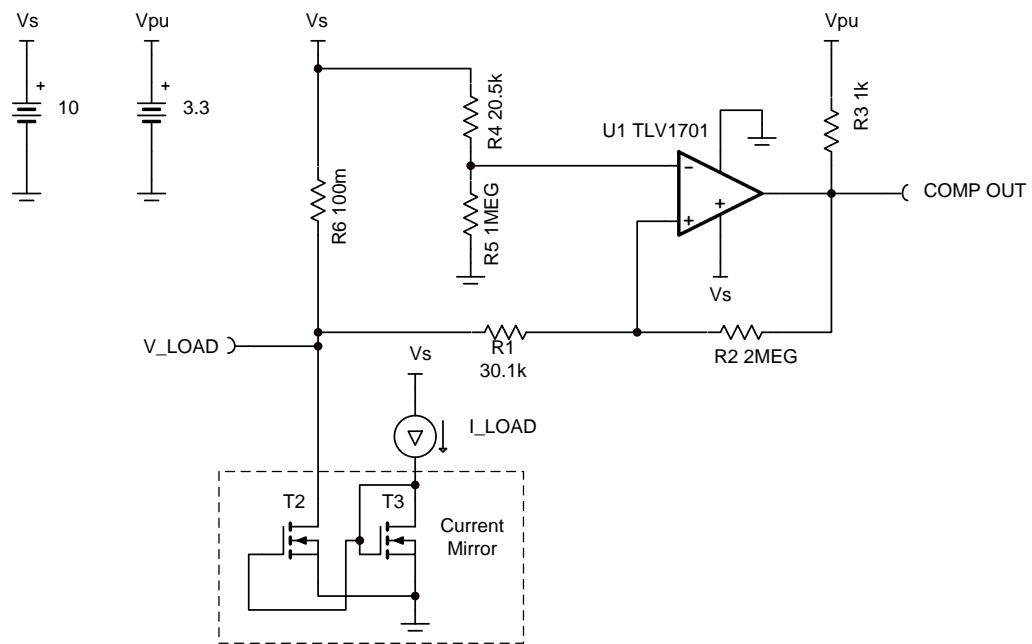
## High-side current sensing with comparator circuit

### Design Goals

Load Current ( $I_L$ )		System Supply ( $V_s$ )	Comparator Output Status	
Over Current ( $I_{OC}$ )	Recovery Current ( $I_{RC}$ )	Typical	Over Current	Normal Operation
1 A	0.5 A	10 V	$V_{OL} < 0.4$ V	$V_{OH} = V_{PU} = 3.3$ V

### Design Description

This high-side, current sensing solution uses one comparator with a rail-to-rail input common mode range to create an over-current alert (OC-Alert) signal at the comparator output (COMP OUT) if the load current rises above 1A. The OC-Alert signal in this implementation is active low. So when the 1A threshold is exceeded, the comparator output goes low. Hysteresis is implemented such that OC-Alert will return to a logic high state when the load current reduces to 0.5A (a 50% reduction). This circuit utilizes an open-drain output comparator in order to level shift the output high logic level for controlling a digital logic input pin. For applications needing to drive the gate of a MOSFET switch, a comparator with a push-pull output is preferred.



### Design Notes

1. Select a comparator with rail-to-rail input common mode range to enable high-side current sensing.
2. Select a comparator with an open-drain output stage for level-shifting.
3. Select a comparator with low input offset voltage to optimize accuracy.
4. Calculate the value for the shunt resistor ( $R_6$ ) so the shunt voltage ( $V_{SHUNT}$ ) is at least ten times larger than the comparator offset voltage ( $V_{IO}$ ).

### Design Steps

1. Select value of  $R_6$  so  $V_{SHUNT}$  is at least 10x greater than the comparator input offset voltage ( $V_{IO}$ ). Note that making  $R_6$  very large will improve OC detection accuracy but will reduce supply headroom.

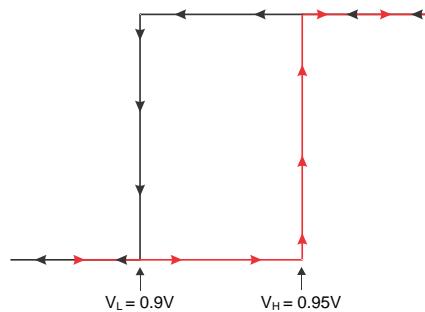
$$V_{SHUNT} = (I_{OC} \times R_6) \geq 10 \times V_{IO} = 55\text{mV}$$

set  $R_6 = 100\text{m}\Omega$  for  $I_{OC} = 1\text{A}$  &  $V_{IO} = 5.5\text{mV}$

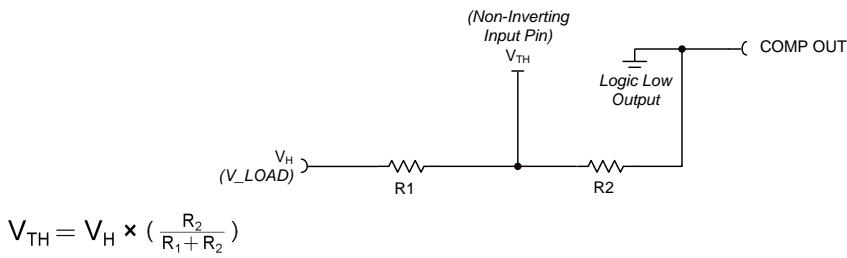
2. Determine the desired switching thresholds for when the comparator output will transition from high-to-low ( $V_L$ ) and low-to-high ( $V_H$ ).  $V_L$  represents the threshold when the load current crosses the OC level, while  $V_H$  represents the threshold when the load current recovers to a normal operating level.

$$V_L = V_S - (I_{OC} \times R_6) = 10 - (1 \times 0.1) = 0.9\text{V}$$

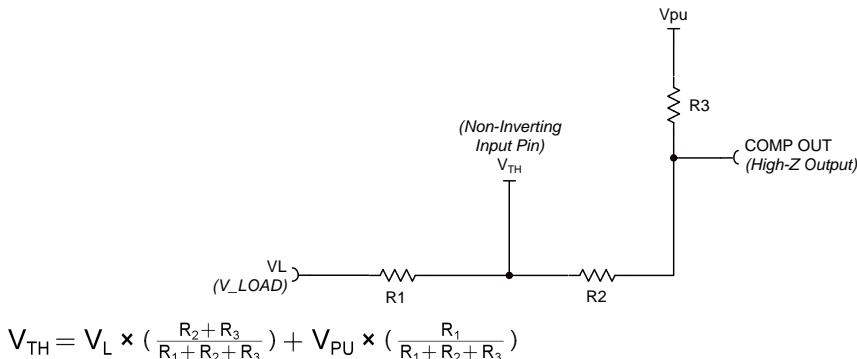
$$V_H = V_S - (I_{RC} \times R_6) = 10 - (0.5 \times 0.1) = 0.95\text{V}$$



3. With the non-inverting input pin of the comparator labeled as  $V_{TH}$  and the comparator output in a logic low state (ground), derive an equation for  $V_{TH}$  where  $V_H$  represents the load voltage ( $V_{LOAD}$ ) when the comparator output transitions from low to high. Note that the simplified diagram for deriving the equation shows the comparator output as ground (logic low).



4. With the non-inverting input pin of the comparator labeled as  $V_{TH}$  and the comparator output in a high-impedance state, derive an equation for  $V_{TH}$  where  $V_L$  represents the load voltage ( $V_{LOAD}$ ) when the comparator output transitions from high to low. Applying "superposition" theory to solve for  $V_{TH}$  is recommended.



5. Eliminate variable  $V_{TH}$  by setting the two equations equal to each other and solve for  $R_1$ . The result is the following quadratic equation. Solving for  $R_2$  is less desirable since there are more standard values for small resistor values than the larger ones.

$$0 = (V_{PU}) \times R_1^2 + (V_{PU} \times R_2 + V_L \times (R_3 + R_2) - V_H \times R_2) \times R_1 + (V_L - V_H) \times (R_2^2 + R_2 \times R_3)$$

6. Calculate  $R_1$  after substituting in numeric values for  $V_{PU}$ ,  $R_2$ ,  $V_L$ ,  $V_H$ , and  $R_3$ . For this design, set  $V_{PU}=3.3$ ,  $R_2=2M$ ,  $V_L=9.9$ ,  $V_H=9.95$ , and  $R_3=1k$ . Please note that  $R_3$  is significantly smaller than  $R_2$  ( $R_3 \ll R_2$ ). Increasing  $R_3$  will cause the comparator logic high output level to increase beyond  $V_{PU}$  and should be avoided. For example, increasing  $R_3$  to a value of 100k can cause the logic high output to be 3.6V.

$$0 = (3.3) \times R_1^2 + (6.591M) \times R_1 - (200.1G)$$

the positive root for  $R_1 = 29.9k\Omega$

using standard 1% resistor values,  $R_1 = 30.1k\Omega$

7. Calculate  $V_{TH}$  using the equation derived in Design Step 3; use the calculated value for  $R_1$ . Note that  $V_{TH}$  is less than  $V_L$  since  $V_{PU}$  is less than  $V_L$ .

$$V_{TH} = V_H \times \left( \frac{R_2}{R_1 + R_2} \right) = 9.802V$$

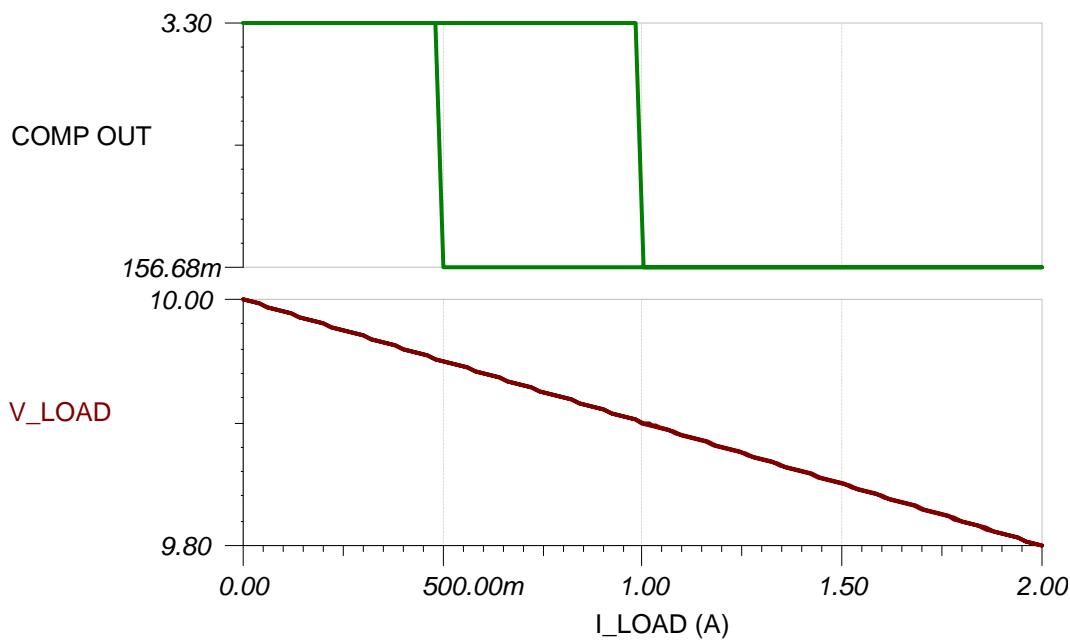
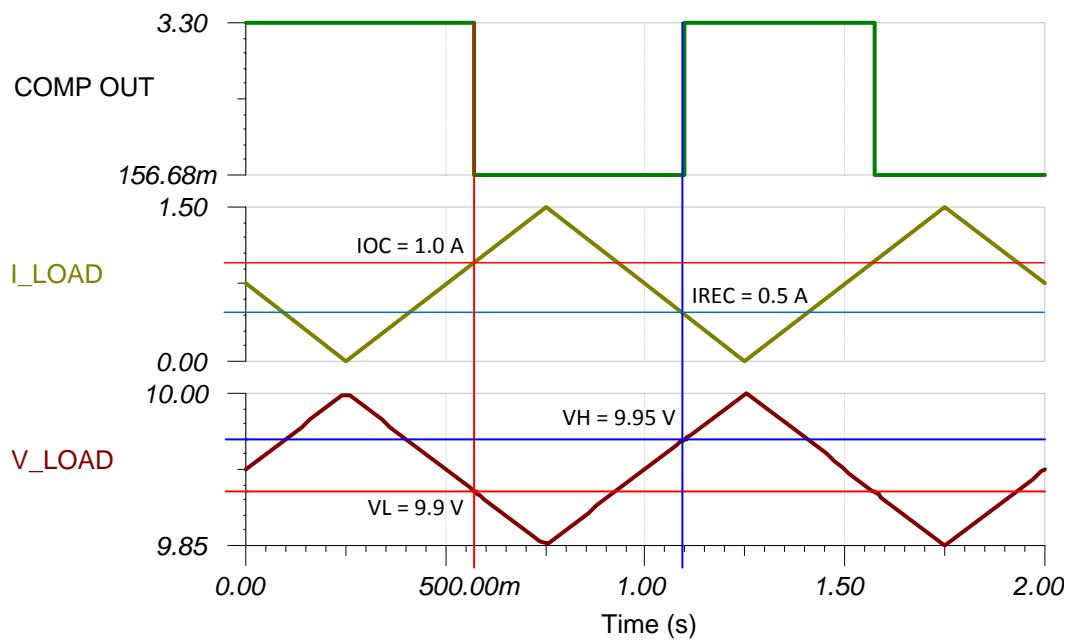
8. With the inverting terminal labeled as  $V_{TH}$ , derive an equation for  $V_{TH}$  in terms of  $R_4$ ,  $R_5$ , and  $V_S$ .

$$V_{TH} = V_S \times \left( \frac{R_5}{R_4 + R_5} \right)$$

9. Calculate  $R_4$  after substituting in numeric values  $R_5=1M$ ,  $V_S=10$ , and the calculated value for  $V_{TH}$ .

$$R_4 = \left( \frac{R_5 \times (V_S - V_{TH})}{V_{TH}} \right) = 20.15k\Omega$$

using standard 1% resistor values,  $R_4 = 20.5k\Omega$

**Design Simulations**
**DC Simulation Results**

**Transient Simulation Results**


### Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See Circuit SPICE Simulation File SLOM456, <http://www.ti.com/lit/zip/sлом456>.

### Design Featured Comparator

TLV170x-Q1, TLV170x	
$V_S$	2.2 V to 36 V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Open-Drain, Rail-to-rail
$V_{os}$	500 $\mu$ V
$I_Q$	55 $\mu$ A/channel
$t_{PD(HL)}$	460 ns
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/tlv1701-q1">www.ti.com/product/tlv1701-q1</a>	

### Design Alternate Comparator

	TLV7021	TLV370x-Q1, TLV340x
$V_S$	1.6 V to 5.5 V	2.7 V to 16 V
$V_{inCM}$	Rail-to-rail	Rail-to-rail
$V_{out}$	Open-Drain, Rail-to-rail	Push-Pull, Rail-to-rail
$V_{os}$	500 $\mu$ V	250 $\mu$ V
$I_Q$	5 $\mu$ A	560 $\mu$ A/Ch
$t_{PD(HL)}$	260 ns	36 $\mu$ s
<b>#Channels</b>	1	1, 2, 4
	<a href="http://www.ti.com/product/tlv7021">www.ti.com/product/tlv7021</a>	<a href="http://www.ti.com/product/tlv3701-q1">www.ti.com/product/tlv3701-q1</a>

## High-speed overcurrent detection circuit

### Design Goal

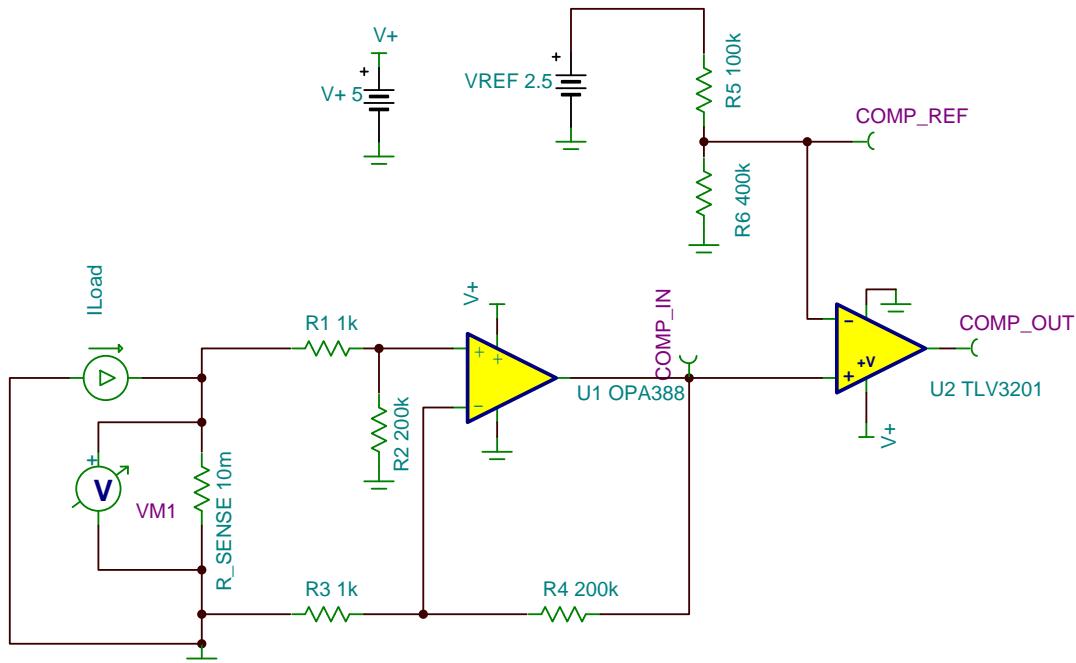
Overcurrent Levels		Supply		Transient Response Time
$I_{IN}$ (min)	$I_{IN}$ (max)	$V_+$	$V_-$	$t$
0A	1.0A	5V	0V	< 10 $\mu$ s

### Design Description

This high-speed, low-side overcurrent detection solution is implemented with a single zero-drift fast-settling amplifier (**OPA388**) and one high-speed comparator (**TLV3201**). This circuit is designed for applications that monitor fast current signals and overcurrent events, such as current detection in motors and power supply units.

The OPA388 is selected for its widest bandwidth with ultra-low offset and fast slew rate. The TLV3201 is selected for its fast response due to its small propagation delay of 40ns and rise time of 4.8ns. This allows the comparator to quickly respond and alert the system of an overcurrent event all within the transient response time requirement. The push-pull output stage also allows the comparator to directly interface with the logic levels of the microcontroller. The TLV3201 also has low power consumption with a quiescent current of 40 $\mu$ A.

Typically for low-side current detection, the amplifier across the sense resistor can be used in a noninverting configuration. The application circuit shown, however, uses the OPA388 as a differential amplifier across the sense resistor. This provides a true differential measurement across the shunt resistor and can be beneficial in cases where the supply ground and load ground are not necessarily the same.



### Design Notes

1. To minimize errors, choose precision resistors and set  $R_1 = R_3$ , and  $R_2 = R_4$ .
2. Select  $R_{SENSE}$  to minimize the voltage drop across the resistor at the max current of 1 A.
3. Due to the ultra-low offset of the OPA388 (0.25  $\mu$ V), the effect of any offset error from the amplifier is minimal on the mV range measurement across  $R_{SENSE}$ .
4. Select the amplifier gain so COMP\_IN reaches 2 V when the system crosses its critical overcurrent value of 1 A.
5. Traditional bypass capacitors are omitted to simplify the application circuit.

### Design Steps

1. Determine the transfer equation where  $R_1 = R_3$  and  $R_2 = R_4$ .

$$COMP\_IN = (R_{SENSE} \cdot I_{LOAD}) \cdot \left( \frac{R_2}{R_1 + R_2} \right) \cdot \left( 1 + \frac{R_4}{R_3} \right)$$

2. Select the SENSE resistor value assuming a maximum voltage drop of 10 mV with a load current of 1 A in order to minimize the voltage drop across the resistor.

$$R_{SENSE} = \frac{V_{SENSE}(\max)}{I_{LOAD}(\text{critical})} = \frac{10\text{mV}}{1\text{A}} = 10\text{m}\Omega$$

3. Select the amplifier gain such that COMP\_IN reaches 2V when the load current reaches the critical threshold of 1A.

$$\text{Gain} = \frac{V_{REF}}{R_{SENSE} \cdot I_{LOAD}(\text{critical})} = \frac{2\text{ V}}{0.01\text{ V}} = \frac{R_2}{R_1 + R_2} \cdot 1 + \frac{R_4}{R_3} = 200$$

Set:

$$R_1 = R_3 = 1\text{k}\Omega$$

$$R_2 = R_4 = 200\text{k}\Omega$$

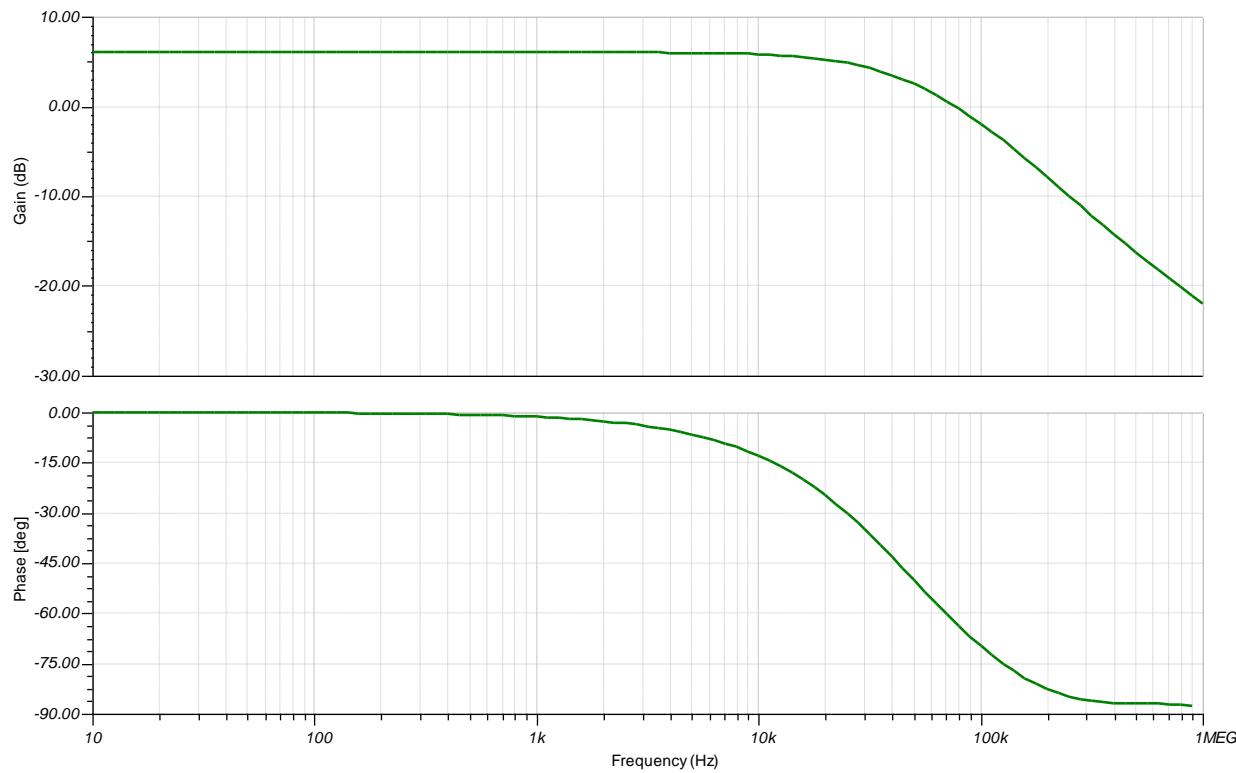
4. Calculate the transimpedance gain of the amplifier in order to verify the following AC simulation results:

$$V_{OUT} = I_{LOAD} \cdot 10\text{m}\Omega \cdot 200$$

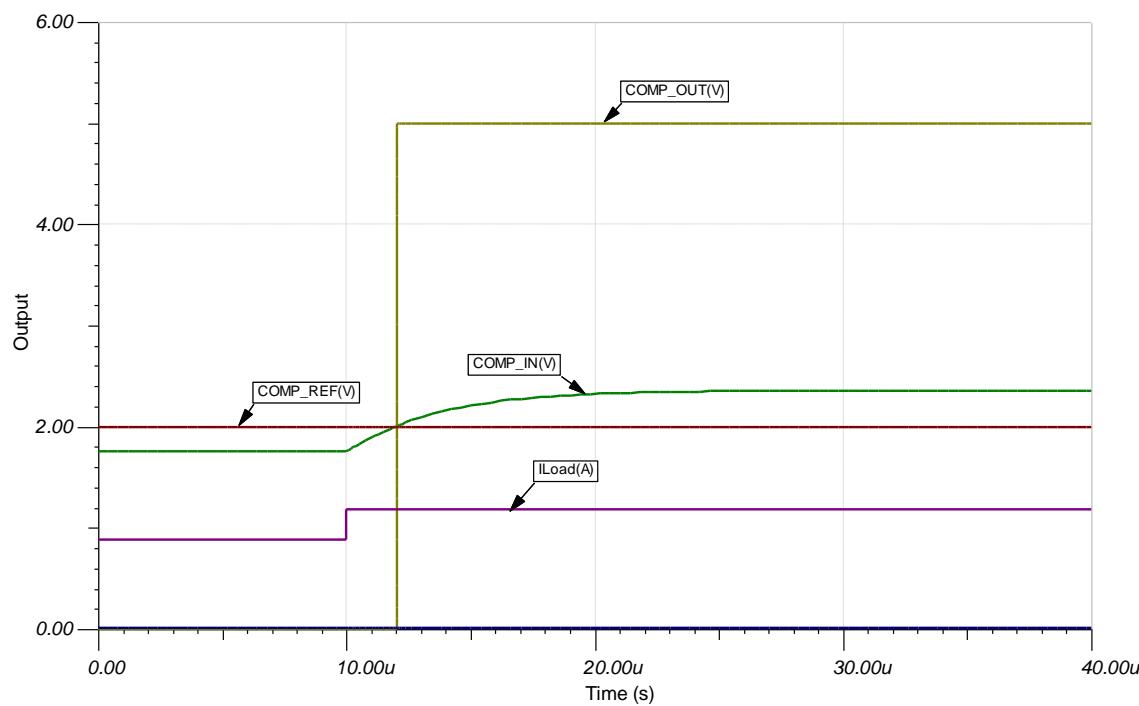
$$\frac{V_{OUT}}{I_{LOAD}} = 10\text{m}\Omega \cdot 200 = 2$$

### Design Simulations

#### COMP\_IN Transimpedance AC Simulation Results



#### Transient Response Simulation Results



## Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See the [Current sensing using nanopower op amps](#) blog.

## References

1. Texas Instruments, [Advantages of using nanopower, zero drift amplifiers for battery voltage and current monitoring in portable applications](#) TI tech note
2. Texas Instruments, [Current sensing in no-neutral light switches](#) TI tech note
3. Texas Instruments, [GPIO Pins power signal chain in personal electronics running on Li-Ion batteries](#) TI tech note

## Design Featured Comparator

TLV3201	
$V_s$	2.7V to 5.5V
$t_{PD}$	40ns
Input $V_{CM}$	Rail-to-rail
$V_{os}$	1mV
$I_q$	40 $\mu$ A
TLV3201	

## Design Alternate Comparator

TLV7021	
$V_s$	1.6V to 5.5V
$t_{PD}$	260ns
Input $V_{CM}$	Rail-to-rail
$V_{os}$	0.5mV
$I_q$	5 $\mu$ A
TLV7021	

## Design Featured Op Amp

OPA388	
$V_s$	2.5V to 5.5V
Input $V_{CM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	0.25 $\mu$ V
$V_{os}$ Drift	.005 $\mu$ V/ $^{\circ}$ C
$I_q$	1.7mA/Ch
$I_b$	30pA
UGBW	10MHz
OPA388	

**Design Alternate Op Amp**

THS4521	
$V_s$	2.5V to 5.5V
Input $V_{CM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	20 $\mu$ V
$V_{os}$ Drift	$\mu$ V/ $^{\circ}$ C
$I_q$	1mA/Ch
$I_b$	0.6 $\mu$ A
UGBW	145MHz
THS4521	

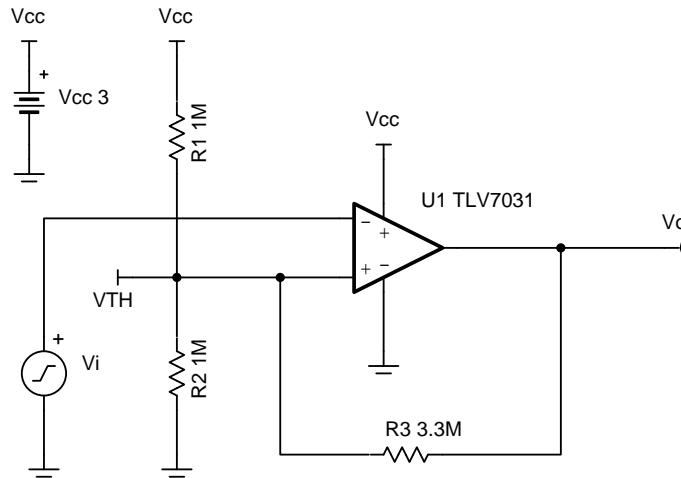
## *Inverting comparator with hysteresis circuit*

### Design Goals

Output		Threshold	Hysteresis	Supply	
$V_o = \text{HIGH}$	$V_o = \text{LOW}$	$V_{TH}$	$V_{HYS}$	$V_{cc}$	$V_{ee}$
$V_i < V_L$	$V_i > V_H$	1.5V	400mV	3V	0V

### Design Description

Comparators are used to differentiate between two different signal levels. When setup in an inverting fashion, the comparator output will be a digital high if the analog input is below a selected threshold. With noise, signal variation, or slow-moving signals at the comparison threshold, undesirable transitions at the output can be observed. Setting upper and lower hysteresis thresholds eliminates these undesirable output transitions. This circuit example will focus on the steps required to design the positive feedback resistor network necessary to obtain the desired hysteresis for an inverting comparator application.

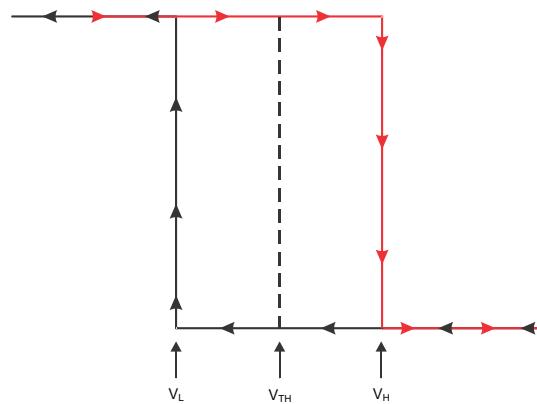


### Design Notes

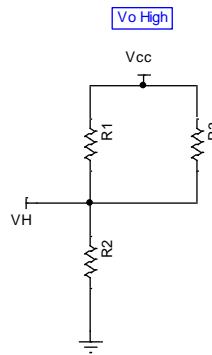
1. The accuracy of the hysteresis threshold voltages are related to the tolerance of the resistors used in the circuit, the selected comparator's input offset voltage specification, and any internal hysteresis already applied to the device.
2. For the TLV7031,  $V_{OH}$  is approximately 200mV below  $V_{cc}$  and  $V_{OL}$  is approximately 250mV above  $V_{ee}$ .
3. The TLV7031 has a push-pull output stage, so no pull-up resistor is needed.

### Design Steps

1. Select  $R_1$ . This can be a high resistance value due to the very low input bias current caused by the CMOS input of the device.  
 $R_1 = 1M\Omega$  (Standard Value)
2. Solve for  $R_2$  based on the desired threshold voltage. Set  $V_{TH}$  to be 50% of  $V_{cc}$  for balanced hysteresis.  
 $R_2 = \frac{R_1 \times V_{TH}}{V_{cc} - V_{TH}} = \frac{1M\Omega \times 1.5V}{3V - 1.5V} = 1M\Omega$
3. Observe the feedback resistor network in the two possible output states: High and Low. Note that the threshold voltage applied to the non-inverting pin by the voltage divider ( $R_1$  and  $R_2$ ) can be further controlled by using the feedback resistor ( $R_3$ ). Below is the hysteresis eye diagram.



4. Derive the equation for  $V_H$ , which is the threshold voltage when  $V_o$  is high. For simplicity, assume  $V_o$  switches to  $V_{cc}$  when  $V_i < V_L$ . When this occurs,  $R_1$  and  $R_3$  are in parallel.



5. For push-pull outputs.

$$V_H = V_{cc} \times \frac{R_2}{(R_1 \parallel R_3) + R_2}$$

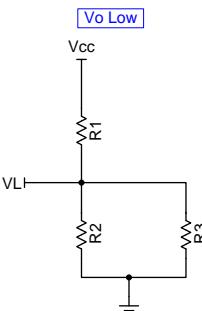
- a. If the comparator in use has an open-drain or open-collector output stage, then the pull-up resistor,  $R_{pu}$ , will be in series with  $R_3$ . The following equation is true if  $V_{pu} = V_{cc}$ . Do note that for some applications the pull-up resistor could be ignored in the  $V_H$  equation since the eventual feedback resistor value could be significantly larger (ideally 10 times larger) than the pull-up resistor.

$$V_H = V_{cc} \times \frac{R_2}{[R_1 \parallel (R_3 + R_{pu})] + R_2}$$

- b. If  $V_{pu} \neq V_{cc}$ , then use the following equation for  $V_H$ .

$$V_H = \frac{(R_1 \times V_{pu} + (R_3 + R_{pu}) \times V_{cc}) \times R_2}{R_1 \times (R_2 + R_3 + R_{pu}) + R_2 \times (R_3 + R_{pu})}$$

6. Derive the equation for  $V_L$ , which is the threshold voltage when  $V_o$  is low. For simplicity, assume  $V_o$  switches to  $V_{ee}$  when  $V_i > V_H$ . When this occurs,  $R_2$  and  $R_3$  are in parallel.



$$V_L = V_{cc} \times \frac{R_2 || R_3}{R_1 + (R_2 || R_3)}$$

7. Derive the equation for  $V_{HYS}$ .

$$V_{HYS} = V_H - V_L = \frac{R_1 \times R_2 \times V_{cc}}{R_1 \times (R_2 + R_3) + (R_2 \times R_3)}$$

8. Solve for  $R_3$ .

$$R_3 = \frac{R_1 \times R_2 \times (V_{cc} - V_{HYS})}{(R_1 + R_2) \times V_{HYS}} = \frac{1M\Omega \times 1M\Omega \times (3V - 0.4V)}{(1M\Omega + 1M\Omega) \times 0.4V} = 3.25M\Omega$$

$$R_3 = 3.3M\Omega \text{ (Standard Value)}$$

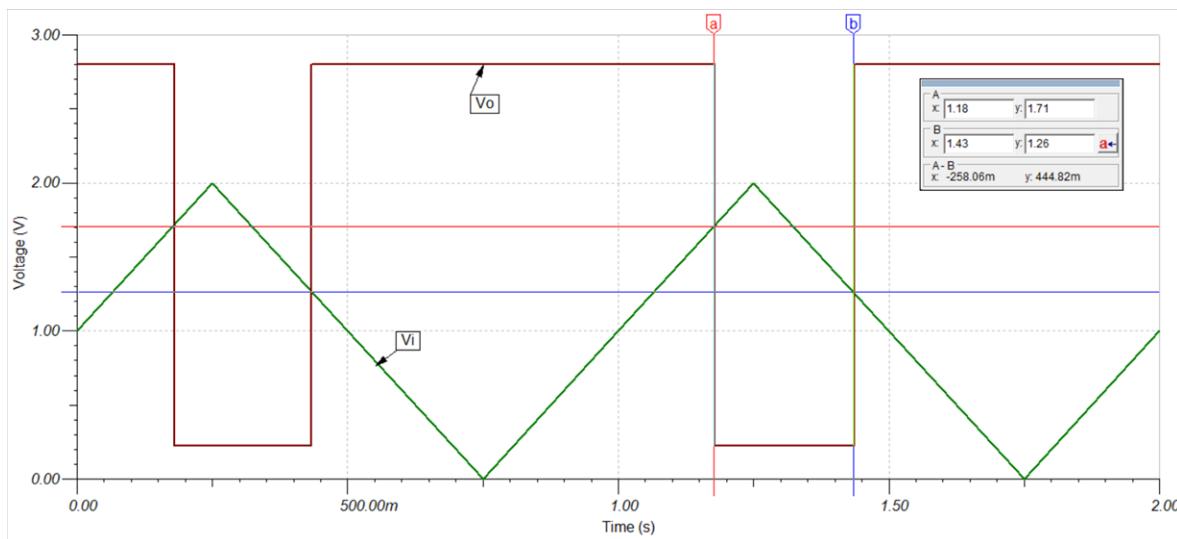
9. Verify  $V_{HYS} = 400mV$  such that  $V_H = 1.7V$  and  $V_L = 1.3V$ .

$$V_H = V_{cc} \times \frac{R_2}{(R_1 || R_3) + R_2} = 3V \times \frac{1M\Omega}{(1M\Omega || 3.3M\Omega) + 1M\Omega} = 1.70V$$

$$V_L = V_{cc} \times \frac{R_2 || R_3}{R_1 + (R_2 || R_3)} = 3V \times \frac{(1M\Omega || 3.3M\Omega)}{1M\Omega + (1M\Omega || 3.3M\Omega)} = 1.30V$$

$$V_{HYS} = V_H - V_L = 1.70V - 1.30V = 400mV$$

### Transient Simulation Results



### Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See Comparator with Hysteresis Reference Design TIPD144, [www.ti.com/tipd144](http://www.ti.com/tipd144).

See Circuit SPICE Simulation File SLVMCQ0, <http://www.ti.com/lit/zip/slvmcq0>.

For more information on many comparator topics including hysteresis, propagation delay and input common mode range please see [training.ti.com/ti-precision-labs-op-amps](http://training.ti.com/ti-precision-labs-op-amps).

### Design Featured Comparator

TLV7031	
<b>Output Type</b>	Push-Pull
$V_{cc}$	1.6V to 6.5V
$V_{inCM}$	Rail-to-rail
$V_{os}$	$\pm 100\mu V$
$V_{HYS}$	7mV
$I_q$	335nA/Ch
$t_{pd}$	3 $\mu s$
<b>#Channels</b>	1
	<a href="http://www.ti.com/product/tlv7031">www.ti.com/product/tlv7031</a>

### Design Alternate Comparator

TLV1701	
<b>Output Type</b>	Open Collector
$V_{cc}$	2.2V to 36V
$V_{inCM}$	Rail-to-rail
$V_{HYS}$	N/A
$V_{os}$	$\pm 500\mu V$
$I_q$	55 $\mu A/Ch$
$t_{pd}$	560ns
<b>#Channels</b>	1, 2, 4
	<a href="http://www.ti.com/product/tlv1701">www.ti.com/product/tlv1701</a>

## Low-power, bidirectional current-sensing circuit

### Design Goals

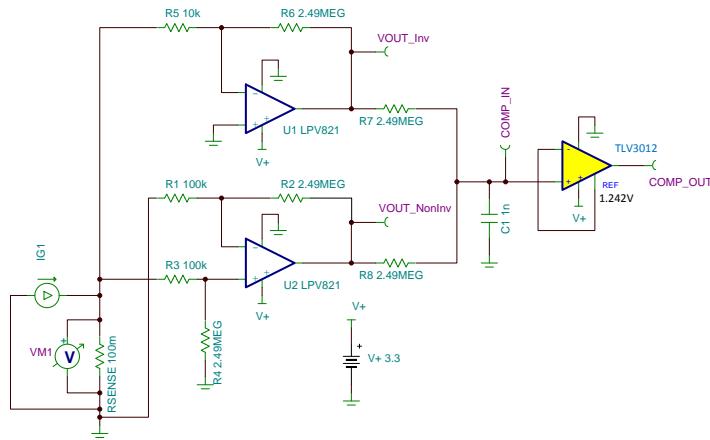
Overcurrent Levels		Supply	
$I_{IN}$ (min)	$I_{IN}$ (max)	$V_+$	$V_-$
-0.1 A	1.0 A	3.3V	0V

### Design Description

This low-power, low-side, bidirectional current sensing solution uses two nano-power, zero-drift amplifiers ([LPV821](#)) and one micro-power comparator with an integrated, precision reference ([TLV3012](#)). This circuit is well-suited for battery powered devices where charging current and system current need to be monitored accurately. The gain of U1 and U2 are set independently.

As shown in the application circuit, the LPV821 amplifiers are connected out of phase across  $R_{SENSE}$  to amplify the currents of opposite polarity. Amplifier U2 linearly amplifies the charging (positive) current while amplifier U1 linearly amplifies the system (negative) current. When U2 is monitoring the positive current, U1 drives its output to ground. Similarly, U2 drives its output to ground when U1 monitors the negative current. The amplifier outputs are ORed together with resistors  $R_7$  and  $R_8$  while U1 or U2 provide the ground reference creating a single output voltage for the comparator to monitor.

If a regulated supply or reference is already available in the system, the TLV3012 can be replaced by a nano-power comparator such as the [TLV7031](#). Moreover, if the charging current and system current have equal magnitudes, the gains of amplifier U1 and U2 can be set equal to each other. Even with the gains of the amplifiers being equal, ORing the amplifier outputs allows one comparator to detect overcurrent conditions for both charging and system current.



### Design Notes

1. To minimize errors, utilize precision resistors and set  $R_1 = R_3$ ,  $R_2 = R_4$ , and  $R_7 = R_8$ .
2. Select  $R_{SENSE}$  to minimize the voltage drop at max current and to reduce amplifier offset error when monitoring minimum current levels.
3. Select the amplifier gains so  $COMP\_IN$  reaches 1.242V when the charging and system currents reach their critical levels and avoid operating the amplifiers outside of their linear range.

## Design Steps

1. Determine the transfer equation given  $R_1 = R_3$ ,  $R_2 = R_4$ , and  $R_7 = R_8$ .

Inverted Path:

$$COMP\_IN = - I_{G1} \times R_{SENSE} \times \left( -\frac{R_6}{R_5} \right) \times \left( \frac{R_8}{R_7 + R_8} \right)$$

Non-Inverted Path:

$$COMP\_IN = I_{G1} \times R_{SENSE} \times \left( \frac{R_4}{R_3 + R_4} \right) \times \left( \frac{R_1 + R_2}{R_1} \right) \times \left( \frac{R_7}{R_7 + R_8} \right)$$

2. Select the SENSE resistor value assuming a maximum voltage drop ( $V_{SENSE}$ ) of 100mV when charging at 1A and a minimum system current of 10mA.

$$R_{SENSE} \text{ (max)} = \frac{V_{SENSE} \text{ (max)}}{I_{G1} \text{ (max)}} = \frac{100 \text{ mV}}{1 \text{ A}} = 100 \text{ m}\Omega$$

with  $I_{G1}(\min) = 10\text{mA}$ ,  $V_{SENSE} = 10\text{mA} \times 100\text{m}\Omega = 1 \text{ mV} > > V_{OS}(\text{max}) = 10 \text{ }\mu\text{V}$

3. Select ORing resistor  $R_7$  and  $R_8$  to generate COMP\_IN.

a. An equal attenuation factor of two is applied to the input of the comparator with  $R_7 = R_8$ . Choose large values to minimize current consumption from the output of the amplifiers.

b. Special care must be taken when validating the voltage at COMP\_IN. Since  $R_7$  and  $R_8$  are large impedance values, the input impedance of an oscilloscope probe or the input to a digital voltmeter can alter the measured voltage. Common probe and voltmeter input impedances are 10MΩ and this will attenuate the signal measured.

with  $R_7 = R_8 = 2.49 \text{ M}\Omega$ ,

$$COMP\_IN = (V_{OUT\_Inv} \text{ or } V_{OUT\_NonInv}) / 2$$

4. Select the amplifier gain such that COMP\_IN reaches 1.242V when the currents reach the critical threshold.

$$Gain = \frac{2 \times Comparator\_REF}{R_{SENSE} \times |I_{G1} \text{ (max)}|}$$

$$Gain \text{ (Inv)} = \frac{2 \times 1.242}{0.1 \times (-0.1)} = \frac{(-R_6)}{R_5} \approx -249 \frac{\text{V}}{\text{V}}$$

$$Gain \text{ (NonInv)} = \frac{2 \times 1.242}{0.1 \times 1.0} = \frac{R_4}{R_3 + R_4} \times \frac{R_1 + R_2}{R_1} \approx 24.9 \frac{\text{V}}{\text{V}}$$

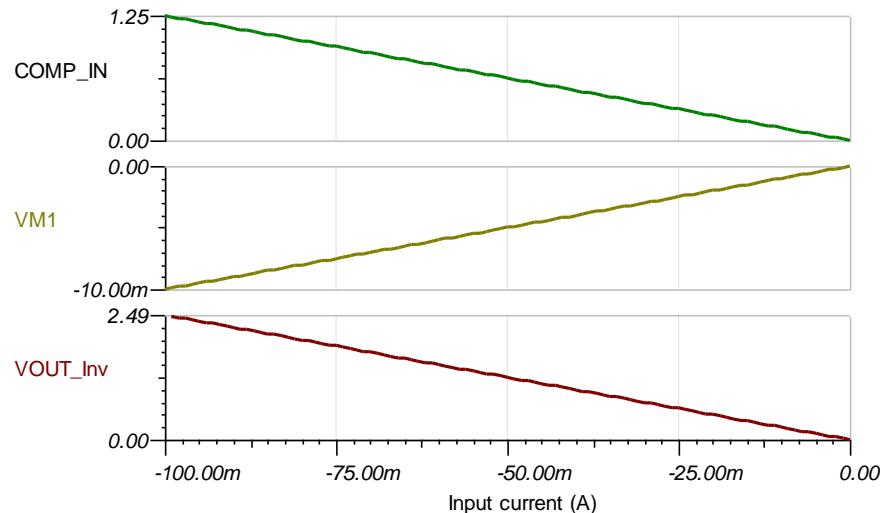
$R_1 = R_3 = 100 \text{ k}\Omega$  (Standard Value)

$R_5 = 10 \text{ k}\Omega$  (Standard Value)

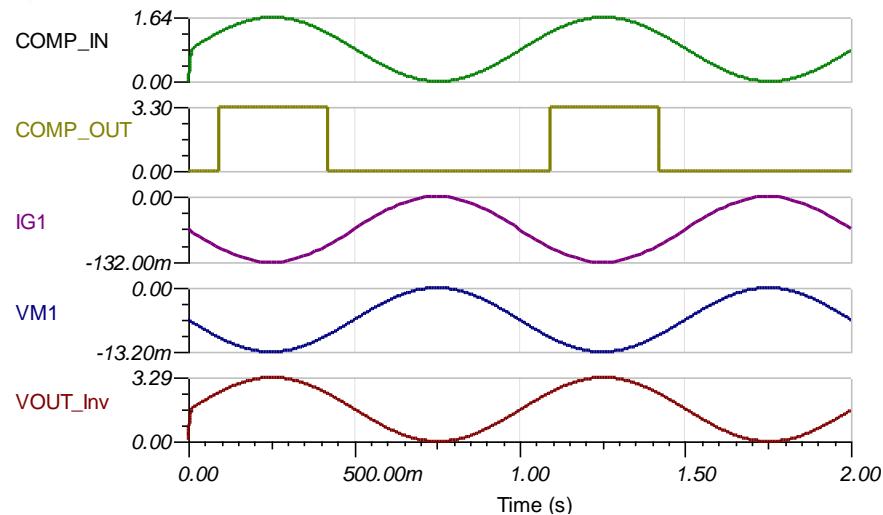
$R_2 = R_4 = R_6 = 2.49 \text{ M}\Omega$  (Standard Value)

## Design Simulations

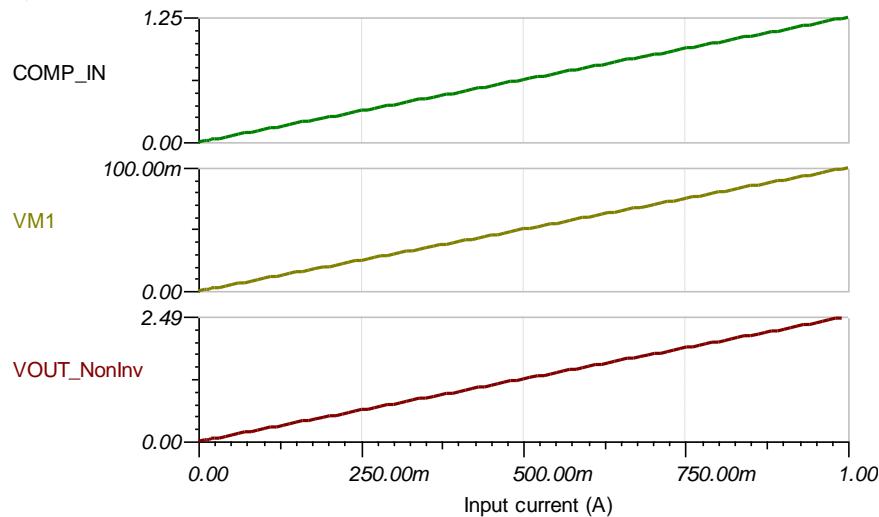
### DC Simulation Results (VOUT\_Inv)



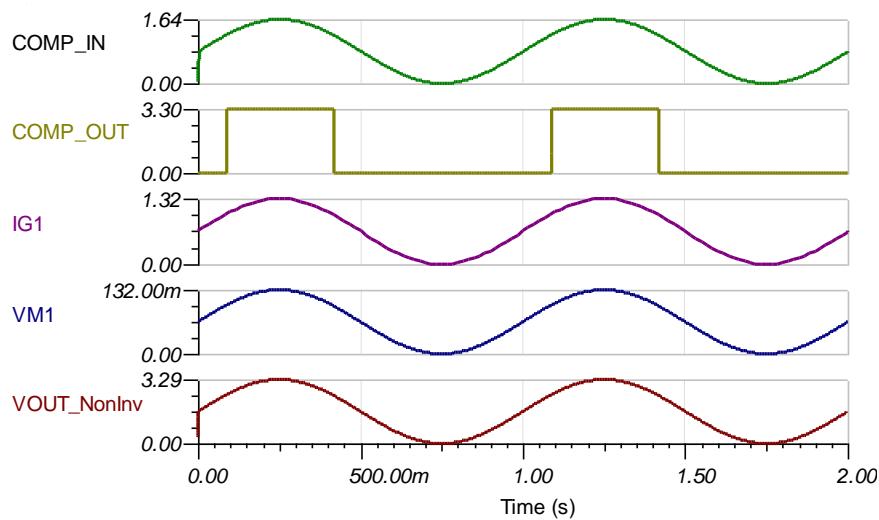
### Transient Simulation Results (VOUT\_Inv)



### DC Simulation Results (VOUT\_NonInv)



### Transient Simulation Results (VOUT\_NonInv)



### Tech Note and Blog References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See [Advantages of Using Nanopower Zero Drift Amp for Mobile Phone Battery Monitoring](#).

See [Current Sensing in No-Neutral Light Switches](#).

See [GPIO Pins Power Signal Chain in Personal Electronics Running on Li-Ion Batteries](#).

See [Current Sensing Using NanoPower Op Amps](#) Blog.

### Design Featured Op Amp

LPV821	
$V_s$	1.7V to 3.6V
<b>Input <math>V_{CM}</math></b>	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	1.5 $\mu$ V
$V_{os}$ Drift	20 nV/°C
$I_q$	650 nA/Ch
$I_b$	7 pA
<b>UGBW</b>	8 kHz
<b>#Channels</b>	1
LPV821	

### Design Alternate Op Amp

TLVx333	
$V_s$	1.8V to 5.5V
<b>Input <math>V_{CM}</math></b>	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	2 $\mu$ V
$V_{os}$ Drift	20 nV/°C
$I_q$	17 $\mu$ A/Ch
$I_b$	70 pA
<b>UGBW</b>	350 kHz
<b>#Channels</b>	1, 2, 4
TLV333	

### Revision History

Revision	Date	Change
A	February 2019	Changed title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page.

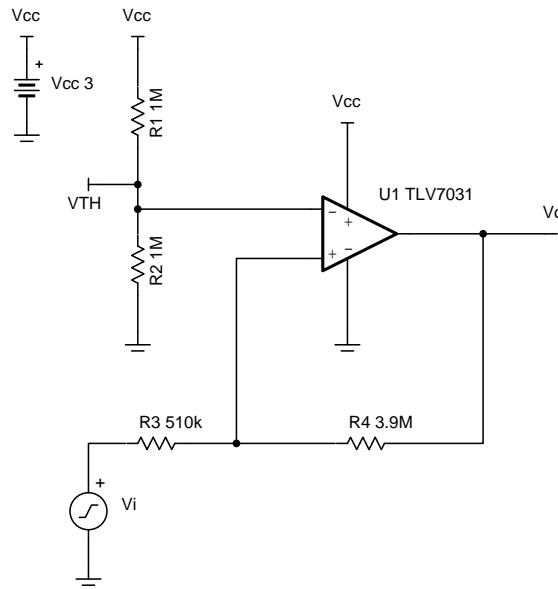
## Non-inverting comparator with hysteresis circuit

### Design Goals

Output		Hysteresis	Thresholds		Supply	
$V_o = \text{HIGH}$	$V_o = \text{LOW}$	$V_{\text{HYS}}$	$V_H$	$V_L$	$V_{\text{cc}}$	$V_{\text{ee}}$
$V_i > V_H$	$V_i < V_L$	400mV	1.7V	1.3V	3V	0V

### Design Description

Comparators are used to differentiate between two different signal levels. When setup in a non-inverting fashion, the comparator output will be a digital high if the analog input is above a selected threshold. With noise, signal variation, or a slow-moving signal at the comparison threshold, undesirable transitions at the output can be observed. Setting upper and lower hysteresis thresholds eliminates these undesirable output transitions caused by the noise. This circuit example will focus on the steps required to design the positive feedback resistor network required to obtain the necessary hysteresis for a non-inverting comparator application.

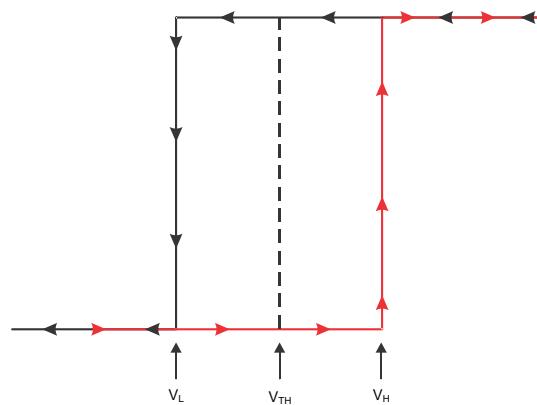


### Design Notes

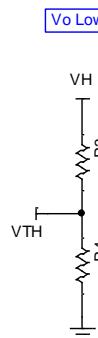
1. Achieving balanced hysteresis will depend on the size of hysteresis and the threshold voltage to  $V_{\text{cc}}$  ratio.
2. In comparison to the inverting comparator circuit, this example has a lower impedance seen at the inputs.
3. The accuracy of the hysteresis threshold voltages are related to the tolerance of the resistors used in the circuit, the selected comparator's input offset voltage specification, and any internal hysteresis already applied to the device.
4. For the TLV7031,  $V_{\text{OH}}$  is approximately 200mV below  $V_{\text{cc}}$  and  $V_{\text{OL}}$  is approximately 250mV above  $V_{\text{ee}}$ .
5. The TLV7031 has a push-pull output stage, so no pull-up resistor is needed.

### Design Steps

1. Select  $R_1$ . This can be a high resistance value due to the very low input bias current caused by the CMOS input of the device.  
 $R_1 = 1M\Omega$  (Standard Value)
2. Solve for  $R_3$ . A common practice is to select  $R_3$  to be the impedance seen at the inverting pin to provide input bias current cancellation. Since  $R_2$  is not known, approximate  $R_3$ . Here  $V_{TH}$  is expected to be 50% of  $V_{cc}$ .  
 $R_3 = R_1 \parallel R_2 \approx \frac{1}{2}R_1 = 500k\Omega$   
 $R_3 = 510k\Omega$  (Standard Value)
3. Observe the feedback resistor network in the two possible output states: Low and High. Note that the input signal plays a role in determining the hysteresis. The hysteresis eye diagram follows.

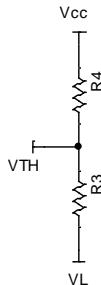


4. Derive the equation for  $V_H$ , the voltage that the input signal must rise to for the output to switch high. Set the voltage at the non-inverting pin to be equal to  $V_{TH}$ . This ensures the correct hysteresis window will be achieved.



$$V_H = R_3 \times \frac{V_{TH}}{R_4} + V_{TH}$$

5. Derive the equation for  $V_L$ , the voltage that the input signal must drop to for the output to switch low. Again, set the voltage at the non-inverting pin to be equal to  $V_{TH}$ .

**[Vo High]**


6. For push-pull outputs.

$$V_L = \frac{V_{TH} \times (R_3 + R_4) - V_{cc} \times R_3}{R_4}$$

7. If the comparator in use has an open-drain or open-collector output stage, then the pull-up resistor,  $R_{pu}$ , will be in series with  $R_3$  and  $R_4$ . The following equation is true if  $V_{pu} = V_{cc}$ . Do note that for some applications, the pull-up resistor could be ignored in the  $V_L$  equation since the eventual feedback resistor value could be significantly larger (ideally 10 times larger) than the pull-up resistor.

$$V_L = \frac{V_{TH} \times (R_{pu} + R_4) - (V_{cc} - V_{TH}) \times R_3}{R_4 + R_{pu}}$$

8. If  $V_{pu} \neq V_{cc}$ , then use the following equation for  $V_L$ .

$$V_L = \frac{V_{TH} \times (R_{pu} + R_4) - (V_{pu} - V_{TH}) \times R_3}{R_4 + R_{pu}}$$

9. Derive the equation for  $V_{HYS}$ .

$$V_{HYS} = V_H - V_L = V_{cc} \times \frac{R_3}{R_4}$$

10. Solve for  $R_4$ .

$$R_4 = \frac{V_{cc}}{V_{HYS}} \times R_3 = \frac{3V}{0.4V} \times 510k\Omega = 3.83M\Omega$$

$$R_4 = 3.9M\Omega \text{ (Standard Value)}$$

11. Use the  $V_H$  equation found in step 4 to now solve for  $V_{TH}$ .

$$V_{TH} = \frac{R_4 \times V_H}{R_3 + R_4} = \frac{3.9M\Omega \times 1.7V}{510k\Omega + 3.9M\Omega} = 1.50V$$

12. Verify the  $V_{TH}$  value with the  $V_L$  equation found in step 6.

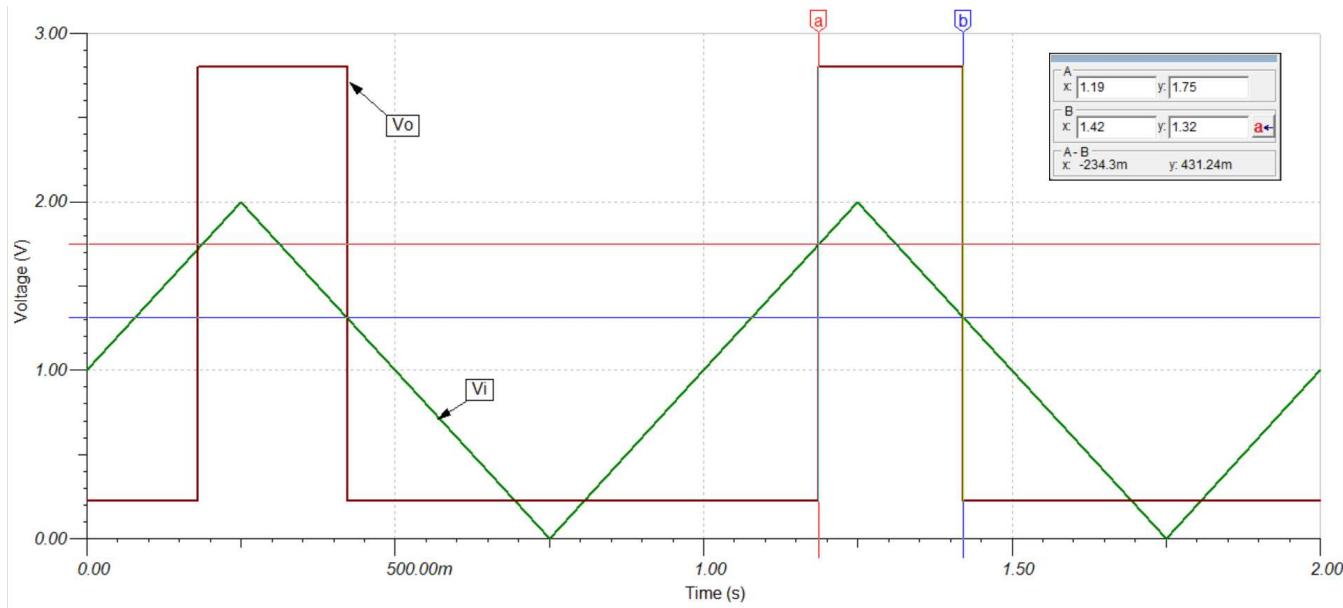
$$V_{TH} = \frac{R_4 \times V_H}{R_3 + R_4} = \frac{3.9M\Omega \times 1.7V}{510k\Omega + 3.9M\Omega} = 1.50V$$

13. Solve for  $R_2$  based on the calculated threshold voltage,  $V_{TH}$ .

$$R_2 = \frac{R_1 \times V_{TH}}{V_{cc} - V_{TH}} = \frac{1M\Omega \times 1.5V}{3V - 1.5V} = 1M\Omega$$

## Design Simulations

### Transient Simulation Results



### Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See Circuit SPICE Simulation File [SLVMCR2](#).

For more information on many comparator topics including hysteresis, propagation delay and input common mode range please see [training.ti.com/ti-precision-labs-op-amps](#).

### Design Featured Comparator

TLV7031	
<b>Output Type</b>	Push-Pull
$V_{cc}$	1.6V to 6.5V
$V_{inCM}$	Rail-to-rail
$V_{os}$	$\pm 100\mu V$
$V_{HYS}$	7mV
$I_q$	335nA/Ch
$t_{pd}$	3 $\mu s$
<b>#Channels</b>	1
	<a href="http://www.ti.com/product/tlv7031">www.ti.com/product/tlv7031</a>

### Design Alternate Comparator

TLV1701	
<b>Output Type</b>	Open Collector
$V_{cc}$	2.2V to 36V
$V_{inCM}$	Rail-to-rail
$V_{HYS}$	N/A
$V_{os}$	$\pm 500\mu V$
$I_q$	55 $\mu A/Ch$
$t_{pd}$	560ns
<b>#Channels</b>	1, 2, 4
	<a href="http://www.ti.com/product/tlv1701">www.ti.com/product/tlv1701</a>

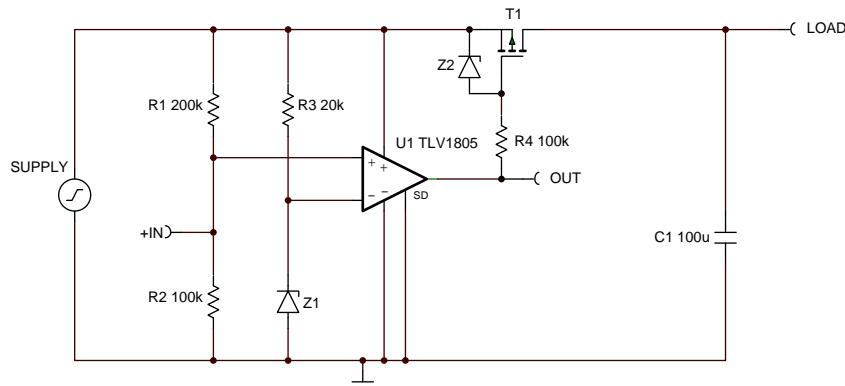
## Overvoltage protection with comparator circuit

### Design Goals

Supply	Load	Comparator Output Status (OUT)	
Operating Voltage Range	MAX Operating Voltage ( $V_{OVER}$ )	SUPPLY $< V_{OVER}$	SUPPLY $\geq V_{OVER}$
12V to 36V	30V	$V_{OL} < 0.4V$	$V_{OH} = SUPPLY$

### Design Description

This overvoltage protection circuit uses a high-voltage comparator with a push-pull output stage to control a P-Channel MOSFET that connects the SUPPLY to the LOAD. When the SUPPLY voltage exceeds the overvoltage threshold ( $V_{OVER}$ ), the output of the comparator goes HIGH and disconnects the LOAD from the SUPPLY by opening the P-Channel MOSFET. Likewise, when the SUPPLY voltage is below  $V_{OVER}$ , the output of the comparator is LOW and connects the LOAD to the SUPPLY.



### Design Notes

1. Select a high-voltage comparator with a push-pull output stage.
2. Select a reference voltage that is below the lowest operating voltage range for the SUPPLY.
3. Calculate values for the resistor divider so the critical overvoltage level occurs when the input to the comparator (+IN) reaches the comparator's reference voltage.
4. Limit the source-gate voltage of the P-Channel MOSFET so that it remains below the device's maximum allowable value.

### Design Steps

1. Select a high-voltage comparator with a push-pull output stage that can operate at the highest possible SUPPLY voltage. In this application, the highest SUPPLY voltage is 36V.
2. Determine an appropriate reference level for the overvoltage detection circuit. Since the lowest operating voltage for the SUPPLY is 12V, a 10V zener diode ( $Z_1$ ) is selected for the reference ( $V_{REF}$ ).
3. Calculate value of  $R_3$  by considering the minimum bias current to keep the  $Z_1$  regulating at 10V. A minimum bias current of 100 $\mu$ A is used along with the minimum SUPPLY voltage of 12V.

$$R_3 = \frac{\text{SUPPLY (min)} - V_{ZENER}}{I_{BIAS} (\text{min})} = \frac{12V - 10V}{100\mu A} = 20 \text{ k}\Omega$$

4. Calculate the resistor divider ratio needed so the input to the comparator (+IN) crosses the reference voltage (10V) when the SUPPLY rises to the target overvoltage level ( $V_{OVER}$ ) of 30V.

$$V_{REF} = V_{OVER} \times \left( \frac{R_2}{R_1 + R_2} \right)$$

$$\left( \frac{R_2}{R_1 + R_2} \right) = \frac{V_{REF}}{V_{OVER}} = \frac{10V}{30V} = 0.333$$

5. Select values for  $R_1$  and  $R_2$  that yield the resistor divider ratio of 0.333V by using the following equation or using the online "Voltage Divider Calculator" at [http://www.ti.com/download/kbase/volt/volt\\_div3.htm](http://www.ti.com/download/kbase/volt/volt_div3.htm).

If using the following equation, choose a value for  $R_2$  in the 100k-ohm range and calculate for  $R_1$ . In this example, a value of 100k was chosen for  $R_2$ .

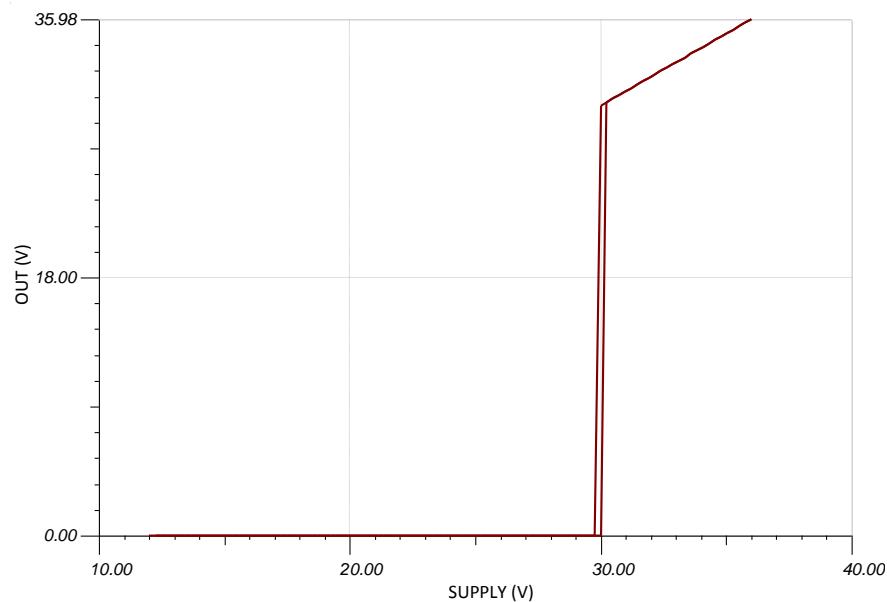
$$R_1 = R_2 \left( \frac{V_{OVER}}{V_{REF}} - 1 \right) = 100 \text{ k}\Omega \left( \frac{30V}{10V} - 1 \right) = 200 \text{ k}\Omega$$

6. Note that the TLV1805 which is used in application circuit has 15mV of hysteresis. This means that the actual switching threshold will be 7.5mV higher than the switching threshold ( $V_{REF}$ ) when the SUPPLY is rising and 7.5mV lower when the SUPPLY is falling. The result of the hysteresis is most easily seen in the DC Simulation curve. Since SUPPLY is resistor divided down by a factor of 3, the net impact to the SUPPLY switching threshold is 3 times this amount.
7. Verify that the current through the resistor divider is at least 100 times higher than the input bias current of the comparator. The resistors can have high values to minimize power consumption in the circuit without adding significant error to the resistor divider.
8. Select a zener diode ( $Z_2$ ) to limit the source-gate voltage ( $V_{SG}$ ) of the P-Channel MOSFET so that it remains below the device's maximum allowable value. It is common for P-Channel, power MOSFETs to have a  $V_{SG}$  max value of 20V, so a 16V zener is placed from source to gate.
9. Calculate a value for the current limiting resistor ( $R_4$ ). When SUPPLY rises above 16V and  $Z_2$  begins to conduct,  $R_4$  limits the amount of current that the comparator output will sink when its output is LOW. With a nominal SUPPLY voltage of 24V, the sink current is limited to 80 $\mu$ A.

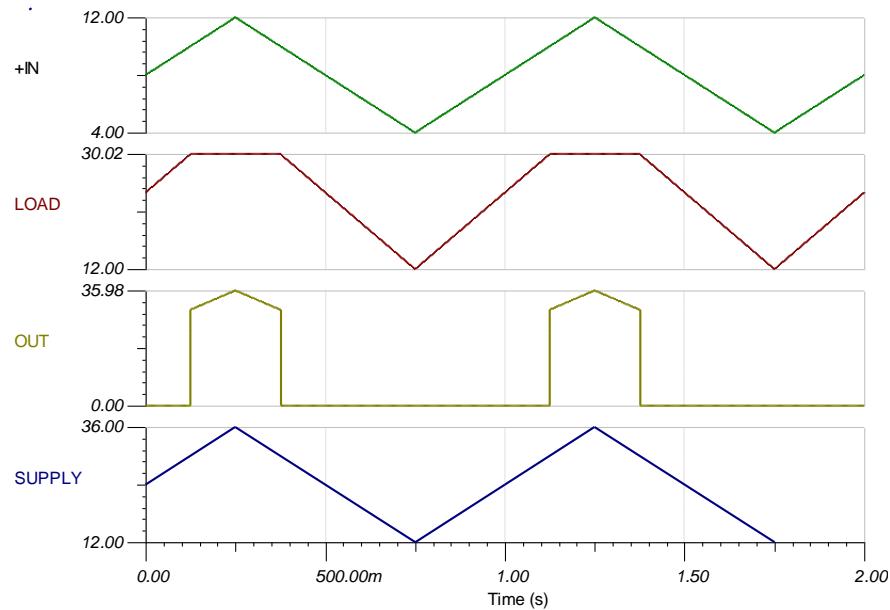
$$I_{SINK} = \left( \frac{\text{SUPPLY} - V_{Z2}}{R_4} \right) = \left( \frac{24V - 16V}{100 \text{ k}\Omega} \right) = 80 \text{ }\mu\text{A}$$

## Design Simulations

### DC Simulation Results



### Transient Simulation Results



**References:**

1. [Analog Engineer's Circuit Cookbooks](#)
2. [SPICE Simulation File SNOAA20](#)
3. [TI Precision Labs](#)

**Design Featured Comparator**

TLV1805-Q1 / TLV1805	
$V_S$	3.3 V to 40 V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Push-Pull
$V_{os}$	500 $\mu$ V
Hysteresis	15 mV
$I_Q$	135 $\mu$ A
$t_{PD(HL)}$	250 ns
<a href="http://www.ti.com/product/tlv1805">www.ti.com/product/tlv1805</a>	

**Design Alternate Comparator**

	TLV3701 / TLV370x-Q1	TLC3702 / TLC3702-Q1
$V_S$	2.5 V to 16 V	4V to 16 V
$V_{inCM}$	Rail-to-rail	-1 V from VDD
$V_{out}$	Push-Pull	Push-Pull
$V_{os}$	250 $\mu$ V	1.2 mV
Hysteresis	n/a	n/a
$I_Q$	0.56 $\mu$ A	9.5 $\mu$ A/Ch
$t_{PD(HL)}$	36 $\mu$ s	0.65 $\mu$ s
	<a href="http://www.ti.com/product/tlv3701">www.ti.com/product/tlv3701</a>	<a href="http://www.ti.com/product/tlc3702">www.ti.com/product/tlc3702</a>

## Window comparator with integrated reference circuit

### Design Goals

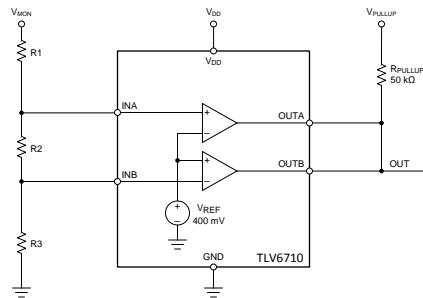
Input		Output		Supply	
$V_{MON\ Min}$	$V_{MON\ Max}$	$V_{OUT\ Min}$	$V_{OUT\ Max}$	$V_{DD}$	$V_{REF}$
0V	6V	0V	3.3V	3.3V	400mV

Lower Threshold ( $V_L$ )	Upper Threshold ( $V_H$ )	Divider Load Current ( $I_{MAX}$ ) at $V_H$
3.2V	4.1V	10uA

### Design Description

This circuit utilizes the TLV6710, which contains two comparators and a precision internal reference of 400mV. The monitored voltage ( $V_{MON}$ ) is divided down by  $R_1$ ,  $R_2$ , and  $R_3$ . The voltage across  $R_2$  and  $R_3$  is compared to the 400mV internal reference voltage ( $V_{REF}$ ). If the input signal ( $V_{MON}$ ) is within the window, the output is high. If the signal level is outside of the window, the output is low.

The TLV6710 will be utilized for this example, which conveniently contains two comparators and a common precision internal reference trimmed to a 400mV threshold. Two discrete comparators and an external reference may also be used.



### Design Notes

1. Make sure the comparator input voltage range is not violated at the highest expected  $V_{MON}$  voltage.
2. If the outputs are to be combined together (ORed), open collector or open drain output devices must be used.
3. It is also recommended to repeat the following calculations using the minimum and maximum resistor tolerance values and comparator positive and negative offset voltages.
4. The TLV6710 has built-in asymmetrical hysteresis, resulting in the rising edge  $V_L$  and falling edge  $V_H$  being slightly shifted. Comparators without hysteresis will meet the calculated thresholds.

## Design Steps

The resistor divider will be calculated in separate  $V_H$  and  $V_L$  segments to create 400mV at the appropriate comparator input at the desired threshold voltage.

1. The total divider resistance  $R_{TOTAL}$  is calculated from the upper threshold voltage and divider current:

$$R_{TOTAL} = R_1 + R_2 + R_3 = \frac{V_H}{I_{MAX}} = \frac{4.1V}{10\mu A} = 410k\Omega$$

2. The upper threshold voltage is set by the "bottom" divider resistor  $R_3$  going into the INB pin. From the reference voltage and the divider current, the value of  $R_3$  is calculated from:

$$R_3 = \frac{V_{REF}}{I_{MAX}} = \frac{400mV}{10\mu A} = 40k\Omega$$

3. The "middle" resistor  $R_2$  is found by looking at  $R_2$  and  $R_1$  as one resistor, and calculating the value for that total resistance for  $V_{REF}$  at  $V_L$ , then subtracting out the known  $R_3$ :

$$R_2 = \left( \left( \frac{R_{TOTAL}}{V_L} \times V_{REF} \right) - R_3 \right) = \left( \left( \frac{410k\Omega}{3.2V} \times 400mV \right) - 40k\Omega \right) = 11.25k\Omega$$

4.  $R_1$  is found by taking the total resistance and subtracting the sum of  $R_2$  and  $R_3$ :

$$R_1 = R_{TOTAL} - (R_2 + R_3) = 410k\Omega - (11.25k\Omega + 40k\Omega) = 358.75k\Omega$$

Because these are calculated ideal resistor values, the next closest 0.1% standard resistor values will be used. The following table summarizes the changes due to the resistor value changes and the resulting trip point voltage change.

### Nearest 0.1% Resistor Values

Resistor	Calculated Ideal Value	Nearest Standard 0.1% (E192) Value
$R_1$	358.750 k $\Omega$	361 k $\Omega$
$R_2$	11.25 k $\Omega$	11.3 k $\Omega$
$R_3$	40 k $\Omega$	40.2 k $\Omega$

Because the values of the divider string resistors were changed, the resulting new threshold voltages must be calculated. The thresholds are found by multiplying the divider ratio by the reference voltage:

$$V_H = \left( \frac{R_1 + R_2 + R_3}{R_3} \right) \times V_{REF} = \left( \frac{361k\Omega + 11.3k\Omega + 40.2k\Omega}{40.2k\Omega} \right) \times 0.4V = 10.26119 \times 0.4V = 4.1045V$$

$$V_L = \left( \frac{R_1 + R_2 + R_3}{R_2 + R_3} \right) \times V_{REF} = \left( \frac{361k\Omega + 11.3k\Omega + 40.2k\Omega}{11.3k\Omega + 40.2k\Omega} \right) \times 0.4V = 8.0097 \times 0.4V = 3.2039V$$

### Ideal and Standard Resistor Thresholds

Threshold	Using Ideal Resistors	Using Standard Resistors	Percent Change
$V_H$	4.1V	4.1045V	+0.109%
$V_L$	3.2V	3.2039V	+0.121%

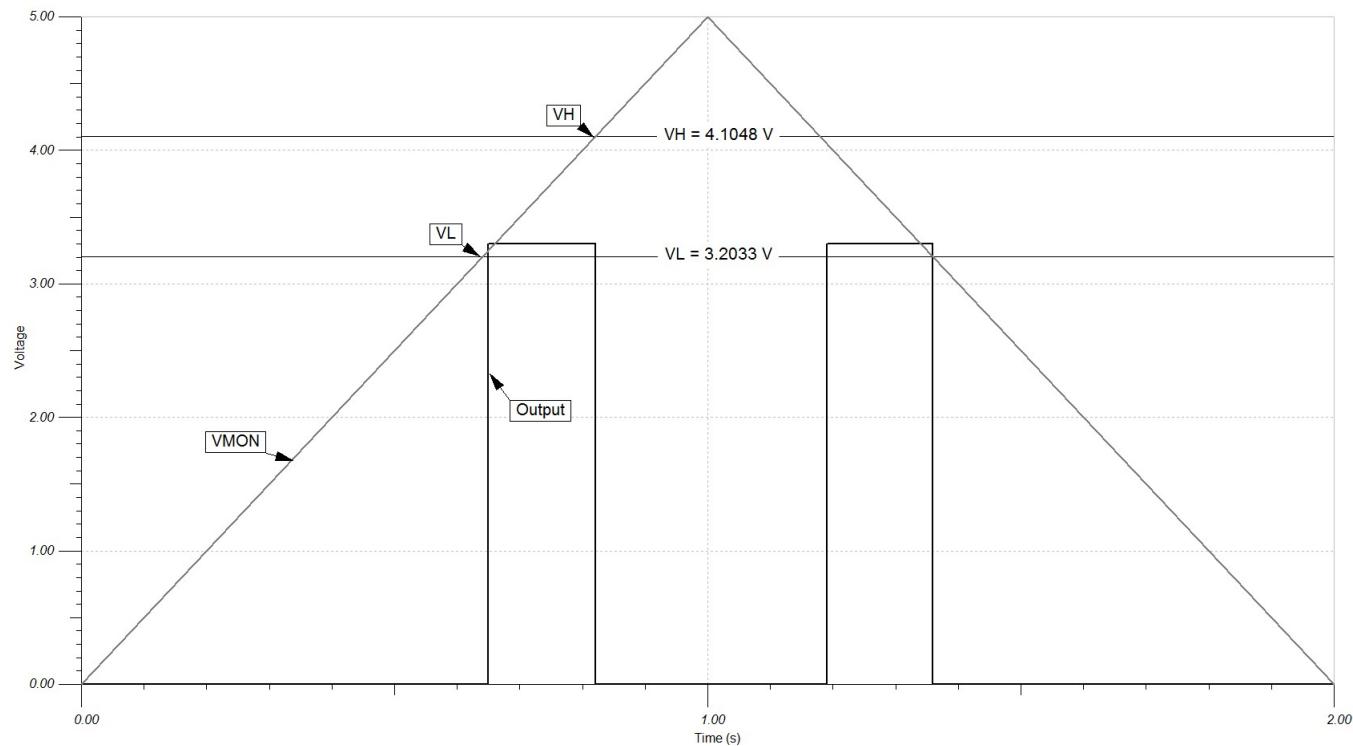
To ensure that the maximum 6V  $V_{MON}$  voltage does not violate the TLV6710 1.7V maximum input voltage rating, the  $V_{MON\_MAX}$  and the  $V_L$  division ratio found in step 4 above are used to calculate the maximum voltage at the TLV6710 input:

$$V_{INPUT\_MAX} = \frac{V_{MON\_MAX}}{V_{L\_RATIO}} = \frac{6V}{8.0097} = 749.1mV$$

The value 749mV is less than 1.7V, so the input voltage is well below the input maximum. If using discrete comparators, make sure the voltage is within the specified input common mode range ( $V_{ICR}$ ) of the device used.

## Design Simulations

### Transient Simulation Results



Note: The Rising edge  $V_L$  and falling edge  $V_H$  thresholds are slightly shifted due to the built-in asymmetrical hysteresis of the TLV6710. Comparators without hysteresis will meet the calculated thresholds.

## Design References

For more information on many comparator topics including input voltage range, output types and propagation delay, please visit [TI Precision Labs - Comparator Applications](#).

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See TINA-TI™ TLV6710 Reference Design circuit simulation file, Literature Number [SNVMB09](#).

## Design Featured Comparator

TLV6710	
$V_{ss}$	2V to 36 V
$V_{inCM}$	0V to 1.7V
$V_{out}$	0V to 25V
$V_{ref}$	400 mV $\pm 0.25\%$
$I_q$	11 $\mu$ A
$I_b$	1 nA
<b>Prop Delay</b>	10 $\mu$ s
<b>#Channels</b>	2
<a href="http://www.ti.com/product/tlv6710">www.ti.com/product/tlv6710</a>	

## Design Alternate Comparator

TLV6700	
$V_{ss}$	1.8V to 18 V
$V_{inCM}$	0V to 6.5V
$V_{out}$	0V to 18V
$V_{ref}$	400 mV $\pm 0.5\%$
$I_q$	5.5 $\mu$ A
$I_b$	1 nA
<b>Prop Delay</b>	29 $\mu$ s
<b>#Channels</b>	2
<a href="http://www.ti.com/product/tlv6700">www.ti.com/product/tlv6700</a>	

## Design Alternate Comparator

TLV1702	
$V_{ss}$	2.7 to 36 V
$V_{inCM}$	Rail to Rail
$V_{out}$	Open Drain to 36 V
$V_{os}$	$\pm 3.5$ mV
$I_q$	75 $\mu$ A
$I_b$	15 nA
<b>Prop Delay</b>	0.4 $\mu$ s
<b>#Channels</b>	2
<a href="http://www.ti.com/product/tlv1702">www.ti.com/product/tlv1702</a>	

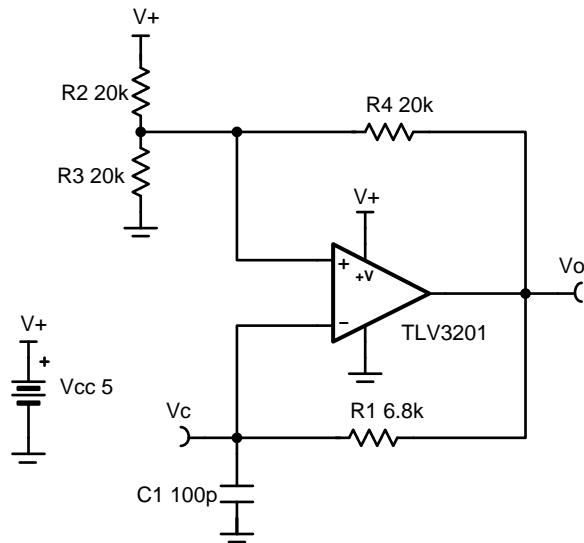
## Relaxation oscillator circuit

### Design Goals

Supply		Oscillator Frequency
$V_{cc}$	$V_{ee}$	$f$
5V	0V	1 MHz

### Design Description

The oscillator circuit generates a square wave at a selected frequency. This is done by charging and discharging the capacitor,  $C_1$ , through the resistor,  $R_1$ . The oscillation frequency is determined by the RC time constant of  $R_1$  and  $C_1$ , and the threshold levels set by the resistor network of  $R_2$ ,  $R_3$ , and  $R_4$ . The maximum frequency of the oscillator is limited by the toggle rate of the comparator and the capacitance load at the output. This oscillator circuit is commonly used as a time reference or a supervisor clock source.



### Design Notes

1. Comparator toggle rate and output capacitance are critical considerations when designing a high-speed oscillator.
2. Select  $C_1$  to be large enough to minimize the errors caused by stray capacitance.
3. If using a ceramic capacitor, select a COG or NPO type for best stability over temperature.
4. Select lower value resistors for the  $R_2$ ,  $R_3$ ,  $R_4$  resistor network to minimize the effects of stray capacitance.
5.  $R_2$ ,  $R_3$ , and  $R_4$  can be adjusted in order to create a duty cycle other than 50%.

### Design Steps

1. When  $R_2 = R_3 = R_4$ , the resistor network sets the oscillator trip points of the non-inverting input at one-third and two-thirds of the supply.
2. When the output is high, the upper trip point will be set at two-thirds of the supply to bring the output back low.

$$V_o = V_s \left( \frac{R_3}{(R_2 \parallel R_4) + R_3} \right) = \frac{2}{3} V_s = 3.33V$$

3. When the output is low, the lower trip point will be set at one-third of the supply in order to bring the output back high.

$$V_o = V_s \left( \frac{R_3 \parallel R_4}{(R_3 \parallel R_4) + R_2} \right) = \frac{1}{3} V_s = 1.67V$$

4. The timing of the oscillation is controlled by the charging and discharging rate of the capacitor  $C_1$  through the resistor  $R_1$ . This capacitor sets the voltage of the inverting input of the comparator. Calculate the time to discharge the capacitor.

$$V_c = V_i e^{-\frac{t}{R_1 C_1}}$$

$$\frac{1.67}{3.33} = e^{-\frac{t}{R_1 C_1}}$$

$$t = 0.69 R_1 C_1$$

5. Calculate the time to charge the capacitor.

$$V_i = V_c (1 - e^{-\frac{t}{R_1 C_1}})$$

$$1.67 = 3.33 (1 - e^{-\frac{t}{R_1 C_1}})$$

$$\frac{1.67}{3.33} = e^{-\frac{t}{R_1 C_1}}$$

$$t = 0.69 R_1 C_1$$

6. The time for the capacitor to charge or discharge is given by  $0.69 R_1 C_1$ . With a target oscillator frequency of 1MHz, the time to charge or discharge should be 500ns.

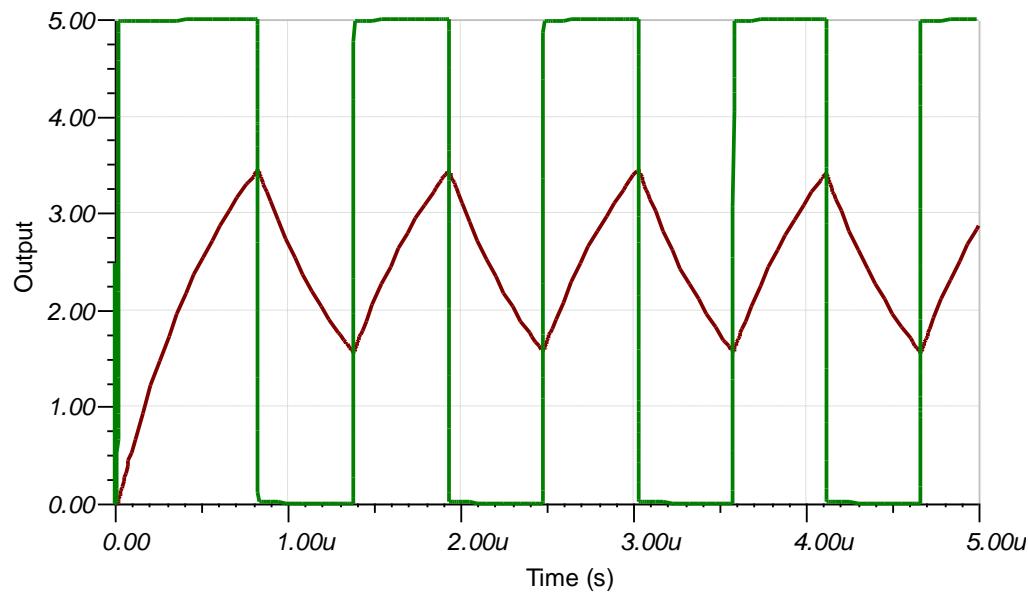
$$0.69 R_1 C_1 = 500\text{ns}$$

$$R_1 C_1 = 724\text{ns}$$

7. Select  $C_1$  as 100 pF and  $R_1$  as 6.8k $\Omega$  (the closest real world value).

**Design Simulations**

**Transient Simulation Results**



## Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit spice simulation file, [SBOMAO3](#).

For more information on many comparator topics including hysteresis, propagation delay and input common mode range please see, [TI Precision Labs](#).

## Design Featured Comparator

TLV3201	
$V_{ss}$	2.7 to 5.5V
$V_{inCM}$	Rail-to-rail
$t_{pd}$	40ns
$V_{os}$	1mV
$V_{HYS}$	1.2mV
$I_q$	40 $\mu$ A
<b>Output Type</b>	Push-Pull
<b>#Channels</b>	1
<a href="http://www.ti.com/product/tlv3201">www.ti.com/product/tlv3201</a>	

## Design Alternate Comparator

TLV7011	
$V_{ss}$	1.6 to 5.5V
$V_{inCM}$	Rail-to-rail
$t_{pd}$	260ns
$V_{os}$	0.5V
$V_{HYS}$	4mV
$I_q$	5 $\mu$ A
<b>Output Type</b>	Push-Pull
<b>#Channels</b>	1
<a href="http://www.ti.com/product/tlv7011">www.ti.com/product/tlv7011</a>	

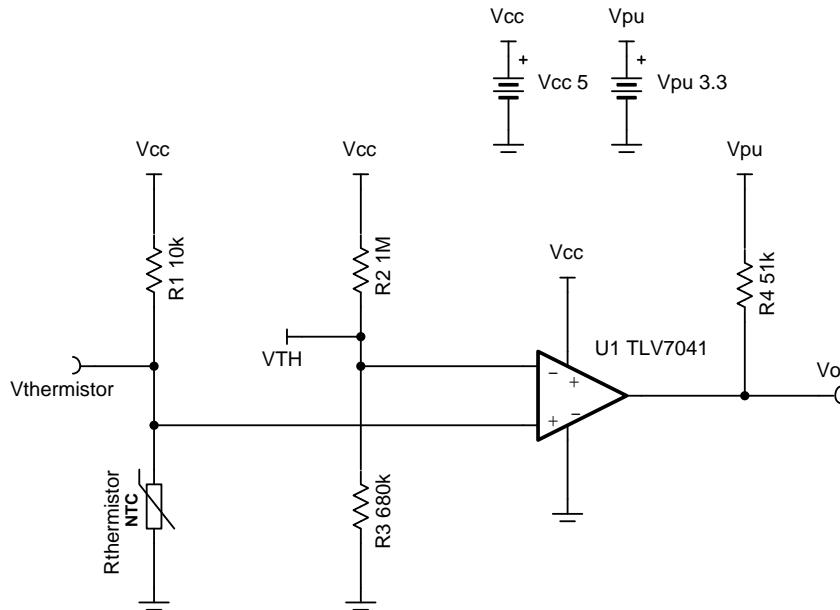
## Thermal switch circuit

### Design Goals

Temperature Switching Point	Output		Supply		
$T_{sp}$	$V_o = \text{HIGH}$	$V_o = \text{LOW}$	$V_{cc}$	$V_{ee}$	$V_{pu}$
100 °C	$T_A < T_{sp}$	$T_A > T_{sp}$	5V	0V	3.3V

### Design Description

This thermal switch solution will signal low (to a GPIO pin) when a certain temperature is exceeded thus alerting when conditions are no longer optimal or device-safe. This circuit incorporates an NTC thermistor with a comparator configured in a non-inverting fashion.



### Design Notes

1. The resistance of an NTC thermistor drops as temperature increases.
2. The TLV7041 has an open drain output, so a pull-up resistor is required.
3. Configurations where the thermistor is placed near the high side of the divider can be done; however, the comparator will have to be used in an inverting fashion to still have the output switch low.
4. To exercise good practice, a positive feedback resistor should be placed to add external hysteresis (for simplicity, it is not done in this example).

## Design Steps

1. Select an NTC thermistor, preferably one with a high nominal resistance,  $R_0$ , (resistance value when ambient temperature,  $T_A$ , is 25 °C) since the TLV7041 has a very low input bias current. This will help lower power consumption, thus reducing the likelihood of reading a slightly higher temperature due to thermal dissipation in the thermistor. The thermistor chosen has its  $R_0$  and its material constant,  $\beta$ , listed below.

$$R_0 = 100k\Omega$$

$$\beta = 3977K$$

2. Select  $R_1$ . For high temperature switching points,  $R_1$  should be 10 times smaller than the nominal resistance of the thermistor. This causes a larger voltage difference per temperature change around the temperature switching point, which helps guarantee the output will switch at the desired temperature value.

$$R_1 = \frac{R_0}{10}$$

$$R_1 = \frac{100k\Omega}{10} = 10k\Omega \text{ (Standard Value)}$$

3. Select  $R_2$ . Again, this can be a high resistance value.

$$R_2 = 1M\Omega \text{ (Standard Value)}$$

4. Solve for the resistance of the thermistor,  $R_{\text{thermistor}}$ , at the desired temperature switching point. Using the  $\beta$  formula is an effective approximation for thermistor resistance across the temperature range of -20 °C to 120 °C. Alternatively, the Steinhart-Hart equation can be used, but several device-specific constants must be provided by the thermistor vendor. Note that temperature values are in Kelvin. Here  $T_0 = 25$  °C = 298.15K.

$$R_{\text{thermistor}}(T_{\text{sp}}) = R_0 \times e^{\beta \times \left( \frac{1}{T_{\text{sp}}} - \frac{1}{T_0} \right)}$$

$$R_{\text{thermistor}}(100\text{ }^{\circ}\text{C}) = 100k\Omega \times e^{3977K \times \left( \frac{1}{373.15K} - \frac{1}{298.15K} \right)}$$

$$R_{\text{thermistor}}(100\text{ }^{\circ}\text{C}) = 6.85 \text{ k}\Omega$$

5. Solve for  $V_{\text{thermistor}}$  at  $T_{\text{sp}}$ .

$$V_{\text{thermistor}}(T_{\text{sp}}) = V_{\text{cc}} \times \frac{R_{\text{thermistor}}(T_{\text{sp}})}{R_1 + R_{\text{thermistor}}(T_{\text{sp}})}$$

$$V_{\text{thermistor}}(100\text{ }^{\circ}\text{C}) = 5V \times \frac{6.85k\Omega}{10k\Omega + 6.85k\Omega} = 2.03V$$

6. Solve for  $R_3$  with the threshold voltage,  $V_{\text{TH}}$ , equal to  $V_{\text{thermistor}}$ . This ensures that  $V_{\text{thermistor}}$  will always be larger than  $V_{\text{TH}}$  until the temperature switching point is exceeded.

$$R_3 = \frac{R_2 \times V_{\text{TH}}}{V_{\text{cc}} - V_{\text{TH}}}$$

$$R_3 = \frac{1M\Omega \times 2.03V}{5V - 2.03V} = 685k\Omega$$

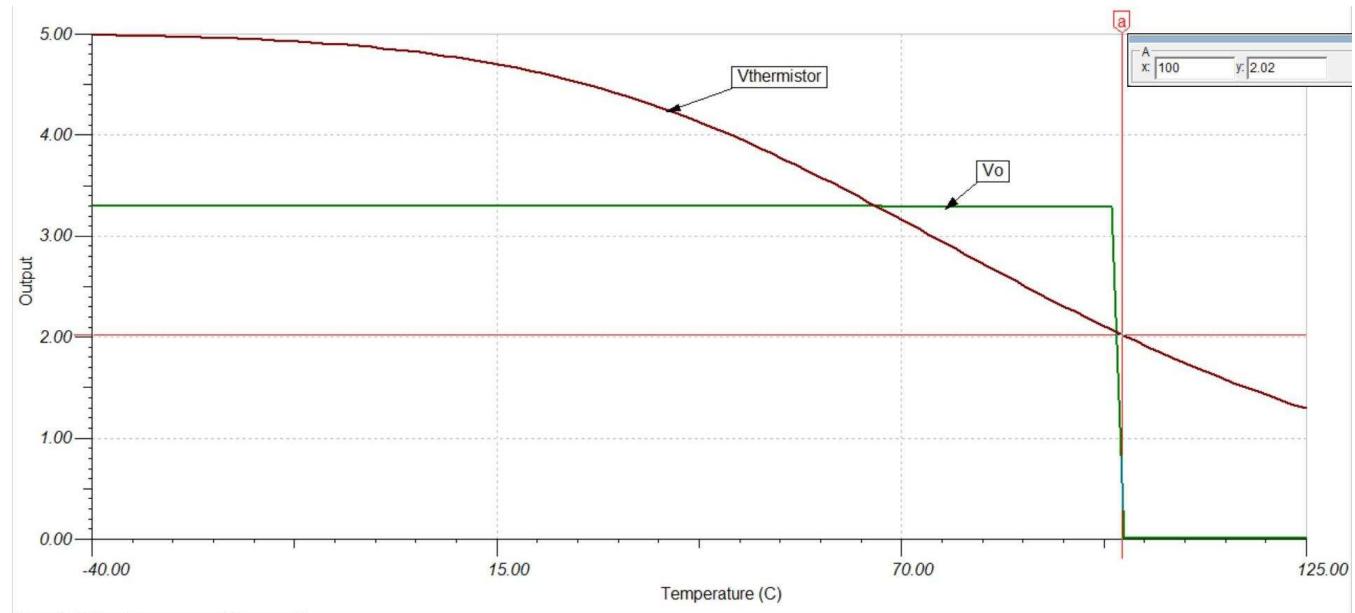
$$R_3 = 680k\Omega \text{ (Standard Value)}$$

7. Select an appropriate pull up resistor,  $R_4$ . Here,  $V_{\text{pu}} = 3.3V$  (digital high for a microcontroller).

$$R_4 = 51k\Omega \text{ (Standard Value)}$$

## Design Simulations

### DC Temperature Simulation Results



## Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See Circuit SPICE Simulation File SLVMCS1, [www.ti.com/lit/zip/slvmcs1](http://www.ti.com/lit/zip/slvmcs1).

## Design Featured Comparator

TLV7041	
<b>Output Type</b>	Open-Drain
$V_{cc}$	1.6V to 6.5V
$V_{inCM}$	Rail-to-rail
$V_{os}$	$\pm 100\mu V$
$V_{HYS}$	7mV
$I_q$	335nA/Ch
$t_{pd}$	3 $\mu s$
<b>#Channels</b>	1
<a href="http://www.ti.com/product/tlv7041">www.ti.com/product/tlv7041</a>	

## Design Alternate Comparator

TLV1701	
<b>Output Type</b>	Open-Collector
$V_{cc}$	2.2V to 36V
$V_{inCM}$	Rail-to-rail
$V_{os}$	$\pm 500\mu V$
$V_{HYS}$	N/A
$I_q$	55 $\mu A$ /Ch
$t_{pd}$	560ns
<b>#Channels</b>	1, 2, 4
	<a href="http://www.ti.com/product/tlv1701">www.ti.com/product/tlv1701</a>
	<a href="http://www.ti.com/product/tlv1701-q1">www.ti.com/product/tlv1701-q1</a>

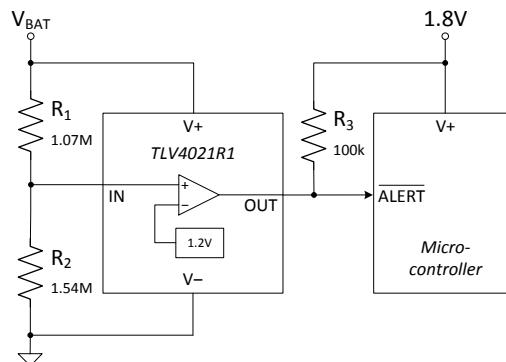
## ***Undervoltage protection with comparator circuit***

### **Design Goals**

Battery Voltage Levels ( $V_{BAT}$ )		Comparator Output Status (OUT)	
Undervoltage ( $V_{LOW}$ )	Start-Up Operating Voltage ( $V_{HIGH}$ )	Low Battery	Normal Operation
$< 2.000V$	$> 2.034V$	$V_{OL} < 0.4V$	$V_{OH} = V_{PU} = 1.8V$

### **Design Description**

This undervoltage protection circuit uses one comparator with a precision, integrated reference to create an alert signal at the comparator output (OUT) if the battery voltage sags below 2.0 V. The undervoltage alert in this implementation is ACTIVE LOW. So when the battery voltage drops below 2.0 V, the comparator output goes low, providing as an alert signal to whatever device is monitoring the output. Hysteresis is integrated in the comparator such that the comparator output will return to a logic high state when the battery voltage rises above 2.034 V. This circuit utilizes an open-drain output comparator in order to level shift the output high logic level for controlling a digital logic input pin. For applications needing to drive the gate of a MOSFET switch, a comparator with a push-pull output is preferred.



### **Design Notes**

1. Select a comparator with a precision, integrated reference.
2. Select a comparator with an open-drain output stage for level-shifting.
3. Select values for the resistor divider so the critical undervoltage level occurs when the input to the comparator (IN) reaches the comparator's negative-going input threshold voltage ( $V_{IT^-}$ ).

## Design Steps

1. Calculate the resistor divider ratio needed so the input to the comparator crosses  $V_{IT-}$  when  $V_{BAT}$  sags to the target undervoltage level ( $V_{LOW}$ ) of 2.0V.  $V_{IT-}$  from the TLV4021R1 data sheet is 1.18V.

$$V_{IT-} = \frac{R_2}{(R_1 + R_2)} \times V_{LOW}$$

$$\frac{R_2}{(R_1 + R_2)} = \frac{V_{IT-}}{V_{LOW}} = \frac{1.18 \text{ V}}{2.00 \text{ V}} = 0.59$$

2. Confirm that the value of  $V_{LOW}$ , the voltage level where the undervoltage alert signal is asserted, is 2.0 V.

$$V_{LOW} = \frac{R_1 + R_2}{R_2} \times V_{IT-} = \frac{1}{0.59} \times 1.18 \text{ V} = 2.0 \text{ V}$$

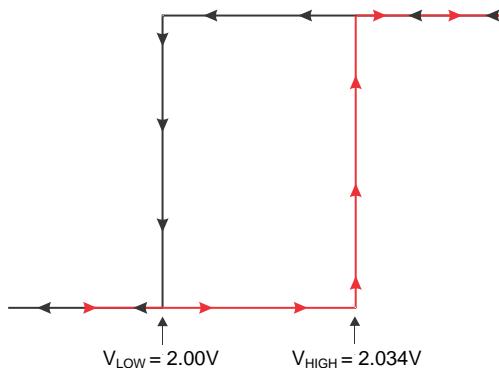
3. Select values for  $R_1$  and  $R_2$  that yield the resistor divider ratio of 0.59 by using the following equation or using the online tool "Voltage Divider Calculator" at [http://www.ti.com/download/kbase/volt/volt\\_div3.htm](http://www.ti.com/download/kbase/volt/volt_div3.htm).

If using the following equation, choose a value for  $R_2$  in the Mega-ohm range and calculate for  $R_1$ . In this example, a value of 1.54 M was chosen for  $R_2$ .

$$R_1 = R_2 \left( \frac{V_{LOW}}{V_{IT-}} - 1 \right) = 1.54 \text{ M}\Omega \left( \frac{2 \text{ V}}{1.18 \text{ V}} - 1 \right) = 1.07 \text{ M}\Omega$$

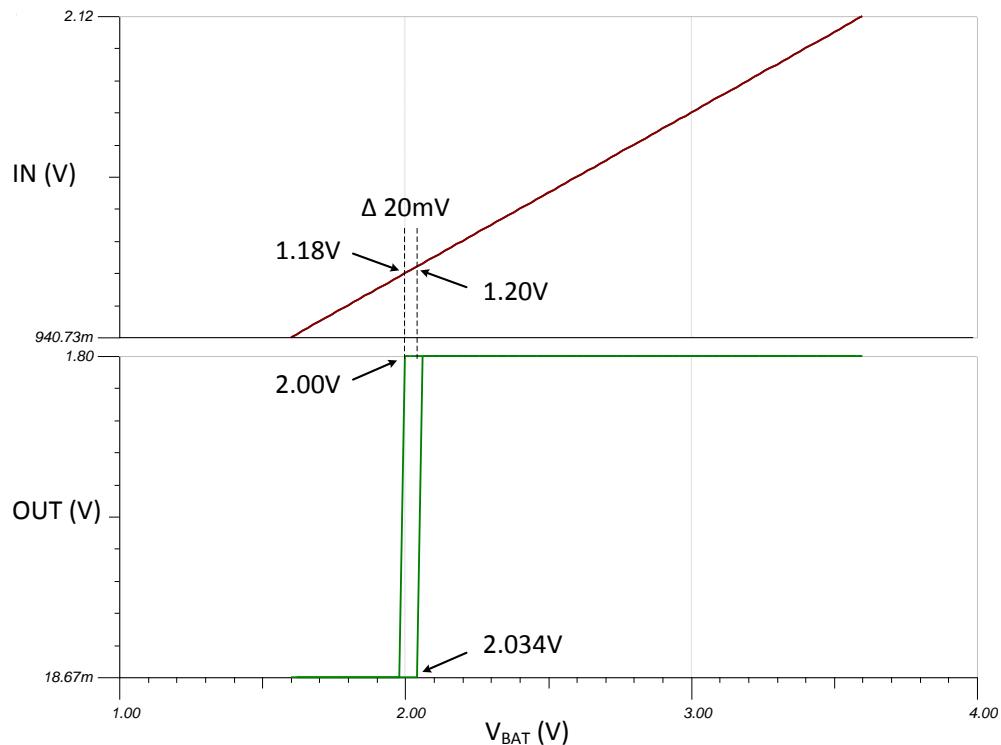
4. Verify that the current through the resistor divider is at least 100 times higher than the input bias current of the comparator. The resistors can have high values to minimize power consumption in the circuit without adding significant error to the resistor divider.
5. Calculate  $V_{HIGH}$ , the battery voltage where the undervoltage alert signal is de-asserted (returns to a logic high value). When the battery voltage reduces below the 2.0-V level or is ramping up at initial start-up, the comparator input needs to exceed ( $V_{IT+}$ ), the positive-going input threshold voltage for the output to return to a logic high.  $V_{IT+}$  from the TLV4021R1 data sheet is 1.20V.

$$V_{HIGH} = \frac{R_1 + R_2}{R_2} \times V_{IT+} = \frac{1.07 \text{ M}\Omega + 1.54 \text{ M}\Omega}{1.54 \text{ M}\Omega} \times 1.20 \text{ V} = 2.034 \text{ V}$$

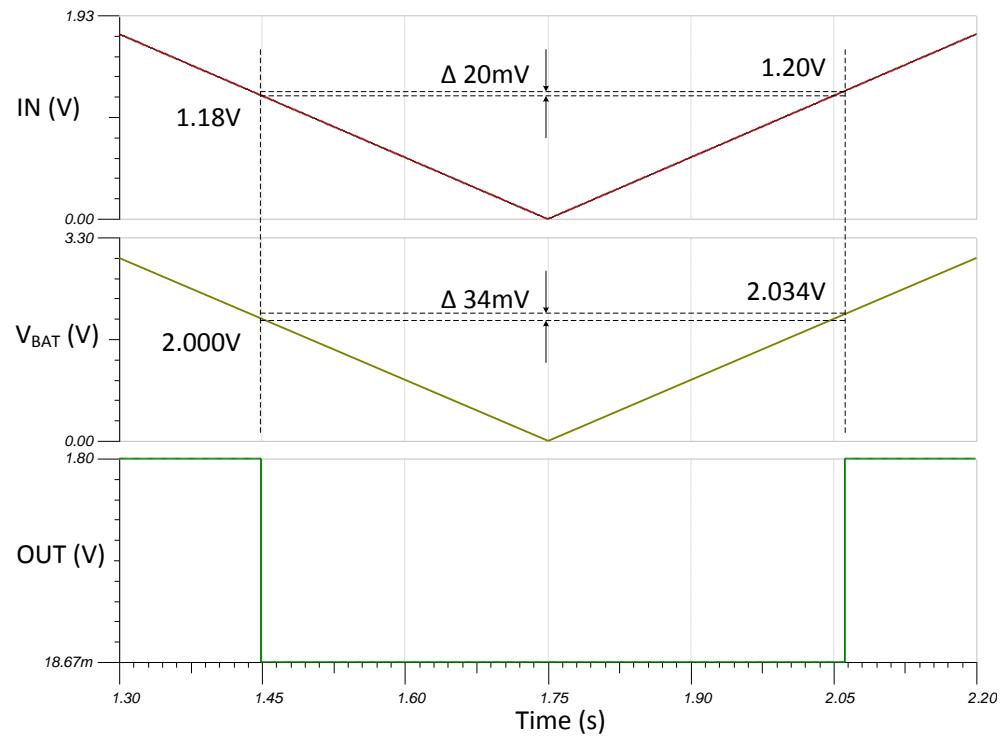


## Design Simulations

### DC Simulation Results



### Transient Simulation Results



**References:**

1. [Analog Engineer's Circuit Cookbooks](#)
2. [SPICE Simulation File – SNOAA18](#)
3. [TI Precision Labs](#)

**Design Featured Comparator**

TLV4021R1	
$V_S$	1.6V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Open Drain
<b>Integrated Reference</b>	1.2V $\pm 1\%$ over temperature
<b>Hysteresis</b>	20 mV
$I_Q$	2.5 $\mu$ A
$t_{PD(HL)}$	450 ns
<a href="http://www.ti.com/product/tlv4021">www.ti.com/product/tlv4021</a>	

**Design Alternate Comparator**

	TLV4041R1	TLV3011
$V_S$	1.6V to 5.5V	1.8V to 5.5V
$V_{inCM}$	Rail-to-rail	Rail-to-rail
$V_{out}$	Push-Pull	Open Drain
<b>Integrated Reference</b>	1.2 V $\pm 1\%$ over temperature	1.242 $\pm 1\%$ room temperature
<b>Hysteresis</b>	20mV	NA
$I_Q$	2.5 $\mu$ A	2.8 $\mu$ A
$t_{PD(HL)}$	450ns	6 $\mu$ s
	<a href="http://www.ti.com/product/tlv4041">www.ti.com/product/tlv4041</a>	<a href="http://www.ti.com/product/tlv3011">www.ti.com/product/tlv3011</a>

## Window comparator circuit

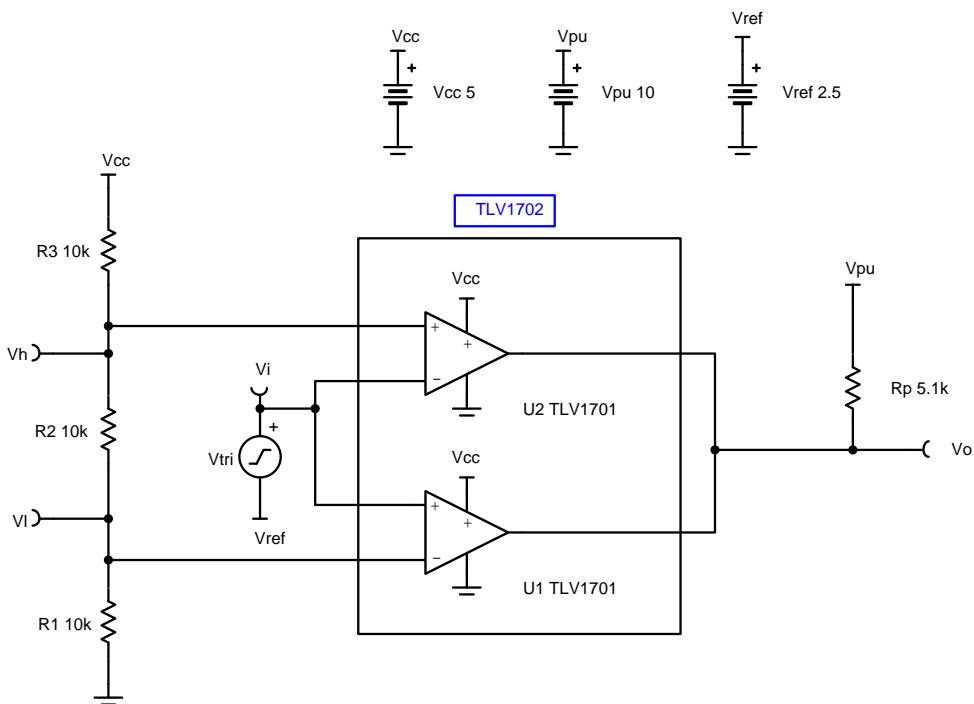
### Design Goals

Input		Output		Supply		
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	$V_{cc}$	$V_{ee}$	$V_{ref}$
0V	5V	0V	36V	5V	0V	2.5V

$V_L$ (Lower Threshold)	$V_H$ (Upper Threshold)	Upper to Lower Threshold Ratio
1.66V	3.33V	2

### Design Description

This circuit utilizes two comparators in parallel to determine if a signal is between two reference voltages. If the signal is within the window, the output is high. If the signal level is outside of the window, the output is low. For this design, the reference voltages are generated from a single supply with voltage dividers.



### Design Notes

1. The input should not exceed the common mode limitations of the comparators.
2. If higher pullup voltages are used,  $R_p$  should be sized accordingly to prevent large current draw. The TLV1701 supports pullup voltages up to 36V.
3. Comparator must be open-drain or open-collector to allow for the ORed output.

### Design Steps

1. Define the upper ( $V_H$ ) and lower ( $V_L$ ) window voltages.

$$V_H = V_{cc} \times \frac{R_1 + R_2}{R_1 + R_2 + R_3} = 3.33 \text{ V}$$

$$V_L = V_{cc} \times \frac{R_1}{R_1 + R_2 + R_3} = 1.66 \text{ V}$$

$$\frac{V_H}{V_L} = 1 + \frac{R_2}{R_1} = \frac{3.33V}{1.66V} = 2$$

2. Choose resistor values to achieve the desired window voltages.

$$\frac{V_H}{V_L} = 1 + \frac{R_2}{R_1} = 2, \text{ so } R_2 = R_1$$

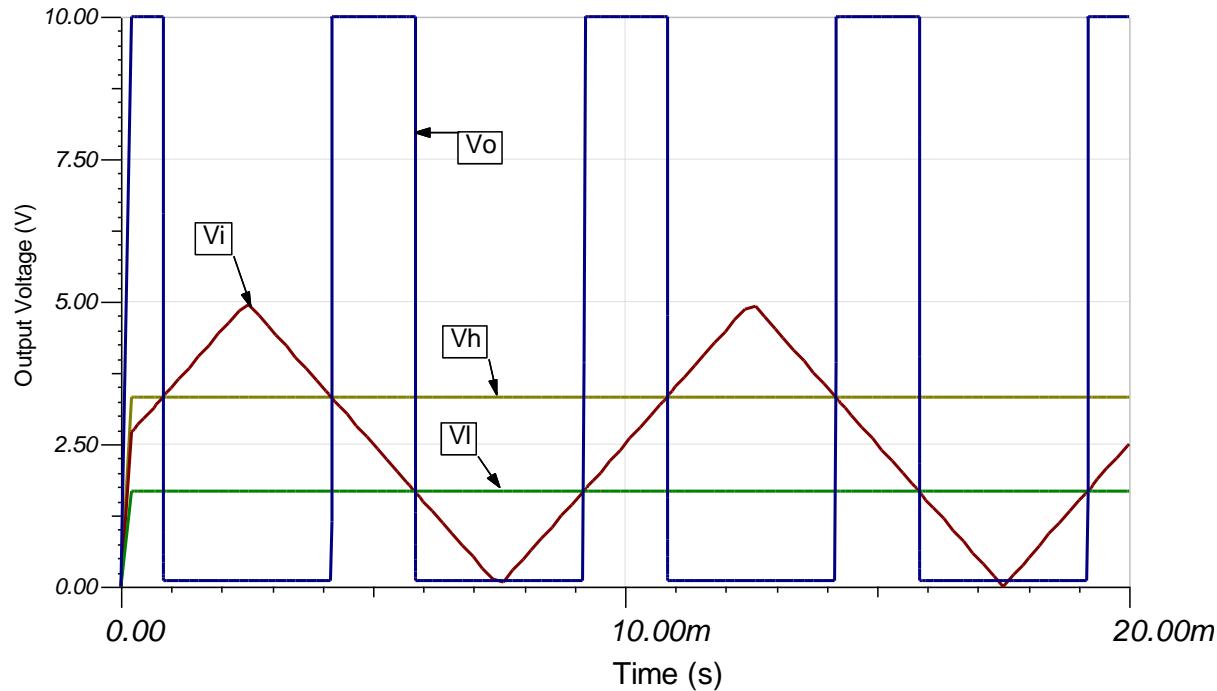
$R_1 = R_2 = 10\text{k}\Omega$  (Selected standard values)

$$R_3 = \frac{R_1 \times V_{cc}}{V_L} - (R_1 + R_2)$$

$$R_3 = \frac{10\text{k}\Omega \times 5\text{V}}{1.66\text{V}} - 20\text{k}\Omega = 10.12 \text{ k}\Omega \approx 10\text{k}\Omega \text{ (Standard Value)}$$

### Design Simulations

#### Transient Simulation Results



### Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See the circuit SPICE simulation file [SBOC516](#).

See TIPD178, [www.ti.com/tool/tipd178](#).

### Design Featured Op Amp

TLV1702	
$V_{cc}$	2.2V to 36V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Open Collector (36V Max)
$V_{os}$	2.5mV
$I_q$	75 $\mu$ A/Ch
$I_b$	15nA
<b>Rise Time</b>	365ns
<b>Fall Time</b>	240ns
<b>#Channels</b>	1, 2, 4
<a href="#">www.ti.com/product/tlv1702</a>	

### Revision History

Revision	Date	Change
A	February 2019	Downscale the title and changed title role to 'Amplifiers'. Added links to circuit cookbook landing page and SPICE simulation file.

## Zero crossing detection using comparator circuit

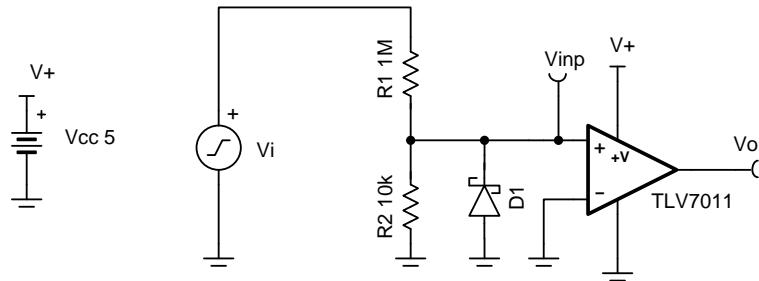
### Design Goals

Supply		Input Signal		MAX AC Mains Leakage Current
$V_{cc}$	$V_{ee}$	Type	$V_i$	$f$
5V	0V	Single	240V AC RMS	50Hz

$I_{ac}$   
<500 $\mu$ A

### Design Description

The zero crossing detector circuit changes the comparator's output state when the AC input crosses the zero reference voltage. This is done by setting the comparator inverting input to the zero reference voltage and applying the attenuated input to the noninverting input. The voltage divider  $R_1$  and  $R_2$  attenuates the input AC signal. The diode  $D_1$  is used to insure the noninverting input never goes below the negative input common mode limit of the comparator. Zero crossing detection is often used in power control circuits.



### Design Notes

1. Some hysteresis should be used to prevent unwanted transitions due to the slow speed of the input signal.
2. Select a comparator with a large input common mode range
3. The phase inversion protection feature of the TLV7011 can prevent phase reversal in situations where the input goes outside of the input common mode limits
4. A diode should be used to protect the comparator when the input goes below the negative input common mode limit.

**Design Steps**

1. Calculate the peak value of the input signal.

$$V_p = V_{RMS} \times \sqrt{2} = 340V$$

2. Select the resistor divider to attenuate the input 340V signal down to 3.4V in order to be within the positive common range of the comparator.

$$340V \times G = 3.4V$$

$$G = 0.01 \frac{V}{V}$$

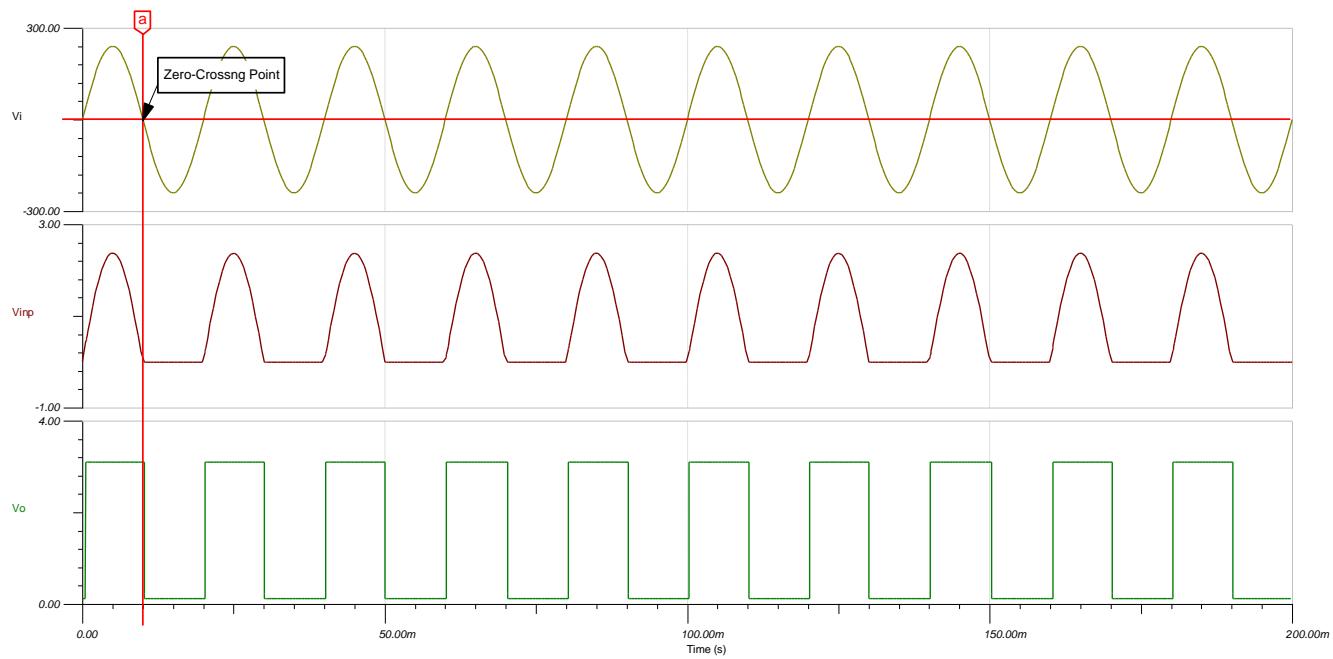
$$\left( \frac{R_2}{R_1+R_2} \right) = 0.01$$

3. Select  $R_1$  as  $1M\Omega$  and  $R_2$  as  $10k\Omega$  (the closest 1% value).
4. Select the diode,  $D_1$ , in order to limit the negative voltage at the noninverting input. A zener diode with a voltage rating of 0.3V can be used.
5. Calculate the AC mains leakage current to check if it meets the leakage current design goal of less than  $500\mu A$ .

$$I_{ac} = \frac{V_p}{R_1} = 340\mu A$$

## Design Simulations

### Transient Simulation Results



## Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit spice simulation file, [SBOMAP5](#).

For more information on many comparator topics including hysteresis, propagation delay and input common mode range please see, [TI Precision Labs](#).

## Design Featured Comparator

TLV7011	
$V_{ss}$	1.6 to 5.5V
$V_{inCM}$	Rail-to-rail
$t_{pd}$	260ns
$V_{os}$	0.5mV
$V_{HYS}$	4mV
$I_q$	5 $\mu$ A
<b>Output Type</b>	Push-Pull
<b>#Channels</b>	1
<a href="http://www.ti.com/product/tlv7011">www.ti.com/product/tlv7011</a>	

## Design Alternate Comparator

TLV3201	
$V_{ss}$	2.7 to 5.5V
$V_{inCM}$	Rail-to-rail
$t_{pd}$	40ns
$V_{os}$	1V
$V_{HYS}$	1.2mV
$I_q$	40 $\mu$ A
<b>Output Type</b>	Push-Pull
<b>#Channels</b>	1
<a href="http://www.ti.com/product/tlv3201">www.ti.com/product/tlv3201</a>	

## Single-supply strain gauge bridge amplifier circuit

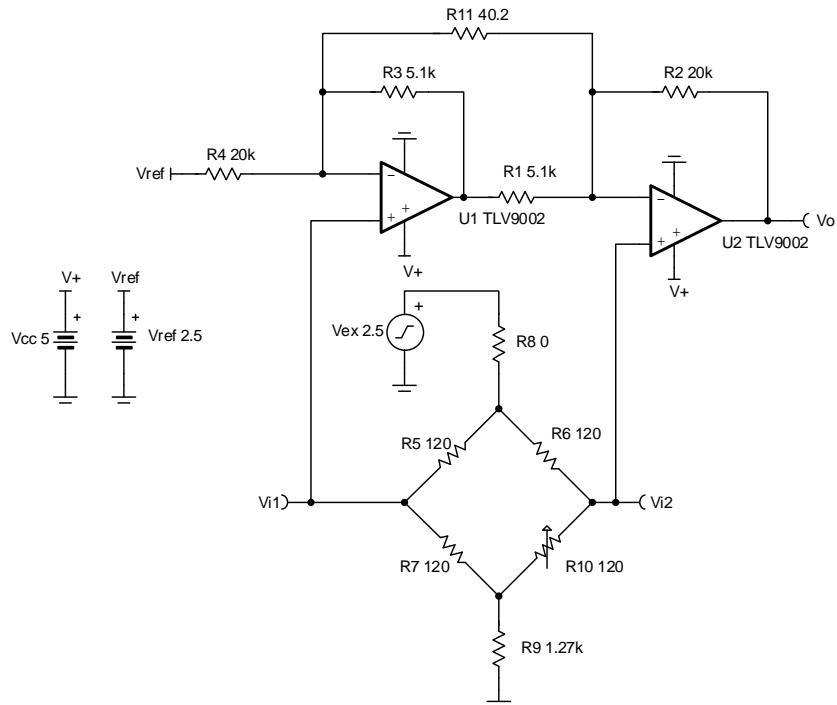
### Design Goals

Input $V_{iDiff}(V_{i2} - V_{i1})$		Output		Supply		
$V_{iDiff\_Min}$	$V_{iDiff\_Max}$	$V_{oMin}$	$V_{oMax}$	$V_{cc}$	$V_{ee}$	$V_{ref}$
-2.22mV	2.27mV	225mV	4.72V	5V	0V	2.5V

Strain Gauge Resistance Variation ( $R_{10}$ )	$V_{cm}$	Gain
115Ω – 125Ω	2.15V	1001V/V

### Design Description

A strain gauge is a sensor whose resistance varies with applied force. The change in resistance is directly proportional to how much strain the sensor is experiencing due to the force applied. To measure the variation in resistance, the strain gauge is placed in a bridge configuration. This design uses a 2 op amp instrumentation circuit to amplify a differential signal created by the change in resistance of a strain gauge. By varying  $R_{10}$ , a small differential voltage is created at the output of the Wheatstone bridge which is fed to the 2 op amp instrumentation amplifier input. Linear operation of an instrumentation amplifier depends upon the linear operation of its primary building block: op amps. An op amp operates linearly when the input and output signals are within the device's input common-mode and output-swing ranges, respectively. The supply voltages used to power the op amps define these ranges.



**Design Notes:**

1. Resistors  $R_5$ ,  $R_6$  and  $R_7$  of the Wheatstone bridge must match the strain gauge nominal resistance and must be equal to avoid creating a bridge offset voltage.
2. Low tolerance resistors must be used to minimize the offset and gain errors due to the bridge resistors.
3.  $V_{ex}$  sets the excitation voltage of the bridge and the common-mode voltage  $V_{cm}$ .
4.  $V_{ref}$  biases the output voltage of the instrumentation amplifier to mid-supply to allow differential measurements in the positive and negative directions.
5.  $R_{11}$  sets the gain of the instrumentation amplifier circuit.
6.  $R_8$  and  $R_9$  set the common-mode voltage of the instrumentation amplifier and limits the current through the bridge. This current determines the differential signal produced by the bridge. However, there are limitations on the current through the bridge due to self-heating effects of the bridge resistors and strain gauge.
7. Ensure that  $R_1 = R_3$  and  $R_2 = R_4$  and that ratios of  $R_2/R_1$  and  $R_4/R_3$  are matched to set the  $V_{ref}$  gain to 1V/V and maintain high DC CMRR of the instrumentation amplifier.
8. Linear operation is contingent upon the input common-mode and the output swing ranges of the op amps used. The linear output swing ranges are specified under the  $A_{ol}$  test conditions in the op amps datasheets.
9. Using high-value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.

**Design Steps:**

1. Select  $R_5$ ,  $R_6$  and  $R_7$  to match the strain gauge nominal resistance

$$R_{gauge} = R_5 = R_6 = R_7 = 120\Omega$$

2. Choose  $R_9$  to set the common mode voltage of the instrumentation amplifier at 2.15V

$$V_{cm} = \frac{\frac{R_{bridge}}{2} + R_5}{R_{bridge} + R_8 + R_9} \times V_{ex}$$

Where  $R_{bridge}$  = total resistance of the bridge

Choose  $R_8 = 0\Omega$  to allow maximum current through the bridge

$$V_{cm} = \frac{\frac{120\Omega \times 4}{2} + R_9}{120\Omega \times 4 + 0\Omega + R_9} \times 2.5V = 2.15V$$

$$\frac{240 + R_9}{480 + 0\Omega + R_9} = \frac{2.15V}{2.5V} = 0.86$$

$$0.14 R_9 = 172.8 \rightarrow R_9 = \frac{172.8}{0.14} = 1.23 k\Omega \rightarrow R_9 = 1.27 k\Omega \text{ (Standard value)}$$

3. Calculate the gain required to produce the desired output voltage swing

$$G = \frac{V_{oMax} - V_{oMin}}{V_{iDiff\_Min} - V_{iDiff\_Max}} = \frac{4.72V - 0.225V}{0.00222V - (-0.00227V)} = 1001\frac{V}{V}$$

4. Select  $R_1$ ,  $R_2$ ,  $R_3$  and  $R_4$ . To set the  $V_{ref}$  gain at 1V/V and avoid degrading the instrumentation amplifier's CMRR,  $R_1$  must equal  $R_3$  and  $R_2$  equal  $R_4$ .

Choose  $R_1 = R_3 = 5.1k\Omega$  and  $R_2 = R_4 = 20 k\Omega$  (Standard value)

5. Calculate  $R_{11}$  to meet the required gain

$$G = 1 + \frac{R_4}{R_3} + \frac{2 \times R_2}{R_{11}} = 1001\frac{V}{V}$$

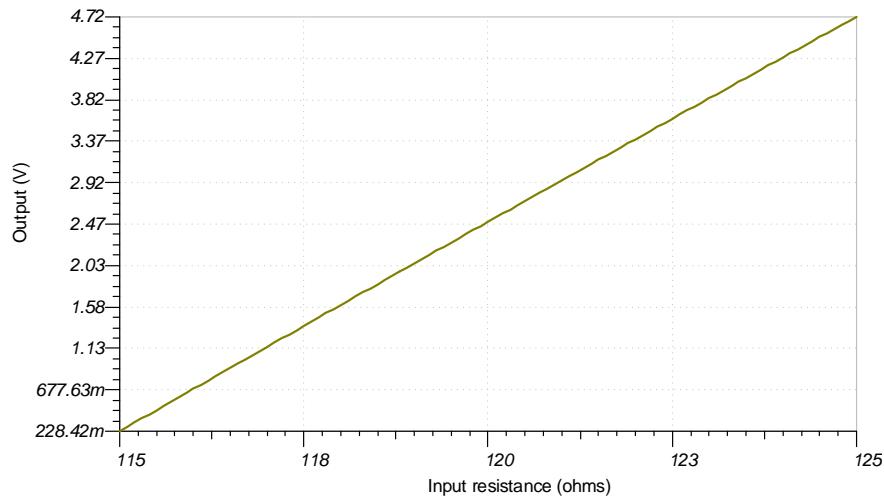
$$G = 1 + \frac{20k\Omega}{5.1k\Omega} + \frac{2 \times R_2}{R_{11}} = 1001\frac{V}{V} \rightarrow 4.92 + \frac{40k\Omega}{R_{11}} = 1001\frac{V}{V} \rightarrow \frac{40k\Omega}{R_{11}} = 996.1 \rightarrow R_{11} = \frac{40k\Omega}{996.1} = 40.15\Omega \rightarrow R_{11} = 40.2\Omega \text{ (Standard Value)}$$

6. Calculate the current through the bridge

$$I_{bridge} = \frac{V_{ex}}{R_8 + R_9 + R_{bridge}} = \frac{2.5V}{0\Omega + 1.27k\Omega + 120\Omega \times 4}$$

$$I_{bridge} = \frac{2.5V}{1.27k\Omega + 480\Omega} \rightarrow I_{bridge} = 1.42mA$$

**Design Simulations:**  
**DC Simulation Results**



**References:**

1. [Analog Engineer's Circuit Cookbooks](#)
2. [SPICE Simulation File SBOMAU4](#)
3. [TI Precision Designs TIPD170](#)
4. [TI Precision Labs](#)
5. [V<sub>CM</sub> vs. V<sub>OUT</sub> plots for instrumentation amplifiers with two op amps](#)

**Design Featured Op Amp:**

TLV9002	
V <sub>ss</sub>	1.8V to 5.5V
V <sub>inCM</sub>	Rail-to-rail
V <sub>out</sub>	Rail-to-Rail
V <sub>os</sub>	0.4mV
I <sub>q</sub>	0.06mA
I <sub>b</sub>	5pA
UGBW	1MHz
SR	2V/μs
#Channels	1,2,4
<a href="http://www.ti.com/product/tlv9002">www.ti.com/product/tlv9002</a>	

**Design Alternate Op Amp:**

OPA376	
V <sub>ss</sub>	2.2V to 5.5V
V <sub>inCM</sub>	(V <sub>ee</sub> –0.1V) to (V <sub>cc</sub> –1.3V)
V <sub>out</sub>	Rail-to-Rail
V <sub>os</sub>	0.005mV
I <sub>q</sub>	0.76mA
I <sub>b</sub>	0.2pA
UGBW	5.5MHz
SR	2V/μs
#Channels	1,2,4
<a href="http://www.ti.com/product/opa376">www.ti.com/product/opa376</a>	

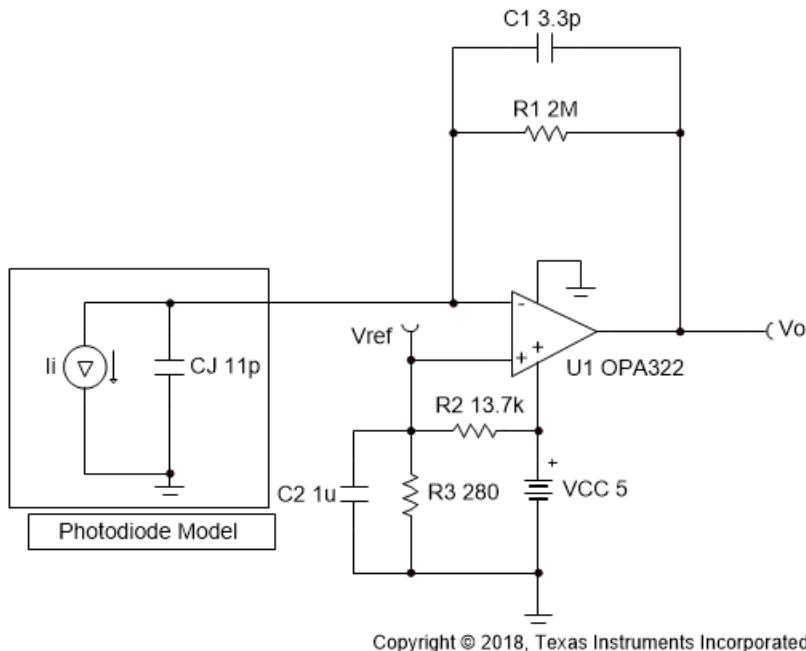
## Photodiode amplifier circuit

### Design Goals

Input		Output		BW	Supply		
$I_{iMin}$	$I_{iMax}$	$V_{oMin}$	$V_{oMax}$	$f_p$	$V_{cc}$	$V_{ee}$	$V_{ref}$
0A	2.4 $\mu$ A	100mV	4.9V	20kHz	5V	0V	0.1V

### Design Description

This circuit consists of an op amp configured as a transimpedance amplifier for amplifying the light-dependent current of a photodiode.



### Design Notes

1. A bias voltage ( $V_{ref}$ ) prevents the output from saturating at the negative power supply rail when the input current is 0A.
2. Use a JFET or CMOS input op amp with low bias current to reduce DC errors.
3. Set output range based on linear output swing (see  $A_{ol}$  specification).

## Design Steps

1. Select the gain resistor.

$$R_1 = \frac{V_{oMax} - V_{oMin}}{I_{IMax}} = \frac{4.9V - 0.1V}{2.4\mu A} = 2M\Omega$$

2. Select the feedback capacitor to meet the circuit bandwidth.

$$C_1 \leq \frac{1}{2\pi R_1 f_p}$$

$$C_1 \leq \frac{1}{2\pi \times 2M\Omega \times 20\text{kHz}} \leq 3.97\text{pF} \approx 3.3\text{pF} \text{ (Standard Value)}$$

3. Calculate the necessary op amp gain bandwidth (GBW) for the circuit to be stable.

$$GBW > \frac{C_i + C_1}{2\pi R_1 C_1^2} > \frac{20\text{pF} + 3.3\text{pF}}{2\pi \times 2M\Omega \times (3.3\text{pF})^2} > 170\text{kHz}$$

where  $C_i = C_j + C_d + C_{cm} = 11\text{pF} + 5\text{pF} + 4\text{pF} = 20\text{pF}$  given

- $C_j$ : Junction capacitance of photodiode
- $C_d$ : Differential input capacitance of the amplifier
- $C_{cm}$ : Common-mode input capacitance of the inverting input

4. Calculate the bias network for a 0.1-V bias voltage.

$$R_2 = \frac{V_{cc} - V_{ref}}{V_{ref}} \times R_3$$

$$R_2 = \frac{5V - 0.1V}{0.1V} \times R_3$$

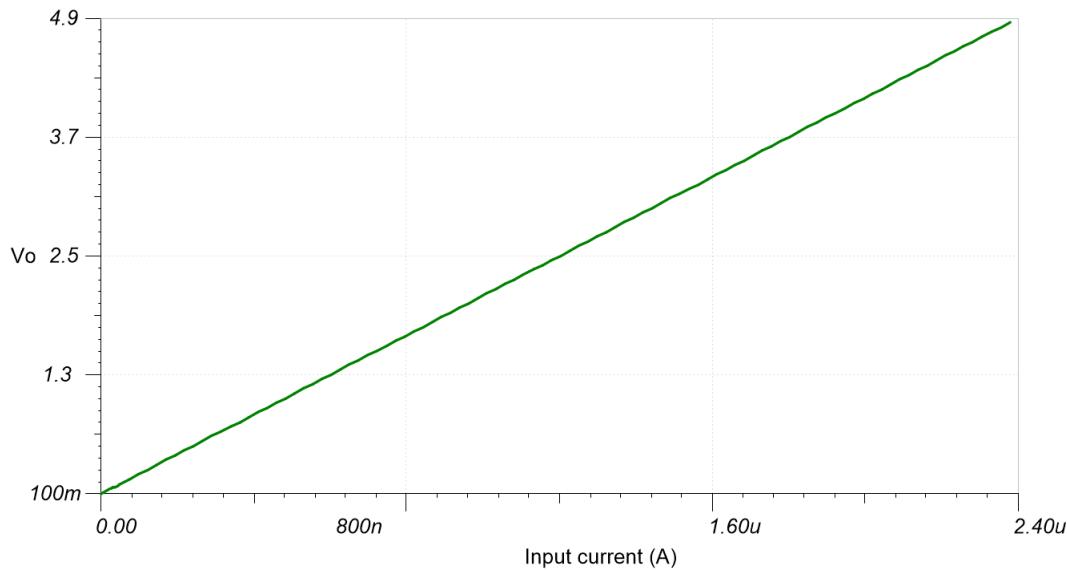
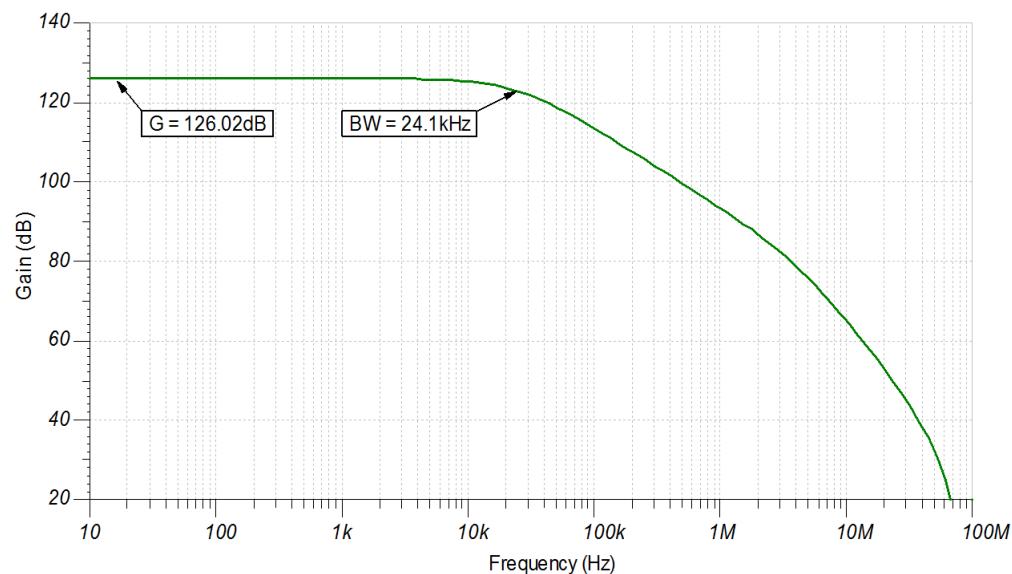
$$R_2 = 49 \times R_3$$

Closest 1% resistor values that yield this relationship are

$$R_2 = 13.7\text{k}\Omega \text{ and } R_3 = 280\Omega$$

5. Select  $C_2$  to be 1 $\mu\text{F}$  to filter the  $V_{ref}$  voltage. The resulting cutoff frequency is:

$$f_p = \frac{1}{2\pi C_2 (R_2 \parallel R_3)} = \frac{1}{2\pi \times 1\ \mu\text{F} \times (13.7\text{k} \parallel 280)} = 580\text{Hz}$$

**Design Simulations****DC Simulation Results****AC Simulation Results**

## Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See the circuit SPICE simulation file [SBOC517](#).

See TIPD176, [www.ti.com/tool/tipd176](http://www.ti.com/tool/tipd176).

## Design Featured Op Amp

OPA322	
$V_{cc}$	1.8V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	0.5mV
$I_q$	1.6mA/Ch
$I_b$	0.2pA
<b>UGBW</b>	20MHz
<b>SR</b>	10V/ $\mu$ s
<b>#Channels</b>	1, 2, 4
<a href="http://www.ti.com/product/opa322">www.ti.com/product/opa322</a>	

## Design Alternate Op Amp

LMP7721	
$V_{cc}$	1.8V to 5.5V
$V_{inCM}$	$V_{ee}$ to ( $V_{cc} - 1V$ )
$V_{out}$	Rail-to-rail
$V_{os}$	26 $\mu$ V
$I_q$	1.3mA/Ch
$I_b$	3fA
<b>UGBW</b>	17MHz
<b>SR</b>	10.43V/ $\mu$ s
<b>#Channels</b>	1
<a href="http://www.ti.com/product/lmp7721">www.ti.com/product/lmp7721</a>	

## Revision History

Revision	Date	Change
A	February 2019	Downscale the title and changed title role to 'Amplifiers'. Added links to circuit cookbook landing page and SPICE simulation file.

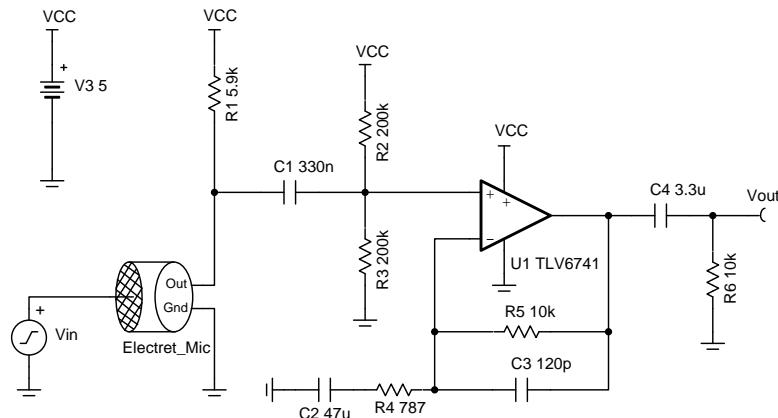
## Non-inverting microphone pre-amplifier circuit

### Design Goals

Input Pressure (Max)	Output Voltage (Max)	Supply		Frequency Response Deviation	
100dB SPL (2 Pa)	1.228V <sub>rms</sub>	V <sub>cc</sub>	V <sub>ee</sub>	@20Hz	@20kHz
		5V	0V	-0.5dB	-0.1dB

### Design Description

This circuit uses a non-inverting amplifier circuit configuration to amplify the microphone output signal. This circuit has very good magnitude flatness and exhibits minor frequency response deviations over the audio frequency range. The circuit is designed to be operated from a single 5V supply.



### Design Notes

1. Operate within the op amp linear output operating range, which is usually specified under the  $A_{OL}$  test conditions.
2. Use low-K capacitors (tantalum, C0G, and so forth) and thin film resistors help to decrease distortion.
3. Use a battery to power this circuit to eliminate distortion caused by switching power supplies.
4. Use low value resistors and low noise op amps for low noise designs.
5. The common mode voltage is equal to the DC bias voltage set using the resistor divider plus any variation caused by the microphone output voltage. For op amps with a complementary pair input stage it is recommended to keep the common mode voltage away from the cross over region to eliminate the possibility of cross over distortion.
6. Resistor  $R_1$  is used to bias the microphone internal JFET transistor to achieve the bias current specified by the microphone.
7. The equivalent input resistance is determined by  $R_1$ ,  $R_2$ ,  $R_3$ . Use large value resistors for  $R_2$  and  $R_3$  to increase the input resistance.
8. The voltage connected to  $R_1$  to bias the microphone does not have to be the same as the op amp supply voltage. Using a higher voltage supply for the microphone bias allows for a lower bias resistor value.

## Design Steps

This design procedure uses the microphone specifications provided in the following table.

Microphone Parameter	Value
Sensitivity @ 94dB SPL (1 Pa)	$-35 \pm 4$ dBV
Current Consumption (Max)	0.5mA
Impedance	2.2kΩ
Standard Operating Voltage	2Vdc

1. Convert the sensitivity to volts per Pascal.

$$10^{\frac{-35\text{dB}}{20}} = 17.78 \frac{\text{mV}}{\text{Pa}}$$

2. Convert volts per Pascal to current per Pascal.

$$\frac{17.78 \frac{\text{mV}}{\text{Pa}}}{2.2\text{k}\Omega} = 8.083 \frac{\mu\text{A}}{\text{Pa}}$$

3. Max output current occurs at max pressure 2Pa.

$$I_{\text{Max}} = 2\text{Pa} \times 8.083 \frac{\mu\text{A}}{\text{Pa}} = 16.166 \mu\text{A}$$

4. Calculate bias resistor. In the following equation,  $V_{\text{mic}}$  is microphone standard operating voltage.

$$R_1 = \frac{V_{\text{cc}} - V_{\text{mic}}}{I_s} = \frac{5\text{V} - 2\text{V}}{0.5\text{mA}} = 6\text{k}\Omega \approx 5.9\text{k}\Omega \text{ (Standard Value)}$$

5. Set the amplifier input common mode voltage to mid-supply voltage. The equivalent resistance of  $R_2$  in parallel with  $R_3$  should be 10 times larger than  $R_1$  so that a majority of the microphone current flows through  $R_1$ .

$$R_{\text{eq}} = R_2 \parallel R_3 > 10 \times R_1 = 100\text{k}\Omega$$

Choose  $R_2 = R_3 = 200\text{k}\Omega$

6. Calculate the maximum input voltage.

$$R_{\text{in}} = R_1 \parallel R_{\text{eq}} = 5.9\text{k}\Omega \parallel 100\text{k}\Omega = 5.571\text{k}\Omega$$

$$V_{\text{in}} = I_{\text{max}} \times R_{\text{in}} = 16.166\mu\text{A} \times 5.571\text{k}\Omega = 90.067\text{mV}$$

7. Calculate gain required to produce the largest output voltage swing.

$$\text{Gain} = \frac{V_{\text{outmax}}}{V_{\text{in}}} = \frac{1.228\text{V}}{90.067\text{mV}} = 13.634 \frac{\text{V}}{\text{V}}$$

8. Calculate  $R_4$  to set the gain calculated in step 7. Select feedback resistor  $R_5$  as 10kΩ.

$$R_4 = \frac{R_5}{\text{Gain}-1} = \frac{10\text{k}\Omega}{13.634-1} = 791\Omega \approx 787\Omega \text{ (Standard Values)}$$

The final gain of this circuit is:

$$\text{Gain} = 20\log \frac{V_{\text{out}}}{V_{\text{in}}} = 20\log \frac{16.166\mu\text{A} \times 5.571\text{k}\Omega \times (1 + \frac{10\text{k}\Omega}{787\Omega})}{2\text{V}} = -4.191\text{dB}$$

9. Calculate the corner frequency at low frequency according to the allowed deviation at 20 Hz. In the following equation,  $G_{\text{pole1}}$  is the gain contributed by each pole at frequency "f". Note that you divide by three because there are three poles.

$$f_c = f \sqrt{(\frac{1}{G_{\text{pole1}}})^2 - 1} = 20\text{Hz} \sqrt{(\frac{1}{\frac{0.5/3}{20}})^2 - 1} = 3.956\text{Hz}$$

10. Calculate  $C_1$  based on the cut off frequency calculated in step 9.

$$C_1 = \frac{1}{2\pi \times R_{\text{eq}} \times f_c} = \frac{1}{2\pi \times 100\text{k}\Omega \times 3.956\text{Hz}} = 0.402\mu\text{F} \approx 0.33\mu\text{F} \text{ (Standard Value)}$$

11. Calculate  $C_2$  based on the cut off frequency calculated in step 9.

$$C_2 = \frac{1}{2\pi \times R_4 \times f_c} = \frac{1}{2\pi \times 787\Omega \times 3.956\text{Hz}} = 51.121\mu\text{F} \approx 47\mu\text{F} \text{ (Standard Value)}$$

12. Calculate the high frequency pole according to the allowed deviation at 20 kHz. In the following equation,  $G_{\text{pole2}}$  is the gain contributed by each pole at frequency "f".

$$f_p = \frac{f}{\sqrt{(\frac{1}{G_{\text{pole2}}})^2 - 1}} = \frac{20\text{kHz}}{\sqrt{(\frac{1}{\frac{0.1}{20}})^2 - 1}} = 131.044\text{kHz}$$

13. Calculate C<sub>3</sub> to set the cut off frequency calculated in step 12.

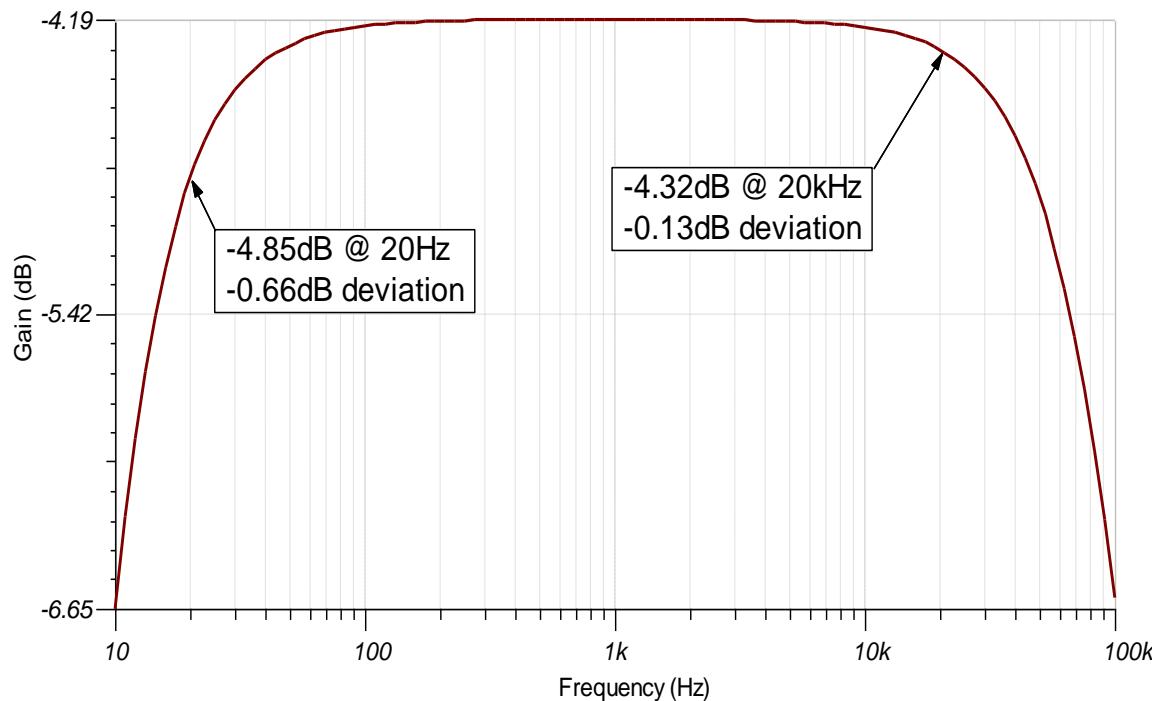
$$C_3 = \frac{1}{2\pi \times R_6 \times f_p} = \frac{1}{2\pi \times 10k\Omega \times 131.044\text{kHz}} = 121.451\text{pF} \approx 120\text{pF} \text{ (Standard Value)}$$

14. Calculate the output capacitor, C<sub>4</sub>, based on the cut off frequency calculated in step 9. Assume the output load R<sub>6</sub> is 10kΩ.

$$C_4 = \frac{1}{2\pi \times R_6 \times f_c} = \frac{1}{2\pi \times 10k\Omega \times 3.956\text{Hz}} = 4.023\mu\text{F} \approx 3.3\mu\text{F} \text{ (Standard Value)}$$

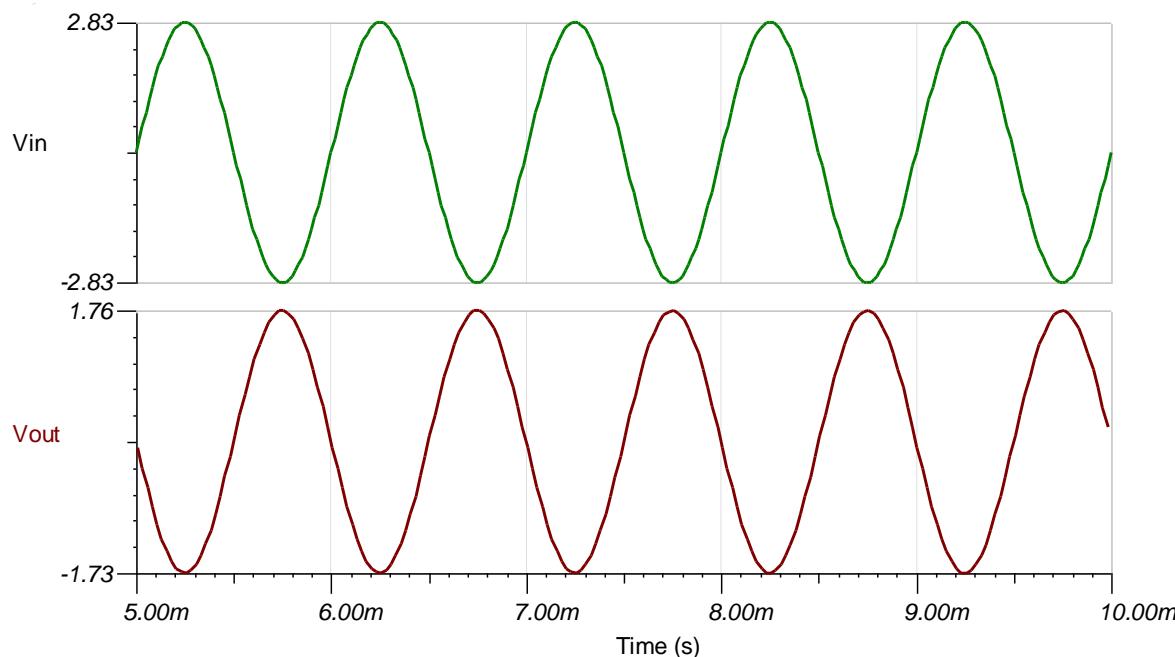
### Design Simulations

#### AC Simulation Results



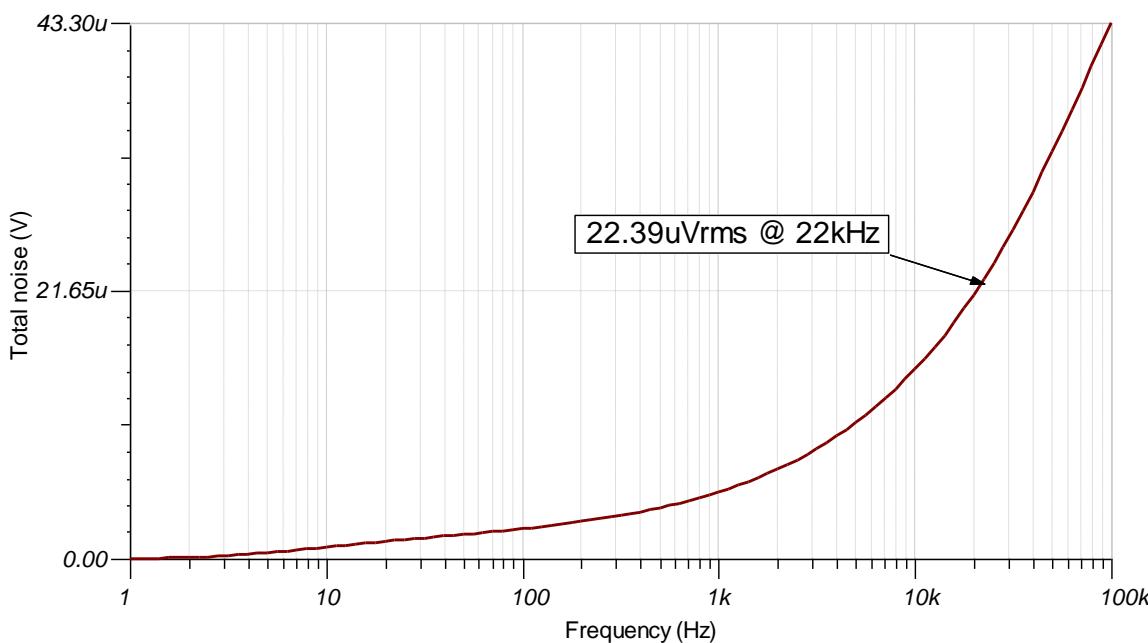
### Transient Simulation Results

The input voltage represents the SPL of an input signal to the microphone. A 1 V<sub>rms</sub> input signal represents 1 Pascal.



### Noise Simulation Results

The following simulation results show 22.39uVrms of noise at 22kHz. The noise is measured at a bandwidth of 22kHz to represent the measured noise using an audio analyzer with the bandwidth set to 22kHz.



**References:**

1. [Analog Engineer's Circuit Cookbooks](#)
2. [SPICE Simulation File SBOC525](#)
3. [TI Precision Designs TIPD181](#)
4. [TI Precision Labs](#)

**Design Featured Op Amp**

TLV6741	
$V_{ss}$	1.8V to 5.5V
$V_{inCM}$	( $V_{ee}$ ) to ( $V_{cc} - 1.2V$ )
$V_{out}$	Rail-to-rail
$V_{os}$	150 $\mu$ V
$I_q$	890 $\mu$ A/Ch
$I_b$	10pA
<b>UGBW</b>	10MHz
<b>SR</b>	4.75V/ $\mu$ s
<b>#Channels</b>	1
<a href="http://www.ti.com/product/tlv6741">www.ti.com/product/tlv6741</a>	

**Design Alternate Op Amp**

OPA320	
$V_{ss}$	1.8V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	40 $\mu$ V
$I_q$	1.5mA/Ch
$I_b$	0.2pA
<b>UGBW</b>	20MHz
<b>SR</b>	10V/ $\mu$ s
<b>#Channels</b>	1, 2
<a href="http://www.ti.com/product/opa320">www.ti.com/product/opa320</a>	

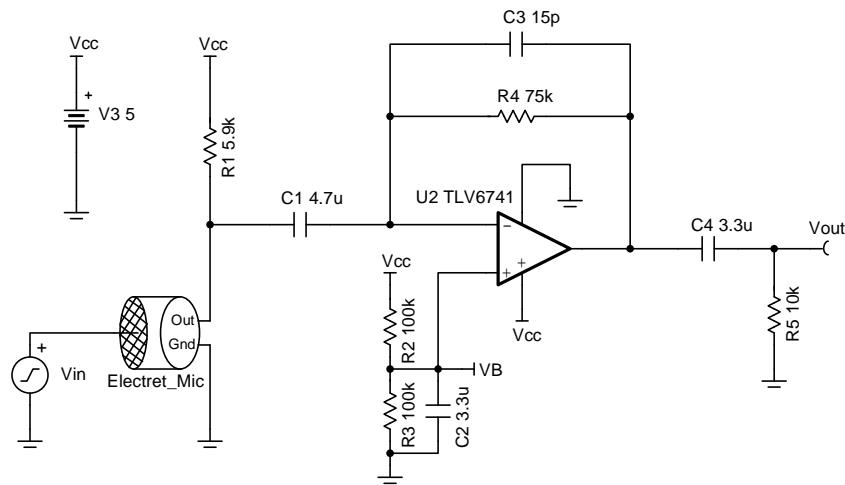
## TIA microphone amplifier circuit

### Design Goals

Input pressure (Max)	Output Voltage (Max)	Supply		Frequency Response Deviation	
100dB SPL(2Pa)	1.228V <sub>rms</sub>	V <sub>cc</sub>	V <sub>ee</sub>	@ 20Hz	@20kHz
		5V	0V	-0.5dB	-0.1dB

### Design Description

This circuit uses an op amp in a transimpedance amplifier configuration to convert the output current from an electret capsule microphone into an output voltage. The common mode voltage of this circuit is constant and set to mid-supply eliminating any input-stage cross over distortion.



### Design Notes

1. Use the op amp in the linear output operating range, which is usually specified under the  $A_{OL}$  test conditions.
2. Use low-K capacitors (tantalum, COG, etc.) and thin film resistors help to decrease distortion.
3. Use a battery to power this circuit to eliminate distortion caused by switching power supplies.
4. Use low value resistors and low noise op amp to achieve high performance low noise designs.
5. The voltage connected to  $R_1$  to bias the microphone does not have to match the supply voltage of the op amp. Using a larger microphone bias voltage allows for a larger value of  $R_1$ , which decreases the noise gain of the op amp circuit while still maintaining normal operation of the microphone.
6. Capacitor  $C_1$  should be large enough that its impedance is much less than resistor  $R_1$  at audio frequency. Pay attention to the signal polarity when using tantalum capacitors.

## Design Steps

The following microphone is chosen as an example to design this circuit.

Microphone parameter	Value
Sensitivity @ 94dB SPL (1 Pa)	$-35 \pm 4$ dBV
Current Consumption (Max)	0.5mA
Impedance	2.2kΩ
Standard Operating Voltage	2V <sub>dc</sub>

1. Convert the sensitivity to volts per Pascal.

$$10^{\frac{-35\text{dB}}{20}} = 17.78 \text{ mV / Pa}$$

2. Convert volts per Pascal to current per Pascal.

$$\frac{17.78\text{mV / Pa}}{2.2\text{k}\Omega} = 8.083 \mu\text{A / Pa}$$

3. Max output current occurs at max sound pressure level of 2Pa.

$$I_{\text{Max}} = 2\text{Pa} \times 8.083 \mu\text{A / Pa} = 16.166 \mu\text{A}$$

4. Calculate the value of resistor R<sub>4</sub> to set the gain

$$R_4 = \frac{V_{\text{max}}}{I_{\text{max}}} = \frac{1.228\text{V}}{16.166\mu\text{A}} = 75.961 \text{k}\Omega \approx 75\text{k}\Omega \text{ (Standard value)}$$

The final signal gain is:

$$\text{Gain} = 20 \times \log \frac{V_{\text{out}}}{V_{\text{in}}} = 20 \times \log \frac{16.166\mu\text{A} \times 75\text{k}\Omega}{2\text{V}} = -4.347 \text{ dB}$$

5. Calculate the value for the bias resistor R<sub>1</sub>. In the following equation, V<sub>mic</sub> is the standard operating voltage of the microphone

$$R_1 = \frac{V_{\text{cc}} - V_{\text{mic}}}{I_s} = \frac{5\text{V} - 2\text{V}}{0.5\text{mA}} = 6\text{k}\Omega \approx 5.9 \text{k}\Omega \text{ (Standard value)}$$

6. Calculate the high frequency pole according to the allowed deviation at 20 kHz. In the following equation, G\_pole1 is the gain at frequency "f".

$$f_p = \frac{f}{\sqrt{(\frac{1}{G_{\text{pole1}}})^2 - 1}} = \frac{20\text{kHz}}{\sqrt{(\frac{1}{10^{20}})^2 - 1}} = 131.044 \text{ kHz}$$

7. Calculate C<sub>3</sub> based on the pole frequency calculated in step 6.

$$C_3 = \frac{1}{2\pi \times f_p \times R_4} = \frac{1}{2\pi \times 131.044\text{kHz} \times 75\text{k}\Omega} = 16.194 \text{ pF} \approx 15\text{pF} \text{ (Standard value)}$$

8. Calculate the corner frequency at low frequency according to the allowed deviation at 20 Hz. In the following equation, G\_pole2 is the gain contributed by each pole at frequency "f" respectively. There are two poles, so divided by two.

$$f_c = f \times \sqrt{(\frac{1}{G_{\text{pole2}}})^2 - 1} = 20\text{Hz} \times \sqrt{(\frac{1}{10^{20}})^2 - 1} = 4.868 \text{ Hz}$$

9. Calculate the input capacitor C<sub>1</sub> based on the cut off frequency calculated in step 8.

$$C_1 = \frac{1}{2\pi \times R_1 \times f_c} = \frac{1}{2\pi \times 5.9\text{k}\Omega \times 4.868\text{Hz}} = 5.541 \mu\text{F} \approx 4.7 \mu\text{F} \text{ (Standard value)}$$

10. Assuming the output load R<sub>5</sub> is 10kΩ, calculate the output capacitor C<sub>4</sub> based on the cut off frequency calculated in step 8.

$$C_4 = \frac{1}{2\pi \times R_5 \times f_c} = \frac{1}{2\pi \times 10\text{k}\Omega \times 4.868\text{Hz}} = 3.269 \mu\text{F} \approx 3.3 \mu\text{F} \text{ (Standard value)}$$

11. Set the amplifier input common mode voltage to mid-supply voltage. Select R<sub>2</sub> and R<sub>3</sub> as 100kΩ. The equivalent resistance equals to the parallel combination of the two resistors:

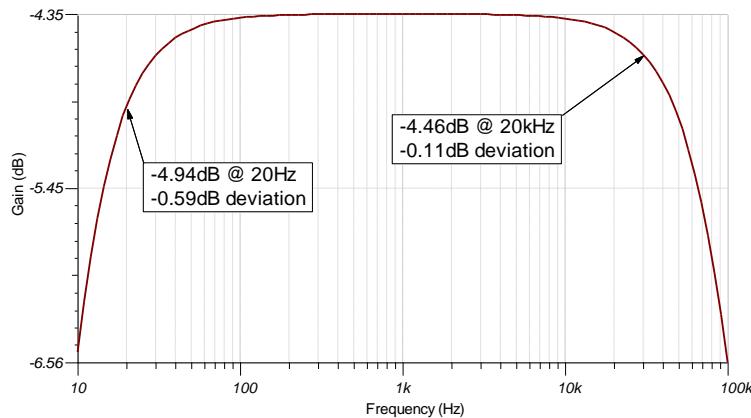
$$R_{\text{eq}} = R_2 \parallel R_3 = 100\text{k}\Omega \parallel 100\text{k}\Omega = 50\text{k}\Omega$$

12. Calculate the capacitor C<sub>2</sub> to filter the power supply and resistor noise. Set the cutoff frequency to 1Hz.

$$C_2 = \frac{1}{2\pi \times (R_2 \parallel R_3) \times 1\text{Hz}} = \frac{1}{2\pi \times (100\text{k}\Omega \parallel 100\text{k}\Omega) \times 1\text{Hz}} = 3.183 \mu\text{F} \approx 3.3 \mu\text{F} \text{ (Standard value)}$$

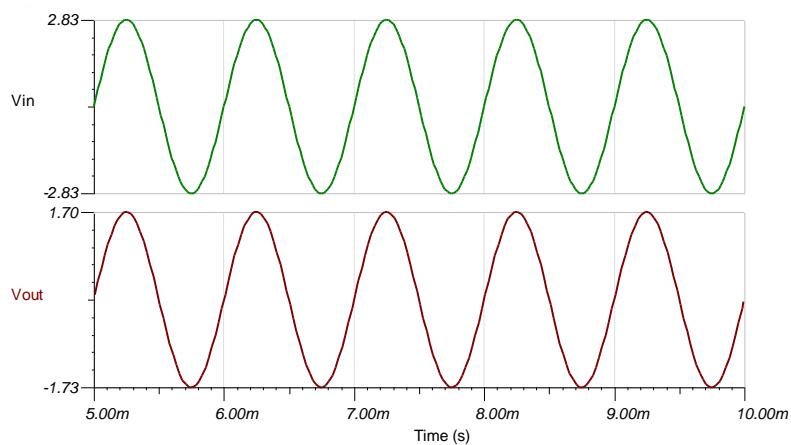
## Design Simulations

### AC Simulation Results



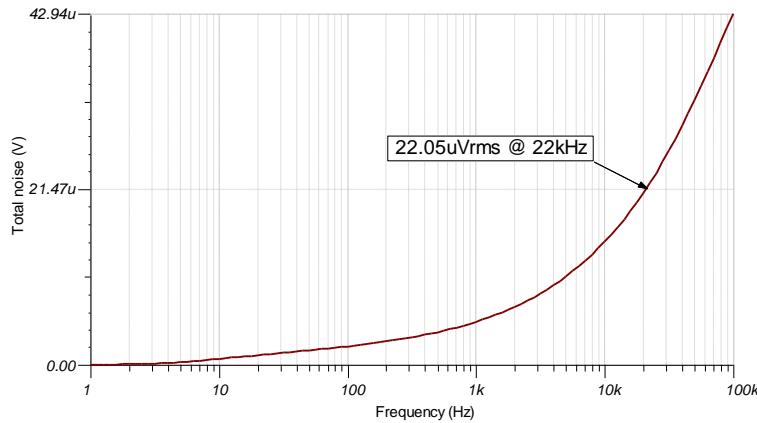
### Transient Simulation Results

The input voltage represents the SPL of an input signal to the microphone. A  $2 \text{ V}_{\text{rms}}$  input signal represents 2 Pascal.



### Noise Simulation Results

The following simulation results show  $22.39 \mu\text{V}_{\text{rms}}$  of noise at 22kHz. The noise is measured at a bandwidth of 22kHz to represent the measured noise using an audio analyzer with the bandwidth set to 22kHz.



**References:**

1. [Analog Engineer's Circuit Cookbooks](#)
2. [SPICE Simulation File SBOC526](#)
3. [TI Precision Designs TIPD181](#)
4. [TI Precision Labs](#)

**Design Featured Op Amp**

TLV6741	
$V_{ss}$	1.8V to 5.5V
$V_{inCM}$	$V_{ee}$ to $V_{cc}$ -1.2V
$V_{out}$	Rail-to-rail
$V_{os}$	150 $\mu$ V
$I_q$	890 $\mu$ A/Ch
$I_b$	10pA
<b>UGBW</b>	10MHz
<b>SR</b>	4.75V/ $\mu$ s
<b>#Channels</b>	1
<a href="http://www.ti.com/product/tlv6741">www.ti.com/product/tlv6741</a>	

**Design Alternate Op Amp**

	OPA172	OPA192
$V_{ss}$	4.5V to 36V	4.5V to 36V
$V_{inCM}$	$V_{ee}$ -0.1V to $V_{cc}$ -2V	$V_{ee}$ -0.1V to $V_{cc}$ +0.1V
$V_{out}$	Rail-to-rail	Rail-to-rail
$V_{os}$	$\pm$ 200 $\mu$ V	$\pm$ 5 $\mu$ V
$I_q$	1.6mA/Ch	1mA/Ch
$I_b$	8pA	5pA
<b>UGBW</b>	10MHz	10MHz
<b>SR</b>	10V/ $\mu$ s	20V/ $\mu$ s
<b>#Channels</b>	1, 2, 4	1, 2, 4
	<a href="http://www.ti.com/product/opa172">www.ti.com/product/opa172</a>	<a href="http://www.ti.com/product/opa192">www.ti.com/product/opa192</a>

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