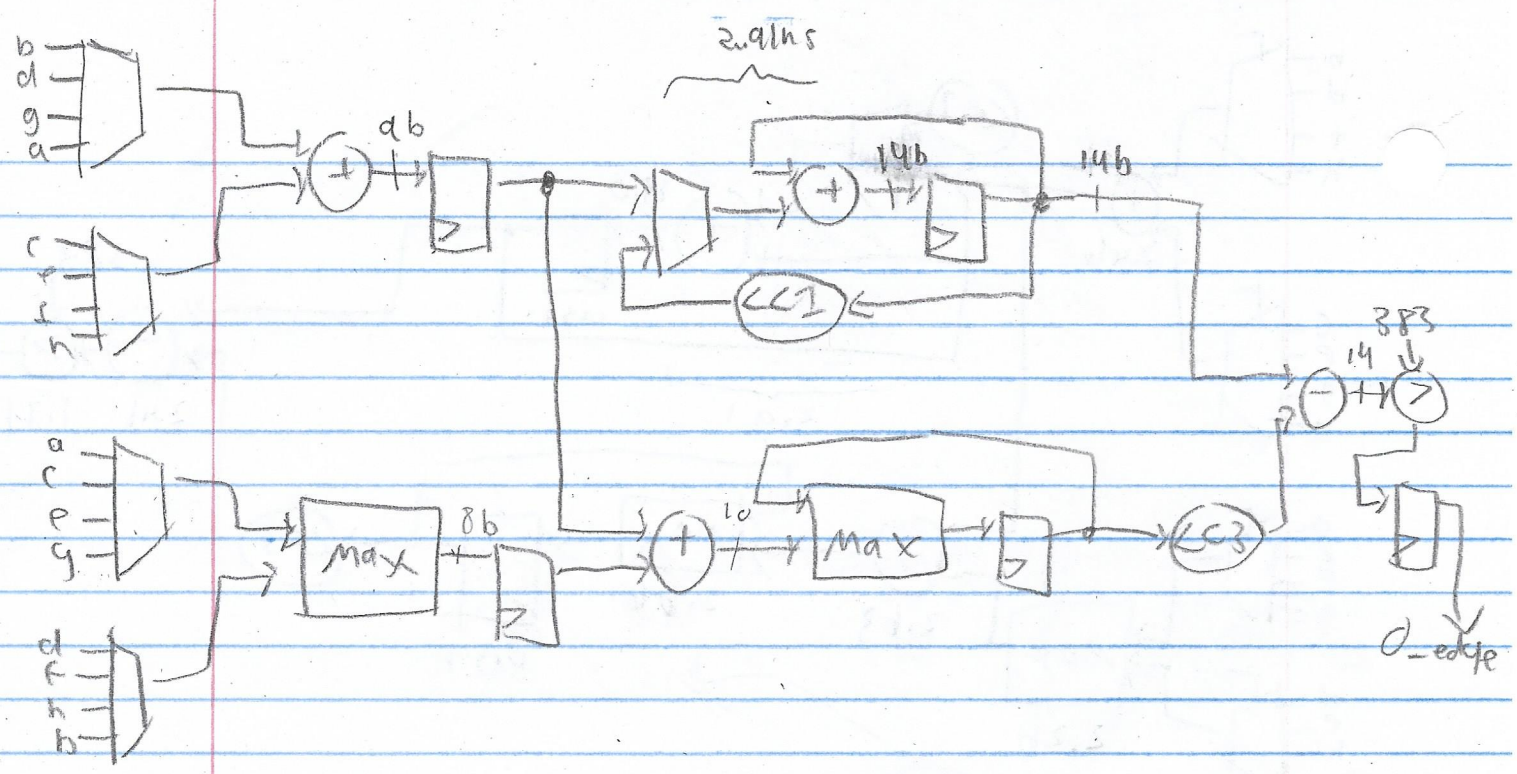

Slowest component: 13 bit adder with 1 mux input: 2.91 ns
upper frequency bound: $\frac{1}{2.91ns} \approx 343.6$ MHz
Through put: 1 input per 6 cycles
Latency: 6 cycles
Area estimate: 1 · 8-bit adder, 2 mux + 1 · 8-bit compare, 2 mux + 1 · 9-bit adder, no mux + 1 · 13 bit adder, 1 mux + 1 reg, no mux + 1-10 bit compare, no mux, + 1 register, 1 mux + 1 · 13 bit subtractor, no mux + 1 · 15 bit compare, no mux + 2 · register, no mux + 1 register, 1 mux = 16 + 18 + 9 + 13 + 1 + 7 + 1 + 14 + 9 + 2 · 0 + 1 = 89 LUTs

Optimality: freq $\propto \frac{1}{2.91 + 2.41 + 1.71 ns} \cong 142.24$ MHz

$$\frac{\text{freq}}{\text{Area}} = \frac{142.24 \text{ MHz}}{89} \cong 1.598 \times 10^6$$