# Design of Streaming Protocol for Real-Time Reliable RFSoC Streaming

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1. Documentation: Is the artifact/code sufficiently documented?

Rate from 0% to 100%, where 0% means "documentation is completely insufficient" and 100% means "documentation is absolutely sufficient". If you need to assess both a dataset and tools, please take the average and comment below. In assessing tools, please consider if they are easy or difficult to install/set up and get to run. In assessing datasets, please consider if the meta data is sufficient.

#### Choices are:

- 1.0%
- **2**. 20%
- **3.** 40%
- 4.60%
- **5.** 80%
- 6. 100%

**Documentation: Comment on/explain your choice above:** 

The documentation is complete and covers the experiment setup well. There is even documentation of the project's progress.

2. Completeness: Do the submitted artifacts/code include all of the key components described in the report?

Rate from 0% to 100%, where 0% means "does not include any key components" and 100% means "includes all key components".

#### Choices are:

- 1.0%
- **2**. 20%
- 3.40%
- 4.60%
- 5. 80%
- **6.** 100%

## Completeness: Comment on/explain your choice above

The code provided is mostly complete and covers both hardware design using Vitis HLS and Python scripts for data processing. The FPGA project is not provided so we cannot run the real experiment to verify the Ethernet transmission via SFP+.

3. Exercisability: Do the submitted artifacts/code include the scripts and data needed to run the experiments described in the paper, and can the software be successfully executed?

Rate from 0% to 100%, where 0% means "the scripts/software cannot be successfully executed and/or no data is included" and 100% means "the artifact includes all necessary scripts/software and data, and scripts/software (if present) can be successfully executed".

#### Choices are:

- 1.0%
- **2**. 20%
- **3**. 40%
- 4.60%
- **5.** 80%
- 6. 100%

Exercisability: Comment on/explain your choice above

Great! The benchmark is easy to run and the plot is also provided.

4. Results attainable: Does the artifact/code make it possible, with reasonable effort, to obtain the key results from the artifact/code?

Rate from 0% to 100%, where 0% means "no results can be obtained" and 100% means "all results can be obtained".

#### Choices are:

- 1.0%
- **2**. 20%
- **3.** 40%
- 4.60%
- **5.** 80%
- 6. 100%

Results attainable: Comment on/explain your choice above

Yes, the results can be obtained easily, with the help of full documentation.

# 5. Results completeness: How many key results of the paper/report is the provided code meant to support?

Rate from 0% to 100%, where 0% means "the artifact is meant to support no key results" and 100% means "the artifact is meant to support all key results".

Choices are:

- 1.0%
- **2**. 20%
- **3**. 40%
- 4.60%
- **5.** 80%
- 6. 100%

## Results completeness: Comment on/explain your choice above

The artifact is meant to support all key results. The FPGA Ethernet connection part is a verification of functions only, so it does not impact the results that is given in the report.

Reviewer Qinpei Luo, Signature

Reviewer Wuqiong Zhao, Signature

Qinpei Luo Wuqing Zhao