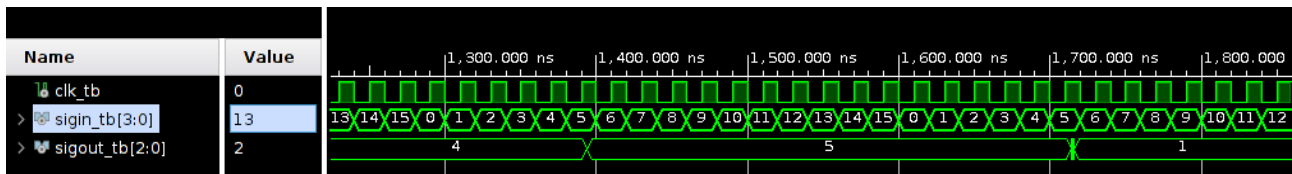
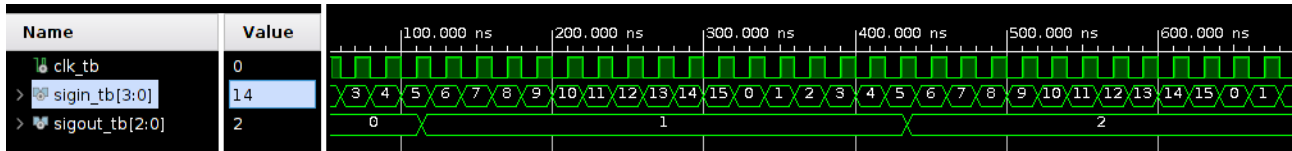


DSD – ΕΡΓΑΣΙΑ 2

ΖΟΥΡΝΑΤΖΗΣ ΔΗΜΗΤΡΙΟΣ

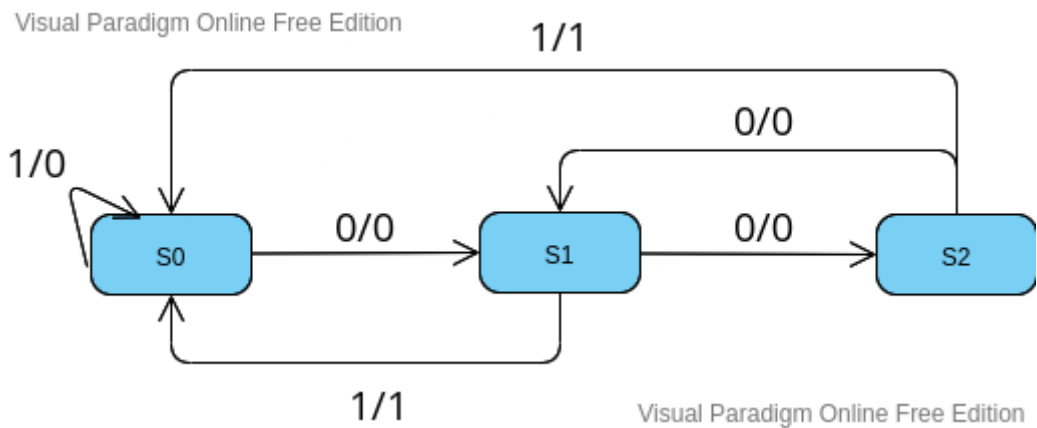
1115201600048

1.



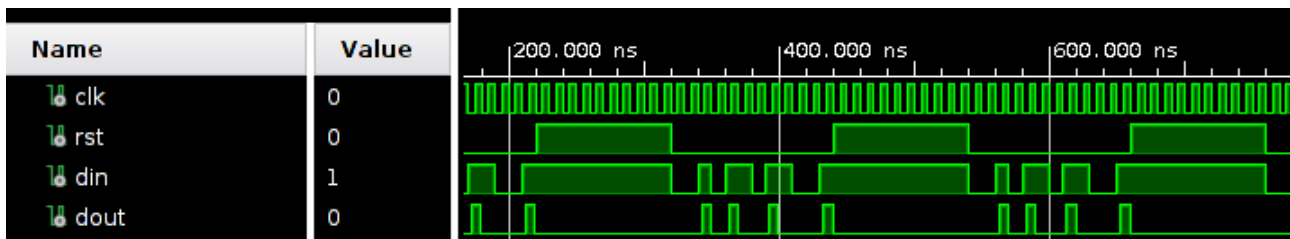
post synthesis timing simulation.

2.



Πίνακας καταστάσεων του FSM

| curr_state | Input | next_state | Output |
|------------|-------|------------|--------|
| S0 | 0 | S1 | 0 |
| S1 | 0 | S2 | 0 |
| S2 | 1 | S0 | 1 |
| S0 | 1 | S0 | 1 |
| S1 | 1 | S0 | 1 |
| S2 | 0 | S2 | 0 |

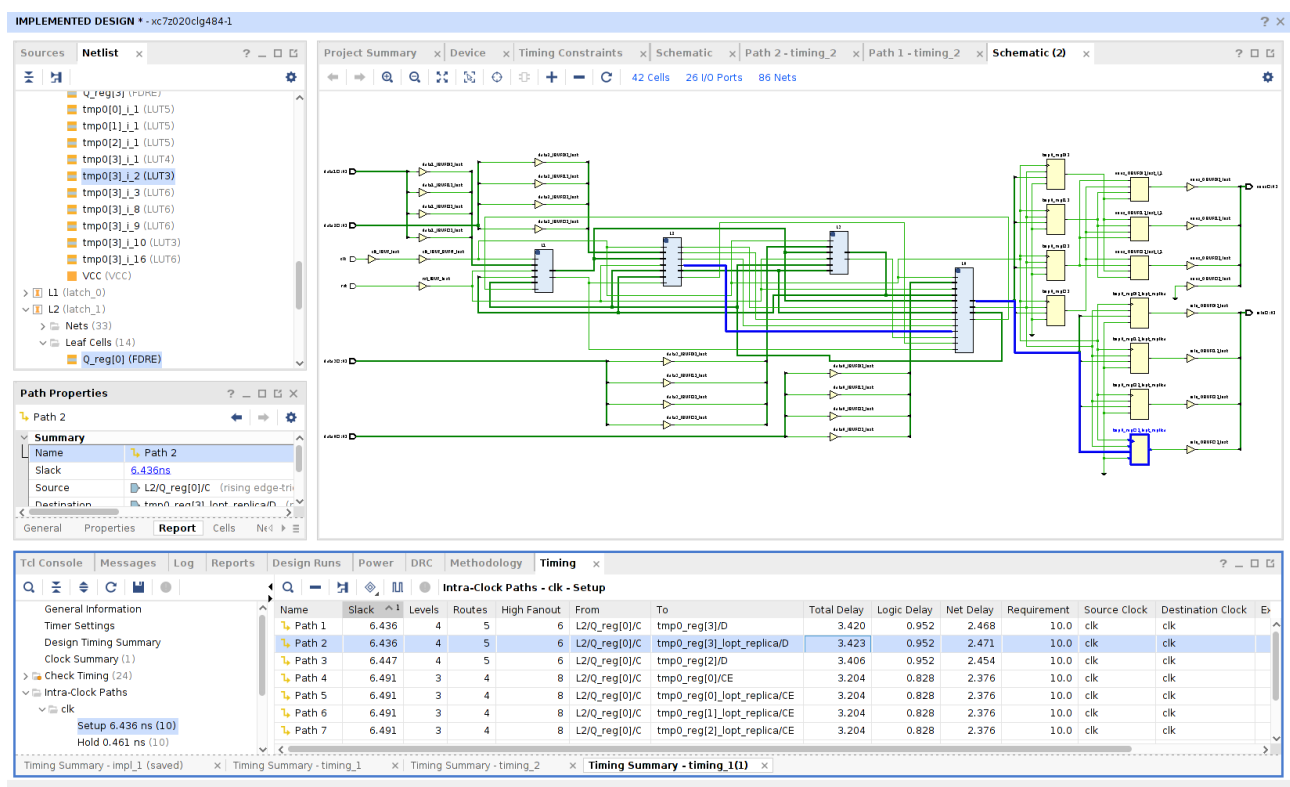


Ο παραπάνω πίνακας επιβεβαιώνεται και από την post-synthesis timing simulation του κυκλώματος.

3.

Οι παρακάτω μετρήσεις έγιναν στο στάδιο του implementation. Στον φάκελο png υπάρχουν και οι αντίστοιχες για το στάδιο του synthesis.

Αρχικά για το non-pipelined



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Sources Netlist x ? - □ □

Q_reg[3] (FDFE)
tmp0[0]_1_1 (LUT5)
tmp0[1]_1_1 (LUT5)
tmp0[2]_1_1 (LUT5)
L0tmp0[3]_1_1 (LUT3)
tmp0[3]_1_2 (LUT3)
tmp0[3]_1_3 (LUT6)
tmp0[3]_1_8 (LUT6)
tmp0[3]_1_9 (LUT6)
tmp0[3]_1_10 (LUT3)
tmp0[3]_1_16 (LUT6)
VCC (VCC)
L1 (latch_0)
L2 (latch_1)
Nets (33)
Leaf Cells (14)
Q_reg[0] (FDFE)

Path Properties ? - □ □ □

Path 2

Summary

Name Path 2
Slack 6.436ns
Source L2/Q_reg[0]/C (rising edge-tri
Destination tmp0_reg[3]_lopt_replica/D

General Properties Report Cells Net

Summary x Device x Timing Constraints x Schematic x Path 2 - timing_2 x Path 1 - timing_2 x Schematic (2) x Path 2 - timing_1(1) x ? □ □ □

IBUF (Prop_ibuf_1_0) (r) 1.490 1.490 Site: Y9 clk_IBUF_inst/I
net (fo=1, routed) 2.171 3.661 Site: Y9 clk_IBUF_inst/O
clk_IBUF
BUFG (Prop_bufg_1_0) (r) 0.101 3.762 Site: BUF...TRL_X0Y0 clk_IBUF_BUFG_inst/I
net (fo=24, routed) 1.874 5.636 Site: BUF...TRL_X0Y0 clk_IBUF_BUFG_inst/O
L2/CLK
FDFE Site: SLICE_X109Y12 L2/Q_reg[0]/C

Data Path

Delay Type Incr (ns) Path ... Location Netlist Resource(s)
FDFE (Prop_fdre_c_q) (f) 0.456 6.092 Site: SLICE_X109Y12 L2/Q_reg[0]/Q
net (fo=6, routed) 0.866 6.958 L2/Q_reg[3]_1_1[0]
L2tmp0[3]_1_17/I0
LUT6 (Prop_lut6_1_0_0) (r) 0.124 7.082 Site: SLICE_X107Y12 L2tmp0[3]_1_17/O
net (fo=1, routed) 0.411 7.494 L2tmp0[3]_1_17_n_0
LUT5 (Prop_lut5_1_1_0) (r) 0.124 7.618 Site: SLICE_X109Y13 L2tmp0[3]_1_12/I
net (fo=5, routed) 0.464 8.081 L2tmp0[3]_1_12_n_0
L2tmp0[3]_1_12_n_0
LUT6 (Prop_lut6_1_4_0) (r) 0.124 8.205 Site: SLICE_X111Y13 L2tmp0[3]_1_7/I
net (fo=1, routed) 0.395 8.601 L0tmp0_reg[3]
L0tmp0_reg[3]
LUT3 (Prop_lut3_1_2_0) (r) 0.124 8.725 Site: SLICE_X113Y13 L0tmp0[3]_1_2/I
net (fo=2, routed) 0.335 9.060 L0tmp0[3]_1_2/O
p_1_in[3]
FDFE Site: SLICE_X110Y13 tmp0_reg[3]_lopt_replica/D

Arrival Time

Destination Clock Path

Delay Type Incr (ns) Path ... Location Netlist Resource(s)

Td Console Messages Log Reports Design Runs Power DRC Methodology Timing x ? - □ □ □

Intra-Clock Paths - clk - Setup

General Information
Timer Settings
Design Timing Summary
Clock Summary (1)
Check Timing (24)
Intra-Clock Paths
clk
Setup 6.436 ns (10)
Hold 0.461 ns (10)

| Name | Slack | Levels | Routes | High Fanout | From | To | Total Delay | Logic Delay | Net Delay | Requirement | Source Clock | Destination Clock |
|--------|-------|--------|--------|-------------|---------------|-----------------------------|-------------|-------------|-----------|-------------|--------------|-------------------|
| Path 1 | 6.436 | 4 | 5 | 6 | L2/Q_reg[0]/C | tmp0_reg[3]/D | 3.420 | 0.952 | 2.468 | 10.0 | clk | clk |
| Path 2 | 6.436 | 4 | 5 | 6 | L2/Q_reg[0]/C | tmp0_reg[3]_lopt_replica/D | 3.423 | 0.952 | 2.471 | 10.0 | clk | clk |
| Path 3 | 6.447 | 4 | 5 | 6 | L2/Q_reg[0]/C | tmp0_reg[2]/D | 3.406 | 0.952 | 2.454 | 10.0 | clk | clk |
| Path 4 | 6.491 | 3 | 4 | 8 | L2/Q_reg[0]/C | tmp0_reg[0]/CE | 3.204 | 0.828 | 2.376 | 10.0 | clk | clk |
| Path 5 | 6.491 | 3 | 4 | 8 | L2/Q_reg[0]/C | tmp0_reg[0]_lopt_replica/CE | 3.204 | 0.828 | 2.376 | 10.0 | clk | clk |
| Path 6 | 6.491 | 3 | 4 | 8 | L2/Q_reg[0]/C | tmp0_reg[1]_lopt_replica/CE | 3.204 | 0.828 | 2.376 | 10.0 | clk | clk |
| Path 7 | 6.491 | 3 | 4 | 8 | L2/Q_reg[0]/C | tmp0_reg[2]_lopt_replica/CE | 3.204 | 0.828 | 2.376 | 10.0 | clk | clk |

Timing Summary - impl_1 (saved) x Timing Summary - timing_1 x Timing Summary - timing_2 x Timing Summary - timing_1(1) x

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Sources Netlist x ? - □ □ □

Q_reg[3] (FDFE)
tmp0[0]_1_1 (LUT5)
tmp0[1]_1_1 (LUT5)
tmp0[2]_1_1 (LUT5)
tmp0[3]_1_1 (LUT4)
tmp0[3]_1_2 (LUT3)
tmp0[3]_1_3 (LUT6)
tmp0[3]_1_8 (LUT6)
tmp0[3]_1_9 (LUT6)
tmp0[3]_1_10 (LUT3)
tmp0[3]_1_16 (LUT6)
VCC (VCC)
L1 (latch_0)
L2 (latch_1)
Nets (33)
Leaf Cells (14)
Q_reg[0] (FDFE)

Netlist Properties ? - □ □ □

top_module

Primitive Statistics

| Primitive type | Count |
|----------------|-------|
| FLOP_LATCH | 24 |
| LUT | 29 |

Statistics Properties I/O Nets

Summary x Device x Timing Constraints x Schematic x Path 2 - timing_2 x Path 1 - timing_2 x Schematic (2) x Path 2 - timing_1(1) x ? □ □ □

Create Clock

Clocks (1)
Create Clock (1)
Create Generated Clock (0)
Rename Auto-Derived Clock (0)
Set Clock Latency (0)
Set Clock Uncertainty (0)
Set Clock Groups (0)
Set Clock Sense (0)
Set Input Jitter (0)
Set System Jitter (0)
Set External Delay (0)
Inputs (0)
Set Input Delay (0)
Outputs (0)

All Constraints

| Position | Command | Scoped Cell |
|----------|--|-------------|
| 1 | create_clock -period 3.564 -name clk -waveform {0.000 1.782} [get_ports clk] | |

Apply Cancel

Td Console Messages Log Reports Design Runs Power DRC Methodology Timing x ? - □ □ □

Design Timing Summary

Setup

Worst Negative Slack (WNS): 0.000 ns
Total Negative Slack (TNS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 16

Hold

Worst Hold Slack (WHS): 0.461 ns
Total Hold Slack (THS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 16

Pulse Width

Worst Pulse Width Negative Slack (WPWS): 1.282 ns
Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 25

All user specified timing constraints are met.

Timing Summary - impl_1 (saved) x Timing Summary - timing_1 x Timing Summary - timing_2 x Timing Summary - timing_1(1) x Timing Summary - timing_3 x

IMPLEMENTED DESIGN - xc7z020clg484-1

Project Summary | **Device** | **Timing Constraints** | **Schematic** | **Path 2 - timing_2** | **Path 1 - timing_2** | **Schematic (2)**

42 Cells 26 I/O Ports 86 Nets

Path Properties - Path 2

Summary

| Name | Path 2 |
|-------------|--------------------------------|
| Slack | 6.436ns |
| Source | L2/Q_reg[0]C (rising edge-tri) |
| Destination | tmp0_reg[3]_lopt_replica/D |

Timing Summary

| Name | Slack | Levels | Routes | High Fanout | From | To | Total Delay | Logic Delay | Net Delay | Requirement | Source Clock | Destination Clock |
|--------|-------|--------|--------|-------------|--------------|-----------------------------|-------------|-------------|-----------|-------------|--------------|-------------------|
| Path 1 | 6.436 | 4 | 5 | 6 | L2/Q_reg[0]C | tmp0_reg[3]_lopt_replica/D | 3.420 | 0.952 | 2.468 | 10.0 | clk | clk |
| Path 2 | 6.436 | 4 | 5 | 6 | L2/Q_reg[0]C | tmp0_reg[3]_lopt_replica/D | 3.423 | 0.952 | 2.471 | 10.0 | clk | clk |
| Path 3 | 6.447 | 4 | 5 | 6 | L2/Q_reg[0]C | tmp0_reg[2]_lopt_replica/D | 3.406 | 0.952 | 2.454 | 10.0 | clk | clk |
| Path 4 | 6.491 | 3 | 4 | 8 | L2/Q_reg[0]C | tmp0_reg[0]_lopt_replica/CE | 3.204 | 0.828 | 2.376 | 10.0 | clk | clk |
| Path 5 | 6.491 | 3 | 4 | 8 | L2/Q_reg[0]C | tmp0_reg[1]_lopt_replica/CE | 3.204 | 0.828 | 2.376 | 10.0 | clk | clk |
| Path 6 | 6.491 | 3 | 4 | 8 | L2/Q_reg[0]C | tmp0_reg[2]_lopt_replica/CE | 3.204 | 0.828 | 2.376 | 10.0 | clk | clk |
| Path 7 | 6.491 | 3 | 4 | 8 | L2/Q_reg[0]C | tmp0_reg[3]_lopt_replica/CE | 3.204 | 0.828 | 2.376 | 10.0 | clk | clk |

IMPLEMENTED DESIGN - xc7z020clg484-1

Path Properties Path 1

Summary

| Name | Path 1 |
|-------------|---------------------------------|
| Slack | 6.661 ns |
| Source | L2/Q_reg[0]/C (rising edge tri) |
| Destination | tmp0_reg[0]/C (rising edge tri) |

Delay Type

| Delay Type | Incr (ns) | Path ... | Location | Netlist Resource(s) |
|----------------------|-----------|----------|---------------------|---------------------|
| FDRE (Prop_fdre_c_0) | (r) 0.456 | 6.094 | Site: SLICE_X113Y11 | L2/Q_reg[0]/Q |
| net (fo=2, routed) | 1.093 | 7.188 | Site: SLICE_X113Y11 | L0/tmp0_reg[0]_I10 |
| LUT6 (Prop_lut6_i_0) | (r) 0.124 | 7.312 | Site: SLICE_X113Y11 | L0/tmp0[3]_I_5/I |
| net (fo=1, routed) | 0.434 | 7.746 | Site: SLICE_X113Y12 | L0/tmp0[3]_I_5_n_0 |
| LUT5 (Prop_lut5_4_0) | (r) 0.124 | 7.870 | Site: SLICE_X113Y12 | L0/tmp0[3]_I_3/I |
| net (fo=1, routed) | 0.149 | 8.019 | Site: SLICE_X113Y12 | L0/tmp0[3]_I_3_n_0 |
| LUT4 (Prop_lut4_3_0) | (r) 0.124 | 8.143 | Site: SLICE_X113Y12 | L0/tmp0[3]_I_1/I |
| net (fo=4, routed) | 0.569 | 8.711 | Site: SLICE_X113Y12 | L0/tmp0[3]_I_1/I |
| FDRE | | | Site: SLICE_X113Y12 | tmp00 |
| Arrival Time | | 8.711 | | tmp0_reg[0]/C |

Destination Clock Path

| Delay Type | Incr (ns) | Path ... | Location | Netlist Resource(s) |
|---------------|-----------|----------|----------|---------------------|
| L2/Q_reg[0]/C | | | | |

Timing Summary - tmp1_1 (saved)

| Name | Slack | Levels | Routes | High Fanout | From | To | Total Delay | Logic Delay | Net Delay | Requirement | Source Clock | Destination Clock |
|--------|-------|--------|--------|-------------|-----------------|----------------------------|-------------|-------------|-----------|-------------|--------------|-------------------|
| Path 1 | 6.661 | 3 | 4 | 4 | L2/Q_reg[0]/C | tmp0_reg[0]/C | 3.073 | 0.828 | 2.245 | 10.0 | clk | clk |
| Path 2 | 6.661 | 3 | 4 | 4 | L2/Q_reg[0]/C | tmp0_reg[1]/C | 3.073 | 0.828 | 2.245 | 10.0 | clk | clk |
| Path 3 | 6.661 | 3 | 4 | 4 | L2/Q_reg[0]/C | tmp0_reg[2]/C | 3.073 | 0.828 | 2.245 | 10.0 | clk | clk |
| Path 4 | 6.661 | 3 | 4 | 4 | L2/Q_reg[0]/C | tmp0_reg[3]/C | 3.073 | 0.828 | 2.245 | 10.0 | clk | clk |
| Path 5 | 6.839 | 3 | 4 | 4 | L1/4/Q_reg[0]/C | tmp3_reg[2]_lopt_replica/D | 3.001 | 0.828 | 2.173 | 10.0 | clk | clk |
| Path 6 | 6.953 | 3 | 4 | 4 | L1/4/Q_reg[0]/C | tmp3_reg[0]_lopt_replica/D | 2.863 | 0.828 | 2.035 | 10.0 | clk | clk |
| Path 7 | 6.969 | 3 | 4 | 4 | L1/4/Q_reg[0]/C | tmp3_reg[0]/D | 2.861 | 0.828 | 2.033 | 10.0 | clk | clk |

The screenshot displays the Xilinx Vivado IDE interface. The top pane shows the 'Create Clock' dialog with the 'clk' clock name and a period of 3.339 ns. The bottom pane shows the 'Design Timing Summary' report, which indicates that all user-specified timing constraints are met.

Create Clock Dialog:

| Position | Clock Name | Period (ns) | Rise At (ns) | Fall At (ns) | Add Clock | Source Objects | Source File | Scoped Cell | Current Instance |
|----------|------------|-------------|--------------|--------------|--------------------------|-----------------|--------------|-------------|------------------|
| 1 | clk | 3.339 | 0.000 | 1.669 | <input type="checkbox"/> | [get_ports clk] | Zedboard.xdc | | |

Design Timing Summary:

| Setup | | Hold | | Pulse Width | |
|------------------------------|----------|------------------------------|----------|--|----------|
| Worst Negative Slack (WNS): | 0.000 ns | Worst Hold Slack (WHS): | 0.163 ns | Worst Pulse Width Slack (WPWS): | 1.169 ns |
| Total Negative Slack (TNS): | 0.000 ns | Total Hold Slack (THS): | 0.000 ns | Total Pulse Width Negative Slack (TPWS): | 0.000 ns |
| Number of Failing Endpoints: | 0 | Number of Failing Endpoints: | 0 | Number of Failing Endpoints: | 0 |
| Total Number of Endpoints: | 72 | Total Number of Endpoints: | 72 | Total Number of Endpoints: | 85 |

All user specified timing constraints are met.

Από τα παραπάνω συμπεραίνουμε πως η πιο γρήγορη λύση είναι η pipelined αλλά σε αντίθεση με την πρώτη χρησιμοποιούνται περισσότεροι πόροι.

Σημειώσεις:

- Τα αρχεία των projects βρίσκονται στον φάκελο ./src.
- Για οποιαδήποτε απορία πάνω στην άσκηση, παρακαλώ να επικοινωνήσετε μαζί μου στο email: sdi1600048@di.uoa.gr