wen-cpu: DMA design of CPU

wen

dingzhiwen18@gmail.com

2023/8/12

1. Overview

General structure of DMA



* 1. Design specifications

a 32-bit AHB Slave Interface.

a 32-bit AHB master Interface.

Four independent configurable channels with fixed priority arbitration.

Supports bi-directional transfer of memory and peripherals.

Programmable data transfer up to 1024 (32×8×4).

1. Transmission method
   1. Memory to Memory

SDRAM → FIFO → SDRAM

* 1. Memory to Peripheral
  2. Peripheral to Memory

Continuous USART data reception

2.4 Peripheral to Peripheral

ADC sampled values are sent out via USART

1. Working mode
   1. Normal mode

After the channel is configured, the DMA transfers only once according to the configuration. When the transfer is completed, the DMA channel is automatically shut down and a new DMA channel needs to be configured to continue the new transfer.

* 1. Cyclic mode

When a transfer is completed once, it will be followed by a new transfer as configured in the previous one, unless the DMA channel is turned off. Suitable for handling continuous data streams.

* 1. Double-buffered mode

There are two memory areas set up so that when the first memory transfer is complete, it automatically switches to the second to continue the transfer and keeps switching. It is generally used for peripheral to memory or memory to peripheral transfer. It is very efficient in signal coding and decoding output, and continuous output of video and audio.

1. Modules
   1. Channel

Consists of four single FIFOs.



* 1. Interface



32-bit control signal: ch\_x\_en= ctrl[0]、ch\_x\_target=ctrl[4]、ch\_x\_size=ctrl[17:8]

32-bit source address: ch\_x\_source

32-bit dest address: ch\_x\_dest

* 1. Ahb\_ctrl



* 1. Arbiter



* 1. Channel\_ctrl