











SN74AHC1G04

SCLS318T-MARCH 1996-REVISED JANUARY 2016

SN74AHC1G04 Single Inverter Gate

Features

- Operating Range 2 V to 5.5 V
- Max t_{pd} of 6.5 ns at 5 V
- Low Power Consumption, 10-µA Max I_{CC}
- ±8-mA Output Drive at 5 V
- Schmitt-Trigger Action at All Inputs Makes the Circuit Tolerant for Slower Input Rise and Fall
- Latch-Up Performance Exceeds 250 mA Per JESD 17

Applications

- Cameras
- E-Meters
- **Ethernet Switches**
- Infotainment

3 Description

The SN74AHC1G04 contains one inverter gate. The device performs the Boolean function $Y = \overline{A}$.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
	SOT-23 (5)	2.90 x 1.60 mm
SN74AHC1G04	SC-70 (5)	2.00 x 1.30 mm
	SOT-553 (5)	1.65 x 1.20 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic







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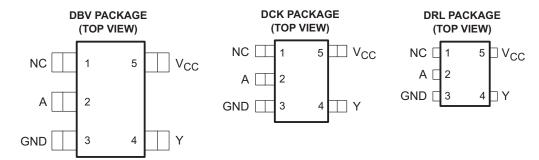
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section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Deleted Ordering Information table.

Changes from Revision Q (June 2005) to Revision R **Page**



5 Pin Configuration and Functions



NC – No internal connection See mechanical drawings for dimensions.

Pin Functions

F	PIN	TYPE	DESCRIPTION				
NO.	NAME	ITPE	DESCRIPTION				
1	NC	_	No Connection				
2	Α	I	Input A				
3	GND		Ground Pin				
4	Υ	0	Output Y				
5	V _{CC}	_	Power Pin				



6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage range	Supply voltage range			
VI	Input voltage range ⁽²⁾		-0.5	7	V
Vo	Output voltage range (2)	-0.5	$V_{CC} + 0.5$	V	
I _{IK}	Input clamp current	V _I < 0		-20	mA
I _{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
Io	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through each V _{CC} or G	IND		±50	mA
T _{stg}	Storage temperature range	-65	150	°C	
TJ	Junction temperature			150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	3500	
V _(ESD)	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	1000	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2	5.5	V
		V _{CC} = 2 V	1.5		
V_{IH}	High-level input voltage	V _{CC} = 3 V	2.1		V
		V _{CC} = 5.5 V	3.85		
		V _{CC} = 2 V		0.5	
V_{IL}	Low-level input voltage	V _{CC} = 3 V		0.9	V
		V _{CC} = 5.5 V		1.65	
V _{IH}	Input voltage		0	5.5	V
Vo	Output voltage		0	V _{CC}	V
	· · · · · ·	V _{CC} = 2 V		-50	μA
I _{OH}	High-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		-4	4
		$V_{CC} = 5 V \pm 0.5 V$		-8	mA
		V _{CC} = 2 V		50	μΑ
I_{OL}	Low-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		4	Λ
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		8	mA
۸ + / ۸	land the relation vice on fall note	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		100	0/
Δt/Δv	Input transition rise or fall rate	$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		20	ns/V
T _A	Operating free-air temperature		-40	125	°C

All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs (SCBA004).

⁽²⁾ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



6.4 Thermal Information

			SN74AHC1G04				
	THERMAL METRIC ⁽¹⁾	DBV	DCK	DRL	UNIT		
			5 PINS	•			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	231.3	287.6	328.7			
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	119.9	97.7	105.1			
$R_{\theta JB}$	Junction-to-board thermal resistance	60.6	65.0	150.3	°C/W		
ΨЈТ	Junction-to-top characterization parameter	17.8	2.0	6.9			
Ψ_{JB}	Junction-to-board characterization parameter	60.1	64.2	148.4			

⁽¹⁾ For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report (SPRA953).

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS	V _{CC}	T	λ = 25°C		-40°C to	85°C	-40°C to 1	25°C	UNIT
PARAMETER	AKAMETEK TEST CONDITIONS		MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
		2 V	1.9	2		1.9		1.9		
	$I_{OH} = -50 \mu A$	3 V	2.9	3		2.9		2.9		
V _{OH}		4.5 V	4.4	4.5		4.4		4.4		V
	$I_{OH} = -4 \text{ mA}$	3 V	2.58			2.48		2.48		
	$I_{OH} = -8 \text{ mA}$	4.5 V	3.94			3.8		3.8		
		2 V			0.1		0.1		0.1	
	$I_{OH} = 50 \mu A$	3 V			0.1		0.1		0.1	
V _{OL}		4.5 V			0.1		0.1		0.1	V
	I _{OL} = 4 mA	3 V			0.36		0.44		0.44	
	I _{OL} = 8 mA	4.5 V			0.36		0.44		0.44	
l _l	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1		±1	μΑ
I _{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			1		10		10	μΑ
C _i	V _I = V _{CC} or GND	5 V		2	10		10		10	pF

6.6 Switching Characteristics, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

The result of the same of the											
DADAMETED	FROM	то	OUTPUT	1	Γ _A = 25°C		−40°C to	85°C	−40°C to	125°C	UNIT
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
t _{PLH}	^	V	C 45 pF		5	7.1	1	8.5	1	9.5	2
t _{PHL}	A	ī	$C_L = 15 pF$		5	7.1	1	8.5	1	9.5	ns
t _{PLH}	^	Y	C 50 pF		7.5	10.6	1	12	1	13	2
t _{PHL}	А		$C_L = 50 pF$		7.5	10.6	1	12	1	13	ns

6.7 Switching Characteristics, $V_{CC} = 5 V \pm 0.5 V$

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM	то	OUTPUT	T	_A = 25°C		−40°C to	85°C	–40°C to	125°C	UNIT			
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII			
t _{PLH}	٨	V	C - 15 pE		3.8	5.5	1	6.5	1	7	20			
t _{PHL}	А	ī	$C_L = 15 pF$		3.8	5.5	1	6.5	1	7	ns			
t _{PLH}	٨	V	C - 50 pF		5.3	7.5	1	6.5	1	7	20			
t _{PHL}	А	Y	Y	Y	Y C _L = 50 pr	$C_L = 50 \text{ pF}$		5.3	7.5	1	6.5	1	7	ns

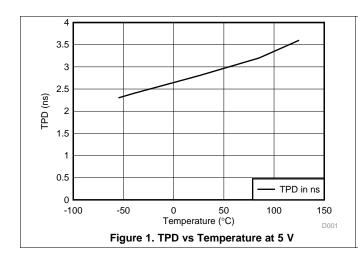


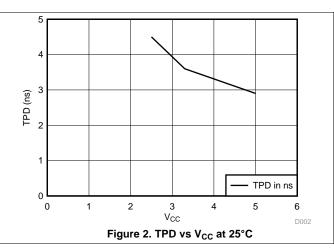
6.8 Operating Characteristics

 V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST C	ONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	12	pF

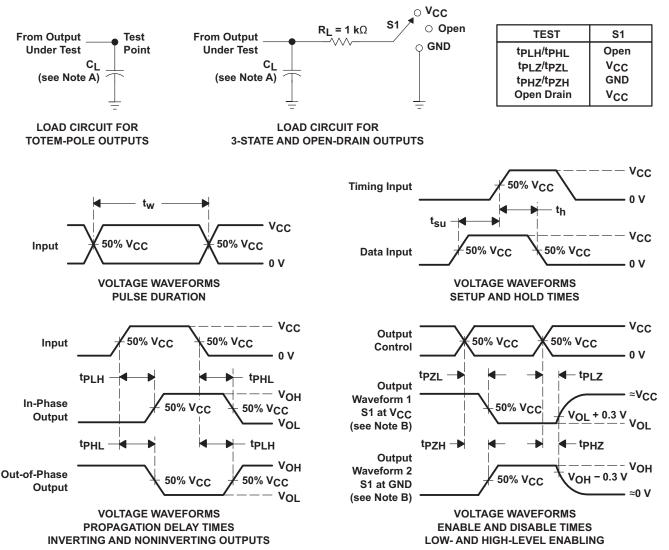
6.9 Typical Characteristics







7 Parameter Measurement Information



- A. C_I includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 - Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 3 ns, $t_f \leq$ 3 ns
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit And Voltage Waveforms

Product Folder Links: SN74AHC1G04

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8 Detailed Description

8.1 Overview

The SN74AHC1G04 device contains one inverter gate. The device performs the Boolean function $Y = \overline{A}$.

This single gate inverter has Schmitt-Trigger action on its input, allowing for slower rise and fall times and some noise rejection. This is not a true Schmitt-Trigger, so there is a limit on rise and fall times.

8.2 Functional Block Diagram



Figure 4. Logic Diagram (Positive Logic)

8.3 Feature Description

- · Wide operating voltage range
 - Operates from 2 V to 5.5 V
- Allows down-voltage translation
 - Inputs accept voltages to 5.5 V
- · Lower drive
 - This will produce slower edges and help prevent ringing on outputs

8.4 Device Functional Modes

Table 1. Function Table

INPUT A	OUTPUT Y
Н	L
L	Н



9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

SN74AHC1G04 is a low-drive CMOS device that can be used for a multitude of inverting buffer type functions. It can produce 8 mA of drive current at 5 V, making it Ideal for driving multiple outputs and good for low-noise applications. The inputs are 5.5-V tolerant, allowing it to translate down to V_{CC} .

9.2 Typical Application

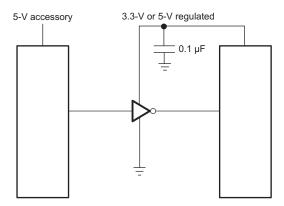


Figure 5. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

- 1. Recommended Input Conditions
 - For rise time and fall time specifications, see $\Delta t/\Delta V$ in the Recommended Operating Conditions table.
 - For specified High and low levels, see V_{IH} and V_{IL} in the Recommended Operating Conditions table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
- 2. Recommend Output Conditions
 - Load currents should not exceed 25 mA per output and 50 mA total for the part.
 - Outputs should not be pulled above V_{CC}.



Typical Application (continued)

9.2.3 Application Curves

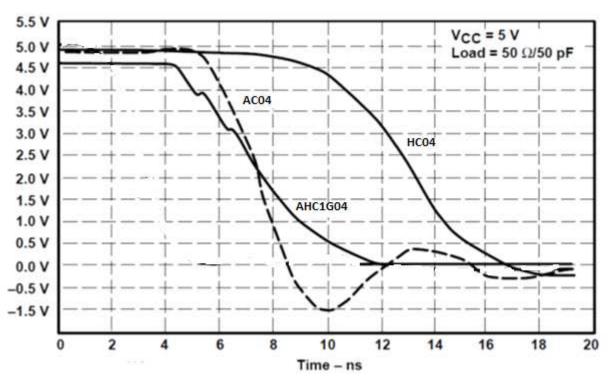


Figure 6. Typical Application Curve

10 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μ F is recommended. If there are multiple V_{CC} pins, 0.01 μ F or 0.022 μ F is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μ F and 1 μ F are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

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11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 7 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

11.2 Layout Example

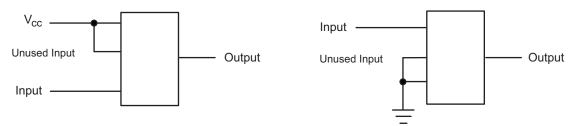


Figure 7. Layout Diagram

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.





3-Apr-2016

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
SN74AHC1G04DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 125	(A043 ~ A04G ~ A04L ~ A04S)	Samples
SN74AHC1G04DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	A04G	Samples
SN74AHC1G04DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	A04G	Samples
SN74AHC1G04DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 125	(A043 ~ A04G ~ A04L ~ A04S)	Samples
SN74AHC1G04DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	A04G	Samples
SN74AHC1G04DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(AC3 ~ ACG ~ ACL ~ ACS)	Samples
SN74AHC1G04DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(AC3 ~ ACG ~ ACL ~ ACS)	Samples
SN74AHC1G04DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(AC3 ~ ACG ~ ACL ~ ACS)	Samples
SN74AHC1G04DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(AC3 ~ ACG ~ ACL ~ ACS)	Samples
SN74AHC1G04DCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(AC3 ~ ACG ~ ACL ~ ACS)	Samples
SN74AHC1G04DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(AC3 ~ ACG ~ ACL ~ ACS)	Samples
SN74AHC1G04DRLR	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(ACB ~ ACS)	Samples
SN74AHC1G04DRLRG4	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(ACB ~ ACS)	Samples
SN74AHC1G04HDCK3	OBSOLETI	E SC70	DCK	5		TBD	Call TI	Call TI	-40 to 85		

⁽¹⁾ The marketing status values are defined as follows: **ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.



PACKAGE OPTION ADDENDUM

3-Apr-2016

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74AHC1G04:

Automotive: SN74AHC1G04-Q1

NOTE: Qualified Version Definitions:

Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC1G04DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHC1G04DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHC1G04DBVR	SOT-23	DBV	5	3000	180.0	9.2	3.17	3.23	1.37	4.0	8.0	Q3
SN74AHC1G04DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHC1G04DBVT	SOT-23	DBV	5	250	180.0	9.2	3.17	3.23	1.37	4.0	8.0	Q3
SN74AHC1G04DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHC1G04DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHC1G04DCKR	SC70	DCK	5	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74AHC1G04DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHC1G04DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AHC1G04DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHC1G04DCKT	SC70	DCK	5	250	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74AHC1G04DRLR	SOT	DRL	5	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
SN74AHC1G04DRLR	SOT	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC1G04DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AHC1G04DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AHC1G04DBVR	SOT-23	DBV	5	3000	205.0	200.0	33.0
SN74AHC1G04DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AHC1G04DBVT	SOT-23	DBV	5	250	205.0	200.0	33.0
SN74AHC1G04DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74AHC1G04DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74AHC1G04DCKR	SC70	DCK	5	3000	205.0	200.0	33.0
SN74AHC1G04DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AHC1G04DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AHC1G04DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AHC1G04DCKT	SC70	DCK	5	250	205.0	200.0	33.0
SN74AHC1G04DRLR	SOT	DRL	5	4000	184.0	184.0	19.0
SN74AHC1G04DRLR	SOT	DRL	5	4000	202.0	201.0	28.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-178 Variation AA.



DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AA.



DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



DRL (R-PDSO-N5)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs.

 Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
- D. JEDEC package registration is pending.



DRL (R-PDSO-N5)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over—print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.



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