Cypress Roadmap:

USB Controllers

Q2 2016

USB Portfolio

	Device	Hub	Bridge	Host	Storage	Type-C
USB 3.1	**CYUSB301x** **FX3** 32-Bit Bus to USB 3.1 Gen 1 ARM9, 512KB RAM	**CYUSB33xx** **HX3** USB 3.1 Gen 1,Shared Link™[1] BC 1.2[2], Ghost Charge™[3]	**CYUSB306x** **CX3** CSI-2[4] to USB 3.1 Gen 1 4 CSI-2[4] Lanes, 1 Gbps/Lane		**CYUSB303x** **FX3S** 16-Bit Bus to USB 3.1 Gen 1 RAID[5], Dual SDXC[6]/eMMC[7]	**CYPD1xxx** **CCG1** USB Type-C Port Controller 1 PD Port, 5 Profiles, 100 W
	FX3PD USB 3.1 Gen 2 Type-C Peripheral Controller with PD **Contact Sales**	NEW **HX3C** Q216 USB 3.1 Gen 1 Type-C Hub with PD **Contact Sales**	**CYUSB361x** **GX3** USB 3.1 Gen 1 to GigE Energy Efficient Ethernet		**CYUSB302x** **SD3** USB 3.1 Gen 1 SD Reader SDXC[6]/eMMC[7], RAID[5]	**CYPD2xxx** **CCG2** USB Type-C Cable Controller 1 PD Port, Termination, ESD
		HX3PD USB 3.1 Gen 2 Type-C Hub with PD **Contact Sales**	**DX3** USB 3.1 Gen 1 to DSI[8] TX **Contact Sales**			NEW **CYPD3xxx** Q216 **CCG3** USB Type-C Port Controller 20-V, Crypto, Billboard
USB 2.0	**CY7C6801x/53** **FX2LP** 16-Bit Bus to USB 2.0 8051, 16KB RAM	**CY7C656x4** **HX2VL** 4 Ports 4 Transaction Translators	**GX2** USB 2.0 to 10/100 Ethernet **Contact Sales**	**CYWB016xBB** **Bay™** HS USB OTG Dual SDXC[6]/eMMC[7]	**CYWB0x2xABS** **Arroyo™, Astoria™** 16-Bit Bus to USB 2.0 8051, Dual SD/eMMC[7]	NEW **CYPD4xxx** Q216 **CCG4/CCG4M** USB Type-C Port Controller 2 PD Ports, 128KB Flash, Mux
	CY7C68003 **TX2UL** ULPI[9] PHY 13, 19.2, 24, 26 MHz	**CY7C656x1** **HX2LP** 4 Ports, Industrial Grade 1 Transaction Translator			**CY7C6803x** **NX2LP** NAND Flash to USB 2.0 8051, 15KB RAM	**CCG5** USB Type-C AFE **Contact Sales**
	CYUSB201x **FX2G2** 32-Bit Bus to USB 2.0 ARM9 512KB RAM				**CY7C683xx** **AT2LP** Parallel ATA to USB 2.0 8051	**Type-C product applies to any USB speed**
USB 1.1	**CY7C638xx** **enCoRe™ II** M8C MCU, 20 GPIOs SPI, 8KB Flash		**CY7C6521x** **USB-Serial** UART/SPI/I²C to USB 2 Channels, CapSense®	**SL811HS** FS USB Host/Device 256Byte RAM		
	CY7C64215 **enCoRe III** M8C MCU, 50 GPIOs, ADC I²C/SPI, 16KB Flash		**CY7C65213** **USB-to-UART (Gen 2)** 3 Mbps, 8 GPIOs	**CY7C67300** **EZ-Host** 4 Ports, FS USB OTG 32 GPIOs		
	CY7C643xx **enCoRe V** M8C MCU, 36 GPIOs, ADC I²C/SPI, 32KB Flash		**CY7C65210/7** **USB Billboard** ARM® Cortex® M0 1 or 2 UART/SPI/I²C channels	**CY7C67200** **EZ-OTG™** 2 Ports, FS USB OTG 25 GPIOs		

[1] Simultaneous USB 2.0 and SuperSpeed traffic on the same port
[2] Battery Charging specification v1.2
[3] Enables USB charging without host connection
[4] Camera Serial Interface v2.0
[5] Redundant array of independent disks
[6] SD extended capacity
[7] Embedded MultiMedia Card
[8] Display Serial Interface
[9] UTMI low-pin interface

	Production	Sampling	Development	Concept
Status				
Availability	QQYY	QQYY		

CCG1: USB Type-C and PD Port Controller

Applications

Notebooks, tablets, monitors, docking stations, power adapters, Type-C EMCAs and dongles

Features

32-bit MCU Subsystem
48-MHz ARM® Cortex®-M0 CPU with 32KB flash and 4KB SRAM

Integrated Analog Blocks
12-bit, 1-Msps ADC for V_{BUS} voltage and current monitoring
Dynamic overcurrent and overvoltage protection

Integrated Digital Blocks
Two configurable 16-bit TCPWM[1] blocks
One SCB[1]: I²C master or slave, SPI master or slave, or UART
Up to eight GPIOs

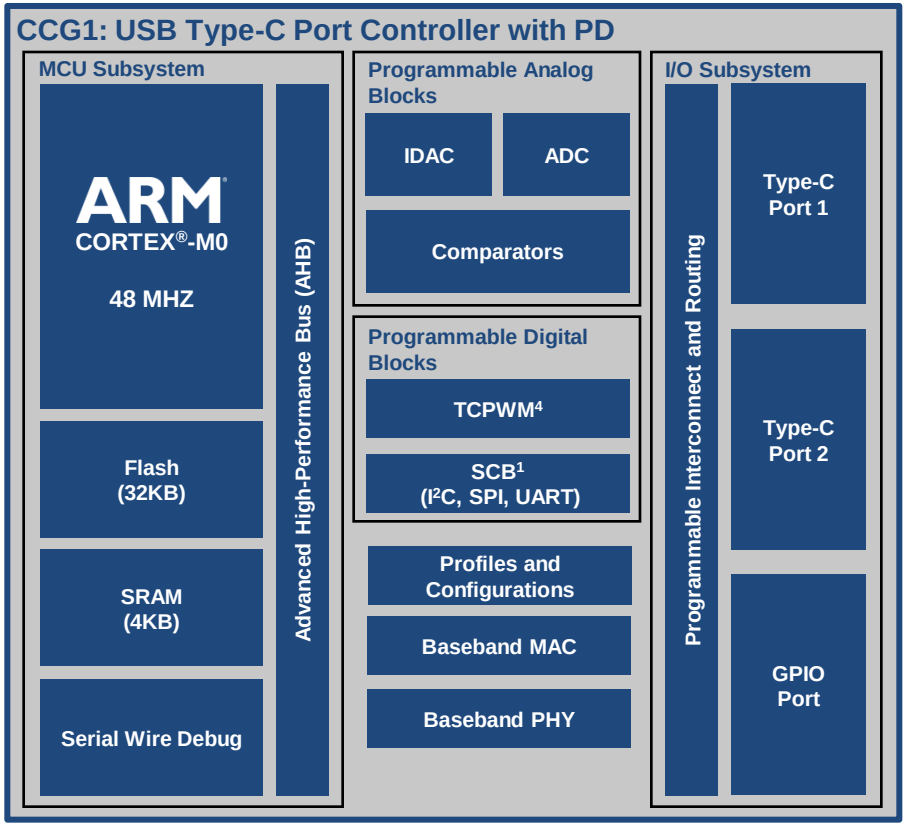
Type-C Support
Integrated Type-C Transceiver, supporting two Type-C ports
Controls routing of all protocols to an external MUX

PD Support
Supports Provider[2] and Consumer[3] roles and all power profiles

Low-Power Operation
1.71-5.5 V operation
Sleep: 1.3 mA, Deep Sleep: 1.3 µA

Packages
40-pin QFN (36 mm²), 35-ball CSP (6.8 mm²),
16-pin SOIC (60 mm²)

Block Diagram



Collateral

Datasheet: CCG1 Datasheet
Reference Design Kit: CCG1 RDK

Availability

Production: Now

[1] Serial communication block
[2] A Type-C port that sources power over V_{BUS}
[3] A Type-C port that sinks power from V_{BUS}
[4] Timer, counter, pulse-width modulation block

CCG2: USB Type-C and PD Port Controller

Applications

USB Type-C EMCA, Powered Accessories, UFP, DFP, DRP

Features

32-bit MCU Subsystem
48-MHz ARM® Cortex® -M0 CPU with 32KB flash and 4KB SRAM

Integrated Digital Blocks
Integrated timers, counters and pulse-width modulators
Two SCBs[1] configurable to I²C, SPI or UART modes

Type-C Support
Integrated transceiver, supporting one Type-C port
Integrated DFP (R_P[2]), UFP (R_D[3]), EMCA (R_A[4]) termination resistors

Power Delivery (PD) Support
Standard power profiles

Low-Power Operation
Two independent V_{CONN} rails with integrated isolation
Independent supply voltage pin for GPIO[5]
2.7-V to 5.5-V operation
Sleep: 2.0 mA; Deep Sleep: 2.5 µA

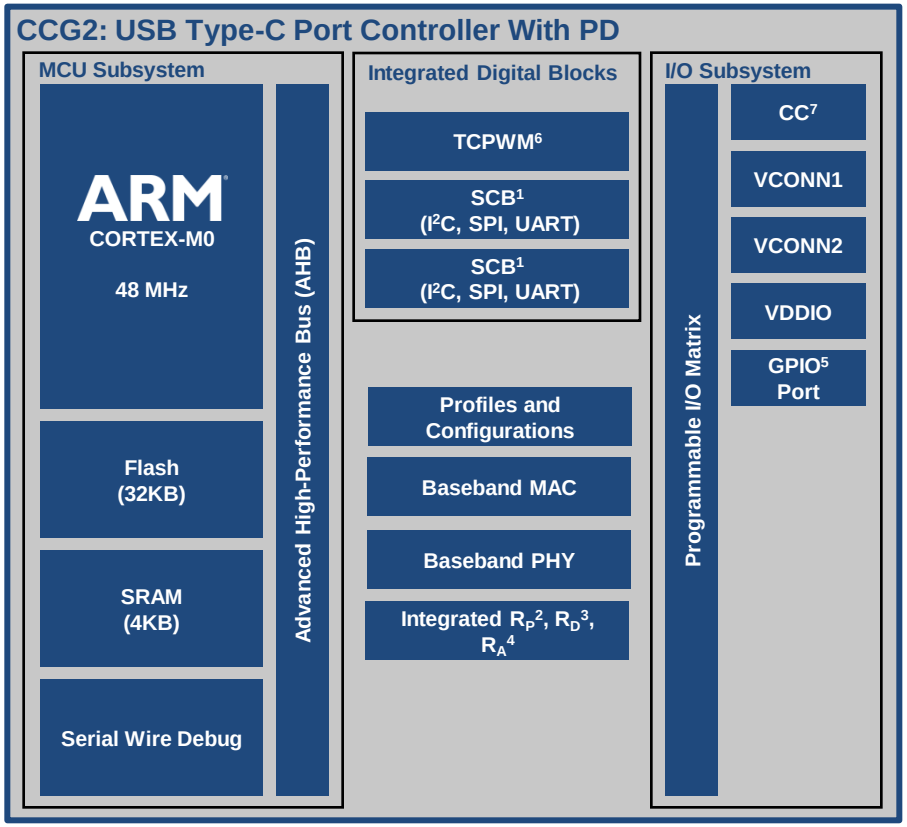
System-Level ESD on CC[6] and VDD Pins
±8-kV contact, ±15-kV Air Gap IEC61000-4-2 level 4C

Packages
20-ball, 3.3-mm² CSP with 0.4-mm ball pitch
14-pin 2.5mm x 3.5mm DFN with 0.6mm pin pitch
24-pin 4mm x 4mm QFN with 0.55mm pin pitch

Collateral

Datasheet: CCG2 Datasheet
Reference Design Kit: CCG2 RDK

Block Diagram



Availability

Production: Now

[1] Serial communication block configurable as UART, SPI or I²C
[2] Termination resistor read as a DFP
[3] Termination resistor read as a UFP
[4] Termination resistor read as an EMCA
[5] General-purpose input/output
[6] Timer, counter, pulse-width modulation block
[7] Configuration Channel

CCG3: USB Type-C and PD Port Controller

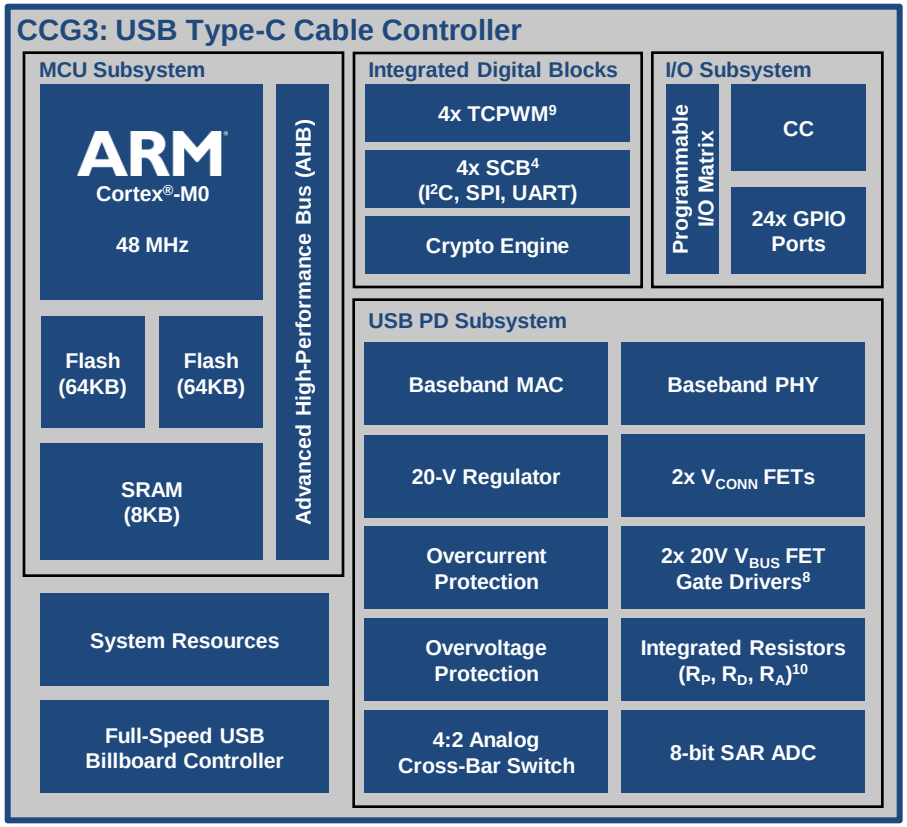
Applications

Accessories and power adapters

Features

Type-C Support
Integrated transceiver, supporting one Type-C port
Alternate Modes[1], Crypto Engine[2] for USB Authentication[3]
Power Delivery (PD) Support for Standard Power Profiles
Integrated Digital Blocks for V_{BUS} Power and MUX Interface
Four timers, counters and pulse-width modulators, 24x GPIOs
Four SCBs[4] for configurable master/slave I²C, SPI or UART
USB Billboard Controller[5] with Billboard Device Class[6] support
Integrated Analog Blocks for OVP, OCP[7]
20-V OVP[7] and OCP[8]; 4:2 cross-bar switch
32-bit ARM® Cortex®-M0 CPU with MCU Subsystem
2x64KB flash for fail-safe updates over CC, I²C or USB interfaces
Low-Power Operation
2x V_{BUS} Gate Drivers[8], for consumer and provider power paths
2x high-voltage (5-20 V, 25 V Max) V_{BUS} voltage inputs
Sleep: 2.0 mA; Deep Sleep: 2.5 µA with wake-on-I²C/wake-on-CC
System-Level ESD on CC/V_{CONN}, V_{BUS}, and SBU Pins
±8-kV contact, ±15-kV Air Gap IEC61000-4-2 level 4C
Packages
42-ball (8.5 mm²) CSP and 40-pin (36 mm²) QFN

Block Diagram



Collateral

Datasheet: CCG3 Datasheet

Availability

Samples: Now Production: Q2 2016

[1] Mode of operation in which the data lines are repurposed to transmit non-USB data
[2] The encryption hardware and software required to implement USB Authentication
[3] A USB-IF specification that defines the authentication protocol for Type-C accessories
[4] Serial communication block configurable as UART, SPI or I²C
[5] A USB Device controller that informs the USB Host of the supported Alternate Modes
[6] A specification that defines the method for a USB Device to communicate the supported Alternate Modes
[7] Overvoltage protection, overcurrent protection
[8] Circuits to control the gates of external power Field-Effect Transistors (FETs) on V_{BUS} (5-20 V)
[9] Timer/counter/pulse-width modulator block
[10] Termination resistors: R_P read as a DFP, R_D as a UFP, R_P as an EMCA

CCG4/4M: USB Type-C and PD Port Controller

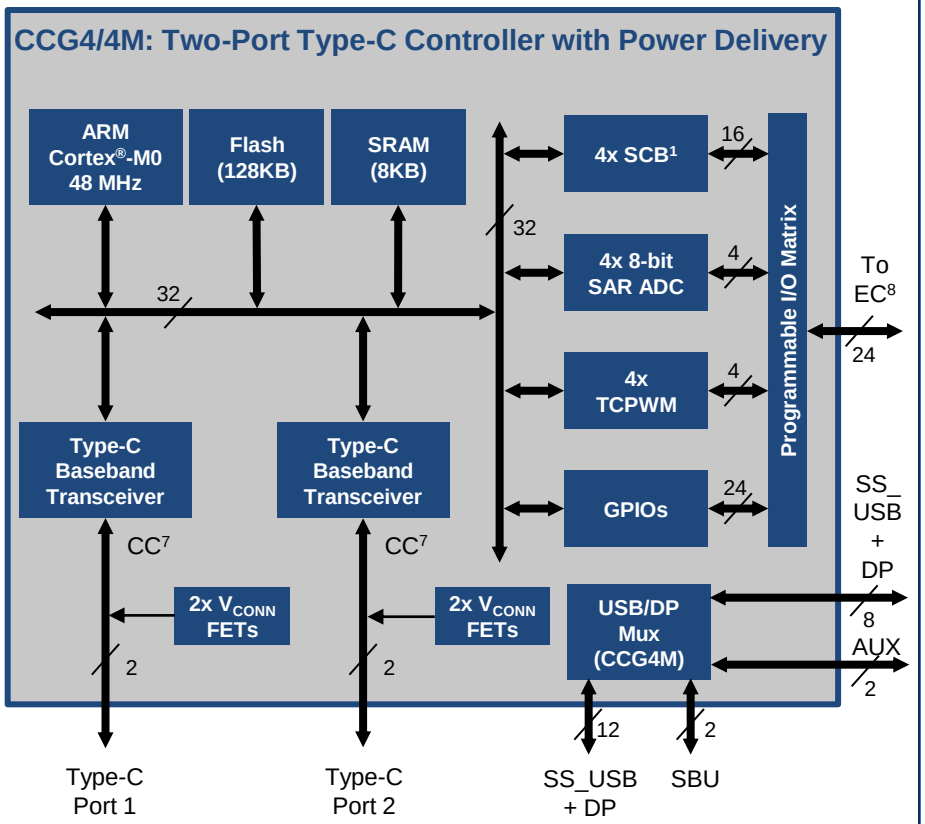
Applications

Notebooks, tablets, monitors, docking stations, power adapters

Features

Integrated USB Type-C Transceivers Support 2 Type-C Ports
Integrated 2x 1-W V_{CONN} FETs and 2x FET control signals, per port programmable R_P[1] and removable R_P[1], and R_D[2] terminations
Supports dead battery mode operation
Integrated SuperSpeed USB/DisplayPort (DP) Mux (CCG4M)
Increased Flash Enables Fail-Safe Bootup
Integrates 128KB flash to store dual firmware images
Dual firmware images enable Fail-Safe Bootup every time
Integrated Digital Blocks for Inter-Chip Communications
Four SCBs[3] master or slave configurable to I²C, SPI or UART
SCBs[3] interconnect CCG4 with embedded controller, two alternate muxes and Thunderbolt[4] controller (optional)
Integrated Blocks for OVP[5] and OCP[6]
Four 8-bit SAR ADCs configurable for OVP[5] and OCP[6]
Low-Power Operation
2.7-V to 5.5-V operation and independent supply voltage for general-purpose input/output (GPIO) Sleep: 2.0 mA; Deep Sleep: 2.5 µA with wake-on-I²C/wake-on-CC[7]
System-Level ESD on CC[7] Pins
±8-kV contact, ±15-kV Air Gap IEC61000-4-2 level 4C
32-bit ARM® Cortex® -M0 CPU with MCU Subsystem
128KB flash, upgradable over CC[7] lines or I²C interface
Packages 40-pin QFN, 96-ball BGA (CCG4M)

Block Diagram



Collateral

Datasheet: CCG4 Datasheet

Availability

Samples: Now Production: Q2 2016

[1] Termination resistor read as a DFP
[2] Termination resistor read as a UFP
[3] Serial communication block configurable as UART, SPI or I²C
[4] An interface jointly defined by intel and Apple that connects peripherals to a computer
[5] Overvoltage protection
[6] Overcurrent protection
[7] Configuration Channel
[8] Embedded controller in a PC

HX3C: USB 3.0 Type-C Hub[1] With Power Delivery (PD)[2]

Applications

USB Type-C charging Hubs[1], adapters and accessories
Docking stations for notebook PCs and tablets
Televisions and monitors
PC motherboards and servers
Set-top boxes, home gateways and routers

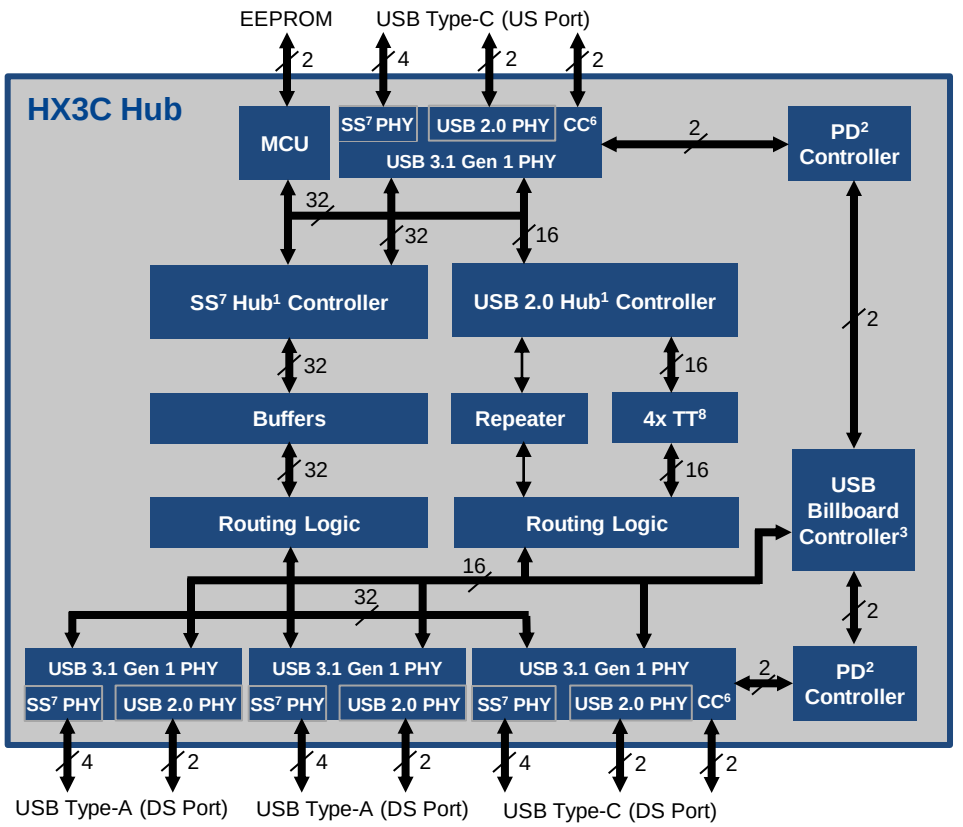
Features

USB 3.1 Gen 1-compliant Hub[1] controller
Upstream (US): Type-C
Downstream (DS): 1 Type-C and 2 Type-A ports
Integrated Type-C transceivers, supporting two ports
Integrated DFP (R_P) and UFP (R_D) termination resistors
Integrated USB Billboard Controller[3]
Charging Support: USB PD[2], BC v1.2[4], Apple Charging Standard[5]
PD policy engine configures power profiles dynamically
Ghost Charge™: Charging DS without US connection
Firmware upgradable over USB
System-Level ESD on CC[6] Pins: 8 kV contact, 15 kV air-configurable USB SS[7] and USB 2.0 PHY (drives 11" trace)
121-ball BGA (10 mm x 100 mm, 0.8 mm ball-pitch)

Collateral

Datasheet: HX3C Datasheet
Product Overview: HX3C Overview
App Note: *EZ-USB™ HX3C: USB Type-C Hub with Power Delivery*

Block Diagram



Availability

Samples: Q2 2016
Production: Q3 2016

[1] Directs data traffic between a USB Host and multiple USB Devices
[2] A new USB standard that increases power delivery over V_{BUS} from 7.5 W to 100 W
[3] A USB Device controller that is used to implement the USB Billboard Device Class Informs the USB Host of the supported Alternate Modes as well as any failures
[4] A specification published by the USB Implementers Forum (USB-IF) for charging portable USB Devices
[5] An Apple-specified battery charging standard for the iPhone, iPod and iPad
[6] Configuration Channel
[7] USB SuperSpeed
[8] Transaction Translator

GX3: USB 3.1 Gen 1 to Gigabit Ethernet Bridge

Applications

USB dongles, docking stations, USB port replicators
Network printers, security cameras
Ultrabooks, home gateways
Game consoles, portable media players
DVRs, IP set-top boxes, IP TVs
Other embedded systems

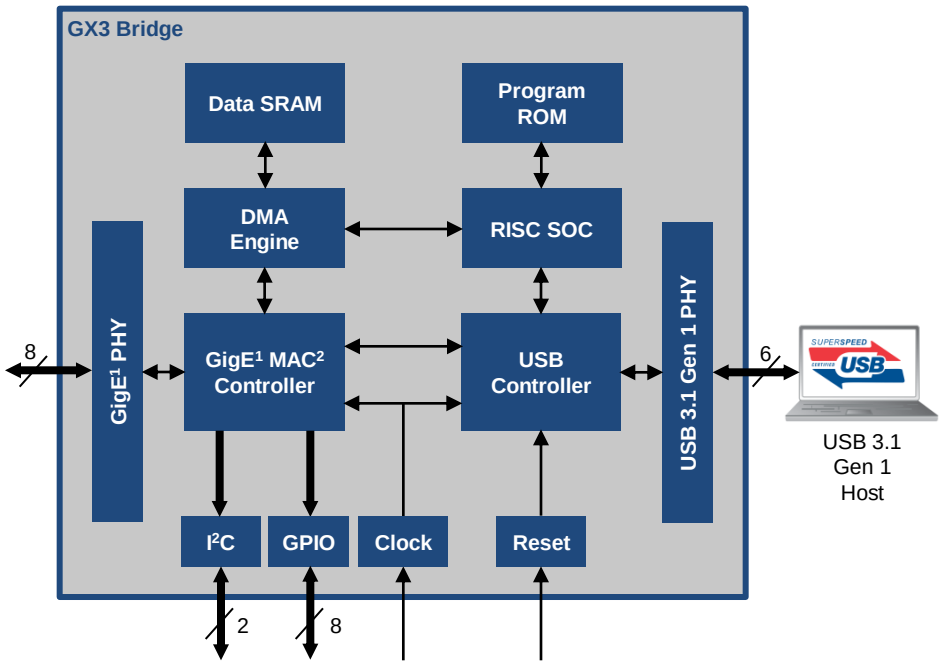
Features

One-chip USB 3.1 Gen 1 to 10/100/1000M GigE[1] bridge
Integrates USB 3.1 Gen 1 PHY and GigE[1] PHY
Integrates USB 3.1 Gen 1 Controller and GigE[1] MAC[2]
Needs only a 25-MHz crystal to drive both USB and GigE[1] PHY
IEEE 802.3az[3] support for low-power idle state
Supports dynamic cable length and power adjustment
Offers multiple power management Wake-on-LAN[4] features
Supports optional EEPROM to store USB descriptors
Integrates on-chip POR[5] circuitry
68-QFN (8 x 8 x 0.85 mm)

Collateral

Datasheet: GX3 Datasheet
Reference Design Kit: GX3 RDK
Software Drivers: GX3 Drivers

Block Diagram



Availability

Production: Now

[1] Gigabit Ethernet
[2] Media access controller that provides the address to an Ethernet node
[3] A new-energy efficient Ethernet standard
[4] An Ethernet standard that allows a computer to be turned on by a network message
[5] Power-on reset

HX3: USB 3.1 Gen 1 Hub

Applications

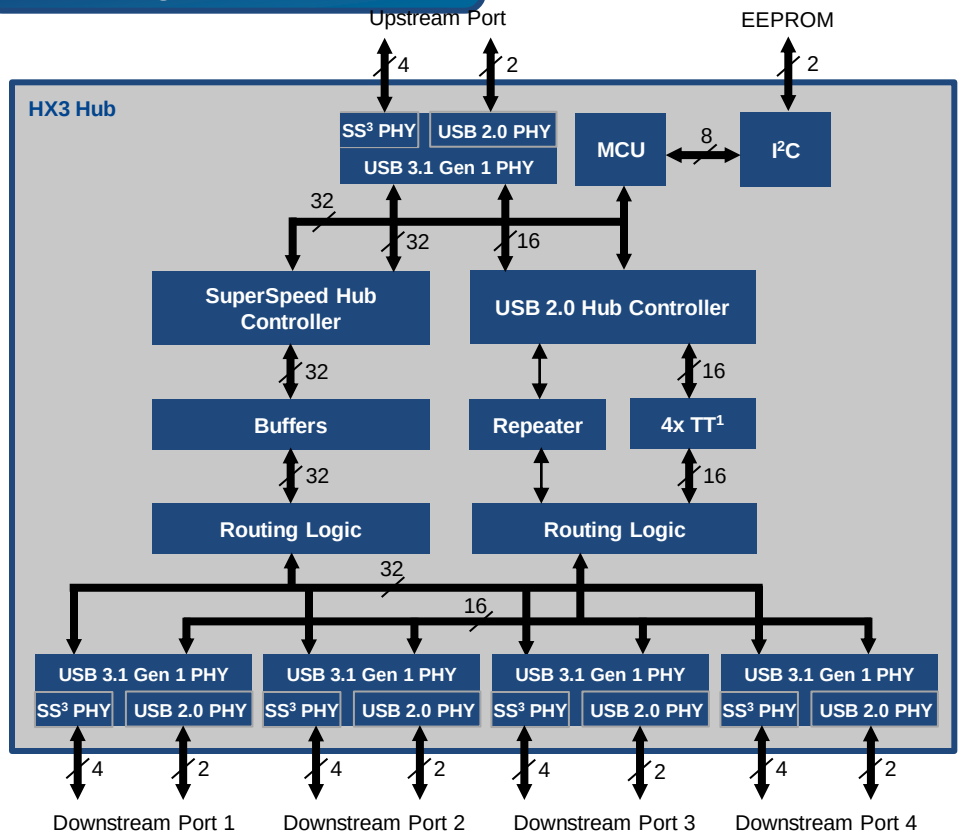
Docking stations for notebook PCs and tablets
PC motherboards, servers
Digital TV, monitors
Retail hub boxes
Printers, scanners
Set-top boxes, home gateways, routers, game consoles

Features

USB 3.1 Gen 1-compliant four-port Hub Controller
USB-IF certified (Test ID: 330000047)
WHQL certified for Windows 7, Window 8, Windows 8.1
Shared Link™: Supports simultaneous USB 2.0 and USB SuperSpeed (SS) Devices on the same port
Ghost Charge™: Enables USB charging while the Hub is disconnected from a USB Host
Charging Standard support:
- USB-IF Battery Charging v1.2
- Apple Charging Standard
- Charging an OTG Host in an ACA-Dock

Programming of external EEPROM via USB
Configurable USB SS & USB 2.0 PHY. Drives 11" trace
68-QFN (8 x 8 x 1.0 mm), 88-QFN (10 x 10 x 1.0 mm), 100-BGA (6 x 6 x 1.0 mm)

Block Diagram



Collateral

Datasheet:	HX3 Datasheet
Application Note:	HX3 Hardware Design Guide
Kits:	CY4609, CY4603, CY4613
Configuration Utility:	Blaster Plus[2]

Availability

Production: Now

[1] Transaction translator
[2] A Cypress GUI-based PC application for setting HX3 configuration parameters
[3] SuperSpeed

FX3: USB 3.1 Gen 1 Peripheral Controller

Applications

Industrial, medical and machine vision cameras
3-D, 1080p Full HD and 4K Ultra HD (UHD) cameras
Document scanners, fingerprint scanners
Videoconferencing systems
Data acquisition systems
Video capture cards and HDMI converters
Protocol and logic analyzers
USB test tools and software-designed radios (SDRs)

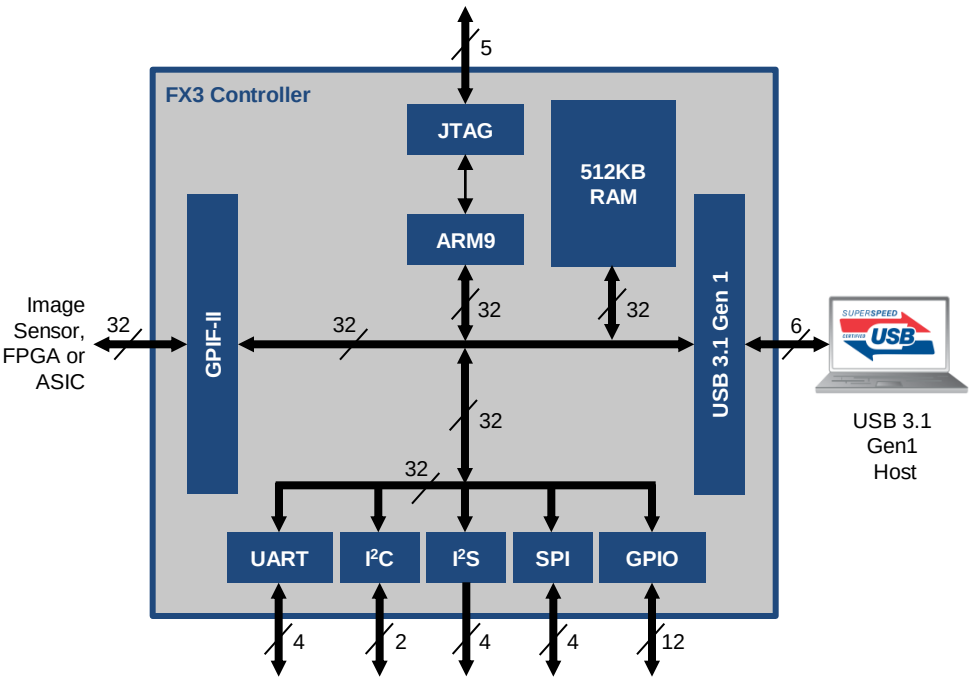
Features

USB 3.1 Gen 1-compliant Peripheral Controller
USB-IF certified (TID:340800007)
Fully accessible 32-bit, 200-MHz ARM926EJ core
512KB of embedded SRAM for code space and buffers
Up to 32-bit, 100-MHz, flexible GPIF II interface
Other peripheral interfaces such as I^2C, I^2S, UART, SPI and 12 GPIOs
Unused I/O pins can be used as GPIOs
Up to 32 USB endpoints
Flexible clock options:
  19.2-MHz crystal
  19.2-MHz, 26-MHz, 38.4-MHz and 52-MHz clock input
121-ball BGA (10 x 10 mm), 131-ball WLCSP (4.7 x 5.1 mm

Collateral

Datasheet:	FX3 Datasheet
Development Kit:	FX3 SuperSpeed Explorer Kit
Software Development Kit:	EZ-USB FX3 SDK

Block Diagram



Availability

Production: Now

FX3S: USB 3.1 Gen 1 RAID[1]-on-Chip

Applications

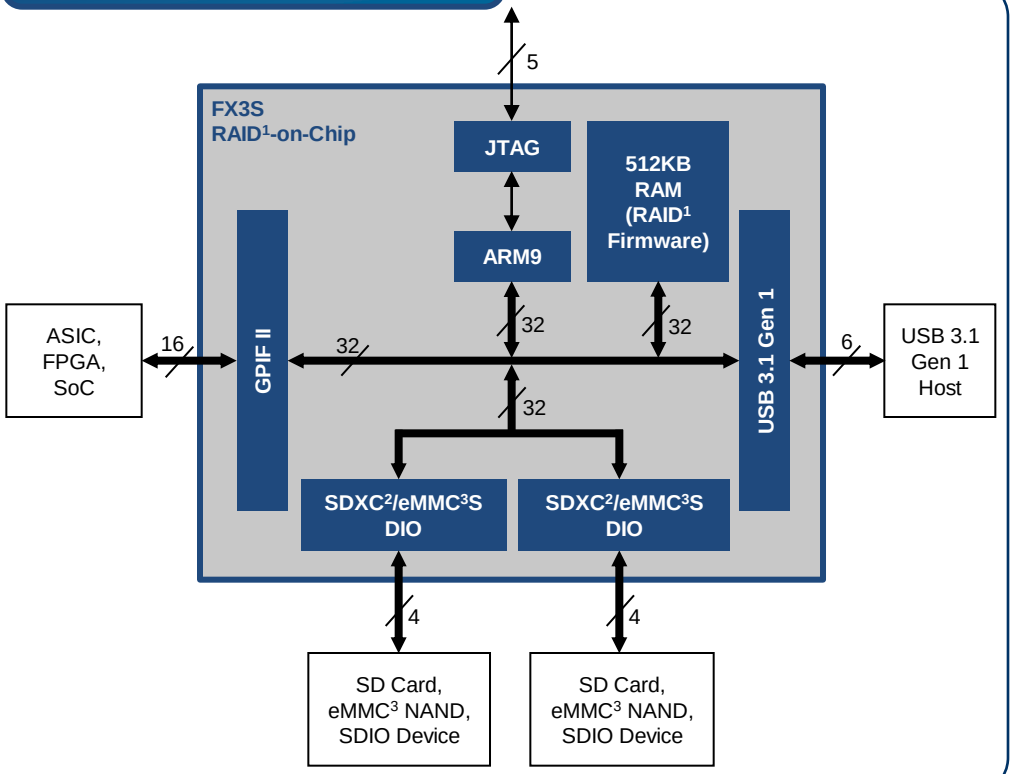
Servers, routers
Mobile storage, USB flash drives
POS terminals
Automatic Teller Machines (ATM)
SDIO expanders
Data logging devices

Features

USB 3.1 Gen 1-compliant Peripheral Controller
USB-IF certified (TID:340800007)
Fully accessible 32-bit, 200-MHz ARM926EJ core
512KB of embedded SRAM for code space and buffers
Up to 16-bit, 100-MHz, flexible GPIF II interface
Peripheral interfaces such as I[2]C, UART, SPI and GPIOs
Supports two SDXC[2], eMMC[3] 4.4, or SDIO 3.0 interfaces
Support RAID0 or RAID1 configurations
Flexible clock options:
- 19.2-MHz crystal
- 19.2-MHz, 26-MHz, 38.4-MHz and 52-MHz clock input

121-ball BGA (10 x 10 mm)
131-ball WLCSP (4.7 x 5.1 mm)

Block Diagram



Collateral

Datasheet	FX3S Datasheet
Kit:	FX3S RAID[1]-on-Chip Boot Disk Kit
Software:	FX3 Software Development Kit (SDK)
App Notes:	FX3S Hardware Design Guidelines
	USB RAID[1]1 Disk Design Using FX3S

Availability

Production: Now

[1] Redundant array of independent disks
[2] SD extended capacity
[3] Embedded MultiMedia Card

CX3: MIPI[1] CSI-2 to USB 3.1 Gen 1 Bridge

Applications

Industrial, medical and machine vision cameras
1080p Full HD and 4K Ultra HD (UHD) camera
Document scanners, fingerprint scanners
Game consoles
Videoconferencing systems
Notebook PCs, tablets
Image acquisition systems

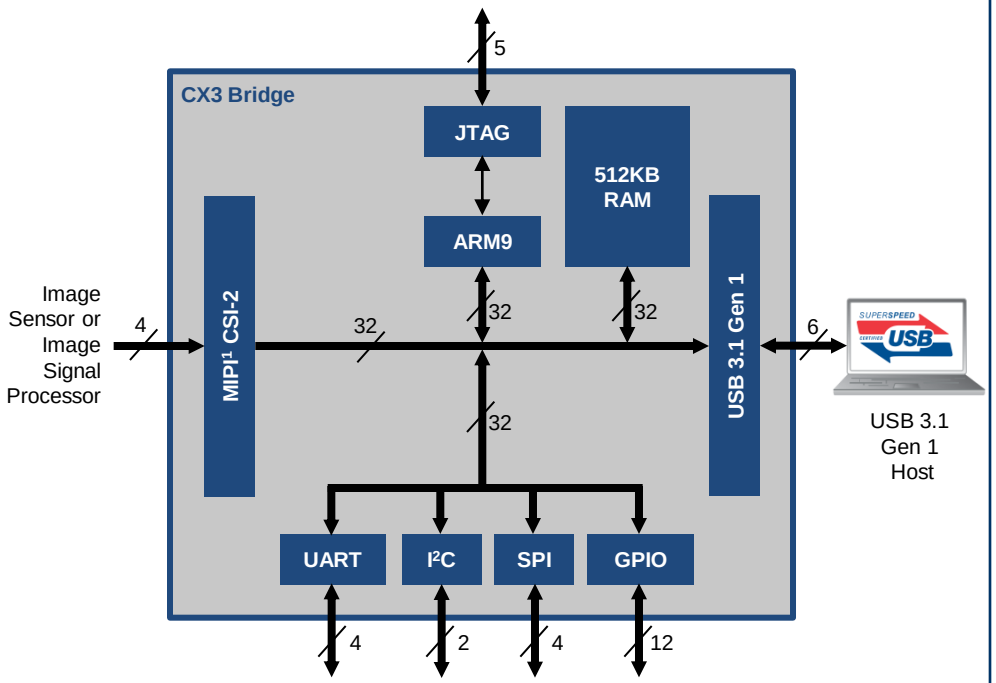
Features

USB 3.1 Gen 1-compliant video-class controller
Four-lane MIPI[1] Camera Serial Interface v2.0 (CSI-2) input
Camera Control Interface (CCI) for image sensor configuration
Supports industry-standard video data formats:
RAW8/10/12/14[2], YUV422/444[3], RGB888/666/565[4]
Supports uncompressed streaming video:
4K UHD at 15 fps, 1080p at 30 fps, 720p at 60 fps
On-chip ARM9 with 512KB RAM for data processing
Supports I²C, I²S, SPI, UART and 12 GPIOs
121-BGA (10 x 10 x 1.7 mm)

Collateral

Datasheet:	CX3 Datasheet
Reference Design Kit:	CX3 RDK
Software Development Kit:	EZ-USB SDK

Block Diagram



Availability

Production: Now

[1] Mobile Industry Processor Interface
[2] Video format for raw video data
[3] Video format for luminance and chrominance components
[4] Video format for red, green and blue pixel components