OPT8241-CDK-EVM SB REV2P0V1

This schematic is provided 'as is'
with no expressed or implied warranty.
The author accepts no liability if it causes any damage
to your system or any other equipment.

For evaluation only; not FCC approved for resale.

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ChangeLog:

Rev1p0: First Revision.
Rev1p1:
Changed all the obsolete part numbers.
Added controllability on the negative voltage supply.
Over voltage and reverse voltage protection added.
I2C level and other schematic bugs corrected.
Test points added according to feedback.
Rev2p0:
Optimimsed power supply assignnment.
Optimised IB supply layout for lower conduction losses.
Reduced indicator LED brightness.
Changed soldermask to black.
Rev2p0v1:
Version changed for matching IB change of increasing hole diameter.

Errata:

Pin D6 of U11 should ideally be connected to VCC_LDOAO. Please connect to VCC_LDOAO in new designs.

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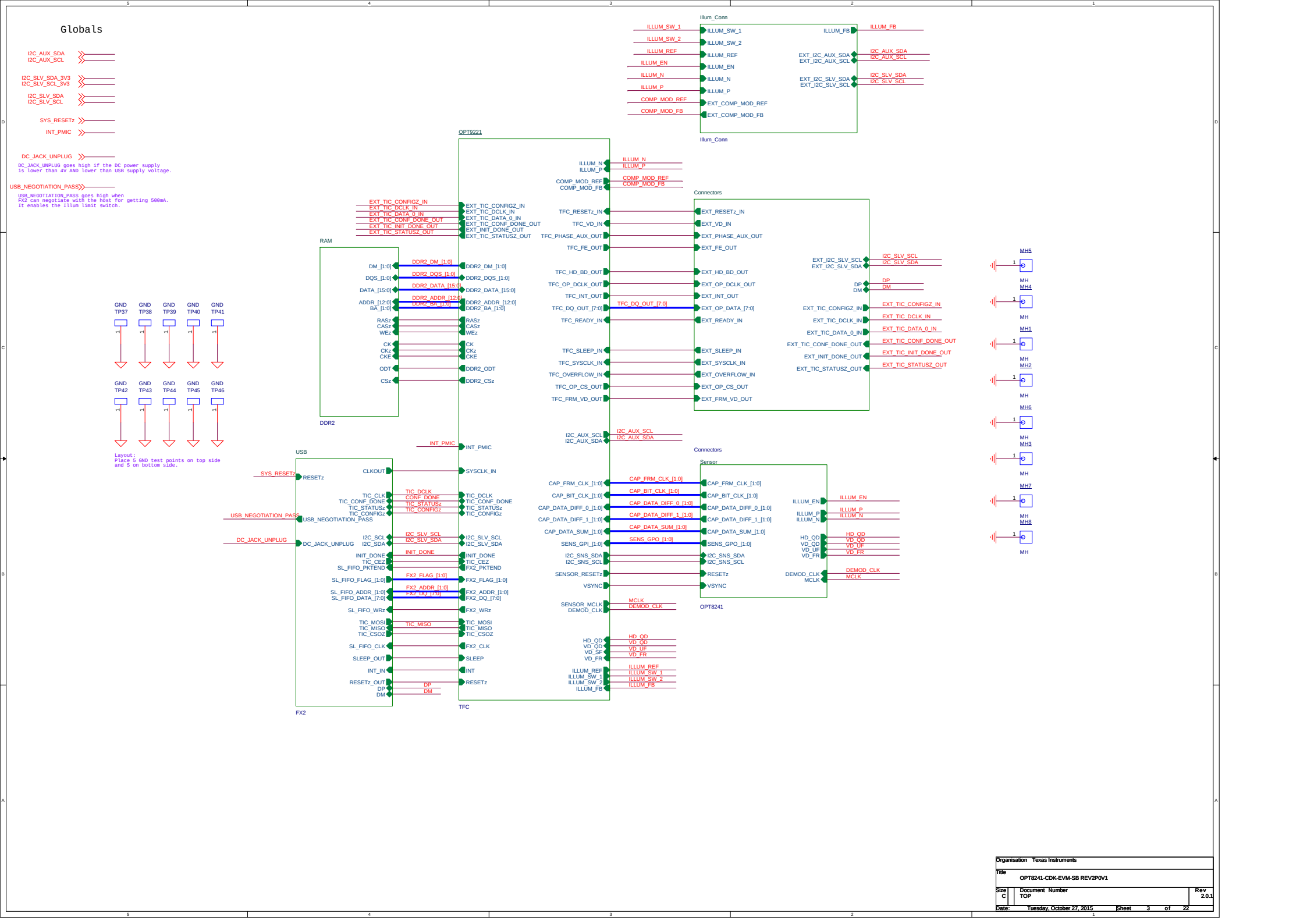
Globals
I2C_AUX_SDA
I2C_AUX_SCL
I2C_SLV_SDA_3V3
I2C_SLV_SCL_3V3
I2C_SLV_SDA
I2C_SLV_SCL
SYS_RESETz
INT_PMIC
DC_JACK_UNPLUG
DC_JACK_UNPLUG goes high if the DC power supply is lower than 4V AND lower than USB supply voltage.
USB_NEGOTIATION_PASS
USB_NEGOTIATION_PASS goes high when FX2 can negotiate with the host for getting 500mA. It enables the Illum limit switch.
GND TP37
GND TP38
GND TP39
GND TP40
GND TP41
GND TP42
GND TP43
GND TP44
GND TP45
GND TP46
Layout: Place 5 GND test points on top side and 5 on bottom side.
Illum_Conn
ILLUM_SW_1
ILLUM_SW_2
ILLUM_REF
ILLUM_EN
ILLUM_N
ILLUM_P
COMP_MOD_REF
COMP_MOD_FB
ILLUM_FB
EXT_I2C_AUX_SDA
EXT_I2C_AUX_SCL
EXT_I2C_SLV_SDA
EXT_I2C_SLV_SCL
EXT_COMP_MOD_REF
EXT_COMP_MOD_FB
OPT9221
EXT_TIC_CONFIGZ_IN
EXT_TIC_DCLK_IN
EXT_TIC_DATA_0_IN
EXT_TIC_CONF_DONE_OUT
EXT_INIT_DONE_OUT
EXT_TIC_STATUSZ_OUT
TFC_RESETz_IN
TFC_VD_IN
TFC_PHASE_AUX_OUT
TFC_FE_OUT
TFC_HD_BD_OUT
TFC_OP_DCLK_OUT
TFC_INT_OUT
TFC_DQ_OUT_[7:0]
TFC_READY_IN
TFC_SLEEP_IN
TFC_SYSCLK_IN
TFC_OVERFLOW_IN
TFC_OP_CS_OUT
TFC_FRM_VD_OUT
I2C_AUX_SCL
I2C_AUX_SDA
INT_PMIC
CAP_FRM_CLK_[1:0]
CAP_BIT_CLK_[1:0]
CAP_DATA_DIFF_0_[1:0]
CAP_DATA_DIFF_1_[1:0]
CAP_DATA_SUM_[1:0]
SENS_GPI_[1:0]
SENS_GPO_[1:0]
I2C_SNS_SDA
I2C_SNS_SCL
SENSOR_RESETz
VSYNC
SENSOR_MCLK
DEMOD_CLK
HD_QD
VD_QD
VD_UF
VD_FR
ILLUM_REF
ILLUM_SW_1
ILLUM_SW_2
ILLUM_FB
TFC
RAM
DM_[1:0]
DQS_[1:0]
DATA_[15:0]
ADDR_[12:0]
BA_[1:0]
RASz
CASz
WEz
CK
CKz
CKE
ODT
CSz
DDR2_DM_[1:0]
DDR2_DQS_[1:0]
DDR2_DATA_[15:0]
DDR2_ADDR_[12:0]
DDR2_BA_[1:0]
DDR2_ODT
DDR2_CSz
DDR2
USB
CLKOUT
RESETz
TIC_CLK
TIC_CONF_DONE
TIC_STATUSz
TIC_CONFIGz
USB_NEGOTIATION_PASS
I2C_SCL
I2C_SDA
INIT_DONE
TIC_CEZ
SL_FIFO_PKTEND
SL_FIFO_FLAG_[1:0]
SL_FIFO_ADDR_[1:0]
SL_FIFO_DATA_[7:0]
SL_FIFO_WRz
TIC_MOSI
TIC_MISO
TIC_CSOZ
SL_FIFO_CLK
SLEEP_OUT
INT_IN
RESETz_OUT
DP
DM
SYSCLK_IN
TIC_DCLK
TIC_CONF_DONE
TIC_STATUSz
TIC_CONFIGz
I2C_SLV_SCL
I2C_SLV_SDA
FX2_PKTEND
FX2_FLAG_[1:0]
FX2_ADDR_[1:0]
FX2_DQ_[7:0]
FX2_WRz
FX2_CLK
SLEEP
INT
RESETz
FX2
Connectors
EXT_RESETz_IN
EXT_VD_IN
EXT_PHASE_AUX_OUT
EXT_FE_OUT
EXT_HD_BD_OUT
EXT_OP_DCLK_OUT
EXT_INT_OUT
EXT_OP_DATA_[7:0]
EXT_READY_IN
EXT_SLEEP_IN
EXT_SYSCLK_IN
EXT_OVERFLOW_IN
EXT_OP_CS_OUT
EXT_FRM_VD_OUT
EXT_I2C_SLV_SCL
EXT_I2C_SLV_SDA
DP
DM
EXT_TIC_CONFIGZ_IN
EXT_TIC_DCLK_IN
EXT_TIC_DATA_0_IN
EXT_TIC_CONF_DONE_OUT
EXT_INIT_DONE_OUT
EXT_TIC_STATUSZ_OUT
Connectors
Sensor
CAP_FRM_CLK_[1:0]
CAP_BIT_CLK_[1:0]
CAP_DATA_DIFF_0_[1:0]
CAP_DATA_DIFF_1_[1:0]
CAP_DATA_SUM_[1:0]
SENS_GPO_[1:0]
I2C_SNS_SDA
I2C_SNS_SCL
RESETz
VSYNC
ILLUM_EN
ILLUM_P
ILLUM_N
HD_QD
VD_QD
VD_UF
VD_FR
DEMOD_CLK
MCLK
OPT8241
MH5
MH4
MH1
MH2
MH6
MH3
MH7
MH8
MH
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I2C_SLV_SDA_3V3
I2C_SLV_SCL_3V3

Power

VCC_USB_5V_IN
VCC_USB_IN
VCC_DC_JACK_5V_IN
VCC_DC_JACK_IN
I2C_SLV_SCL
I2C_SLV_SDA
I2C_AUX_SCL
I2C_AUX_SDA
SYS_RESETz
INT_PMIC
INT_OUT
DC_JACK_UNPLUG
USB_NEGOTIATION_PASS
USB_NEGOTIATION_PASS
VCC_OUT_1V5
VCC_OUT_1V8
VCC_OUT_3V3
VCC_OUT_PVDD
VCC_OUT_1V2
VCC_OUT_2V5
VCC_LDO_OUT_1V8
VCC_OUT_0V9
VCC_OUT_5V0_NEG
VCC_LDO_OUT_3V3
VCC_MAIN_OUT_5V
VCC_ILLUM_OUT_5V
VCC_FB
VCC_ILLUM_REF
VCC_AVDD_OUT_3V3
VCC_1V5
VCC_1V8
VCC_3V3
VCC_PVDD
VCC_1V2
VCC_2V5
VCC_LDO_1V8
VCC_0V9
VCC_5V0_MINUS
VCC_LDO_3V3
VCC_5V0_MAIN
VCC_5V0_ILLUM
VCC_ILLUM_FB
VCC_ILLUM_VREF
VCC_AVDD_OUT_3V3
Power

Illum

VCC_5V0_MINUS B7 BK1005HS100-T VCC_5V0_MINUS_ILLUM

VCC_ILLUM_FB B25 BK1005HS100-T VCC_ILLUM_FB_REF

3V3 and 1V8 powered from main power supply
to ensure power to EEPROMs etc if illum supply cuts off.
Use judiciously.

VCC_3V3 B4 100mA BK1005HS100-T VCC_ILLUM_DRV_3V3

VCC_1V8 B12 BKP1005EM100-T VCC_ILLUM_DRV_1V8

FX2

VCC_LDO_3V3 B22 BK1005HS100-T VCC_I2C_3V3

VCC_1V8 B23 85mA BK1005HS100-T VCC_FX2_1V8

VCC_LDO_3V3 B21 25mA BK1005HS100-T VCC_FX2_AVCC_3V3

TFC

VCC_3V3 B27 10mA BK1005HS100-T VCC_TFC_IOVDD_3V3

VCC_1V8 B20 50mA BK1005HS100-T VCC_TFC_IOVDD_1V8

VCC_1V2 B18 175mA BK1005HS100-T VCC_TFC_CORE_1V2

B14 75mA BK1005HS100-T VCC_TFC_PLL_1V2

DDR2

VCC_1V8 B19 100mA BK1005HS100-T VCC_DDR2_1V8

VCC_0V9 B13 5mA BK1005HS100-T VCC_DDR2_0V9

Sensor

VCC_LDO_1V8 B5 20mA BK1005HS100-T VCC_SENSOR_PLL_1V8

VCC_1V8 B9 5mA BK1005HS100-T VCC_SENSOR_IOVDD_1V8

B10 75mA BK1005HS100-T VCC_SENSOR_DVDD_1V8

B11 75mA BK1005HS100-T VCC_SENSOR_AVDD_1V8

VCC_3V3 B3 50mA BK1005HS100-T VCC_SENSOR_DVDD_3V3

VCC_AVDD_OUT_3V3 B2 50mA BK1005HS100-T VCC_SENSOR_AVDD_3V3

VCC_PVDD B6 5mA BK1005HS100-T VCC_SENSOR_PVDD

VCC_5V0_MINUS B1 20mA BK1005HS100-T VCC_5V0_MINUS_FSC

VCC_1V5 B26 500mA BK1005HS100-T VCC_MIX

TFC

VCC_2V5 B15 50mA BK1005HS100-T VCC_TFC_IOVDD_2V5

B16 5mA BK1005HS100-T VCC_TFC_CONFIG

B17 50mA BK1005HS100-T VCC_TFC_PLL_2V5

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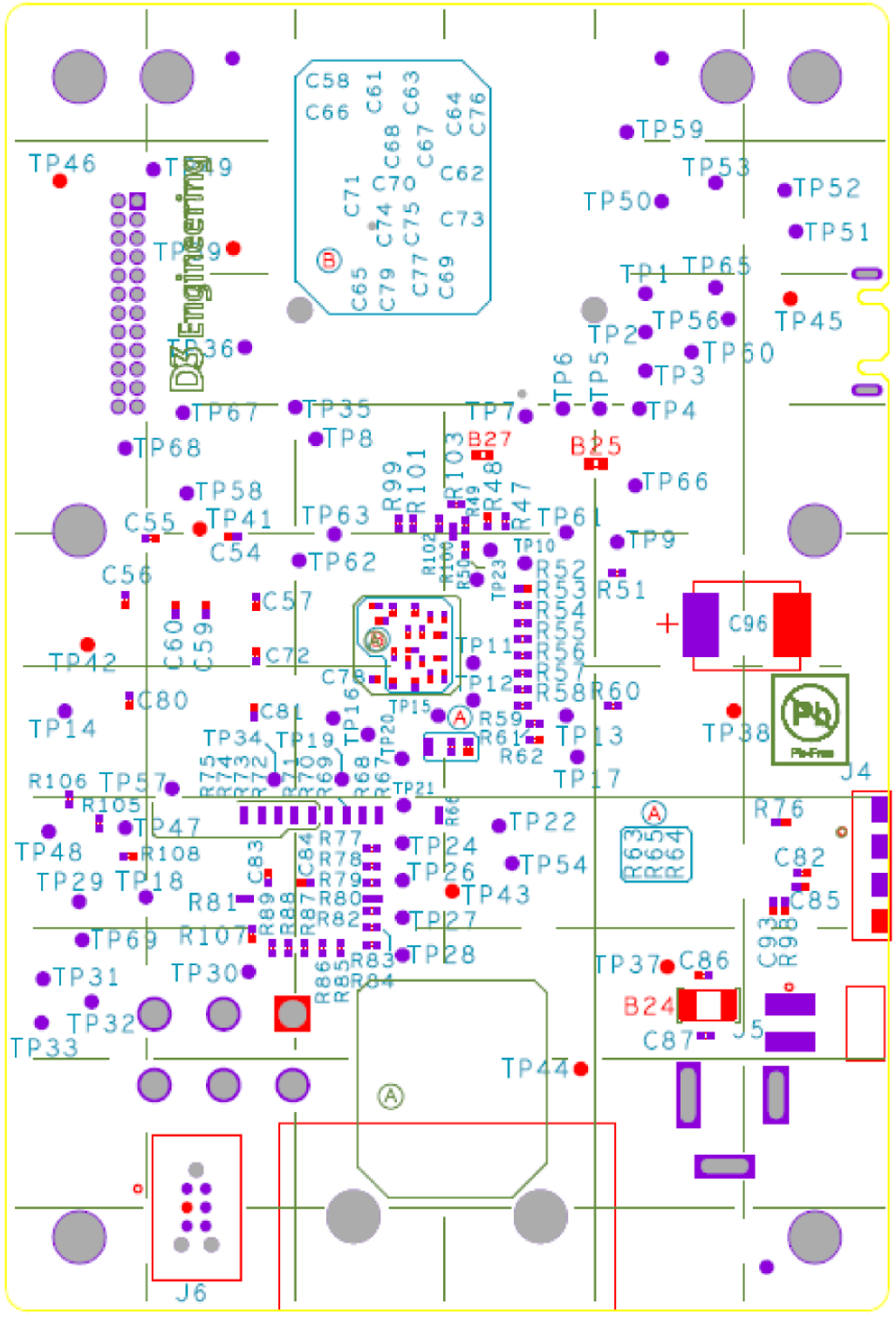

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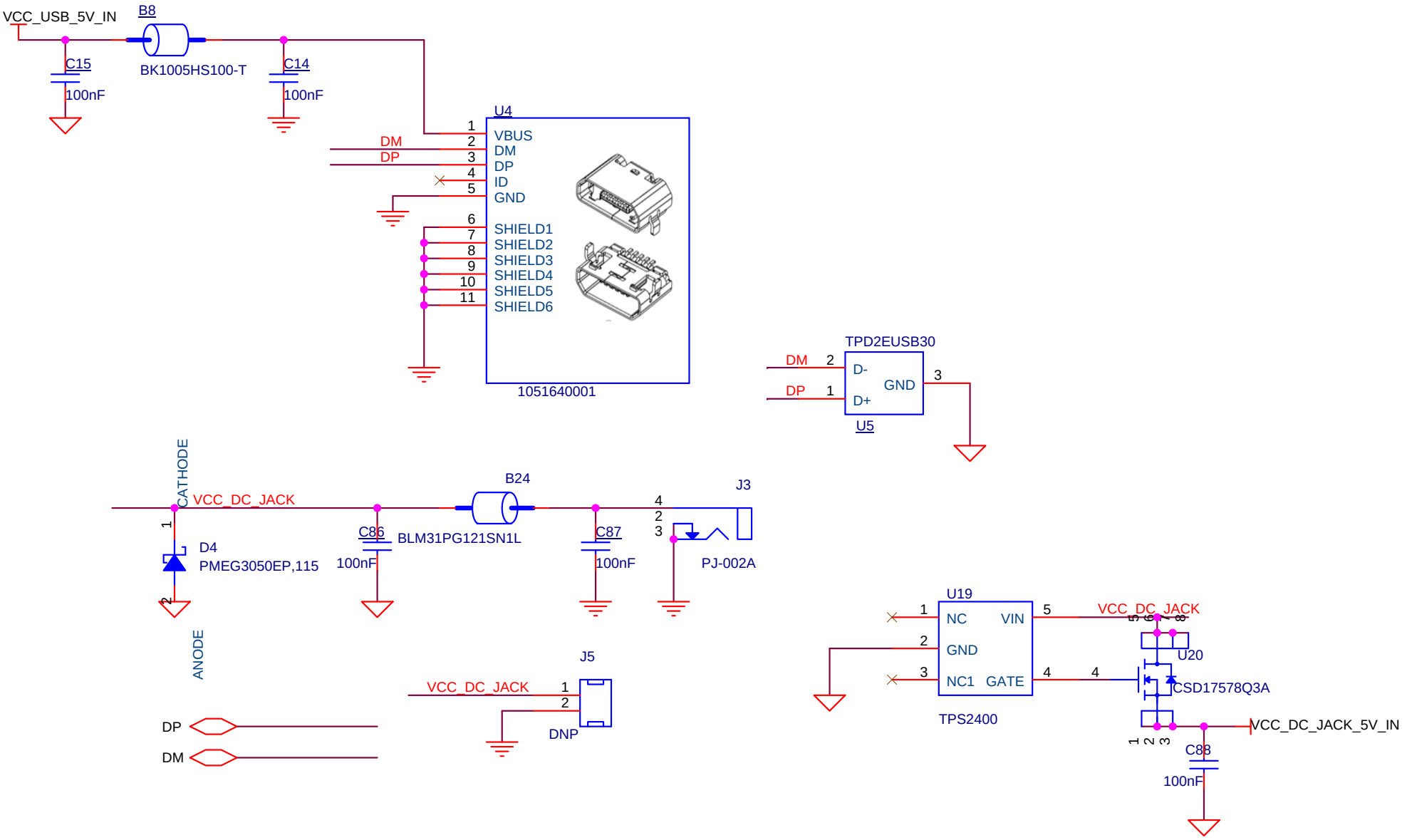

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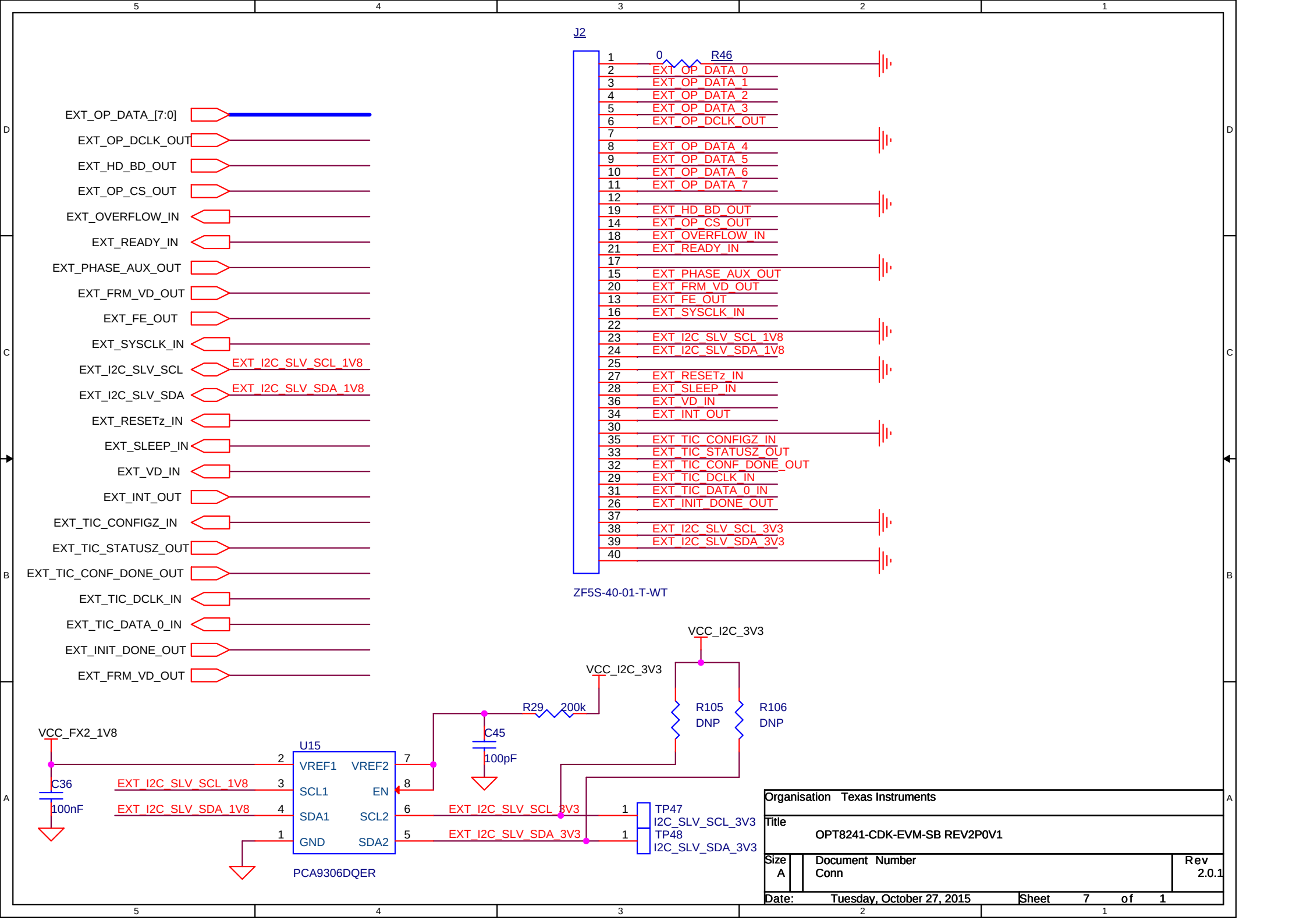
J2
1 0 R46
2 EXT_OP_DATA_0
3 EXT_OP_DATA_1
4 EXT_OP_DATA_2
5 EXT_OP_DATA_3
6 EXT_OP_DCLK_OUT
7
8 EXT_OP_DATA_4
9 EXT_OP_DATA_5
10 EXT_OP_DATA_6
11 EXT_OP_DATA_7
12
19 EXT_HD_BD_OUT
14 EXT_OP_CS_OUT
18 EXT_OVERFLOW_IN
21 EXT_READY_IN
17
15 EXT_PHASE_AUX_OUT
20 EXT_FRM_VD_OUT
13 EXT_FE_OUT
16 EXT_SYSCLK_IN
22
23 EXT_I2C_SLV_SCL_1V8
24 EXT_I2C_SLV_SDA_1V8
25
27 EXT_RESETz_IN
28 EXT_SLEEP_IN
36 EXT_VD_IN
34 EXT_INT_OUT
30
35 EXT_TIC_CONFIGZ_IN
33 EXT_TIC_STATUSZ_OUT
32 EXT_TIC_CONF_DONE_OUT
29 EXT_TIC_DCLK_IN
31 EXT_TIC_DATA_0_IN
26 EXT_INIT_DONE_OUT
37
38 EXT_I2C_SLV_SCL_3V3
39 EXT_I2C_SLV_SDA_3V3
40
ZF5S-40-01-T-WT
EXT_OP_DATA_[7:0]
EXT_OP_DCLK_OUT
EXT_HD_BD_OUT
EXT_OP_CS_OUT
EXT_OVERFLOW_IN
EXT_READY_IN
EXT_PHASE_AUX_OUT
EXT_FRM_VD_OUT
EXT_FE_OUT
EXT_SYSCLK_IN
EXT_I2C_SLV_SCL
EXT_I2C_SLV_SCL_1V8
EXT_I2C_SLV_SDA
EXT_I2C_SLV_SDA_1V8
EXT_RESETz_IN
EXT_SLEEP_IN
EXT_VD_IN
EXT_INT_OUT
EXT_TIC_CONFIGZ_IN
EXT_TIC_STATUSZ_OUT
EXT_TIC_CONF_DONE_OUT
EXT_TIC_DCLK_IN
EXT_TIC_DATA_0_IN
EXT_INIT_DONE_OUT
EXT_FRM_VD_OUT
VCC_I2C_3V3
VCC_I2C_3V3
R29 200k
R105 DNP
R106 DNP
C45 100pF
VCC_FX2_1V8
U15
2 VREF1 VREF2 7
3 SCL1 EN 8
4 SDA1 SCL2 6
1 GND SDA2 5
C36 100nF
EXT_I2C_SLV_SCL_1V8
EXT_I2C_SLV_SDA_1V8
EXT_I2C_SLV_SCL_3V3
EXT_I2C_SLV_SDA_3V3
1 TP47 I2C_SLV_SCL_3V3
1 TP48 I2C_SLV_SDA_3V3
PCA9306DQER
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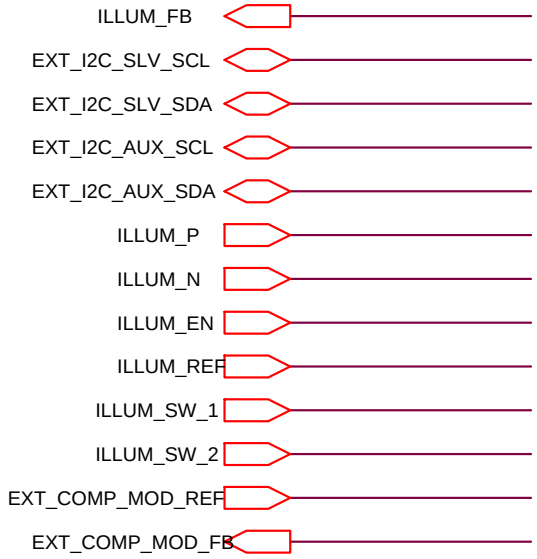
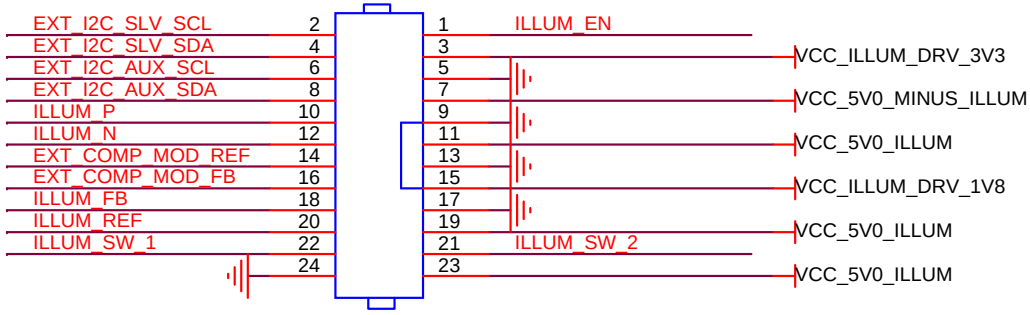


3V3 and 1V8 powered from main power supply
to ensure power to EEPROMs etc if illum supply cuts off.
Use judiciously.



SHF-112-01-L-D-RA
Connector cable assembly: FFSD-12-D-02.00-01-N

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I2C_SLV_SCL
I2C_SLV_SDA

FX2_CLK
FX2_ADDR_[1:0]
FX2_DQ_[7:0]
FX2_WRz

FX2_PKTEND
FX2_FLAG_[1:0]

SYSCLK_IN
SLEEP

INT
INT_PMIC

RESETz

TFC_SYSCLK_IN
TFC_SLEEP_IN
TFC_RESETz_IN
TFC_INT_OUT
TFC_DQ_OUT_[7:0]
TFC_OP_DCLK_OUT

TFC_OVERFLOW_IN
TFC_READY_IN
TFC_FE_OUT
TFC_OP_CS_OUT
TFC_PHASE_AUX_OUT
TFC_HD_BD_OUT

TFC_FRM_VD_OUT

U8-1

INT_PMIC G5
TFC_INT_OUT G2
INT_PMIC
INT_OUT

I2C_SLV_SCL F1
I2C_SLV_SDA F2
I2C_SLV_SCL
I2C_SLV_SDA

DEBUG D1 QPORT

SYSCLK_IN E1 TFC_SYSCLK_IN

SLEEP B1 TFC_SLEEP_IN
RESETZ C2 TFC_RESETZ_SW

F3 RSVD1
G1 RSVD2

OPT9221

VCC_TFC_IOVDD_1V8

R65 10k

Layout:
Match data and control line lengths to within 200mils.

U8-2

TFC_OP_DCLK_OUT K5
OP_CLK

TFC_DQ_OUT_7 L4
TFC_DQ_OUT_6 L2
TFC_DQ_OUT_5 L1
TFC_DQ_OUT_4 N2
TFC_DQ_OUT_3 N1
TFC_DQ_OUT_2 P2
TFC_DQ_OUT_1 P1
TFC_DQ_OUT_0 R1
OP_DATA_7
OP_DATA_6
OP_DATA_5
OP_DATA_4
OP_DATA_3
OP_DATA_2
OP_DATA_1
OP_DATA_0

OVERFLOW L3 TFC_OVERFLOW_IN
READY M1 TFC_READY_IN
FE L6 TFC_FE_OUT
OP_CS K6 TFC_OP_CS_OUT
PHASE_AUX K2 TFC_PHASE_AUX_OUT
VD K1 TFC_FRM_VD_OUT
HD/BD J2 TFC_HD_BD_OUT
RSVD3 J1
RSVD_IN1 M2

OPT9221

R66 10k
TFC_RESETZ_SW R22 10k TFC_RESETz_IN

C28 1uF

Layout:
Place Switch next to board edge on top side for
easy accessibility. It should not be under the Illumination board.

Layout:
Place all 0 ohm resistors close to each other.
They should not be covered by illumination board on top side.
Bottom side is also ok.

Layout:
Match all wires to expansion connector to 100 mils.
Exceptions: RESETz, I2C

TP34 1 TFC_OP_DCLK_OUT — TFC_OP_DCLK_OUT — R75 0 — FX2_CLK
TP24 1 TFC_OVERFLOW_IN — TFC_OVERFLOW_IN — R77 0 — FX2_FLAG_1
TP19 1 TFC_READY_IN — TFC_READY_IN — R68 0 — FX2_FLAG_0
TP33 1 TFC_FE_OUT — TFC_FE_OUT — R85 0 — FX2_PKTEND
TP28 1 TFC_OP_CS_OUT — TFC_OP_CS_OUT — R84 0 — FX2_ADDR_1
TP27 1 TFC_PHASE_AUX_OUT — TFC_PHASE_AUX_OUT — R82 0 — FX2_ADDR_0
TP31 1 TFC_HD_BD_OUT — TFC_HD_BD_OUT — R81 0 — FX2_WRz
TP69 1 TFC_FRM_VD_OUT — TFC_FRM_VD_OUT

FX2_DQ_7 — R69 0 — TFC_DQ_OUT_7
FX2_DQ_6 — R79 0 — TFC_DQ_OUT_6
FX2_DQ_5 — R70 0 — TFC_DQ_OUT_5
FX2_DQ_4 — R71 0 — TFC_DQ_OUT_4
FX2_DQ_3 — R72 0 — TFC_DQ_OUT_3
FX2_DQ_2 — R73 0 — TFC_DQ_OUT_2
FX2_DQ_1 — R83 0 — TFC_DQ_OUT_1
FX2_DQ_0 — R74 0 — TFC_DQ_OUT_0

TP32 1 TFC_SYSCLK_IN — TFC_SYSCLK_IN — R88 0 — SYSCLK_IN
TP30 1 TFC_SLEEP_IN — R87 0 — SLEEP
TFC_RESETz_IN — R89 0 — RESETz
TFC_INT_OUT — R78 0 — INT

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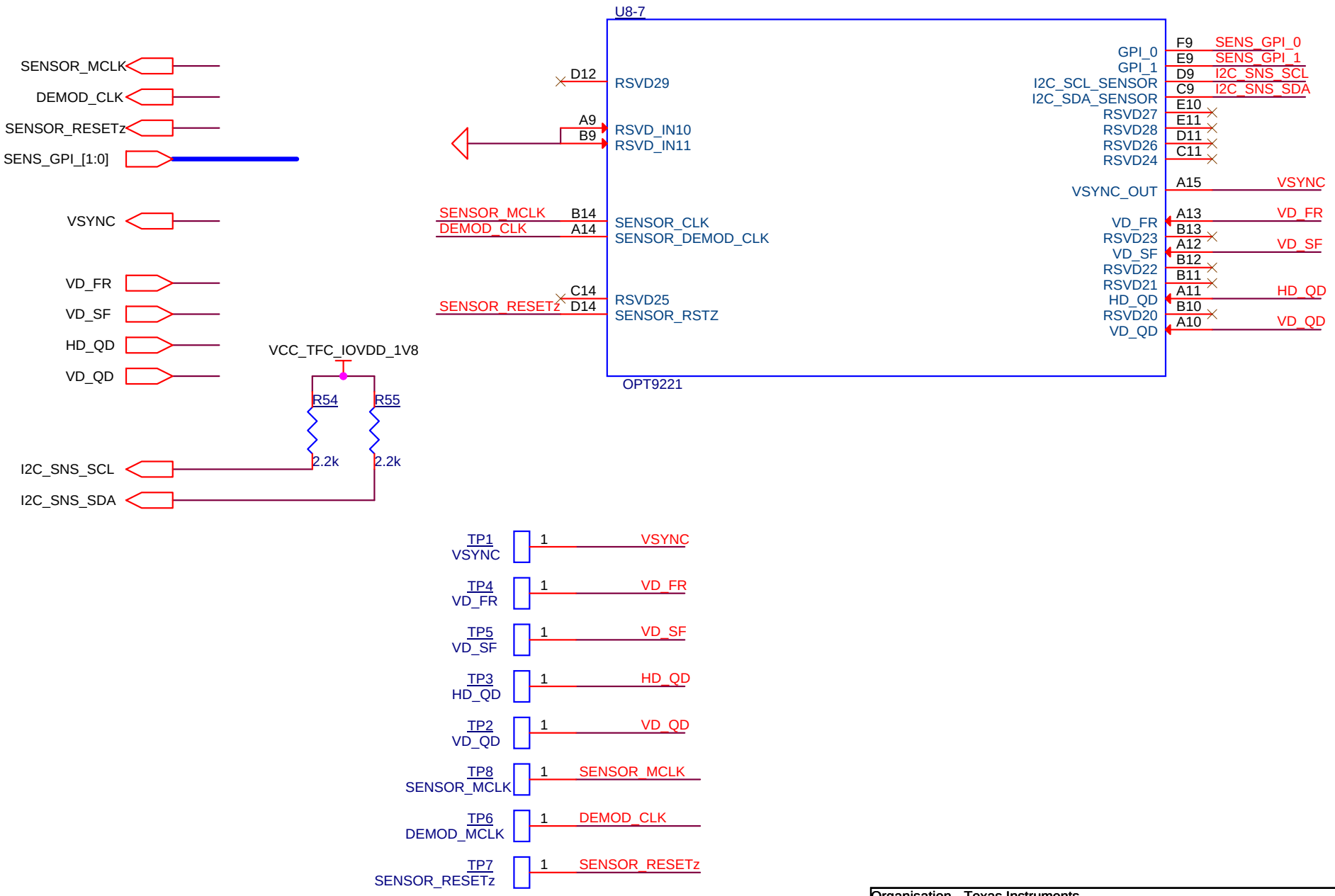

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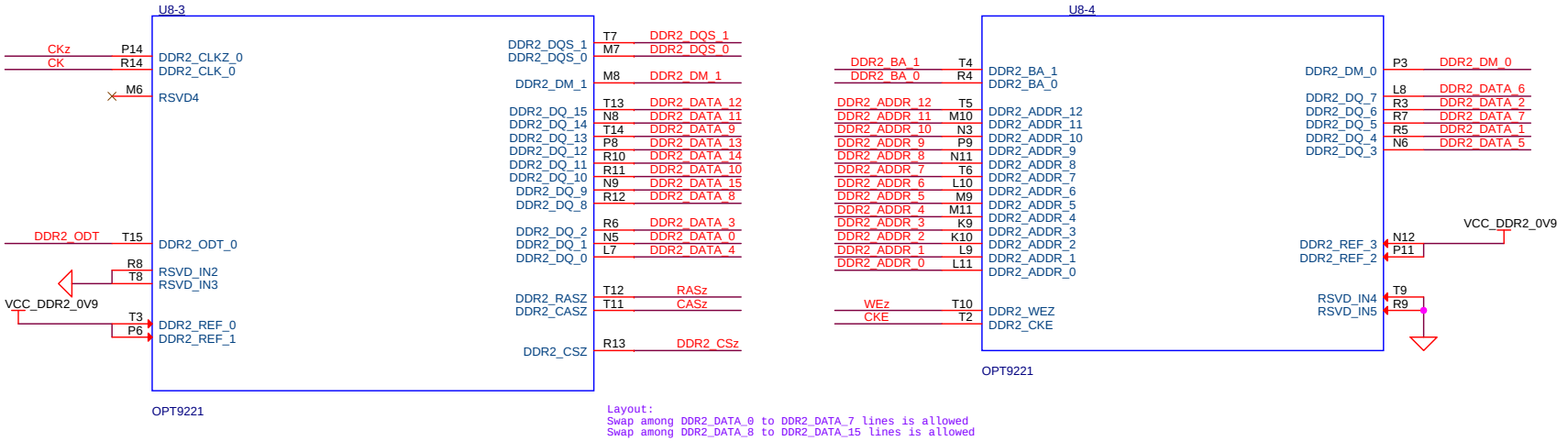
DDR2_DATA_[15:0]
DDR2_DM_[1:0]
DDR2_DQS_[1:0]

DDR2_BA_[1:0]
DDR2_ADDR_[12:0]

CK
CKz
CKE

RASz
CASz
WEz

DDR2_ODT
DDR2_CSz



Layout:
Swap among DDR2_DATA_0 to DDR2_DATA_7 lines is allowed
Swap among DDR2_DATA_8 to DDR2_DATA_15 lines is allowed

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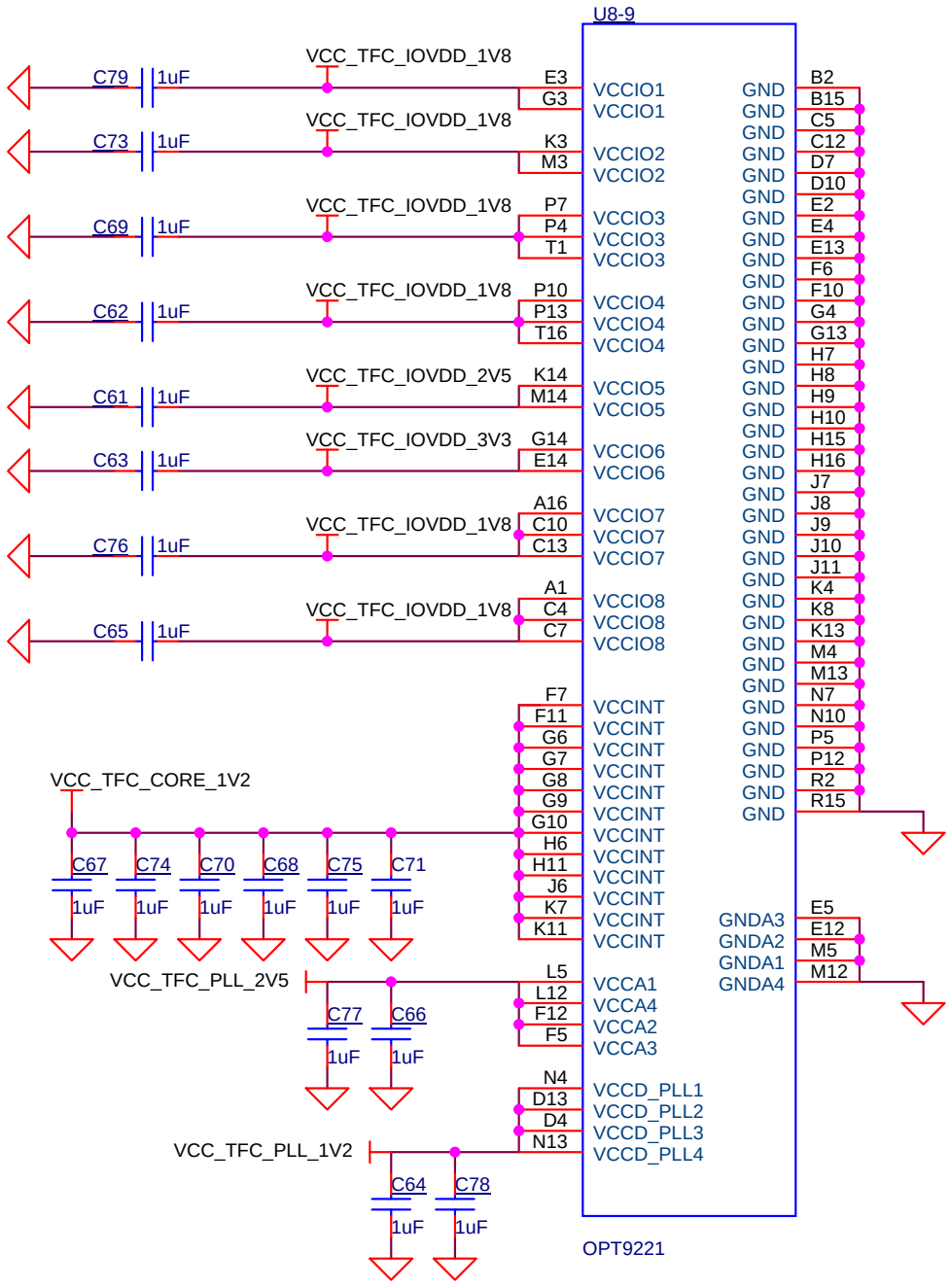

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Title	OPT8241-CDK-EVM-SB REV2P0V1	
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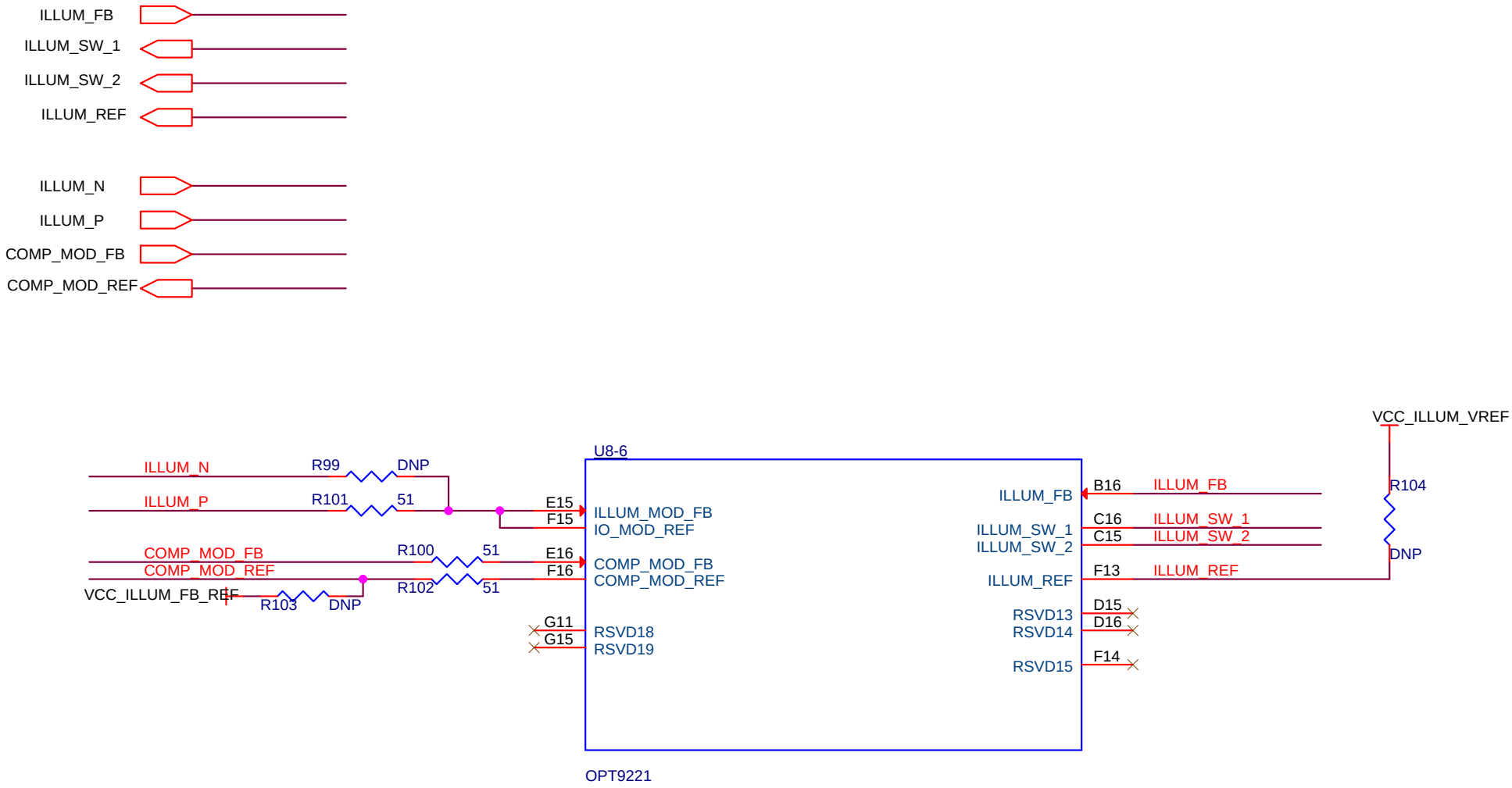

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Size: A	Document Number: TFC/Illum	Rev: 2.0.1
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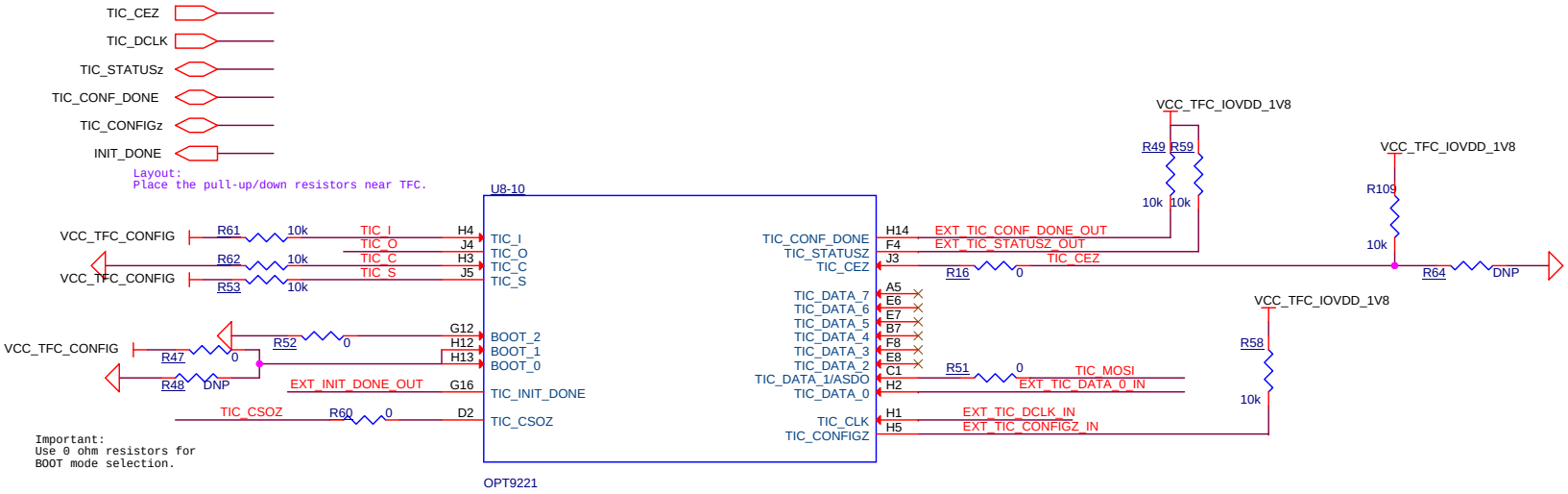

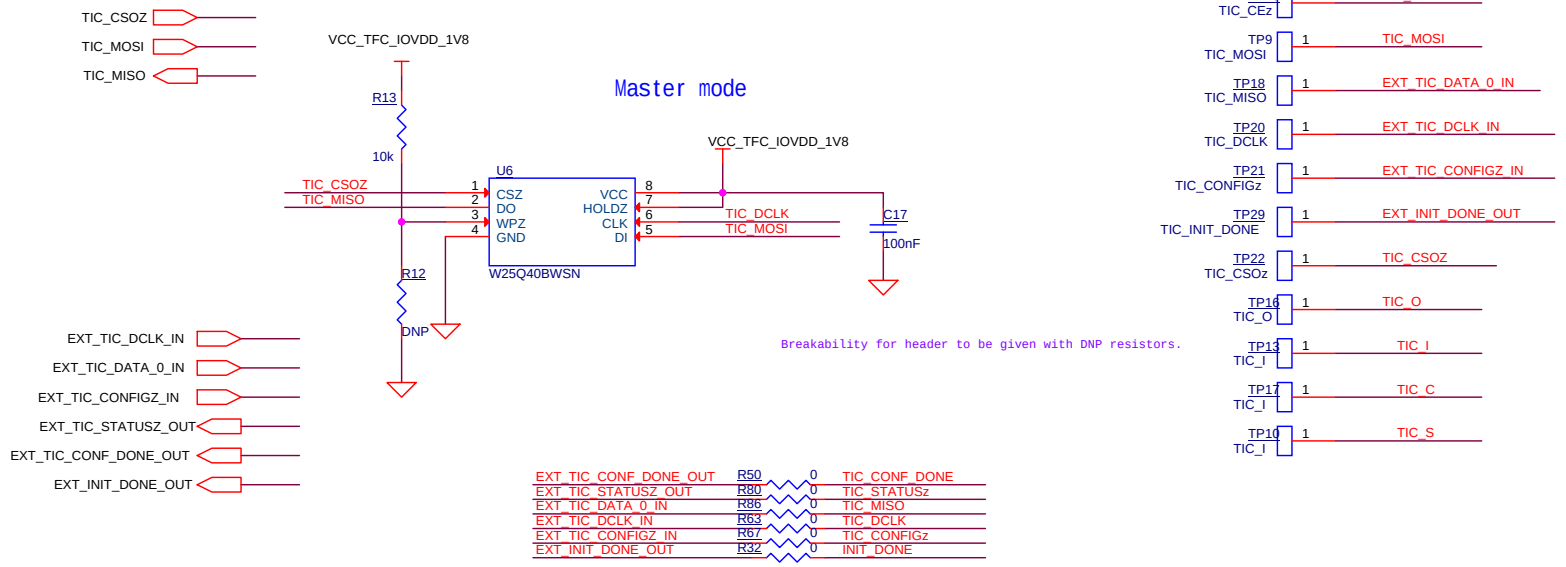

Organisation Texas Instruments		
Title OPT8241-CDK-EVM-SB REV2P0V1		
Size B	Document Number TFC/Config	Rev 2.0.1
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CAP_BIT_CLK_[1:0]

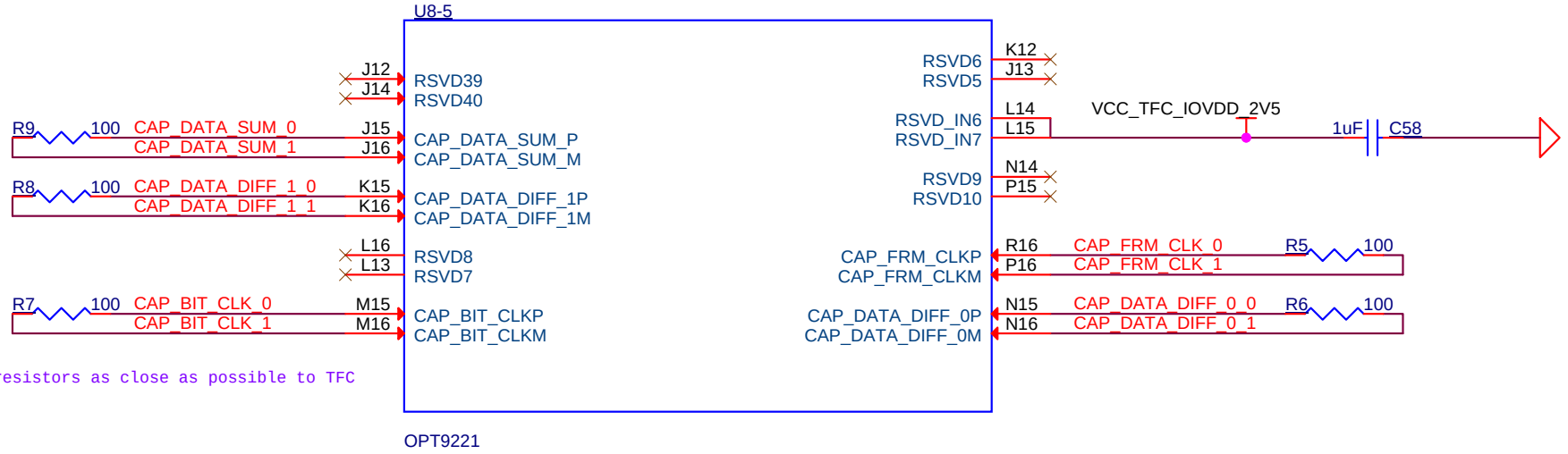
CAP_FRM_CLK_[1:0]

CAP_DATA_DIFF_0_[1:0]

CAP_DATA_DIFF_1_[1:0]

CAP_DATA_SUM_[1:0]

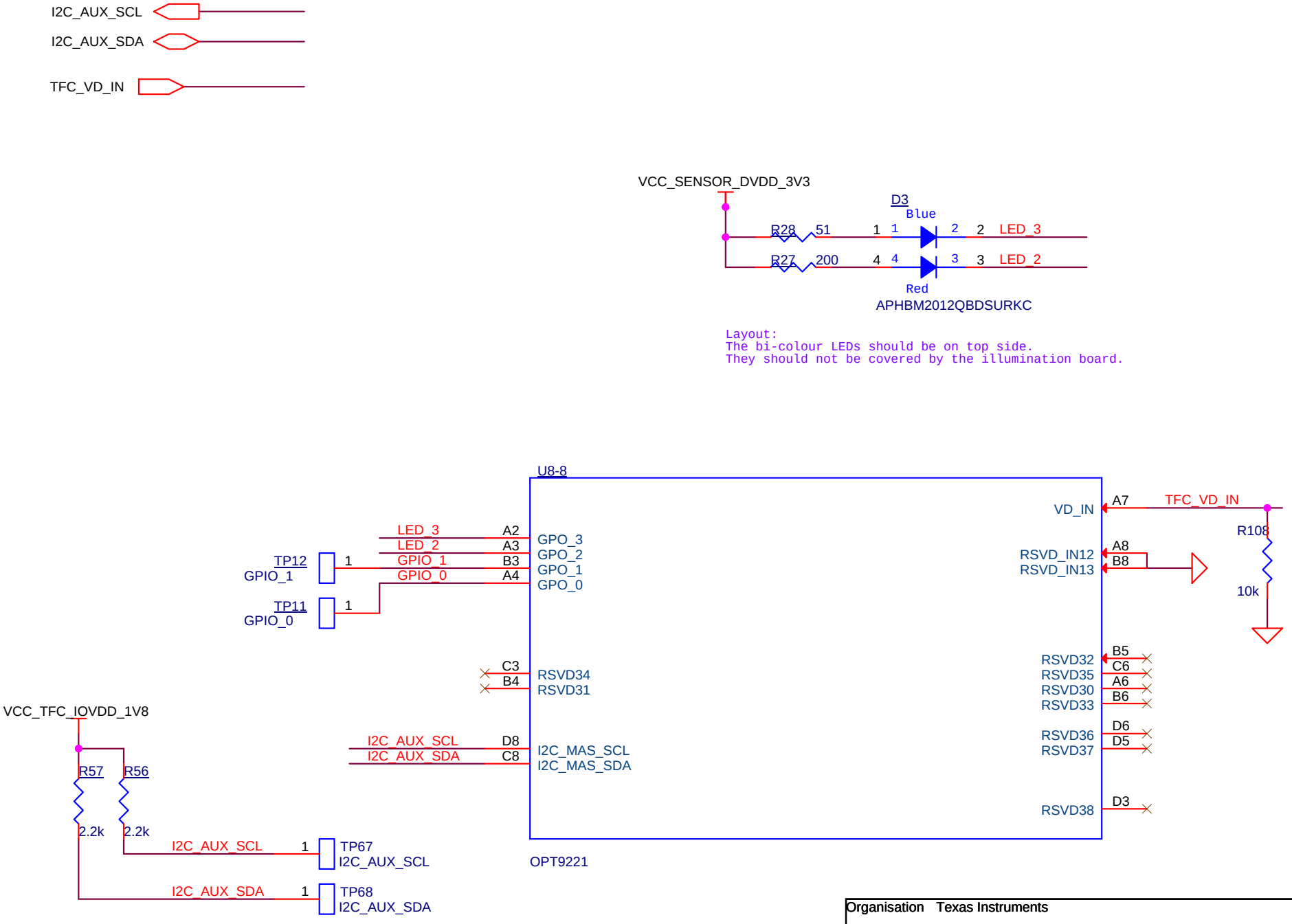
Layout:
Length match all the CAP differential LVDS signals
within 50 mils of each other.



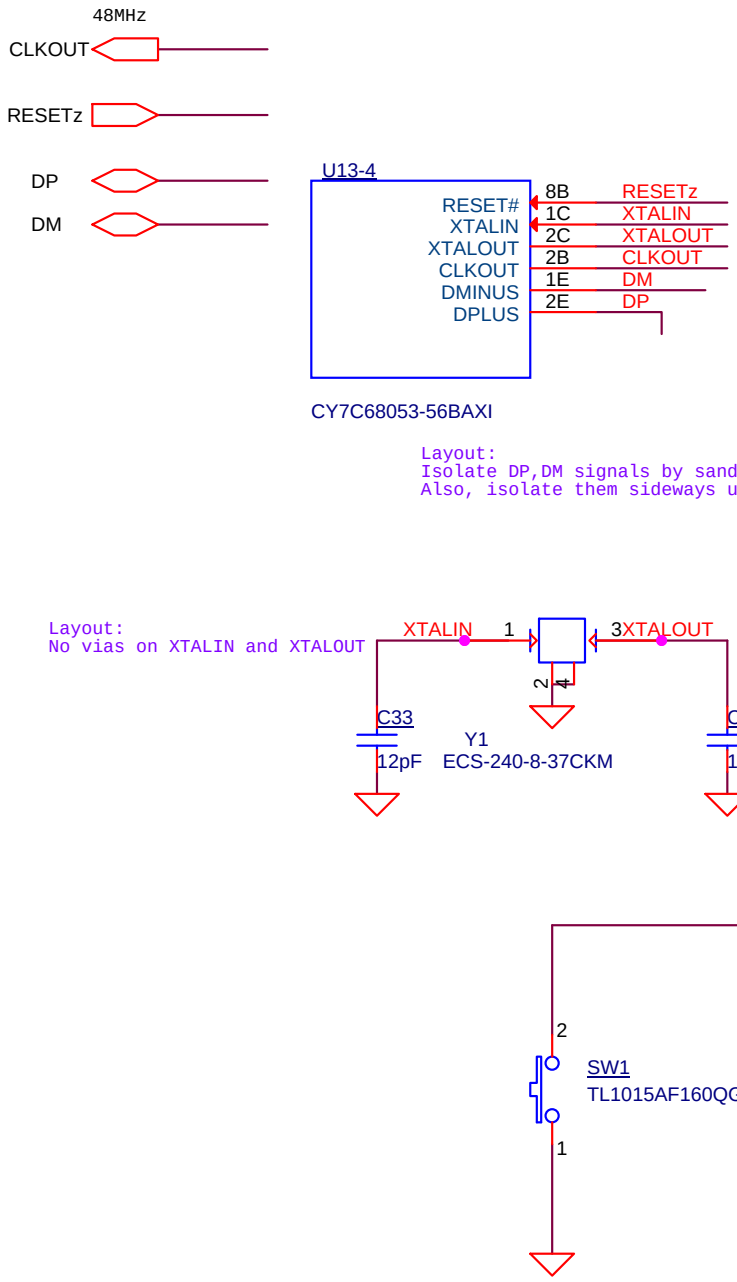
Layout:
Keep the 100ohm resistors as close as possible to TFC

Layout:
Place the diif pair test points close to the 100 ohm termination resistors, TFC pins or sensor pins.
Use existing vias. Test points for each diff pair should be separated by 100 mil for differential probe.

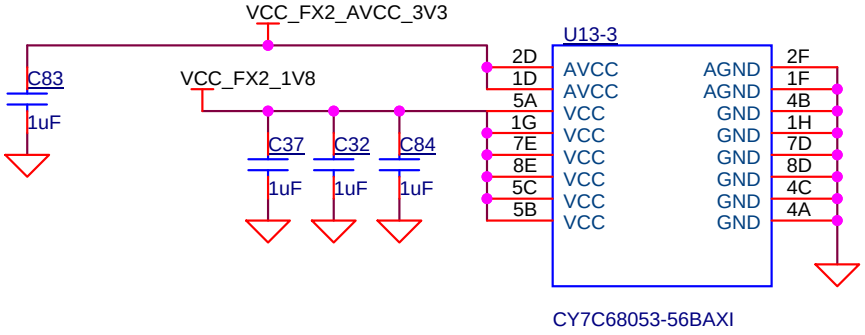
Organisation	Texas Instruments	
Title	OPT8241-CDK-EVM-SB REV2P0V1	
Size: A	Document Number: TFC/Capture	Rev: 2.0.1
Date: Tuesday, October 27, 2015	Sheet 15 of 22	



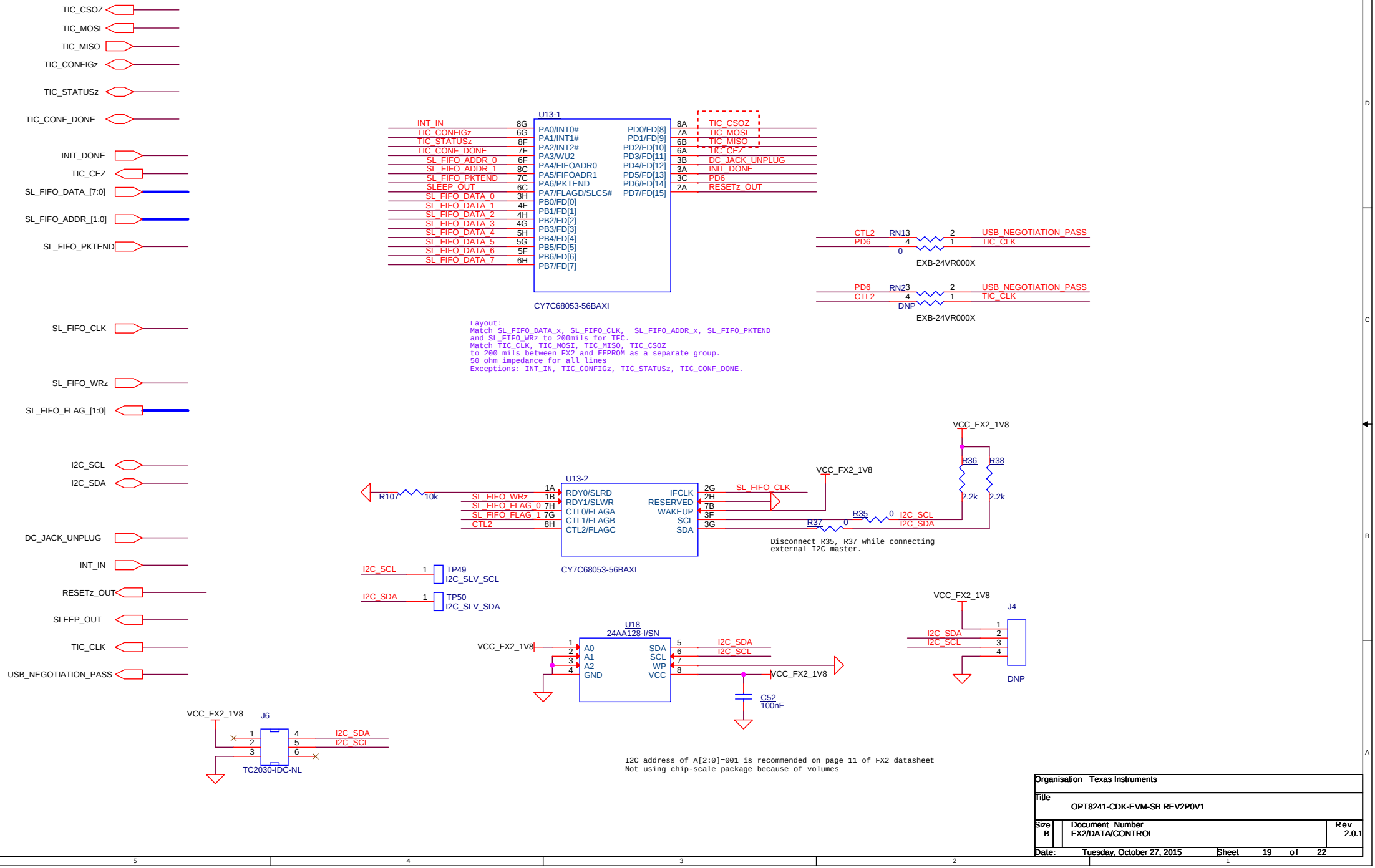
Organisation	Texas Instruments		
Title	OPT8241-CDK-EVM-SB REV2P0V1		
Size A	Document Number TFC/ADC		Rev 2.0.1
Date: Tuesday, October 27, 2015		Sheet 16 of 22	



Organisation	Texas Instruments	
Title	OPT8241-CDK-EVM-SB REV2P0V1	
Size: A	Document Number: FX2/BUS	Rev: 2.0.1
Date: Tuesday, October 27, 2015	Sheet 17 of 22	



Organisation Texas Instruments			
Title OPT8241-CDK-EVM-SB REV2P0V1			
Size A		Document Number FX2/Power	Rev 2.0.1
Date: Tuesday, October 27, 2015		Sheet 18 of 22	



Organisation	Texas Instruments
Title	OPT8241-CDK-EVM-SB REV2P0V1
Size	B
Document Number	FX2/DATA/CONTROL
Rev	2.0.1
Date:	Tuesday, October 27, 2015
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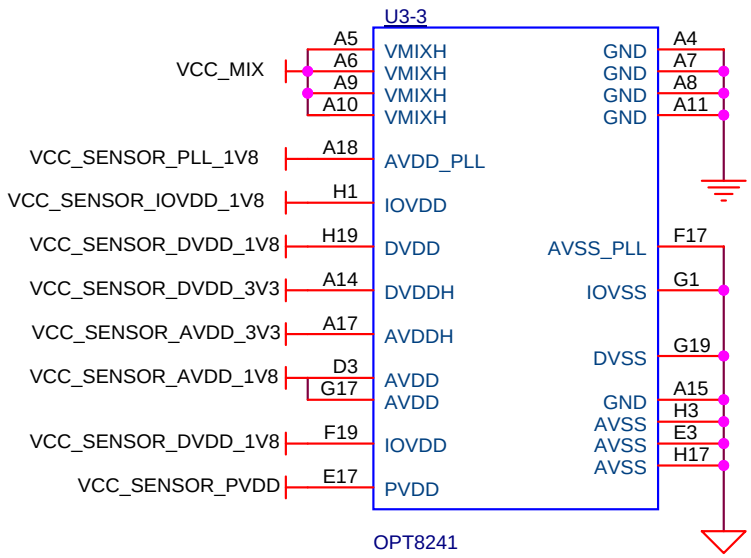
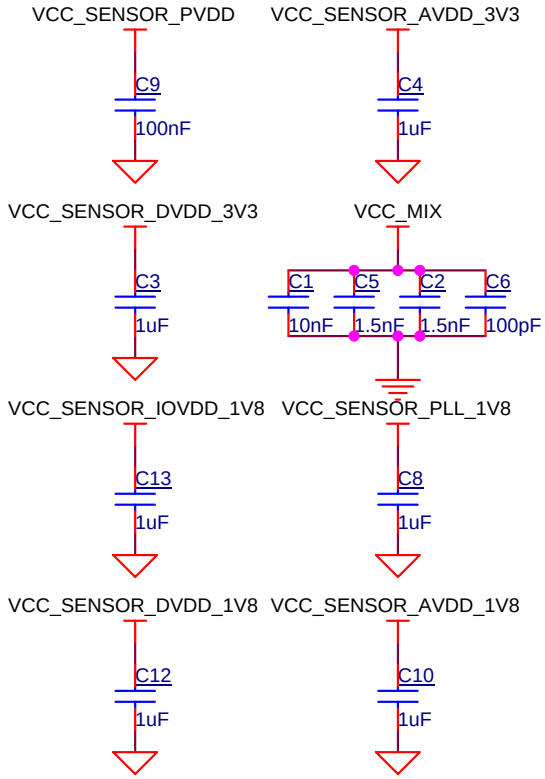
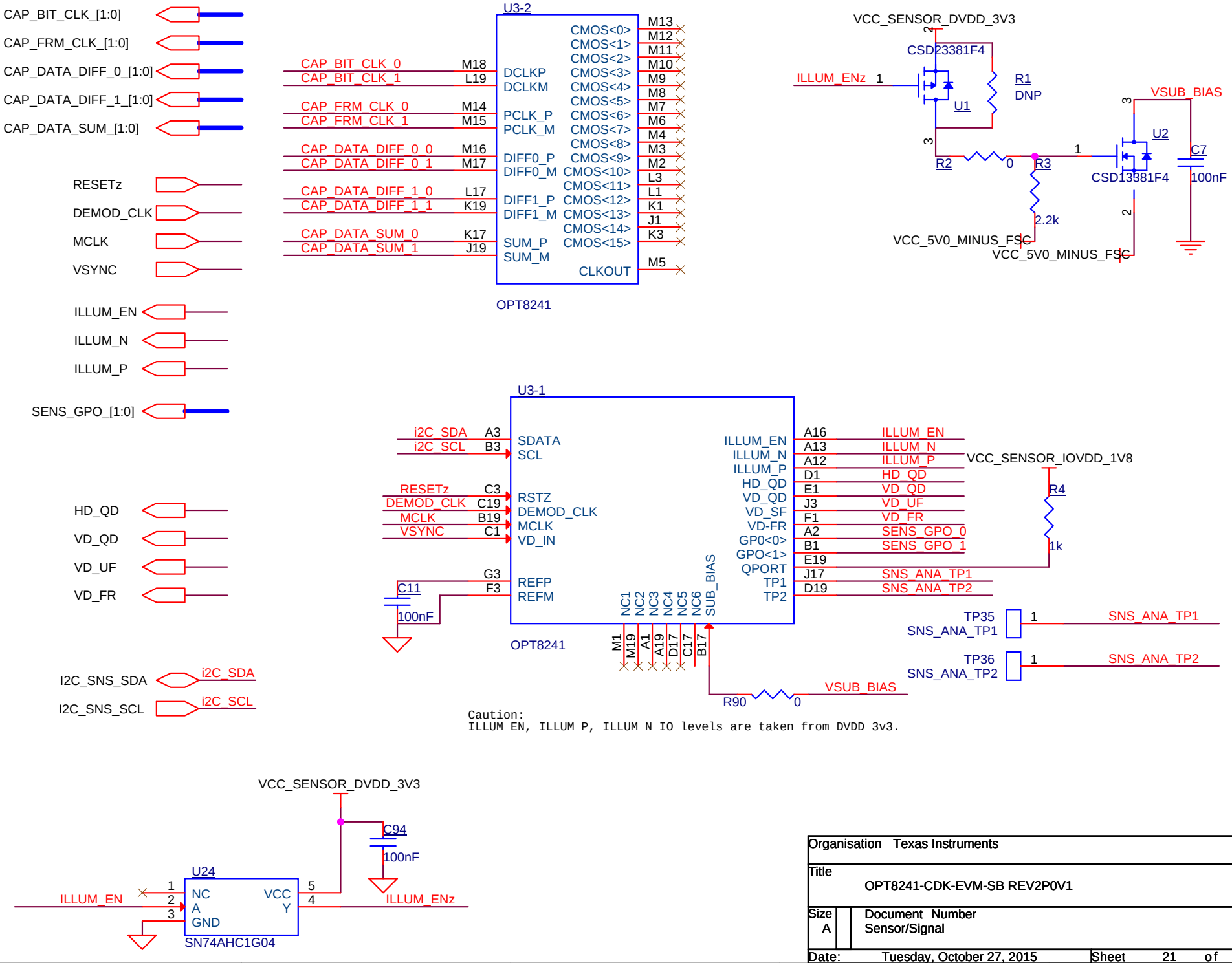
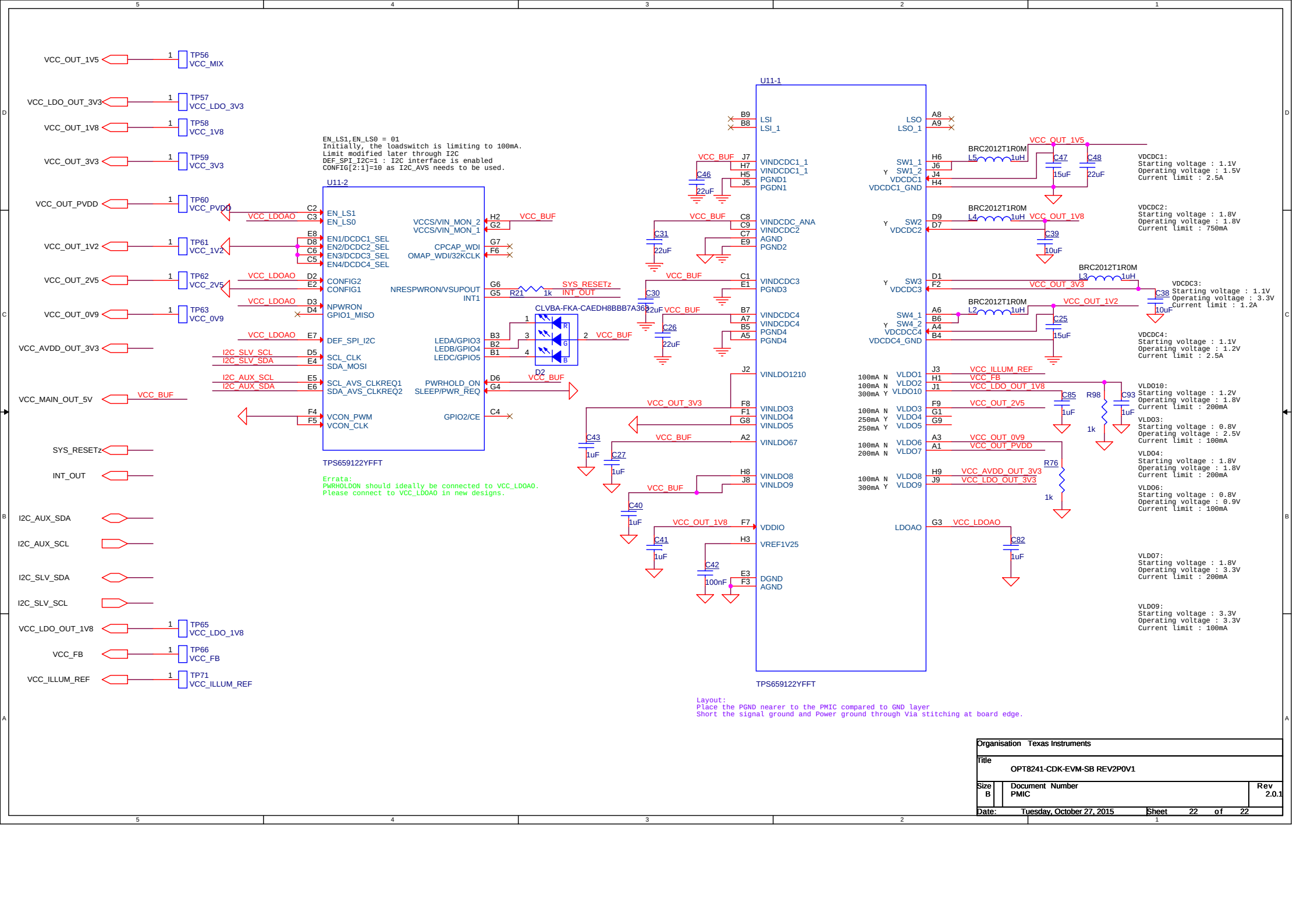




Organisation Texas Instruments		
Title OPT8241-CDK-EVM-SB REV2P0V1		
Size A	Document Number Sensor/Power	Rev 2.0.1
Date: Tuesday, October 27, 2015	Sheet 20 of 22	



Organisation	Texas Instruments		
Title	OPT8241-CDK-EVM-SB REV2P0V1		
Size A	Document Number Sensor/Signal		Rev 2.0.1
Date:	Tuesday, October 27, 2015	Sheet 21 of 22	


VCC_OUT_1V5
TP56 VCC_MIX
VCC_LDO_OUT_3V3
TP57 VCC_LDO_3V3
VCC_OUT_1V8
TP58 VCC_1V8
VCC_OUT_3V3
TP59 VCC_3V3
VCC_OUT_PVDD
TP60 VCC_PVDD
VCC_OUT_1V2
TP61 VCC_1V2
VCC_OUT_2V5
TP62 VCC_2V5
VCC_OUT_0V9
TP63 VCC_0V9
VCC_AVDD_OUT_3V3
VCC_MAIN_OUT_5V
VCC_BUF
SYS_RESETz
INT_OUT
I2C_AUX_SDA
I2C_AUX_SCL
I2C_SLV_SDA
I2C_SLV_SCL
VCC_LDO_OUT_1V8
TP65 VCC_LDO_1V8
VCC_FB
TP66 VCC_FB
VCC_ILLUM_REF
TP71 VCC_ILLUM_REF
EN_LS1,EN_LS0 = 01
Initially, the loadswitch is limiting to 100mA.
Limit modified later through I2C
DEF_SPI_I2C=1 : I2C interface is enabled
CONFIG[2:1]=10 as I2C_AVS needs to be used.
U11-2
EN_LS1
EN_LS0
EN1/DCDC1_SEL
EN2/DCDC2_SEL
EN3/DCDC3_SEL
EN4/DCDC4_SEL
CONFIG2
CONFIG1
NPWRON
GPIO1_MISO
DEF_SPI_I2C
SCL_CLK
SDA_MOSI
SCL_AVS_CLKREQ1
SDA_AVS_CLKREQ2
VCON_PWM
VCON_CLK
VCCS/VIN_MON_2
VCCS/VIN_MON_1
CPCAP_WDI
OMAP_WDI/32KCLK
NRESPWRON/VSUPOUT
INT1
LEDA/GPIO3
LEDB/GPIO4
LEDC/GPIO5
PWRHOLD_ON
SLEEP/PWR_REQ
GPIO2/CE
TPS659122YFFT
Errata:
PWRHOLDON should ideally be connected to VCC_LDOAO.
Please connect to VCC_LDOAO in new designs.
R21 1k
SYS_RESETz
INT_OUT
CLVBA-FKA-CAEDH8BBB7A363
D2
U11-1
LSI
LSI_1
VINDCDC1_1
VINDCDC1_1
PGND1
PGND1
VINDCDC_ANA
VINDCDC2
AGND
PGND2
VINDCDC3
PGND3
VINDCDC4
VINDCDC4
PGND4
PGND4
VINLDO1210
VINLDO3
VINLDO4
VINLDO5
VINLDO67
VINLDO8
VINLDO9
VDDIO
VREF1V25
DGND
AGND
LSO
LSO_1
SW1_1
SW1_2
VDCDC1
VDCDC1_GND
SW2
VDCDC2
SW3
VDCDC3
SW4_1
SW4_2
VDCDC4
VDCDC4_GND
VLDO1
VLDO2
VLDO10
VLDO3
VLDO4
VLDO5
VLDO6
VLDO7
VLDO8
VLDO9
LDOAO
TPS659122YFFT
BRC2012T1R0M
1uH
VCC_OUT_1V5
VCC_OUT_1V8
VCC_OUT_3V3
VCC_OUT_1V2
VCC_ILLUM_REF
VCC_FB
VCC_OUT_2V5
VCC_OUT_0V9
VCC_OUT_PVDD
VCC_AVDD_OUT_3V3
VCC_LDO_OUT_3V3
VCC_LDOAO
R76 1k
R98 1k
VDCDC1:
Starting voltage : 1.1V
Operating voltage : 1.5V
Current limit : 2.5A
VDCDC2:
Starting voltage : 1.8V
Operating voltage : 1.8V
Current limit : 750mA
VDCDC3:
Starting voltage : 1.1V
Operating voltage : 3.3V
Current limit : 1.2A
VDCDC4:
Starting voltage : 1.1V
Operating voltage : 1.2V
Current limit : 2.5A
VLDO10:
Starting voltage : 1.2V
Operating voltage : 1.8V
Current limit : 200mA
VLDO3:
Starting voltage : 0.8V
Operating voltage : 2.5V
Current limit : 100mA
VLDO4:
Starting voltage : 1.8V
Operating voltage : 1.8V
Current limit : 200mA
VLDO6:
Starting voltage : 0.8V
Operating voltage : 0.9V
Current limit : 100mA
VLDO7:
Starting voltage : 1.8V
Operating voltage : 3.3V
Current limit : 200mA
VLDO9:
Starting voltage : 3.3V
Operating voltage : 3.3V
Current limit : 100mA
Layout:
Place the PGND nearer to the PMIC compared to GND layer
Short the signal ground and Power ground through Via stitching at board edge.
Organisation Texas Instruments
Title
OPT8241-CDK-EVM-SB REV2P0V1
Size B
Document Number
PMIC
Rev 2.0.1
Date: Tuesday, October 27, 2015
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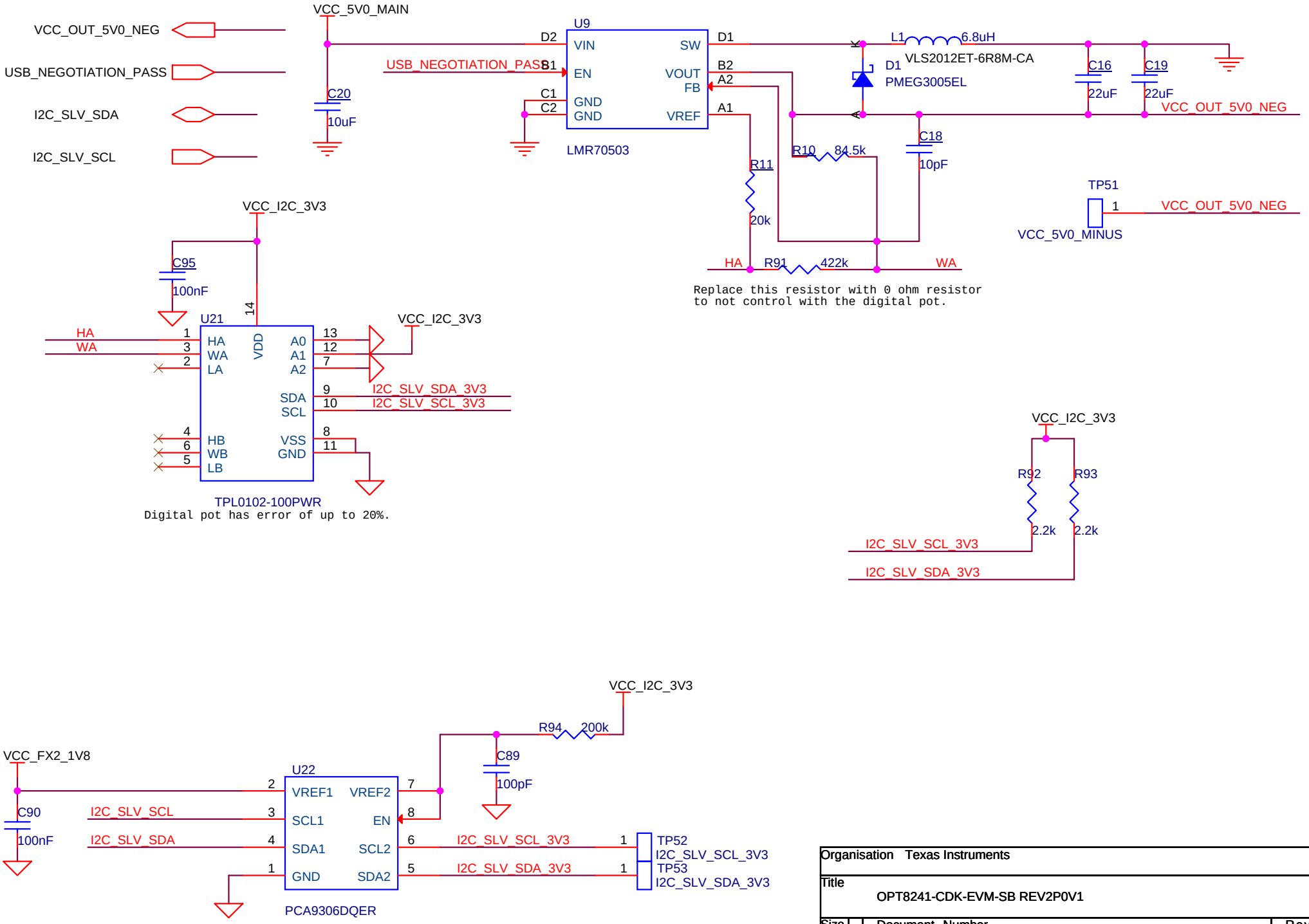
VCC_OUT_5V0_NEG
USB_NEGOTIATION_PASS
I2C_SLV_SDA
I2C_SLV_SCL
VCC_5V0_MAIN
C20
10uF
U9
VIN
EN
GND
GND
SW
VOUT
FB
VREF
D2
B1
C1
C2
D1
B2
A2
A1
LMR70503
L1
6.8uH
VLS2012ET-6R8M-CA
D1
PMEG3005EL
C16
22uF
C19
22uF
VCC_OUT_5V0_NEG
C18
10pF
R10
84.5k
R11
20k
HA
R91
422k
WA
Replace this resistor with 0 ohm resistor
to not control with the digital pot.
TP51
1
VCC_OUT_5V0_NEG
VCC_5V0_MINUS
VCC_I2C_3V3
C95
100nF
U21
14
VDD
HA
WA
LA
HB
WB
LB
A0
A1
A2
SDA
SCL
VSS
GND
TPL0102-100PWR
Digital pot has error of up to 20%.
I2C_SLV_SDA_3V3
I2C_SLV_SCL_3V3
R92
R93
2.2k
2.2k
VCC_FX2_1V8
C90
100nF
U22
VREF1
SCL1
SDA1
GND
VREF2
EN
SCL2
SDA2
R94
200k
C89
100pF
I2C_SLV_SCL
I2C_SLV_SDA
TP52
TP53
PCA9306DQER
Organisation Texas Instruments
Title
OPT8241-CDK-EVM-SB REV2P0V1
Size
A
Document Number
Negative Voltage
Rev
2.0.1
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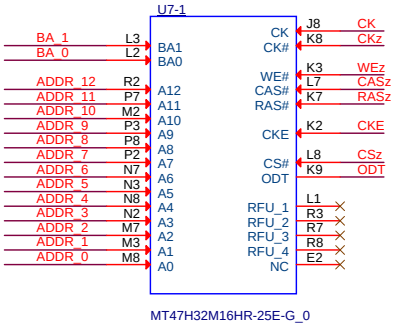
Sheet 23 of 22

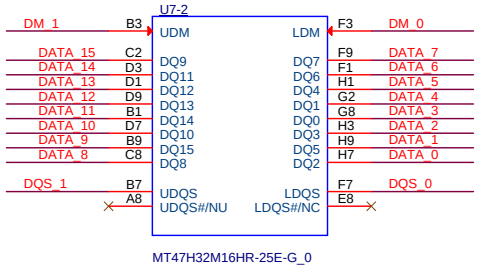
DATA_[15:0]
ADDR_[12:0]
BA_[1:0]
DQS_[1:0]
DM_[1:0]
RASz
CASz
WEz
CSz
CKE
CK
CKz
ODT

ADDRESSING/CONTROL



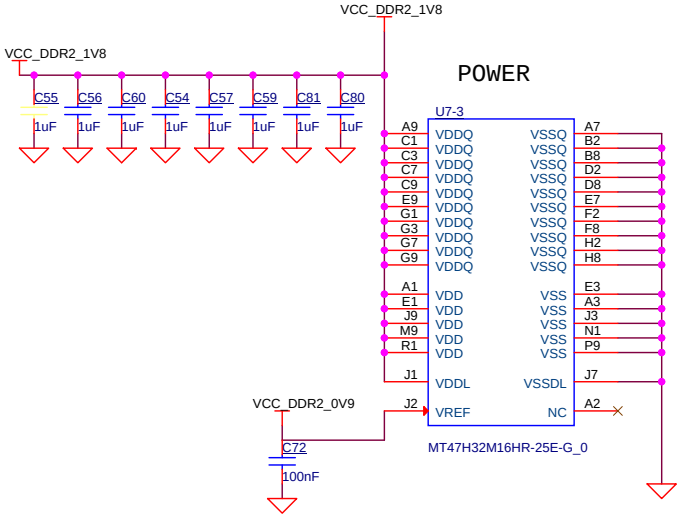
Layout:
100 mil matching between addr/control lines.
50 ohm impedance
Clock pair : 100 ohm differential impedance

DATA

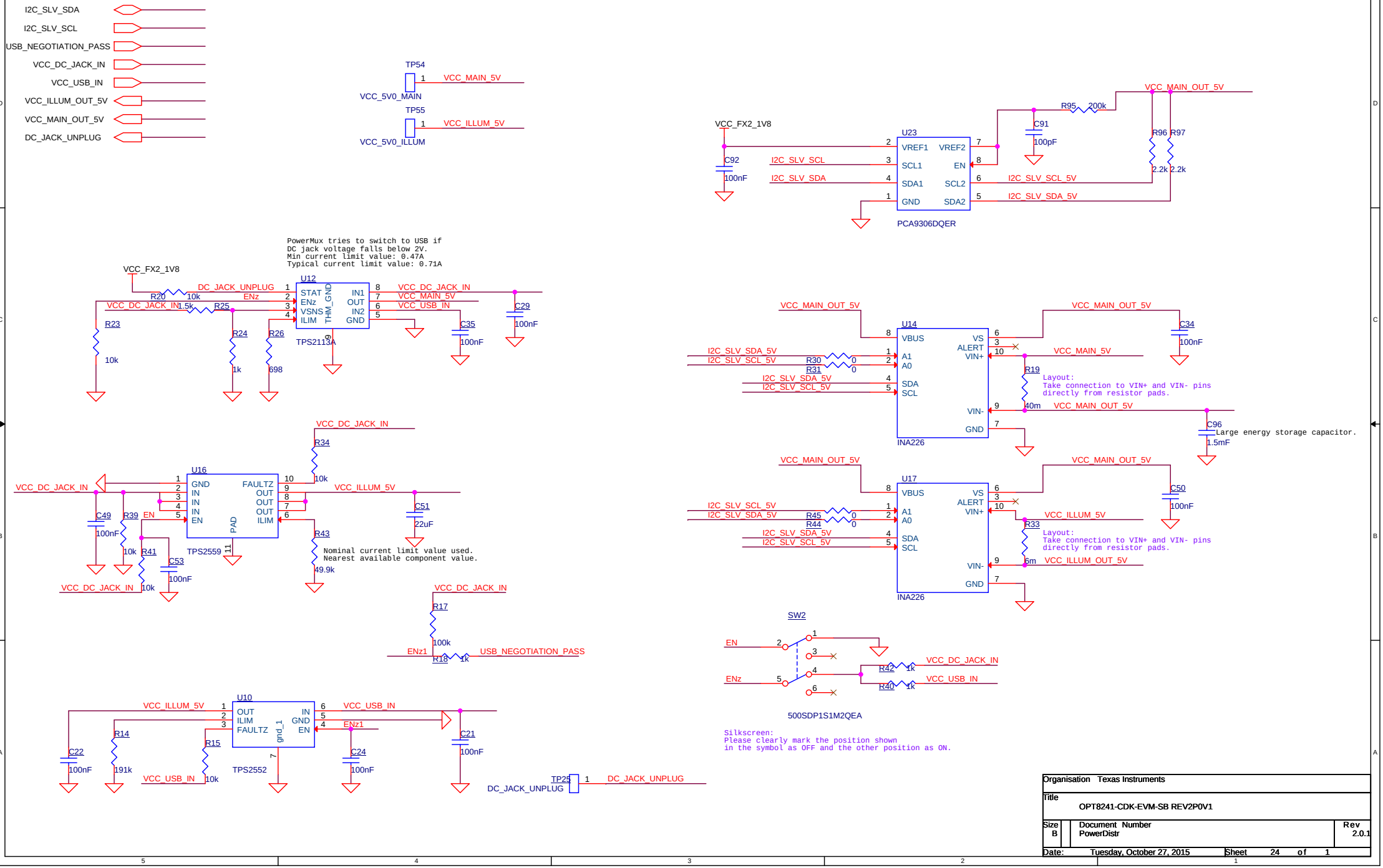


Layout:
50 mil matching between data lines.
50 ohm impedance

POWER



Organisation Texas Instruments			
Title OPT8241-CDK-EVM-SB REV2P0V1			
Size B	Document Number DDR2		Rev 2.0.1
Date: Tuesday, October 27, 2015	Sheet 24 of 22		



Organisation	Texas Instruments		
Title	OPT8241-CDK-EVM-SB REV2P0V1		
Size B	Document Number PowerDistr		Rev 2.0.1
Date: Tuesday, October 27, 2015	Sheet 24 of 1		