HT160A/HT120A

4/3-Type 16.78-mega pixel and 1.1-Type 12.58-mega pixel CMOS Image Sensor

The specifications are subject to change without notice.

General Description

The HT160A is a 4/3-type 16.78-mega pixel high resolution CMOS image sensor, the frame rate is up to 46.8fps at full resolution of 4096 (H) x 4096 (V). The HT120A is a 1.1-type 12.58-mega pixel high resolution CMOS image sensor, the frame rate is up to 62.3fps at full resolution of 4096 (H) x 3072 (V). Both sensors are featured with global shutter pixels, high-resolution ADC and high-speed readout circuits. The sensors meet the high-performance and high-resolution requirements in applications such as intelligent traffic system, machine vision and high-resolution industrial inspection, etc.

Features

- Active pixel array
  - HT160A: 4112 (H) × 4112 (V)
    - 14.4mm (H) × 14.4 mm (V), 20.4mm (Diagonal)
  - HT120A: 4112 (H) × 3088 (V)
    - 14.4mm (H) × 10.8 mm (V), 18.0mm (Diagonal)
- Global shutter pixel
- Programmable analog gain and digital gain
- 14-bit ADC
- Master mode, Slave mode and TRIGEXP mode
- External electronic shutter control (only in TRIGEXP mode)
- Other functions
  - Multi-ROI windowing (V-direction only)
  - Vertical/Horizontal binning
  - Vertical/Horizontal sub-sampling

Specifications

Table 1. Sensor specifications

Parameters	Specifications
Image Format	HT160A: 4/3-Type, diagonal 20.4mm HT120A: 1.1-Type, diagonal 18.0mm
Number of Total Pixels	HT160A: 4336 (H) x 4184 (V) HT120A: 4336 (H) x 3160 (V)
Number of Active Pixels	HT160A: 4112 (H) x 4112 (V) HT120A: 4112 (H) x 3088 (V)
Pixel Size	3.5µm x 3.5µm
Pixel Type	Global shutter pixel
Sensitivity	T.B.D. (> 2V/lux·s)
Saturation (Linear)	T.B.D. (> 0.9V)
Dynamic Range	T.B.D.
Read noise (with Pixel)	T.B.D.
Windowing (ROI)	V-direction only with multi-ROI
ADC Resolution	14bit
Frame Rate	Maximum frame rate at full resolution HT160A: 46.8fps, HT120A: 62.3fps
LVDS Outputs	16/8/4 LVDS pairs
Data Rate	Max. 1039.5 Mbps/pair
Power Supply	1.2V/1.8V/3.3V
Power Consumption	T.B.D
Chroma	Mono and Color
Type of Package	230-pin CLGA

Applications

- Intelligent traffic system
- Machine vision
- Industrial inspection

Contents

Block Diagram

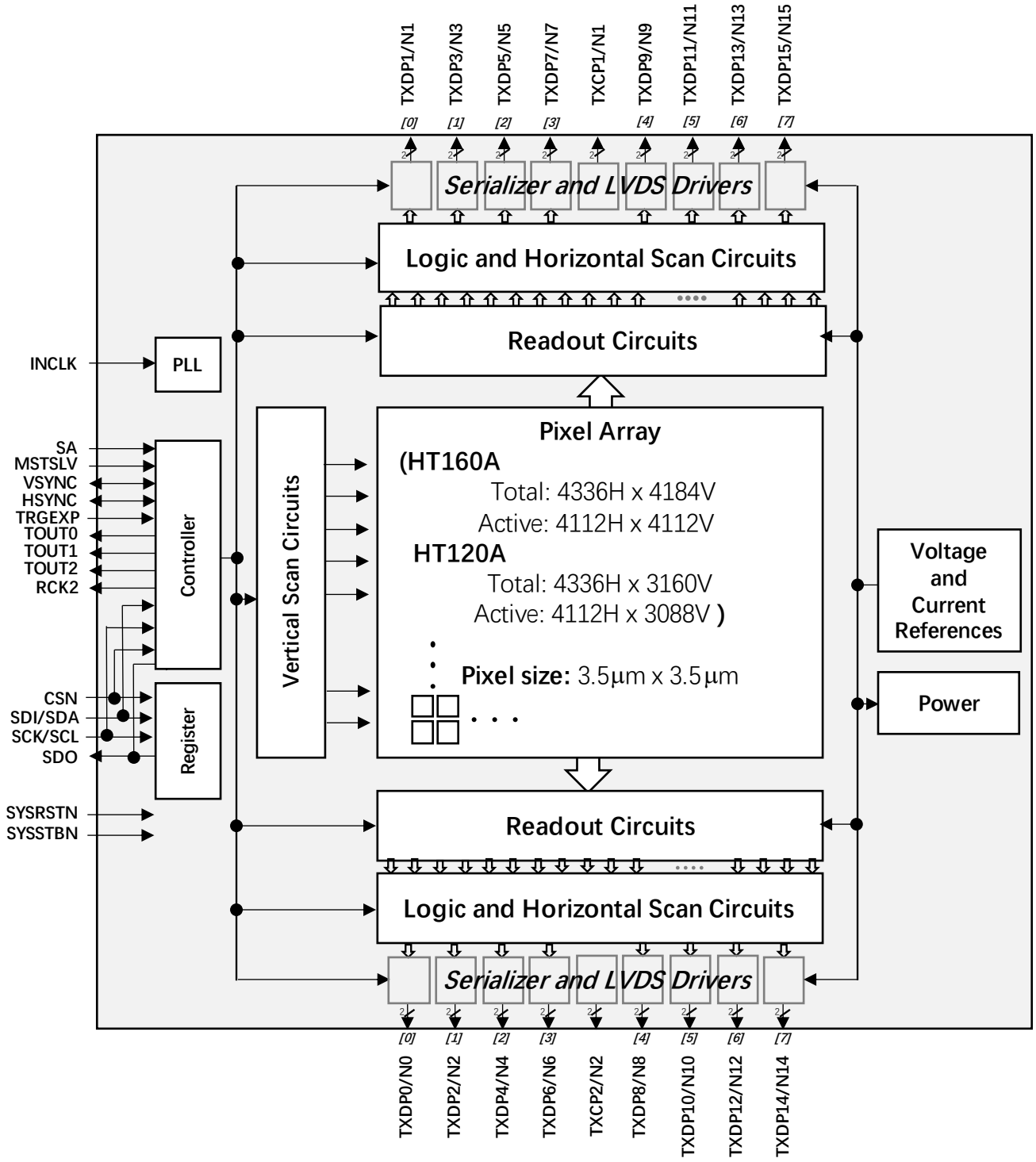
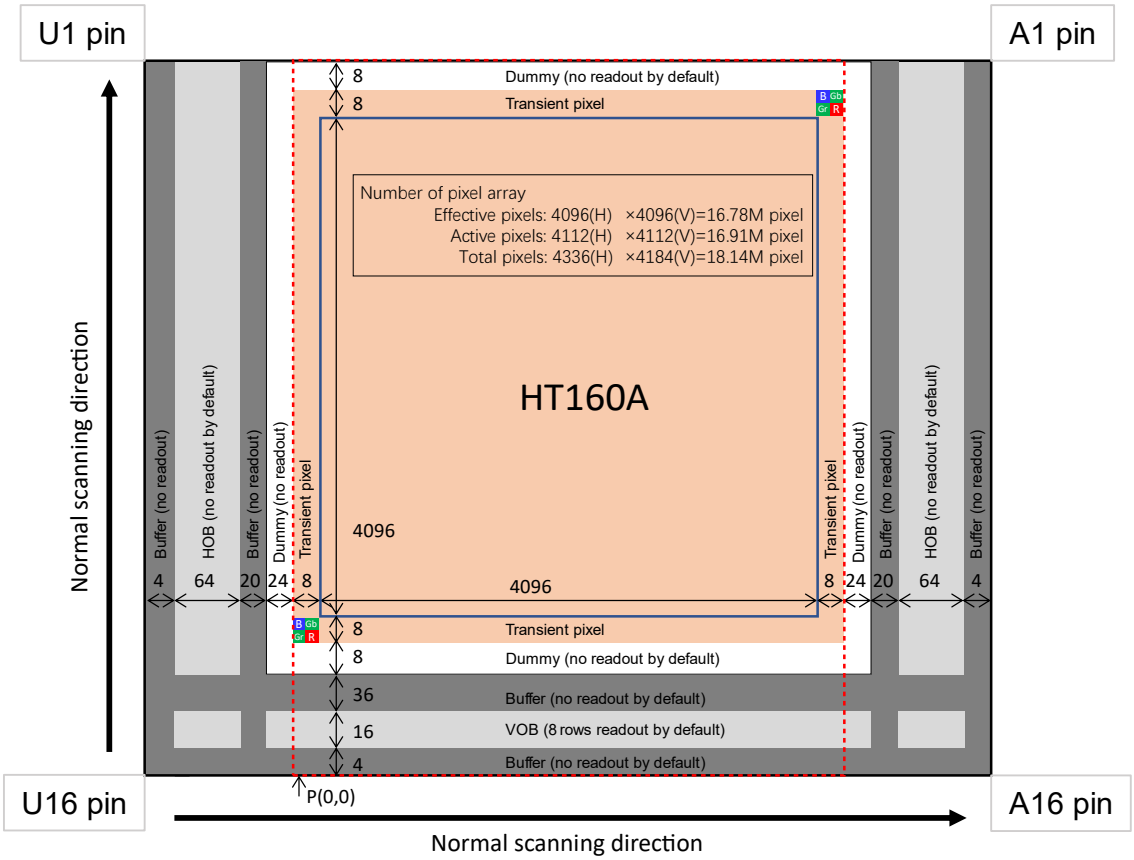


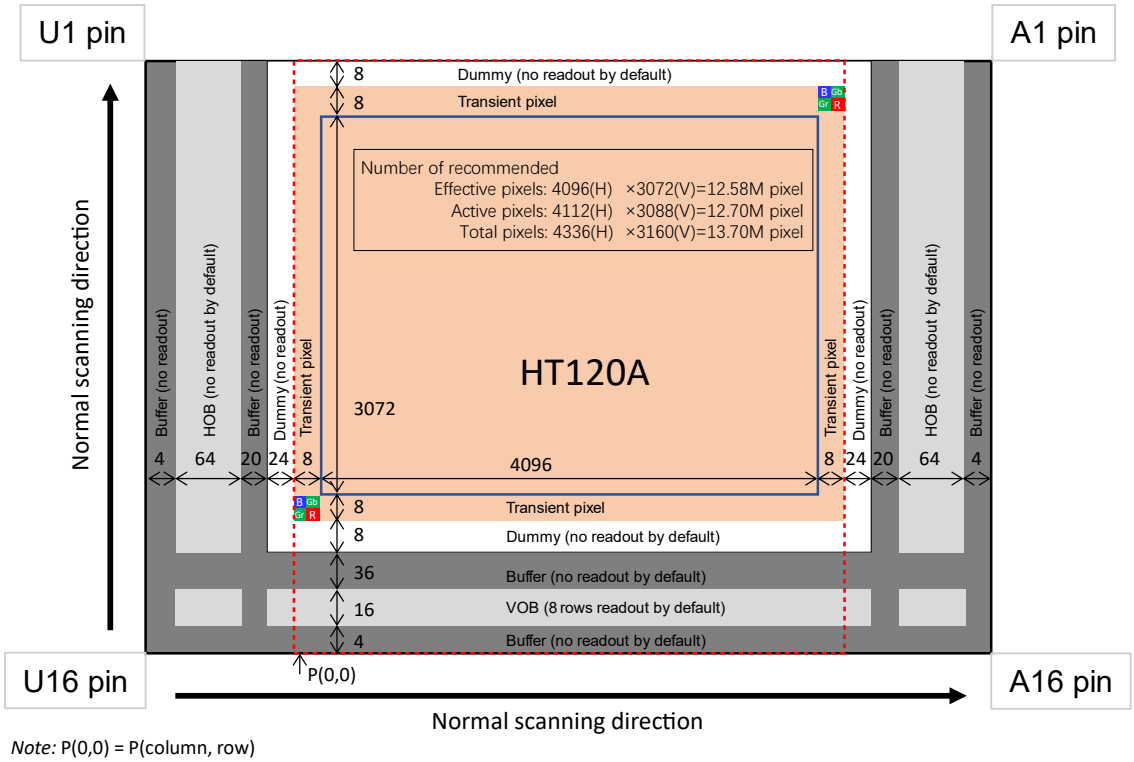
Figure 1. Block Diagram

Pixel Array



Note: P(0,0) = P(column, row)

Figure 2. HT160A Pixel Array



Note: P(0,0) = P(column, row)

Figure 3. HT120A Pixel Array

Pin Arrangement

	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A
1	NC	U1	NC	DTSTL0	VSYNC	VDD12T	SDO	SA	VDD12T	VSS12T	VDD12T	TOUT0	DTSTR0	NC6	NC	NC	A1
2			NC	DTSTL1	HSYNC	VSS12T	CSN	NC	VSS12T	VSS12T	VSS12T	TOUT2	DTSTR1	VDD12T	VNSUB		
3	NC	TXDN6	TXDP6	NC	TRGEXP	SDI	SCK	SYSRSTN	MSTSLV	SYSSTBN	TOUT1	NC	NC	VSSR	VSSR	NC	VRP_T
4	TXDN4	TXDP4	TXDN2	TXDP2	NC	VSSA1	VSSP	VSSA1	VSSA1	VSSP	VSSP	NC	VSSP	NC	VSSR	VDDR	VRA0_T
5	TXCN1	TXCP1	TXDN0	TXDP0	VSS18L	VDDA1	VDDP	NC	VDDA1	VDDP	VDDP	VDDCH	VSSP	NC	VSSR	VDDR	VRA1_T
6	TXDN1	TXDP1	TXDN3	TXDP3	VSS18L	VSS12L						TX2H	VSSP	RSL	VDDCL	NC	VRA2_T
7	TXDN5	TXDP5	TXDN7	TXDP7	VSS18L	VDD18						RSH	VSSP	VSSR	VIREF	TX1L	VSSR
8	VSS12L	ATST2	VSS18L	VSS18L	VDD18L	VSS12L			Top View			TX1H	VSSP	VSSR	VSSR	TX2L	GRSTL
9	INCLK	NC	VSS18L	VSS18L	VDD18L	VDD12L						GRSTH	VSSP	ATSTIN	VSSR	VDDR	VSSR
10	TXDN12	TXDP12	TXDN14	TXDP14	VSS18L	VDD12D						NC	VSSP	VSSCP	VCP1	ATST1	VRA2_B
11	TXDN8	TXDP8	TXDN10	TXDP10	VSS18L	VSS12D						VDDP	VSSP	VSSCP	VCP1IN	ATST0	VRA1_B
12	TXCN2	TXCP2	TXDN9	TXDP9	VSS18L	VDDA2	NC	VDDP	VDDA2	NC	NC	VR_EXTS	VR_EXTR	VCP2	VSSCP	VDDCP	VRA0_B
13	TXDN13	TXDP13	TXDN11	TXDP11	NC	VSSA2	NC	VSSP	VSSA2	VSSA2	NC	NC	NC	VCP2IN	NC	NC	VRP_B
14	NC	TXDN15	TXDP15	NC2	NC3	NC	NC	NC	NC	NC	NC	NC	VDD12CP	VSSCP	VSSCP	NC	NC
15	U16		NC1	DTSTL4	NC4	VSS12B	NC	VSS12B	NC	VSS12B	NC	VSS12B	DTSTR4	VDD12CP	VDDCP	A16	
16	NC		RCK2	DTSTL3	NC5	VDD12B	NC	VDD12B	NC	VDD12B	NC	VDD12B	DTSTR3	NC	NC	NC	

Figure 4. Package pin arrangement (Top View)

Pin Descriptions

#	PIN#	I/O	A/D	PIN Function	Description
1	A1	-	-	NC	-
2	A3	I	A	VRP_T	Voltage reference for readout circuits, connect to a capacitor to GND.
3	A4	I	A	VRA0_T	Voltage reference for readout circuits, connect to a capacitor to GND.
4	A5	I	A	VRA1_T	Voltage reference for readout circuits, connect to a capacitor to GND.
5	A6	I	A	VRA2_T	Voltage reference for readout circuits, connect to a capacitor to GND.
6	A7	GND	A	VSSR	3.3V analog ground.
7	A8	I	A	GRSTL	Pixel driving signal low level voltage power supply, connect to 10uF+0.1uF to GND.
8	A9	GND	A	VSSR	3.3V analog ground.
9	A10	I	A	VRA2_B	Voltage reference for readout circuits, connect to a capacitor to GND.
10	A11	I	A	VRA1_B	Voltage reference for readout circuits, connect to a capacitor to GND.
11	A12	I	A	VRA0_B	Voltage reference for readout circuits, connect to a capacitor to GND.
12	A13	I	A	VRP_B	Voltage reference for readout circuits, connect to a capacitor to GND.
13	A14	-	-	NC	-
14	A16	-	-	NC	-
15	B3	-	-	NC	-
16	B4	PWR	A	VDDR	3.3V analog power supply.
17	B5	PWR	A	VDDR	3.3V analog power supply.
18	B6	-	-	NC	-
19	B7	I/O	A	TX1L	Pixel driving signal low level voltage power supply, connect to 10uF+0.1uF to GND.
20	B8	I/O	A	TX2L	Pixel driving signal low level voltage power supply, connect to 10uF+0.1uF to GND.
21	B9	PWR	A	VDDR	3.3V analog power supply.
22	B10	O	A	ATST1	Analog test output.
23	B11	O	A	ATST0	Analog test output.
24	B12	PWR	A	VDDCP	3.3V analog power supply.
25	B13	-	-	NC	-
26	B14	-	-	NC	-
27	C1	-	-	NC	-
28	C2	PWR	A	VNSUB	Chip substrate potential, 3.3V.
29	C3	GND	A	VSSR	3.3V analog ground.
30	C4	GND	A	VSSR	3.3V analog ground.
31	C5	GND	A	VSSR	3.3V analog ground.
32	C6	GND	A	VDDCL	Pixel driving signal low level voltage power supply, connect to 2.2uF+0.1uF to GND.
33	C7	O	A	VIREF	Connect to analog ground through a 62k resistance.
34	C8	GND	A	VSSR	3.3V analog ground.
35	C9	GND	A	VSSR	3.3V analog ground.
36	C10	O	A	VCP1	Charge pump output, connect to VCP1IN and 22uF+0.1uF to GND.
37	C11	I	A	VCP1IN	LDO power supply, connect to VCP1.
38	C12	GND	A	VSSCP	3.3V analog ground.
39	C13	-	-	NC	-
40	C14	GND	A	VSSCP	3.3V analog ground.
41	C15	PWR	A	VDDCP	3.3V analog power supply.
42	C16	-	-	NC	-
43	D1	-	-	NC6	-
44	D2	PWR	D	VDD12T	Digital power supply, 1.2V.
45	D3	GND	A	VSSR	3.3V analog ground.
46	D4	-	-	NC	-
47	D5	-	-	NC	-
48	D6			RSL	Pixel driving signal low level voltage power supply.

49	D7	GND	A	VSSR	3.3V analog ground.
50	D8	GND	A	VSSR	3.3V analog ground.
51	D9	I	A	ATSTIN	Test pin. Leave this pin open.
52	D10	GND	D	VSSCP	Analog ground.
53	D11	GND	D	VSSCP	Analog ground.
54	D12	O	A	VCP2	Charge pump output, connect to VCP2IN and 22uF+0.1uF to GND.
55	D13	I	A	VCP2IN	LDO power supply, connect to VCP2.
56	D14	GND	D	VSSCP	Analog ground.
57	D15	PWR	D	VDD12CP	Digital power supply, 1.2V.
58	D16	-	-	NC	-
59	E1	O	D	DTSTR0	Digital test output.
60	E2	O	D	DTSTR1	Digital test output.
61	E3	-	-	NC	-
62	E4	GND	A	VSSP	3.3V analog ground.
63	E5	GND	A	VSSP	3.3V analog ground.
64	E6	GND	A	VSSP	3.3V analog ground.
65	E7	GND	A	VSSP	3.3V analog ground.
66	E8	GND	A	VSSP	3.3V analog ground.
67	E9	GND	A	VSSP	3.3V analog ground.
68	E10	GND	A	VSSP	3.3V analog ground.
69	E11	GND	A	VSSP	3.3V analog ground.
70	E12	I	A	VR_EXTR	Test pin. Leave this pin open.
71	E13	-	-	NC	-
72	E14	PWR	D	VDD12CP	Digital power supply, 1.2V.
73	E15	O	D	DTSTR4	Digital test output.
74	E16	O	D	DTSTR3	Digital test output.
75	F1	O	D	TOUT0	Pulse output. TOUT0 is High during pixel exposure period.
76	F2	O	D	TOUT2	Leave this pin open if do not use.
77	F3	-	-	NC	-
78	F4	-	-	NC	-
79	F5	PWR	A	VDDCH	Pixel driving signal high level voltage power supply.
80	F6	PWR	A	TX2H	Pixel driving signal high level voltage power supply, connect to 2.2uF+0.1uF to GND.
81	F7	PWR	A	RSH	Pixel driving signal high level voltage power supply, connect to 2.2uF+0.1uF to GND.
82	F8	PWR	A	TX1H	Pixel driving signal high level voltage power supply, connect to 4.7uF+0.1uF to GND.
83	F9	PWR	A	GRSTH	Pixel driving signal high level voltage power supply, connect to 2.2uF+0.1uF to GND.
84	F10	-	-	NC	-
85	F11	PWR	A	VDDP	3.3V analog power supply.
86	F12	I	A	VR_EXTS	Test pin. Leave this pin open.
87	F13	-	-	NC	-
88	F14	-	-	NC	-
89	F15	GND	D	VSS12B	Digital ground.
90	F16	PWR	D	VDD12B	Digital power supply, 1.2V.
91	G1	PWR	D	VDD12T	Digital power supply, 1.2V.
92	G2	GND	D	VSS12T	Digital ground.
93	G3	O	D	TOUT1	Leave this pin open if not use.
94	G4	GND	A	VSSP	3.3V analog ground.
95	G5	PWR	A	VDDP	3.3V analog power supply.
96	G12	-	-	NC	-
97	G13	-	-	NC	-
98	G14	-	-	NC	-
99	G15	-	-	NC	-

100	G16	-	-	NC	-
101	H1	GND	D	VSS12T	Digital ground.
102	H2	GND	D	VSS12T	Digital ground.
103	H3	I	D	SYSSTBN	System standby signal, low active.
104	H4	GND	A	VSSP	3.3V analog ground.
105	H5	PWR	A	VDDP	3.3V analog power supply.
106	H12	-	-	NC	-
107	H13	GND	A	VSSA2	3.3V analog ground.
108	H14	-	-	NC	-
109	H15	GND	D	VSS12B	Digital ground.
110	H16	PWR	D	VDD12B	Digital power supply, 1.2V.
111	J1	PWR	D	VDD12T	Digital power supply, 1.2V.
112	J2	GND	D	VSS12T	Digital ground.
113	J3	I	D	MSTSLV	Master/Slave selection input. Low: Master, High: Slave.
114	J4	GND	A	VSSA1	3.3V analog ground.
115	J5	PWR	A	VDDA1	3.3V analog power supply.
116	J12	PWR	A	VDDA2	3.3V analog power supply.
117	J13	GND	A	VSSA2	3.3V analog ground.
118	J14	-	-	NC	-
119	J15	-	-	NC	-
120	J16	-	-	NC	-
121	K1	I	D	SA	Slave device address selection for 2-wire serial communication interface.
122	K2	-	-	NC	-
123	K3	I	D	SYSRSTN	System reset signal. Low active.
124	K4	GND	A	VSSA1	3.3V analog ground.
125	K5	-	-	NC	-
126	K12	PWR	A	VDDP	3.3V analog power supply.
127	K13	GND	A	VSSP	3.3V analog ground.
128	K14	-	-	NC	-
129	K15	GND	D	VSS12B	Digital ground.
130	K16	PWR	D	VDD12B	Digital power supply, 1.2V.
131	L1	O	D	SDO	Data output of the 4-wire serial communication interface.
132	L2	I	D	CSN	Enable signal of the 4-wire serial communication interface. Pull low to enable the communication.
133	L3	I	D	SCK/SCL	SCK is the clock input of the 4-wire serial communication interface. This pin shares with SCL of the 2-wire serial communication interface.
134	L4	GND	A	VSSP	3.3V analog ground.
135	L5	PWR	A	VDDP	3.3V analog power supply.
136	L12	-	-	NC	-
137	L13	-	-	NC	-
138	L14	-	-	NC	-
139	L15	-	-	NC	-
140	L16	-	-	NC	-
141	M1	PWR	D	VDD12T	Digital power supply, 1.2V.
142	M2	GND	D	VSS12T	Digital ground.
143	M3	I	D	SDI/SDA	SDI is the data input of the 4-wire serial communication interface. This pin shares with SDA of the 2-wire serial communication interface.
144	M4	GND	A	VSSA1	3.3V analog ground.
145	M5	PWR	A	VDDA1	3.3V analog power supply.
146	M6	GND	D	VSS12L	Digital ground.
147	M7	PWR	D	VDD18	I/O power supply, 1.8V.
148	M8	GND	D	VSS12L	Digital ground.
149	M9	PWR	D	VDD12L	Digital power supply, 1.2V.

150	M10	PWR	D	VDD12D	Digital power supply, 1.2V.
151	M11	GND	D	VSS12D	Digital ground.
152	M12	PWR	A	VDDA2	3.3V analog power supply.
153	M13	GND	A	VSSA2	3.3V analog ground.
154	M14	-	-	NC	-
155	M15	GND	D	VSS12B	Digital ground.
156	M16	PWR	D	VDD12B	Digital power supply, 1.2V.
157	N1	I/O	D	VSYNC	Vertical scanning period sync signal output (Master mode) or input (Slave mode).
158	N2	I/O	D	HSYNC	Horizontal scanning period sync signal output (Master mode) or input (Slave mode).
159	N3	I	D	TRGEXP	Trigger input.
160	N4	-	-	NC	-
161	N5	GND	D	VSS18L	1.8V LVDS Digital ground.
162	N6	GND	D	VSS18L	1.8V LVDS Digital ground.
163	N7	GND	D	VSS18L	1.8V LVDS Digital ground.
164	N8	PWR	D	VDD18L	Digital power supply, 1.8V.
165	N9	PWR	D	VDD18L	Digital power supply, 1.8V.
166	N10	GND	D	VSS18L	1.8V LVDS Digital ground.
167	N11	GND	D	VSS18L	1.8V LVDS Digital ground.
168	N12	GND	D	VSS18L	1.8V LVDS Digital ground.
169	N13	-	-	NC	-
170	N14	-	-	NC3	-
171	N15	-	-	NC4	-
172	N16	-	-	NC5	-
173	P1	O	D	DTSTL0	Digital test output.
174	P2	O	D	DTSTL1	Digital test output.
175	P3	-	-	NC	-
176	P4	O	D	TXDP2	LVDS data output.
177	P5	O	D	TXDP0	LVDS data output.
178	P6	O	D	TXDP3	LVDS data output.
179	P7	O	D	TXDP7	LVDS data output.
180	P8	GND	D	VSS18L	1.8V LVDS Digital ground.
181	P9	GND	D	VSS18L	1.8V LVDS Digital ground.
182	P10	O	D	TXDP14	LVDS data output.
183	P11	O	D	TXDP10	LVDS data output.
184	P12	O	D	TXDP9	LVDS data output.
185	P13	O	D	TXDP11	LVDS data output.
186	P14	-	-	NC2	-
187	P15	O	D	DTSTL4	Digital test output
188	P16	O	D	DTSTL3	Digital test output
189	R1	-	-	NC	-
190	R2	-	-	NC	-
191	R3	O	D	TXDP6	LVDS data output.
192	R4	O	D	TXDN2	LVDS data output.
193	R5	O	D	TXDN0	LVDS data output.
194	R6	O	D	TXDN3	LVDS data output.
195	R7	O	D	TXDN7	LVDS data output.
196	R8	GND	D	VSS18L	1.8V LVDS Digital ground.
197	R9	GND	D	VSS18L	1.8V LVDS Digital ground.
198	R10	O	D	TXDN14	LVDS data output.
199	R11	O	D	TXDN10	LVDS data output.
200	R12	O	D	TXDN9	LVDS data output.

201	R13	O	D	TXDN11	LVDS data output.
202	R14	O	D	TXDP15	LVDS data output.
203	R15	-	-	NC1	-
204	R16	O	D	RCK2	Internal clock output. Its frequency is half that of the internal reference clock.
205	T3	O	D	TXDN6	LVDS data output.
206	T4	O	D	TXDP4	LVDS data output.
207	T5	O	D	TXCP1	LVDS clock output.
208	T6	O	D	TXDP1	LVDS data output.
209	T7	O	D	TXDP5	LVDS data output.
210	T8	O	A	ATST2	Analog test output.
211	T9	-	-	NC	-
212	T10	O	D	TXDP12	LVDS data output.
213	T11	O	D	TXDP8	LVDS data output.
214	T12	O	D	TXCP2	LVDS clock output.
215	T13	O	D	TXDP13	LVDS data output.
216	T14	O	D	TXDN15	LVDS data output.
217	U1	-	-	NC	-
218	U3	-	-	NC	-
219	U4	O	D	TXDN4	LVDS data output.
220	U5	O	D	TXCN1	LVDS clock output.
221	U6	O	D	TXDN1	LVDS data output.
222	U7	O	D	TXDN5	LVDS data output.
223	U8	GND	D	VSS12L	Digital ground.
224	U9	I	D	INCLK	Input reference clock.
225	U10	O	D	TXDN12	LVDS data output.
226	U11	O	D	TXDN8	LVDS data output.
227	U12	O	D	TXCN2	LVDS clock output.
228	U13	O	D	TXDN13	LVDS data output.
229	U14	-	-	NC	-
230	U16	-	-	NC	-

Peripheral Connections

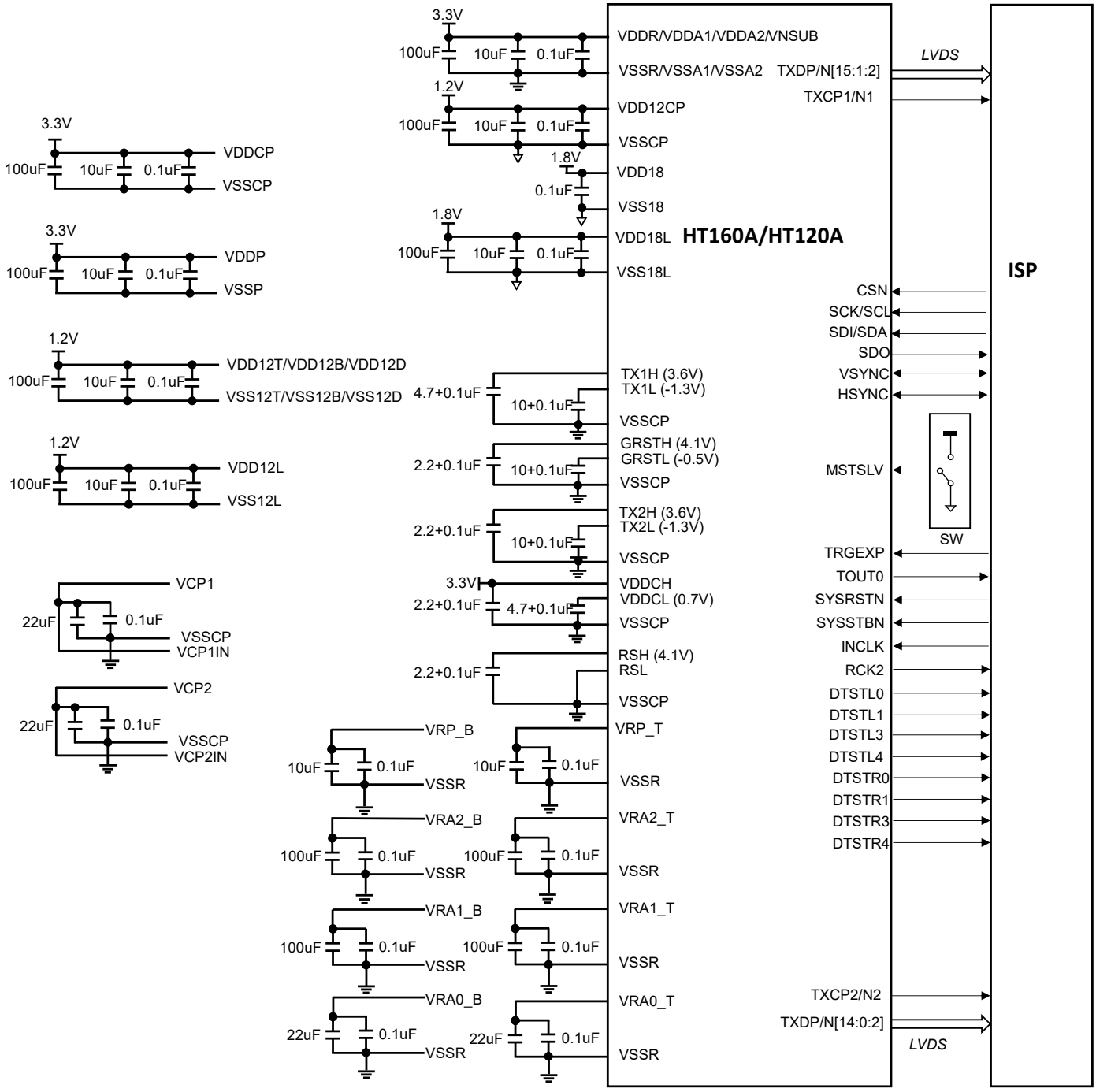


Figure 5. Peripheral connections

Absolute Maximum Ratings

Table 2. Absolute maximum ratings

Operation ambient temperature (T_A)		T.B.D (-30 ~ 75 ℃)
Storage ambient temperature (T_{STOR})		T.B.D (-40 ~ 85 ℃)
Supply voltage (With respect to ground)	VDDR, VDDA1, VDDA2, VDDP, VDDCP, VNSUB	-0.3V ~ 4.6V
	VDD18, VDD18L	-0.3V ~ 3.3V
	VDD12T, VDD12B, VDD12D, VDD12L, VDD12CP	-0.3V ~ 1.7V
Digital I/O (DIO/DI/DO. With respect to ground.)		-0.3V ~ VDD18 + 0.3V but <3.3V
Analog I/O (AIO. With respect to ground.)		-0.3V ~ VDD33 + 0.3V but <4.6V

Note: Exceeding the absolute maximum ratings listed above will affect all AC and DC electrical characteristics and may result in permanent damage to the device.

DC Electrical characteristics

Table 3. DC electrical characteristic

Parameter Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Power Supplies						
3.3V analog/digital power supply	AV33		3.3		V	Analog core power supply. Pin VDDR, VDDA1, VDDA2 and VNSUB.
3.3V analog power supply	VDDCP		3.3		V	-
1.8V I/O power supply	VDD18		1.8		V	-
1.8V I/O (LVDS) power supply	VDD18L		1.8		V	-
1.2V digital power supply	DV12		1.2		V	Digital core power supply Pin VDD12T, VDD12B, VDD12D, VDD12L and VDD12CP.
3.3V operation current	IAV33		420		mA	Design target. With both AV33 and VDDCP.
1.8V I/O operation current	IVDD18		1		mA	Design target.
1.8V LVDS operation current	IVDD18L		43		mA	16 channels. Design target.
1.2V operation current	IDV12		252		mA	Design target.
Pixel power supply Note 1						
Pixel power supply	TX1H		3.6		V	-
	TX1L		-1.3		V	-
Pixel power supply	GRSTH		4.1		V	-
	GRSTL		-0.5		V	-
Pixel power supply	TX2H		3.6		V	-
	TX2L		-1.3		V	-
Pixel power supply	VDDCH		3.3		V	-
	VDDCL		0.7		V	-
Pixel power supply	RSH		4.1		V	-
	RSL		0		V	-
Pixel power supply	VDDP		3.3		V	Pixel/analog core power supply.
Readout Circuits Reference Voltage Note 2						
PGA voltage reference	VRP		1.25		V	-
ADC voltage reference	VRA2		2.2		V	-
	VRA1		1.2		V	-
	VRA0		1.2		V	-
Digital I/O						
Output High Voltage	VOH	VDD18 - 0.4			V	IOH = 2mA
Output Low Voltage	VOL			0.4	V	IOL = 2mA
Input High Voltage	VIH	VDD18 x 0.8			V	-
Input Low Voltage	VIL			VDD18 x 0.2	V	-
Low Level Output Current	IOL		2		mA	VOL = 0.4 V
High Level Output Current	IOH		2		mA	VOH = VDD18-0.4 V
LVDS I/O						
Output Common Voltage	VOCOM		0.9		V	-
Output Differential Voltage	|VOD|	200	300	400	mV	Depending on the board design

Note 1: Pixel power supplies are generated on-chip (TX1H, TX1L, TX2H, TX2L, GRSTH, GRSTL, VDDCH, VDDCL, RSH and RSL). Please refer to **Peripheral Connections** for details about connections. These reference voltages can also be generated by off-chip circuits. When use the off-chip voltage generator, the internal voltage generator must be disabled by register settings.

Note 2: These reference voltages are generated on-chip (VRP_T/B, VRA2_T/B, VRA1_T/B and VRA0_T/B). For details about connection, please refer to **Peripheral Connections**. These reference voltages can also be generated by off-chip circuits. When use the off-chip voltage generator, the internal voltage generator must be disabled by register settings.

AC Electrical characteristics

Input reference clock (INCLK)

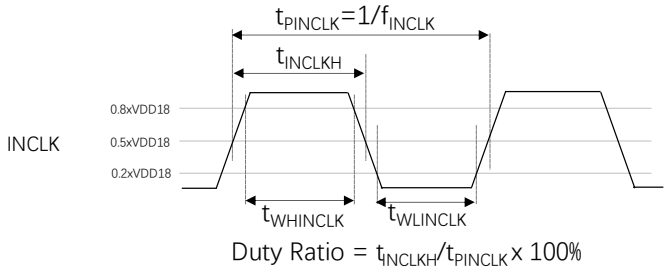


Figure 6. INCLK input waveform diagram

Table 4. INCLK AC electrical characteristics

Parameter Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Clock frequency of INCLK	f_{INCLK}	12	37.125	62.5	MHz	-
INCLK high level pulse width	$t_{WHINCLK}$	T.B.D	-	-	ns	-
INCLK low level pulse width	$t_{WLINCLK}$	T.B.D	-	-	ns	-
Duty Ratio	-	45	50	55	%	-

Sync signal output waveform diagram (Master Mode)

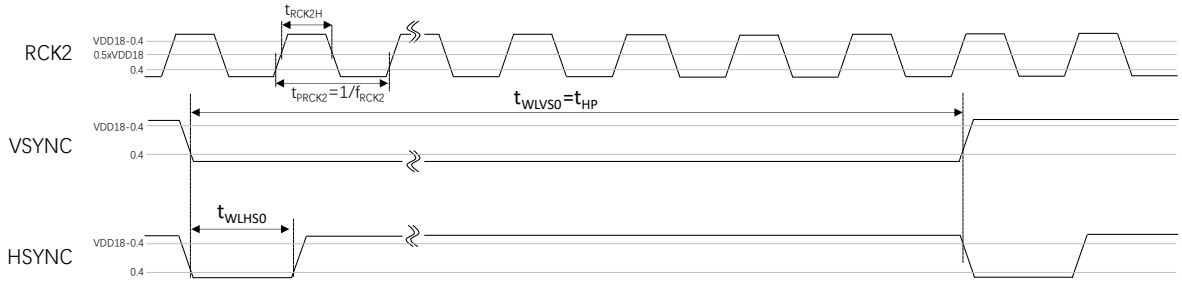


Figure 7. Sync signal output waveform diagram in master mode

Table 5. Sync signal output AC electrical characteristics in master mode

Parameter Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Clock frequency of clock output RCK2	f_{RCK2}	-	55.7	-	MHz	$t_{PRCK2}=1/f_{RCK2}$. *Note1*
RCK2 Duty Ratio	-	T.B.D	50	T.B.D	%	t_{RCK2H}/t_{PRCK2} x 100%
Vertical sync signal output low level pulse width	t_{WLVS0}	-	1x t_{HP}	-	us	*Note2*
Horizontal sync signal output low level pulse width	t_{WLHS0}	2xt_{PRCK2}	-	-	us	-

Note 1. Refer to **Input Reference Clock and Clock System** for detail
Note 2. t_{HP} is the period of one horizontal scanning period. Refer to **Frame Rate and Output Data Rate** for details.

Sync signal input waveform diagram (Slave Mode)

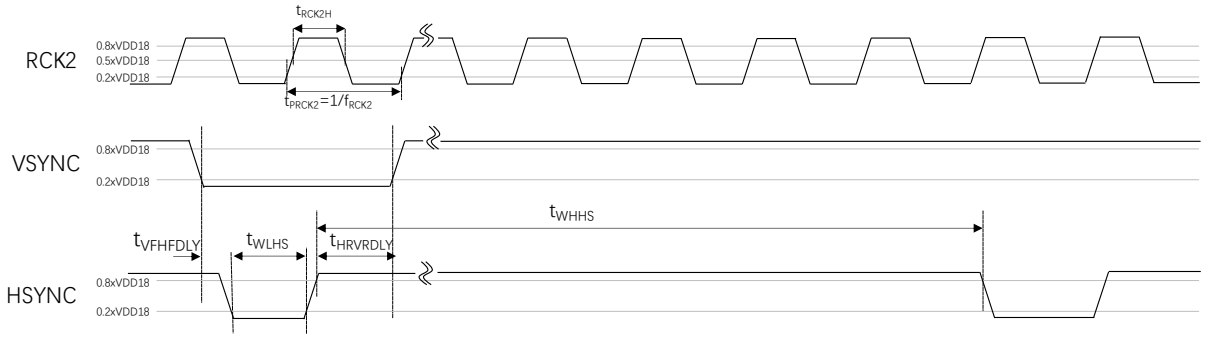


Figure 8. Sync signal input waveform diagram in slave mode

Table 6. Sync signal input AC electrical characteristics in slave mode

Parameter Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Clock frequency of clock output RCK2	f_{RCK2}	-	55.7	-	MHz	$t_{PRCK2}=1/f_{RCK2}$
RCK2 Duty Ratio	-	T.B.D	50	T.B.D	%	t_{RCK2H}/t_{PRCK2} x 100%
Horizontal sync signal input low level pulse width.	t_{WLHS}	4 x t_{PRCK2}	-	-	us	-
Horizontal sync signal input high level pulse width.	t_{WHHS}	4 x t_{PRCK2}	-	-	us	-
VSYNC falling edge to HSYNC falling edge delay	$t_{VFHFDLY}$	2 x t_{PRCK2}	-	-	us	-
HSYNC rising edge to VSYNC rising edge delay	$t_{HRVRDLY}$	2 x t_{PRCK2}	-	-	us	-

Sync signal input waveform diagram (TRIGEXP Mode)

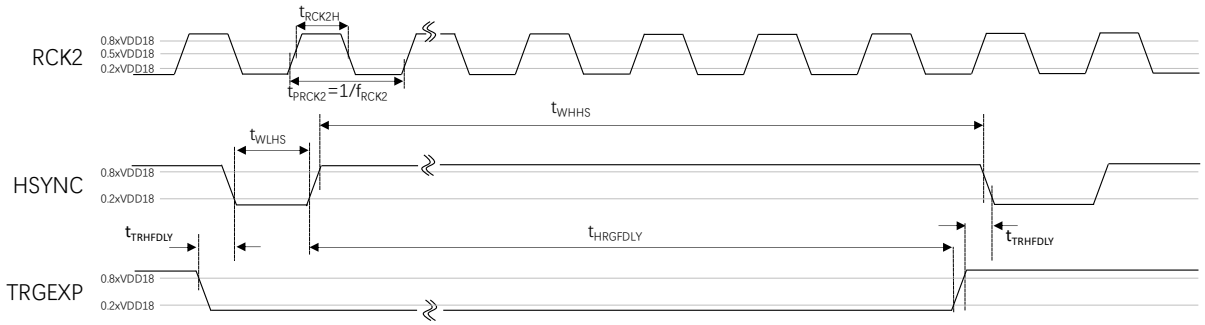
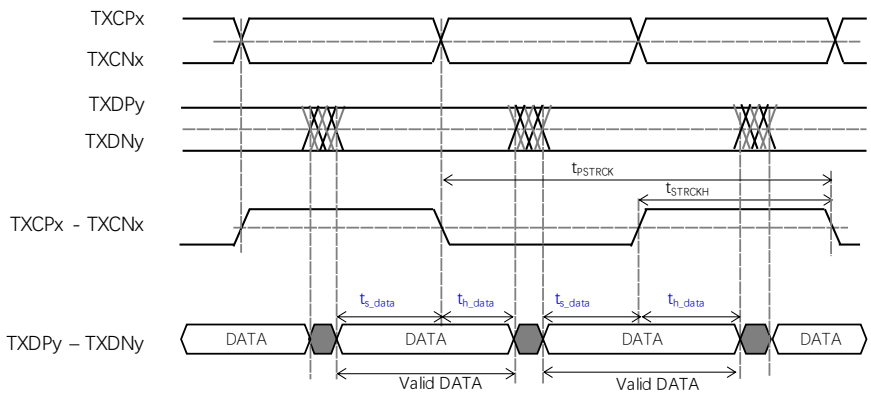


Figure 9. Sync signal input waveform diagram in TRIGEXP mode

Table 7. Sync signal input AC electrical characteristics in TRIGEXP mode

Parameter Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Clock frequency of clock output RCK2	f_{RCK2}	-	55.7	-	MHz	$t_{PRCK2}=1/f_{RCK2}$
RCK2 Duty Ratio	-	T.B.D	50	T.B.D	%	t_{RCK2H}/t_{PRCK2} x 100%
Horizontal sync signal input low level pulse width.	t_{WLHS}	4 x t_{PRCK2}	-	-	us	-
Horizontal sync signal input high level pulse width.	t_{WHHS}	4 x t_{PRCK2}	-	-	us	-
TRGEXP rising edge to HSYNC falling edge delay	$T_{TRHFDLY}$	2 x t_{PRCK2}	-	-	us	-
TRGEXP falling edge to HSYNC falling edge delay	$T_{TFHFDLY}$	2 x t_{PRCK2}	-	-	us	-

LVDS Outputs



TXCPx/TXCNx , where x: 1,2
TXDPy/TXDNy, where y: 0,1,2···15

Figure 10. LVDS signal waveform diagram

Table 8. LVDS signals AC characteristics

Parameter Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Serial Data clock frequency	f_{SRCK}	-		1039.5	MHz	Note 1
LVDS strobe clock frequency	f_{STRCK}	-		779.625	MHz	$f_{STRCK} = 1/t_{PSTRCK} = f_{SRCK}/2$
LVDS strobe clock duty ratio	-		50		%	t_{STRCKH}/t_{PSTRCK} x 100%
LVDS data setup time	t_{s_data}	-	T.B.D. (0.35)	-	UI	$1UI = 1/ f_{STRCK}$
LVDS data hold time	t_{h_data}	-	T.B.D. (0.35)	-	UI	$1UI = 1/ f_{STRCK}$

Note 1. Please refer to **Input Reference Clock and Clock System.**

4-wire SPI-like serial communication interface timing diagram

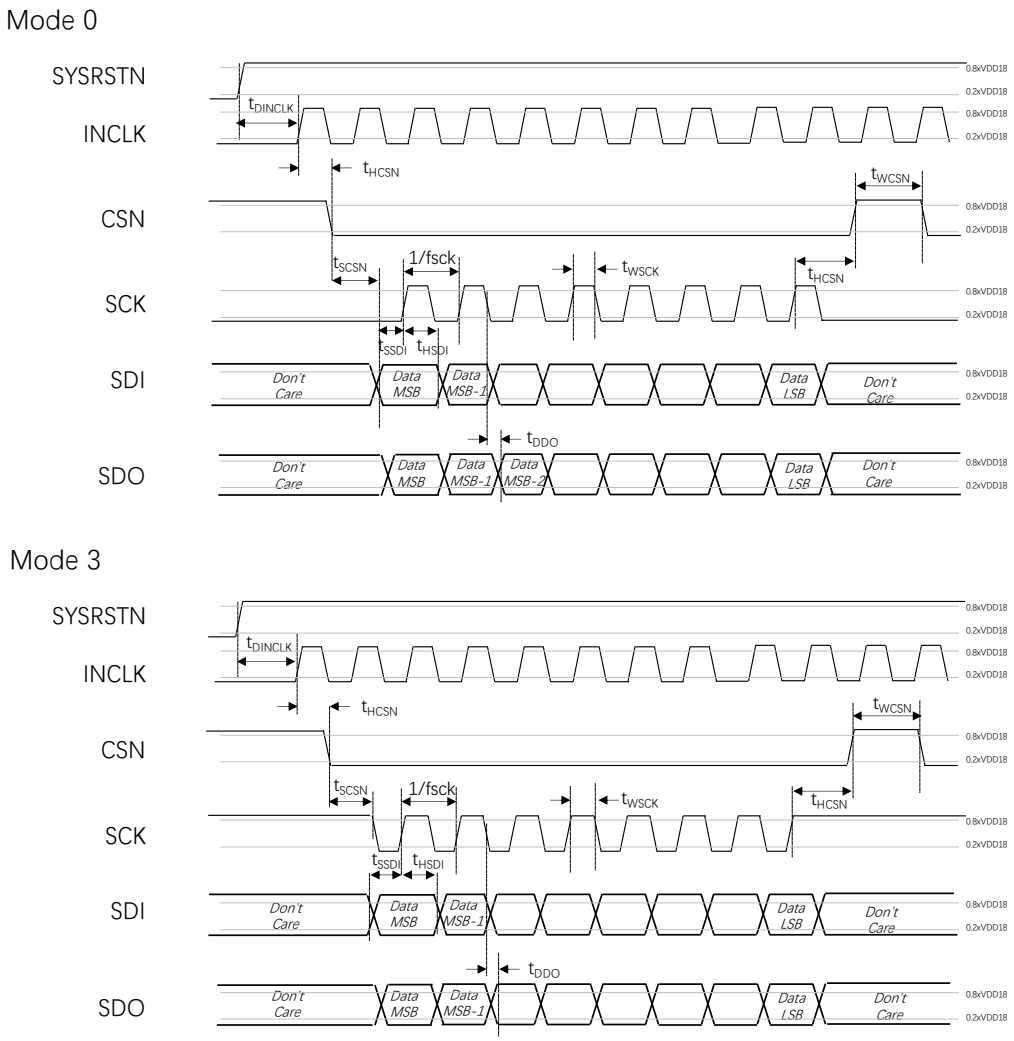


Figure 11. 4-wire serial interface timing diagram

Table 9. 4-wire serial interface AC electrical characteristics

Parameter Item	Symbol	Specs				Note
		Min.	Typ.	Max.	unit	
SCK input frequency	f_{SCK}	-	-	$f_{INCLK}/5$	MHz	-
CSN input high level pulse width	t_{WCSN}	2 x t_{PINCLK}	-	-	us	$t_{PINCLK}=1/f_{INCLK}$
Clock input delay	t_{DINCLK}	1.5 x t_{PINCLK}	-	-	us	-
SCK input high level pulse width	t_{WSCK}	2 x t_{PINCLK}	-	-	us	-
CSN input setup time	t_{SCSN}	2 x t_{PINCLK}	-	-	us	-
CSN input hold time	t_{HCSN}	2.5 x t_{PINCLK}	-	-	us	-
SDI input setup time	t_{SSDI}	t_{PINCLK}+0.005	-	-	us	-
SDI input hold time	t_{HSDI}	t_{PINCLK}+0.005	-	-	us	-
SDO data output delay	t_{DDO}	t_{PINCLK}+0.005	-	-	us	-

2-wire serial communication interface timing diagram

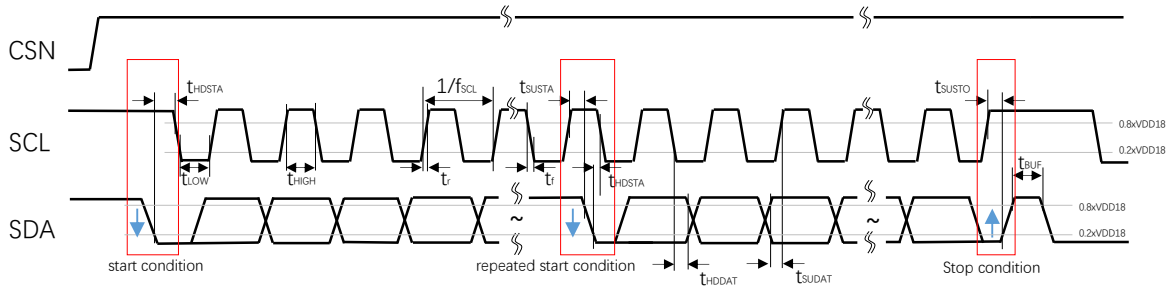


Figure 12. 2-wire serial interface timing diagram

Table 10. 2-wire serial interface AC electrical characteristics

Parameter Item	Symbol	Specs				Note
		Min.	Typ.	Max.	unit	
SCL *Note1* input frequency	f_{SCL}	-	-	1	MHz	-
Setup time (Start condition)	t_{HDSTA}	0.26	-	-	us	-
Hold time (Repeated start condition)	t_{SUSTA}	0.26	-	-	us	-
SCL input low level pulse width	t_{LOW}	0.50	-	-	us	-
SCL input high level pulse width	t_{HIGH}	0.26	-	-	us	-
Data setup time	t_{SUDAT}	0	-	0.45	us	-
Data hold time	T_{HDDAT}	0.05	-		us	-
Setup time (Stop condition)	t_{SUSTO}	0.26	-	-	us	-
Bus free time between a Stop and a Start condition	t_{BUF}	0.50	-	-	us	-
SDA *Note 2*, SCL rising time	t_r	-	-	0.12	us	-
SDA, SCL falling time	t_f	-	-	0.12	us	-

Note 1. Share the same package pin with SCK.

Note 2. Share the same package pin with SDI.

Internal Register Access

This part describes the register access through 4-wire and 2-wire serial communication interface.

Internal Register Access

Please refer to AC Electrical characteristics for detailed waveform diagram.

4-wire SPI-like serial communication interface

1. Command packet, address packet and data packet
   The first 8-bit is command packet. The first bit is command-bit, “0” for write mode and “1” for read mode, and followed by four “0”s. The last three bits “S2,S1,S0” are used to select register block .
   The second 8-bit packet is address packet that specifies the address to write or read.
   Starting from the third packet, all packets are data packet, which in write mode are the data to write (input through SDI) and in read mode are the read out data from the corresponding address (output through SDO).

2. Random access to any address is possible.

3. It is also possible to access multi continuous addresses starting from a random address.
   In this mode, after the access to the address specified by address packet is completed, the target address will automatically point to the next address.

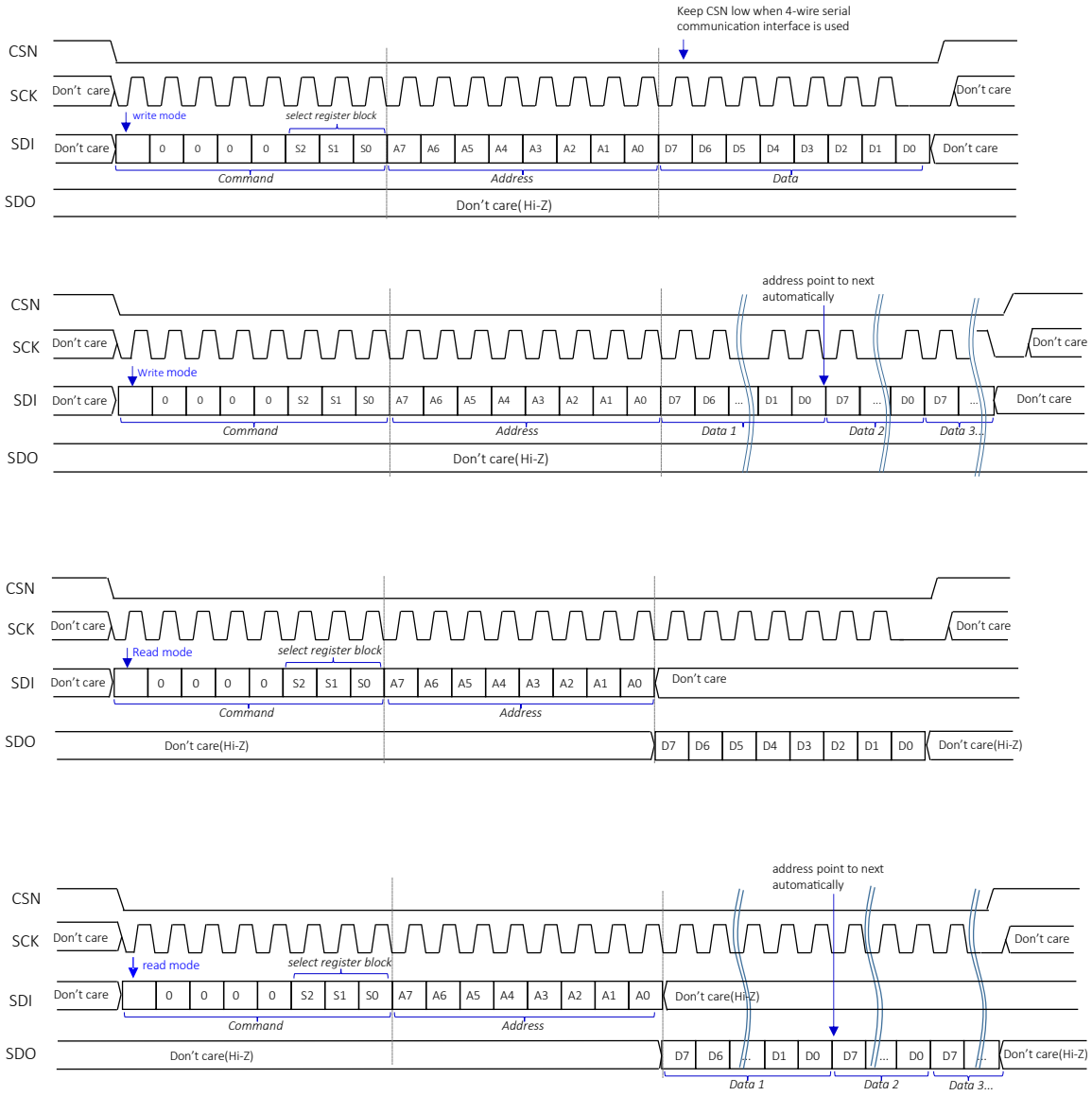


Figure 13. 4-wire serial communication interface timing diagram

2-wire serial communication interface

1. Start and stop condition (refer to Figure 14 for details)
   SDA can change only while SCL is high, so the start condition is that when SDA goes **from high to low** while SCL is high, and stop condition is that when SDA goes **from low to high** while SCL is high. When the stop condition is not generated in the previous communication phase and start condition is generated for the next communication, that start condition is recognised as a repeated start condition.

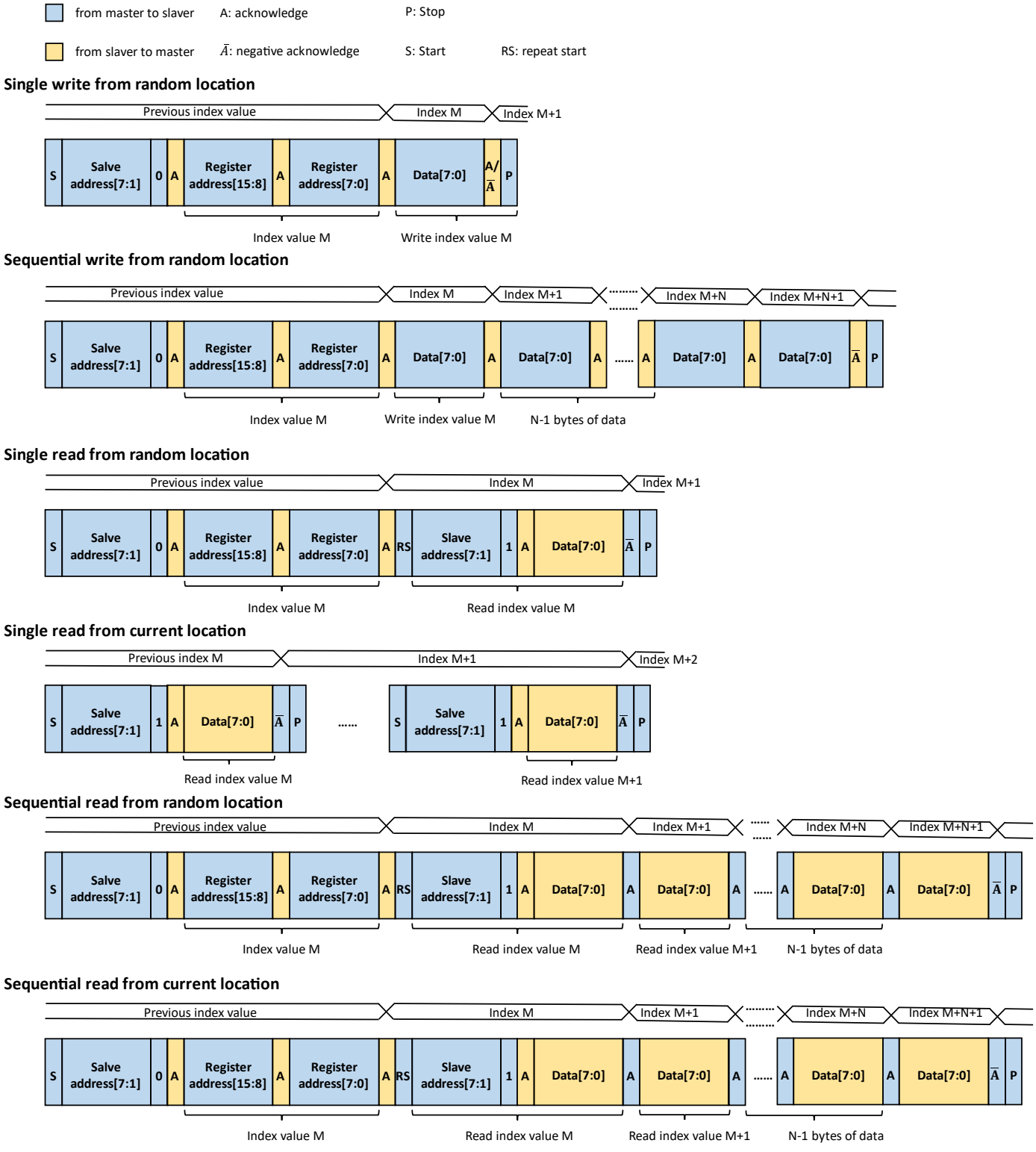


Figure 14. 2-wire serial communication interface timing diagram

2. Acknowledgment
   After master transferred a data byte to slaver, a bit of acknowledgment(A) or negative acknowledgment($\bar{A}$) is transferred from slaver to master, indicates the data byte to slaver is valid or invalid. And after slaver transferred a

data byte to master, a bit of acknowledgment(A) or negative acknowledgment($\bar{A}$) is transferred from master to slaver, indicates the data byte to master is valid or invalid.

3. Command packet, address packet and data packet
   The first 8-bit is command packet, in which the first 7 bits are slave address, and the last bit is command bit,"0" for write mode and "1" for read mode. Slave device address is set to "0010000" or "0011010" when the pin SA set to "0" or "1" . The second and third 8-bit packets are register address packets that specifies the address to write or read. Starting from the fourth packet, all packets are data packet, which in write mode are the data to write and in read mode are the read out data from the corresponding address. Data are transfered serially in 8 bits unit with MSB first.

4. Random access to any address is possible.

5. It is also possible to access multi continuous addresses starting from a random address.
   In this mode, after the access to the address specified by address packet is completed, the target address will automatically point to the next address.

Register Reflection Timing

There are two types of register reflection timing, immediately and sync-to-vertical-period. In **Register Map**, the column "reflection timing" marks each register's reflection timing, "I" for immediately and "V" for sync-to-vertical-period.

Immediately reflection timing

The registers will take into effect immediately after the input of 8-bit data packet.

Sync-to-vertical-period

Sync-to-vertical-period is controlled by register REGHOLD (address FBh, bit [0]).
When REGHOLD = "0", the registers will take into effect after the next VSYNC pulse.
When REGHOLD = "1", the registers will NOT take into effect till the first VSYNC pulse after REGHOLD being set to "0".

Serial communication period

Serial communication is forbidden during the periods before and after the VSYNC pulse as illustrated in Figure 15. The registers that will take into effect immediately after writing are recommended to set during power-on sequence.

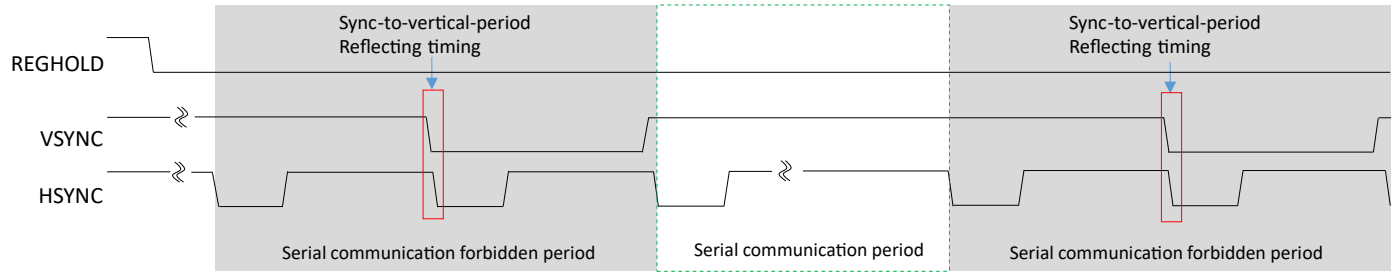


Figure 15. Register reflection timing diagram

Register Map

Please refer to other document for details.

Input Signals

Master Mode and Salve Mode

The sensors can operate at master mode and slave mode. The operation mode is selected by pin input and register setting. By default, since the register RMSTSLV and MSTSLV_SEL are both set to “0” , operation mode can be switched by pin MSTSLV.

Table 11. Register setting of master mode and slave mode

Operation Mode	pin input	Register setting	
	MSTSLV	RMSTSLV address 4Ch, bit [6]	MSTSLV_SEL Address 4Eh, bit [7]
Master mode	0	x	**0 (default)**
	x	**0 (default)**	1
Slave mode	1	x	**0 (default)**
	x	1	1

Note: TRIGEXP mode is same as slave mode

Input Signals

The sensors need input signals to operate properly.

Table 12. Input signals

	Master mode	Slave mode	TRIGEXP mode
Input Signals			
Reference clock (pin INCLK)	Yes	Yes	Yes
Synchronization signals (VSYNC/HSYNC)	No (Pin VSYNC, HSYNC are outputs)	Yes (Pin VSYNC, HSYNC are inputs)	Yes (Pin HSYNC is input)
Trigger signal (pin TRGEXP)	No (Do not care the input of pin TRIGEXP)	No (Do not care the input of pin TRIGEXP)	Yes (Pin TRGEXP is input)
Power supplies and voltage references	Yes[Note 1]	Yes The same as Master mode.	Yes The same as Master mode.

Note 1: Please refer to **DC Electrical characteristics** for details.

Input Reference Clock and Clock System

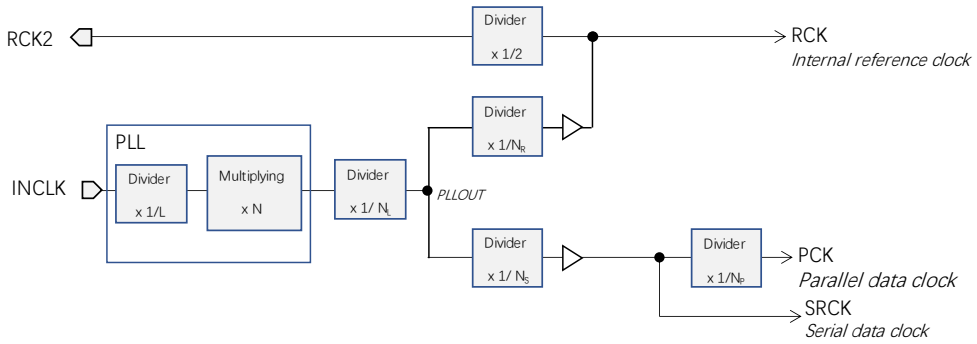


Figure 16. Clock system diagram

Input reference clock is input through pin INCLK and multiplied by PLL. From the PLL output clock, dividers generate internal reference clock (RCK), the parallel data clock (PCK) and the serial data clock (SRCK, it is also the LVDS strobe clock.).

The frequency of internal clock respect to the input reference clock are as shown below.

$f_{PLLOUT} = f_{INCLK} \times N / L / N_L$

$f_{RCK} = f_{PLLOUT} / N_R$

$f_{SRCK} = f_{PLLOUT} / N_S$

$f_{PCK} = f_{SRCK} / N_P$

f_{PCK} and f_{SRCK} must be set that, $f_{SRCK} = DBW \times f_{PCK}$ or $N_p = DBW$, where DBW is the output data bit-width and can be set to 14,12 ,10 or 8. N_P, N, L, N_L, N_R, and N_S are set by the registers in Table 13 ~ Table 18.

(By default,

L = 2, N = 42, N_L = 1, N_R = 7, N_S = 1, N_P = 14, DBW = 14

f_{INCLK} = 37.125 MHz

$f_{PLLOUT} = f_{INCLK} \times N / L / N_L$ = 37.125MHz × 42 / 2 / 1 = 779.625 MHz

$f_{RCK} = f_{PLLOUT} / N_R = 779.625MHz / 7 = 111.375$ MHz
$f_{SRCK} = f_{PLLOUT} / N_S = 779.625$ MHz
$f_{PCK} = f_{SRCK} / N_P = 779.625MHz / 14 = 55.6875$ MHz)

Table 13. Register setting of DBW or N_P

BS[1:0] Register address:C2h, bit [1:0]	Feedback Divider Ratio DBW or N_P
00b	8
01b	10
10b	12
11b (default)	**14**

Table 14. Register setting of N

DIV_N[6:0] Register address:62h, bit [6:0]	Feedback Divider Ratio N
00h～0Bh	Not defined
0Ch (default)	**12**
0Dh	13
0Eh	14
…	…
7Eh	126
7Fh	127

Table 15. Register setting of L

DIV_L[3:0] Register address: 61h, bit [3:0]	Input Divider Ratio L
0h	1
1h (default)	**2**
2h	3
…	…
Eh	15
Fh	16

Note: L = DIV_L + 1, where DIV_L is the register value in decimal.

Table 16. Register setting of N_L

DIV_NL[1:0] Register address: 65h, bit [7:6]	Post divider Ratio N_L
0h (default)	**1**
1h	2
2h	3
3h	4

Note: N_L = DIV_NL + 1, where DIV_NL is the register value in decimal.

Table 17. Register setting of N_R

CKGEN_RCKDIV[4:0] Register address:4Dh, bit [4:0]	RCK divider Ratio N_R
01h	1
02h	2
……	……
07h (default)	**7**
……	……
1Fh	31

Table 18. Register setting of N_S

DIV_NS[4:0] Register address:4Ch, bit [4:0]	SCK divider Ratio N_S
00h	0
01h (default)	**1**
02h	2
……	……
1Eh	30
1Fh	31

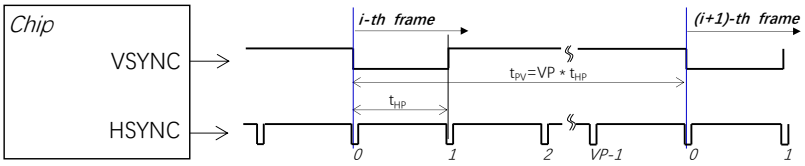
Synchronize Signal

In master mode, the sensors will internally generate a vertical scanning sync signal (VSYNC) and a horizontal scanning sync signal (HSYNC). These two sync signals are output through pin VSYNC and HSYNC, respectively. The waveforms are as shown in Figure 17, t_{HP} is the time of one horizontal period, VP is the number of horizontal periods in one vertical period.

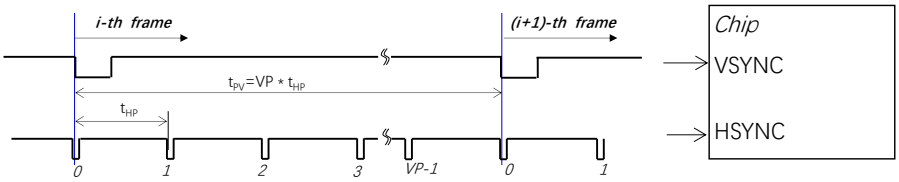
In slave mode, the vertical sync signal and horizontal sync signal must be input from pin VSYNC and HSYNC respectively. Refer to Figure 8 for electrical requirements. As shown in Figure 17, the vertical period and horizontal period are determined by the time between two adjacent pulses of VSYNC and HSYNC, respectively. The vertical period and horizontal period must be set carefully for proper operation, please refer to **Frame Rate and Output Data Rate** for details.

In TRIGEXP mode , the vertical sync signal VSYNC will be ignored, instead a trigger signal TRGEXP and HSYNC are the sync inputs. Refer to Figure 9 for electrical requirements.

Master Mode



Slave Mode



TRIGEXP Mode

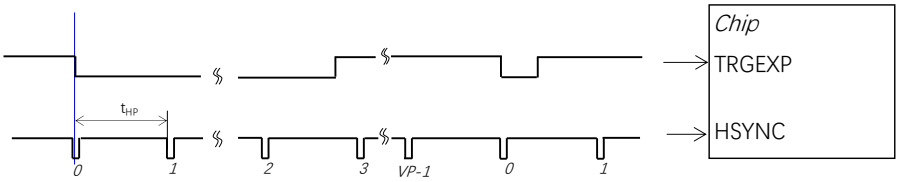


Figure 17. Timing diagram of synchronize signal

In master mode, the vertical period, VP, and horizontal period, HP, are set by the following registers.

Table 19 Vertical period and horizontal period settings.

Register	Unit	Register address and bits	Default value	Comment
VP[23:0]	t_{HP}, One horizontal period	0Eh [7:0], 0Fh [7:0], 10h [7:0]	HT160A: 001021h (4129d) HT120A: 000C21h (3105d)	The vertical period VP is VP[23:0] + 1. By default, VP is 4130 and 3160 for HT160A and HT120A respectively.
HP[15:0]	One RCK period	11h [7:0], 12h [7:0]	HT160A: 023Fh (575d) HT120A: 023Fh (575d)	The horizontal period HP is HP[15:0] + 1. By default, HP is 576 for both HT160A and HT120A.

Frame Rate and Output Data Rate

The following tables list the default settings of internal reference clock frequency, vertical and horizontal scanning period and data rate. When it is necessary to adjust frame rate according to the requirement of a specific application, instead of horizontal period, it is recommended to adjust the vertical period or internal reference clock frequency.

Table 20. Frame rate and output data rate for HT160A

A/D conversion resolution	Number of Serial LVDS channels	Frame rate [fps]	Data rate [Gbps]	Number of active pixels		Total number of all data[Note 1]		Number of **INCLK** in 1H	
				H	V	H	V	37.125 MHz	-
14	16	46.82	12.474	4112	4112	4608	4130	192	-
	8	31.21	8.316					288	-
	4	15.61	4.158					576	-
12	16	46.82	10.692					192	-
	8	36.41	8.316					246.9	-
	4	18.21	4.158					493.7	-
10	16	46.82	8.91					192	-
	8	43.7	8.316					205.7	-
	4	21.84	4.158					411.4	-
8	16	46.82	7.128					192	-
	8	46.81	7.128					192	-
	4	27.31	4.158					329.1	-

Note 1. including sync code and blank.

Table 21. Frame rate and output data rate for HT120A

A/D conversion resolution	Number of Serial LVDS channels	Frame rate [fps]	Data rate [Gbps]	Number of active pixels		Total number of all data[Note 1]		Number of **INCLK** in 1H	
				H	V	H	V	37.125 MHz	-
14	16	62.25	12.474	4112	3088	4608	3106	192	-
	8	41.5	8.316					288	-
	4	20.75	4.158					576	-
12	16	62.25	10.692					192	-
	8	48.42	8.316					246.9	-
	4	24.21	4.158					493.7	-
10	16	62.25	8.910					192	-
	8	58.1	8.316					205.7	-
	4	29.05	4.158					411.4	-
8	16	62.25	7.128					192	-
	8	62.25	7.128					192	-
	4	36.31	4.158					329.1	-

Note 1. including sync code and blank.

Image Data Output Format

Pixel Read Out Order

As shown in the Figure 2 and Figure 3, in default mode, the vertical scanning direction is from bottom to top, the horizontal scanning direction is from left to right.

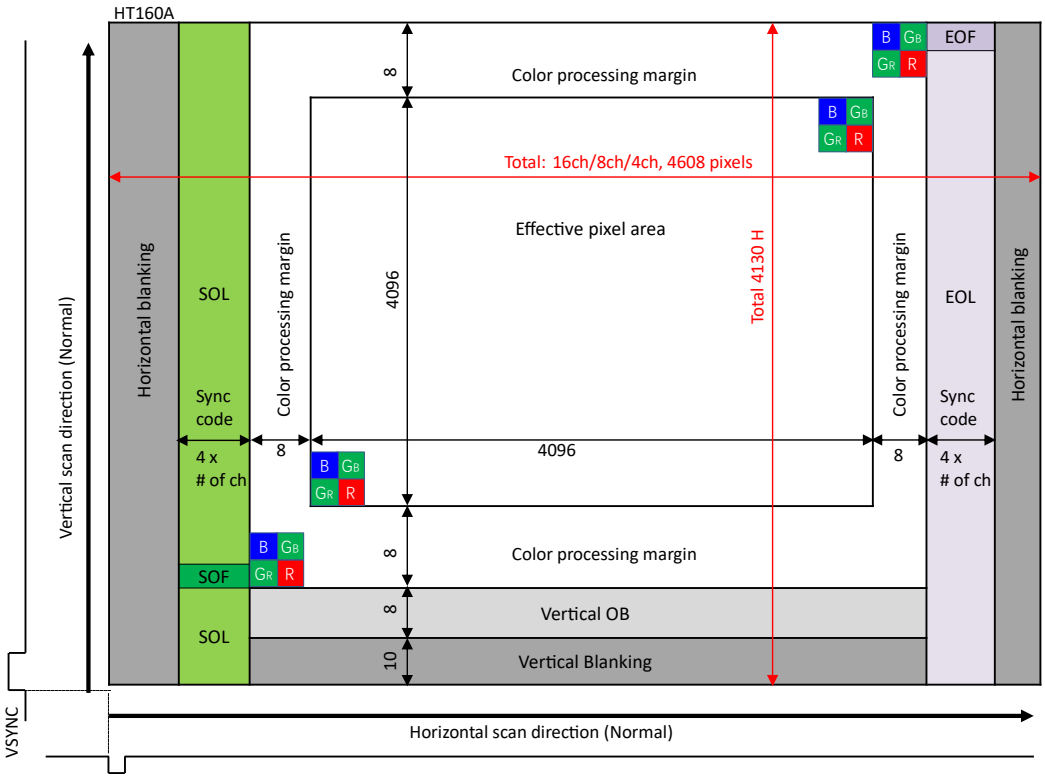


Figure 18. HT160A Image drawing of output data format

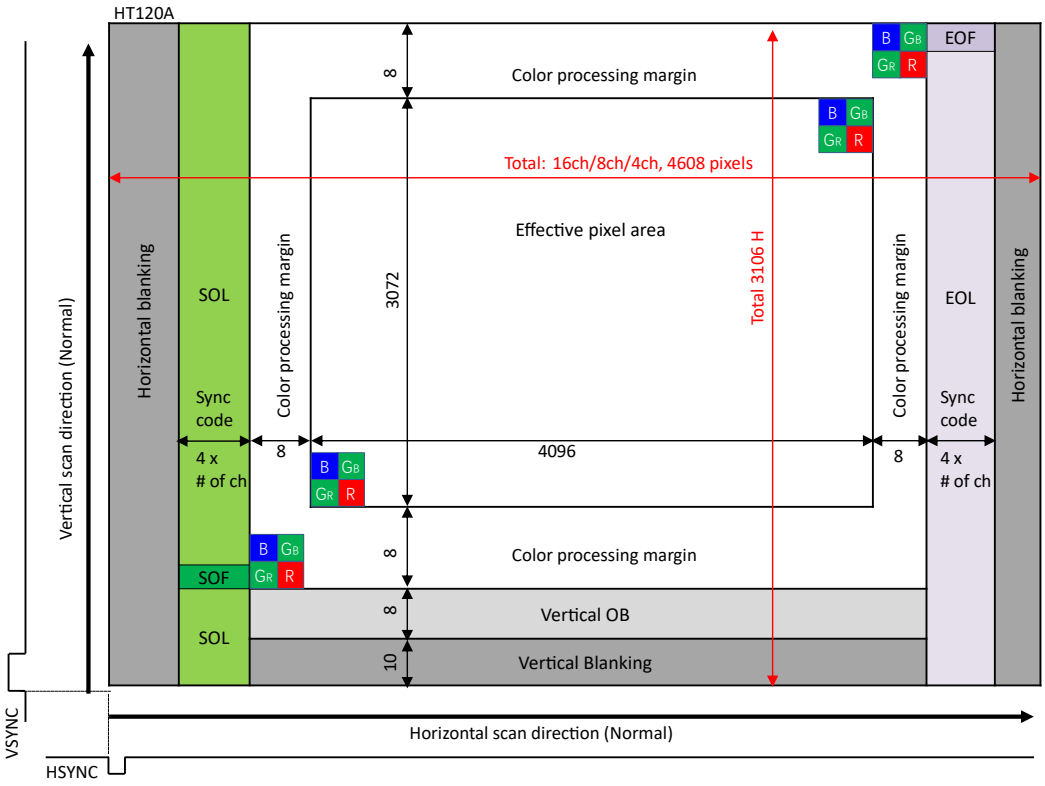


Figure 19. HT120A Image drawing of output data format

Image Output Data Format

Image output data include sync codes, pixel data, vertical blanking (VBLANK) and horizontal blanking (HBLANK). Figure 18 and Figure 19 are image drawings of output data format for HT160A and HT120A respectively. The data need to capture are enclosed by sync codes.

There are four types of sync code, SOF, SOL, EOL and EOF.

SOF, start of frame. SOF will be at the start of the first line when a new frame starts.

SOL, start of line. SOL will be at the start of each line (except the first line).

EOL, end of line. EOL will be at the end of each line (except the last line).

EOF, end of frame. EOF will be at the end of the last line of one frame, which indicates the end of one frame.

Please find details in Table 22, Table 23, Table 24 and Table 25.

Figure 20 and Figure 21 show data output sequence from each LVDS pairs.

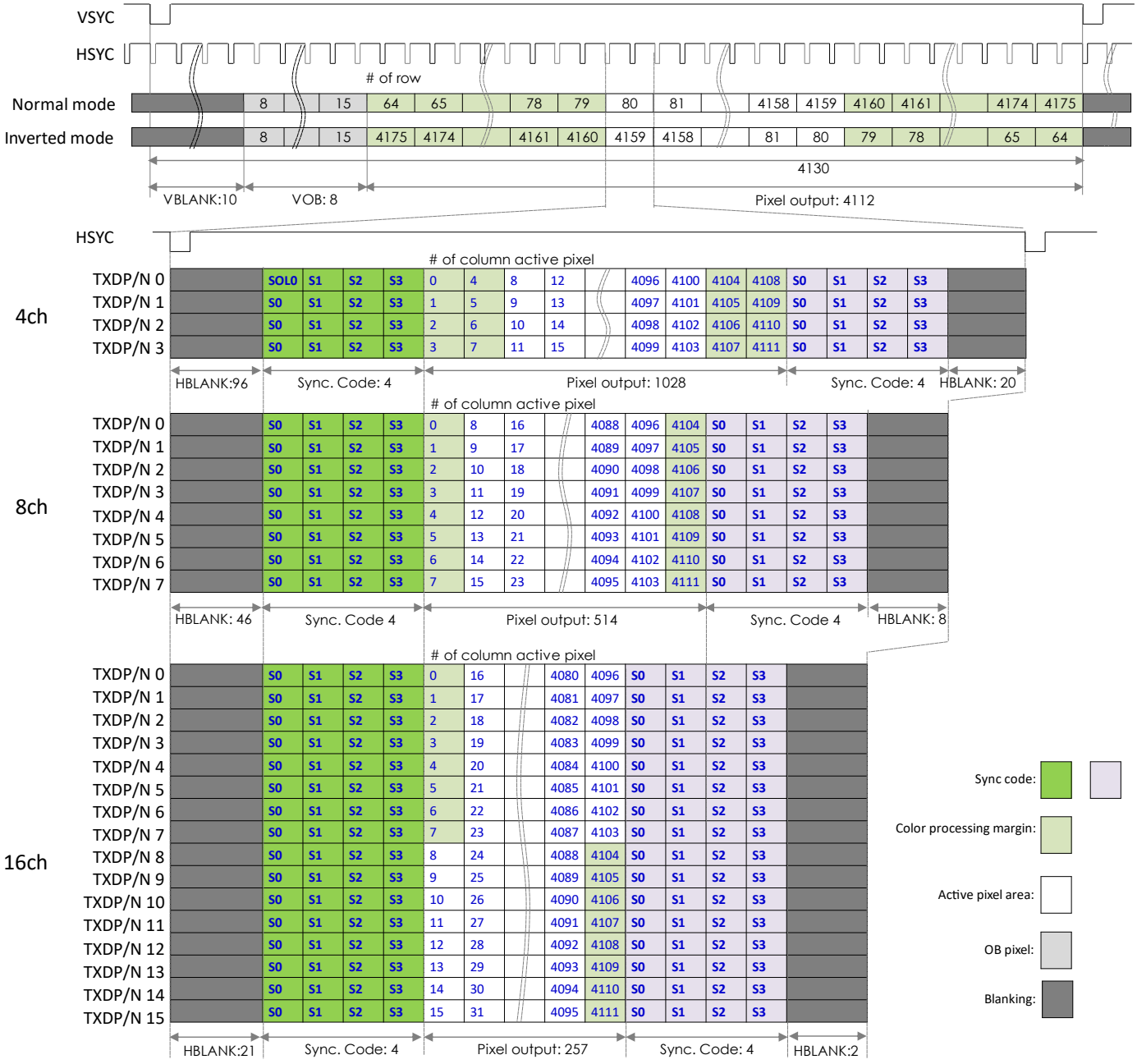


*Figure 20. **HT160A** LVDS channels output data sequence in normal mode*

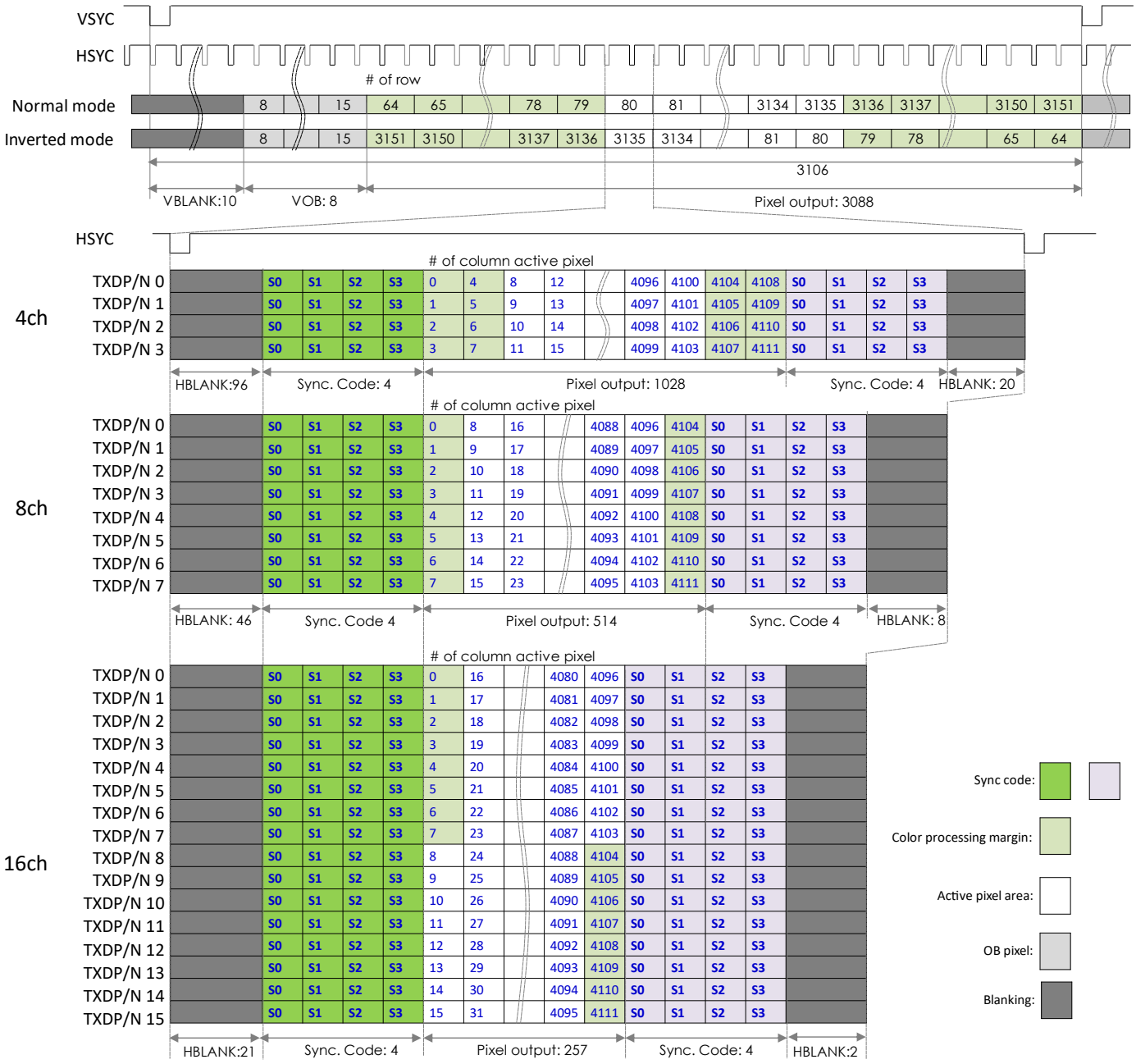


*Figure 21. **HT120A** LVDS channels output data sequence in normal mode*

Sync Code

Each sync code has 4 words (1 word has same data width of a pixel data) as list in the following tables, from Table 22 to Table 25. By default, the sync codes are as listed in Table 22. Please note only the last word is designated to be different between the sync codes.

The sensors support multi-frame WDR (Wide Dynamic Range) mode. By default, WDR mode is disabled, and can be enabled by setting WDR_EN register to high level. In WDR mode, sync codes of N consecutive frames automatically switch between N sets of sync codes (Sync Code 0, Sync Code 1, Sync Code 2 and Sync Code 3).

N is the number of frames in the WDR mode and is set by WDR_MODE register,
when WDR_MODE = 00b, N=2,
when WDR_MODE = 01b, N=3 and
when WDR_MODE = 10b or 11b, N=4.
Please refer to **WDR mode** for details.

Table 22. Sync code 0

Symbol	Output Bit-Width	Sync Code 0			
		SOL	EOL	SOF	EOF
S0	8	FFh	FFh	FFh	FFh
	10	3FFh	3FFh	3FFh	3FFh
	12	FFFh	FFFh	FFFh	FFFh
	14	3FFFh	3FFFh	3FFFh	3FFFh
S1	8	00h	00h	00h	00h
	10	000h	000h	000h	000h
	12	000h	000h	000h	000h
	14	0000h	0000h	0000h	0000h
S2	8	00h	00h	00h	00h
	10	000h	000h	000h	000h
	12	000h	000h	000h	000h
	14	0000h	0000h	0000h	0000h
S3	8	**80h**	**9Dh**	**ABh**	**B6h**
	10	**200h**	**274h**	**2ACh**	**2D8h**
	12	**800h**	**9D0h**	**AB0h**	**B60h**
	14	**2000h**	**2740h**	**2AC0h**	**2D80h**

*Note: S0, the 1st word; S1, the 2nd word; S2, the 3rd word; S3, the 4th word.

Table 23. Sync code 1

Symbol	Output Bit-Width	Sync Code 1			
		SOL	EOL	SOF	EOF
S0	8	FFh	FFh	FFh	FFh
	10	3FFh	3FFh	3FFh	3FFh
	12	FFFh	FFFh	FFFh	FFFh
	14	3FFFh	3FFFh	3FFFh	3FFFh
S1	8	00h	00h	00h	00h
	10	000h	000h	000h	000h
	12	000h	000h	000h	000h
	14	0000h	0000h	0000h	0000h
S2	8	00h	00h	00h	00h
	10	000h	000h	000h	000h
	12	000h	000h	000h	000h
	14	0000h	0000h	0000h	0000h
S3	8	**81h**	**A1h**	**AFh**	**B9h**
	10	**204h**	**284h**	**2BCh**	**2E4h**
	12	**810h**	**A10h**	**AF0h**	**B90h**
	14	**2040h**	**2840h**	**2BC0h**	**2E40h**

Table 24. Sync code 2

Symbol	Output Bit-Width	Sync Code 2			
		SOL	EOL	SOF	EOF
S0	8	FFh	FFh	FFh	FFh
	10	3FFh	3FFh	3FFh	3FFh
	12	FFFh	FFFh	FFFh	FFFh
	14	3FFFh	3FFFh	3FFFh	3FFFh
S1	8	00h	00h	00h	00h
	10	000h	000h	000h	000h
	12	000h	000h	000h	000h
	14	0000h	0000h	0000h	0000h
S2	8	00h	00h	00h	00h

	10	000h	000h	000h	000h
	12	000h	000h	000h	000h
	14	0000h	0000h	0000h	0000h
S3	8	**82h**	**A2h**	**AEh**	**BAh**
	10	**208h**	**288h**	**2B8h**	**2E8h**
	12	**820h**	**A20h**	**AE0h**	**BA0h**
	14	**2080h**	**2880h**	**2B80h**	**2E80h**

Table 25. Sync code 3

Symbol	Output Bit-Width	Sync Code3			
		SOL	EOL	SOF	EOF
S0	8	FFh	FFh	FFh	FFh
	10	3FFh	3FFh	3FFh	3FFh
	12	FFFh	FFFh	FFFh	FFFh
	14	3FFFh	3FFFh	3FFFh	3FFFh
S1	8	00h	00h	00h	00h
	10	000h	000h	000h	000h
	12	000h	000h	000h	000h
	14	0000h	0000h	0000h	0000h
S2	8	00h	00h	00h	00h
	10	000h	000h	000h	000h
	12	000h	000h	000h	000h
	14	0000h	0000h	0000h	0000h
S3	8	**83h**	**A3h**	**AFh**	**BBh**
	10	**20Ch**	**28Ch**	**2BCh**	**2ECh**
	12	**830h**	**A30h**	**AF0h**	**BB0h**
	14	**20C0h**	**28C0h**	**2BC0h**	**2EC0h**

Note:

WDR_MODE = 00b , sync codes switch between **Sync Code 0** and **Sync Code 1.**

WDR_MODE = 01b , sync codes switch between **Sync Code 0** and **Sync Code 1, Sync Code 2.**

WDR_MODE = 10b or 11b, sync codes switch between **Sync Code 0** and **Sync Code 1, Sync Code 2, Sync Code 3.**

LVDS Data Bit Output Order

The output data bit width (DBW) can be selected from 14-bit, 12-bit, 10-bit or 8-bit using register BS[1:0] (address C0h, bit [1:0]), please refer to Table 13 for details. The on-chip ADC resolution does not change accordingly to DBW width settings, when DBW setting is changed, the upper bits of setting number are picked and sent out as shown in following figure.

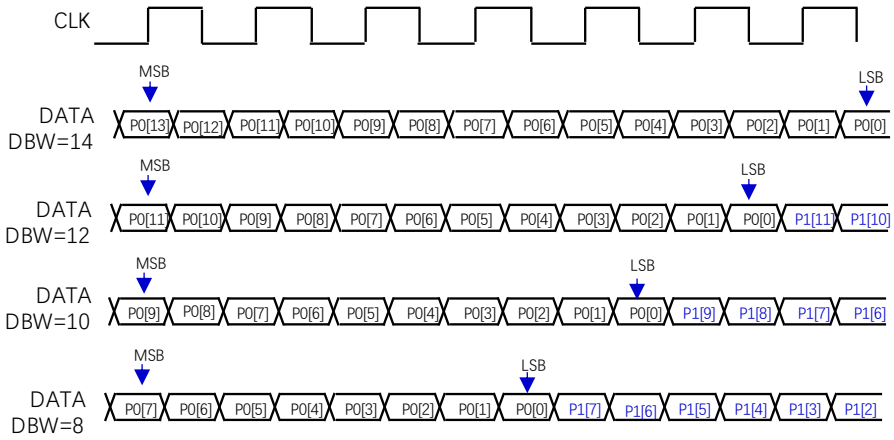


Figure 22. Output Data Bit Output Order

Exposure Time Adjustment

The sensors operate in a charge-domain global shutter mode. Each pixel has a memory node for charge storage during read-out period. During the global charge transfer period, all pixels move the charges in the photo diode to its own memory node. Then the charge will be stored in the memory node until be read out row by row.

Internal Expsoure Time Control Mode

In internal exposure time control mode, the exposure time is determined by registers. This mode is available for both master mode and slave mode.

The charge transfer period, read out period and exposure time etc. are shown in the following figure.

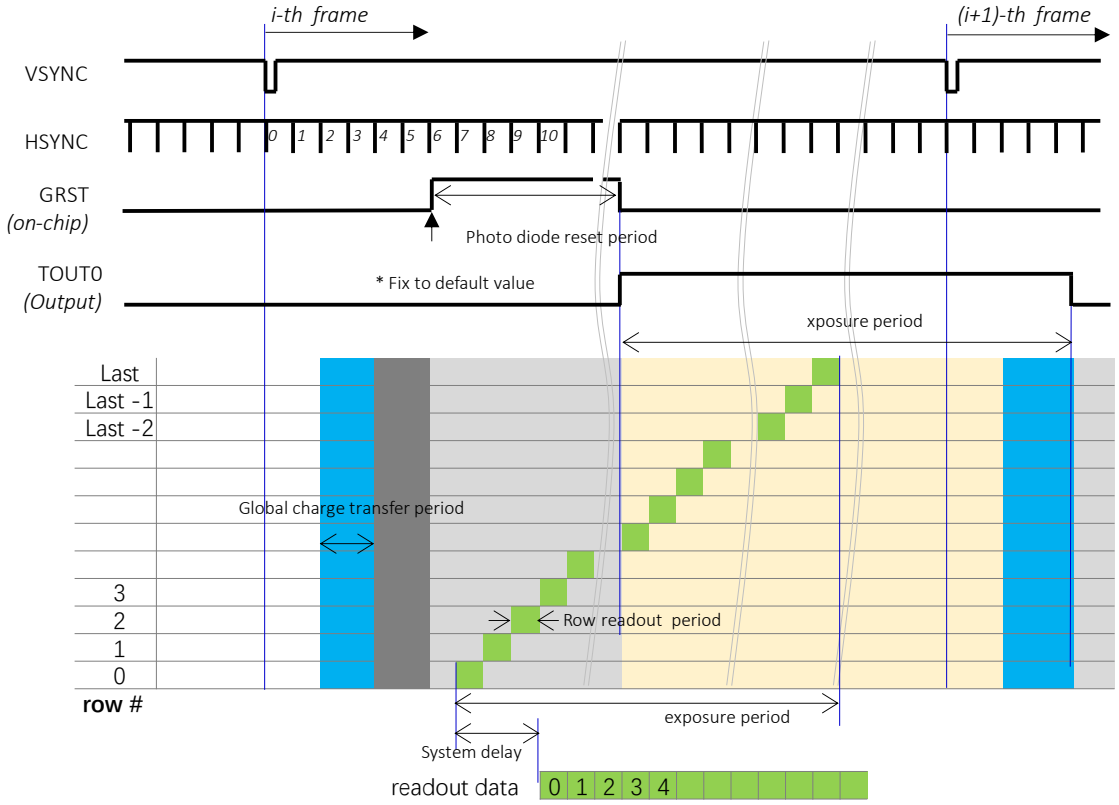


Figure 23.Timing diagram of internal exposure time control

The exposure time is determined by the position of the width of GRST (respect to pulse of VSYNC). The register settings and exposure time calculation is explained as following.

The width of GRST:

GRSTW[23:0], register 16h, bit [7:0]; 17h, bit [7:0]; 18h, bit [7:0], default value: 000001h(1d)

unit: one horizontal scanning period

Exposure time calculation:

The exposure time is the vertical period, VP, minus the width of GRST pulse, GRSTW.

Exposure time = VP - 2 - GRSTW

unit: one horizontal scanning period

*Please note, this is a rough calculation, if more precious calculation is preferred, please ask for technical support. As shown in the figure, the output pin TOUT0 is high during exposure period roughly indicates the start and end position of the exposure period.

External Exposure Time Control Mode

The exposure time can be also controlled by input pulse from pin TRGEXP. This mode is only available in TRIGEXP mode. The exposure period, charge transfer period and read out period etc. are shown in the following figure.

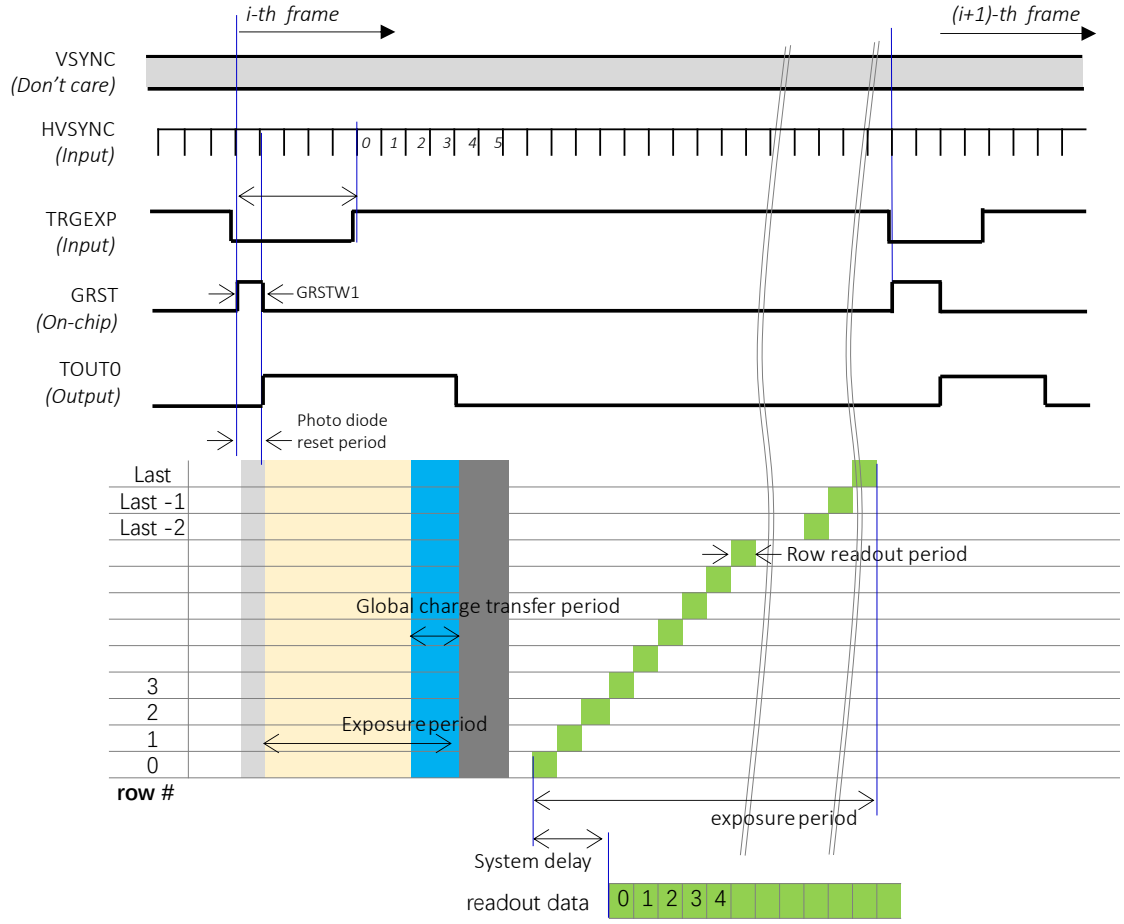


Figure 24.Timing diagram of external exposure time control

The exposure period is not the same with the internal control mode, it is determined by the low-level pulse width of TRGEXP, the width of GRST and the charge transfer period, where the latter two parameters are set by registers.

GRST width:

GRSTW1[3:0], register 2Eh, bit [7:4], default value: 2h(2d).
unit: one horizontal scanning period
Please note GRSTW1 is different from GRSTW.

Exposure time calculation:

The exposure time is calculated by the following equation,
Exposure time = TRGEXPW + 3 – GRSTW1
unit: one horizontal scanning period
where, TRGEXPW is the low-level pulse width of TRGEXP and "3" stands for the additional time including charge transfer period, which is setting by internal register settings.

*Please note, as the internal exposure timing control, this is a rough calculation, if more precious calculation is preferred, please ask for technical support.
As shown in the figure, the output pin TOUT0 is high during exposure period roughly indicates the start and end position of the exposure period.

Various Function Description

Windowing

The sensors support vertical multi-ROI windows but do not support overlap windows. When a smaller number of rows need to read out, vertical windowing can achieve higher frame rate. Please ask technical support for details.

Gain

Programmable gain control consists of analog gain and digital gain control, the total of analog gain and digital gain can be set up to 48dB by register settings.

Analog Gain

The pixel signal is amplified by a programmable gain amplifier before input to ADC (Analog-to-Digital Converter). The gain of 1(0dB), 2(6dB) ,4(12dB) ,8(18dB) and 16(24dB) are available.

Table 26. Register setting of analog gain

Register name	Address and bit	Default value	Setting value and gain
PGAGAIN_T[5:0]	94h bit [5:0]	2Fh	Analog gain of odd columns. 2Fh: 1x, 37h: 2x, 3Bh: 4x, 3Dh: 8x, 3Eh: 16x
PGAGAIN_B[5:0]	93h bit [5:0]	2Fh	Analog gain of even columns. 2Fh: 1x, 37h: 2x, 3Bh: 4x, 3Dh: 8x, 3Eh: 16x

Digital Gain

The digital signal that shows the value of pixel signal is amplified in digital region before serializer and LVDS. The range of gain is 0~24dB by steps of 0.1dB.

Table 27. Register setting of digital gain

Register name	Address and bit	Default value	Setting value	Gain
OUTDGAIN[7:0]	B7h bit [7:0]	00h	00h~F0h (0d~240d)	Gain(dB) = Setting value in decimal/10

Test Pattern

The sensors can output a gray scale test pattern as shown below. The pixel array is horizontally divided into 15 blocks, each block has different output as listed in the following table. Please note, when DWB is less than 14, the upper bits will be output.

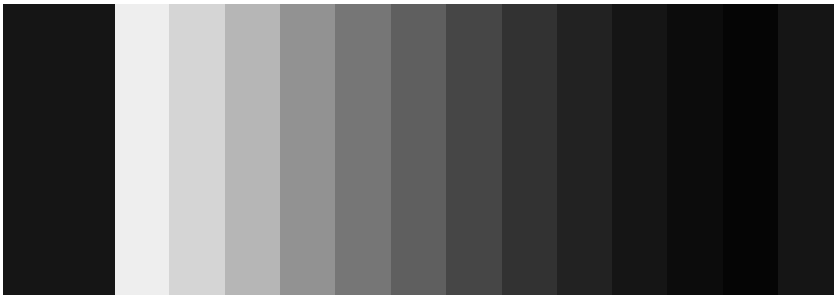


Figure 25.Gray scale test pattern output

Table 28. Register settings for gray scale test pattern output

Register name	Address	Default value	Setting value
-	A0h	24h	25h
-	A4h	93h	83h

Table 29. Pixel array output of gray scale chart

Block	1 Note 1	2	3	4	5	6	7	8
Output (decimal)	2949	2949	15237	13599	11633	9339	7537	6062
Output (Hex)	B85h	B85h	3B85h	351Fh	2D71h	247Bh	1D71h	17AEh

Block	9	10	11	12	13	14	15	
Output (decimal)	4424	3113	2130	1311	655	328	2949	
Output (Hex)	1148h	C29h	852h	51Fh	28Fh	148h	B85h	

Note 1. Most left block.

LVDS Receiver Training Code Output

The sensors can send fixed pattern code for the purpose of LVDS receiver training. The register settings are shown as below.

Table 30. Register setting of LVDS receiver training

Register name	Address and bit	Default value	Setting value
OUTTRNEN	BFh bit [6]	0b	0b: Training code output disable 1b: Training code output enable
OUTTRN[13:0]	BFh bit [5:0], C0h bit [7:0]	070Fh	Training code. Change the default value if needed.
OUTSYNC_EN	BFh bit [7]	1b	0b: Sync code output disable. 1b: Sync code output enable. In case sync code is not necessary, set to 0b.

Vertical/Horizontal Binning

The sensors support vertical 2-pixel FD (Floating Diffusion) binning mode and horizontal 2-pixel binning mode.

With vertical 2-pixel FD binning mode, because half rows to read out, it results in almost double frame rate. Please note, this mode will not increase the dynamic range.

With horizontal binning mode, outputs of 2 pixels are added or averaged which depends on register settings. Horizontal binning mode cannot increase frame rate, only decrease LVDS data rate.

Vertical/Horizontal Sub-sampling

The sensors support vertical/horizontal 1/2 and 1/4 sub-sampling mode.

With vertical 1/2 sub-sampling mode, because half rows to read out, it results in almost double frame rate, meanwhile, since same number of rows to read out, the horizontal 1/2 sub-sampling mode cannot increase frame rate.

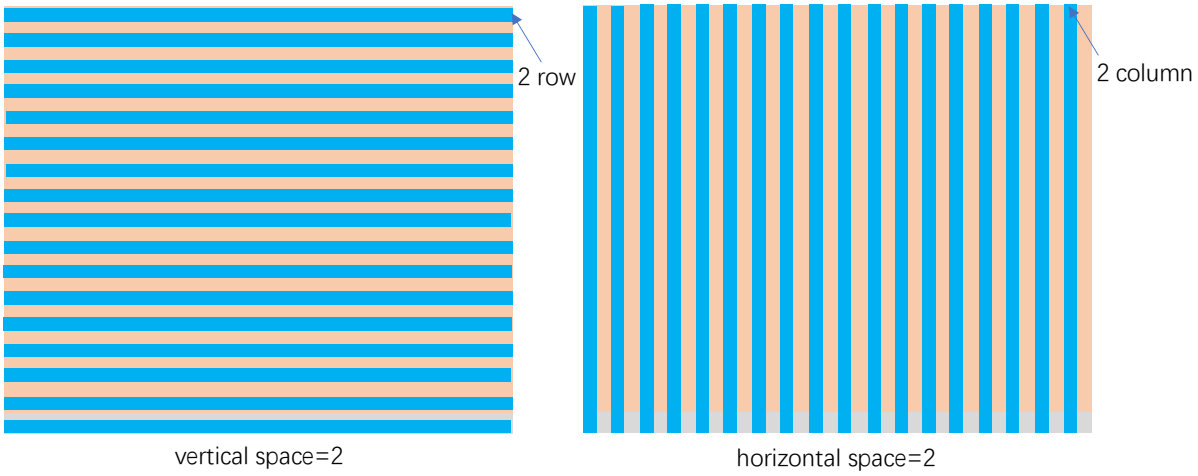


Figure 26. Vertical/Horizontal 1/2 sub-sampling mode

With vertical 1/4 sub-sampling mode, because 1/4 rows to read out, it results in almost fourfold frame rate, meanwhile, since same number of rows to read out, the horizontal 1/4 sub-sampling mode cannot increase frame rate.

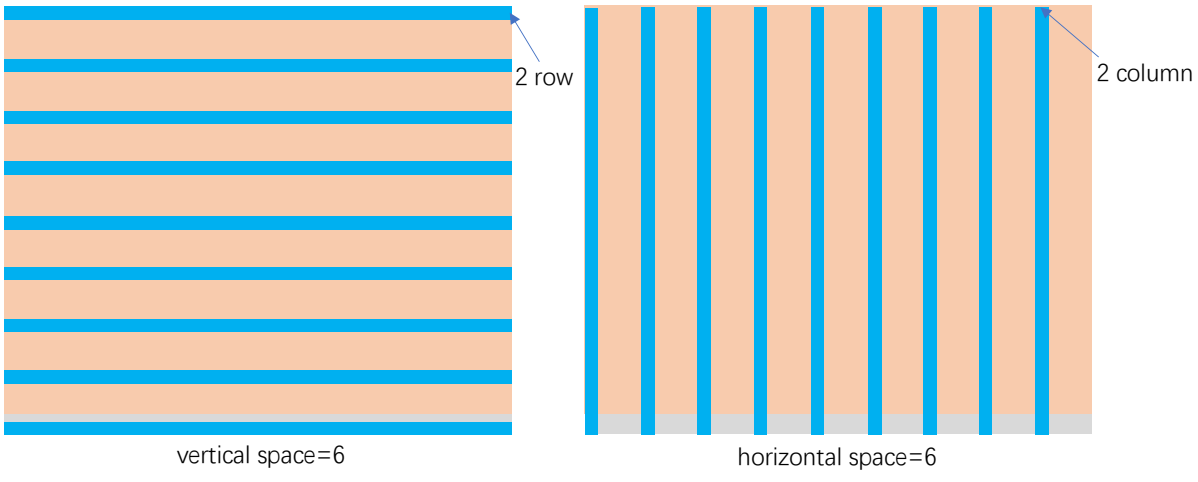


Figure 27. Vertical/Horizontal 1/4 sub-sampling mode

WDR mode

The sensors support multi-frame WDR (Wide Dynamic Range) mode by allowing different exposure times for several continuous frames. The external ISP (Image Signal Processor) can combine these frames of various exposure times to generate a wide dynamic range image.

WDR mode exposure times are calculated as following:

Exposure time 0 = VP- 2- GRSTW
Exposure time 1 = VP- 2- GRSTW_WDR1
Exposure time 2 = VP- 2- GRSTW_WDR2
Exposure time 3 = VP- 2- GRSTW_WDR3
unit: one horizontal period

The registers are listed as follows:

GRSTW[23:0], register 16h bit [7:0], 17h bit [7:0], 18h bit [7:0], default value: 000001h(1d)
GRSTW_WDR1[23:0], register 2Fh bit [7:0], 30h bit [7:0], 31h bit [7:0], default value: 0003E8h(1000d)
GRSTW_WDR2[23:0], register 32h bit [7:0], 33h bit [7:0], 34h bit [7:0], default value: 0007D0h(2000d)
GRSTW_WDR3[23:0], register 35h bit [7:0], 36h bit [7:0], 37h bit [7:0], default value: 000BB8h(3000d)
unit: one horizontal period

Table 31. Registers for WDR mode controlling

Register name	Address and bit	Default value	Setting value
WDR_EN	2Eh bit [2]	0b	0b: WDR disable 1b: WDR enable
WDR_MODE	2Eh bit [1:0]	0h	0h: 2-frame WDR mode, exposure time switches between exposure time 0 and 1. 1h: 3-frame WDR mode, exposure time switches between exposure time 0, 1 and 2. 2h: 4-frame WDR mode, exposure time switches between exposure time 0, 1, 2 and 3.

Digital offset

Table 32. Register for Digital offset

Register name	Address and bit	Default value	Setting value
OFFSET	B5h bit [6:0], B6h bit [7:0]	0000h	T.B.D

Digital saturation clip and Black-sun Clip

The digital saturation clip levels are set by the registers in Table 33, both upper level and lower level can be set separately. The sensors can detect black-sun pixels, by default, their outputs will be forced to a black-sun saturation level, BS_SAT[13:0], which is usually set to the same value with normal saturation level.

Table 33. Register for digital saturation clip

Register name	Address and bit	Default value	note
OUTCLIP_EN	B8h bit [6]	1b	By default, the output saturation clip is enabled.
OUTSATH[13:0]	B8h bit [5:0], B9h bit [7:0]	3F00h (16128d)	-
OUTSATL[13:0]	BAh bit [5:0], BBh bit [7:0]	0001h	-
BSCLIP_EN	BCh bit [6]	1b	By default, the black-sun saturation clip is enabled.
BS_SAT[13:0]	BCh bit [5:0], BDh bit [7:0]	3F00h (16128d)	-

Power-On Sequence

It is recommended to turn on the power supplies by the order of 1.8V(VDD18 and VDD18L), 1.2V and 3.3V.

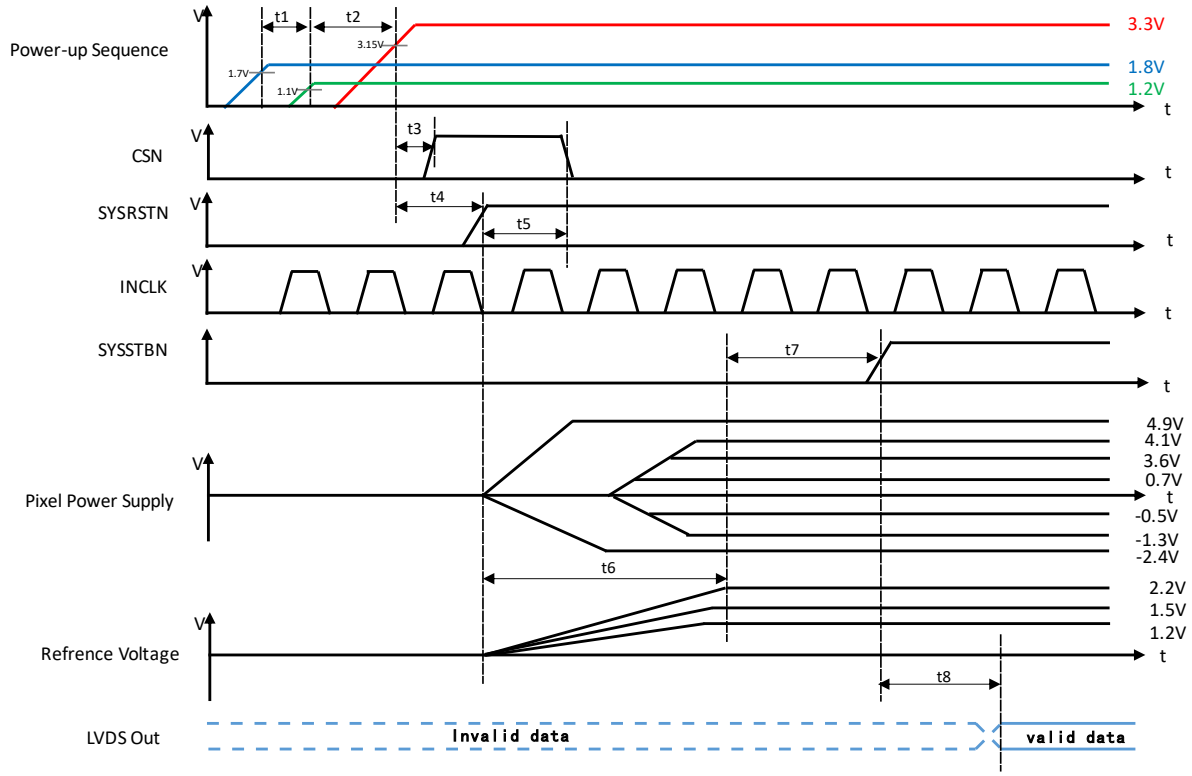


Figure 28. Power-on sequence

Table 34. Power-on sequence parameters

Symbol	min	unit	note
t1	0	ms	-
t2	0	ms	-
t3	0	us	-
t4	0.5	us	The time from external power-on to reset release
t5	20	us	Internal reset releasing time
t6	20	ms	Internal power on time
t7	0	us	Stand-by period before operation
t8	8	frame	The time from the stand-by release to valid data output.

Spectrum Response

T.B.D.

Package

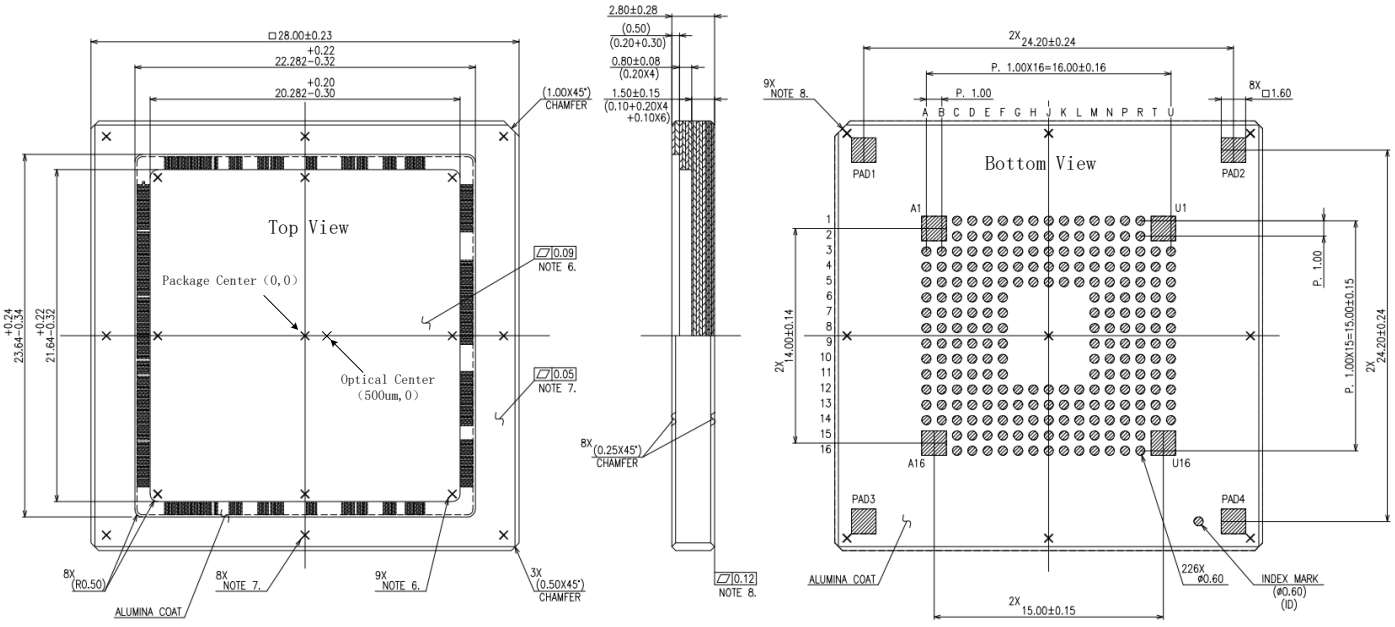


Figure 29. Detail of package

Note: Optical center is not the same with package center.

Document History

Version	Date	Description	Author
0.1	2020/08/19	New release	
0.5	2020/10/19	Update	
0.6	2020/12/18	Modify Input Reference Clock and Clock System and Image Output Data Format	
0.7	2021/10/25	Revision. 1. Figure 2, Figure 3, revised 2. Delete figure 4 and figure 5 in Ver. 0.6 3. Table 3, revised. 4. Figure 10, Table 8, revised. 4. Internal Register Access - Figure 12, minor change - Table 10, correct typos 5. Register Reflection Timing, revised. 6. Update Frame Rate and Output Data Rate 7. Revised Image Output Data Format - delete figure 20, figure23 to figure 26 in Ver. 0.6 - revised figure 21 in Ver 0.6 and divide to Figure 18 and Figure 19 in Ver. 0.7 - revised figure 21 in Ver 0.6 and divide to Figure 20 and Figure 21 in Ver. 0.7 8. Delete Example Data Output of One LVDS Pair 9. Revise Exposure Time Adjustment 10. Revised Various Function Description - Added details on WDR mode - Added Digital offset and Digital saturation clip and Black-sun Clip 11. revised Package - add optical center.	yxb