Analyzer Report {Dataflow}

This report generated by Convolutional Neural Network Inference Analyzer (CNN-IA) to summarize the analysis needed to reach the optimal dataflow exploration for mlp_fc3_batch16 using restricted schedule space.

Memory Architecture:

	L0	L1	L2
Capacity	16	16384	536870912
Access cost	0.05	3.84	200.0
Static cost	0.0	0.0	0.0
Parallel count	256	1	1
Parallel mode	1	0	0
Parallel cost	2.0	0.0	0.0

Precision : 16
Minimum utilization : 0.0%
Outputs can be buffered by MAC : 0
Replication to improve utilization : True

Glossary:

- Memory Levels : (L0, L1, L2)
  The smallest index the nearest to CPU.

- Loop Notations : (FX, FY, OX, OY, OC, IC, ON)

FX : FILTER WIDTH
FY : FILTER HEIGHT
OX : OUTPUT WIDTH
OY : OUTPUT HEIGHT
OC : OUTPUT CHANNEL
IC : INPUT CHANNEL
ON : BATCH

OC, IC [cost: 33050440.0pJ, utilization: 0.09765625%]

Loop Blocking (factors):

	L0	L1	L2
FX	1.0	1.0	1.0
FY	1.0	1.0	1.0
OX	1.0	1.0	1.0
OY	1.0	1.0	1.0
OC	2.0	1.0	25.0
IC	4.0	25.0	1.0
ON	1.0	16.0	1.0

Loop Partitioning (units):

	L0	L1	L2
FX	1.0	1.0	1.0
FY	1.0	1.0	1.0
OX	1.0	1.0	1.0
OY	1.0	1.0	1.0
OC	5.0	1.0	1.0
IC	5.0	1.0	1.0
ON	1.0	1.0	1.0

Loop Ordering (from the innermost):

	L0	L1	L2
FX	6.0	6.0	6.0
FY	6.0	6.0	6.0
OX	6.0	6.0	6.0
OY	6.0	6.0	6.0
OC	0.0	6.0	0.0
IC	1.0	1.0	6.0
ON	6.0	0.0	6.0

OC, ON [cost: 32071160.0pJ, utilization: 0.078125%]

Loop Blocking (factors):

	L0	L1	L2
FX	1.0	1.0	1.0
FY	1.0	1.0	1.0
OX	1.0	1.0	1.0
OY	1.0	1.0	1.0
OC	2.0	1.0	25.0
IC	1.0	500.0	1.0
ON	4.0	1.0	1.0

Loop Partitioning (units):

	L0	L1	L2
FX	1.0	1.0	1.0
FY	1.0	1.0	1.0
OX	1.0	1.0	1.0
OY	1.0	1.0	1.0
OC	5.0	1.0	1.0
IC	1.0	1.0	1.0
ON	4.0	1.0	1.0

Loop Ordering (from the innermost):

	L0	L1	L2
FX	6.0	6.0	6.0
FY	6.0	6.0	6.0
OX	6.0	6.0	6.0
OY	6.0	6.0	6.0
OC	0.0	6.0	0.0
IC	6.0	0.0	6.0
ON	1.0	6.0	6.0

IC, ON [cost: 32079160.0pJ, utilization: 0.15625%]

Loop Blocking (factors):

	L0	L1	L2
FX	1.0	1.0	1.0
FY	1.0	1.0	1.0
OX	1.0	1.0	1.0
OY	1.0	1.0	1.0
OC	1.0	250.0	1.0
IC	4.0	1.0	25.0
ON	2.0	1.0	1.0

Loop Partitioning (units):

	L0	L1	L2
FX	1.0	1.0	1.0
FY	1.0	1.0	1.0
OX	1.0	1.0	1.0
OY	1.0	1.0	1.0
OC	1.0	1.0	1.0
IC	5.0	1.0	1.0
ON	8.0	1.0	1.0

Loop Ordering (from the innermost):

	L0	L1	L2
FX	6.0	6.0	6.0
FY	6.0	6.0	6.0
OX	6.0	6.0	6.0
OY	6.0	6.0	6.0
OC	6.0	0.0	6.0
IC	0.0	6.0	0.0
ON	1.0	6.0	6.0

Optimal cost

[b: blocking factor, p: partitioning unit]

MEM - L2:
for (OC, 25b, 1p)

MEM - L1:
for (IC, 500b, 1p)

MEM - L0:
for (ON, 4b, 4p)
for (OC, 2b, 5p)
spatially unrolled loops: (OC)(ON)

Optimal utilization

MEM - L2:
for (IC, 25b, 1p)

MEM - L1:
for (OC, 250b, 1p)

MEM - L0:
for (ON, 2b, 8p)
for (IC, 4b, 5p)
spatially unrolled loops: (IC)(ON)