Analyzer Report {Dataflow}

This report generated by Convolutional Neural Network Inference Analyzer (CNN-IA) to summarize the analysis needed to reach the optimal Dataflow for mlp_fc3_batch16 using restricted schedule space.

Memory Architecture :

	L0	L1	L2
Capacity	16	16384	536870912
Access cost	0	3	200
Static cost	0	0	0
Parallel count	256	1	1
Parallel mode	1	0	0
Parallel cost	2	0	0

Precision	:	16
Minimum utilization	:	0.0%
Outputs can be buffered by mac	:	0
Replication to improve utilization	:	True

Glossary :

- Memory Levels : (L0, L1, L2)
  The smallest index the nearest to CPU.

- Loop Notations : (FX, FY, OX, OY, OC, IC, ON)

FX	:	FILTER WIDTH
FY	:	FILTER HEIGHT
OX	:	OUTPUT WIDTH
OY	:	OUTPUT HEIGHT
OC	:	OUTPUT CHANNEL
IC	:	INPUT CHANNEL
ON	:	BATCH

OC, IC

[cost: 33050440.0pJ, utilization: 0.09765625%]

Loop Blocking (factors):

	L0	L1	L2
FX	1	1	1
FY	1	1	1
OX	1	1	1
OY	1	1	1
OC	2	1	25
IC	4	25	1
ON	1	16	1

Loop Partitioning (units):

	L0	L1	L2
FX	1	1	1
FY	1	1	1
OX	1	1	1
OY	1	1	1
OC	5	1	1
IC	5	1	1
ON	1	1	1

Loop Ordering (from the innermost):

	L0	L1	L2
FX	6	6	6
FY	6	6	6
OX	6	6	6
OY	6	6	6
OC	0	6	0
IC	1	1	6
ON	6	0	6

OC, ON   [cost: 32071160.0pJ, utilization: 0.078125%]

Loop Blocking (factors):

	L0	L1	L2
FX	1	1	1
FY	1	1	1
OX	1	1	1
OY	1	1	1
OC	2	1	25
IC	1	500	1
ON	4	1	1

Loop Partitioning (units):

	L0	L1	L2
FX	1	1	1
FY	1	1	1
OX	1	1	1
OY	1	1	1
OC	5	1	1
IC	1	1	1
ON	4	1	1

Loop Ordering (from the innermost):

	L0	L1	L2
FX	6	6	6
FY	6	6	6
OX	6	6	6
OY	6	6	6
OC	0	6	0
IC	6	0	6
ON	1	6	6

IC, ON

[cost: 32079160.0pJ, utilization: 0.15625%]

Loop Blocking (factors):

	L0	L1	L2
FX	1	1	1
FY	1	1	1
OX	1	1	1
OY	1	1	1
OC	1	250	1
IC	4	1	25
ON	2	1	1

Loop Partitioning (units):

	L0	L1	L2
FX	1	1	1
FY	1	1	1
OX	1	1	1
OY	1	1	1
OC	1	1	1
IC	5	1	1
ON	8	1	1

Loop Ordering (from the innermost):

	L0	L1	L2
FX	6	6	6
FY	6	6	6
OX	6	6	6
OY	6	6	6
OC	6	0	6
IC	0	6	0
ON	1	6	6

Optimal cost

MEM - L2:
    for (OC, 25b, 1p)

MEM - L1:
    for (IC, 500b, 1p)

MEM - L0:
    for (ON, 4b, 4p)
       for (OC, 2b, 5p)
spatially unrolled loops: (OC)(ON)

Optimal utilization

MEM - L2:
    for (IC, 25b, 1p)

MEM - L1:
    for (OC, 250b, 1p)

MEM - L0:
    for (ON, 2b, 8p)
       for (IC, 4b, 5p)
spatially unrolled loops: (IC)(ON)