EDA for Nanoelectronics

Project 1

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1 Introduction

The metal oxide semiconductor field effect transistors (MOSFETs) are among the most common components used in analog and digital electronic circuits. These voltage-controlled field effect transistors are suitable for several applications, as they enable rapid switching, minimal power consumption, and high-density capacity [1].

Traditionally, the electric behaviour of MOSFETs is defined by the Shockley Model, which predicts the generated current as function of the applied voltage in three different performance regions: cut-off, linear and saturation.

However, modern technology industries demand the manufacture of smaller electronic products and devices, which require complex MOSFET topologies. This trend – also known as miniaturization – is based on the improvement of heat and mass transfer, and presents various advantages [2]:

- Smaller transistors and interconnections lead to an overall capacitance reduction, which enables the usage of higher frequency signals;
- Miniaturized MOSFET circuits operate at a lower input voltage and, therefore, decrease energy consumption;
- Cost reduction, by manufacturing more transistors per chip.

Notwithstanding the obvious benefits, the reduction of MOSFET's channels to the nanoscale introduces non-ideal effects that the Shockley model does not account for, such as the velocity saturation effects of carriers at this scale [3]. Therefore, the performance of short channel length MOSFETs continues to be difficult to describe mathematically.

The motivation behind this report is to test the scalability of the Shockley model by simulating two n-type MOSFETs with different dimensions and then fitting the data to the model in question. By analysing the respective relative errors, it will be possible to conclude how the miniaturization of the MOSFETs affects the model. Additionally, an alternative of this model, known as N-power model, will be briefly studied in this project and compared to Shockley's, accordingly.

2 Models

In this study, two different models will be evaluated and compared: the Shockley model (conventionally adopted in most literature) and the n-power model. Regarding both models, the main distinction to be tested in this project is the electric behaviour in the saturated region (discussed in more detail in Section 4).

2.1 Shockley model

The Shockley model is commonly used to describe the behaviour of a MOSFET with long channel length (L), according to its working region: when the voltage between the gate and the source is low, no current will flow in the device; when this voltage surpasses a certain value (known as the threshold voltage), the current is no longer null, and is influenced by various factors, such as the drain and gate biases. This is mathematically described by the set of equations (1), adapted from [4].

$$I_D = \begin{cases} 0 & ,V_{GS} \leq V_T : \text{cutoff region} \\ K\left[(V_{GS} - V_T) - 0.5V_{DS}^2\right] & ,V_{GS} > V_T \wedge V_{DS} < V_{DSat} : \text{linear region} \\ 0.5K(V_{GS} - V_T)^2 & ,V_{GS} > V_T \wedge V_{DS} \geq V_{DSat} : \text{saturation region} \end{cases} \tag{1}$$

V_{GS} is the voltage defined between the gate and the source of the MOSFET, V_{DS} is the voltage between the drain and source, V_T is the threshold voltage (represents the gate bias at which the conductive channel is formed between the source and the drain of the transistor) and $V_{Sat} = V_{GS} - V_T$. K is a drivability factor, defined by equation (2), where μ is the charge mobility, ϵ_{ox} is the dielectric constant of the the gate oxide, t_{ox} is the oxide thickness, W is the channel width and L_{eff} is the effective channel length.

$$K = \mu \frac{\epsilon_{ox}}{t_{ox}} \frac{W}{L_{eff}} \tag{2}$$

The physical chain of events that characterizes each MOSFET region of operation are as follows:

- Cutoff region: The gate bias is not sufficient to form an inversion region (channel through which current can pass between source and drain terminals) and therefore the the device is OFF.
- Linear region: The inversion region is formed, as the gate bias surpasses its threshold value, and the electrons in the semiconductor flow, due to the electric field formed in the material. The drain current increases significantly as the gate bias rises.
- Saturation region: As the gate bias increases, the potential difference between the drain and gate terminals is reduced and the number of electrons in the inversion region near the drain decreases.

When this region becomes very narrow, the drain current saturates (pinch-off) and becomes independent of the drain bias.

2.2 N-Power model

The N-power model, adapted from [4], is an alternative to the Shockley model that aims to predict the electrical behavior of the MOSFET. This model takes into account the effect of the saturation rate of charge carriers, by testing the reliability of the quadratic nature of the Shockley model in the saturated region, as represented in equation (3).

$$I_D = K(V_{GS} - V_T)^n \tag{3}$$

Where V_{GS}, V_T, I_D and K are the same variables as in the Shockley model and n defines the exponent ($n = 2$ in the previous model). Similarly to the previous model, $I_D = 0$ in the cutoff region.

3 Methodology for parameter evaluation

The methodology adopted in this report can be divided in two section: the simulation of two differently sized NMOS devices, followed by the analysis of the results and the attainment of the electric parameters of the models.

The given specifications for the MOSFETs and respective circuits polarization are:

- 65 nm Technology
- $L_{eff} = 48nm$
- $V_{DD} = 1.1V$
- $W = 2L$

As previously mentioned, two different geometries will be analysed: $L = 1.5L_{eff} = 72nm \wedge W = 144nm$ and $L = 3L_{eff} = 144nm \wedge W = 288nm$. It is important to note that the physical length of the channel (L) is not the same as the effective channel length (L_{eff}), that defines the size of region near the semiconductor-isolator interface, in which the inversion zone is controlled by the gate voltage.

3.1 LTspice simulation

The MOSFETs were integrated into a circuit and simulated in the software *LTspice*. This resulted in a set of data that demonstrates the I-V interdependence in the device.

Figure 1 shows the schematics and simulation parameters for obtaining the transfer characteristics (fig. 1 a)) and for the output characteristics (fig. 1 b)). In Appendix no.1, it is possible to find the characteristics of the NMOS model, that were transfered from *NanoHub* [5], and incorporated in the schematics, by employing the *SPICE .inc* directive. In this layout, the '*Vdd*' source is connected to the drain and source terminals of the NMOS, so it is safe to conclude that $V_{DS} = V_{DD}$. Similarly, V_{GS} is defined by the voltage source, '*Vgs*'. Moreover, the bulk of the MOSFET is connected to the source/ground, eliminating the possibility of body-effect.

Figure 1 a) shows the simulation command for a DC sweep of V_{GS}, from 0V to 1V, with a step of 0.01V. In this case, V_{DD} is constant and equal to 1.1V. This schematic can provide the I_D and V_{GS} values, necessary for plotting the transfer characteristics, $I_D(V_{GS})$, and the transconductance curves, $\frac{\delta I_D}{\delta V_{GS}}(V_{GS})$. By defining these simulation commands and respective parameter variances, the transistor is only operational in the cutoff and saturation regions, as $V_{GS} \in [0,1]$V and $V_{DS} = 1.1V$, and therefore $V_{DS} > (V_{GS} - V_T)$ (the threshold voltage is positive in enhancement mode NMOS).

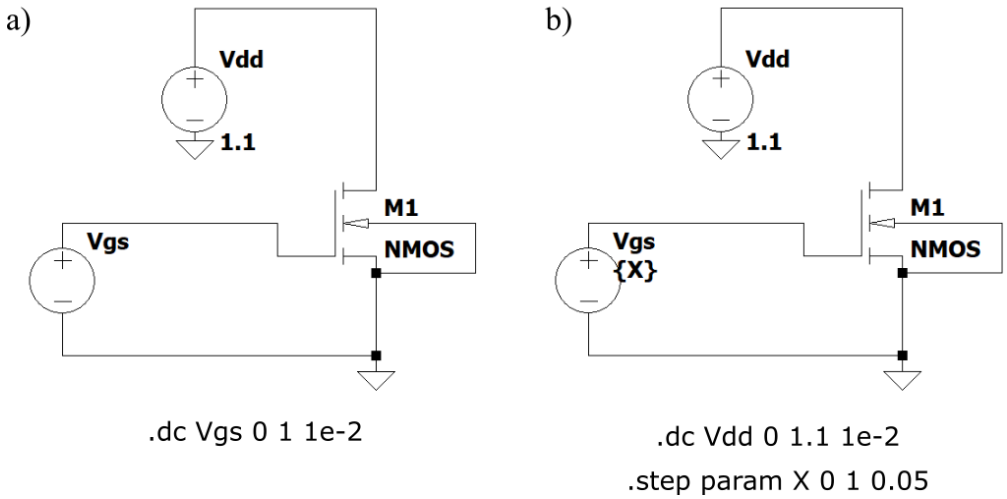

Figure 1: Schematics for obtaining a) the transfer characteristic and transconductance, and b) the output characteristic

Figure 1 b) shows the simulation command for a DC sweep of V_{DD}, from 0V to 1.1V, with a step of 0.01V and a parameter sweep of V_{GS}, from 0V to 1V, with a step of 0.05V. This allows the program to overlay simulation results and obtain the output curves for different gate biases.

3.2 Shockley model approximation

Following the simulation of the two transistors, the resulting data was analysed in *Python*, by running the code in Appendix no.2. This code will be interpreted in this section.

The following steps are inserted in a '*for*' cycle, to be repeated for both transistors, $L = 1.5L_{eff}$ and $L = 3L_{eff}$ (as written in lines 11 and 12 of the code).

In order to analyse the simulation data, it is necessary to load it into a *DataFrame*, by reading the .txt files extracted from LTspice. After importing the *pandas* package, the files are read by line 14 of the code, by employing the command '*pd.read_csv*'.

After the insertion of the data, the relevant variables are defined as *numpy arrays*, in lines 15 and 16: '*Vgs*' contains the gate-source voltage values, in volts, and '*Id*' holds the current flowing through the MOSFETs, in amps. These values are then plotted, as lines 18 to 23 detail, resulting in the transfer characteristics of the MOSFETs.

The following step consists in defining the Shockley function and then fitting the data accordingly, in order to extract the parameters V_T and K. The quadratic function is defined in lines 25 and 26. As previously mentioned, the polarization of the circuit in figure 1 ensures that the MOSFET is only operational in the cutoff and saturations regions; therefore, this function can be reduced to equation (4).

$$I_D = \begin{cases} 0 & ,V_{GS} < V_T : \text{cutoff region} \\ K(V_{GS} - V_T)^2 & ,V_{GS} \geq V_T : \text{saturation region} \end{cases} \tag{4}$$

As such, the function in lines 25 and 26 takes the input parameters V_{GS}, V_T and K and returns the results of equation (4) (the distinction between cutoff and saturation regions is executed by the command '*np.piecewise*').

Lines 29 to 31 carry out the extraction of the Shockley model parameters, by inserting the previous function in a *scipy.optimize.curve_fit* function, which fits the input data (V_{GS} and I_D) and returns the most adequate model parameters, V_T and K. As to facilitate the convergence of the function to the most physically correct local minimum values, these parameters are initially set to $K = 10^{-4} AV^{-2}$ and $V_T = 0.3V$ (this value corresponds to an approximation of the most likely threshold voltage, according to the tranfer characteristics, as later explained in section 4).

The next phase consists in plotting the Shockley model transfer curve with the previously obtained parameters (lines 37 to 40), as well as its relative error, according to equation (5) (lines 67 and 71 to 78).

$$\text{Relative error} = \frac{\left| I_D - I_{D,model} \right|}{I_D} \tag{5}$$

Where $I_{D,model}$ is an array that contains the current values returned by the model function.

3.3 N-power model approximation

Identically to the Shockley model, the data is fitted to the n-power model by employing the same packages and similar functions.

The model function, defined in lines 42 and 43, takes the input parameters V_{GS}, V_T, K and n and returns equation (3), in saturation regime, and 0 when in cutoff regime.

Lines 46 to 49 extract the model parameters, V_{GS}, V_T, K and n, by making use of the *curve_fit* function, as previously explained. The initial values set for these parameters are $V_T = 0.3V$, $K = 10^{-4} AV^{-2}$ and $n = 2$.

Lines 56 to 64 plot the Shockley model transfer curve with the found parameters, and its relative error, according to equation (5), is calculated and plotted in lines 68 and 81 to 88.

4 Results

After writing the script and extracting the model parameters, it is necessary to analyse the results and to reach conclusions regarding the applicability of the Shockley and n-power models for short channel MOSFETs.

4.1 Transfer Characteristics: Simulation and Models

4.1.1 Shockley Model Parameters

The fitted parameters for both MOSFET are in table 1. The threshold voltages of the transistors are close to 0V, presenting a negative value for $L = 1.5L_{eff}$. Considering an NMOS in enhancement mode, the threshold value ought to be positive, which is the first indication that the model is not a correct depiction of the electrical behaviour of the device. The values of K seem to be consistent.

Table 1: Shockley model parameters for MOSFET channel lengths $L = 1.5L_{eff}$ and $L = 3L_{eff}$.

	$L = 1.5L_{eff}$	$L = 3L_{eff}$
$V_T\,[V]$	-0.00917	0.08467
$K\left[AV^{-2}\right]$	0.00014	0.00024

Figure 2 shows the transfer characteristics of the two MOSFETs, as well as the fitted Shockley model plots. An initial analysis of the collected data points to the fact that, despite the parameter fitting, the Shockley model approximation is evidently not suitable for the saturation regions, and the threshold voltages from table 1 do not coincide with the end of the cutoff zones of the NMOS, as the fitted curves return significant drain current at much lower gate biases than the simulation results. Once again, this suggests that the Shockley model is not proper for short channel MOSFETs.

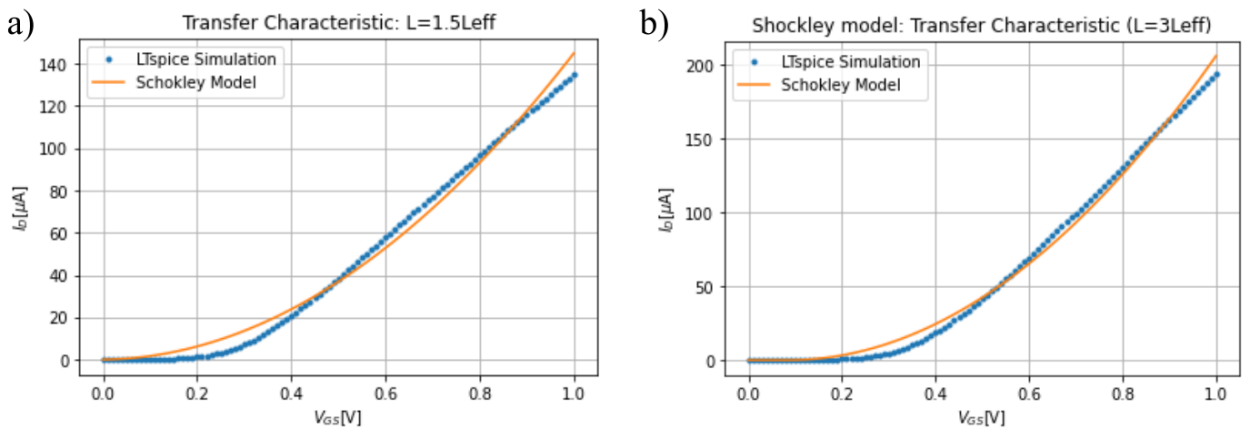

Figure 2: Transfer Characteristic curves for NMOS transistors with channel length equal to a) $L = 1.5L_{eff}$ and b) $L = 3L_{eff}$, and corresponding Shockley model curve approximation.

Furthermore, by observing the shape of the simulation plots, it is possible to conclude that the real threshold is around 0.3V for both MOSFETs, as the current begins to rise significantly at this value; this does not match the extracted values from table 1, showing a substantial discrepancy for the shortest channel device, $L = 1.5L_{eff}$.

An overall observation of figure 2 points to a key difference in the plots: the data extracted from LTspice does not seem to follow a quadratic function in the saturation zone, as it ensues a behaviour nearly linear.

Figures 3 a) and c) show the relative errors of the Shockley model for $L = 1.5L_{eff}$ and $L = 3L_{eff}$, respectively, which seem to be consistently lower for the latter.

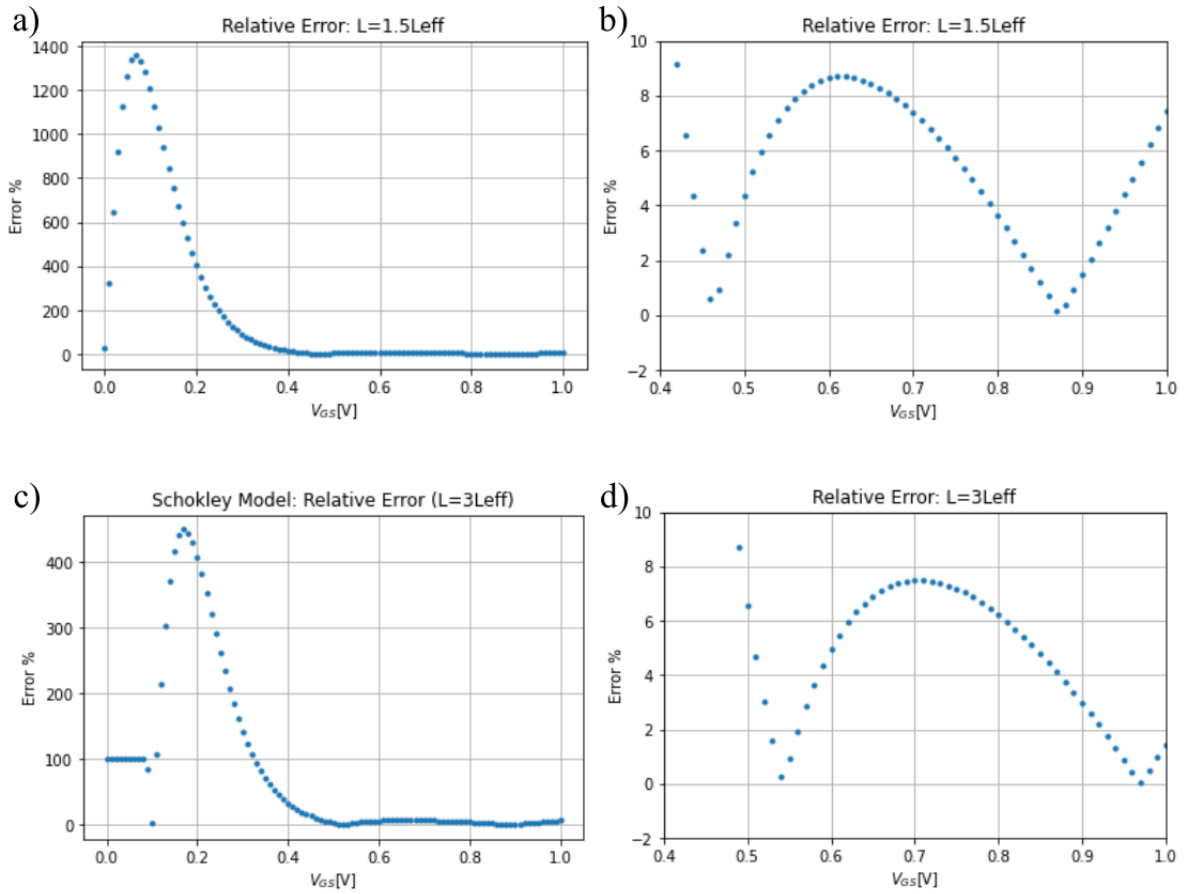

Figure 3: Relative error of the Shockley model, relative to the data attained by simulation, for an NMOS with channel length equal to a), b) $L = 1.5L_{eff}$ and c), d) $L = 3L_{eff}$.

The graphs in figure 3 illustrate a significant upsurge for gate bias within the values of $[0.0, 0.3]\,V$, up to around 1400% (not only due to how inadequate the model is, but also to how low the current is, which, by equation 4, increases the relative error significantly); beyond these values, figures b) and d) show relative errors consistently lower than 10%. The oscillation of the error curve in the saturation region is due to the linearity of the data curve and its incompatibility with the quadratic nature of the

Shockley model.

Once more, these error spectra show the inadequacy of the model, particularly for the transistor with shorter channel length.

4.1.2 N-power Model Parameters

The resulting n-model parameters are in table 2. The threshold values are $V_T = 0.24909V$ and $V_T = 0.28571V$, for the shortest and longest channels, respectively, which are much closer to the value previously assumed from the LTspice data plot, $V_T \approx 0.3V$, when compared to the previous model, $V_T \approx 0V$. As predicted, the exponents are $n \approx 1$, which are a more accurate depiction of the saturation regions in the transfer characteristic curves. The shortest channel NMOS suffered a more significant difference in the exponent variable between the two models (from $n = 2$ to $n \approx 1.14$), which reflects how the Shockley model fails the scalability test.

Table 2: N-power model parameters for MOSFET channel lengths $L = 1.5L_{eff}$ and $L = 3L_{eff}$.

	$L = 1.5L_{eff}$	$L = 3L_{eff}$
$V_T\,[V]$	0.24909	0.28571
$K\left[AV^{-2}\right]$	0.00019	0.00030
n	1.13763	1.26412

Figure 4 shows the transfer characteristic curves of the transistors and respective n-power model fit with the parameters from table 2.

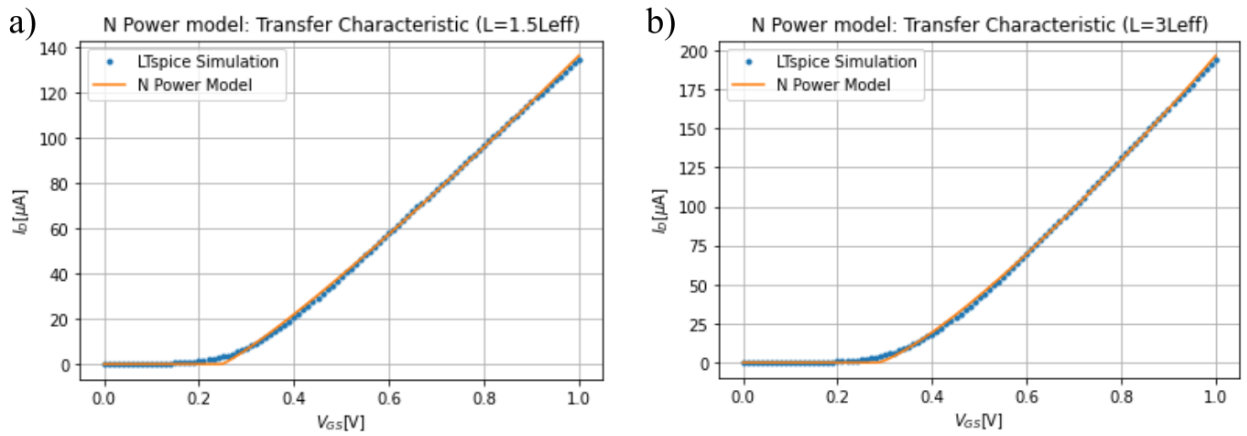

Figure 4: Transfer Characteristic curves for NMOS transistors with channel length equal to a) $L = 1.5L_{eff}$ and b) $L = 3L_{eff}$, and corresponding n-power model curve fitting.

The graphs from fig. 4 reveal a good approximation of the model to the simulated values in the cutoff and saturation operating regions, for both channel lengths. However, it is possible to see slight differences between plots in the transition region, from the cutoff zone to the saturation zone. These dispari-

ties result from the fact that the model considers, as previously discussed, a nearly linear approximation through the exponent $n \approx 1$ which, for regions where $V_{GS} \approx V_T$, leads to an abrupt change between the two operating regions.

Figures 5 a) and b) show the relative errors of the n-power model for $L = 1.5L_{eff}$ and $L = 3L_{eff}$, respectively, which seem to be identical, and consistently lower than the errors obtained for the Shockley model, in figure 3.

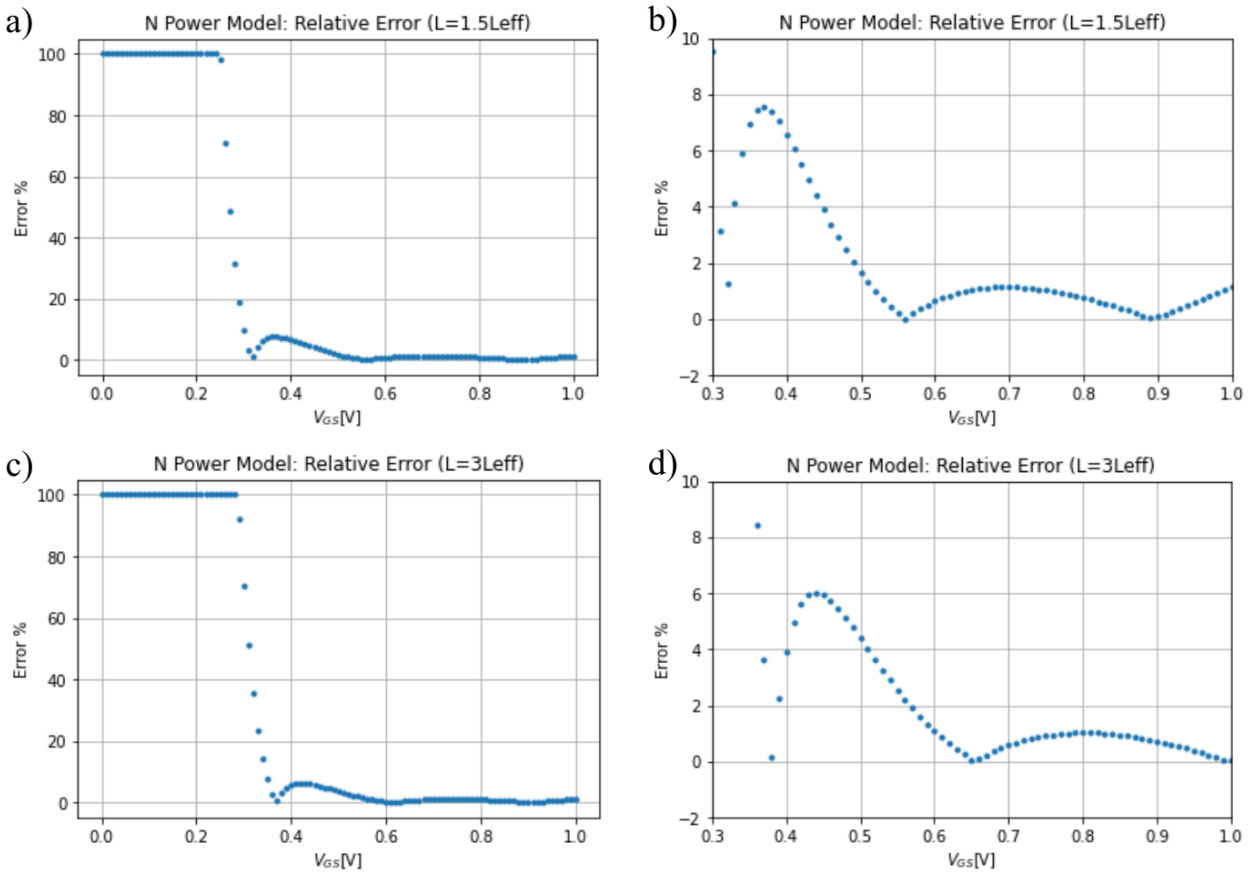

Figure 5: Relative error of the n-power model, relative to the data attained by simulation, for an NMOS with channel length equal to a), b) $L = 1.5L_{eff}$ and c), d) $L = 3L_{eff}$.

In order to interpret the graphs in figure 5, it is important to note that an error of 100% does not necessarily depict a significant inconsistency between the model and the simulation data, as supported by the results in figure 4. In this case, the relative error is high in the cutoff regions of both transistor curves because $I_D = 0A$; referring back to equation (5), this leads to an error equal to 100%, up to $V_{GS} \approx V_T$. Moreover, when the gate bias is $V_{GS} \geq 0.6V$, the relative error is below 2%. Both these regions show improvements when compared to the Shockley model. However, the n-power model presents its highest relevant error (around 8% in fig 5 b) and 6% in fig 5 d)) in the transition zone, between cutoff and saturation regions, as previously predicted.

The relative errors are less affected by the transistor's channel length in the n-power model (figure 5)

than in the Shockley model (figure 3).

4.2 Transconductance

The transconductance of a MOSFET defines the change in the drain current with respect to the change in gate voltage, whilst the drain bias remains constant. As such, it is a merit figure of the electrical behaviour of the device.

By simulating the schematic in figure 1 a), it was possible to extract the data relative to the transconductance for both transistors, a) $L = 1.5L_{eff}$ and b) $L = 3L_{eff}$, seen in figure 6. The transconductance increases significantly along with the gate bias, as the inversion zone begins to form, between $V_{GS} = 0.2V$ and $V_{GS} = 0.4V$, around the real threshold voltage.

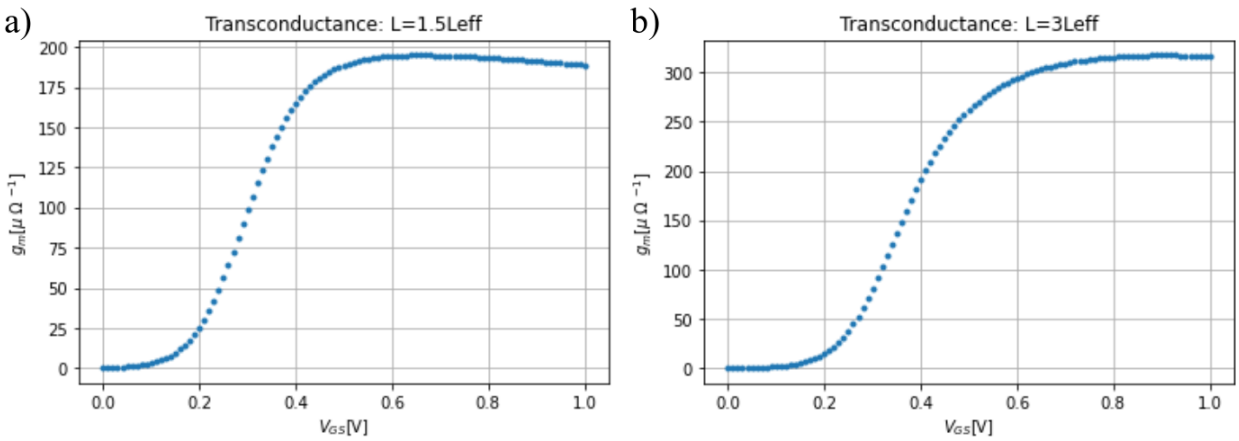

Figure 6: Transconductance as function of gate bias, for an NMOS with channel length equal to a) $L = 1.5L_{eff}$ and b) $L = 3L_{eff}$.

In MOSFETs, as V_{GS} increases, the electrical field along the channel reaches a critical value, the free carrier velocity tends to saturate and the mobility degrades, due to intensive electron scattering. This causes a reduction in channel conductance, which is reflected in the decline of the curves in figure 6. This decline is more distinct in the shortest channel transistor (fig. 6 a)), as it is more dominated by velocity saturation, as previously concluded in literature [3].

4.3 Output Characteristics

The output curves of transistors represent the output current as a function of the output voltage or, specifically, the electrical current in the drain as a function of the voltage drop between the drain and the source.

Figure 7 a) and b) show the output characteristic curves for the NMOS with channel length equal to $L = 1.5L_{eff}$ and $L = 3L_{eff}$, respectively. In these curves, I_D increases in value, due to a reduction

in the channel resistance as the drain bias increases, and then stabilizes, becoming nearly exclusively dependent on V_{GS}.

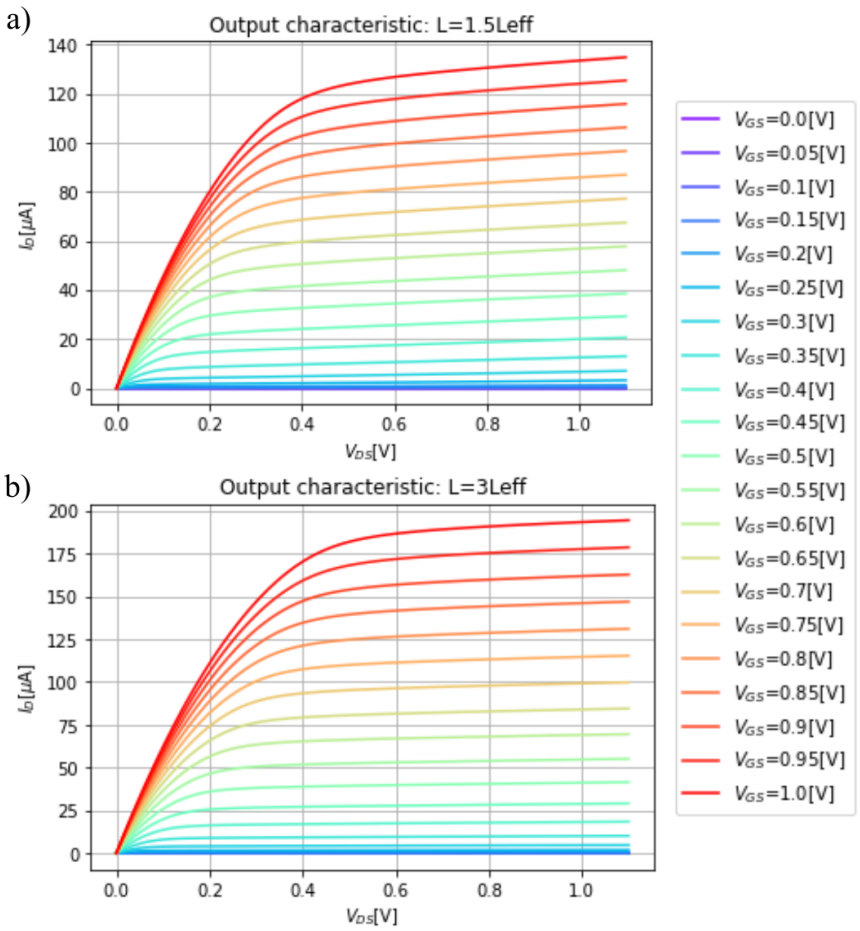

Figure 7: Output characteristic curves for NMOS with channel length equal to a) $L = 1.5L_{eff}$ and b) $L = 3L_{eff}$.

As V_{DS} increases and the NMOS saturates, the number of electrons in the inversion region decreases near the drain, due to pinch-off: both the gate and the drain are positively biased, the potential difference across the isolator is smaller near the drain end, which means the amount of negative charge in the semiconductor needed to preserve charge neutrality will also be smaller near the drain. The reduced number of carriers causes a reduction in the channel conductance, which is reflected in the smaller slope of the output characteristics as V_{DS} approaches V_{Dsat}. As the drain current saturates, it starts to lose its dependence on the drain bias.

5 Conclusions

The purpose of this project was to explore and compare the Shockley and the N-power models, in response to the inability of the former in predicting the electrical behavior of miniaturized transistors.

The strategy behind this project consisted in simulating the operation of two different sized n-type MOSFETs and approximating each model to the simulation results. This grants the opportunity to take conclusions regarding the scalability of each model.

The Shockley model is the most commonly used mathematical approximation for MOSFET characteristics, but the n-power model adds a degree of freedom to the function, which gives it an obvious advantage. As a result, the n-power model showed significant improvements, compared to Shockley's.

The results of Shockley's model approximation showed that the quadratic dependence on gate-source voltage is not suitable for these devices; furthermore, the fitted parameters (specifically V_T) were not physically plausible.

On the other hand, the approximation of the n-model resulted in congruent parameters, and the fitted transfer curve overlaid the simulation curve almost perfectly (with the exception of the transition between cutoff and saturation regions).

Additionally, the relative error graphs showed a significantly larger error in Shockley's approximation, throughout the gate bias increase, whilst the error of the n-power model was consistently low, for both NMOS.

In terms of scalability, the performance of the shortest channel MOSFET is considerably worse, according to the results attained by Shockley's fitting: the relative errors were higher for $L = 1.5L_{eff}$, as the calculation of the threshold voltage returned a negative value, which is an inane result. Such issue was not observed in the n-power model, as the characteristics showed identical behaviour, despite the channel length.

Overall, the purpose of this work was resolved, as it was possible to disclose both model performances and to parameterize the transistors, while also exposing the issues of the models in the face of modern electronics.

6 References

[1] C. C. Hu, *Modern Semiconductor Devices for Integrated Circuits*, 1st ed. Prentice Hall, 2009.

[2] "Miniaturized, High Performance, Energy-and-Area-Efficient Field-Effect Transistor Expands Computational Capability of Electronic Devices | KAUST Innovation." [Online]. Available: https://innovation.kaust.edu.sa/technologies/miniaturized-high-performance-energy-and-area-efficient-field-effect-transistor-expands-computational-capability-of-electronic-devices/

[3] G. W. Taylor, "Velocity-Saturated Characteristics of Short-channel MOSFETs," *ATT Bell Laboratories Technical Journal*, vol. 63, no. 7, 1984.

[4] T. Sakurai and A. Newton, "Alpha-power law mosfet model and its applications to cmos inverter delay and other formulas," *IEEE Journal of Solid-State Circuits*, vol. 25, no. 2, pp. 584–594, 1990.

[5] "nanoHUB.org - Simulation, Education, and Community for Nanotechnology." [Online]. Available: https://nanohub.org/

7 Appendix

7.1 Appendix no.1

In this section, it is possible to see the NMOS model inserted in the *LTspice* simulations.

```
* Customized PTM 65nm NMOS

.model  nmos  nmos  level = 54

+version = 4.0    binunit = 1    paramchk= 1    mobmod  = 0
+capmod  = 2      igcmod  = 1    igbmod  = 1    geomod  = 1
+diomod  = 1      rdsmod  = 0    rbodymod= 1    rgatemod= 1
+permod  = 1      acnqsmod= 0    trnqsmod= 0

* parameters related to the technology node
+tnom = 27    epsrox = 3.9
+eta0 = 0.0058    nfactor = 1.9    wint = 5e-09
+cgso = 1.5e-10    cgdo = 1.5e-10    xl = -3e-08

* parameters customized by the user
+toxe = 1.85e-09    toxp = 1.2e-09    toxm = 1.85e-09    toxref = 1.85e-09
+dtox = 6.5e-10    lint = -6.5e-09
+vth0 = 0.274    k1 = 0.363    u0 = 0.06127    vsat = 124340
+rdsw = 165    ndep = 1.39e+18    xj = 3.84e-08


* secondary parameters
+ll      = 0           wl      = 0           lln     = 1           wln     = 1
+lw      = 0           ww      = 0           lwn     = 1           wwn     = 1
+lwl     = 0           wwl     = 0           xpart   = 0
+k2      = 0.01        k3      = 0
+k3b     = 0           w0      = 2.5e-006    dvt0    = 1           dvt1    = 2
+dvt2    = -0.032      dvt0w   = 0           dvt1w   = 0           dvt2w   = 0
+dsub    = 0.1         minv    = 0.05        voffl   = 0           dvtp0   = 1.0e-009
+dvtp1   = 0.1         lpe0    = 0           lpeb    = 0
+ngate   = 2e+020      nsd     = 2e+020      phin    = 0
+cdsc    = 0.000       cdscb   = 0           cdscd   = 0           cit     = 0
+voff    = -0.13       etab    = 0
+vfb     = -0.55       ua      = 6e-010      ub      = 1.2e-018
+uc      = 0           a0      = 1.0         ags     = 1e-020
+a1      = 0           a2      = 1.0         b0      = 0           b1      = 0
+keta    = 0.04        dwg     = 0           dwb     = 0           pclm    = 0.04
+pdiblc1 = 0.001       pdiblc2 = 0.001       pdiblcb = -0.005      drout   = 0.5
+pvag    = 1e-020      delta   = 0.01        pscbe1  = 8.14e+008   pscbe2  = 1e-007
+fprout  = 0.2         pdits   = 0.08        pditsd  = 0.23        pditsl  = 2.3e+006
+rsh     = 5           rsw     = 85          rdw     = 85
+rdswmin = 0           rdwmin  = 0           rswmin  = 0           prwg    = 0
+prwb    = 6.8e-011    wr      = 1           alpha0  = 0.074       alpha1  = 0.005
+beta0   = 30          agidl   = 0.0002      bgidl   = 2.1e+009    cgidl   = 0.0002
+egidl   = 0.8

+aigbacc = 0.012       bigbacc = 0.0028      cigbacc = 0.002
+nigbacc = 1           aigbinv = 0.014       bigbinv = 0.004       cigbinv = 0.004
+eigbinv = 1.1         nigbinv = 3           aigc    = 0.012       bigc    = 0.0028
+cigc    = 0.002       aigsd   = 0.012       bigsd   = 0.0028      cigsd   = 0.002
+nigc    = 1           poxedge = 1           pigcd   = 1           ntox    = 1
```

```
+xrcrg1   = 12          xrcrg2   = 5
+cgbo     = 2.56e-011   cgdl     = 2.653e-10
+cgsl     = 2.653e-10   ckappas  = 0.03       ckappad = 0.03       acde    = 1
+moin     = 15          noff     = 0.9        voffcv  = 0.02

+kt1      = -0.11       kt11     = 0          kt2     = 0.022      ute     = -1.5
+ua1      = 4.31e-009   ub1      = 7.61e-018  uc1     = -5.6e-011  prt     = 0
+at       = 33000

+fnoimod  = 1           tnoimod  = 0

+jss      = 0.0001      jsws     = 1e-011     jswgs   = 1e-010     njs     = 1
+ijthsfwd= 0.01        ijthsrev= 0.001       bvs     = 10         xjbvs   = 1
+jsd      = 0.0001      jswd     = 1e-011     jswgd   = 1e-010     njd     = 1
+ijthdfwd= 0.01        ijthdrev= 0.001       bvd     = 10         xjbvd   = 1
+pbs      = 1           cjs      = 0.0005     mjs     = 0.5        pbsws   = 1
+cjsws    = 5e-010      mjsws    = 0.33       pbswgs  = 1          cjswgs  = 3e-010
+mjswgs   = 0.33        pbd      = 1          cjd     = 0.0005     mjd     = 0.5
+pbswd    = 1           cjswd    = 5e-010     mjswd   = 0.33       pbswgd  = 1
+cjswgd   = 5e-010      mjswgd   = 0.33       tpb     = 0.005      tcj     = 0.001
+tpbsw    = 0.005       tcjsw    = 0.001      tpbswg  = 0.005      tcjswg  = 0.001
+xtis     = 3           xtid     = 3

+dmcg     = 0e-006      dmci     = 0e-006     dmdg    = 0e-006     dmcgt   = 0e-007
+dwj      = 0.0e-008    xgw      = 0e-007     xgl     = 0e-008

+rshg     = 0.4         gbmin    = 1e-010     rbpb    = 5          rbpd    = 15
+rbps     = 15          rbdb     = 15         rbsb    = 15         ngcon   = 1
```

7.2 Appendix no.2

This section contains the code developed in *python*.

```
# -*- coding: utf-8 -*-
"""
Created on Mon Sep 26 15:28:35 2022

@author: Utilizador
"""
import numpy as np
from scipy.optimize import curve_fit
import matplotlib.pyplot as plt
import pandas as pd
run=['1.5Leff','3Leff']
for i in run:
#_____________transfer curve: data extraction and plotting_____________________
    transf=pd.read_csv('P1_transfer_charac_'+ i +'.txt',sep='\t')
    Vgs=np.array(transf['v2'])
    Id=np.array(transf['Id(M1)'])

    plt.figure()
    plt.plot(Vgs,Id*1e6,'.',label='LTspice Simulation')
    plt.legend()
    plt.grid()
    plt.xlabel('$V_{GS}$[V]')
    plt.ylabel('$I_{D}$[$\mu \alpha$A]')
#_____________________________Schokley Model_____________________________________
    def quad_func(Vgs,k,vt):
        return np.piecewise(Vgs,[Vgs<vt,Vgs>=vt],[0,lambda Vgs:k*(Vgs-vt)**2])

    #vari veis modelo Schokley
    var_quad,er_quad=curve_fit(quad_func,Vgs,Id,[1e-4,0.3])
    k_quad=var_quad[0]
    vt_quad=var_quad[1]

    print('Quadratic Model',i,': k=',k_quad)
    print('Quadratic Model',i,': vt=',vt_quad)

    #gr fico do modelo de Schokley
    Id_Schokley=quad_func(Vgs,k_quad,vt_quad)
    plt.plot(Vgs,Id_Schokley*1e6,label='Schokley Model')
    plt.legend()
    plt.title('Shockley model: Transfer Characteristic (L='+i+')')
#_____________________________N Power Mode_____________________________________
    def n_func(Vgs,k_n,vt_n,n):
        return np.piecewise(Vgs,[Vgs<vt_n,Vgs>=vt_n],[0,lambda Vgs:k_n*(Vgs-vt_n)**n])

    #vari veis modelo n power
    var_n,er_n=curve_fit(n_func,Vgs,Id,[1e-4,0.3,2])
    k_n=var_n[0]
    vt_n=var_n[1]
    n=var_n[2]

    print('N Power Model',i,': k=',k_n)
    print('N Power Model',i,': vt=',vt_n)
    print('N Power Model',i,': n=',n)
```

```
54
55      #gr fico modelo n power
56      Id_n=n_func(Vgs,k_n,vt_n,n)
57      plt.figure()
58      plt.plot(Vgs,Id*1e6,'.',label='LTspice Simulation')
59      plt.plot(Vgs,Id_n*1e6,label='N Power Model')
60      plt.legend()
61      plt.title('N Power model: Transfer Characteristic (L='+i+')')
62      plt.xlabel('$V_{GS}$[V]')
63      plt.ylabel('$I_{D}$[$\mu \alpha$A]')
64      plt.grid()
65  #_____________________________Relative error_____________________________________
66      #c lculo dos erros relativos para ambos os modelos
67      erro_Schokley=((abs(Id-Id_Schokley))/Id)*100
68      erro_n=((abs(Id-Id_n))/Id)*100
69
70      #gr fico dos erros relativos do modelo de Schokley
71      plt.figure()
72      plt.plot(Vgs,erro_Schokley,'.')
73      #plt.ylim(-2,10)
74      #plt.xlim(0.4,1)
75      plt.xlabel('$V_{GS}$[V]')
76      plt.ylabel('Error %')
77      plt.title('Schokley Model: Relative Error (L='+i+')')
78      plt.grid()
79
80      #gr fico dos erros relativos do modelo n power
81      plt.figure()
82      plt.plot(Vgs,erro_n,'.')
83      #plt.ylim(-2,10)
84      #plt.xlim(0.3,1)
85      plt.xlabel('$V_{GS}$[V]')
86      plt.ylabel('Error %')
87      plt.title('N Power Model: Relative Error (L='+i+')')
88      plt.grid()
```