CSE 436/536 Assignment 1:

Design and Simulate CMOS Inverter, 2-input NAND, and 2-input NOR Using Magic Layout and SPICE

Deadline: 29/10/2024 23:59

In this homework, you will design a CMOS inverter, a 2-input NAND gate, and a 2-input NOR gate using the **Magic Layout** tool. After laying out the designs, you will extract the layout into SPICE format and simulate the circuits using **TSMC 0.25µm technology** to verify their functionality.

Objectives:

1. **Design layouts** for an inverter, a 2-input NAND, and a 2-input NOR gate using Magic.
2. **Extract the layouts** into SPICE circuits.
3. **Add TSMC 0.25µm model parameters** to the SPICE file.
4. **Simulate** the circuits in SPICE and verify their functionality.

Tools Required:

- **Magic VLSI Layout Tool** for designing the layouts.
- **SPICE simulator** (ngspice) for simulation.
- **TSMC 0.25µm technology file** (tsmc_cmos025)

1. Designing the Layouts in Magic

Step 1: Setup Magic for TSMC 0.25µm Technology

Before starting the layout, ensure that Magic is configured to use the TSMC 0.25µm technology. You will need the technology file and any associated rules (contact your instructor if you don't have it). The height of all your cells MUST be 100λ. For all your designs, NMOS W/L = 4λ/2λ, PMOS W/L = 8λ/2λ.

To load the technology in Magic:

```
magic -T SCN5M_DEEP.12.TSMC.tech27
```

Step 2: Design the CMOS Inverter

A CMOS inverter is made up of an NMOS and a PMOS transistor. The layout consists of:

1. Draw the **PMOS** in the n-well, and the **NMOS** below it.
2. Connect the **source** of the PMOS to **VDD** and the **source** of the NMOS to **GND**.
3. The **drains** of both transistors should connect together to form the output.
4. Draw a **poly gate** crossing both the NMOS and PMOS to form the input.
5. Use **metal1** to wire up the connections.

Step 3: Design the 2-input NAND Gate

A 2-input NAND gate requires:

- **Two NMOS transistors in series** and **two PMOS transistors in parallel**.

1. Draw the **PMOS transistors in parallel** in the n-well.
2. Draw the **NMOS transistors in series**.
3. Connect the **drain** of the PMOS pair and NMOS pair to form the output.
4. Use **poly** to connect both gates to form the two inputs, A and B.
5. Use **metal1** to connect the PMOS sources to **VDD** and NMOS sources to **GND**.

Step 4: Design the 2-input NOR Gate

A 2-input NOR gate requires:

- **Two NMOS transistors in parallel** and **two PMOS transistors in series**.

1. Draw the **PMOS transistors in series** in the n-well.
2. Draw the **NMOS transistors in parallel**.
3. Connect the **drains** of the PMOS and NMOS to form the output.
4. Use **poly** for the two inputs, A and B.
5. Use **metal1** to wire the connections to **VDD** and **GND**.

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2. Extracting the Layout to SPICE

Once the layouts are complete, the next step is to extract the netlist and other necessary components for SPICE simulation.

Step 1: Extract the Layout

In Magic, run the following commands to extract the layout into SPICE format:

bash

Copy code

```
: extract do all
: extract all
: ext2spice cthresh 0.001
: ext2spice rthresh 1
: ext2spice merge none
: ext2spice extresist off
: ext2spice
```

The extract all command extracts the layout information.The ext2spice command generates a .spice file with the extracted netlist.

You will now have a .spice file corresponding to the design (e.g., inverter.spice, nand2.spice, nor2.spice).

Step 2: Edit the Extracted SPICE File

Open the generated .spice file in a text editor. You'll see the transistor netlist and connections. The file will be missing the technology-specific parameters and models for NMOS and PMOS transistors. You need to add the TSMC 0.25µm technology model cards for simulation.

1. At the top of the SPICE file, add:

```
.include tsmc_cmos025
```

2. Also, define the power supply, input signals, and output load. For example, for an inverter:

```
Vdd VDD 0 2.5V
Vin in 0 PULSE(0 2.5 0ns 10ns 10ns 20ns 40ns)
CL out 0 1fF
.TRAN 1ns 100ns
```

- Vdd provides the supply voltage.
- Vin generates a pulse input (0 to 2.5V).
- CL is a small load capacitor at the output node.
- .TRAN is for transient analysis, i.e. the analysis of signals with respect to time.

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3. Running the SPICE Simulation

Step 1: Load the SPICE Model

Ensure that you have the **TSMC 0.25µm technology file** (tsmc025.lib) in the same directory as your .spice files or provide the correct path in the .lib statement.

Step 2: Run the Simulation

1. Open your SPICE simulator (ngspice).
2. Load the .spice file:

   ```
   source your_gate.spice
   run
   ```

3. Plot vin and vout on the same plot (assuming your input(s) are A and B and output is Y):

   ```
   .plot V(A) V(B) V(Y)
   ```

This command will simulate the circuit for 100ns with a time step of 1ns.

4. Analyze the output waveform for correctness:

- For the inverter, verify that the output is the complement of the input.
- For the NAND gate, check that the output is low only when both inputs are high.
- For the NOR gate, confirm that the output is high only when both inputs are low.

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4. Submission Requirements

1. **Magic Layout Files**: Submit the .mag files for the inverter, 2-input NAND, and 2-input NOR gates.
2. **SPICE Files**: Submit the extracted .spice files with the added TSMC 0.25µm model parameters.
3. **Simulation Results**: Include screenshots or plots of the output waveforms for all three circuits (inverter, NAND, and NOR) demonstrating correct functionality.
4. **Report**: A brief report explaining:
    - How you designed the layouts.
    - How you extracted the netlist and set up the simulation.
    - Your interpretation of the simulation results.

Tips:

- Use grid snapping and layers effectively in Magic to ensure proper DRC compliance.
- Check for design rule violations using the drc check command.

Deadline:

Please submit your files and report by **29/10/2024 to Teams before midnight.**

This homework will give students hands-on experience in layout design, circuit extraction, and functional verification using industry-standard tools. It integrates both physical design and circuit simulation, offering a comprehensive understanding of digital CMOS circuit design.