

An integrated Silicon-on-sapphire Patch-clamp amplifier

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Abstract—We fabricated an integrated patch-clamp amplifier capable of recording from pico- to tens of micro-amperes of current. The high-dynamic range of seven decades and the picoampere sensitivity of the instrument was designed for wholecell patch-clamp recordings. The prototype was fabricated on a 0.5 μ m silicon-on-sapphire process. The device employs an integrating headstage with a frequency-modulated output pulse ranging from 3Hz to 10MHz. A digital interface produces a 16bit output conversion of the input currents. We report on electrical measurements from the fabricated device, and measurements conducted on cells in a typical patch-clamp experiment.

INTRODUCTION

The need for fast and sensitive drug testing in the pharmaceutical industry requires the implementation of rapid, highly parallel screening techniques [1, 2, 3]. Ion channels are excellent drug targets as they play a major role in many common diseases [4]. The most sensitive technique available for screening ion channel active drugs (ICADs) is patch clamp recording from cell membranes, which allows even single ion channels to be probed with great accuracy [5, 6]. The major drawbacks of this technique for industrial applications are the low throughput and the high personnel costs due to the labor intensive evaluation of individual drugs. Given the large number of drugs generated by combinatorial chemistry and the high degree of selectivity required, a rapid and efficient screening method is particularly important. Recently, different instruments for the automated analysis of ion channel function have been developed for ion channels expressed in *Xenopus Oocytes* [7] as well as mammalian cells [8, 9].

We designed, fabricated and assembled an integrated patch-clamp amplifier targeted to whole-cell patch-clamp measurements. The device is capable of recording from pico- to tens of micro-amperes of current, providing a very high-dynamic range and sensitivity. The prototype was fabricated on a conventional 0.5 μ m silicon-on-sapphire process, taking advantage of the low-power and low-noise property of the device and the insulating substrate. The device uses an integrating headstage with pulse-modulated output ranging from 3Hz to 10MHz and operating with a system clocks of 10Hz to 50MHz. A digital interface produces a 16bit output conversion of the input currents.

- Die Size: 1.5 x 1.5mm
- Technology: 0.5 μ m SOS CMOS
- Supply: 3.3V
- ADC: 12b Sigma-Delta
- Output Data: Serial
- Range: 3pA to 100 μ A
- Noise: 3pA RMS
- Bandwidth: 10Hz - 50MHz

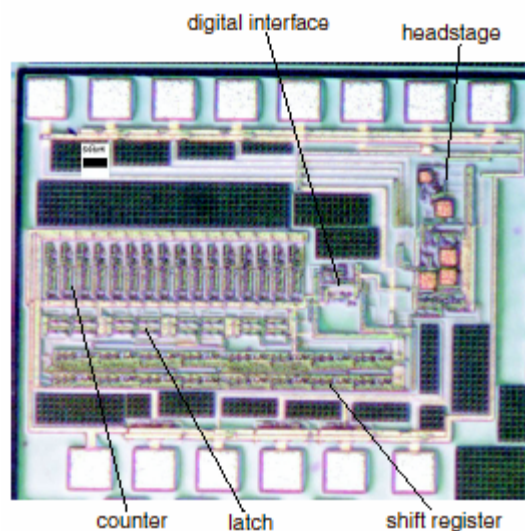


Figure 1. System Die micrograph.

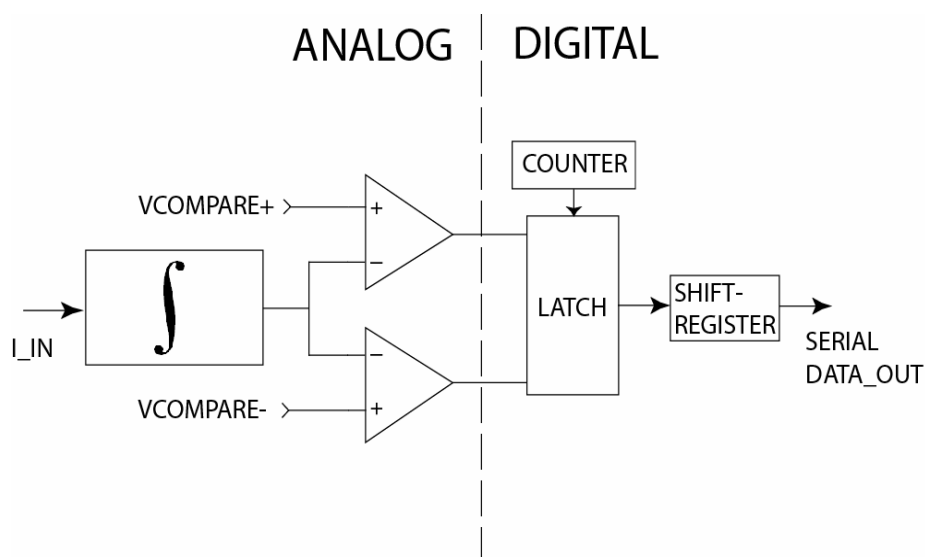


Figure 2. Integrated Patch Clamp Block Diagram.

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