A 16 $\times$ 16 PIXEL SILICON ON SAPPHIRE CMOS PHOTOSENSOR ARRAY WITH A DIGITAL INTERFACE FOR ADAPTIVE WAVEFRONT CORRECTION

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ABSTRACT

We report on a 16 $\times$ 16 pixel CMOS photosensor array fabricated in silicon on sapphire CMOS technology. The transparency of the substrate allows imaging from both the back and front side and opens new applications for CMOS active pixel sensor arrays. A digital asynchronous interface is employed to minimize the design complexity and the the power consumption. The analog pixel value is encoded as a pulse density stream of address events. The multiple threshold MOS transistors available in this technology enable circuit optimizations for low power and low voltage operation. We characterize the pixel sensitivity and show experimental data from both back and front side imaging.

1. INTRODUCTION

Silicon on Sapphire CMOS (SOS-CMOS) available from Peregrine semiconductors [1] is a promising technology for hybrid optoelectronic microsystems [2]. The transparency of the substrate to wavelengths from infra-red to ultra-violet, opens opportunities for applications in high speed free space interconnects and 3D integration. An example of such an application is adaptive optical wavefront correction [3]. In addition to the transparent substrate, this particular SOI process offers MOS transistors with three different thresholds thus enabling the optimization of both analog and digital circuits for low power.

In this paper we report on a 16 by 16 pixels SOS-CMOS photosensor array fabricated in the Peregrine SOS-CMOS 0.5μm process. To the best of our knowledge the first standard CMOS photosensor array capable of transducing light simultaneously from both sides of the die.

2. PHOTODIODE DESIGN AND CHARACTERIZATION

The fabricated SOS-CMOS imager employs a native PIN photodiode as photosensitive element. Spectral and temporal characterization of such structures have been reported previously in [4, 5] and more recently in [6].

Using the ultra thin silicon photodiodes has advantages and disadvantages. Photon absorbtion in the ultra thin (100nm) silicon layer is small thus severely degrading the quantum efficiency to blue and UV wavelengths. This is in contrast to bulk CMOS photo-detectors that are sensitive to red and infra-red and have weak response to blue. Blue and ultraviolet sensitivity requires ultra-shallow junctions that are hard to achieve in standard bulk CMOS processes. Using a PIN photodiodes decreases junction capacitance and thus yields devices with bandwidth in excess of 5GHz [5]. The photodiode used in our pixel has a horizontal structure $100nm$ thick and 16.4μm long, with a 1.2μm intrinsic silicon layer between anode and cathode. The photocurrent is integrated on a $250fF$ capacitor. In our application, of an adaptive wavefront correction system, the poor absorbtion in the PIN photodiodes is an advantage as we are only employing the photosensor array in the feedback loop and the PIN photodiode is present just to sample the light from the laser beam.

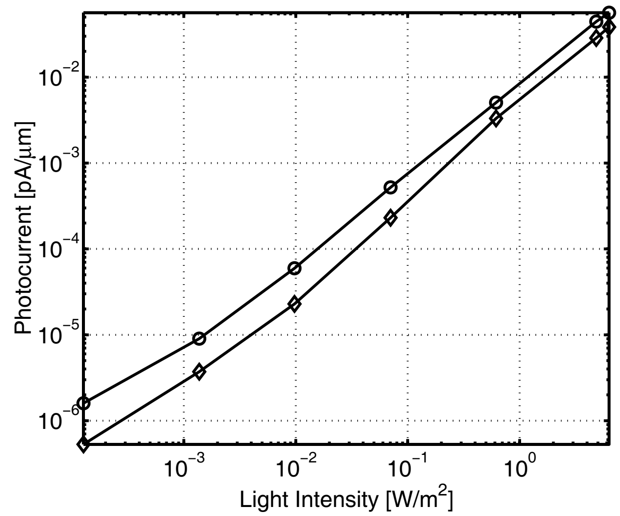

Fig. 1. Front (diamond) and back (circle) side photocurrent at $555nm$

When the PIN photodiode is reverse-biased with the nominal supply voltage of $3.3V$, we measured high levels of dark current ($17pA$) (approximately $1pA/\mu m$ of diode length). This imposes a lower bound on the lower limit on the sensor's dynamic range. Assuming a conservative threshold of $0.5V$ for triggering an event, in the dark a pixel takes $250fF \cdot 0.5V/17pA = 7ms$ to integrate enough light to produce an event. This is clearly a small time constant compared to other image sensor based on the same architecture [7], and ultimately limits the quality of the images. Integrating for longer period of time reduces the noise in integrating pixels. High level of dark current result in decreased image contrast. Events from the sensor arise with time constant of $27\mu s$ ($7ms/256$, where 256 is the number of cells). This is the minimum event rate at the output of the image sensor. Ambient light generates a photocurrent of $30 - 40pA$, therefore the image sensors SNR is only 2-3. A low-power ($5mW$) laser pointer light generates $100pA$ and an integration time of $1.25ms$. A high intensity illumination lamp generates a maximum of $600pA$ with an integration time of $0.2ms$. The problem with excess leakage currents in the the PIN photodiodes can be solved by re-designing the photosensitive structure.

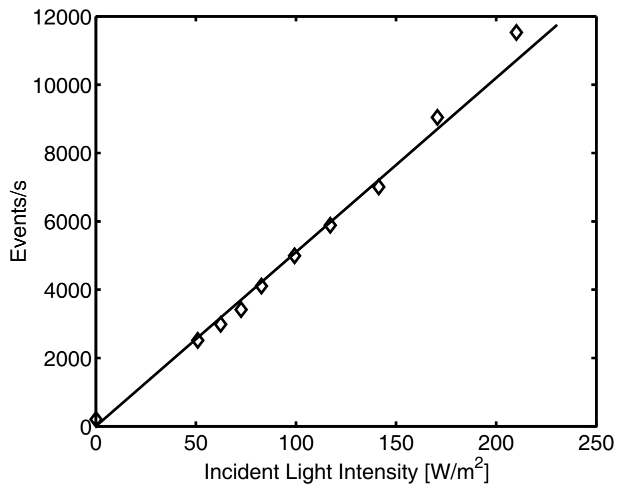

Fig. 2. Event rate versus light intensity

Figure 1 shows a plot of the photocurrent per unit length of the SOS PIN photodiode from both front and back side of the die. Light intensity was measured with a calibrated photometer and a variable high intensity source. Note that light integrated from the back side generates higher photocurrents than the front side. This occurs because the front side of the die is covered by metal and SiO_2 layers that filter some of the incident light. Figure 2 reports the event frequency versus incident light intensity at $555nm$ for a single pixel in the array. Using backside illumination a 100% fill factor can be achieved. For the data in this figure, the light was focused on a single pixel on the array using a lens, and the light intensity from the laser was varied using neutral density filters. The event frequency f_{ev} is linear with light intensity I_{in}. The relationship is given in formula 1 where the parameter L_s equals to 51.

$$f_{ev}[Hz] = L_s \cdot I_{in}[W/m^2]) \qquad (1)$$

The output event frequency spans approximately 2 orders of magnitude (200 to 11500Hz) and thus the array is capable of encoding data with 4 to 6 bits of precision, which is sufficient for the intended application.

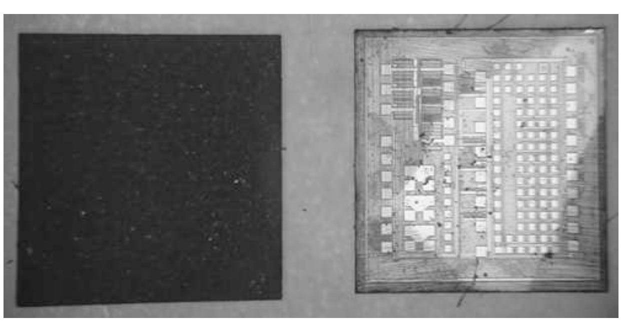

Fig. 3. An SOS-CMOS test-die before and after mechanical polishing.

3. SYSTEM ARCHITECTURE

Conventional optical image sensor arrays convert light into a time varying voltages that are buffered at the pixel level using a voltage follower and subsequently synchronously serially scanned to the output. The read-out circuit thus allocates equal portion of the channel bandwidth to all pixels independently of activity and continuously dissipates power as the scanner is always active. The system presented in this paper employs pulse frequency modulation at the pixel level converting the analog data into asynchronous pulses at the pixels' output. Such digital representation of light intensity yields devices capable of large dynamic range imaging and low-power dissipation [8, 9, 7]. Pulse modulated output has also been reported for biomimetic image gradient sensors [10].

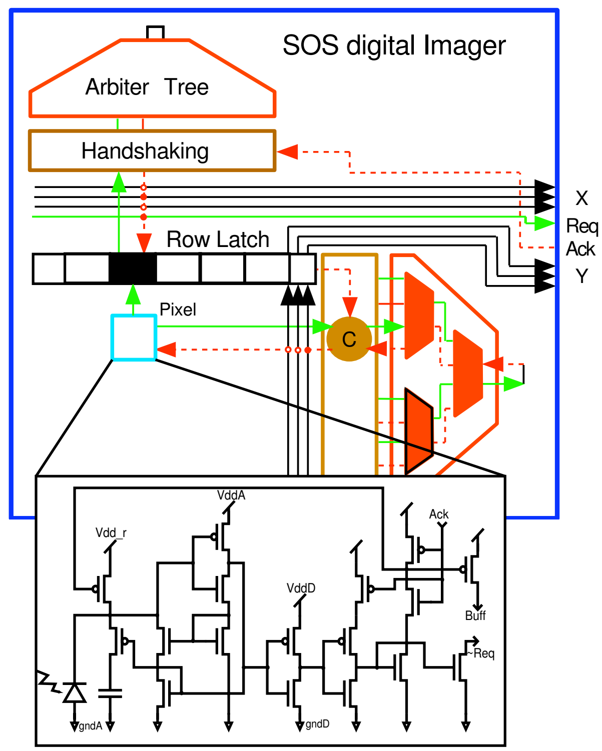

Fig. 4. SOS-CMOS Photosensor Array Architecture

We now describe the pulse frequency modulation scheme implemented at the pixel. Individual pixels integrate light on a local capacitor and when a threshold is reached, they request access to the output bus. Their address (X, Y locations) appears at the output after arbitration (refer to Arbiter Tree in Figure 4) in the form of an event. The value of the light intensity is inversely proportional to the inter-event interval. The image sensor read-out is initiated by individual pixels, therefore the available output bandwidth is allocated according to pixels demand. A detail analysis and comparison of synchronous and asynchronous readout schemes is beyond the scope of this paper and can be found in [11]. The pixel circuit implementing the pulse density modulation is shown as insert in Figure 4. The layout of the pixel is shown in Figure 5.

Arbitration is executed in two steps: rows are arbitrated first then arbitration occurs between active pixel in the selected row [7]. Once a row has been selected and row events are stored in the

Row Latch of Figure 4, other rows of pixels can proceed with light integration and competition for the output bus. This organization increases the sensor's throughput. An Address bus as well as a Request and an Acknowledge signal interface the system to the receiver which reconstructs the analog signal. Reconstruction of the images can be performed by counting the number of events in a given window of time (*histogram imaging*), or by computing the inter-event time between successive events from the same pixel (*inter-event imaging*) [7]. An analysis of optimal receiver design for such class of imagers is discussed in the paper by Apsel and Andreou [12].

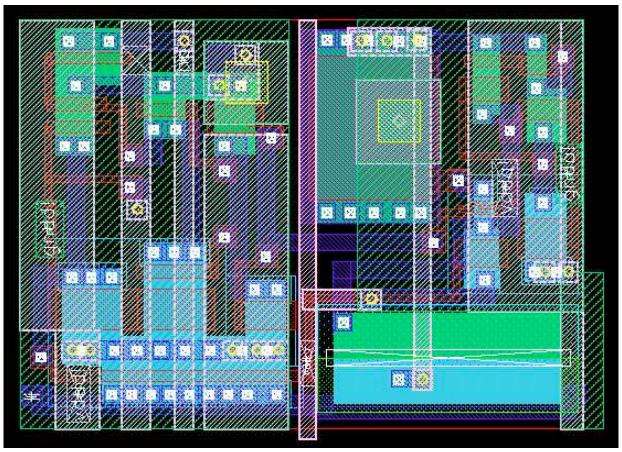

Fig. 5. Pixel Layout

4. EXPERIMENTAL RESULTS

The die area for the sensor array is $0.66cm^2$ without output pads, and $1.23cm^2$ with pads. Pixel size is 29.6 by $42\mu m$. A micrograph of the die is shown in Figure 8. The SOS wafer was polished only on the front side after fabrication. To obtain a clear die on both sides, we have polished the back side of the die using a mechanical lapping machine. Lapping was performed up to a surface roughness of $1\mu m$. The mechanical polishing resulted in an optically clear die on both side. Alternatively index matching fluid can be employed to fill in the asperities of the backside [2]. The effectiveness of the mechanical polishing is evident in figure 3.

Sample image sequences given from the sensor are given in Figure 6 and 7. Figure 6 is obtained by illuminating on the front side, Figure 7 on the back side of the die (BSI). In both Figure a moving spot is sampled 4 times and the output event rate was $0.48MSamples/s$. These images were reconstructed by creating a normalized histogram after collecting 10000 events. Noisiness of the images is due to errors in the collections of addresses and to the limited number of pixels.

Power consumption of the analog array is: $0.60\mu W$. Since there are 256 pixels in the array, this amounts to a consumption of about $2.32nW$ per pixel. Low power operation is a result of employing the pulse frequency modulation pixel [7] as well as optimized circuit design employing MOS transistors with three different thresholds. The energy consumption for each event is on the order of $4.83fJ$. Digital power consumption was measured to be $1.1mW$. This includes the use of 3 pseudo-CMOS logic signals in

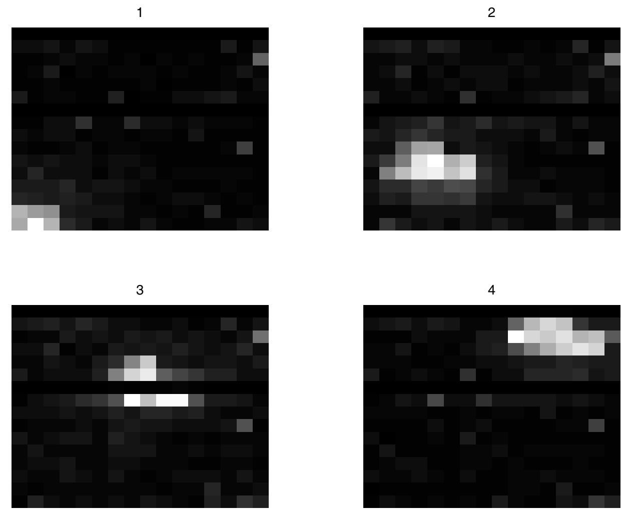

Fig. 6. Output from a light spot moving up-right impinging on the front side of the sensor array

the array, that account for most of the power consumption. In the next version of the chip, the wired-or will be replaced with a tree based fully CMOS design, thus reducing dramatically the power dissipation. The circuit design both for the pixel and periphery employs the available zero threshold transistors [2] to reduce the complexity, minimizing the number of transistors and wires necessary for bias circuits.

Both analog and digital power consumption measurements were conducted using a supply voltage of $3.3V$ and with an output event rate of $0.48Mevents/s$. The average amount of energy spent by the array to communicate an event to an external receiver is $2.3\mu J$. This figure takes into account the switching of 9 pads (4 + 4 addresses and a $request$ signal) and the power consumption of the pad drivers, that in this technology is 40pJ/event (from simulation data).

5. SUMMARY

We have designed, fabricated and tested a 16 by 16 pixel SOS-CMOS photoreceptor array with a digital interface. We characterize the individual components of the array and demonstrate functionality for both front and back side imaging.

6. ACKNOWLEDGEMENTS

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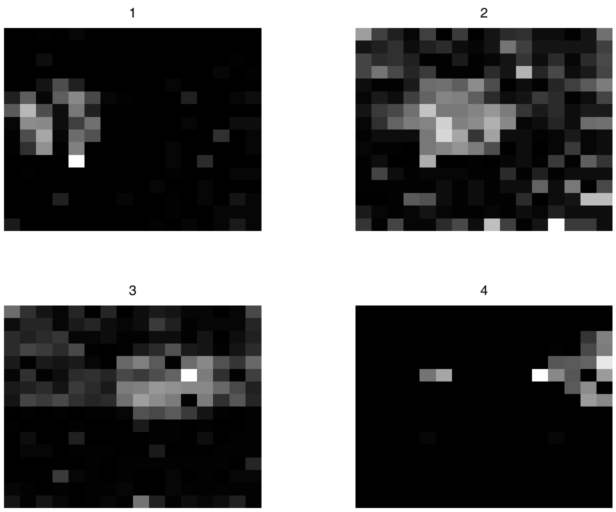

Fig. 7. Output from a light spot moving up-right impinging on the back side of the sensor array

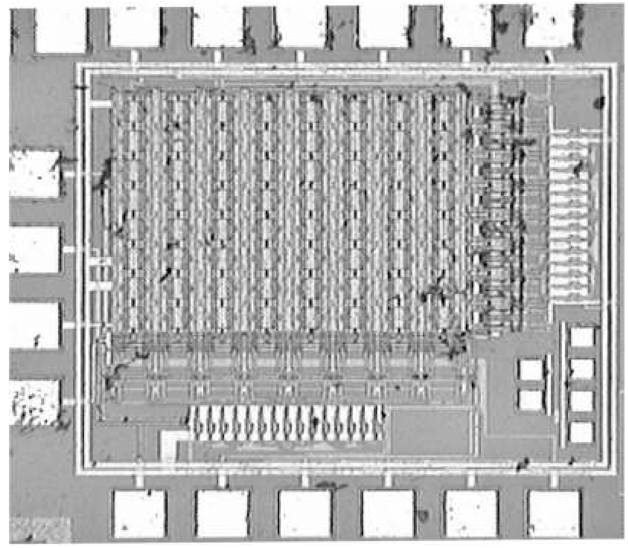

Fig. 8. Die micrograph for the 16x16 sensor array.

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