A Pulse-based Amplifier and Data Converter for Bio-potentials

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***Abstract*— We present a low-power pulse-based amplifier and data conversion circuit for recording bio-potentials. The circuit is designed for data reduction in neurophysiological sensor and communication systems. A low-power low-noise AC amplifier with an asynchronous delta A/D converter is implemented. The asynchronous delta modulation has the advantage of data reduction, clock-less and no quantization noise. The amplifier gain is 53dB (bandwidth of 200Hz-20kHz) with DC variation rejection. The input-referred rms noise is 2μV. The delta amplitude in the A/D converter is 0.1V at 3.3V voltage supply. The system is fabricated with AMI 0.5μm CMOS technology. The chip size is 1191 μm by 713 μm. The power consumption with 3.3V supply is 75.9 μW in static state and 194.7 μW with 60kbps data conversion rate. A graphic user interface was developed to monitor the transmitted signal in real time.**

I. Introduction

In recent years, there has been a growing demand of bio-potential sensor and communication technologies [1]. The direct and continuous monitoring of neural activities is essential for neuroscientists and clinicians to understand the basis of physiological functions. Current neural recording system realizations are facing several significant challenges. First, the speed of wireless devices are not sufficient to carry the large data streams from the sensor array [2]. Second, the high power consumption due to the high-speed sampling and data conversion limits the feasibility of the implantable device. The third challenge for this low-noise mixed signal system is the clock in A/D circuit working at fixed sampling rate. Noise interference from digital transitions of the clock can become the dominant source of noise in the system [3].

Instead of the synchronous sampling and conversion method, we designed an asynchronous delta modulation to perform data conversion. The advantage of an asynchronous delta A/D converter originates from the characteristics of the neural signal. A typical active neuron generates 10-100 spikes per second. A neural spike has a duration around 250μs [2]. If we consider a neural with spike rate of 50 spikes per second and use a 12bit 80kSample/s synchronous data conversion system to record the signal, there will be 20 samples in each spike. The data amount in one second is 960kb but 948kb will be zero (if we don't consider noise) as the neural spikes are very sparse. These "zero" data occupies the majority of the transmission bandwidth, which is the main reason of the limitation in the system.

If we use asynchronous delta A/D conversion in the same situation, assuming the spike can be amplified to 1V peak to peak amplitude and the delta step is 0.1V, there will also be 20 samples in each spike (10 samples in the rising edge and 10 samples in the falling edge). The data amount is only 1kb per second and there is no "zero" data. In other words, the circuit provides 960 times data rate reduction compared with the conventional method. Although the data stream is not quantized in time, the asynchronous A/D conversion doesn't have quantization noise in amplitude [4]. Moreover, as the A/D conversion circuit works asynchronously, the system is free from the noise interference by the fixed-sampling-rate clock. The comparison of the two methods in a neural recording system (with the typical value) is summarized in Table I, in which we assume that the input spike duration (D_s) is 250μs and spike rate (F_s) is 50 spikes per second. The asynchronous

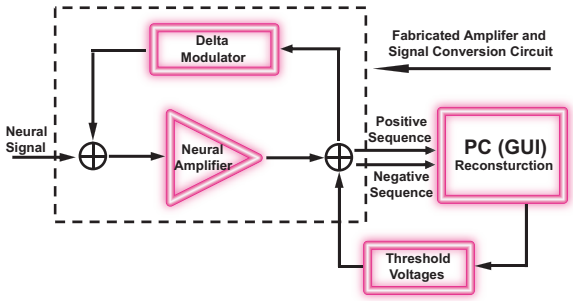

Fig. 1. Block diagram of the amplifier and signal conversion circuit. The input neural signal is amplified and modulated to digital pulse sequence by delta modulator. Threshold voltages determine the delta step. A graphic user interface (GUI) reconstructs the waveform based on the digital pulse sequence and threshold voltages.

	Synchronous Conversion	Asynchronous Delta
System parameters	N: resolution bits (12) S: sampling rate (80kS/s)	A: signal swing (1V) d: delta step (0.1V)
Samples per spike	SD_s (20)	2A/d (20)
Total data rate	NS (960kbps)	$2F_s$A/d (1kbps)
Non-zero data rate	NSD_sF_s (12kbps)	$2F_s$A/d (1kbps)
Quant. in Amplitude	Yes	Yes
Quant. in Time	Yes	No
Requirement of Sampling clock	Yes	No

TABLE I
Comparison of data conversion scheme.

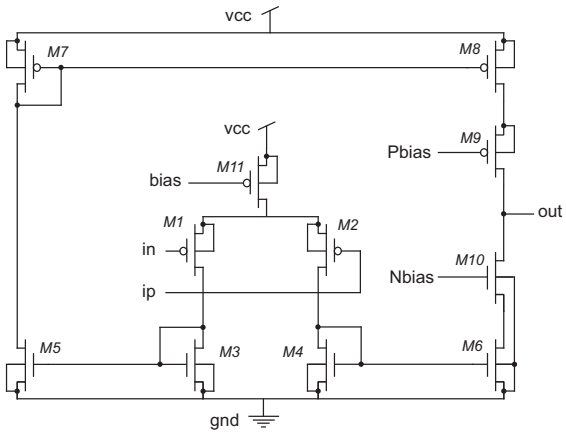

Fig. 2. Schematic of the low-power low-noise operational amplifier (OP AMP). The input stage is a PMOS pair to reduce noise. The output stage is a cascade amplifier to increase the gain.

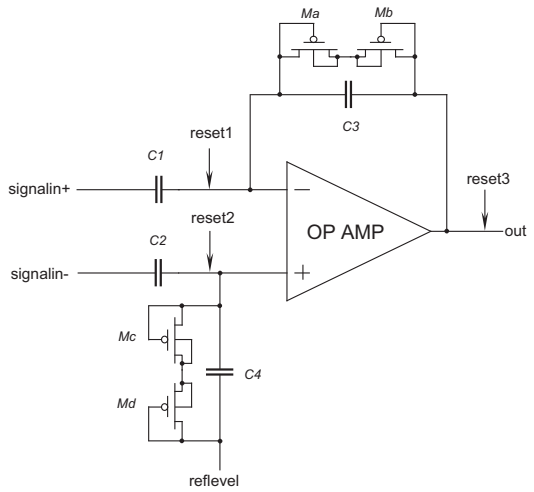

Fig. 3. Schematic of the AC amplifier (AC AMP). The capacitor feedback is designed to filter out the DC component of the input signal while rejecting common-mode noise. The MOS-bipolar pseudoresistor elements are working as large resistors to amplify low frequency signal and reject the DC offset. Three reset signals can reset the output of the amplifier to the signal ground.

delta A/D conversion will reduce the data amount remarkably and remove the sampling clock, while keeping the number of the samples during the spike.

Besides the data reduction, the budget of power dissipation of implantable device suggests that the sensor unit only performs minimum required functions [2]. The asynchronous delta A/D conversion only executes amplitude domain quantization but leave the time domain quantization to the receiver part. The circuit power consumption is reduced observably.

II. System Design

The asynchronous A/D conversion produces a pulse when the signal increases or decreases by a fixed threshold (as the positive delta and negative delta). The block diagram of the pulse-based amplifier and signal conversion system is illustrated in Fig. 1. The system consists of a low-power low-noise operational amplifier and a delta modulation circuit. The threshold voltages are provided to the circuit to control the delta step amplitude. The output of the amplified signal is converted to positive and negative pulse sequences and sent to the computer. The pulse rate is directly proportional to the rate of the signal change.

Reconstruction of the pulse streams is performed by a data sequence in the computer. According to the timing of the positive and negative pulses, the value in the data sequence is increased by a positive delta with each positive pulse, and decreased by a negative delta with each negative pulse. Plotting the data sequence over time reconstructs the original signal. In the asynchronous A/D conversion, the signal is sampled only when it changes. Accumulation of the offsets can be removed from the data collecting program by the computer.

The design of the integrated circuit contains the amplifier and delta modulation A/D circuit.

1) Amplifier: A low-power low-noise operational transconductance amplifier (*OP AMP*) [5] is used as the main amplifier, which is shown in Fig. 2. The bias current of M11 is set to 5μA and current in M1-M10 is 2.5μA. A cascade structure is used in output stage to boost the gain. The circuit is designed to

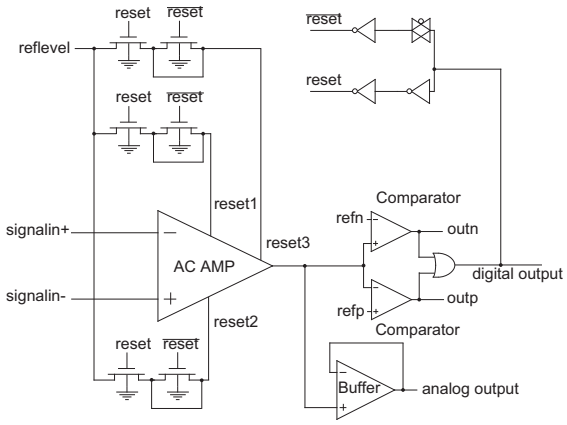

Fig. 4. Schematic of the fabricated amplifier and signal conversion circuit. The *analog output* is compared with the threshold voltages. When the comparator triggers, a digital pulse is send to the output and the amplifier is reset. The reset signal of the amplifier is generated from *digital output*.

suppress noise while maintain relevant speed for neural signal processing. The W/L ratio of the input differential PMOS transistor pair is large (1000μm/5μm) to set the input devices working in subthreshold region. The intrinsic gain of the OTA is 94dB.

Capacitor feedback is designed to work with the *OP AMP* to reject DC variation of the neural signal. The design bandwidth was 200Hz-20kHz. The schematic of the design is shown in Fig. 3. *Ma-Md* are utilized as large pseudoresistors [5] to amplify low frequency signals and reject DC offsets. In amplification mode, the gain of the AC amplifier is 53dB. In reset mode, three reset signals are connected to reference level (*reflevel*, which is 0.5 *Vdd*) to reset the output voltage to signal ground.

2) Delta Modulation and A/D conversion: The delta modulation is carried by an asynchronous reset signal, which is the

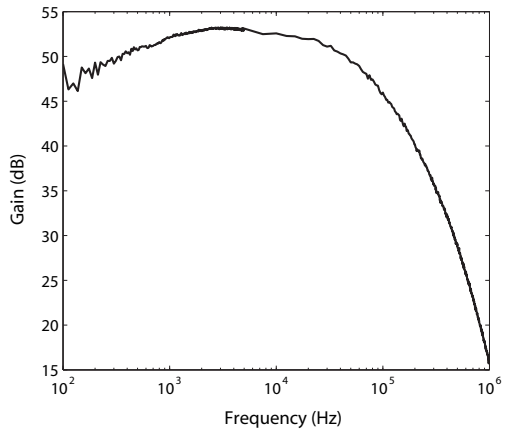

Fig. 5. Measured gain response of AC amplifier. The gain is over 50dB between 200Hz and 20kHz.

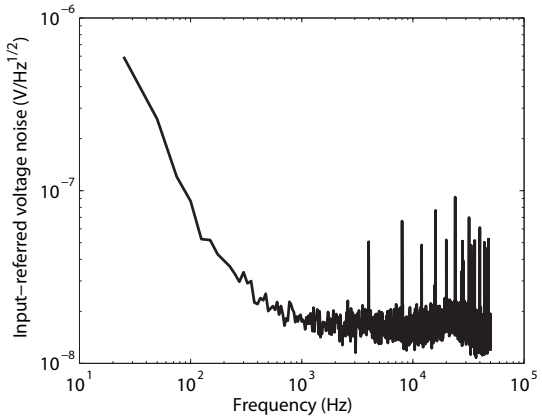

Fig. 6. Measured input referred noise of AC amplifier. The rms noise is 0.7μV for ECG signal (0.5Hz-50Hz) and 1μV for neural signal (10Hz-20kHz). The total input-referred rms noise is less than 2μV

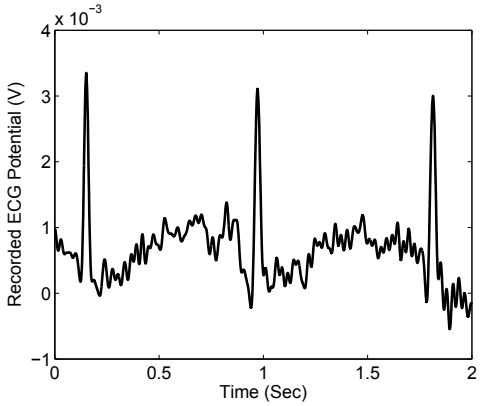

Fig. 7. Input-referred ECG recording signal. Converted from the output signal and amplifier gain.

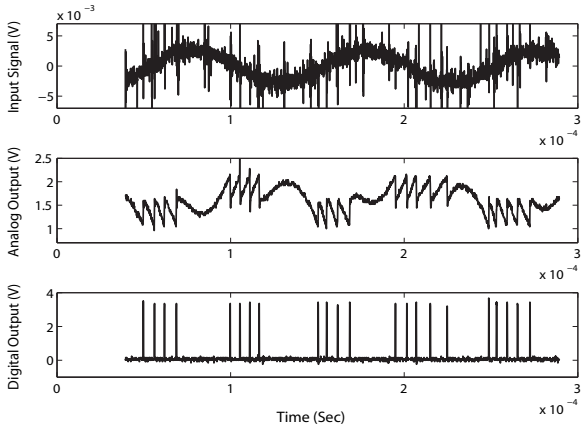

Fig. 8. Measured chip input and output waveform in 3.3V single power supply. Top: 10kHz input signal with amplitude of 3mV. Middle: Analog output signal with delta modulation. The positive threshold is 2.2V and negative threshold is 1.1V. Signal ground is 1.65V. Bottom: Digital output (reset) as OR result from both the positive and negative comparator outputs.

digital output shown in schematic in Fig. 4. Two threshold voltages are compared with the *AC AMP* output. The gap between the threshold voltage (*refn* or *refp*) and signal ground is the positive or negative delta. If the amplifier output is larger than the positive threshold or smaller than the negative threshold, the comparator output will set to logical high and so does the digital output. The high digital output will reset the *AC AMP* output (*analog output*) to signal ground. After reset, the outputs of the comparators will be logic low as the signal ground is in the window between the two threshold voltages. Then the reset signal is released to make the amplifier return to the amplification mode automatically. After reset, a voltage difference between the two input signals (*signalin+* and *signalin-*) could exist, but this difference will be considered as DC difference and hence will not be amplified. This process will generate a pulse in one of the comparator output (*outn* or *outp*). The comparator output is the result of the pulse-based A/D conversion. The self-reset scheme makes the circuit a clock-less A/D converter.

III. Experimental Results

The circuit is fabricated using AMI 0.5μm 3M2P process. The capacitor is build from PIP (polysilicon-insultor-polysilicon). *C1,C2* is 35pF and *C3,C4* is 50fF. The measurement result of the *AC AMP* is shown in Fig. 5 and Fig. 6. The gain is over 50dB between 200k and 20kHz. With in this bandwidth, the input referred noise is 20nV/$\sqrt{Hz}$ with rms of 2μV. The input-referred noise is calculated from the measured output noise and amplifier gain. We used the AC amplifier as a preamplifier to record human electrocardiograph (ECG) activity, as shown in Fig. 7. The amplifier consumes 49.5μW at 3.3V power supply.

Fig. 8 shows the measured input and output waveform of the amplifier and data conversation circuit. The input signal is a 10kHz 3mV peak-to-peak sine signal. Referring to Fig. 4, the *analog output* signal is compared with the positive (2.2V) and negative (1.1V) threshold voltages. If the *analog output* exceeds the window between the two threshold voltages, the amplifier output will be reset to the signal ground. During the reset mode, the comparator generates a digital pulse. An OR

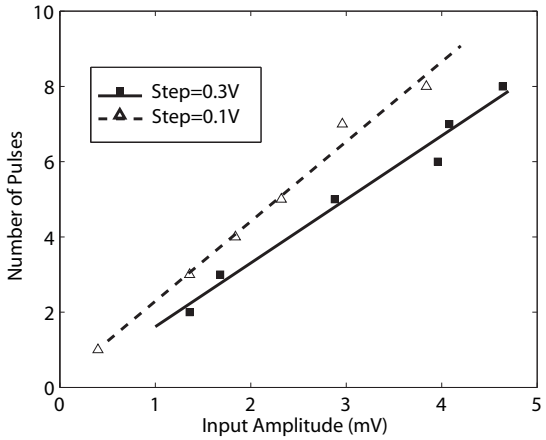

Fig. 9. Measured linearity of delta modulation. The input signal is 6kHz sine wave. The number of the pulses when input signal changes from peak-to-peak (half cycle in sine wave) is proportional to the input signal amplitude.

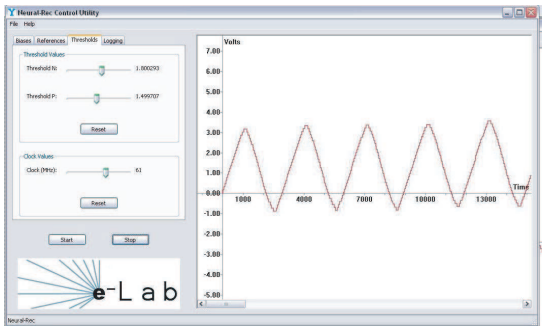

Fig. 10. Reconstructed waveform in GUI, running in real time.

operation of the two pulse sequences from comparators will produce the asynchronous reset signal for the delta modulation, shown as *digital output*.

We measured the linearity of the delta modulation as illustrated in Fig. 9. We use a 6kHz sine signal as the input signal and set the delta step to 0.1V and 0.3V, then count the number of pulses in *digital output* while the input changes from peak to peak (half cycle of the sine wave). When the delta step is fixed, the number of pulses are linearly proportional with the input signal amplitude.

A demo system is developed using OpalKelly 3001v2 FPGA as the interface between the chip and PC (GUI). In the system, the pulses are sampled and sent to the PC, where the output waveform is reconstructed by adding or subtracting the delta amplitude according to the pulse sequences. The amplitude of the delta step can be controlled at the GUI via a 12 bit DAC (AD7398). The system is running in realtime for monitoring the activities of the input signal. The reconstructed waveform is displayed in the GUI as shown in Fig. 10.

IV. Summary

We designed and tested a low-power low-noise pulse-based amplifier and signal conversion circuit for neural signal recording. The chip micrograph is illustrated in Fig. 11 with main building blocks highlighted. The chip area is 1191 μm by 713 μm. Table II summarizes the main properties of the chip. The test result shows that our circuit consumes 75.9μW in statical mode and 194.7 μW when the pulse rate is at 60k/sec (60kbps data rate). The system provides remarkable data reduction, clock-less A/D conversion and low power consumption. This design is a competitive solution in neural recording system.

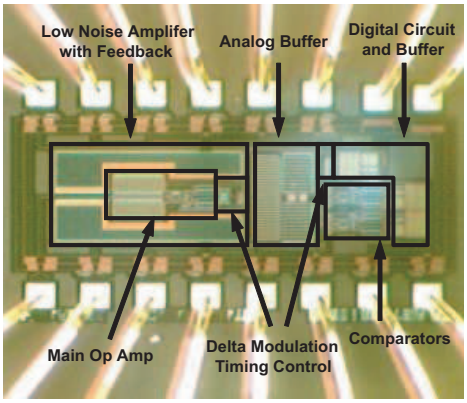

Fig. 11. Chip micrograph with main building blocks highlighted.

Process technology	AMI 0.5μm CMOS
Chip size	1191 μm by 713 μm
Supply voltage	3.3V
Amplifier Bandwidth	200Hz-20kHz
Amplifier Gain	53dB
Amplifier Output swing	2V
Input-referred rms noise	less than 2μV
Amplifier power	49.5μW
Chip power (static)	75.9μW
Chip power (pulse rate 60k/sec)	194.7μW

TABLE II
SUMMARY OF THE CHIP CHARACTERISTICS.

V. Acknowledgements

This project is funded by ONR grant number 439471 and 396490, and NSF award 0649349. The support of MOSIS in chip fabrication is gratefully acknowledged. We also thank Berin Martini for the help in the GUI development, and Dongsoo Kim for the help in the chip measurement.

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