A 3D Integrated Feature-Extracting Image Sensor

Zhengming Fu, Eugenio Culurciello
Electrical Engineering Department
Yale University
New Haven CT 06520
{zhengming.fu, eugenio.culurciello}@yale.edu

***Abstract*— In this paper we present a feature-extracting image sensor targeted to wireless image sensor networks. The image sensor was designed and fabricated on a 3D integrated 0.18μm silicon-on-insulator CMOS process. The image sensor can simultaneously capture an intensity image and extract image features, which include temporal illumination differentiations and contours. By taking advantage of massively parallel, vertical connectivity, the image sensor can perform more analog computations at higher speed and higher communication efficiency. The top layer is covered by photodiodes and the pixel fill factor is 95%.**

I. Introduction

Recently an emerging technology, called three dimensional integrated circuit (3D IC), turns out to be a promising high-density integrated circuit technique [1], [2], [3]. The 3D IC is a vertically interconnected integrated circuit structure. Multiple silicon-on-insulator (SOI) wafers are stacked on top of each other and circuits on the different layers are connected by inter-layer vias (3D vias). A recent publication [4] presents us with a 3D integrated image sensor capturing only intensity images. This paper focuses on a feature-extracting image sensor, which benefits more from this novel 3D IC technology. The features include temporal illumination differences and object contours. This image sensor design is motivated by three factors. First, by taking advantage of the massively parallel, vertical connectivity, the image sensor performs more analog computations at higher speed and higher communication efficiency. Second, the light collection efficiency is maximized because photodiodes fully cover the top layer of the image sensor. Third, the image sensor can capture intensity images and extract the image features simultaneously.

The feature-extracting image sensor is targeted to wireless image sensor networks applications. A wireless image sensor network is a collection of wirelessly connected low-power image sensors specializing for recognition and detection [5], [6]. A feature-extracting image sensor filters the information at the sensor level and reduces the data to be transmitted. Extracting features on the sensor also speeds up recognition in the sensor network and shortens latency to get the desired information.

II. Sensor System Overview

A. Image Sensor Architecture

The image sensor block diagram is shown in Figure 1. The core pixel array consists of 97×97 pixels. The pixels are sequentially accessed and reset by column/row shift registers. The selected pixel connects to the analog output buffer. The output buffer is a two-stage operational transconductance amplifier (OTA) to drive the pads and the off-chip loads. Each pixel connects with its eight adjacent neighbor pixels through NMOS transistors. The NMOS transistors connect the pixels and form a diffusor network. When the NMOS transistors are biased by global voltages, they act as a spatial low-pass filter, smoothing out the voltage difference among pixels [7].

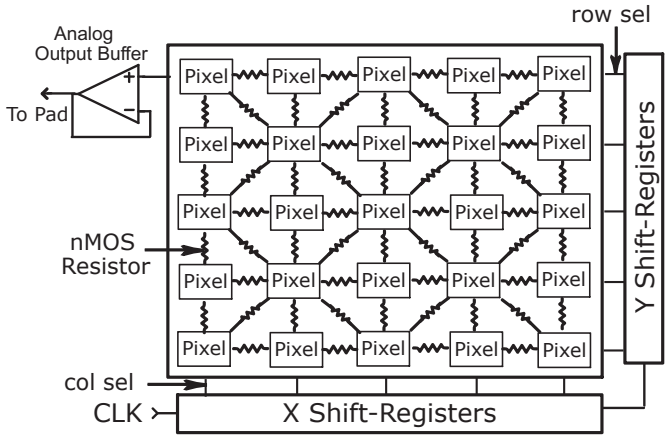

Fig. 1. 3D image sensor architecture. The pixel array is simplified in the figure. The array in the sensor consists of 97×97 pixels.

B. Signal Path from Pixel to Analog Output Buffer

A signal path from the pixel to the analog output buffer is shown in Figure 2. The front-end of the pixel consists of a photodiode and an in-pixel transconductance amplifier, acting as a source-follower. PMOS transistors are used in the photodiode reset path to allow the photodiode reset voltage to V_{ddr}. The in-pixel amplifier is biased by a global voltage $V_{PixBias}$. The pixels are connected with the output amplifier through two complementary switches. The output switches are controlled by the signals *Col*, *ColN*, *Row* and *RowN* from the scan registers. (The signals *RowN* and *ColN* are complementary to the signals *Row* and *Col*.) Figure 3 shows the timing diagram for the row and column selecting signals. The signal *SysClk* is the clock driving the scan register chains. When both the output switches are closed, the pixel is selected. The selected pixel connects to the analog output buffer and reads out the voltage. The pixel is reset at the end of the

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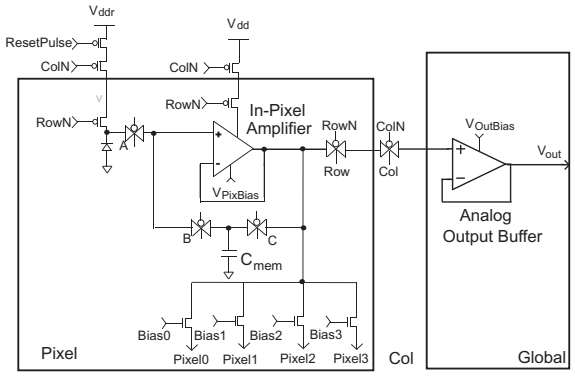

Fig. 2. Pixel to analog output buffer signal path.

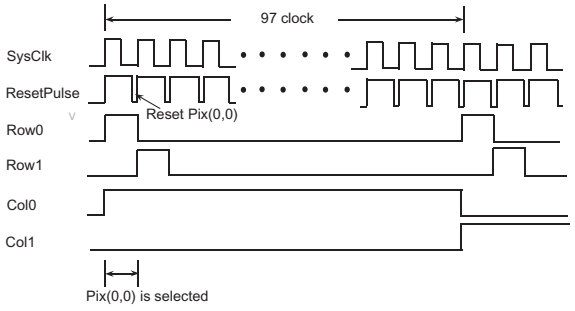

Fig. 3. Row and column timing diagram. Row0 and Col0 are the select signals for the first row and the first column.

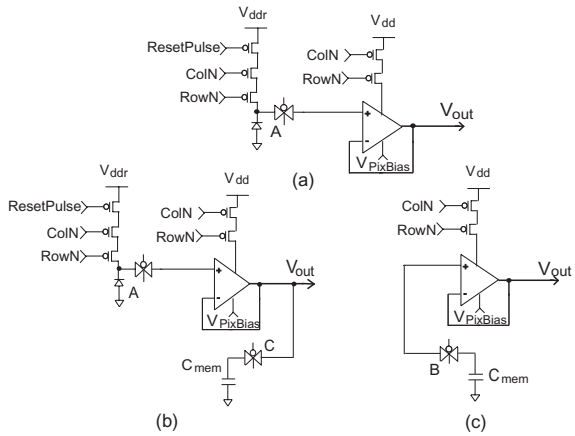

Fig. 4. Three operation modes for a pixel. Mode (a), directly read out light integration voltage. Mode (b) store the integration voltage on the analog memory. Mode (c) retrieve the stored voltage from the analog memory

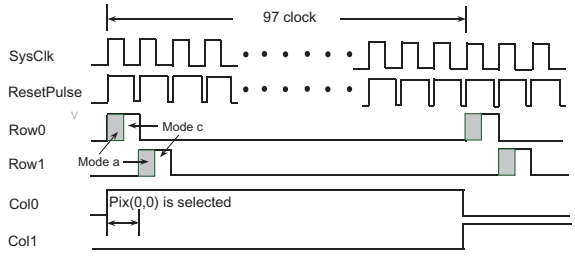

Fig. 5. Timing diagram of interleaving frame read-out. The pixels switch between Mode a and Mode c when reading out.

selection period. When the pixels are not selected, the in-pixel amplifiers are turned off to save power.

Each pixel also contains a capacitor memory to store the light integration voltage when necessary. The pixel connects with its eight neighbors with NMOS transistors. In the layout each pixel contains four NMOS transistors connecting the adjacent neighbors on the orientations of 0^o (Pixel0), 45^o (Pixel1), 90^o (Pixel2) and 135^o (Pixel3). There are three complementary switches, *A B C*, which are controlled by digital signals to implement different pixel operation modes.

C. Pixel Operation Modes

Figure 4 shows three operation modes for the in-pixel signal processing. The details of the operation modes are illustrated as follows.

Mode (a) Switch A is closed, while switch B and C are opened. The pixel acts as a standard active pixel sensor (APS) unit, connected to the output buffer. In this mode, the pixel directly reads out the light-integration voltage.

Mode (b) Switch A and B are closed, while switch C is opened. The pixel is connected to the analog memory. The integration voltage is stored on the capacitor C_{mem}.

Mode (c) Switch B is closed, while switch A and C are opened. The pixel retrieves the analog voltage from the capacitor C_{mem}.

By changing the digital control signals and the operation modes, some useful image feature-extracting functions can be achieved.

Temporal differentiation

Temporal illumination differentiation is a basic image processing function, which detects moving objects. By subtracting the current frame from a previous frame, the image sensor can filter out intensity differences usually related to motions on the scene. Transmitting these extracted data through wireless channels will prolong whole network's lifetime. The first frame is initially stored on the capacitor memories with mode (b). When reading out the second frame, the pixels switch between mode (a) and mode (c), and alternatively output the stored and the current integration voltages. Figure 5 shows the timing diagram of the interleaving output. An off-chip subtraction of two frames is used to obtain the illumination difference for each pixel.

Contour extracting

The pixels are connected through the diffusors network. The diffusors act as a spatial low-pass filter, which blur the image stored on the analog memories. The diffusor biases on different orientations are individually controlled so that the smoothing can be orientated on 0^o, 45^o, 90^o and 135^o. The smoothing operation is controlled by modulating the bias

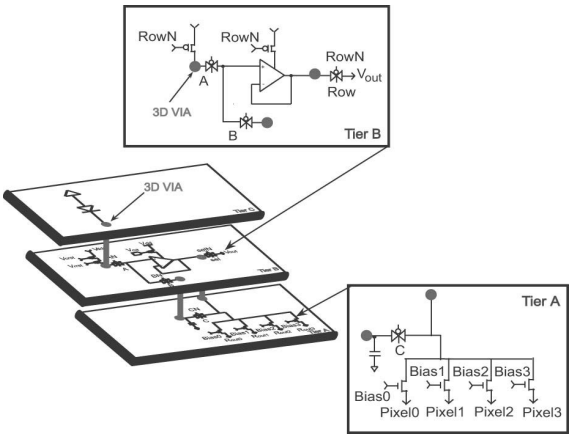

Fig. 6. Mapping of a single pixel circuit on 3 SOI layers.

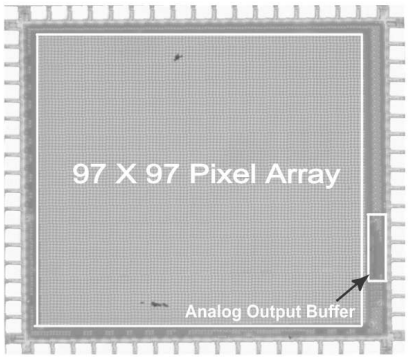

Fig. 7. Annotated 3D integrated image sensor die micrograph.

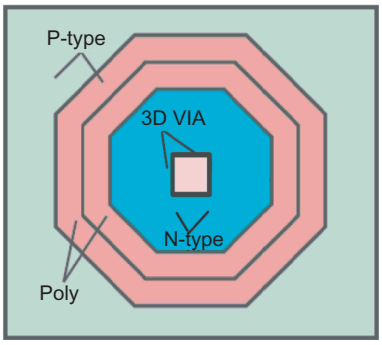

Fig. 8. The layout of fabricated photodiode.

voltages of the diffusors and the diffusion timing. The sensor alternatively reads out the diffused and the current voltages. When a diffused frame is subtracted from the current frame, an object contour can be extracted.

III. 3D Mapping of the Sensor Design

Figure 6 shows the mapping of a single pixel on the three SOI layers. The top layer is dedicated to photodiode to maximize the photodiode fill factor. The second layer contains the in-pixel amplifier and the three operation-mode switches. The bottom layer consists of a capacitor memory and four NMOS transistors connected with its neighbors. The pixel array is addressed by row/column scan registers on the middle layer, while the diffusor network is laid on the bottom layer.

IV. Test Results

The image sensor was fabricated in a research multi-project run, which uses a 3D integrated 0.18μm fully-depleted SOI process (V_{tn}=0.53V, V_{tp}=$-$0.64V) offered by MIT Lincoln Laboratory. The die micrograph of the top layers is shown in Figure 7. The process features three stacked SOI layers. Each one includes three metal layers, as well as a polysilicon layer. The circuits on different SOI layers are connected through 3D vias. The die size is 1.7$\times$1.6mm^2 and 2$\times$2mm^2 with pads, including test structures. The image sensor operates at 1.5V power supply.

Figure 8 shows the layout of our fabricated photodiodes used in the 3D integrated image sensor. The top layer is fully covered by the photodiodes, excluding the 3D vias connecting them to the middle layer. The fill factor of the top layer is 95%. Figure 9 shows the data collected from the photodiode placed in the top layer of the 3D process. We biased the photodiode at 0.5V, 1V and 1.5V, with light intensities ranging from 1 to 2$\times 10^5$lux. There is no significant difference between the bias voltage of the photodiode and its influence on the photosensitivity. The diode responsivity (R_p) is linearly modeled as $R_p = I_{in} \times 2 \times 10^{-15}$. I_{in} is the incident illumination in lux.

The electrical Quantum Efficiency (QE) for the photodiode of 3.5% at 1V bias. The low QE is due to the shallow thickness of the SOI silicon layer (50nm) and the vertical junction with small depletion region (2μm from preliminary calculations and abrupt junction [8]).

We measured the voltage output of a single pixel integration after the output buffer. The power supply is 1.5V. Figure 10 shows the pixel integration waveforms under a white light with the illuminance ranging from 0 to 2000lux. The output voltage is measured on the pad. The pixel integration capacitance C_{int} is 20fF [9]. The maximum output swing is 0.9V. The integration time of a photodiode in the dark is 10s. The photodiode dark current is estimated in equation (1).

$$I_d = C_{int} \times \frac{dV_{int}}{dt_{int}} = 20fF \times \frac{0.9V}{10s} = 1.8fA \qquad (1)$$

We experienced test difficulties due to problems with the digital circuits and the scan registers. The problems are under investigation.

V. Power Consumption

Table I shows simulated power consumption of main components on the sensor operating at 30frame/second. The power

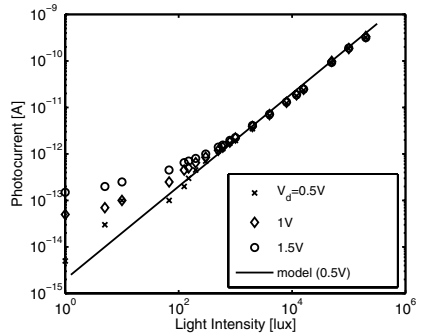

Fig. 9. Responsivity of the top-layer photodiode.

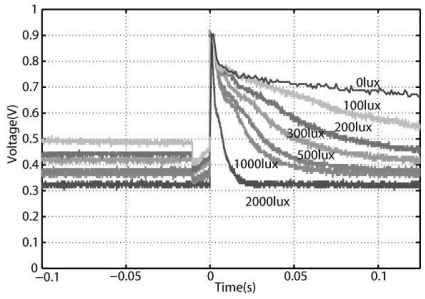

Fig. 10. The output of a single pixel integration under illuminance from 0 to 2000lux (V_{DD}=1.5V).

for an active pixel provides current for in-pixel source follower, charging/discharging of analog capacitor and resetting of the pixel. The power consumption is 1.04mW. The in-pixel source followers are turned off when pixels are not addressed. The power for an inactive pixel delivers the leakage current of photodiodes inside the pixels, which is 2.7fW. The analog output buffer consumes 2.67mW to drive 10fF capacitive load of the sensor. The power consumption for digital scan registers is 0.87mW.

VI. Conclusion

We presented a feature-extracting image sensor using a 3D integrated CMOS technology. The image sensor was fabricated on a 3D integrated 0.18μm silicon-on-insulator CMOS process. The feature-extracting image sensor is targeted to the wireless image sensor network applications. The primary parameters are summarized in Table II. The image sensor obtains the light intensity image and extracts the image features simultaneously. Because of the massively parallel, vertical connectivities, the image sensor performs more analog computations at higher speed and higher communication efficiency. The light collection efficiency is maximized when the top layer of the image sensor is fully covered by the photodiodes. The pixel fill factor is 95%. The photodiode dark current is 1.8fA. The Quantum Efficiency of the photodiode is 3.5%.

TABLE I

Simulated Sensor Power Portfolio at 30frame/second

Component	Power consumption
Analog output buffer	2.67mW
Scan-shift registers	0.87mW
Active pixel	1.04mW
Inactive pixel	2.7fW

TABLE II

Summary of Image Sensor Specification

Technology	3D integrated 0.15μm fully depleted silicon-on-insulator CMOS
Resolution	97×97 pixels
Pixel size	$15\times16\mu m^2$ photodiode APS
Pixel fill factor	95%
Die size	$1680 \times 1800\mu m^2$ $1950 \times 1950\mu m^2$ with pads
Sensor output	0 to 1V analog voltage
Estimated photodiode dark current	1.8fA
Operating voltage	1.5V

VII. Acknowledgements

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