# Phototransistor Image Sensor in Silicon on Sapphire

Joon Hyuk Park, Eugenio Culurciello
Electrical Engineering Department
Yale University
New Haven, CT 06520
joonhyuk.park, eugenio.culurciello@yale.edu

***Abstract*— We present a back-illuminated 32 x 32 pixel image sensor in 0.5-$\mu$m silicon-on-sapphire process. The imager performs "snap-shot" image acquisition and analog readout at a continuous rate of thousands of frames/s and consumes as little as 250 $\mu$W. Each pixel consists of a phototransistor and a memory capacitor in 40 $\mu$m x 40 $\mu$m with a fill factor of 43%. The image sensor is suited for hyper-spectral imaging at high speeds.**

## I. Introduction

In recent years, silicon-on-insulator (SOI) circuits have been used for a variety of applications. Several groups have shown working photodetectors [1], [2]. However, there is no working system in existence - only characterizations and simulations of full image arrays are available [3], [4], [5], [6].

In this paper, we present an image sensor array implemented in Peregrine Semiconductor's silicon-on-sapphire (SOS) technology [7]. As opposed to other SOI technologies, SOS features an insulating and transparent sapphire substrate that makes it ideal for optical applications.

The image sensor presented in this paper features the following innovations: (1) It is the first fully-functional array implemented in SOI/SOS technology, (2) it can be operated with back illumination, (3) the pixels feature a reflector that allows light to pass twice through the photodetector, (4) it was designed to be able to operate at 1000s of frames per second, (5) it is intrinsically radiation tolerant.

The sapphire substrate in SOS is optically transmissive from the UV (200 nm) to the infrared (5500 nm) spectrum [8], and makes this device favorable for hyper-spectral imaging in multiple bands with the use of back illumination. The back illumination also allows the pixels to have higher fill factors than traditional CMOS photodetectors because the metalization layer will not block the light. The tolerance to ionizing radiation makes this SOS image sensor suitable for outer-space instrumentation.

We engineered a fully-functional camera pictured in Figure 1 based on the SOS image sensor. The camera can be operated by any computer with an USB port.

The rest of the paper is organized as follows. In Section II, we describe the architecture and operation of the image sensor. In Section III, we describe the details of the complete camera system. In Section IV, we describe the test setup and chip characterization results including linearity, fixed pattern noise, sample images, and power consumption.

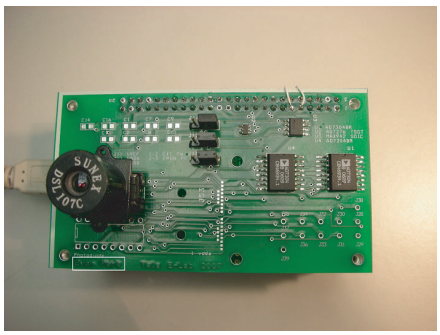

Fig. 1. A camera designed for our SOS image sensor. The image sensor is mounted on a custom-built PCB with external components connected to the USB-based FPGA board.

## II. System Overview

The image sensor was designed in a 0.5-$\mu$m silicon-on-sapphire process. The block diagram of the image sensor is shown in Figure 2. The array is composed of 32 x 32 pixels. A scan shift register is used to address individual pixels. A global operational amplifier is used as a buffer to convey the pixel integration voltages to the output.

The pixel is shown in Figure 3. The size of each pixel is 40 $\mu$m x 40 $\mu$m with a fill factor of 43%. The capacitor is used as a memory element to store the integrated voltage. The *Read* signal connects/disconnects the phototransistor from the rest of the pixel circuitry. *S1* and *S2* signals connect the storage capacitor to the phototransistor. The *Reset* signal shorts the capacitor, resetting the capacitor voltage to a pre-defined value (voltage at the *Bias* pin). *ColSel* is a signal from the scan shift register to connect the storage capacitor to the *Out* pin. The *Vdda* pin is set to 3.3V and *Out* is connected to the input pin of the global operational amplifier.

A normal pixel operation consists of three phases, as shown in Figure 4. First, the storage capacitor is reset to an initial value (voltage at the *Bias* pin) during the reset phase by setting the *Reset* pin to *VDD*, which shorts the storage capacitor. Then, during the integration phase, *Read* is set to *VDD*, connecting the phototransistor to the rest of the pixel circuitry. *S1* is set to *VDD*, *S2* is set to *GND*, and *Reset* is set to *GND*, which connects the phototransistor to the capacitor. The current from the phototransistor discharges the capacitor as a function of the light intensity. Lastly, during the read out phase, *Read* is set to *GND* and the scan shift register sets *ColSel* to *GND*. This

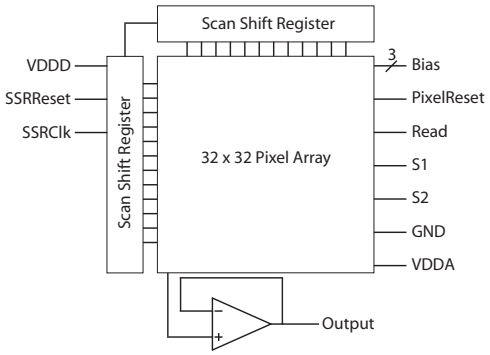


Fig. 2. Block diagram of the image sensor. The system is composed of a 32 x 32 phototransistor array. The two scan shift registers are used to access the individual pixels. A global operational amplifier is used as a buffer to the output.

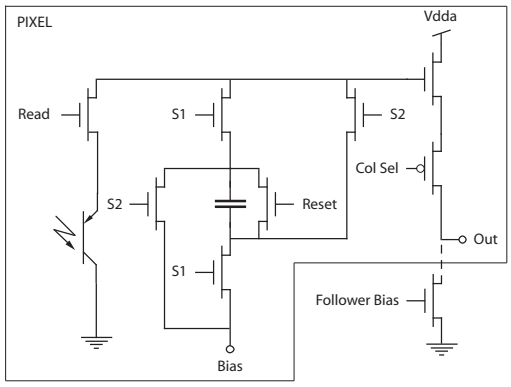


Fig. 3. Pixel schematic. The *Read* signal connects/disconnects the phototransistor from the pixel. *Reset* switch shorts the storage capacitor to *Bias* voltage. *S1* and *S2* signals connect the capacitor to the phototransistor and the output. *ColSel* is controlled by the scan shift registers to select the pixel.

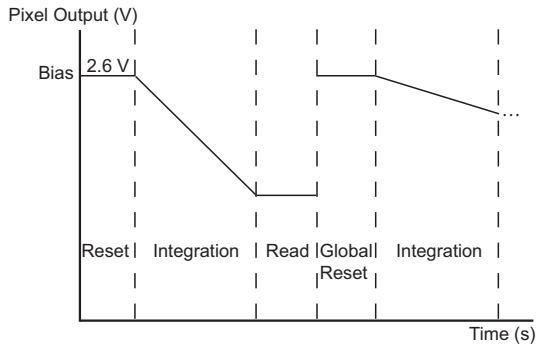


Fig. 4. The three phases during a normal operation of the pixel. (1) During Reset, the storage capacitor is set to the voltage at the *Bias* pin. (2) During Integration, *S1* is set to *VDD* and *S2* is set to *GND*, which discharges the storage capacitor relative to the light intensity at the phototransistor. (3) During Read, the transistor is disconnected by setting the *Read* signal to *GND* and the capacitor stops discharging. This process is repeated for video streams.

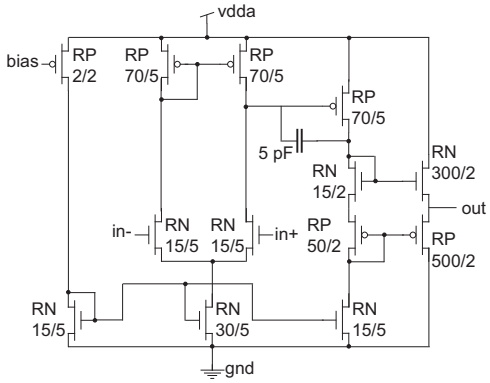


Fig. 5. The global operational amplifier is set up as a non-inverting amplifier with a gain of 1 (voltage buffer). The output of the amplifier is fed back into the negative input and the positive input is connected to the pixel output.

connects the storage capacitor to *Out*, which is connected to the global operational amplifier.

The *S2* switch was designed to allow frame differencing on pixel. The first frame would be stored in the capacitor while *S1* is set *VDD* and *S2* to *GND*. Then, the second frame would be stored by setting *S1* to *GND* and *S2* to *VDD*. However, due to capacitive coupling between the capacitance of the photodetector and the storage capacitor during the switching, there is a voltage offset between the two frames related to light intensity and the frame subtraction feature cannot be used.

The image sensor performs a "snap-shot" image acquisition [9] because all the pixels are reset at the same time and integrate over the same interval before being read out. Unlike image sensors with rolling shutters [10], motion artifacts are not a problem for the image sensor.

The global operational amplifier in Figure 5 is connected in a feedback loop and has a gain of 1. The primary purpose of the operational amplifier is to act as a voltage buffer between the output of the pixel and the rest of the system circuitry.

## III. Camera System

An OpalKelly XEM3001 FPGA integration module was used to measure the performance of individual phototransistors and the image sensor (Figure 1). The XEM3001 controlled a digital-to-analog converter (AD7304) to bias the image sensor and an analog-to-digital converter (AD7276) to convert the analog output of the image sensor for memory storage. The XEM3001 also provided the necessary digital signals to operate the image sensor. A graphical user interface was designed to control the whole system. The GUI has the ability to capture a still-frame from the camera as well as a continuous sequence of frames.

## IV. Testing and Characterization

The nonlinearity of the phototransistor was measured by observing the photocurrent integration curve at different light intensities. The photocurrent generated by the phototransistor is not initially linear, but settles to a linear curve after certain amount of time. The initial nonlinearity is shown in Figure 6. The nonlinearity reduces the total possible integration time. At 256 lux, the phototransistor saturates after 25 $\mu$s. Under

normal conditions, anything below 200 fps (greater than 4 ms integration time) results in a saturated image.

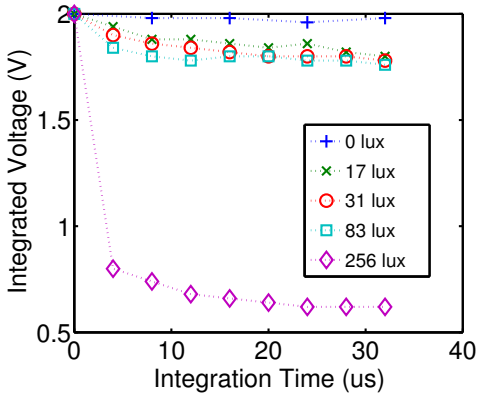


Fig. 6. Initial nonlinearity of the phototransistor. The data was gathered by measuring the integration voltage at different light intensities. Due to the nonlinearity, the phototransistor saturates after 25 $\mu$s at 256 lux.

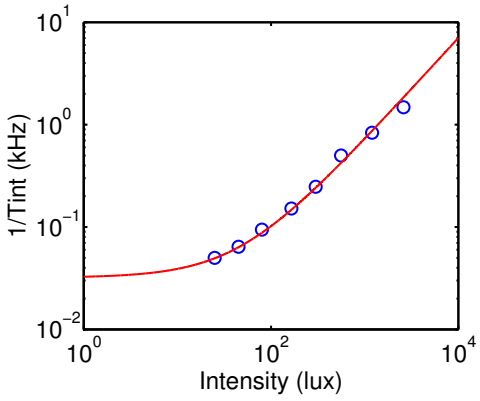


Fig. 7. Linearity of the phototransistor and model fit. The data was gathered by measuring the integration time of 1 V at different light intensities. The equation of the linear model is ${T_{int}}^{-1} = 0.7 \cdot L_I + 32$.

The time to integrate 1V at different intensities was measured to determine the integration characteristics of the phototransistor. A dispersing filter was placed between a white light source (Genesys LS-150) and the image sensor. The light intensities were measured using a commercial photographic digital lux meter.

The integration time ($T_{int}$) and the light intensity ($L_I$) have an inversely linear relationship for the phototransistor at certain light intensities, as shown in Figure 7. Since the change in voltage (1 V) and the capacitance of the storage element (200 fF) is known, the current drawn by the phototransistor relative to the light intensity can be calculated using the measured relationship between integration time and intensity (Eq. (3)). This relationship between the current drawn by the phototransistor ($I_{in}$) and the intensity is shown in Eq. (4), where the coefficient is $1.4 \cdot 10^{-13} A/lux$ and the dark current is $6.4 \cdot 10^{-12} A$.

$$I_{in} = 200fF \cdot \frac{1V}{T_{int}} \quad (1)$$

$$T_{int}^{-1} = \frac{I_{in}}{(200fF)(1V)} \quad (2)$$

$$= 0.7 \cdot L_I + 32 \quad (3)$$

$$I_{in} = (1.4 \cdot 10^{-13}) \cdot L_I + (6.4 \cdot 10^{-12}) \quad (4)$$

The quantum efficiency of the phototransistor was obtained by using the model derived from the integration characteristics (Eq. (1)). A HORIBA Jobin Yvon Fluoromax-3 generated wavelengths from 275 nm to 1000 nm. The calculated photocurrent was compared to the photocurrent from a Newport 818-UV photodiode with known spectral responsivity under the same conditions. The quantum efficiency of the backside phototransistor is shown in Figure 8. The SOS phototransistor has a higher quantum efficiency in near UV. However, at longer wavelengths, the quantum efficiency drops off because the thickness of silicon in the SOS process is 95 nm. This results in a depletion region thinner than traditional CMOS processes and photons at longer wavelengths do not generate electron-hole pairs.

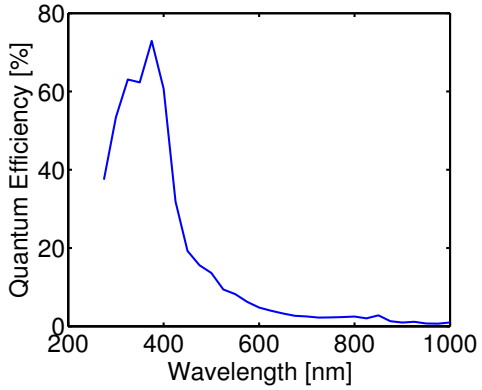


Fig. 8. Quantum efficiency of the backside phototransistor. The peak occurs at 375 nm.

The output of the image sensor at different frames rates and power consumption are shown in Figure 9. The phototransistor operates correctly with a F/# 2.4 lens even at 1200 frames per second (200 $\mu$s integration time) with the help of a contrast boosting algorithm.

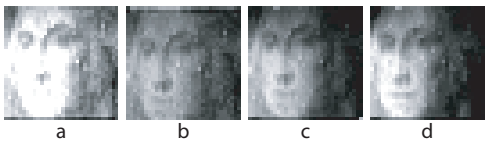


Fig. 9. Image captured with lens at various frame rates: (a) 200 fps, (b) 500 fps, (c) 1000 fps and (d) 1200 fps.

Another three sets of images (of 64 frames each) were captured to measure the fixed pattern noise of the image sensor. First, the image sensor was placed in the dark and the

photodetector signal was integrated for 10 $\mu$s to calculate the reset noise. Next, the image sensor was placed in the dark and the photodetector signal was integrated for 100 $\mu$s to measure the dark current. Lastly, light was focused on the image sensor and adjusted to be near saturation point for a given integration time for 30 fps to calculate the gain noise. The fixed pattern noise was calculated using the standard deviations of each pixel over the 64 frames were calculated and the mean of the standard deviations of the 1024 pixels were calculated for the above three cases. The standard deviation was 4.3 mV for a short integration time (10 $\mu$s) in the dark with a swing of 17.7 mV, 7 mV for a long integration time (100 $\mu$s) in the dark with a 51.6 mV swing, and 39.8 mV when the image sensor was close to saturation while running at 200 fps with a 1.4 V swing. The signal-to-noise ratio was calculated by taking the mean swing of each pixel at near saturation over 64 frames and dividing it by the mean of the standard deviation of each pixel over 64 frames.

The power consumption was measured by observing how much current the image sensor was drawing through the *VDDD* and *VDDA* lines. The global operational amplifier and the pixels are powered by *VDDA* and the scan shift registers are powered by *VDDD*. A Keithley 2400 General-Purpose SourceMeter was used to measure the current. The scan shift register consumes 45 $\mu$W, while the phototransistor array and the global operational amplifier consume 200 $\mu$W. The power consumption remained constant for all frame rates tested.

The operational amplifier is able operate up to 10.5 MHz, or 10250 fps and is the limiting factor in the system. Also, the analog-to-digital converter used in the system is only capable of 3 MSPS, thus no images above 3000 fps can be obtained unless we use a faster ADC.

## V. Conclusion

We have presented the first fully-working back-illuminated image sensor in SOS 0.5-$\mu$m process that is very sensitive at lower wavelengths. The image sensor has a resolution of 32 x 32 pixels. Each 40 $\mu$m x 40 $\mu$m pixel contains a phototransistor and memory capacitor. Pixel reset, integration and output occur in full frame "snap-shot" fashion. The image sensor is able to achieve continuous 2900 frames/s operation and can consume as low as 250 $\mu$W of power. A better operational amplifier and analog-to-digital converter will greatly improve both the analog read out and digital conversion speeds up to 10250 frames/s.


## Acknowledgment

The authors would like to acknowledge the many contributions of Aleksandar Vacic and Wei Tang.


TABLE I

Image sensor properties

| | |
|---|---|
| Technology | 0.5-$\mu$m silicon-on-sapphire |
| Array Size | 32 (H) x 32 (V) |
| Total Size | 1.5mm x 1.5mm |
| Pixel Size | 40$\mu$m x 40$\mu$m |
| Fill Factor | 43% |
| Power Consumption | 250 $\mu$W (@ 3.3V) |
| Fixed Pattern Noise | 4.3 mV (dark, 10 $\mu$s integration)<br>7.0 mV (dark, 100 $\mu$s integration)<br>39.8 mV (light, before saturation) |
| Output Voltage Swing | 1.5 V |
| Dark Current | 6.2 pA |
| Conversion Gain | 0.8 $\mu$V/e- |
| SNR | 31 dB |
| Max Frame Rate | 2900 fps (limited by ADC) |

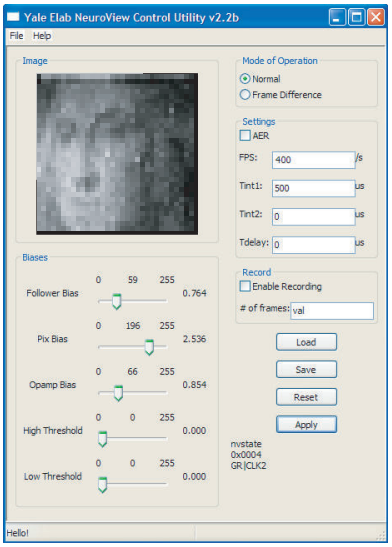


Fig. 10. GUI to control the image sensor system.

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