An Integrated Patch-Clamp Amplifier for High-Density Whole-Cell Recordings

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***Abstract*— We fabricated an integrated patch-clamp amplifier capable of recording nano-amperes of current in whole-cell patch recording. Patch-clamp amplifiers presently consist of a head-stage and a large controller box that contains many hundreds of components. Our design compresses the function of the head-stage and the controller box into one chip that can be mounted near the patch-clamp electrode and can be controlled through a high-speed serial bus paving the way for higher densities in parallel patch-clamp systems. We report on the electrical measurements from the fabricated device.**

I. Introduction

Patch-clamp is a technique used in electrophysiology to measure the currents flowing through the membranes of living cells. These recordings are crucial for the study of ion channels, which are membrane structures responsible for cell membrane conductivity [1], [2]. A patch-clamp can measure the cell conductance as it depolarizes and is normally used to study the effect of drugs and medical treatment on the dynamics of action potentials. The progress of ion channel research and the study of living cells are strictly related to the availability of advanced instruments. Emerging integrated circuit technologies, especially the planar patch-clamp technology, is beginning to make large-scale screens of genes and compounds possible [3], [4], [5].

Due to the importance of the patch-clamp recording technique in drug testing, pharmaceutical companies have long sought ways to increase the number of recordings per unit time [6]. The need for higher throughput screening instrumentation is thus a limiting factor for pharmaceutical companies' efforts to bring better and safer medicines to the consumer market [7]. A previous paper by our group showed the feasibility of using a high-performance integrated patch-clamp amplifier to provide low noise amplification of ion-channel currents [8]. An integrated version of the patch-clamp amplifier not only reduces noise but also obtains better electrical performance, since cabling and parasitic capacitances that lower the measurement bandwidth are kept to a minimum. The integrated amplifier can be employed in high density parallel patch-clamp systems that would increase the throughput of drug testing. This paper advances the previous integrated circuit designs [9], [8] by incorporating a capacitive compensation loop that compensates for the stray electrode capacitance and a resistive compensation loop that compensates for the voltage drop across the the recording electrode. This design also differs from previous design [8] because it uses a continuous-time amplifier with resistive feedback instead of a delta-sigma head-stage with capacitive feedback. Our patch-clamp amplifier uses a custom designed high-performance low-noise operational amplifier to provide amplification.

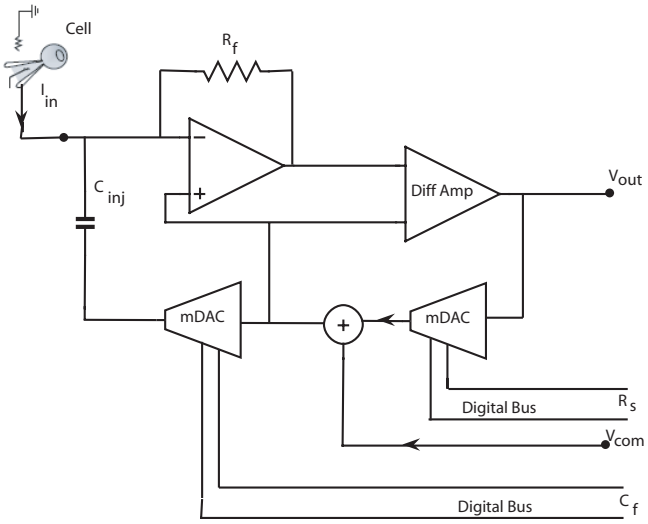

Fig. 1. Patch-clamp amplifier overview. A trans-impedance amplifier followed by a difference amplifier produces an output proportional to the input current. Two feed forward loops compensates for the series resistance and stray capacitance. The amount of compensation is controlled by two multiplying digital to analog converters (mDAC)s.

II. System Overview

The current measured in whole-cell patch recording is typically in the range of a few nano-amperes. Command voltage steps (V_{com}) between 10mV and 100mV are applied to the membrane during experiments, in order to activate ion channel proteins and to permit ionic currents to flow across the membrane. Currents are bidirectional depending on the channel type and the membrane potential. The bandwidth of interest is between a few Hz to 10 kHz [6]. A block diagram of our patch-clamp system is shown in Fig 1.

The system consists of an input current-to-voltage trans-impedance amplifier that uses a feedback resistor R_f along with a difference amplifier which subtracts the command

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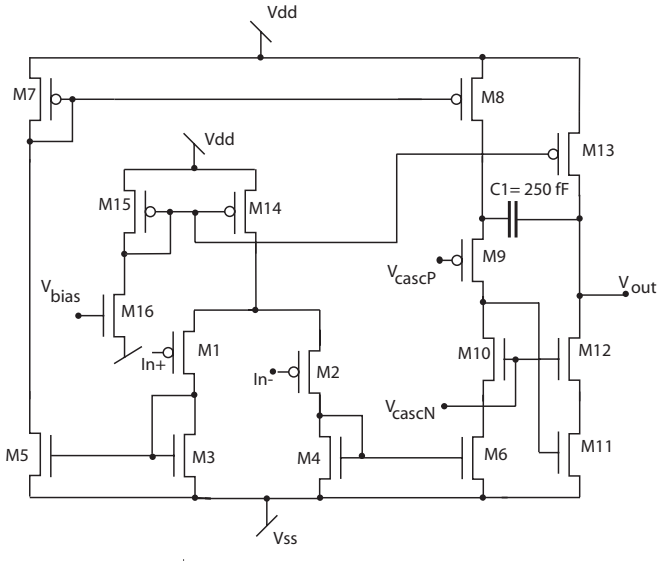

Fig. 2. The operational amplifier used in the design. The input stage was optimized for low noise performance.

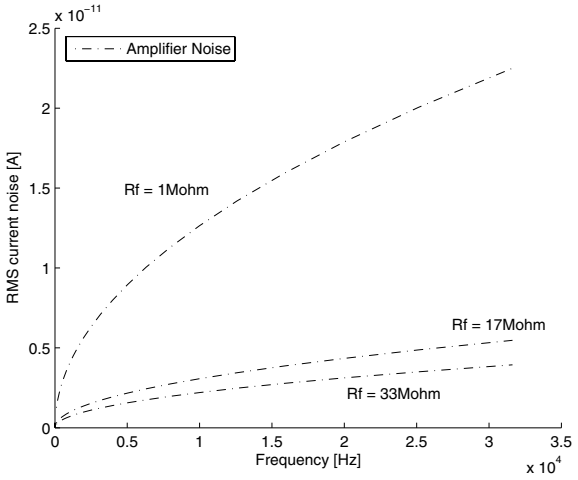

Fig. 3. Total rms noise of the patch-clamp amplifier with varying values of R_f.

voltage from its output. The resultant output voltage is proportional to the input current, as in equation (1).

$$V_{out} = I_{in} R_f \tag{1}$$

The system also has two compensation circuits. The first is a series resistance compensation loop which compensates for the voltage drop across the series resistance. A digital setting of the compensated resistance R_S is applied to a multiplying digital to analog converter (mDAC). This mDAC scales the current monitor signal V_{out} and adds it to the command membrane potential V_{com} in positive feedback polarity. The second compensation for 'fast' capacitance is necessary to remove the effect of electrode's stray capacitance from introducing errors into the R_S compensation. The fast capacitance compensation is a feed-forward loop in which a small capacitor C_{inj} of 5 pF injects a current that is scaled to match the charging current of the electrode capacitance typically of 1-2 pF in typical electrodes and any other parasitic capacitance. The scaling of the injected current is set by a mDAC using a digital setting of C_f.

III. System Components

There are three main components in the circuitry of the chip: the trans-impedance amplifier, the difference amplifier, and the mDACs used in capacitive and resistive compensation feedback loops. All amplifiers are implemented using a low noise three stage operational amplifier shown in Fig 2. The input differential stage is followed by a second stage which allows for higher output swing. The third stage is an output stage. The input V_{bias} sets the quiescent point for the circuit and the inputs V_{cascP} and V_{cascN} provide biases to the cascode devices in the second stage that increases the bandwidth of the operational amplifier.

The patch-clamp technique is extremely sensitive to noise due to the low amplitude of the membrane current and hence low-noise amplification is critical to our design. The critical parameters for low noise amplifier design are the input capacitance, the voltage noise and the input leakage current. The input transistors are vital in establishing these characteristics. The gate capacitance C_g of the input MOSFET is proportional to the area of the transistor, while the thermal noise e_n decreases as the square root of the area (assuming constant gate length). The noise of the recording system is proportional to $C_{in}e_n$ where the total input capacitance is C_{in} = C_g + C_{el} with C_{el} being the capacitance of the electrode and any other capacitance on the input node. The optimal gate can be shown to be the gate width corresponding to C_g = C_{el}. The flicker noise due to the trapping of charges below the gate of the transistor is a significant problem in making low-noise measurements using MOSFETs. This problem was alleviated using P-channel transistors which have been shown to have one or two orders lower flicker noise than n-channel devices [10]. As discussed in section II, the trans-impedance amplifier multiplies the input current by R_f to produce a voltage proportional to the input. The current noise at the input can be shown to be inversely proportional to R_f. However, the parasitic capacitance and the physical size of of R_f in layout limits its maximum usable value. A conservative R_f of 25MΩ was chosen for our design. This yields an output noise level of about 4pA rms at a 10kHz bandwidth which gives a signal to noise ratio of - 1nA/4pA = 250 in whole-cell measurements. The total noise as a function of feedback resistor R_f is shown in Fig 3. The slew rate of the operational amplifier was measured to be 1.5 $\mu V/s$. The input dynamic range of the amplifier was measured to be 2V pk-pk. The gain-bandwidth product was measured as 2MHz.

A schematic of the difference amplifier is shown in Fig 4. In our design RD_x =10kΩ and the output of the difference amplifier is related to its input by equation (2). Therefore,

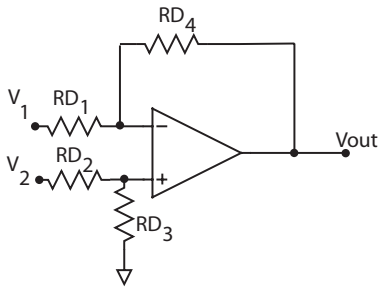

Fig. 4. The difference amplifier used in the design.

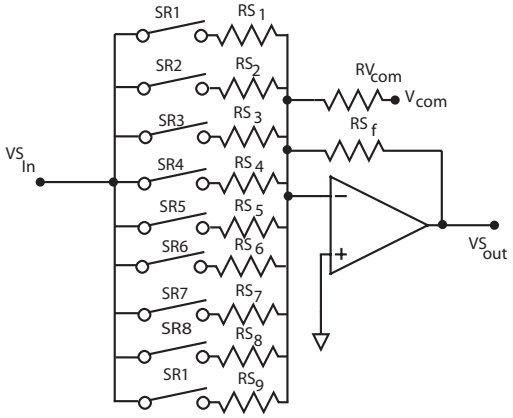

Fig. 5. The series resistance compensation mDAC. The mDAC scales the current monitoring output voltage (v_{out}) by a value set by a digital serial bus and adds it to the command voltage V_{com}

the input voltage step V_{com} subtracted from the output of the trans-impedance amplifier resulting in an output voltage proportional to the input current.

$$V_{out} = V_2 - V_1 \tag{2}$$

The series resistance compensation mDAC scales the current monitoring output voltage of the difference amplifier by an external digital value. The mDAC was designed to scale the output voltage between 0.1-30 times (9 bit resolution). A diagram of the 9 bit DAC is shown in Fig 5. The series resistance compensation mDAC was implemented as a summing amplifier using branches 1-9 that has input resistances RS_1-RS_9 and switches SR_1-SR_9. The summing amplifier also consists of a feedback resistor RS_f. If switch SR_i is closed then a scaled version of input voltage VS_{in} given by equation (3) appears at the output VS_{out} of the summing amplifier.

$$VS_{out} = -\frac{RS_f}{RS_i} \times VS_{in} \tag{3}$$

In addition to the branches that scale the voltage output, the summing amplifier also contains an additional tenth branch with input resistance RV_{com}=RS_f which adds the command voltage V_{com} with a gain of negative one to the output of the summing amplifier. Therefore, the total output at the summing

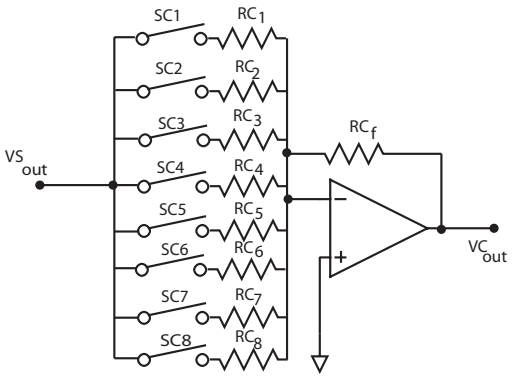

Fig. 6. The capacitive compensation mDAC. The mDAC scales the output of the serial compensation voltage (vout) and connects it to Cinj which injects a current that tries to match the charging current of the electrode capacitance.

amplifier when switch SR_i is closed is given by equation (4).

$$VS_{out} = -[\sum \frac{RS_f}{RS_i} \times VS_{in} + V_{com}] \tag{4}$$

In our design, RS_f was chosen as 10kΩ and values of 612.5Ω, 1.25kΩ, 2.5kΩ, 5kΩ, 10kΩ, 20kΩ, 40kΩ, 80kΩ and 160kΩ were chosen for resistors RC_1-RC_9 respectively. Hence if one desires to add 2 times the output voltage of the difference amplifier to V_{com}, one would close SR_4 and leave SR_{1-3} and SR_{5-9} open.

The mDAC for capacitive compensation scales the output of the serial compensation mDAC and connects to a small capacitance C_{inj} which injects a current that matches the current charging the electrode capacitance. The compensation value is 1-2 times the output voltage of the series resistancs mDAC and has eight bit resolution. The implementation of the mDAC for capacitive compensation is identical to the implementation of the series resistance mDAC and is shown in Fig 6.

When switches SC_i are closed, the output of the capacitive compensation mDAC is given by equation 5.

$$VC_{out} = -\sum \frac{RC_f}{RC_i} \times VS_{out} \tag{5}$$

IV. Results

We tested the integrated patch-clamp amplifier by sourcing a range of inputs currents from a fraction of a nano-ampere to a few nano-amperes, while recording the output voltage. The amplifier was powered at 3.3V using an external battery and the biases and the command voltage was provided by an Analog Instruments AD7304 digital to analog converter (DAC) controlled through an Opal Kelly 3010 FPGA board. The output of the amplifier was digitized using an Analog Instruments AD7475 analog to digital converter (12 bit resolution). The voltage noise on the power supply and the bias voltages was measured as less than 10mV (corresponding to a 0.4nA rms of input-referred current noise). The input current was sourced by applying a V_{com} of 100mV across a variable resistance of 18MΩ to 120MΩ. We obtained a linear dependency across the

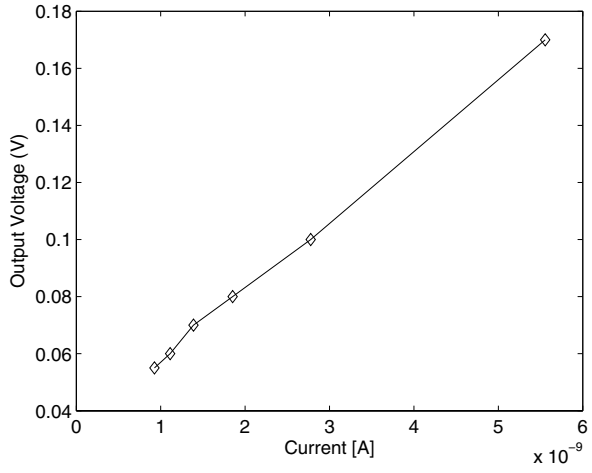

Fig. 7. Output voltage of the integrated patch clamp amplifier as a function of input current.

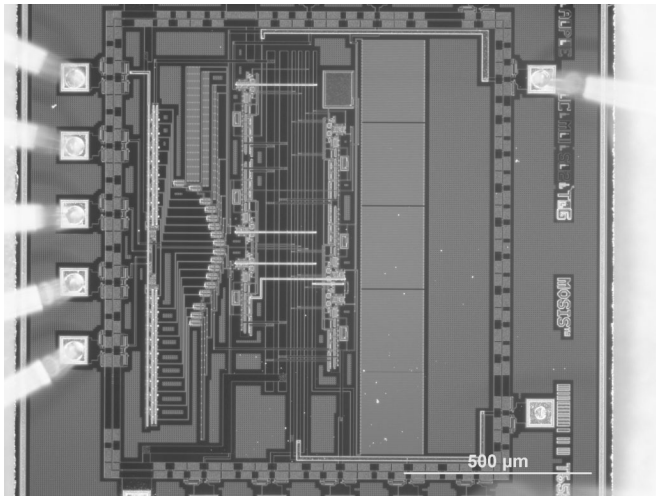

Fig. 8. Figure 7. Die micrograph of the integrated patch-clamp amplifier

entire range of tested currents as shown in Fig 7. The feedback resistance of the device was measured to be 25MΩ through a linear fit of the data and is identical to the theoretical value. The devices consumed 3.3mW of power when operated with a 3.3V power supply. Tests are currently underway to determine the usefulness of the resistive compensation and capacitive cancellation circuits in a real patch-clamp experiment and will be reported in a future publication.

The die size of the integrated patch clamp amplifier is 1479 μm x 1316 μm. A micrograph of the fabricated die is shown in Fig 8.

V. Summary

We designed, fabricated and assembled an integrated patch clamp amplifier with capacitive and serial resistance compensation targeted for whole-cell patch-clamp measurements. The device uses a transimpedance amplifier to convert an input current to a voltage output. The prototype was fabricated on conventional AMI 0.5 micron technology. The device is capable of measuring nano-amperes of current. This integrated patch-clamp amplifier is the enabling technology for high density parallel patch-clamp systems.

VI. Acknowledgements

This work was partly funded by US ARO award W911NF-06-1-0336. The authors would like to thank Ryan Munden for his support with wirebonding.

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