An integrated Silicon-on-sapphire Patch-clamp amplifier

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***Abstract*— We fabricated an integrated patch-clamp amplifier capable of recording from pico- to tens of micro-amperes of current. The high-dynamic range of seven decades and the pico-ampere sensitivity of the instrument was designed for whole-cell patch-clamp recordings. The prototype was fabricated on a 0.5μm silicon-on-sapphire process. The device employs an integrating headstage with a frequency-modulated output pulse ranging from 3Hz to 10MHz. A digital interface produces a 16bit output conversion of the input currents. We report on electrical measurements from the fabricated device, and measurements conducted on cells in a typical patch-clamp experiment.**

I. Introduction

Patch-Clamp is an extraordinary technique used in electrophysiology to measure the currents flowing through the membranes of living cells. These recordings are crucial for the study of ion channels, which are the molecular structures responsible for the membrane conductivity [1], [2]. Patch-clamp can measure the cell conductance as it depolarizes and is normally used to study the effect of drugs and medical treatments on the dynamics of action potentials. The progress of ion-channel research and the study of living cells is strictly related to the availability of advanced instrumentation. Emerging integrated circuit technologies, especially the planar patch-clamp technology, are beginning to make large-scale screens of genes and compounds possible.

In this paper we present a high-performance integrated patch-clamp amplifier. Our design employs emergent integrated circuit technologies to provide low-noise amplification of ion-channel currents and high-density integration of electronic components. The silicon-on-sapphire (SOS) fabrication process for integrated circuits [3] features a non-conductive substrate and high-quality component isolation.

II. System Overview

Ion channel currents range from a few pico-amperes for single-channel recordings to tens of nano-amperes for whole-cell measurements. Voltage steps between 10mV and 100mV are applied to the membrane during an experiment, in order to activate ion channel proteins and permit ionic currents to flow across the membrane. Currents are bi-directional, depending on channel type and membrane potential, and the bandwidth of interest is between a few Hertz to 10kHz in bench-top systems. Higher sampling rates and bandwidth are desired for more precise characterization of ion channels. The patch-clamp amplifier must have a large dynamic range

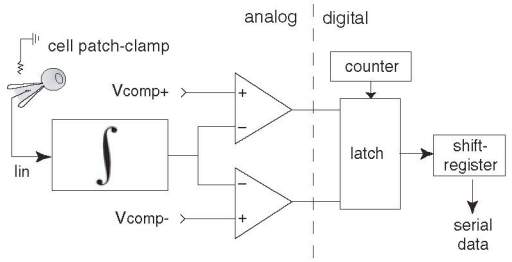

Fig. 1. Patch-clamp amplifier overview. The analog portion of the circuit integrates the input current up to a positive or negative threshold V_{comp+} and V_{comp-}. After integration, a digital pulse latches an oversampled 16-bit counter to produce a digital output.

in order to record the large transient currents after the stimuli, and must be highly sensitive to currents in the pico- to nano-ampere range. To this purpose, we have designed an integrated circuit based on asynchronous sigma-delta analog-to-digital converters. The sensor is based on a pulsed-output current integrator circuit with reset frequency proportional to the input current. This architecture permits high oversampling ratios at the bandwidths of interest. A block diagram of our patch-clamp system is shown in Figure 1.

The input current is integrated over a capacitor until the integrator output reaches either of the compare voltages V_{comp+} or V_{comp-}. At the end of integration, the change in the comparator's state generates a pulse. The digital components of the system comprise a 16-bit counter, latch and shift-register. The counter is free-running, and its value is latched when a pulse from the analog circuitry is detected. This value is then transferred to the shift-registers, and serially communicated to a computer-based data-acquisition system. Since the output data is oversampled and synchronous by means of an external clock, the time between two integration pulses can be measured accurately. The difference between two latched values thus yields the integrator's reset frequency. This frequency can be used along with the system transfer function in equation 1 to calculate the input current.

$$I_{in} = C_{int} \Delta V f_{pulse} \tag{1}$$

I_{in} is the input current, C_{int} the integration capacitance used in the integrator, and ΔV is the voltage swing of the integrator.

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III. System Components

The patch-clamp technique is very sensitive to noise, due to the low amplitude of the membrane current. In order to minimize the impact of the noise sources in our integrated system, we have employed a switched-capacitor implementation [4]. This realization also reduces the power consumption. The major sources of noise in the patch-clamp amplifier circuits are Johnson noise, shot noise and flicker noise. Flicker noise is the dominant source of noise in integrated MOSFET circuits. It is caused by the entrapment of electrons in the transistor gate-oxide and varies as the inverse of operating frequency, becoming a serious problem at the low frequencies of operation of the patch clamp amplifier. Since it is a noise correlated in time, flicker noise can be subtracted using Correlated Double Sampling (CDS). The switching capacitors introduce reset noise (kT/C) but the noise generated by this source is minor in comparison to the headstage shot noise, which is the dominant noise source in our system. An analysis of the noise sources in our system shows that at a sampling frequency of 10kHz, we expect 2.5pA rms noise current while measuring a 3nA input current.

There are two main components in the analog circuitry of our chip: the *integrator* and the *comparator*. All amplifiers are implemented using single-stage cascoded inverters which offer high-gain and low noise when operated in the sub-threshold region. The active transistor loads on the input transistor increase the gain of the inverter. The gain of the amplifier can be controlled by tuning V_{bias} and operating the circuit in the high-gain subthreshold region. The gain was measured in simulation to be 2000, and to vary only 2% with a 10K temperature change.

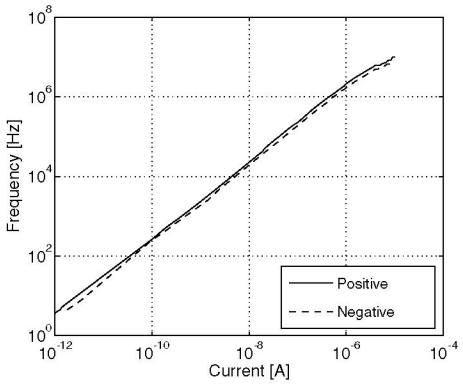

Fig. 2. Output pulse frequency of the headstage integrator as a function of positive and negative input currents, as integrated on a 600fF capacitor. The dynamic range of the patch-clamp amplifier was measured to be 7 decades.

IV. Results

We tested the integrated patch-clamp amplifier by sourcing a range of input currents from a few micro-amperes to a pico-ampere, while recording the frequency of the output pulse. We obtained a linear transfer function across the entire range of tested currents in the range: [3pA, 10μA], as shown in Figure 2. The output pulse frequency was in the range: [3Hz, 10MHz], and was observed to increase in discrete steps when very high currents were sourced, as quantization noise due to low oversampling became dominant. We operated the device with clock frequencies of up to 50MHz, and were thus able to extend the upper-limit of the current measurements. The use of fast clocks and the silicon-on-sapphire process make this device one of the largest dynamic-range current measuring system reported [4].

V. Experiments

To verify the usefulness of the patch-clamp amplifier in life-science applications, we used the patch clamp amplifier to measure the ionic conductances of rat basophilic leukemia cells (RBL). The data collected from the RBL cells is due to inward rectifier potassium channels, which conduct only in the inward direction. Figure 3 show the time response as step voltages are applied to the RBL cells. The y-axis shows the measured voltage, which relates linearly to the measured current.

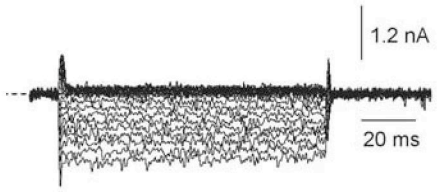

Fig. 3. Patch clamp measurement of membrane currents in a RBL cell. Currents recorded in response to repeated step changes in membrane potential from -200mV to +200mV, incremented by 10mV. The current represents the inward rectifier current native to these cells.

VI. Acknowledgements

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