An Ultra-Low Power Silicon-on-Sapphire ADC for Energy-Scavenging Sensors

Zhengming Fu, Eugenio Culurciello
Electrical Engineering Department
Yale University
New Haven CT 06520
{zhengming.fu, eugenio.culurciello}@yale.edu

***Abstract*— We designed and fabricated an 8-bit analog-to-digital converter (ADC) in a 0.5μm Silicon-on-Sapphire CMOS technology. The ultra-low power and low voltage design of the ADC was targeted for wireless sensor interfaces and energy-scavenging systems. The ADC is capable of 4.5MHz operation, producing 409kS/s, consuming 3μWatt at 1.5V power supply. It uses an active area of 615×782μm^2. The acceptable input range is 0.97V at 1.5V power supply.**

I. Introduction

The recent years have witnessed remarkable progress in the field of untethered sensors. Many pioneering applications have demonstrated that networks of sensors can tremendously advance the scientific efforts to understand indoor, natural, civil and tactical environments by providing information from locations that were not reachable before [1]. For wireless sensors, power management is one of the most crucial bottlenecks of the design. Because of the limitation of battery operation in long-term deployments of sensors, self-powered systems have become increasingly attractive [2]. Solar cells and Micro Electro-Mechanical Systems (MEMS) have widely been used in many self-powered systems since their fabrication methods can be combined with IC technology. Because chip-sized energy scavenging devices can provide limited power, sensory circuitry should be designed for ultra-low power budgets. Table I shows the recent publication results for chip-sized energy scavenger systems.

As the interface between the sensing environment and the digital processing modules, the analog-to-digital converters are crucial to the energy-scavenging sensory system's performance. A recent publication [3] presented us with a good example of an ultra-low energy ADC with moderate speed. This paper focuses on an ultra-low power and higher rate ADC and its application. One example application is the ADCs in scavenging untethered sensor, the *PixEye*, represented in Figure 1. The PixEye is a millimeter-sized energy-scavenging sensor used to monitor a CRT computer or TV screen of homeland security targets. It employs a single high-dynamic range photodiode to detect the electron beam signal of a CRT screen. A high-speed and low-power ADC converts the signal into digital pulses and then the transmitter sends it with ultra-wide-band (UWB) pulse communication. Suppose the target screen has a 640×480 pixels, up to 10fps, and the photodiode scans one frame every second, the analog-to-digital converter is required to operate at least at 300kS/s. We designed an analog-to-digital converter, which consumes 3μW power and operates at 409kS/s. A 1×1mm^2 solar cell [2] can deliver a power of 100μW. Using the proposed SOS ADC, 97% of the power budget could be used for communication.

TABLE I
List of Energy-Scavenger Performance

Technique	Power	Voltage
Solar Cell [2]	100mW/cm^2 (sunshine)	0.6-3V
Piezoelectric converter [4]	70μW/cm^3	3-10V
Thermoelectric converter [5]	60μW/cm^2	3V with with 5C° difference

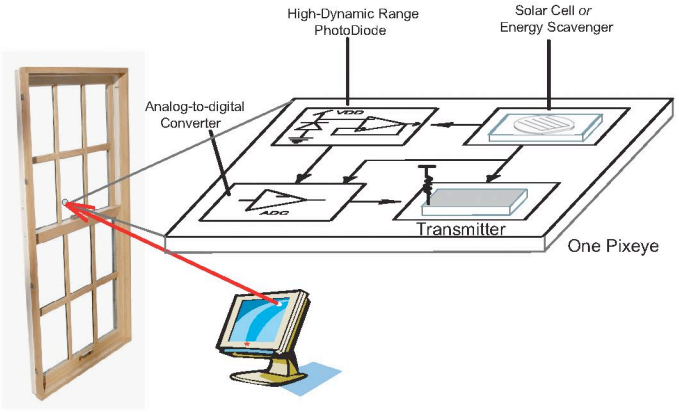

Fig. 1. "PixEye" die with a high-range photodie, ultra-low-power, high speed ADC and ultra-wide band transmitter.

The ultra-low power analog-to-digital converter reported in this paper innovates in two points. First, a switched capacitor with cascoded inverter is chosen as a high-speed and ultra-low power comparator. Second, the ADC is using a split capacitor array and fabricated in the Silicon-on-Sapphire (SOS) CMOS process. The attenuation capacitor is floating. In bulk CMOS process, the floating plate couples with the substrate forming parasitic capacitance, which corrupts the ADC performance at high speed. The SOS process is immune to this problem because its substrate is an insulator.

II. ADC System Overview

The ADC uses a conventional successive approximation architecture, but innovates by using both a split capacitor array and a switched capacitor comparator.

A. Conversion Algorithm

A successive approximation architecture is chosen because the simplicity of the design allows for low power consumption, while keeping the high sampling speed. Figure 2 shows the successive approximation architecture with a split capacitor array. A linearly scaled voltage is delivered by setting and resetting the successive approximation registers. A binary search through all possible quantization levels is performed before converging to a final digital answer, which is stored in the successive approximation registers.

The voltage of the upper plates is expressed in Equation (1)

$$V_{ca} = V_{in} + \sum \frac{D_k \times 2^{N-k}}{2^N} V_{cmp} \qquad (1)$$

where D_k is the digital output of the successive approximation registers, N is the total number of bits in the ADC (8 in this case).

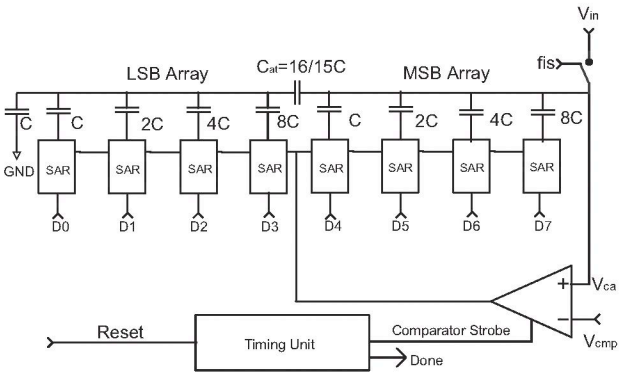

Fig. 2. Split capacitor array and successive approximation register (SAR).

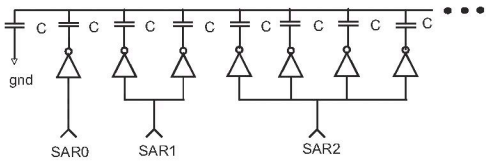

Fig. 3. Capacitor array driven by minimum size inverters. Three LSB capacitors are displayed. Each capacitor is of unit capacitance.

B. Capacitor Array

The main component in a successive approximation ADC is a capacitor array DAC, which provides a linearly scaled voltage. Figure 2 shows the capacitor array DAC used in our implementation. In order to reduce the total capacitance and chip area, a split capacitor array is chosen. For a 8-bit ADC, the split capacitor array uses 32 unit capacitance instead of 256 used in a full array. As shown in Figure 2, two parallel arrays of binary weighted capacitors are separated by an attenuation (scaling) capacitor C_{at}. [6] The attenuation capacitor is floating because it is not directly charged or discharged by a voltage source. In bulk CMOS process, the floating plate couples with the substrate forming parasitic capacitance, which corrupts the ADC performance at high speed. The SOS process is immune to this problem because its substrate is an insulator.

The total capacitances for the LSB and MSB array are $16C_{unit}$ and $15C_{unit}$, where C_{unit} is equal to 215fF. The attenuation capacitance is computed with Equation (2).

$$C_{at} = \frac{\sum C_{LSB\ array}}{\sum C_{MSB\ array}} \times C_{unit} = \frac{16}{15} \times C_{unit} \qquad (2)$$

In order to reduce the parasitic capacitance from the wires connecting the capacitor arrays, a minimum-sized inverter is introduced to drive each unit capacitor as shown in Figure 3.

C. Comparator

To minimize the power consumption in the comparator, which is the most power hungry component in ADC, we used a switched capacitor comparator based on a cascoded inverter [7]. A cascoded inverter implementation offers two advantages over the basic common-source amplifier: first, a higher gain due to the larger output resistance; second, a higher operational speed due to the reduced Miller capacitance. The schematic of the comparator is shown in Figure 4. Two pMOS and two nMOS are connected in series. M4 is separated by a capacitor with the input, which is switching between the input signal V_{ca} and the reference voltage V_{cmp}. Three transistors, M_1, M_2 and M_3, operate at the subthreshold region for the higher device gain. The biases for them are 0.6V, V_{ddA} and 0V respectively. Two intrinsic transistors [8] were used for M_2 and M_3, to eliminate the need of additional biases for the cascoded inverter. A buffered register is laid after the comparator in order to store the comparing result and drive the next stage. A correlated double sampling (CDS) technique [9] was used in the comparator to eliminate the correlated noise, such as the mismatch in devices. Complementary CMOS switches with dummy switches are used to reduced the effects of charge injections [10]. A comparison is obtained after two phases:

1) Reset Phase: Switches S_1 and S_2 are closed, while switch S_3 is opened. The reference voltage V_{cmp} is stored on

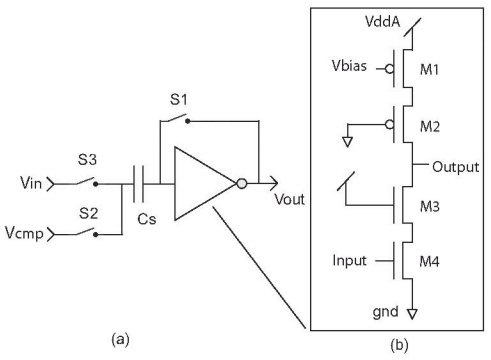

Fig. 4. Cascoded inverter as a ultra-low power comparator.

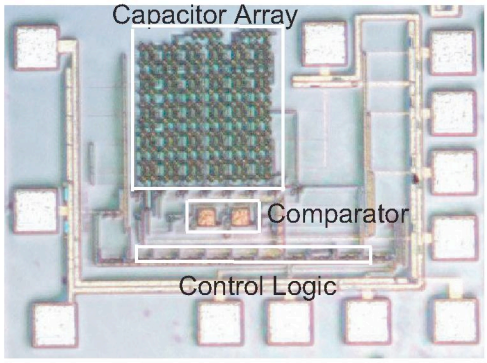

Fig. 5. Anottated 8-bit ADC die micrograph.

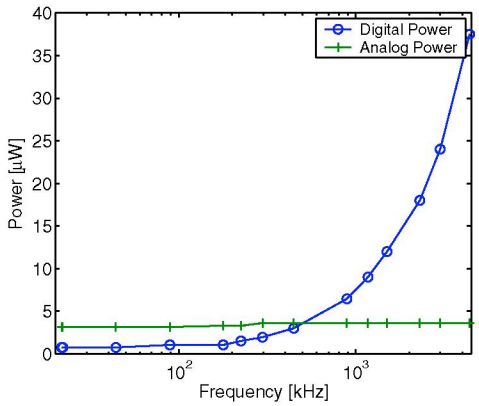

Fig. 6. Power consumption versus operational clock frequency (Vdd=1.5V).

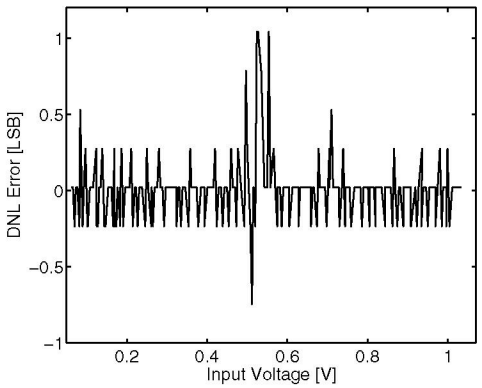

Fig. 7. Differential non-linearity versus input voltage at 2kS/s

the capacitor C_s, together with any correlated noise. The inverter is also initialized to its logic threshold.

2) Compare Phase: Switch S_3 is closed, while switch S_1 and S_2 are opened. The input V_{ca} is connected and the comparator changes state when this voltage exceeds V_{cmp}.

Simulations indicate that the comparator consumes as low as 200nW while operating at 10MHz. The gain of the comparator drops 1% with 10 degree increase in Kelvin temperature.

III. Experiment Results

The analog-to-digital converter was fabricated with a commercially available 0.5μm Silicon-on-Sapphire process (Vtn = 0.7V, Vtp = -0.8V) offered by Peregrine [8]. The process features three metal layers, including a metal-thick layer for high quality passive capacitors, as well as a single polysilicon layer. The die size is 620$\times$780μm and 770$\times$1120μm with pads. The die micrograph is shown in Figure 5. The converter operates at 1.5V power supply. The reference voltage was set to 1V throughout the testing.

Figure 6 shows the analog and digital power consumption at different frequencies. The power for analog components provides the current for charging and discharging of the capacitors and operating of the comparator. The power consumption is 3μW. The digital power supplies the control logic and the output buffers and increases linearly with the frequency. At higher clock rate, more power is consumed to drive the 50pF capacitive load of testing equipment. The digital power becomes negligible when the ADC is used in a system-on-a-chip.

The analog-to-digital converter operates from 22kHz to 4.5MHz clock rate, which corresponds to a sampling frequency from 2kS/s to 409kS/s. Figure 8 and Figure 7 show the Integral Non Linearity (INL) and Differential Non Linearity (DNL). This data is collected at a clock frequency of 22kHz, corresponding to a sampling frequency of 2kS/s. The analog-to-digital converter performed with an average of 0.12 LSB Differential Non-Linearity (DNL) and an average of 0.38 LSB Integral Non-Linearity (INL). The maximum INL is 0.825 LSB. Notice an increase of the DNL and INL in the middle of the input range, due to the difference between the required attenuation capacitance (C_{at}) in Equation 2 and the actual capacitance available in the SOS layout. The ideal ADC requires 229.3fF, while the closest value available in layout is 228.4fF.

The Effective Number of Bits (ENOB) was 7.62 bits for a operational frequency of up to 3.4MHz (309kS/s), while decreased to 7 bits at a clock frequency of 4.5 MHz (409kS/s). Figure 9 represents the ENOB as the function of the operational clock frequency. The drop in precision is due to a problem with the on-chip non-overlapping clocks. This problem will be corrected in future iterations. The clocks were provided off-chip and they became distorted at the high rate due to the RC delay. Simulations indicate that the SOS ADC is able to run at more than 1MS/s without performance degeneration. The total Harmonic Distortion (THD) was measured at a 100kS/s. A plot of the FFT spectrum for a sampled 1kHz sine waveform is given in Figure 10. The Total Harmonic Distortion (THD) was measured to be -52dB. The Spurious Free Dynamic Range (SFDR) for the same input was measured to be 50dB. The input range was measured as 0.97V using a 1.5V supply with reference voltage V_{ref} set to 1V.

IV. Summary

We presented an 8-bit, 3μW analog-to-digital converter, which samples at the speed of 409kS/s. The performance of the ADC is summarized in the Table II. The chip was fabricated

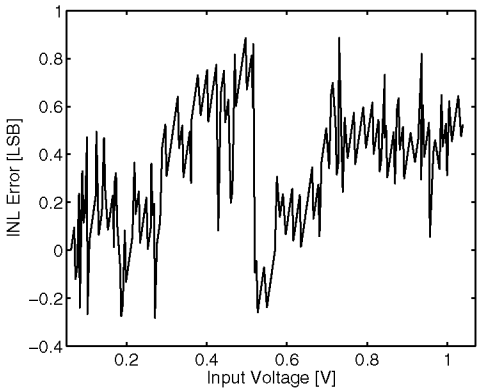

Fig. 8. Integral non-linearity versus input voltage at 2kS/s

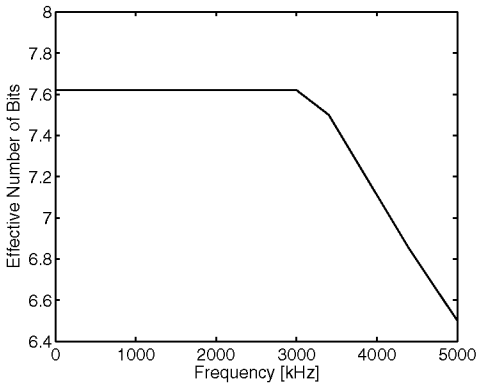

Fig. 9. Effective number of bits for V_{in}=720mV

on a commercially available Silicon-on-Sapphire process. The ADC showed the precision, accuracy and effective number of bits equal to 8. The low-power circuit design trends raise the possibility of using ambient energy to power sensory systems. Because chip-sized energy-scavenging devices can deliver limited power, the sensory circuitry should be designed for ultra-low power budgets.

V. Acknowledgements

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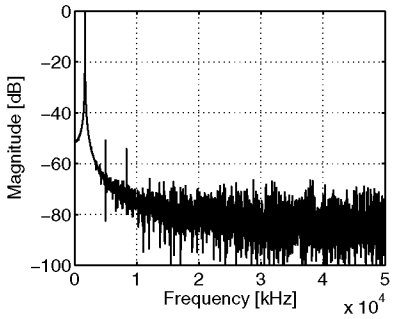

Fig. 10. Measured FFT spectrum for a 1.67kHz sine waveform sampled at 100kS/s

TABLE II
Summary of ADC Performance

Power Supply	1.5V
Analog Power	3μW
Digital Power	4.3μW@100kS/s with 50pF loads
Process Technology	0.5 μm Silicon-on-Sapphire
Operational Clock Frequency	22kHz $\sim$ 4.5MHz
Sampling Rate	2kS/s $\sim$ 409kS/s
Resolution	8 bits
Active Area	615x782μm^2
Input Range	65mV $\sim$ 1.035V
Unit Capacitance	215fF
Input Capacitance	3.44pF
DNL	0.12 LSB
INL	0.38 LSB
THD	-52dB
SFDR@2kS/s	50dB
SNR@2kS/s	47dB
ENOB@2kS/s	7.62LSB

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