A Monolithic Isolation Amplifier in Silicon-on-Insulator CMOS

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***Abstract*— We designed and fabricated a 4-channels digital isolation amplifier in a $0.5\mu m$ Silicon-on-Sapphire (SOS) technology, by taking advantage of the isolation properties of the SOS substrate. The individual isolation channels can operate in the excess of $100Mbps$ using a differential transmission scheme. The device can tolerate ground bounces of $1V/us$ and isolate more than $800V$. The device uses an isolated charge pump circuit to power the input circuit from the isolated output side and thus can be used as sensing device. Applications are in the industrial, medical and military: high reliability systems, harsh industrial environments, transportation, medical and life critical systems.**

I. Introduction

A digital isolation buffer is an electrical circuit that communicates an input digital voltage from one region to an output digital voltage in a second region where the ground node is galvanically isolated from the first one. Isolation of circuit communication is desirable in locations with ground loops, or where it is not possible to ensure a common ground signal between output and input nodes. Typical applications are in the industrial field and in the presence of harsh industrial environments, where ground currents are present. Also to prevent personnel or equipment damage. In the medical field, where it is necessary or desirable to isolate human subject from data acquisition systems and life critical systems. Applications are also in the military field, for high reliability systems and transportation.

An integrated version of an isolation circuit is conventionally an assembly of two separate dies packaged together, as in the case of optocouplers [1] and bulk capacitive coupling [2]. The cost of the isolator can be high because of the expenses and the difficulties in packaging two dies with the desired isolation properties. In addition the power consumption is higher due to the parasitic capacitances and inductances of multi-chip modules. Conventional bulk processes cannot provide isolation of two portions of a die because of the presence of a common galvanic substrate. Capacitive coupling has been employed in bulk CMOS multi-chip modules to transfer data signals between multiple dies [3], [4], [5]. On-chip isolation using a Silicon-On-Insulator (SOI) substrate has been demonstrated for modem lines and for data only [6].

By taking advantage of the isolation properties of the Silicon-on-Sapphire (SOS) substrate [7], we designed and fabricated a monolithic single chip isolation device capable of $100V$ continuous isolation from input to output grounds. The device is composed by a transmitter or input circuit and a receiving or output circuit. Isolation is provided by capacitive coupling at baseband, avoiding modulation of the input signal or any galvanic connection. In this article we report on the design, modeling and test results of the SOS digital isolation device.

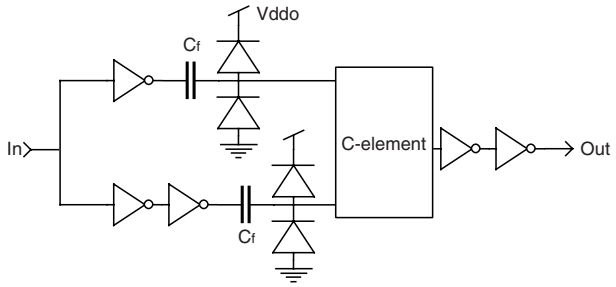

Fig. 1. Capacitive isolator circuit: the isolation cell *isoCap2sc*.

II. System Overview

A schematic of one isolation channel *isoCap2sc* is given in Figure 1. Specification were for a data rate of $100Mbps$, military temperature range, ground bouncing rejection of $1V/us$, input signal rise/fall time between $10ns$ and $1.5ns$. The required isolation was at least $100V$ in continuous mode.

The device is designed to withstand ground bouncing of more than $1V/\mu s$ by using asynchronous circuitry to reject spurious transitions. This property is obtained by employing a differential scheme at the input, before the capacitive isolation interface of Figure 1. A schematic of the asynchronous C-element circuit *celiso* is given in Figure 2. The asynchronous C-element circuit *celiso* is a static logic cell that switches its output only when it detects a valid differential transition. A valid transition is a transition where one output has a logic level *1* and the other level *0*. If only one of its inputs switches because of a ground bounce, the inputs will both be *0*s or both *1*s, and the output will not commute.The *celiso* function can be expressed in Concurrent Hardware Process (CHP) production rules by equation 1.

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$$[\neg a \wedge b] \rightarrow out \uparrow, [a \wedge \neg b] \rightarrow out \downarrow \quad (1)$$

The input signal is buffered by digital inverters at the transmitter/input side of *isoCap2sc* (see Figure 1) and communicated differentially to the receiver/output circuit using capacitive coupling. The coupling capacitors C have a capacitance of $150fF$ and have been designed using metal-1 and metal-3 plates. The silicon area used by the capacitor is 175 x $60\mu m^2$. The differential signal is buffered with inverters and recombined using the asynchronous circuit to reproduce a final digital output signal (*Out* in Figure 1). At the receiver side, protection diodes (see Figure 1 located at the receiver input node enforce that the voltage at the floating nodes always drifts to one of the supplies, to prevent damage.

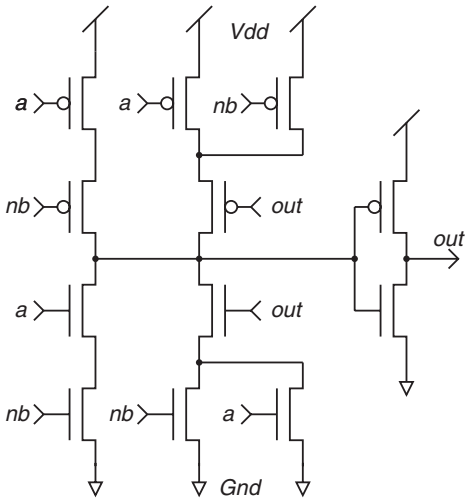

Fig. 2. Asynchronous c-element cell for the capacitive isolator: *celiso*.

The unit can be powered from input and output side or, alternatively, from the output side only. A charge pump operating on the output power supply is capable of powering the input differential circuitry [8]. A schematic of the charge pump circuit is given in Figure 3. The pump generates the required $3.3V$ input supply with enough current ($1.5mA$) to drive the inputs at $100MHz$. Protection diodes ensure that an unbound received voltage does not damage the input circuits. The charge pump has separate external supply connections, so it can be disabled to save power when the input side is externally powered. The charge pump of Figure 3 is based on the Dickson [8] charge pump design and it is composed by four stages. It uses a eleven stages ring oscillator at the output side to produce a $350MHz$ digital clock signal that controls the pump (represented by an oscillator symbol in Figure 3). The output of the oscillator is buffered to drive the isolation capacitances. The Dickson charge pump operates by pumping charge along the diode chain as the capacitors are successively charged and discharged during each clock cycle. The capacitor size is $450fF$ and they consist of three parallel units of the isolation capacitors used in any the four channels *isoCap2sc*.

The isolation input pads are protected against surges by using protection clamp diodes connected to their power supply. Outputs are buffered with digital inverters to be able to drive a $50pF$ capacitive load. The final prototype of the capacitive isolation buffer named *isoCap* is organized as an array of 4 independent isolation channels *isoCap2sc* in one single chip. All channels share the same input and output power supplies.

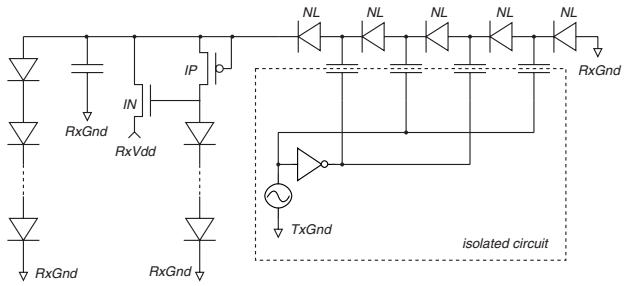

Fig. 3. Charge pump circuit.

III. Capacitive Coupled Isolation Circuit Model

To ensure proper operation of the capacitive coupled isolation circuit, the isolation capacitance must be much higher than the receiver input capacitance. This is to avoid capacitive division of the transmitted voltage.

Referring to Figure 4, C is the isolation capacitor, C_a and C_b are the parasitic capacitances at the two terminals of the isolation capacitor.

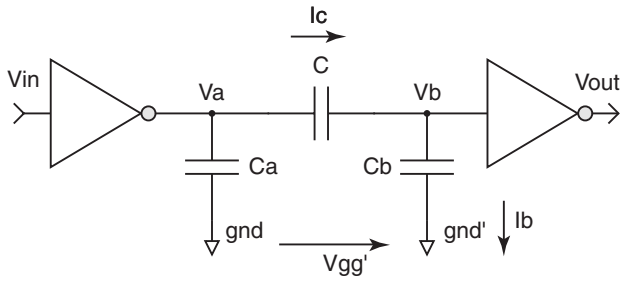

Fig. 4. Model of operation of a capacitively coupled isolation circuit.

Consider now an AC model of the capacitive coupling. V_{in} is a digital signal whose value is always between V_{dd} and 0 volts. Equivalently V_a, is the inverted voltage of V_{in}, and its is always between 0 and V_{dd} volts. The voltage V_b can be calculated by using equation 2.

$$V_b = V_a \frac{C}{C + C_b} \quad (2)$$

As can be seen from the capacitive divider equation 2, for proper operation the capacitance C must be much larger than the parasitic C_b. In contrary case the transmitted signal amplitude is going to be smaller than V_{dd} and errors occur.

Let us consider the charge at nodes V_b and across the isolation capacitance C: $Q_b = C_b V_b$ and $Q_c = C(V_a - V_b)$.

The maximum charge at V_b is C_bV_{dd} and the minimum is $0V$. The maximum charge across C is $C(V_{dd}+2V_{th})$ and the minimum is $0V$. This assumes that the node V_b is protected towards the power supplies by two diodes of threshold V_{th}.

To assess whether the capacitive link is functional, we need to see if a swing of V_a can change the state of V_b (charge it by $\pm V_{dd}$). As an example, consider the case when $V_b = -V_{th}$ and V_a switching from $0V$ to V_{dd}. We obtain that the initial charge $Q_{bi} = -C_bV_{th}$ and the initial charge across C is: $Q_{ci} = CV_{th}$. The final value of the charge across the isolation capacitance is therefore $Q_{cf} = C(V_{dd} + V_{th})$. Therefore the final charge at node V_b is $Q_{bf} = -C_bV_{th} + C(V_{dd} + V_{th})$. If we chose $C \gg C_b$ then the voltage $V_b \geq V_{dd}$, limited by the protection diodes. Thus operation requires that $C \gg C_b$.

A problem of capacitive isolation is that input voltage swings have to be detected while ground bounce swings have to be rejected. In fact only the former is the desired signal, while the latter is a noise signal. Let us consider the currents across the isolation capacitor C. The current i_c is expressed by equation 3.

$$i_c = C\frac{dV_a}{dt} - C\frac{dV_b}{dt} \tag{3}$$

By examining the second term on the right hand side of equation 3 we can express it as in equation 4.

$$\frac{dV_b}{dt} = f(\frac{dV_{gg'}}{dt}, \frac{dV_a}{dt}) \tag{4}$$

The second variable on the right hand side of equation 3 is governed by the input voltage V_{in}. The first variable is governed by the ground bounce (voltage $V_{gg'}$) and it is to be rejected. V_b can be influenced both by a change in V_a and $V_{gg'}$. Using superimposition of effects we can write equation 5.

$$i_b = C_b\frac{dV_{gb}}{dt} - C_b\frac{dV_{gg'}}{dt} \tag{5}$$

With V_{gb} being the voltage between node b and the input ground ($iGnd$). The first term on the right hand side of equation 5 is due to V_a or the input signal. The second term is the interference or noise due to ground bounce. We conclude that, for correct device operation, equation 6 has to be satisfied.

$$\frac{dV_a}{dt} \gg \frac{dV_{gg'}}{dt} \tag{6}$$

This imposes a constraint on the minimum signal slew rate. If the signal slew rate is much higher than the ground slew rate (equation 6) then the ground bounces can be attenuated using a high-pass filter at the receiving node. This can be done by having a leaky node at the receiver node.

As an example consider the case of $(dV_a/dt)_{min}$. This value must be bigger than $(dV_{gg'}/dt)_{max}$. With a power supply of $3V$ and $10Mbps$ communication, the value of $(dV_a/dt)_{min}$ is approximately 1.5 x 10^7. While the expected grounds slew rate $(dV_{gg'}/dt)_{max}$ is about 1 x 10^6. These values satisfy equation 6.

IV. Results and Measurements

We successfully simulated the isolation buffer at the design corners for temperature, and transistors characteristics. We simulated at -60C, $+130$C for typical, fast and slow transistors. We repeated the measurements at $10Mbps$ and $100Mbps$. We tested the circuit in two configurations: powered from input and output, and output-only. The circuit performed correctly in all settings. We also tested the circuits with a power supply $\pm 10\%$ of the nominal value at $10Mbps$. In both cases the circuit was operational as in the nominal $3.3V$ supply setting. All simulations have been conducted with all four inputs tied together, which corresponds to a worse case scenario for the charge pump loading.

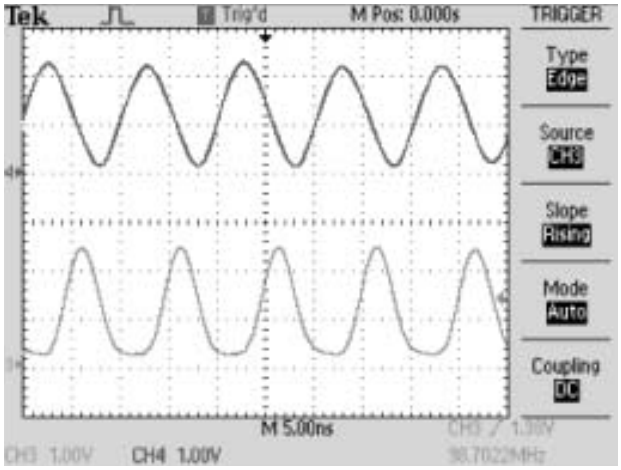

Fig. 5. Isolation channel input (top trace) and output (bottom) operating at $100MHz$.

The measured supply current was $6mA$ (both transmitter and receiver), measured at $30MHz$, with the charge pump circuit turned off and $3.3V$ power supply. No cross talk from any channel to any other channel was observed. All these measurement were conducted with the isolation chip driving $2ft$ of coaxial cable and a $25pF$ load (oscilloscope load). Figure 5 shows the output of one isolation channel (bottom trace) when driven with a $100MHz$ input (top trace).

When the charge pump was turned on, the static current consumption was $2.5mA$ with an output supply of $3.3V$. The received power supply output of the charge pump was $rVdd = 2.68V$ (measured with open circuit, unloaded). We measured the current drawn from the power supply of $3.3V$ for various speed of operation, with the charge pump off and operating one single channel. At $1Mhz$ input square wave, the current was $0.31mA$, at $10MHz$ was $2.7mA$, at $100MHz$ was $8mA$. Driving all four channels in parallel with the same $30MHz$ square input wave drew $14mA$. Setting the output power supply $oVdd$ to $1.5V$, the circuit worked perfectly with an input square wave of $30MHz$, and absorbing $3mA$ from the power supply, with the charge pump circuit turned on.

Operation while providing isolation was verified experimentally, with the circuit operating with an input square wave of

$30MHz$, $oVdd$ = 3.3 and $V_{oGnd-iGnd}$ = $25V$. The isolation

Figure 6 illustrates the isolation property of two SOS metal layers. Specifications for the device described in this chapter were a ground to ground isolation of up to $100V$. We measured the isolation of the amplifier up to $110V$ with a Keithley unit 236 and measured no significant current (Figure 6), as evidence that the isolation in the SOS die is holding to the specifications. The actual *measured* breakdown of the device occurred in the proximity of $820V$ between the grounds of input and output circuits. This isolation is guaranteed by the $3.6\mu m$ of separation from the metal-1 and metal-3 coils composing the interface between input and output. The breakdown measurements were conducted using an electrophoresis equipment FisherBiotech FB400.

A picture of the fabricates SOS isolator amplifier is give in Figure 7. The die has 16 bonding pads: the bottom eight are (left to right) two input supplies (supply for the input isolation circuit and output of the charge pump), four data inputs and two grounds (circuit and charge pump output ground), the top eight are (left to right) the two output supplies (output circuit supply and charge pump input supply), four data outputs and two grounds (output circuit ground and charge pump input ground).

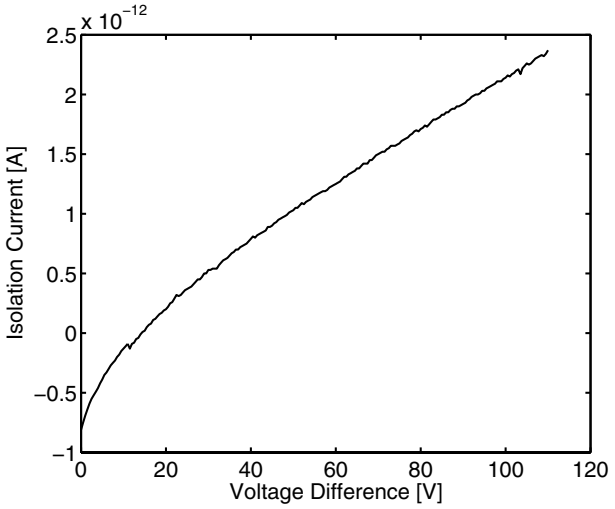

Fig. 6. Isolation performance between metal-1 and metal-3 in the SOS process.

V. Summary

We designed and fabricated a 4-channels digital isolation amplifier in a $0.5\mu m$ SOS technology. We took advantage of the isolation properties of the SOS substrate. The individual isolation channels operate in the excess of $100Mbps$ using a differential transmission scheme. We have shown the ability of the device to tolerate ground bounces of $1V/us$ and isolate more than $800V$. The device uses an isolated charge pump circuit to power the input circuit from the isolated output side and thus can be used as sensing device.

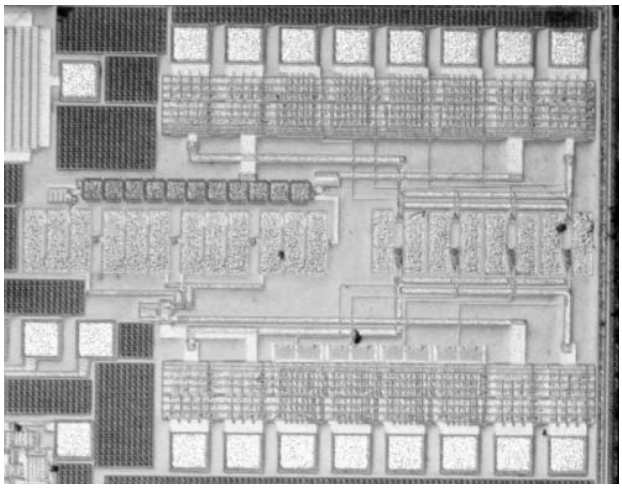

Fig. 7. Micrograph of the fabricated SOS isolation amplifier.

VI. Acknowledgements

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