Vertically-Integrated Three-Dimensional SOI Photodetectors

Eugenio Culurciello, Pujitha Weerakoon
Electrical Engineering Department
Yale University
New Haven CT 06520
eugenio.culurciello@yale.edu

***Abstract*— We report on the design and measurement results of three-dimensional (3D) photo-detectors in a 0.18μm silicon-on-insulator technology. The photodiodes respond to light in the range of 1-200,000lux with currents of 2fA to 300pA and can be arranged in a 3D stack. The phototransistors respond to light intensities of 5-200,000lux with currents from 50fA to 2.3μA. We also report spectral data obtained from the photodiode and show that a photodiode stack can be used to extract color information without the use of color filters. The data in this paper is essential to the design of advanced imaging arrays and color sensors in 3D SOI processes.**

I. Introduction

Three-dimensional integrated-circuit technologies promise to offer integrative advantages in the vertical dimension for stacking both homogenous and heterogeneous layers of conventional CMOS dies [1], [2]. These advantages also reflect on circuit design into power-savings due to short interconnects, higher circuit bandwidth resulting from reduced wire capacitances, and increased computation density due to multiple active silicon layers [3], [4].

In the very recent years the research on 3D integration culminated in the availability of vertical integration from both research centers and companies worldwide. One such example is the MIT Lincoln Laboratories three-dimensional process. A cross-section of the Lincoln Labs three-dimensional die stack is given in Figure 1. Two thinned SOI dies (tiers 2 and 3) are stacked upside-down on top of another die (tier-1). Vertical interconnects are obtained by means of a low-temperature metallization process. Based on this process, an heterogeneous imaging sensor array has been recently presented [5]. This sensor array featured more than a million vertical connections between two heterogenous dies. The sensor was obtained by wafer-stacking of a 0.35μm silicon-on-insulator (SOI) CMOS on top of 0.35μm bulk CMOS used for the photosensitive elements. The bottom bulk die was thinned to allow back-light illumination to reach the detectors, and mounted on a glass substrate for mechanical stabilization. The main reason for the use of a combination of bulk CMOS and SOI CMOS, was the unavailability of photo-detectors in SOI CMOS.

The purpose of this paper is to present design and measurements obtained from native SOI photo-detectors fabricated in the first available three-dimensional multi-project run offered by MIT Lincoln Laboratories in 2005. The contribution of this paper is to: 1) present photo-detectors obtained with native rules on the 3D SOI process, 2) show a stack of photosensitive SOI devices capable of imaging light in the vertical dimension and in multiple silicon active layers, and 3) to show the possibility of color imaging with stacked photodiodes.

Our device will allow to use the standard SOI layer as photo-detector layer for vertically integrated image sensor arrays. This device eliminates the need of heterogeneous integration of bulk CMOS dies and the need of die-thinning techniques to image light. The photodiode is also the first SOI photosensitive device to have been integrated in a large 3D image sensor array.

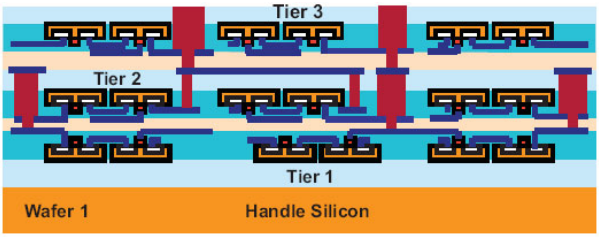

Fig. 1. A cross-section of the MIT Lincoln Laboratories three-dimensional integration of three SOI dies.

II. Photosensitive Devices

The SOI photo-detectors presented in this paper are implemented in a thin SOI silicon layer between buried oxide and deposited interconnect layers of oxides. In the MIT LL process the active silicon layer thickness is 50nm. The three active layers are separated by 7.5μm between tier-3 and tier-2, and 12μm between tier-2 and tier-1 (refer to Figure 1). While we have no control over process parameters as layers thickness and organization, we have designed and optimized the detectors for maximum dynamic-range, taking advantage of the process specifications. We characterized the light-sensitivity of three photo-detector structures in the 3D process: a top-layer photodiode and a phototransistor (implemented in tier-3 of Figure 1), and a 3D photodiode stack (implemented in all tiers).

The photodiodes are obtained abiding N-type and P-type silicon regions and feature a vertical junction. The P and N silicon regions did not receive the highly-doped drain/source implant to maximize the depletion region of the diode. In order

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to maximize the devices dynamic-range, particular care has been taken in the layout topology to avoid possible causes of leakage currents at the diode junction. The layout of the detector is quasi-circular (octagonal), to avoid interfaces between the N and P-type silicon regions and the deposited silicon oxide usually referred to as the local oxidation of silicon (LOCOS). For the same reason, the photodiode junction between N and P regions has been gated with a poly-crystalline silicon layer to avoid having deposited silicon oxide above the diode. The poly layer insures a low-leakage thermally grown oxide layer and thus prevents the interface currents that plagued previous SOI photo-detectors [6], [7]. The polysilicon gate was left electrically floating. Figure 2 (left) shows a layout of the 3D photodiode. The photodiode area is 16 x 16μm^2.

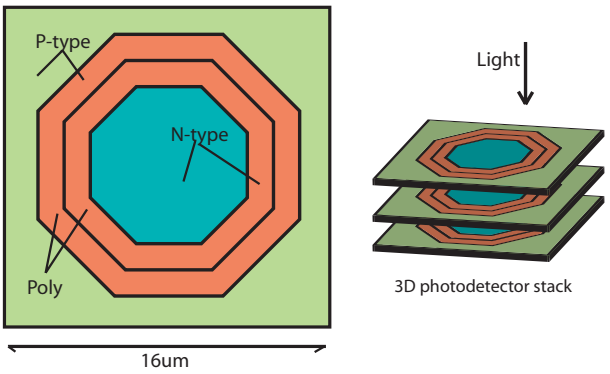

Fig. 2. Layout of the photodiode and phototransistor (left). The three-dimensional photodiode stack (right).

Taking advantage of the multiple active silicon layers, we have also designed a vertical stack of photo-detectors in the 3D process. This device has been obtained by overlapping three photodiodes obtained in each of the available active silicon layers of the 3D fabrication process (Figure 2-right). Each photodiode is identical to the one reported above and in Figure 2 (left).

Finally, we have designed and measured the light-sensitivity of an N-type phototransistor in the 3D process. The phototransistor has the same circular layout and dimensions of the photodiode in Figure 2 (left). The phototransistor gate (polysilicon layer) was left floating (unconnected). Among the other test structures we tested, the P-type phototransistors and all other photo-detectors without the CBN/CBP process layers did not provide any photo-sensitivity. The CBN/CBP layers are the transistor channel implants in the 3D process. The CBN/CBP channel doping is of $5 \cdot 10^{17}$. As mentioned, this layer was not used in the layout of the photodiodes.

III. Results and Measurements

Photo-induced currents were measured and collected using a Keithley 236 picoammeter unit. We used a conventional halogen light as a source, since the final application is the use of this sensor for indoor lighting (white spectrum). The light meter was a commercial photographic unit with a range of 1-20,000lux. We used neutral density filters to measure high light intensities. Also, 1.5V is the nominal supply voltage rating of the 3D process.

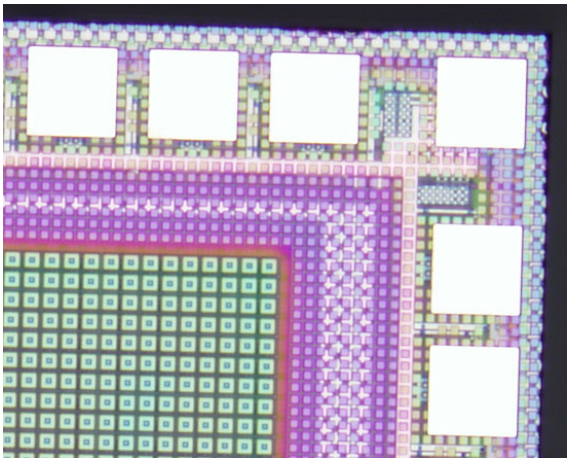

Fig. 3. Micrograph of the fabricated array of 3D photodiodes (visible on the lower left corner). The photodiode area is 16 x 16 μm^2. Pads are 75 x 75 μm^2

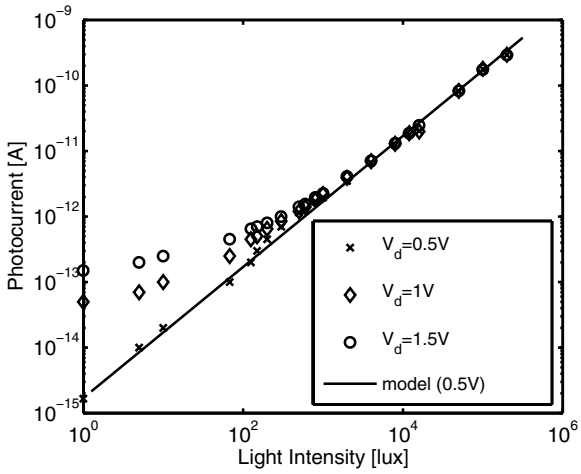

Fig. 4. Responsivity of the top-layer photodiode.

A. Photodiodes Results

Figure 4 shows the data collected from the phototransistor placed in the topmost layer of the 3D process (tier-3 in Figure 1). We have biased the phototransistor with three voltage settings: 0.5, 1 and 1.5V. There is no significant difference between the bias voltages of the photodiode and its influence on the photosensitivity at light intensity higher than 200lux. The different biasing conditions manifest themselves on the photodiode responsivity in the form of an higher dark current (and deviation from the linear model). At higher bias voltages, the electric-field in the depletion region of the diode is sweeping a larger number of thermally-generated carriers to the diode terminals [8]. We computed a model of the diode photocurrent (I_ph) as in equation 1, where I_{in} is the incident

illumination in lux. The model corresponds to a Responsivity of 0.0016 at 535nm.

$$I_{ph} = I_{in} \cdot 1.7 \cdot 10^{-15} \tag{1}$$

We measured photocurrents below 50fA by means of integration in an active pixel sensor configuration. By integrating on a 20fF capacitor for 10s we measured a dark current of 4fA for a 0.5V reset bias applied to the photodiode.

We also measured the external Quantum Efficiency (QE) for the photodiode of 0.0037 at a 0.5V bias. We calculated the QE as the ratio between the photodiode current and the incident optical power at the detector (in Watts) at 535nm. The low QE is due to the shallow thickness of the SOI silicon layer (50nm) and the vertical junction with small depletion region (2μm from preliminary calculations and abrupt junction [8]), both contributing to a small active photosensitive region.

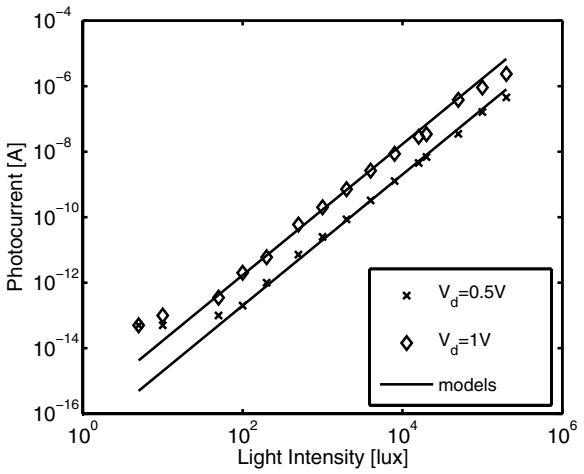

Fig. 5. Responsivity of the MOS top-layer phototransistor.

B. Phototransistor Results

In Figure 5 we report on the responsivity of the 3D phototransistor implemented in the the topmost silicon layer (tier-3). We computed the photocurrent models for biases of 0.5V and 1V as reported in equation 2 and 3 respectively (I_{in} is the incident illumination in lux).

$$I_{ph}(0.5V) = I_{in}^2 \cdot 1.7 \cdot 10^{-16} \tag{2}$$

$$I_{ph}(1V) = I_{in}^2 \cdot 2 \cdot 10^{-17} \tag{3}$$

In this MOS structure the photocurrent is proportional to the square of the incident light power. This power law is due to two combined effect: (1) the light-induced generation of carriers in the device body, and (2) the resilience of majority carriers in the device body [9]. Equation 4 shows the dependance of the body voltage on the incident illumination ($V_{bs} = V_{th} log(I_{in}/I_{in0})$) [9], with I_{in0} beng the dark-generated photocurrent. I_s, k_1, k_2, k_3 are bias and process merged constants, V_{th} is the thermal voltage.

$$I_{ph} = I_s e^{\frac{V_{bs}}{V_{th}}} = k_1 I_{in} e^{V_{th} log(k_2 I_{in})} = k_3 I_{in}^2 \tag{4}$$

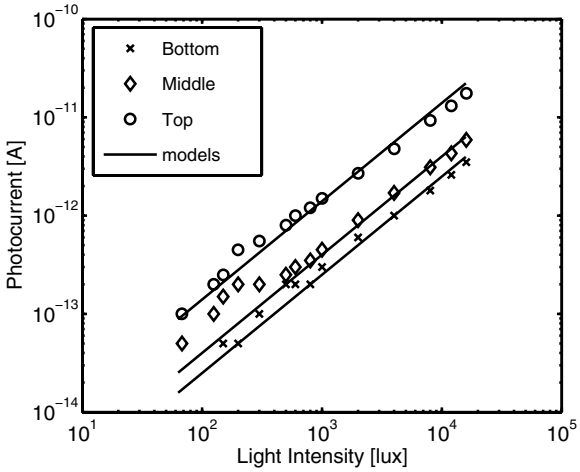

Fig. 6. Responsivity of a 3D stack of photodiodes.

C. Photodiode 3D Stack Results

Figure 6 reports the data collected from the stacked 3D photodiode device. Since light is traveling in the vertical dimension through the three-layer stack (top, middle and bottom), the responsivity of the lower layers is reduced. The photocurrent models for the top, middle and bottom layer (tier-3,-2 and -1 respectively in Figure 1) are given by equations 5-7 (I_{in} is the incident illumination in lux).

$$I_{top} = I_{in} \cdot 1.4 \cdot 10^{-15} \tag{5}$$

$$I_{mid} = I_{in} \cdot 0.4 \cdot 10^{-15} \tag{6}$$

$$I_{bottom} = I_{in} \cdot 0.25 \cdot 10^{-15} \tag{7}$$

The data in Figure 6 has been obtained with a bias voltage of 0.5V. Notice that most of light is collected at the top layer (tier-3), where the highest energy photons are absorbed. This is because the peak collection efficiency is in the lower wavelengths, as will be shown in the next paragraph on spectral response. The inefficiency of the 50nm silicon layer in transducing low-energy intensities (larger wavelenghts) makes the lower two layers have similar responsivities.

D. Photodiodes Spectrum Results

We have measured the spectral response of the topmost layer (tier-3) photodiode. We have used a DLP-based LCD projector as illumination source. We used a Newport 2832-C light power-meter coupled with a 883-UV detector (S/N 2958). This meter allowed is calibrated with respect to input wavelengths. The input light's wavelength has been matched to a standard color chart.

The responsivity of the topmost layer photodiode (tier-3) as a function of frequency is given in Figure 7. Ten wavelength setting have been used in the measurement. The data has been interpolated by splines. Due to the thin silicon active layer, the response is higher at lower wavelengths [7], [9].

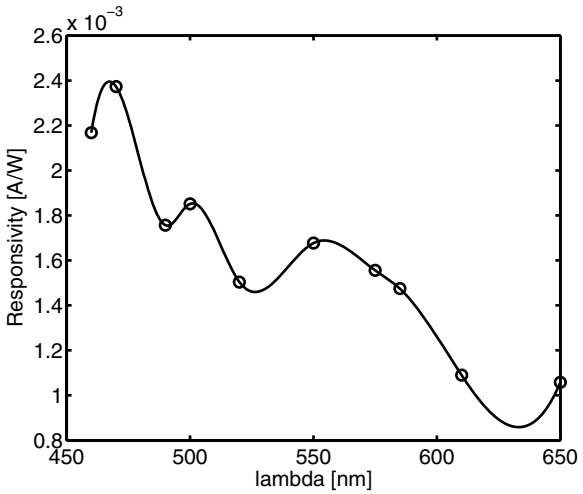

Fig. 7. Responsivity of the top-layer photodiode (tier-3) as a function of input illumination wavelength. Data-points have been interpolated with splines.

We have also investigated the spectral response of the three-layer photodiode stack of Figure 2 (right). We have plotted the responsivity as a function of wavelength of each layer in Figure 8. This figure reports the relative responsivity of each layer's referred to it maximum value. By expressing the relative responsivity we can show the difference between light absorbtion of each photodiode and related them to wavelength. All photodiodes respond maximally in the lower wavelengths (blue), but the topmost photodiode (tier-3) reports a larger signal (Figure 6). Tier-2 photodiode responds in the same way as the lowest tier-1 photodiode to the mid-band wavelengths (yellow-green). On the other hand tier-1 photodiode responds maximally to higher wavelengths (red).

By using a system of three relative responsivity equations one can induce the wavelength of the input signal based on the data of Figure 8. This approach suggest that color vision without filters is possible by using a photodiode stack.

IV. Conclusions

We have designed and measured photo-detector devices in a 3D SOI process. The photodiodes respond to light in the range of 1-200,000lux with currents of 2fA-300pA and can be arranged in a 3D stack. The phototransistors respond to light intensities of 5-200,000lux with currents from 50fA to 2.3μA. We also report spectral data obtained from the photodiode and show that a photodiode stack can be used to extract color information without the use of color filters. The device measurements reported here show that the SOI photo-detectors can be used for the design of high-density imaging arrays in three-dimensional CMOS fabrication processes.

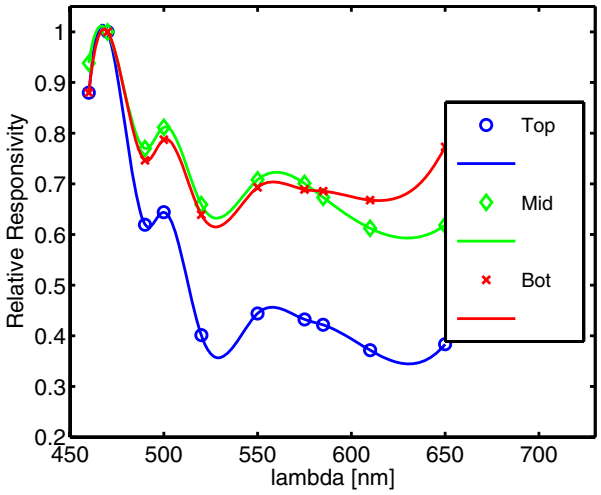

Fig. 8. Relative responsivity of the 3D photodiode stack as a function of input illumination wavelength. Data-points have been interpolated with splines. The relative difference in color response allows to obtain color vision without the use of filters.

V. Acknowledgements

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