Capacitive Coupling of Data and Power for 3D Silicon-on-Insulator VLSI

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***Abstract*— We designed a 3D integrated multi-chip module that uses non-galvanic capacitive coupling to provide bi-directional communication and exchange power supply between two separate dies. A prototype was fabricated on a conventional 0.5μm Silicon-on-Sapphire (SOS) process. We demonstrated that bi-directional communication can be achieved between the two dies at 1Hz-15MHz (100MHz from simulations) while at the same time also transferring power to the receiver die. The non-galvanically connected prototype is an enabling technology for the simplification of 3D VLSI fabrication, wafer stacking and packaging.**

I. Introduction

Three-dimensional VLSI fabrication technologies are extremely attractive for the impact they would provide on the density and integration of sensory arrays, sensory computation and communication systems [1], [2]. As an example, high-density low-power systems for complex visual processing would significantly benefit from 3D VLSI technologies by combining large image sensor arrays with stacked and interconnected processing and communication layers. This would overcome the restriction of standard 2D VLSI processes in terms of type and number of parallel sensing and processing units that can be placed on a single die or connected across chip boundaries. An example of a 3D image sensor is given in Figure 1. The photosensors array is placed at the top of a three die system to obtain high fill factor and resolution. Image processing and communication circuits are placed in the remaining two dies to minimize noise, crosstalk and improve the density of computation. The stacking of the 3 dies achieves high component density without compromising the image quality.

As a proof-of-concept for future more complex 3D systems, we designed a multi-chip module that uses non-galvanic capacitive coupling (flip-chip coupling in Figure 1) to provide both bi-directional communication and also exchange power supply between two separate dies. A prototype was fabricated on a flavor of Silicon-on-Insulator (SOI) process: a 0.5μm Silicon-on-Sapphire (SOS) process. Capacitive coupling has been employed in multi-chip modules to transfer data signals between multiple dies [3], [4], [5]. The coupling capacitors consist of two metal plates residing in separate dies and separated by a dielectric. The dies are aligned to form the coupling capacitance between the metal plates, which are generally

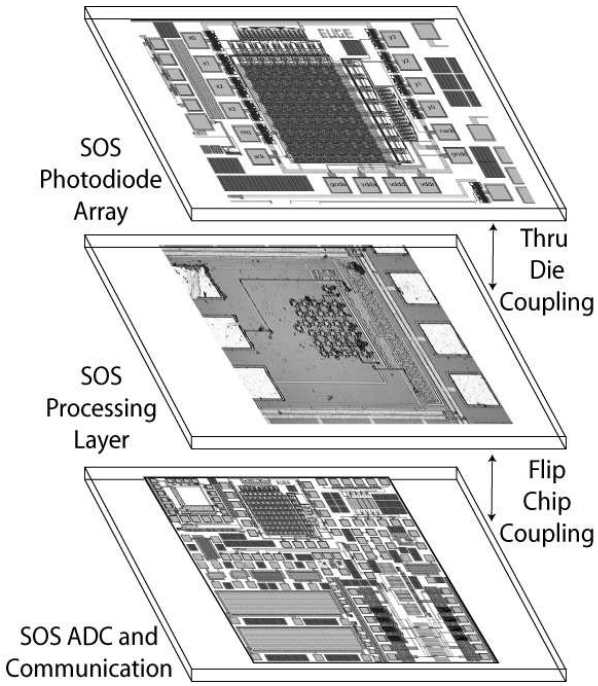

Fig. 1. Capacitive coupling multi chip module for data and power is an enabling technology for 3D VLSI fabrication. Here a image sensor is obtained by stacking three dies.

bonding pads (refer to the bottom two dies in Figure 1). Capacitive coupling has been used successfully only to transfer signals [6], [7], while still requiring electrical connections for both dies in order to provide the required power supply. These physical connection are generally obtained using ball grid array, wire bonds or probes, all imposing mechanical and cost limitations on the number and density of data signal connections to the package.

The main advantage of capacitive coupling is its implicit simplicity. Installation of a die in the package would just require alignment of the die with the package's coupling metal plates and the use of an adhesive. The alignment is unproblematic due to the transparency of the sapphire substrate. This is in contrast to the prevalent bump bond flip-chip techniques, where the yield of the multi-chip module is proportional to

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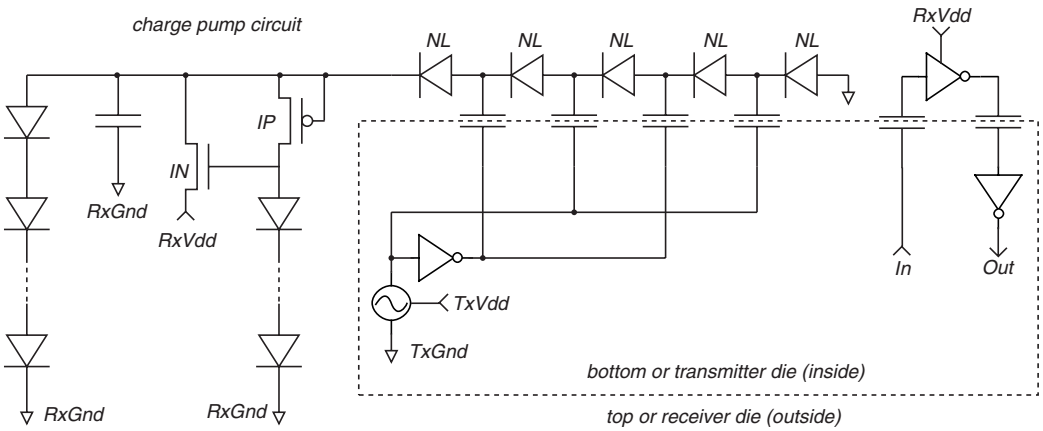

Fig. 2. Schematic caption of the circuit: a charge pump is used to transfer the power using capacitive coupling between two dies. The transmitter is the schematic inside the dashed box and the receiver schematic is outside the box. *In, Out, TxVdd, TxGnd* are external connections for the transmitter circuit.

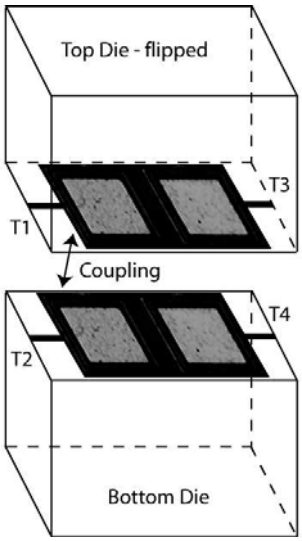

Fig. 3. Coupling is performed through capacitance obtained facing bonding pads (*coupling*) of two separate SOS dies.

the number of bonds that have to be physically connected [8]. This technique can also be used to test dies before assembling them into a multi-chip module [8]. Capacitive coupling can provide high data throughput [6] while minimizing noise and parasitic inductance typical of wire-bonds. The reduction of the undesired inductance of the bonds can provide higher signal bandwidths, while the short interconnections by capacitive coupling reduce antenna effect noise and thermal noise. The combination of short interconnects and reduced parasitic capacitances relaxes the required current from the interconnect driver circuits, thus reducing the communication power consumption [9].

II. System Overview

Our prototype consists of the bottom two SOS dies in Figure 1, one acting as transmitter and one as receiver. The transmitter die (bottom die) is placed and bonded into a common dual-in-line package. The receiver die (middle die) is flipped and aligned on top of the transmitter die, so that the required capacitive connection are formed between the bonding pads metal plates of both dies. Figure 3 shows a mock of the alignments of the pads between the transmitter bottom circuit (pads T2, T4) and the receiver circuit (pads T1, T3). The alignment of the dies was performed manually under a microscope. The precision of the alignment was $15\mu m$, and the dies have been bonded together using a layer of transparent varnish. The number of pads aligning is six, four of which are used by the charge pump and two more for bidirectional communication of two signals. Figure 4 is a micrograph of the fabricated and assembled multi chip module. The bottom (transmitter) die is bonded to a package through bonding wires visible on the left side of the figure. The top (receiver) circuit is on the right side and is flipped so that its bonding pads are facing the bottom circuit's pads. This forms the capacitor for coupling the signal and power across the two dies. The capacitive coupling in air is about $8fF$, with a plates distance of $10\mu m$ (3+$3\mu m$ for the bond to passivation step and an estimated $4\mu m$ for the varnish layer).

Figure 2 is a schematic caption of the integrated circuit, the transmitter circuit is enclosed with a dotted box, while the circuit outside the box is the receiver circuit. The bi-directional communication circuit is composed of an input pad (*in*) at the receiver circuit which is bonded to the package for external stimulation. The input pad is connected capacitively to the receiver circuit which uses an inverter to buffer the digital signal and drive the return coupling capacitance. The signal is the buffered again and output to a pad of the transmitter circuit (*out*). The rest of the transmitter and receiver circuits is the charge pump circuit.

The charge pump is based on the Dickson [10] charge pump design and it is composed by four stages. An eleven stages ring oscillator at the transmitter side produces a 350MHz digital clock signal that controls the pump (represented by an oscillator symbol in Figure 2. The output of the oscillator is buffered to drive the isolation capacitances. The Dickson

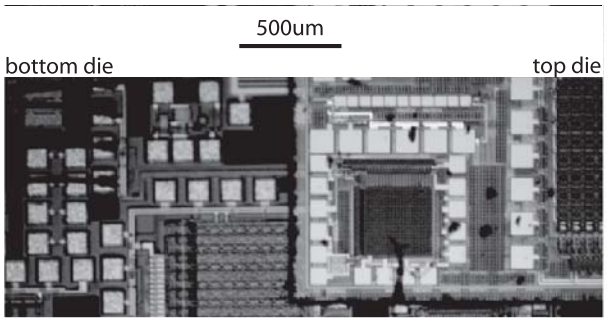

Fig. 4. Micrograph of the assembled multi chip module. The bottom (transmitter) die is bonded to a package through bonding wires visible on the left side of the figure. The top (receiver) circuit is on the right side and is flipped so that its bonding pads are facing the bottom circuit's pads. This forms the capacitor for coupling the signal and power across the two dies.

charge pump operates by pumping charge along the diode chain (four stages therefore five diodes) as the capacitors are successively charged and discharged during each clock cycle. The capacitors are obtained by using coupling between pads, exactly like the signal capacitors.

III. Results

We successfully tested the functionality of the communication link and power transfer at from $1Hz$ to $15MHz$ ($100MHz$ reliably from simulations). Figures 5 and 6 show screen frames of the simulations verifying functionality of the prototype with an input square wave respectively at $15MHz$ and $100MHz$. Figure 7 shows screen shot from the oscilloscope. For each screen the top waveform is the input signal at the transmitter and the bottom waveform is the output signal from the receiver. The top left is at $1V$ supply and $1MHz$ input. The top right is at $3.3V$ and $1KHz$, the bottom left at $1MHz$ and the bottom right at $15MHz$ input frequency. The current drawn was $9mA$ at $3.3V$ supply from $1KHz$ to $15MHz$. The current was $3mA$ at $1V$ supply and $1MHz$ operation.

Notice the close match between simulations and measured data, due to the fidelity of the SOS models above threshold. The square wave output of the $15MHz$ trace in Figure 7 appears corrupted due to impedance mismatch with the prototype's package.

Figure 8 reports the charge pump output voltage (*RxVdd*) as a function of the input power supply (*TxVdd*). The charge pump was tested with three loading conditions: unloaded, and loaded with a $5k\Omega$ and $22k\Omega$ resistors. This figure is useful to calculate the imposable load and the expected received output voltage from the charge pump.

IV. Summary

We designed, fabricated and assembled a multi-chip module that uses non-galvanic capacitive coupling to provide bi-directional communication and exchange power supply between two separate Silicon-on-Insulator dies. The prototype was fabricated on a conventional $0.5\mu m$ Silicon-on-Sapphire

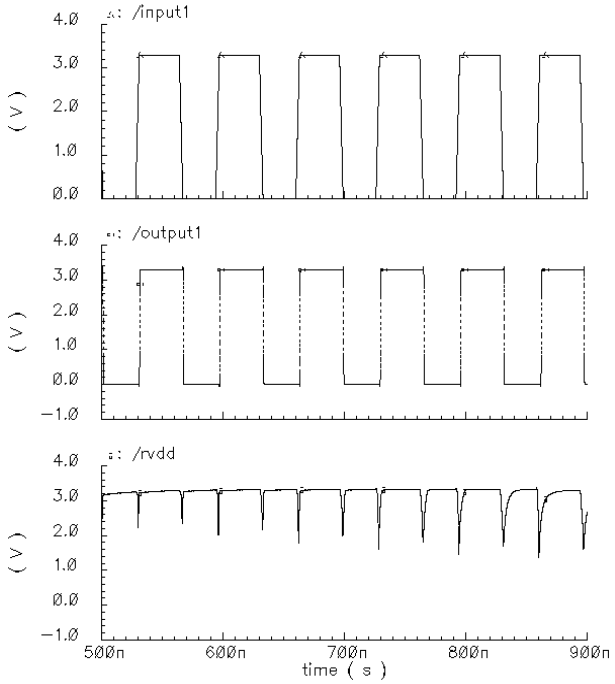

Fig. 5. Simulation verifying functionality of the prototype with an input square wave at 15MHz. The top trace is the input channel and the middle trace is the output signal. The bottom trace is the received voltage (*rxVdd* in Figure 2) output of the charge pump at the receiver side.

(SOS) process. We demonstrated that bi-directional communication can be achieved between the two dies at $1Hz-15MHz$, and up to $100MHz$ from simulations. We also show that capacitive coupling is capable of transferring power to the receiver die, by employing a charge pump. The pump generated voltages in the excess of $2V$ when powered with a supply of $3.3V$ and with a load of $5.3k\Omega$. This proof-of-concept communication multi-chip module is a test-bed for future more complex 3D systems. In particular the middle and top dies of Figure 1 will be connected with a more complex through-die capacitive coupling technique. This technique, based on filled cavities through the die substrate, is currently being developed and we will provide results in the very near future.

V. Acknowledgements

Fabrication was provided by MOSIS. Supported by the Johns Hopkins Applied Physics Laboratory, Laurel MD 20723, NASA Mars Advanced Technology Development grant 1243213, point of contact Steve Jaskulek.

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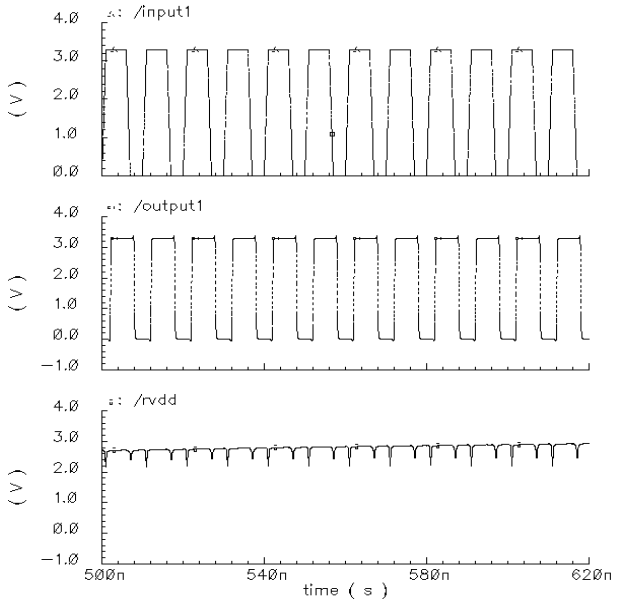

Fig. 6. Simulation verifying functionality of the prototype with an input square wave at $100MHz$. The top trace is the input and the middle trace is the output signal. The bottom trace is the received voltage (*rxVdd* in Figure 2) output of the charge pump at the receiver side.

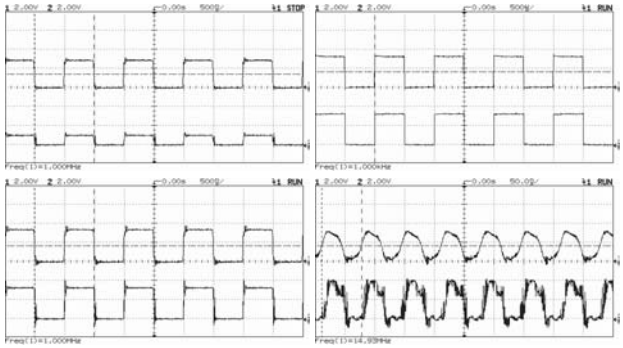

Fig. 7. Oscilloscope traces verifying functionality of the prototype. The top left trace is obtained with $1V$ power supply and $1MHz$ input square wave. The top right with $3.3V$ and $1kHz$ input. The bottom left trace with $3.3V$ and $1MHz$ input. The bottom right trace with $3.3V$ and $15MHz$ input.

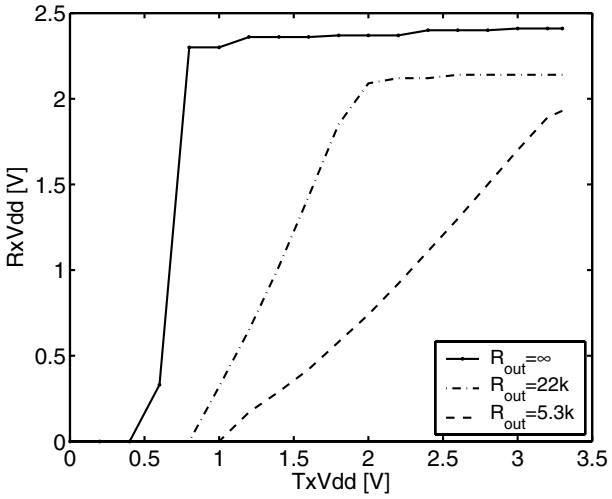

Fig. 8. Output power supply (*RxVdd) from the charge pump) as a function of the input power supply (TxVdd) for three different resistive loads.

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