# A Low-Noise Miniaturized Patch-Clamp Amplifier

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***Abstract*— We present measurement results from a low-noise miniaturized patch-clamp amplifier with electrode compensation. The patch clamp amplifier has less than 4 pA of rms noise at a 10 kHz bandwidth and is capable of accurately measuring nano-Amperes of current. The device measurements shown here show that the integrated amplifier can be used for the design of high-density patch-clamp arrays.**

## I. Introduction

Electrophysiologists use the patch-clamp technique to measure the currents flowing through the membranes of living cells. These measurements depict the behavior of ion channels, the structures responsible for cell membrane conductivity [1]. The cell currents measured by the patch-clamp is used to study the effect of drugs and to study the dynamics of action potentials. The advancement of ion channel research is heavily dependant on the availability of advanced high throughput instrumentation. High throughput patch-clamp systems are now becoming possible with emerging integrated circuit technologies such as the planar patch-clamp technology [2], [3], [4].

Since patch-clamps are used extensively to test drugs, it is highly attractive to pharmaceutical companies to possess high throughput screening instrumentation that would increase the number of recordings made per unit time. Therefore, by introducing a high throughput patch-clamp system, it would be possible to bring safer and better drugs to the consumer market [5]. Other than minimizing the space requirements, an integrated patch-clamp amplifier reduces noise. It also offers better electrical performance by decreasing cabling and other parasitic capacitances that lower the measurement bandwidth. In this paper, we show the feasibility of using a custom designed high performance, low noise integrated patch-clamp amplifier with electrode compensation to build a high-throughput patch-clamp system similar to the one shown in Fig. 1. Parallel simultaneous recording can be performed in a conventional 384 well plate. The resulting data is digitized using analog to digital converters and transmitted to a computer via a high speed USB bus. The protocols for the test sites are implemented using digital to analog converters controlled through the same USB bus.

This paper advances the previous integrated circuit designs [6], [7] by incorporating a capacitive compensation circuit that reduces the stray electrode capacitance and a resistive compensation circuit that reduces the voltage drop across the the recording electrode. This design also differs from previous designs [7] because it uses a continuous-time amplifier with resistive feedback instead of a delta-sigma head-stage with capacitive feedback. This design offers better performance since it allows the electrophysiologist to monitor analog current signal directly. Since no clock is necessary during normal operation of the amplifier, switching noise is kept to a minimum.

Fig. 1. A high-throughput patch-clamp system that uses our integrated patch-clamp amplifiers. This system allows to perform simultaneous patch-clamp recordings on an entire 384 well plate.

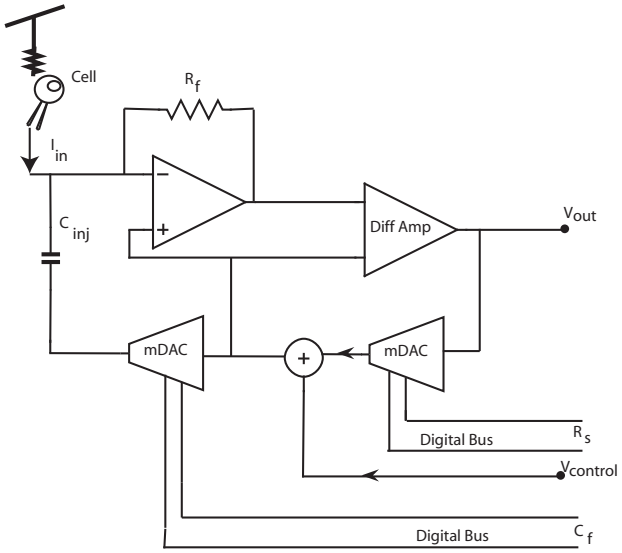


Fig. 2. Patch-clamp amplifier overview. A trans-impedance amplifier followed by a difference amplifier produces an output proportional to the input current. Two feed forward loops provides electrode compensation. The amount of compensation is controlled by two multiplying digital to analog converters (mDAC)s.

## II. System Overview

A whole-cell patch recording system typically measures currents in the range of a few nano-Amperes. A whole-cell clamp reports the current across the entire cell membrane, as opposed to a patch of membrane. Command voltage steps ($V_{com}$) between 10mV and 100mV are applied to the cell membrane during experiments, in order to activate ion channel proteins and to permit ionic currents to flow across the membrane.

Currents are bidirectional depending on the channel type and the membrane potential. The bandwidth of interest is from a few Hz to 10 kHz [6]. A block diagram of our patch-clamp recording system is shown in Fig. 2.

The system consists of an input current-to-voltage trans-impedance amplifier that uses resistive feedback ($R_f$). A difference amplifier subtracts the command voltage from the tranimpedance amplifier's output. The resultant output voltage is proportional to the input current, as in equation 1.

$$V_{out} = I_{in} R_f \tag{1}$$

The system also has two compensation circuits. The first is a series resistance compensation loop which compensates for the voltage drop across the series resistance. A digital setting of the compensated resistance $R_S$ is applied to a multiplying digital to analog converter (mDAC). This mDAC scales the current monitoring signal $V_{out}$ and adds it to the command membrane potential $V_{com}$ in positive feedback polarity. The second compensation for 'fast' capacitance is necessary to remove the effect of electrode's stray capacitance from introducing errors into the $R_S$ compensation [8]. The fast capacitance compensation is a feed-forward loop in which a small capacitor $C_{inj}$ of 5 pF injects a current that is scaled to match the charging current of the electrode capacitance of 1-2 pF in typical electrodes and any other parasitic capacitance. The scaling of the injected current is set by a mDAC using a digital setting of $C_f$.

## III. System Components

The patch-clamp measurement system has three main components: a trans-impedance amplifier, a difference amplifier, and mDACs used for capacitive and resistive compensation. All amplifiers are implemented using a low-noise three stage operational amplifier shown in Fig. 3. The input differential stage is followed by a second stage which allows for higher output swing. The third stage is an output stage. The input $V_{bias}$ sets the quiescent point for the circuit and the inputs $V_{cascP}$ and $V_{cascN}$ provide biases to the cascode devices in the second stage that increases the bandwidth of the operational amplifier.

The series resistance compensation mDAC scales the current-monitoring output voltage of the difference amplifier by an external digital value. The mDAC was designed to scale the output voltage between 0.1-30 times (9 bit resolution). A diagram of the 9 bit DAC is shown in Fig. 4. The series resistance compensation mDAC was implemented as a summing amplifier that has input resistances $RS_1$-$RS_9$ and switches $SR_1$-$SR_9$. The summing amplifier also consists of a feedback resistor $RS_f$. If switch $SR_i$ is closed then a scaled version of input voltage $VS_{in}$ given by equation 2 appears at the output $VS_{out}$ of the summing amplifier.

$$VS_{out} = -\frac{RS_f}{RS_i} \times VS_{in} \tag{2}$$

In addition to the branches that scale the voltage output, the summing amplifier also contains an additional tenth branch

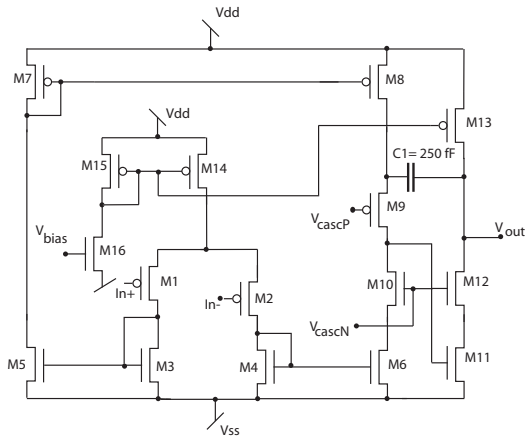


Fig. 3. The operational amplifier used in the design. The input stage was optimized for low-noise performance.

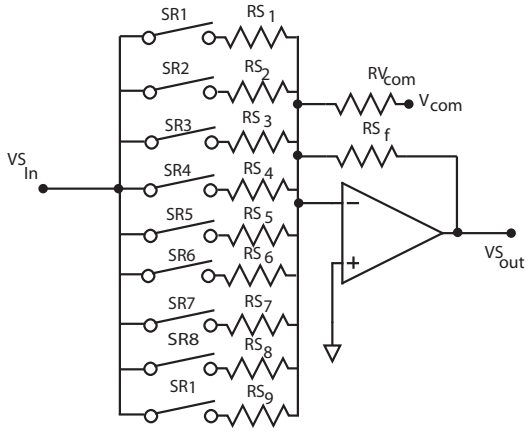


Fig. 4. The series resistance compensation mDAC. The mDAC scales the current monitoring output voltage ($v_{out}$) by a value set by a digital serial bus and adds it to the command voltage $V_{com}$

with input resistance $RV_{com}$=$RS_f$ which adds the command voltage $V_{com}$ with a gain of negative one to the output of the summing amplifier. Therefore, the total output at the summing amplifier when switch $SR_i$ is closed is given by equation 3.

$$VS_{out} = -[\sum \frac{RS_f}{RS_i} \times VS_{in} + V_{com}] \tag{3}$$

In our design, $RS_f$ was chosen as 10kΩ and values of 612.5Ω, 1.25kΩ, 2.5kΩ, 5kΩ, 10kΩ, 20kΩ, 40kΩ, 80kΩ and 160kΩ were chosen for resistors $RC_1$-$RC_9$ respectively. Hence if one desires to add 2 times the output voltage of the difference amplifier to $V_{com}$, one would close $SR_4$ and leave $SR_{1-3}$ and $SR_{5-9}$ open.

The mDAC for capacitive compensation scales the output of the series resistance compensation mDAC. Its output drives a capacitance $C_{inj}$ to compensate for the current lost while charging the electrode capacitance. The compensation value is 1-2 times the output voltage of the series resistance mDAC and has eight bit resolution. The implementation of the mDAC

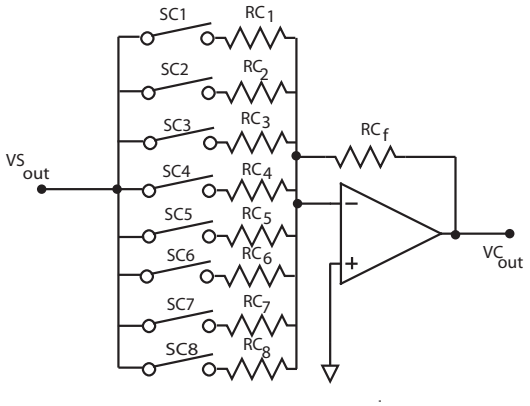


Fig. 5. The capacitive compensation mDAC. The mDAC scales the output of the serial compensation voltage (vout) and connects it to Cinj which injects a current that tries to match the charging current of the electrode capacitance.

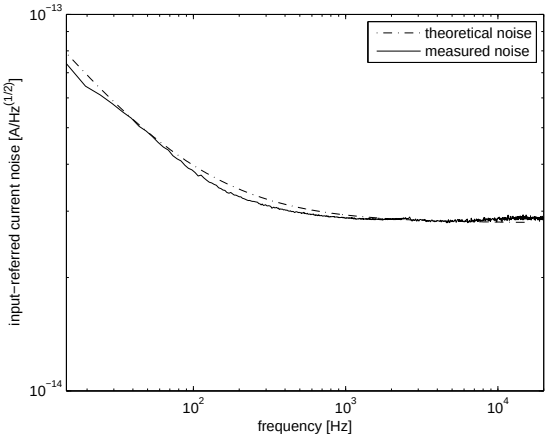


Fig. 6. The measured and simulated amplifier input-referred current noise spectrum. Integration under this curve yields and rms noise current of 4 pA.

for capacitive compensation is identical to the implementation of the series resistance mDAC and is shown in Fig. 5.

When switches $SC_i$ are closed, the output of the capacitive compensation mDAC is given by equation 4.

$$VC_{out} = -\sum \frac{RC_f}{RC_i} \times VS_{out} \tag{4}$$

## IV. Low-Noise Patch-Clamp Amplifier Design

The patch-clamp technique is extremely sensitive to noise due to the low amplitude of the membrane current and hence low-noise amplification is critical to our design. The input-referred current noise of the patch-clamp amplifier is given by equation 5.

$$\begin{aligned} S_I &= \frac{4KT}{R_f} + \left[\frac{8KT}{3g_m} + \frac{K_f g_m^2}{C_{OX} L^2 f}\right] \frac{1}{R_f^2} \\ &\quad + \left[\frac{8KT}{3g_m} + \frac{K_f g_m^2}{C_{OX} L^2 f}\right] 4\pi^2 (C_g + C_{el})^2 f^2 \end{aligned} \tag{5}$$

where K is the boltzmann constant and T is the absolute temperature. The transconductance of the input transistors is given by $g_m$. $K_f$ is the process dependant flicker noise parameter which was extracted as $10^{-25}$ $V^2F$. The critical parameters for low noise amplifier design are the input capacitance, the voltage noise and the input leakage current. The input transistors are vital in establishing these characteristics. The gate capacitance $C_g$ of the input MOSFET is proportional to the area of the transistor, while the thermal noise $e_n$ decreases as the square root of the area (assuming constant gate length). The noise of the recording system is proportional to $C_{in}e_n$ where the total input capacitance is $C_{in}$ = $C_g$ + $C_{el}$ with $C_{el}$ being the capacitance of the electrode and any other capacitance on the input node. By differentiating equation 6 with respect to $C_g$, the optimal gate can be shown to be the gate width corresponding to $C_g$ = $C_{el}$. The flicker noise due to the trapping of charges below the gate of the transistor is a significant problem in making low-noise measurements using MOSFETs. This problem was alleviated using P-channel transistors which have been shown to have one or two orders lower $K_f$ than n-channel devices [9]. As discussed in section II, the trans-impedance amplifier multiplies the input current by $R_f$ to produce a voltage proportional to the input. The current noise at the input can be shown to be inversely proportional to $R_f$. However, the parasitic capacitance and the physical size of of $R_f$ in layout limits its maximum usable value. A conservative $R_f$ of 25MΩ was chosen for our design.

## V. Experimental Results

Fig. 6 shows the measured input-referred current noise spectrum compared with the theoretical current noise spectrum shown by equation 5. Integrating under this curve yields a rms noise current of 4 pA integrated under a bandwidth of 10Hz to 10 kHz bandwidth. The 10Hz limit is due to maximum recording time of 100 ms. This yields a signal to noise ratio of 1nA/4pA = 250 or approximately 7 bits in whole-cell measurements.

We tested the integrated patch-clamp amplifier by sourcing a range of inputs currents from a fraction of a nano-Ampere to a few nano-Amperes, while recording the output voltage. The amplifier was powered at 3.3V using an external battery and the biases and the command voltage was provided by an Analog Instruments AD7304 digital to analog converter (DAC) controlled through an Opal Kelly 3010 FPGA board. The output of the amplifier was digitized using an Analog Instruments AD7475 analog to digital converter (12 bit resolution). The voltage noise on the power supply and the bias voltages was measured as less than 10mV (corresponding to a 0.4nA rms of input-referred current noise). The input current was sourced by applying protocol corresponding to a bidirectional $V_{com}$ of 10mV to 100mV across an Axon Instruments Patch-1U model cell. Fig. 7 shows the protocol used to evaluate the performance of the patch-clamp amplifier.

We obtained a linear dependency across the entire range of tested currents as shown in Fig. 8. The devices consumed

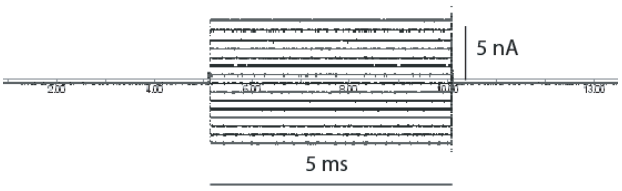


Fig. 7. The protocol used on the Patch-1U model cell to evaluate the patch-clamp amplifier.

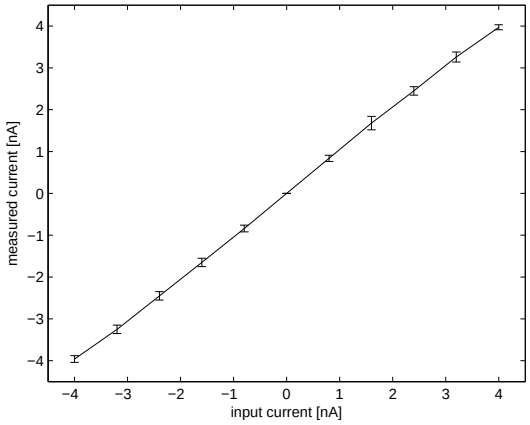


Fig. 8. The measured current from the integrated patch clamp amplifier as a function of input current.

3.3mW of power when operated with a 3.3V power supply.The slew rate of the operational amplifier was measured to be 1.5 $\mu V/s$. The input dynamic range of the amplifier was measured to be 2V pk-pk. The gain-bandwidth product was measured as 2MHz.

We have not tested the electrode compensation because it was designed for the small parasitic capacitance of a planar electrode (1-5 pF). Planar electrodes are currently being acquired to be tested on our system. The usefulness of the electrode compensation circuitry and will be reported in a future publication.

The die size of the integrated patch clamp amplifier is 1479 $\mu m$ x 1316 $\mu m$. A micrograph of the fabricated die is shown in Fig. 9.

## VI. Summary

We designed, fabricated and assembled an integrated patch clamp amplifier with electrode compensation targeted for building high throughput patch-clamp systems. The device uses a transimpedance amplifier to convert an input current to a voltage output. The prototype was fabricated on conventional AMI 0.5 micron technology. The low-noise amplifier used in the design produced less than 4 pA of rms noise. The device is capable of measuring nano-amperes of current making it ideally suited to fabricate high-throughput whole-cell patch recordings arrays.

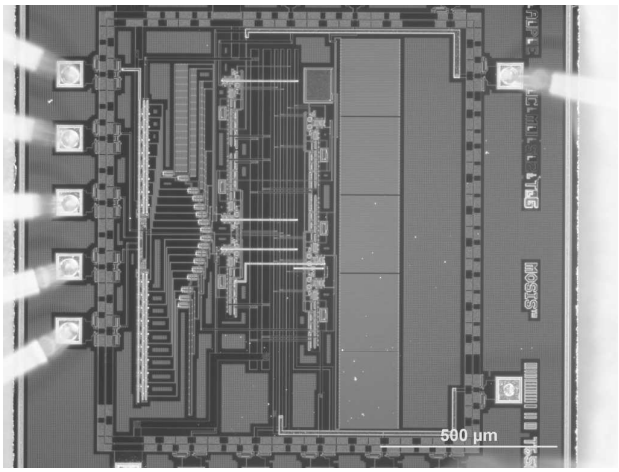


Fig. 9. Figure 7. Die micrograph of the integrated patch-clamp amplifier

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