# An Integrated Patch-Clamp Amplifier in Silicon-on-Sapphire CMOS

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***Abstract*— We fabricated an integrated patch-clamp amplifier capable of recording from pico- to tens of micro-amperes of current. The high-dynamic range of seven decades and the pico-ampere sensitivity of the instrument was designed for whole-cell patch-clamp recordings. The prototype was fabricated on a 0.5$\mu$m silicon-on-sapphire process. The device employs an integrating headstage with a frequency-modulated output pulse ranging from 3Hz to 10MHz. A digital interface produces a 16bit output conversion of the input currents. We report on electrical measurements from the fabricated device, and measurements conducted on cells in a typical patch-clamp experiment.**

## I. Introduction

*Patch-Clamp* is an extraordinary technique used in electrophysiology to measure the currents flowing through the membranes of living cells. These recordings are crucial for the study of ion channels, which are the molecular structures responsible for the membrane conductivity [1], [2]. Patch-clamp can measure the cell conductance as it depolarizes and is normally used to study the effect of drugs and medical treatments on the dynamics of action potentials. The progress of ion-channel research and the study of living cells is strictly related to the availability of advanced instrumentation. Emerging integrated circuit technologies, especially the planar patch-clamp technology, are beginning to make large-scale screens of genes and compounds possible.

Because of the importance of the patch-clamp technique in drug testing, pharmaceutical companies have long sought ways to increase the number of tests per unit time by using integrated circuits. The proposed instrumentation is now key to the development of pharmaceutical drugs. Recently, several common prescription medicines have been recalled or curtailed [3]. The peril is that these drugs can potentially contribute to patient's sudden death due to cardiac arrhythmias by prolonging the action potential in the heart's ventricles. As a result, the U.S. Federal Drug Administration now requires that every drug be screened for its impact on the length of ventricular action potential, and recommends a test for drug effects on ion-channel function [4]. The need for higher throughput screening instrumentation is thus a limiting factor for pharmaceutical companies' efforts to bring better and safer medicines to the consumer market.

In this paper we present a high-performance integrated patch-clamp amplifier. Our design employs emergent integrated circuit technologies to provide low-noise amplification of ion-channel currents and high-density integration of electronic components. The silicon-on-sapphire (SOS) fabrication process for integrated circuits [5] features a non-conductive substrate and high-quality component isolation. These features can significantly reduce electronic coupling noise in sensitive current-recording equipment such as patch-clamp amplifiers.

An integrated version of the patch-clamp amplifier not only reduces the size of the instrumentation, but also obtains better electrical performance, since cabling and parasitic capacitances that lower the measurement bandwidth are kept to a minimum. The implementation of the integrated circuit in silicon-on-sapphire further reduces the capacitance by removing the influence of the substrate.

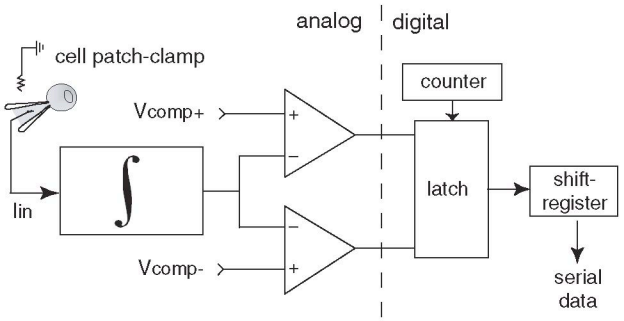


Fig. 1. Patch-clamp amplifier overview. The analog portion of the circuit integrates the input current up to a positive or negative threshold $V_{comp+}$ and $V_{comp-}$. After integration, a digital pulse latches an oversampled 16-bit counter to produce a digital output.

## II. System Overview

Ion channel currents range from a few pico-amperes for single-channel recordings to tens of nano-amperes for whole-cell measurements. Voltage steps between 10mV and 100mV are applied to the membrane during an experiment, in order to activate ion channel proteins and permit ionic currents to flow across the membrane. Currents are bi-directional, depending on channel type and membrane potential, and the bandwidth of interest is between a few Hertz to 10kHz in bench-top systems. Higher sampling rates and bandwidth are desired for more precise characterization of ion channels. The patch-clamp amplifier must have a large dynamic range in order to record the large transient currents after the stimuli, and

must be highly sensitive to currents in the pico- to nano-ampere range. To this purpose, we have designed an integrated circuit based on asynchronous sigma-delta analog-to-digital converters. The sensor is based on a pulsed-output current integrator circuit with reset frequency proportional to the input current. This architecture permits high oversampling ratios at the bandwidths of interest. A block diagram of our patch-clamp system is shown in Figure 1.

The input current is integrated over a capacitor until the integrator output reaches either of the compare voltages $V_{comp+}$ or $V_{comp-}$. At the end of integration, the change in the comparator's state generates a pulse. The digital components of the system comprise a 16-bit counter, latch and shift-register. The counter is free-running, and its value is latched when a pulse from the analog circuitry is detected. This value is then transferred to the shift-registers, and serially communicated to a computer-based data-acquisition system. Since the output data is oversampled and synchronous by means of an external clock, the time between two integration pulses can be measured accurately. The difference between two latched values thus yields the integrator's reset frequency. This frequency can be used along with the system transfer function in equation 1 to calculate the input current.

$$I_{in} = C_{int} \Delta V f_{pulse} \tag{1}$$

$I_{in}$ is the input current, $C_{int}$ the integration capacitance used in the integrator, and $\Delta V$ is the voltage swing of the integrator.

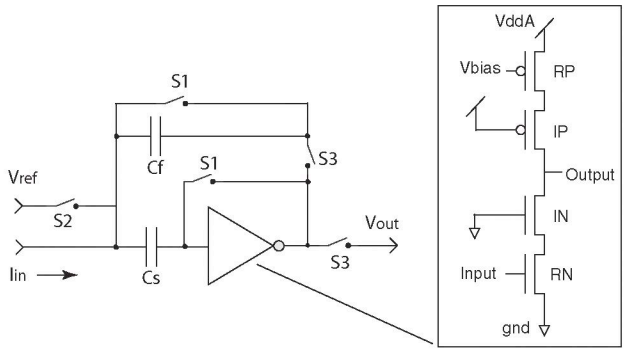


Fig. 2. The headstage of the patch-clamp amplifier is a current integrator. During the reset phase switches S1 and S2 are closed. During the integration phase switch S3 is closed. The cascoded inverter is portrayed in the insert.

## III. System Components

The patch-clamp technique is very sensitive to noise, due to the low amplitude of the membrane current. In order to minimize the impact of the noise sources in our integrated system, we have employed a switched-capacitor implementation [6]. This realization also reduces the power consumption. The major sources of noise in the patch-clamp amplifier circuits are Johnson noise, shot noise and flicker noise. Flicker noise is the dominant source of noise in integrated MOSFET circuits. It is caused by the entrapment of electrons in the transistor gate-oxide and varies as the inverse of operating frequency, becoming a serious problem at the low frequencies of operation of the patch clamp amplifier. Since it is a noise correlated in time, flicker noise can be subtracted using Correlated Double Sampling (CDS) [7]. We have used CDS in our design to cancel flicker noise and to reject noise at low frequencies. The switching capacitors introduce reset noise ($kT/C$) but the noise generated by this source is minor in comparison to the headstage shot noise, which is the dominant noise source in our system. An analysis of the noise sources in our system shows that at a sampling frequency of 10kHz, we expect 2.5pA rms noise current while measuring a 3nA input current.

There are two main components in the analog circuitry of our chip: the *integrator* and the *comparator*. All amplifiers are implemented using single-stage cascoded inverters which offer high-gain and low noise when operated in the sub-threshold region [8]. The cascoded inverter schematic is shown as an insert in Figure 2 and 3. The active transistor loads on the input transistor increase the gain of the inverter. The gain of the amplifier can be controlled by tuning $V_{bias}$ and operating the circuit in the high-gain subthreshold region. The gain was measured in simulation to be 2000, and to vary only 2% with a 10K temperature change.

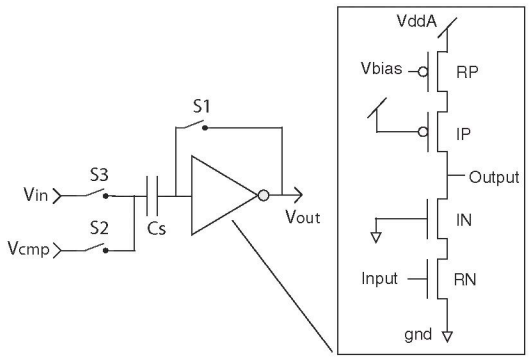


Fig. 3. Comparators used in the patch-clamp amplifier to detect the end of integration cycles. During the reset phase switches S1 and S2 are closed, while S3 is closed during the comparison phase. The cascoded inverter is portrayed in the insert.

### A. Integrator

A schematic of the integrator is shown in Figure 2. The integrator uses a user-selectable 60fF or 600fF feedback capacitor $C_f$ to sense the input current. The integrator is initially reset to a reference voltage $V_{ref}$, chosen to be approximately at the middle of the integration voltage swing. Using a 3.3V supply, $V_{ref}$ is set to 1.6V, to maximize the integration range. Since the system uses CDS, two samples are taken for each measurement. The first sample is taken during the reset phase of the system, when $V_{ref}$ is connected to the input of the amplifier and switches S1 and S2 are closed. This voltage is stored on capacitor $C_s$, together with any correlated input noise. The input and output of the inverter are shorted, forcing both nodes to the inverter's logic threshold and highest gain.

The second sample is collected during the operating phase of the circuit (switch S3 is closed), when the device is integrating the input current. Since the voltage noise is stored on $C_s$, the current seen by the integrator is the difference between the samples. Time-correlated noise such as flicker noise is thus subtracted from the integration voltage. The integrator's three-phase reset is designed to minimize the charge injection due to simultaneous switching. The switching sequence is S1, S2, S3 in Figure 2.

### *B. Comparator*

The comparator design uses the same principles as the integrator headstage. The schematic for the comparator is shown in Figure 3. The input node is switched between the integrator output $V_{in}$ and the compare voltage $V_{cmp}$, and the amplifier is operating in open-loop configuration. The operation is divided in two phases. During the reset phase (switches S1 and S2 are closed), the compare voltage $V_{cmp}$ is stored on capacitor $C_s$, together with any correlated noise. The inverter is also initialized to its logic-threshold. During the comparison phase switch S3 is closed. The input $V_{in}$ is connected and the comparator changes state when this voltage exceeds $V_{cmp}$. We employ two separate comparators in our circuit, one with a positive compare voltage and the other with a negative one with respect to $V_{ref}$, as portrayed in Figure 1. The value of $|V_{ref} - V_{cmp}|$ was set to 0.5V. The device logic circuitry is designed so that each comparator generates a positive output when it reaches the comparison point. This pulse latches the counter and serves as reset signal for the entire system.

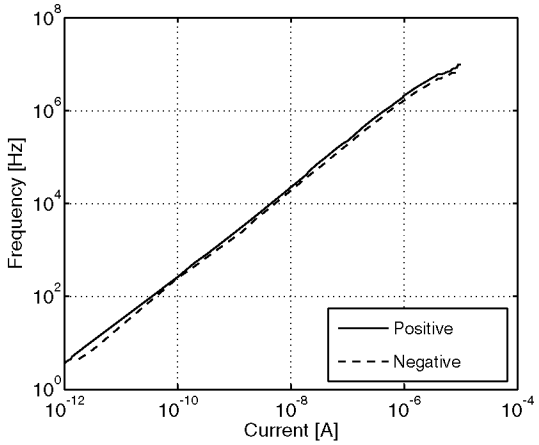


Fig. 4. Output pulse frequency of the headstage integrator as a function of positive and negative input currents, as integrated on a 600fF capacitor. The dynamic range of the patch-clamp amplifier was measured to be 7 decades.

## IV. Results

We tested the integrated patch-clamp amplifier by sourcing a range of input currents from a few micro-amperes to a pico-ampere, while recording the frequency of the output pulse. The amplifier was powered at 3.3V with an Agilent 3631A DC power supply. The voltage noise on the power supply and the bias voltages was measured as less than 2mV rms. The input currents were sourced by applying a voltage across a mega-ohm resistor. A Keithley 2400 Source Meter was used to source and measure the input current. The frequency of the output pulse was measured using a Tektronic TDS2014 Four Channel Digital Storage Oscilloscope. We obtained a linear transfer function across the entire range of tested currents in the range: [3pA, 10$\mu$A], as shown in Figure 4. The output pulse frequency was in the range: [3Hz, 10MHz], and was observed to increase in discrete steps when very high currents were sourced, as quantization noise due to low oversampling became dominant. We operated the device with clock frequencies of up to 50MHz, and were thus able to extend the upper-limit of the current measurements. The use of fast clocks and the silicon-on-sapphire process make this device one of the largest dynamic-range current measuring system reported [6].

In order to obtain reliable whole-cell recordings, it is important to have a highly linear response in the nano-ampere range. We quantified the chip response for source currents of up to a few nano-amperes, using two different integrating capacitors. The difference in the integration of positive and negative current is due to charge-injection from the switches in both the integrator and the comparators. The charge-injection affects the small integrating capacitor and reduces the integration voltage-swing of positive current as opposed to negative ones.

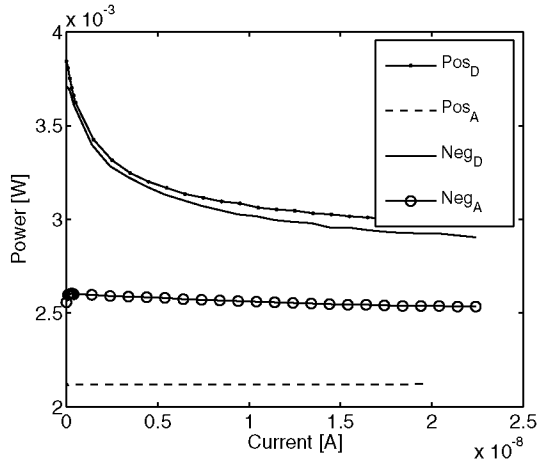


Fig. 5. Power consumption of analog and digital circuitry of the SOS integrated patch-patch amplifier. The power consumption was estimated for both positive and negative currents and for both analog and digital supplies.

The power consumption of the patch-clamp amplifier was estimated for both positive and negative currents and for both analog and digital supplies. The results for the nano-scale currents range of interest are plotted in Figure 5. We observed that the power consumption increases at very low currents and low output pulse frequencies. The slow integration of low currents causes the digital interface to spend a long time near the logic threshold. This causes short circuit currents in the digital supply. Also notice the dependency of the analog power consumption on the direction of the current, due to charge

injection. For higher current (not in Figure 5) both analog and digital power consumption increases with current as the reset frequency rises.

The die size of the integrated patch-clamp amplifier measures 1260$\mu$m by 1040$\mu$m with pads and 1140$\mu$m by 560$\mu$m without pads. The headstage integrator measures 150$\mu$m by 225$\mu$m. A micrograph of the fabricated die is reported in Figure 6.

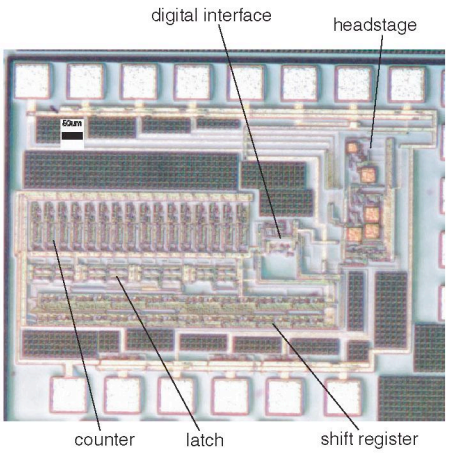


Fig. 6. Die micrograph of the SOS integrated patch-patch amplifier. The die size is 1260$\mu$m by 1040$\mu$m.

## V. Experiments

To verify the usefulness of the patch-clamp amplifier in life-science applications, we used the patch clamp amplifier to measure the ionic conductances of Rat Baso-Lateral cells (RBL). The data collected from the RBL cells is due to inward rectifier potassium channels, which conduct only in the inward direction. Figure 7 show the time response as step voltages are applied to the RBL cells. The y-axis shows the measured voltage (at the output of the analog filter), which relates linearly to the measured current.

We have connected our device in series to a commercial patch-clamp amplifier, so that we could use its data acquisition software and real-time visualization. DACs driven by the commercial HEKA amplifier software were used to provide voltage steps to an external resistor connected to the amplifier's input node. We decoded the amplifier response by taking the digital reset pulse train at the output of the amplifier and RC filtering it with a time constant of 100$\mu$s. The filtered positive and negative reset spikes were then passed through a difference amplifier and low-pass filtered using an analog 8-pole Bessel filter. This was equivalent to converting the variable-frequency reset spikes to scaled analog voltages and provided an efficient way for quantifying circuit current. The filter output was digitized at 10KHz by standard patch-clamp software Digidata and visualized using Clampfit version 8.2.

## VI. Summary

We designed, fabricated and assembled an integrated patch-clamp amplifier targeted to whole-cell patch-clamp measurements. The device is capable of recording from pico- to tens of micro-amperes of current, providing a very high-dynamic range and sensitivity. The prototype was fabricated on a conventional 0.5$\mu$m silicon-on-sapphire process, taking advantage of the low-power and low-noise property of the device and the insulating substrate. The device uses an integrating headstage with pulse-modulated output ranging from 3Hz to 10MHz and operating with a system clocks of 10Hz to 50MHz. A digital interface produces a 16bit output conversion of the input currents.

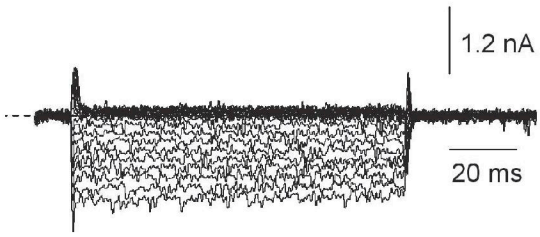


Fig. 7. Patch clamp measurement of membrane currents in a RBL cell. Currents recorded in response to repeated step changes in membrane potential from -200mV to +200mV, incremented by 10mV. The current represents the inward rectifier current native to these cells.

## VII. Acknowledgements

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