MODELING HOT-ELECTRONS EFFECTS IN SILICON-ON-SAPPHIRE MOSFETS

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ABSTRACT

A unified, closed form analytical drain current model for partially and fully depleted SOS MOSFETs was investigated. The analytical model was developed using first order principles of operation of the device and basic explanation of the physical constraints responsible for hot carriers effects. The approach solved for the channel field to find closed form solutions for the critical voltages giving rise to kink effects and output nonlinearities. The reliability of the model was addressed and verified with experimental data.

1. INTRODUCTION

Hot electron effects generally limit the performance of analog circuits designed in Silicon on Insulator (SOI) technologies. These effects are responsible for many floating body behaviors and irregularities in SOI devices.

At high values of drain to source voltage (Vds) and in saturation, SOI devices typically produce an undesirable deviation from classical MOSFET operation in the saturation region. The drain current exhibits a change of slope for higher Vds due to hot carrier effects. Figure 1 shows typical characteristics measured for regular threshold MOSFETs fabricated in Peregrine Semiconductor's Silicon on Sapphire (SOS) process.

The kink-like behavior in the SOS devices is due to the acceleration of channel carriers. As Vds rises, the pinch-off of the device causes carriers in the channel to group around the source (Figure 2). This accumulation generates a high electric field between the channel and the drain of the device. If the field surpasses a critical value, carriers from the channel itself are accelerated to the point at which they provoke impact ionization as they reach the drain.

Impact ionization generates two carriers from a single one at the drain of the device. Generated minority carriers

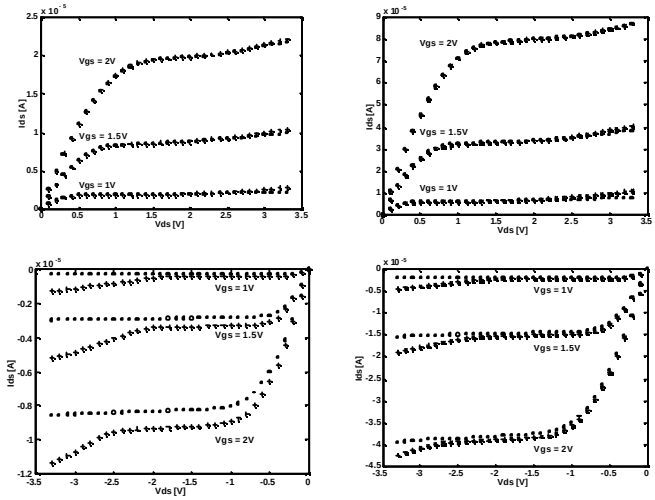

Figure 1. Hot Carrier effect in regular threshold SOS devices with bulk contact (circle) and with bulk floating (plus). Right pictures are for W/L = 5x1.2um devices, left pictures for 5x5um devices. Top pictures are for a NMOS, bottom for a PMOS.

move rapidly up the drain, while the majority carriers flow into the floating body of the device.

Data collected from our sample transistors shows that PMOS devices have a much more noticeable kink effect. This is due to the enhancement of the carrier lifetime to match the mobility of p-channel devices to the mobility of n-channel devices.

In thin-film SOI devices [1], full depletion gives the silicon below the gate an almost infinite resistance, which renders body contacts completely ineffective. Since the devices we tested and measured still produced a significant reduction of the kink effect by using bulk contacts, we conclude that the devices are not fully depleted.

For the devices to be fully depleted, the maximum depletion region, given by:

$$x_{d\max} = \sqrt{\frac{4e_{si}f_F}{qN_A}}$$

must be higher than the silicon thin film. In our case xdmax = 52nm at threshold, while the silicon locos thickness is 60nm.

The kink effect can be eliminated by providing a contact to the floating body of the device. This contact allows the draining of majority carriers out of the device body, provided that the resistance of the body is not too large. In this case, in fact, the body contact is not completely sufficient to eliminate kink effects.

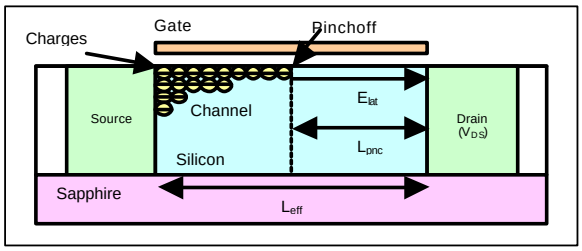

Figure 2. Electric field and pinched channel in a SOS MOSFET.

Kink behavior is generally not modeled and not included in circuit simulators. This in turn renders the design of analog circuits more intriguing and more prone to undesired output mismatches with the original model. While the kink does not constitute a problem for digital design, where the increase in current makes the circuit faster, for analog circuits it is certainly a worrisome behavior that has to be taken into account. Conventional circuit blocks like current mirrors may have unpredicted additional mismatch, while the gain of amplifiers is doomed to nonlinearities and lower amplification ratios.

In the following sections a comparison of conventional modeling techniques for SOI processes and novel modeling techniques will be given.

2. STANDARD KINK EFFECT MODELS

It has been pointed out by the literature [4] [5] that the kink effect due to hot carrier degeneration can be attributed to avalanche phenomena. Specifically, the current increase in the drain due to impact ionization would generate a positive feedback mechanism. When the energy of the hot carriers is high, avalanche phenomena occur, and the current is multiplied by an exponential factor M. This parameter models the exponential behavior of the device under the influence of high-energy carriers from the channel. The value of M can be computed by assessing the positive feedback current generated by impact ionization.

$$M = 1 + A(V_{DS} - V_{DSk})\exp\left(-\frac{B}{V_{DS} - V_{DSk}}\right)$$

$$I_{DSk} = MI_{DS}, \quad V_{DS} \geq V_{DSk}$$

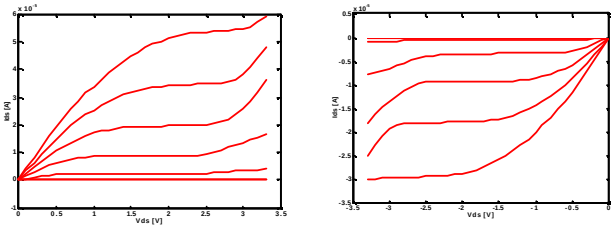

Figure 3. Standard SOI MOSFET avalanche kink model. Left picture is for 5x1.2um NMOS, right picture for same size PMOS.

This equation [3] gives an expression for the drain current in the kink region as a function of the drain current obtained with standard models. The multiplicative factor is linearly proportional to the drain to source voltage for small Vds after the critical Vdsk, then assumes an exponential dependence. In the model A, B are process dependent parameters, while Ids is the first order model for a transistor in saturation, defined as:

$$I_{DS} = \frac{K}{2}(V_{GS} - V_{th})^2 [1 + l(V_{DS} - V_{DSsat})], \quad V_{DS} \geq V_{GS} - V_{th}$$

When Vds surpasses the critical value Vdsk, the drain current is multiplied by a factor that models the effect of avalanche in the impact ionization.

After trying to fit our data with the above model it was discovered that the SOS process under consideration was not able to replicate the exponential behavior in the kink. Figure 3 shows a fit of the conventional avalanche model applied to our set of data. The kink effect clearly has a more linear dependence with the drain to source voltage Vds, and there was no trace of the exponential behavior found in the literature, at least for Vds in the conventional operational range of up to 3.3V. This signifies that no avalanche current multiplication occurs in a SOS RP MOSFET, on the other hand the hot carrier clearly generate a linear increase in the drain current, proportional to their number. The impact ions are instead not able to generate secondary ions by ionization, since their energy is at the most half of the originating hot carrier.

3. HOT CARRIER GENERATED KINK EFFECT

The generation of hot carriers appears when the electric field inside the pinched channel surpasses a critical value. Values of this field are at minimum 10^6 V/m [2] or $2 \cdot 10^7$ V/m [4]. The value of the critical voltage Vdsk at which kink effect arises is determined by the distance between the pinched-off channel and the drain (Lpnc in Figure 2).

When reaching this value of Vds, electrons from the channel can accelerate to the drain area and therefore produce impact ionization. Vdsk, similarly to Vdssat, is influenced by Vgs. In fact, the channel profile is flattened by higher Vgs, when Vds is held constant. When the

channel is flattened, at higher Vgs, the effective critical length Leffk is attained later than predicted. If Vgs increases, so must Vds in order to maintain the same Lpnc and the same electric field. In other terms, Vgs subtracts to Vds and reduces the pinched off region of the channel. The electric field manifests between the channel and the drain in the pinched off region. Although the electric field is high for short pinched off length Lpcn, the distance is not enough to accelerate the carrier above the impact ionization energy. Therefore both high channel electric field and a high Lpcn is necessary to give carriers the sufficient energy to provoke impact ionization at the drain region.

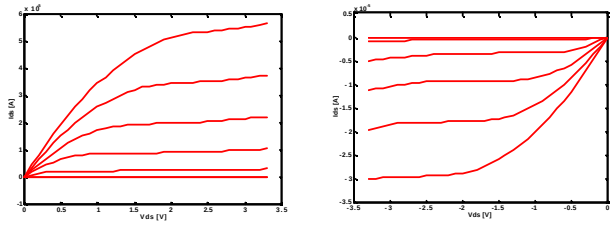

Figure 4. Proposed SOS MOSFET kink model. Left picture is for 5x1.2um NMOS, right picture is for an identical size PMOS.

We can also express the energy Ej of a carrier immersed into the pinched-off device electric field using the relation:

$$E_J = q\int_l \vec{E}_{lat}\, dl$$

Carriers in the channel must surpass a critical energy threshold in order to provoke impact ionization at the drain, we will call this critical energy Ejc. Ejc is the value of Ej, imposed by some limit values of the pinched off length 'l' and the lateral electric field. We can therefore express the critical drain Vdsk voltage, since the voltage scalar is itself defined as the work the field has to perform on a particle to move it from one region to another:

$$V_{DSk} = E_{Jc} / q$$

A value of the electric field inside the channel can be computed by solving the Gauss equation in an small box contour region. Since solving the integral for Ej is very involving and brings excessive complication into the model, we can approximate the value of the lateral electric field at the point where the channel is pinched-off as:

$$E_{Jc} = \frac{-q(2-h_1)\cdot V_{DSsat}}{L_{eff} - L_{pnc}}$$

η1 is a fitting parameter that takes into consideration the error in the approximation of the field and its distribution between the source and drain. Leff and Lpnc are respectively the effective channel length and the pinched-off length of the channel. Vdsk can be therefore expressed as:

$$V_{DSk} = \int_l \vec{E}_{lat}\, dl = q\int_l \frac{-(2-h_1)\cdot V_{DSsat}}{L_{eff} - L_{pnc}} dl$$

The value of this integral results into:

$$V_{DSk} = V_{DSk\,0} + \frac{-(2-h_1)\cdot V_{DSsat}}{L_{eff} - L_{pnc}} L_{pnc}$$

Note that the pinched off region of the channel is only the depletion region of the drain to channel reverse biased diode. In fact, the pinched off area is the region that contains no inverted minority carriers by definition. While a bi-dimensional computation of the depletion region would require numerical methodologies, the only important value for our analysis is the value at the interface with the silicon dioxide, where the electric field is confined by the boundary conditions imposed by the MOSFET geometry. The depletion region between drain and channel can be computed as:

$$L_{pnc} = \sqrt{\frac{e_{si}}{q}\frac{N_A + N_D}{N_A N_D}(f_F - V)}$$

Where V = Vds-Vgs+Vth (being the difference between drain voltage and the pinch-off point of the channel), while εsi, Na, Nd, ϕf are the permittivity of silicon, the drain and channel implants and the Fermi level of the drain to channel diode respectively. The potential at the drain is Vds, the pinch-off voltage is Vdssat. Imposing Vdssat = Vgs-Vth, a final value for Vdsk can therefore be calculated.

The dependence of the critical voltage on Vgs can be explained by thinking about the distribution of charge in the channel. Submicron devices constructed on thin silicon will have a nonlinear channel shape. Rising Vgs will stretch the channel toward the source, at a given Vds. This in turn decreases the pinched-off region of the channel. The electric field seen by channel's electrons will then be lower than the critical value. Because of this, at higher Vgs the kink appears at higher Vds. That is equivalent to say that Vdsk increases with Vgs.

When the lateral electric field surpasses the critical value, the carriers accelerated by such a field are able to create impact ionization close to the drain region. This mechanism increases the drain current and at the same time generates a majority carrier current to the bulk. The minority current influences the bulk potential effectively modulating the transistor threshold [3].

The majority carriers injected into the body can forward bias the source body diode, creating a current:

$$I_{BS} = I_{S0}\left(e^{\left(\frac{V_{BS}}{V_T}\right)} - 1\right)$$

The drain current of the SOS MOSFET can then be calculated using the following relation, given that the device is in saturation and the drain to source voltage exceeds the critical voltage Vdsk.

$$I_{DS} = \frac{K}{2}(V_{GS} - V_{thk})^2[1 + l(V_{DS} - V_{DSsat})],\quad V_{DS} \geq V_{GS} - V_{th}, V_{DS} \geq V_{DSk}$$

Note that the drain-current slope n changes slope once reached the critical voltage Vdsk,. This effect is the kink

behavior itself. Given the linearity of the kink drain current with the drain to source voltage, we can model the kink itself as a change in the threshold of the device. This change is linearly proportional to the drain to source voltage Vds.

$$V_{th} = V_{th0} - x(V_{DS} - V_{DSk})$$

The threshold of the transistor is the shifted down by a quantity proportional to the Vds voltage. The parameter ξ was estimated empirically to be of 0.03 for an NMOS transistor and 0.09 for a PMOS transistor both of 5x1.2um channel size.

When a contact to the bulk is provided, modulation of the bulk by injection of majority carriers cannot occur. In fact, when the bulk is connected to the source or a lower potential, all the majority carriers are collected by the source diffusion. Figure 5 shows the bulk current for a RP SOS MOSFET with 4 terminals. The currents are exponential and follow the behavior modeled by the above equation.

The model for the saturation region was the same simple first order model discussed in the previous section.

4. RESULTS AND DISCUSSION

All transistor characteristics tests were conducted in an electrically shielded, dark chamber. The environment temperature was not strictly controlled, but remained around 293K for the duration of the experiments.

The SOS devices, as can be seen in Figure 1, present not only a kink effect but also a noticeable change in the saturation currents when operated with 3 terminals, with respect to the same device operated with 4 terminals and bulk contact. This effect is due to a threshold change in the devices resulting from the accumulation of majority carriers in the channel. Since the saturation current is higher for a floating body (3 terminal) MOSFET, the threshold is effectively diminished. The decrease of the threshold voltage Vth was measured to be on the order of 0.07V for a RP SOI transistor while there was no threshold change for the corresponding NMOS device. Both devices size was 5x1.2um. The threshold change can be attributed to the creation of a charge pocket inside the bulk of the PMOS device. The lower threshold is due to the bulk modulation resulting from the majority carriers trapped inside the bulk. This modulation manifests as a non-zero bulk to source voltage Vbs. Inverting the floating body equation, we can calculate the resulting Vbs voltage:

$$V_{BS} = \left(\frac{\Delta V_{th}}{g} + \sqrt{|2f_F|} \right)^2 - |2f_F|$$

Our measurements on a RP 5x1.2um transistor, lead to a Vbs of 0.154V. Using the Ibs current relation we can therefore assume that the Ibs current is on the order of 44.48nA.

A measure of the bulk current in a 4 terminal PMOS device, as appears in Figure 5, proves the effectiveness of the bulk contact in the removal of the majority carriers trapped in the body and also provides means to assess their amplitude.

Note again that Vbs remained practically zero for the NMOS device. Therefore, we report that no trapping of majority carriers occurs in the bulk of a floating body NMOS device in the SOS process.

The kink effect reported for our devices can be modeled purely by a threshold shift. The majority carriers injected from the drain to the channel increases with the onrise of hot electrons. This in turn generates a current to the bulk. Since the lifetime of the carriers in the bulk is higher than the recombination rate, the bulk voltage Vbs rises and results in a effective decrease of the threshold.

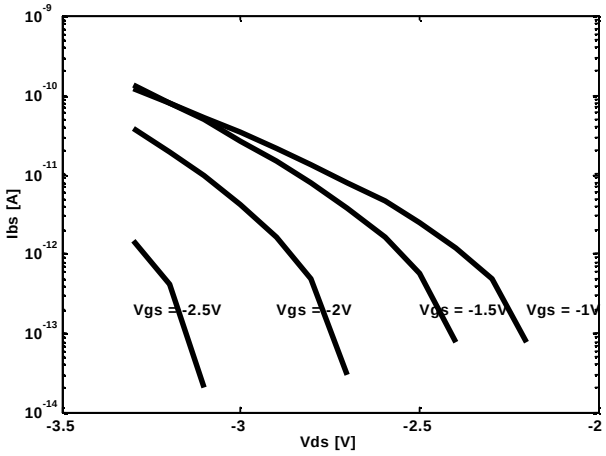

Figure 5. Bulk current in a four terminal RP SOS transistor .

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