Digital Phase-Shift Modulation for an Isolation Buffer in Silicon-on-Sapphire CMOS

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***Abstract*— We designed and fabricated a 4-channels digital isolation amplifier in a 0.5μm Silicon-on-Sapphire technology. The isolation device was fabricated on a single die, taking advantage of the isolative properties of the sapphire substrate. The individual isolation channels can operate in excess of 40Mbps using digital phase-shift-keying modulation. Modulation of the input signal is used to increase immunity to errors at low input data rates. The device can tolerate ground bounces of 1V/μs and isolate more than 800V. The device uses N+1 capacitors for N channels as opposed to $2N$ of previous implementations, thus minimizing the coupling silicon area and increasing reliability. Typical applications are in harsh industrial environments, transportation, medical and life-critical systems.**

I. Introduction

A digital isolation amplifier is an electrical circuit that communicates an input digital signal from one region to an output digital signal in a second region that are electrically isolated from the first one. The isolation of communication circuits is desirable in environments where ground loops are present, or where it is not possible to ensure a common ground reference between output and input nodes. Typical applications are in harsh industrial environments, where ground currents are present due to leakage from the machinery's power supply. Isolation is also used to prevent human personnel injuries or equipment damage and in the medical field, where it is necessary to isolate human subjects from data-acquisition and life-critical systems. Applications are also found in the military field, for high reliability systems and transportation.

An integrated version of an isolation circuit is conventionally an assembly of two separate dies packaged together, as in the case of optocouplers [1], bulk capacitive coupling [2], and optical interconnections [3]. The cost of the isolator can be high because of the expenses and the difficulties in packaging two dies with the desired isolation properties. In addition, the power consumption is higher due to the parasitic capacitances and inductances of multi-chip modules. In a conventional bulk process, the isolation of two circuits on the same die is not achievable because of the presence of a common galvanic substrate. Capacitive coupling has been employed in bulk CMOS multi-chip modules to transfer data signals between multiple dies [4], [5], [6]. On-chip isolation using a Silicon-On-Insulator (SOI) substrate has been demonstrated for modem lines and for data only [7].

By taking advantage of the isolation properties of the Silicon-on-Sapphire (SOS) substrate [8], we previously designed and fabricated a monolithic single chip isolation device [9], [10]. In this paper we improve on this design by employing a digital phase-shift-keying modulation of the input signals and reducing the silicon area and the number coupling capacitors per channel (Figure 1). Modulation is used to increase immunity to errors at low input data rates. The device uses N+1 coupling capacitors for N channels, in contrast to the $2N$ capacitors used in previous implementations. Thus the coupling area and number of capacitors is minimized to obtain higher reliability. The following sections report on the design, modeling and test results of the SOS digital isolation amplifier.

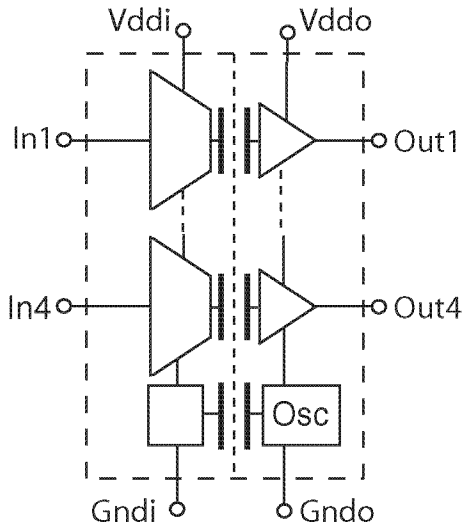

Fig. 1. System architecture: the four channels digital isolation amplifier. The digital modulating clock is powered by the receiver side (right) and transmitted capacitively to the transmitter (left).

II. System Overview

Figure 2 is a detailed schematic of one of the four isolation channels named *isoCap3sc*. The specification for each channel required a data rate of 40Mbps, military range temperatures, and input signal rise/fall time between 10ns and 1.5ns. The required isolation was at least 100V in continuous mode. The

device is designed to withstand ground bouncing of more than 1V/μs using a circuit topology able to reject spurious transitions. This feature is obtained by using digital modulation of the input signal before transmission to the receiver through the capacitive isolation interface of Figure 2. The use of modulation increases the switching frequency across the coupling capacitor. Spurious transitions are eliminated if the switching frequency is higher than the maximum allowed ground-bouncing. The input signal is buffered and modulated at the transmitter (input) side and communicated to the receiver (output) circuit using capacitive coupling. Each stage's coupling capacitor C_f has a capacitance of 150fF and has been designed using metal-1 and metal-3 plates. The silicon area used by the capacitor is 175 x 60μm^2.

Notice that our first isolation device [9], [10] used two capacitors per channels, while *isoCap3sc* only uses one capacitor, thus saving precious silicon area. In addition the previous device provided non-zero bit-error-rates (BER) at low input rates. We measured BER of $6 \cdot 10^{-7}$ for a 10KHz input. The device reported in this article, thanks to the digital modulation of the input signal, did not suffer from bit-errors at low frequencies.

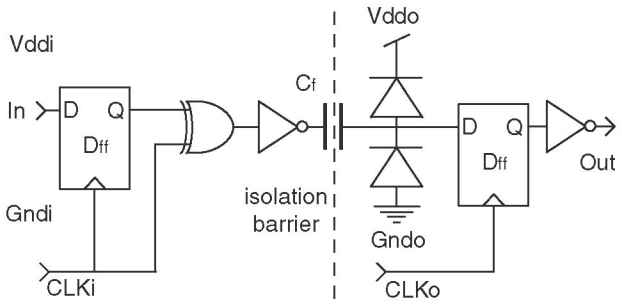

Fig. 2. The *isoCap3sc* isolation channel

A 180 degrees phase-shift-keying modulation is performed by XOR-ing the input signal with the transmitter clock *CLKi*. The transmitter clock is obtained through capacitive coupling from the receiver side, where the global clock is generated. We use a 13-stage ring oscillator at the output side to produce an approximately 200MHz digital clock signal that modulates the input signal. A D-Type Flip-Flop synchronizes the modulation and demodulation to avoid spurious transitions of the output due to transmission delay. The input Flip-Flop operates on the rising clock edge. The demodulator is a Flip-Flop synchronized to the falling edge of the clock *CLKo*. The output of the *isoCap3sc* isolation channel is the terminal *Out* in Figure 2. At the receiver side, protection diodes located at the receiver input node enforce that the voltage at the floating nodes always drifts to one of the supplies, to prevent damage in case the ground-bouncing rate is much faster than the modulation rate.

The final prototype of the capacitive isolation buffer in Figure 1 (named *isoCap3*) is organized as an array of 4 independent isolation channels *isoCap3sc* in one single chip. All channels share the same input and output power supplies. For each channel the input pads are protected against surges by using protection clamp diodes connected to their power supply. Output pads are buffered with digital inverters to be able to drive a 25pF capacitive load.

III. Capacitive Coupled Isolation Circuit Model

In an effort to model the performance of the isolation circuit, we compute here two important design parameters:

(A) the minimum isolation capacitance for signal coupling

(B) the minimum input slew-rate necessary to detect a transition

A. Minimum Capacitance:

Figure 3 is a model of the capacitive-coupling circuit: C is the isolation capacitor, C_a and C_b are the parasitic capacitances at the two terminals of the isolation capacitor.

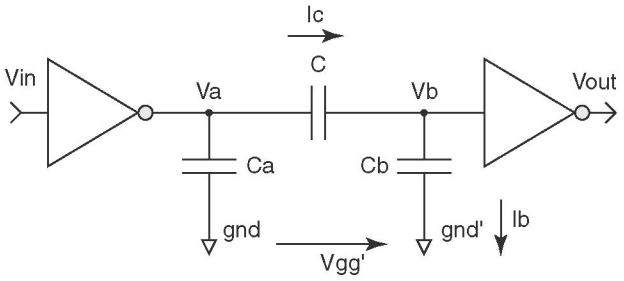

Fig. 3. Model of operation of a capacitively coupled isolation circuit.

Consider now an AC model of the capacitive coupling. V_{in} is a digital signal whose value is always between V_{dd} and 0 volts. Equivalently V_a, is the inverted voltage of V_{in}, and its is always between 0 and V_{dd} volts. The voltage V_b can be calculated by using equation 1.

$$V_b = V_a \frac{C}{C + C_b} \tag{1}$$

As can be seen from the capacitive divider in equation 1, the capacitance C must be much larger than the parasitic C_b for proper operation. If equation 1 is not satisfied, the transmitted signal amplitude is going to be smaller than V_{dd} and errors will occur at the receiver.

Let us consider the charge at nodes V_b and across the isolation capacitance C: $Q_b = C_b V_b$ and $Q_c = C(V_a - V_b)$. The maximum charge at V_b is $C_b V_{dd}$ and the minimum is $0V$. The maximum charge across C is $C(V_{dd} + 2V_{th})$ and the minimum is $0V$. This assumes that the node V_b is protected by two diodes connected to the power supplies and with threshold V_{th}.

To assess whether the capacitive link is functional, we need to see if a swing of V_a can change the state of V_b (charge it by $\pm V_{dd}$). As an example, consider the case when $V_b = -V_{th}$ and V_a switching from $0V$ to V_{dd}. We obtain that the initial charge $Q_{bi} = -C_b V_{th}$ and the initial charge across C is: $Q_{ci} = CV_{th}$. The final value of the charge across the isolation capacitance

is therefore $Q_{cf} = C(V_{dd} + V_{th})$. As a result, the final charge at node V_b is $Q_{bf} = -C_b V_{th} + C(V_{dd} + V_{th})$. If we choose $C \gg C_b$ then the voltage $V_b \geq V_{dd}$, limited by the protection diodes. Thus operation requires that $C \gg C_b$.

B. Minimum Slew-Rate:

When employing capacitive isolation, the input voltage swings is the desired signal to be detected, while ground bounce swings have to be rejected. Let us consider the currents across the isolation capacitor C. The current i_c is expressed by equation 2.

$$i_c = C\frac{dV_a}{dt} - C\frac{dV_b}{dt} \tag{2}$$

Using the results in [10], we can write equation 3.

$$i_b = C_b\frac{dV_{gb}}{dt} - C_b\frac{dV_{gg'}}{dt} \tag{3}$$

With V_{gb} being the voltage between node b and the input ground ($iGnd$). The first term on the right hand side of equation 3 is due to V_a or the input signal. The second term is the interference or noise due to ground bounce. We conclude that, for correct device operation, equation 4 has to be satisfied.

$$\frac{dV_a}{dt} \gg \frac{dV_{gg'}}{dt} \tag{4}$$

This imposes a constraint on the minimum signal slew rate. The prototype in this paper satisfies this condition using digital modulation of the input signal. Since the modulating signal is much faster than the input signal, the input slew-rate is effectively masked. As an example consider the case of $(dV_a/dt)_{min}$. This value must be bigger than $(dV_{gg'}/dt)_{max}$. With a power supply of 3V and a 200MHz modulating clock, the value of $(dV_a/dt)_{min}$ is approximately 3 x 10^8V/s. While the expected grounds slew rate $(dV_{gg'}/dt)_{max}$ is about 1 x 10^6V/s. These values satisfy equation 4.

IV. Results and Measurements

We simulated the isolation buffer *isoCap3* at the design corners for temperature, and transistors characteristics. We simulated with a temperature range of [-55C, +125C] for typical, fast and slow transistors. We conducted the measurements at 25Mbps. The circuit performed correctly in all settings. We also tested the circuits with a power supply of 3.3V $\pm$10% of the nominal value at 40Mbps. In both cases the circuit was operational. All simulations have been conducted with all 4 inputs tied together and the output connected to a 25pF capacitance, corresponding to a worse case scenario for the power consumption.

The measured supply current of 4 channels in parallel was 1.5mA at low data rates and 3.3V power supply. This consumption is attributed to the ring oscillator operating at the receiver's side and generating the global modulation clock. The consumption rose to 4mA with a 10MHz input and 16mA with a 40MHz input. The majority of the power consumption was due to the output drivers, designed to drive capacitances

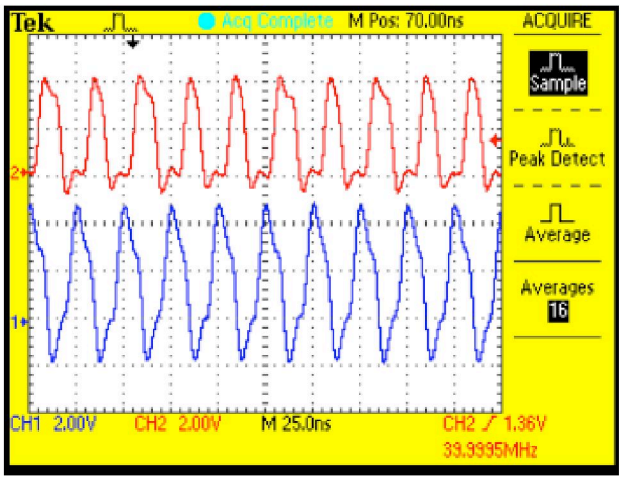

Fig. 4. Isolation channel input (top trace) and output (bottom) operating at 40MHz.

of up to 25pF. A plot of the measured power consumption using 4 channels in parallel is given in Figure 5.

No crosstalk between channels was observed. All these measurement were conducted with the isolation chip driving 2ft of coaxial cable and a 25pF load (oscilloscope load). Figure 4 shows the output of one isolation channel (bottom trace) when driven with a 40MHz input (top trace).

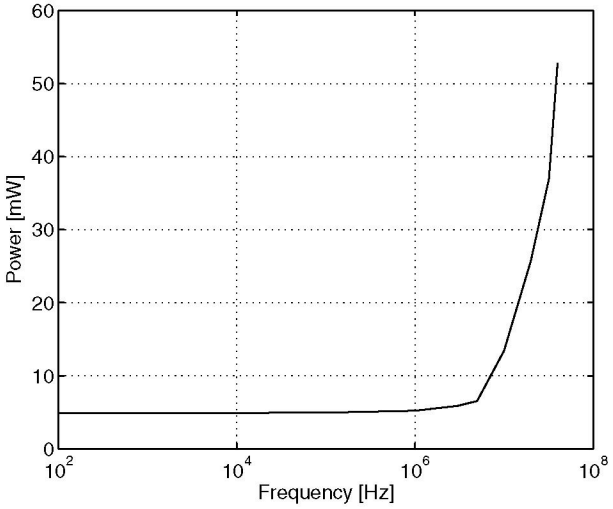

Fig. 5. Power consumption of the isolation amplifier versus input frequency. The device was operated with four channels in parallel driven by the same input.

Operation while providing isolation was verified experimentally, with the circuit operating with an input square wave of 30MHz, $Vddo$ = 3.3V and $V_{Gndo-Gndi}$ = 25V. Figure 6 illustrates the isolation property of two SOS metal layers. Specifications for the device described in this chapter were a ground to ground isolation of up to 100V. We measured the isolation of the amplifier up to 110V with a Keithley unit 236 and measured no significant current (Figure 6), as

evidence that the isolation in the SOS die is conforming to the specifications. The actual *measured* breakdown of the device occurred in the proximity of 820V between the grounds of input and output circuits. This isolation is guaranteed by the 3.6μm of separation from the metal-1 and metal-3 capacitance plates. The breakdown measurements were conducted using an electrophoresis equipment FisherBiotech FB400.

A picture of the fabricated SOS isolator amplifier is given in Figure 7. The die has 12 bonding pads: the left six are (top to bottom) the input supply, four data inputs and the transmitter's ground; the right six are the output supply, four data outputs and the receiver's ground.

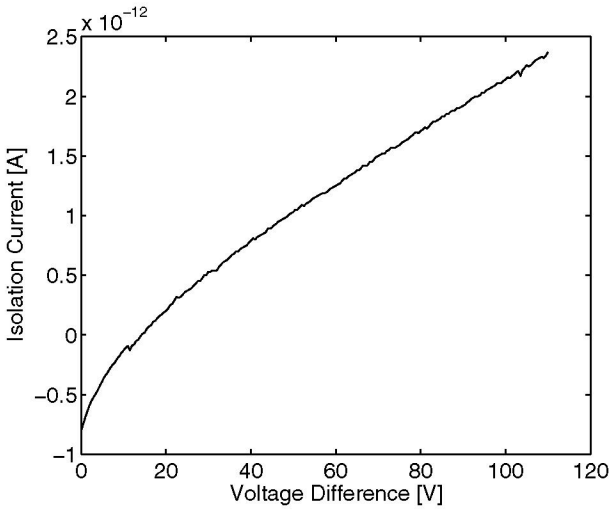

Fig. 6. Isolation performance between metal-1 and metal-3 in the SOS process.

Finally we report that each channel *isoCap3sc* uses 230 x 60μm^2 of silicon area, as opposed to the 230 x 140μm^2 used in our first implementation [9], [10]. Taking into account that one channel *isoCap3sc* is used to transmit the global clock from receiver to transmitter, the four channel device presented in this paper uses approximately 1/2 of the silicon area of our previous devices.

V. Summary

We designed and fabricated a 4-channels digital isolation amplifier in a 0.5μm silicon-on-sapphire technology. The isolation properties of the sapphire substrate allow to integrate this isolation amplifier in a single die. Modulation of the input signal is used to increase immunity to errors at low input data rates. The individual isolation channels operate in excess of 40Mbps using a differential transmission scheme. We have shown the ability of the device to tolerate ground bounces of 1V/μs and isolate more than 800V. Compared to our previous design we reduced the silicon area by half and eliminated BER at low input frequencies.

VI. Acknowledgements

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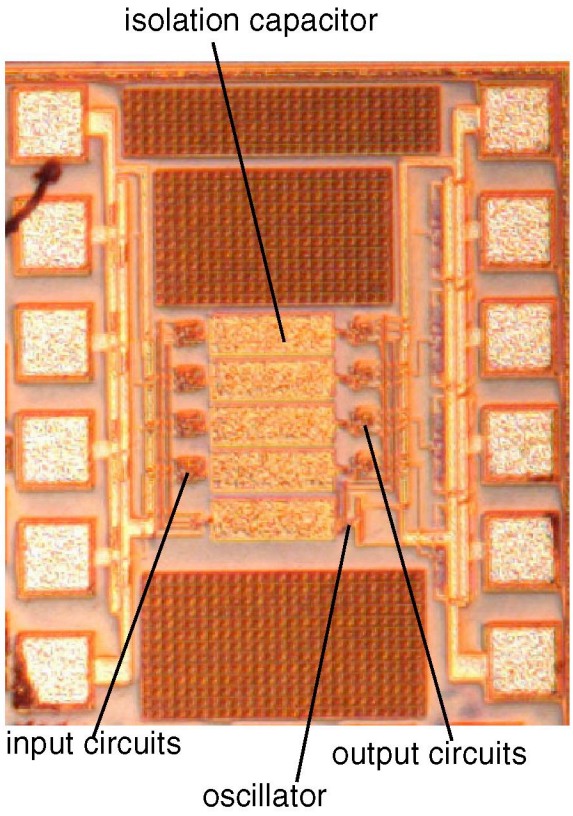

Fig. 7. Micrograph of the fabricated SOS isolation amplifier.

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