SECOND GENERATION OF HIGH DYNAMIC RANGE, ARBITRATED DIGITAL IMAGER

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ABSTRACT

A second generation 80 x 60 pixels arbitrated address-event imager has been designed and fabricated in a 0.6μm CMOS process. Its pixel has been improved for image quality, power consumption and dynamic range. The improved pixel dynamic range is 203dB. The array has a dynamic range of 119dB. The power consumption is 1.7mW in uniform indoor light and a mean event rate of 142Kevents/s (2.8K effective fps). The imager is capable of updating its images 10.4K times/s.

1. INTRODUCTION

The first generation of arbitrated address-event image sensor [1] while providing higher dynamic range and faster frame rates than APS based CMOS image sensor [3,4,5,6], was deficient in terms of image quality. Improvements on the image quality require careful pixel design and minimization of fixed and dynamic noise sources. We analyzed the first generation of event-based sensors [1] with the intent to reduce fixed pattern noise (FPN) on the sensor, one of the main causes of noise in the image.

A second generation 80 x 60 (1/8 VGA) fully arbitrated Address-Event Representation (AER) imager has been fabricated in a 0.6μm CMOS process. Enhancements of many of the pixel analog components and a theoretical study of the sources of FPN are provided in this article.

Section 2 provides an overview of the new address-event digital pixel used in this second generation sensor, as compared the first generation's pixel. Section 3 describes a theoretical framework for motivating additional improvements on the pixel. Section 4 shows the data collected with the image sensor and quantifies its performance. Section 5 is a summary of the sensor specifications.

2. IMPROVING THE PIXEL

The pixel transistor count of the first generations of Address-Event event generator or pixel can be reduced after careful inspection. In Figure 1 is reported a schematic caption of the first generation pixel. The first two stages of the pixel's AE digital circuitry are two digital inverters in series. Usually an even number of inverters can be removed, but in this case the second inverter is connected to an additional PMOS transistor (see Figure 1). This transistor is needed to prevent race conditions. In case an acknowledge signal (*Ack*) is still pending (is still *high*), the PMOS would impede the propagation of a new event.

In order to remove the two series inverter we therefore had to combine the function of this PMOS transistor into the analog portion of the pixel. This was accomplished by moving the PMOS transistor between the feedback inverter in the analog portion and its power supply (Figure 2). The effect of the PMOS is identical to the original first generation pixel, where it would impede new events from propagating to a request (*~Req*) if the acknowledge signal *Ack* has not been previously reset to the initial *low* state.

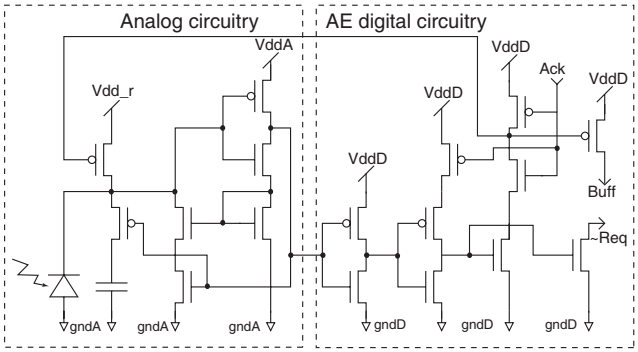

Figure 1: First generation pixel schematic

The second generation improved pixel, designed to eliminate the redundant series of digital inverters in the digital circuitry, is portrayed in Figure 2. This pixel features a smaller footprint, for a reduction to approximately ¾ of the original size. The space once occupied by the removed couple of inverters can be used to improve on sensitive analog components in the array, to improve the performance of the pixel in image quality and photo-transduction.

The second generation imager was designed to improve on image quality, therefore we chose to accommodate better analog components in the new version of the pixel, instead of reducing its size. This also allowed to reuse the same boundary Address-Event circuitry of the first generation of arbitrated digital image sensor, saving time to synthesize a new one.

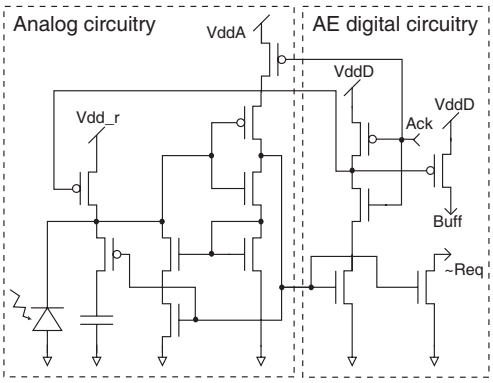

Figure 2: Improved second generation pixel schematic

3. PIXEL NOISE PERFORMANCE

The first generation of the bio-inspired digital image sensor with current feedback event generator suffered from a high degree of fixed pattern noise (FPN). The reduction of systematic noise sources was a main priority in the development of the second generation of imagers using temporal coding.

Size mismatch of the devices was attributed to be the main reason for mismatch between pixels. Thus the size of critical devices in the pixel was increased to mitigate the effect of mismatch. The photodiode area was increased by a factor of 2 and the integrating capacitor by a factor of 2.33. This ratio was chosen to reduce the firing rate at the output, one of the design specifications for the second generation imager. In fact a lower output event rate increases the dynamic range, since it decreases its lower bound. The integrating capacitor C and the photodiode shape were also kept strictly rectangular to minimize border effect on corners, a main source of mismatch.

Transistors Q_2 to Q_5 (Figure 3) were all increased in size to reduce mismatch. Transistor size was augmented by an average factor 1.5, keeping the pixel size the same (30 x 32μm). This was possible because of the use of stacked contacts available in the newer fabrication processes. Transistors Q_2 and Q_3 relate to the spike threshold of the event generator. Transistor Q_4 and Q_5 create the current feedback that generates the event. It is therefore important to keep mismatch of these devices to a minimum to prevent generation of fixed pattern noise.

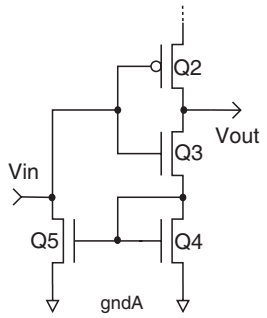

Figure 3: Analog portion of the event generating pixel

Let us now examine in detail a model of FPN noise in the pixel. Given a constant light, both in time and space, mismatch in pixel light integration and spike generation occurs for two main reasons.

First the slope of the capacitor voltage versus time varies with the amount of photocurrent I_{ph} and the integrating capacitor effective size C. Secondarily the threshold of the event generator $V_{in,sw}$ is also a variable and thus produces modulation of the integration time. Both these phenomena are represented in Figure 4. Note that an event is generated when the slope reaches the threshold. In Figure 4 there are therefore 9 possible different times for 9 different events. Clearly in the real circuit the time it takes for different pixels to generate an event is a random process. We can assume that the process is *ergodic* and the events are Gaussian distributed in time. In this case we can measure a single frame and compute the FPN noise even when this is time dependent. We therefore assume that the statistics are not dependent on the initial conditions of the event generators or pixels.

The slope (Sl) mismatch is due to photocurrent I_{ph} or integrating capacitor C mismatch, since the slope is proportional to these quantities:

$$Sl \propto I_{ph} \frac{1}{C}$$

Mismatch in size of the area of the photodiode or the area of the MOS capacitor that constitute C can both generate differences in the slope amongst pixels. A measure of the relative standard deviation of the slope Sl is given by:

$$\frac{\Delta Sl}{Sl} = \sqrt{\left(\frac{\Delta I_{ph}}{I_{ph}}\right)^2 + \left(\frac{\Delta C}{C}\right)^2}$$

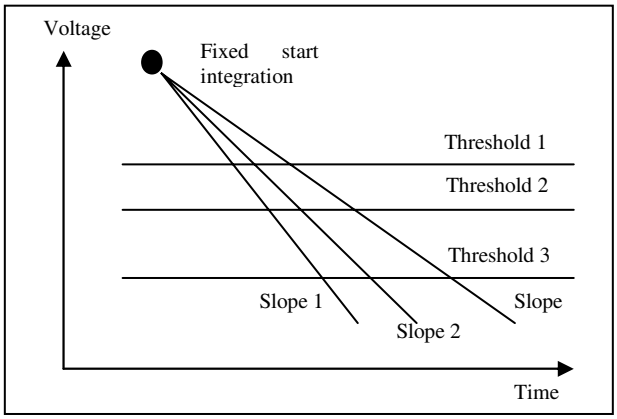

Figure 4: Mismatch in a current feedback event generator

Because the size of the transistor influences the MOS capacitance as well, we can use the results from the literature [2] relating output current mismatch of a transistor array for assessing the above quantity. In fact both the MOS gate capacitance C and the photocurrent I_{ph} are directly proportional to the transistor/photodiode area. And since the mismatch coefficient β relates directly to the same length and width of the transistor that correspond to its area, then we can express:

$$\frac{\Delta Sl}{Sl} = \sqrt{2}\frac{\Delta\beta}{\beta}$$

The literature [2] gives mismatch result in parameter β (0.75% for 10 x 4μm transistors – approximately the same size as the photodiode and integrating capacitor) for a similar process to the one used for fabrication of the retina chip. The relative standard deviation of the mismatch in slope Sl can therefore be calculated to be approximately 1.3%.

A mismatch calculation of the switching threshold of the event generator instead is calculated by assessing the propagation of error of the threshold point $V_{in,sw}$:

$$V_{in,sw} = \frac{nkT}{q}\ln\left(\frac{I_{ph}}{\left(\frac{W}{L}\right)_{Q4}\left(\frac{L}{W}\right)_{Q5}\left(\frac{W}{L}\right)_{Q2} I_{Q2}}\right)$$

By using a Taylor expansion of the natural logarithm function, the standard deviation of the error due to mismatch is:

$$\Delta V_{in,sw} = \sqrt{\left(\frac{\Delta I_{ph}}{I_{ph}}\right)^2 + \left(\frac{\Delta\beta}{\beta}\right)^2_{Q4} + \left(\frac{\Delta\beta}{\beta}\right)^2_{Q5} + 2\left(\frac{\Delta\beta}{\beta}\right)^2_{Q2}}$$

We can assess the standard deviation of the mismatch in $V_{in,sw}$ by using a similar methodology as used above for the calculation of the slope mismatch. In particular the mismatch of transistors Q_2, Q_4, Q_5 is 1.5% since their size is 2 x 2μm, while it is 0.75% for the photocurrent, since the transistor size is in this case 10 x 4μm. $\Delta V_{in,sw}$ thus results approximately 2.8%.

Note that adding the uncertainty in the slope and the event generator threshold, we obtain a value of 4.1%, very close to the value of 4% observed in the first generation of imager using temporal coding.

The measured FPN in the second generation image sensor is 1.4% in ambient light.

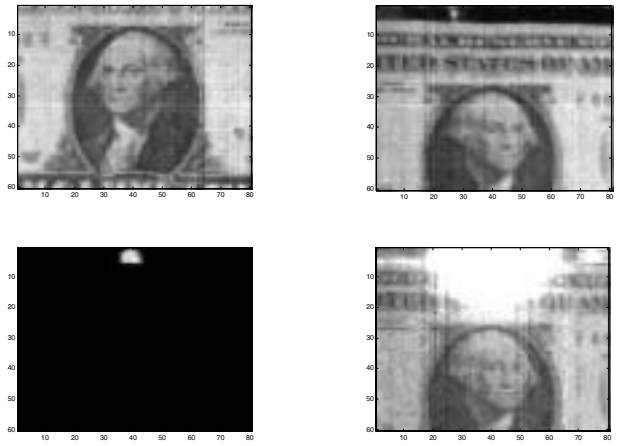

Figure 5: Sample images

4. RESULTS AND DISCUSSION

The image quality of the second generation of arbitrated address-event image sensor improved was improved by means of improving the FPN noise. A sample image is given in the upper left corner of Figure 5. The rest of the images of Figure 5 show an example of high dynamic range imaging using our digital sensor. The upper right picture show president Jackson with an off light source on the upper mid portion of the image. When the light source is turned on, the lower left image is obtained. Notice that the image saturated because of the bright light source. Performing the logarithm of the data in the histogram of this third image, we obtain the fourth image (lower-right)

in Figure 5. In this last image president Jackson is still visible despite the saturation of many pixels.

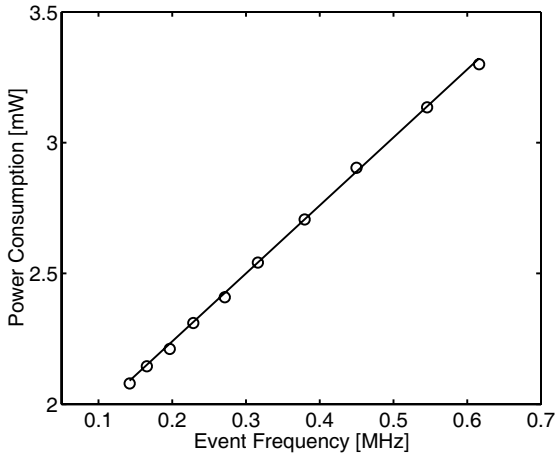

Figure 6: Power consumption versus event frequency

The measured dynamic range for an individual pixel is 203dB (70mHz–50MHz). Similarly, under uniform illumination, the array has a dynamic range of 119dB (340Hz–50MHz), supposing that a single pixel has access to the output bus.

Power consumption versus output event rate is reported in Figure 6. The data (circles) is modeled by the following mathematical relation:

$$\text{Power [mW]} = 1.72 + 2.60 \cdot f \text{ [Mhz]}$$

Power consumption was measured by targeting a bright spot of light on the image sensor and measuring the time needed to collect 1M events. The analog and digital power supply and the reset voltage *Vdd_r* are kept at 3.3V. The static dissipation is produced by the pseudo-CMOS logic used in this design.

Power consumption is clearly reduced by a factor of 3 or more than the previous generation of address-event digital image sensors [1]. In addition, the image sensor is capable of updating its image 10.4Ktimes/s. The performance of the imager is improved in all aspects when compared to the first generation [1], making it one of the most competitive in the literature [3,4,5,6].

5. SUMMARY

An 80 x 60 pixels fully arbitrated address-event imager was fabricated and tested. The imager provides a very large dynamic range of 119dB, a low power consumption of 1.7mW and is capable of 10.4K effective fps. Table I summarizes the characteristics of the array. The digital power usage can be further improved by removing all pseudo-MOS logic devices.

Technology	0.6µm 3M CMOS
Array Size	80 (H) x 60(V)
Pixel Size	32µm x 30µm
Fill Factor	7.5%
Dynamic Range	203dB (Pix.) 119dB (Array)
Bandwidth	70mHz – 50MHz (Pix.) 340Hz-50MHz (Array)
Sensitivity [Hz/mW/cm^2]	2x10^6 (Array) 42 (Pix.)
FPN (STD/Mean pixel-pixel)	1.4% @ 0.1 mW/cm^2
Max. FPS	10.4K (effective)
Power Consumption [mW]	1.72 + 2.60·f [Mhz]

Table I: Summary of chip characteristics.

6. ACKNOWLEDGEMENTS

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7. REFERENCES

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