AN 8-BIT, 1MW SUCCESSIVE APPROXIMATION ADC IN SOI CMOS

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ABSTRACT

A low-power 8-bit successive approximation Analog to Digital Converter (ADC) was designed and fabricated in a 0.5μm Silicon on Sapphire CMOS technology. The ADC is capable of 32MHz operation, producing 1.23MS/s, consuming 1.5mW at 3.3V supply. It uses an active area of 450x315μm^2 and 916x790μm^2 including output pads. The acceptable input swing is 2.1V at 3.3V supply. The ADC is a mixed mode analog-digital circuitry performing algorithmic conversion of an analog input voltage into an 8-bit binary code. The lack of parasitics in the Silicon on Sapphire fabrication process simplifies the design of analog to digital converters. The circuit design is freed from the unaccounted bulk capacitances which generate feedback and corrupt the performance of the ADC at high frequency.

1. INTRODUCTION

Successive approximation analog to digital converters have the advantage of using low power, having a small footprint, and being able to report high resolutions [2, 3, 4]. We designed and fabricated a 8-bit Successive Approximation Register (SAR) analog to digital converter (ADC) in a 0.5μm Silicon on Sapphire (SOS) CMOS technology. The proposed ADC was targeted for low-power applications and average conversion performance needed in data acquisition, systems on a chip, embedded systems and vision systems employing column parallel architecture.

The ADC is a mixed mode analog-digital circuit performing algorithmic conversion of an analog input voltage into an 8-bit binary code. Conversion is performed by recursively comparing a stored reconstructed voltage to the sampled input, until the desired precision is met [5].

The absence of parasitics in the Silicon on Sapphire CMOS fabrication process simplifies the design of analog to digital converters. The circuit design is in fact freed from the unaccounted bulk CMOS capacitances that generate feedback and corrupt the performance of the ADC at high frequency [6]. The design of interconnects and top metal layers, on the other hand, assumes higher importance in the design of the ADC. In fact while the substrate capacitances are greatly minimized, interconnections and line-crosstalk are the critical point in the Silicon on Sapphire process.

In addition, passive components, the main source of mismatch in algorithmic converters, can be fabricated in Silicon on Sapphire with high precision and without the additional uncertainty value of the bulk CMOS passive capacitances.

Section 2 will provide a description of the ADC components and circuits. Section 3 reports measurements and performance of the described ADC architecture.

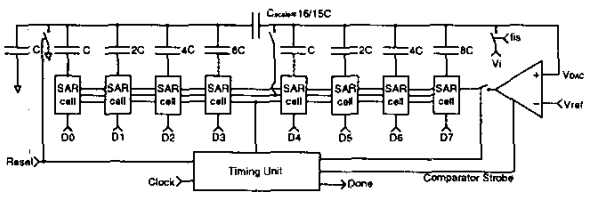

Figure 1: Split Capacitive Array and Successive Approximation Register

2. SUCCESSIVE APPROXIMATION REGISTER

2.1. Conversion Algorithm

The successive approximation register is a classic CMOS mixed mode analog-digital circuit that is capable of performing analog to digital conversion as well as digital to analog conversion internally. This characteristic is of great importance for understanding its working principle.

Figure 1 illustrates a schematic caption of the ADC system. An array of capacitive elements is used in the analog to digital converter to perform the algorithmic conversion. The capacitor array is a digital to analog converter. The ADC performs a binary search over all possible quantization steps to converge on the final digital output value. This is done by adjusting the capacitor voltage with successive approximation. Successive approximations are a series of capacitive charging, comparing the value with the input and updating the output register (SAR cells in figure 1) [1, 5].

A conversion begins with a global reset that discharges all the capacitors in the array (*reset* signal in figure 2). Capacitor plates are connected to ground during the reset phase. In addition all the bits in the SAR cells are reset to a zero value. The input signal V_i is then sampled by strobing the signal *fis*. Notice that the signal is sampled on the MSB bank for charge distribution of the capacitive network. At this point the capacitor array stores the input voltage V_i. The input signal must be smaller than the input reference voltage V_{ref}. The algorithmic conversion begins by adding $V_{ref}/2$ to V_i and comparing the value to V_{ref}. If the value is larger, the corresponding capacitor is reset and its register cleared. If the value is smaller, the MSB will be set to a logical one. The second most significant bit is then tested. Now a voltage of *Vref/4* is added to the capacitor array and the value compared. The algorithm follows as described above for all the remaining bits. The voltage on the upper plates of the capacitor array slowly converges to the input value V_i, until the desired precision is reached.

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$$V_{DAC} = \sum_{k=0}^{N-1} D_k 2^{k-N} V_{ref} \quad (1)$$

The above equation gives a value of the V_{DAC} (see figure 1) voltage at the internal input node of the capacitor array. This value is compared with the reference voltage V_{ref} at each iteration. D_k is the digital output value of the $k-$th SAR cells [5].

2.2. Capacitive ladder and Charge Scaling

The basic structure of the analog to digital converter is a capacitive ladder. The capacitive ladder implements a charge scaling digital to analog converter, which algorithmically minimizes the error between its output voltage and the analog input to be converted. This is a very popular architecture in CMOS technology. $N+1$ weighted capacitors, where N is the number of bits of the ADC (here 8), are switched on or off to generate an output voltage v_{out}.v_{out} is a function of the voltage division between the capacitors. The total capacitance of the SAR is $2^N C$, where C is the minimum capacitance used for the least significant bit. Given the high chip area and power consumption derived by using large capacitance, suggested the use of 'split capacitive array' (SCA) architecture. SCA provides a good tradeoff between capacitors size and accuracy, especially when taking advantage of the ideality of the Silicon on Sapphire substrate, which greatly reduces crosstalk and spurious bulk capacitances that would limit the precision of the ADC. Figure 1 shows a pictorial representation of the SCA architecture.

The figure represents the two sides of the capacitors array, connected by a scaling capacitor C_{scale} of value:

$$C_{scale} = \frac{1 + \sum LSB\ capacitors}{\sum MSB\ capacitors} \quad (2)$$

For obtaining 8-bit precision C_{scale} results: 16/15C [5].

Figure 2 represents a successive approximation register cell [1]. The cell is responsible for charging and discharging the capacitors in the array and for storing the digital code for each bit of the ADC. Comparator Flag (*CF*) allows the comparator to set the value of the bit after comparing the capacitor array voltage to the input voltage. Bit Select (*BS*) line activates only active bit per conversion step. *BS* is set by the timing logic circuitry. CS signal selects the bits for readout on the Bit Out line *BO*. The *Reset* signal stores a zero value at the beginning of the conversion and also discharges the capacitor. *Cap* line is connected to the capacitor in the array belonging to the SAR cell. This line sets and resets the capacitor value at the beginning of conversion or after a comparator decision.

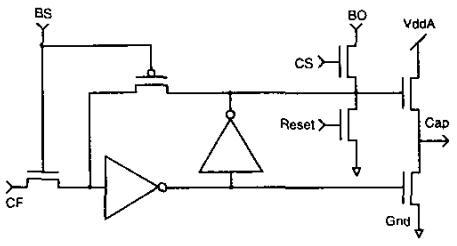

Figure 2: Successive Approximation Register cell

2.3. Comparator

The comparator is a critical component of the ADC since not only it has to provide accuracy of comparison better than $^1/_2$LSB, but it also has to compare with very high speed if high sampling rates are desired.

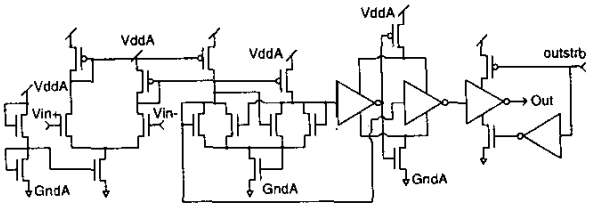

Figure 3: Fast comparator circuit

The comparator uses an active load configuration with fast decision circuit. The decision circuit is a mixed mode circuit that switches the decision *Out* signal fast. SOS simulation showed switching time on the order of a nanosecond. The decision circuit is a cross coupled pull-down network with positive feedback. Using a couple of sized transistors, one as diode load and one as pull-down, it is capable of amplifying input voltage differences smaller than $^1/_2$LSB and output a digital signal (*Out*). The output of the comparator is a self biasing differential amplifier [5].

The digital output signal is strobed using the *outstrb* line (comparator strobe in figure 1), which activates the output only when a comparison is in process. At all the other times, the output line is left floating and the bit line of the activated SAR cell is not overwritten.

3. EXPERIMENTAL RESULTS

The analog to digital converter is the first fabricated on a 0.5μm commercially available Silicon on Sapphire (SOS) (V_{tn} = 0.7V, V_{tp} = -0.8V) offered by MOSIS. The process features 3 metal layers, including a metal-thick layer for high quality passive capacitors, as well as a single polysilicon layer.

The design of the ADC was simplified by using this process. The time-consuming layout optimization in order to minimize substrate parasitic effects was not necessary in the SOS process. In addition, the layout area is minimized and compact. The ADC occupies an area of 450x315μm^2 and 916x790μm^2 with output pads. Figure 4 shows a micrograph of the fabricated chip. The minimum size capacitor for the array is 100.6fF and the total input capacitance at the conversion input is 3pF, excluding the pad capacitance. The ADC operates with a power supply of 3.3V nominally. The reference voltage V_{ref} was set to 2.7V throughout the testing.

The operational voltage can be decreased to 2.9V with unaccounted loss of precision. The power consumption of the chip is divided into analog and digital power supplies. The analog power supply provides currents for the charging and discharging of the capacitors, the DAC and the comparator. The digital power supply provides current to the digital logic, clocking logic and output buffers. The analog power supply uses 0.77mW over the operational range, 1kHz to 32MHz. Digital power consumption accounts for 0.79mW at 1kHz operation. The digital power consumption increases with the frequency because of the high capac-

itive load of the output buffers and pads. A numerical fit of the digital power consumption P_d is given by:

$$P_d = 0.78 + 1.2 \cdot 10^{-7} (f[Hz]) \quad [mW] \qquad (3)$$

This value, when related to the general formula $P_d = f_{clock} C_L V_{dd}^2$ at the described parameters gives a C_L = 11pF. This capacitance is an effective model of the dynamic power dissipation of the circuit at high frequency. Static power dissipation for the ADC is 1.55mW. Figure 8 shows a plot of both digital and analog power consumptions versus ADC clock operating frequency with a 3.3V supply.

Operational frequency of the ADC is 500Hz – 32MHz, which corresponds to a sampling frequency of 19S/s – 1.23MS/s since 26 clock ticks are necessary to complete a conversion.

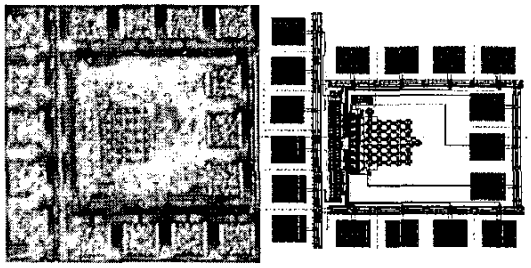

Figure 4: Die Photograph and Layout Caption

The 8-bit analog to digital converter performed with an average of 0.18 LSB Differential Non-Linearity (DNL) and a mean Integral Non-Linearity (INL) of 0.87 LSB. Figure 5 and figure 6 respectively report plots of DNL and INL as a function of the output digital code. This data was collected at a clock frequency of 1kHz, corresponding to a sampling frequency of 38S/s. At this rate the ADC presented 8 bits of resolution and 8 bits of accuracy. The number of bits was 7.92 bits for operational frequency of up to 3MHz (115kS/s), while decreased to 7 bits at a clock frequency of 10MHz (384kS/s). Figure 7 represents the number of bits as a function of the operational frequency of the ADC clock. At faster speeds the precision dropped significantly due to insufficient settling time for charging and discharging of the capacitor array as well as comparator settling time.

Total Harmonic Distortion (THD) was measured sampling a 2V peak-to-peak 1kHz sine wave with a 1.38MHz clock (53KS/s). A plot of the measured FFT spectrum for the sampled 1kHz waveform is given in figure 9. THD was measured to be -29.42dB. The Spurious Free Dynamic Range (SFDR) for the same input was measured to be 29.09dB.

The conversion input range was measured as 2.1V (0.2 – 2.3V) using a 3.3V supply with V_{ref} set to 2.7V.

4. SUMMARY

Advancements in process technology create opportunities for improving and optimizing existing architectures, especially with respect to better mixed-mode analog/digital circuits. An 8 bits analog to digital converter with digital to analog capability was designed and fabricated on a commercially available Silicon on Sapphire process. The ADC showed precision, accuracy and effective

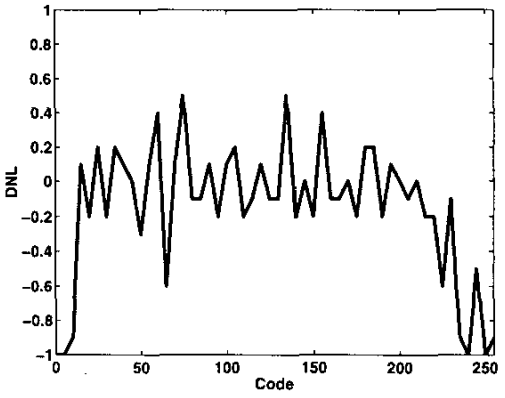

Figure 5: ADC Differential Non-Linearity at 1kHz

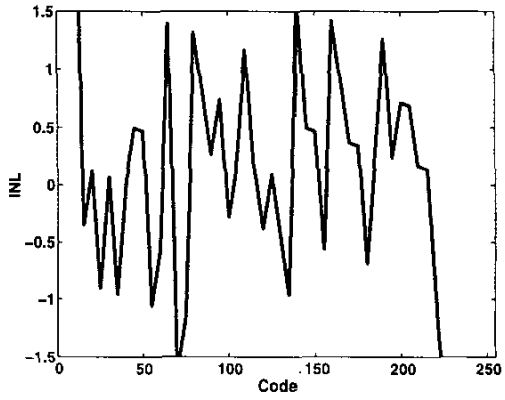

Figure 6: ADC Integral Non-Linearity at 1kHz

number of bits equal to 8 bits. It also provided conversion speeds over 1.23MS/s and low-power operation of 1.55mW. The circuit benefits from the process reduced crosstalk. The design is simplified and fast conversion and accuracy can be achieved without the need for internal compensation and complex circuit components. The authors believe the Silicon on Sapphire process is a very valuable process for the design of critical mixed-mode circuits for data converters and signal conditioning. Table I reports a summary of the performance of the analog to digital converter.

5. REFERENCES

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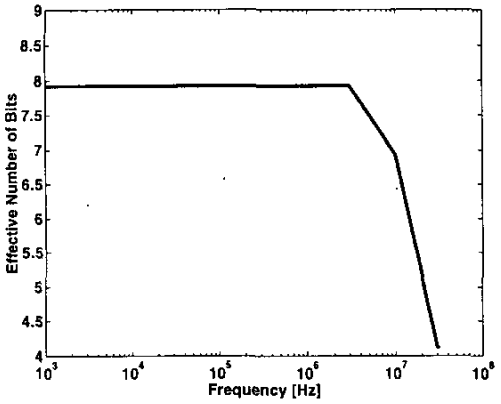

Figure 7: Number of Bits for Vin = 2.01V

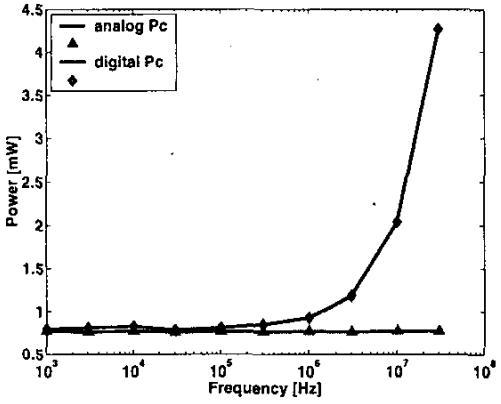

Figure 8: Power Consumption (P_c) of the ADC versus operational clock frequency

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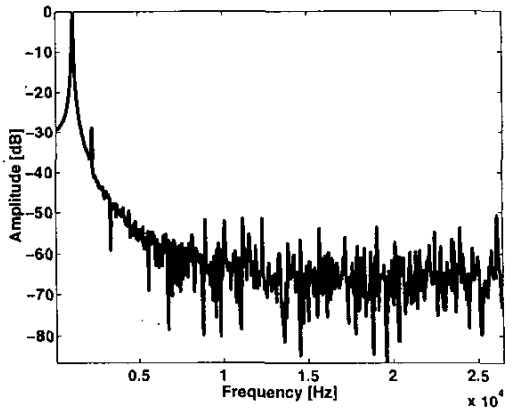

Figure 9: Measured FFT spectrum for a 1kHz sine waveform (2Vpp) sampled at 53KS/s

Supply Voltage	3.3V
Digital Power	0.79mW @ 1KHz 0.78 + 1.210-7f(f[Hz]) [mW]
Analog Power	0.77mW
Technology	0.5mm SOS (Vtn = 0.7V, Vtp = -0.8V)
Operational Frequency	500Hz - 32MHz
Sampling Rate	19S/s - 1.23MS/s
Resolution	8 bits
Active Area	450x315mm2, 916x790mm2 with pads
Input Range/Swing	2.1V (0.2 - 2.3V) on 3.3V supply
Unit Capacitor	100.6fF
Input Capacitance	3pF
DNL	0.18 LSB
INL	0.87 LSB
THD @ 1kHz	-31.48dB
SFDR @ 1kHz	31.65dB
Number of Bits @ 1kHz	7.92 bits (Vin = 2.01V)

Table 1: Measured ADC Performance