3D Integrated Sensors in Silicon-on-Sapphire CMOS

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***Abstract*— We fabricated a 3D-integrated multi-chip sensor and actuator and demonstrated the ability of communication with a floating die and no galvanic connection. The prototype was fabricated on a conventional 0.5μm Silicon-on-Sapphire (SOS) process. We designed a heater and a temperature sensor module with digital output based on a bandgap voltage reference. We used capacitive coupling to provide both intra-die communication of the digital temperature readings and also energy-harvesting by means of a charge pump. The non-galvanically interconnected prototype is an enabling technology for three-dimensional VLSI fabrication, 3D CMOS, wafer stacking and packaging.**

I. Introduction

Three-dimensional fabrication technologies are recently becoming more popular for advancing the integration density of current CMOS technology [1], [2]. The use of the third dimension to stack multiple dies is extremely attractive for the impact it would provide on the density and integration of sensory arrays, sensory computation and communication systems [3], [4]. Vision sensors are one example of a system that would significantly benefit from 3D VLSI technologies by combining low-power sensory arrays with high-density stacked and interconnected processing and communication layers [5], [2]. 3D VLSI has the potential of overcoming the density limitations of standard 2D VLSI processes. Sensing and processing modules are not restricted to a single die but can be connected across chip boundaries.

Capacitive coupling has been employed in multi-chip modules to transfer data signals between multiple dies [6], [7]. The coupling capacitors consist of two metal plates residing in separate dies and separated by a dielectric. The dies are aligned to form the coupling capacitance between the metal plates, which are generally bonding pads (refer to the bottom two dies in Figure 1). Capacitive coupling has been used successfully only to transfer signals [8], while still requiring electrical connections for both dies in order to provide the required power supply. These physical connection are generally obtained using ball-grid arrays, wire bonds or probes, all imposing mechanical and cost limitations on the number and density of data signal connections to the package.

We have recently demonstrated the feasibility of communication and power transfer in a multi-chip module that uses non-galvanic capacitive coupling to provide both bi-directional communication and also exchange power supply between two separate dies [9]. In this paper, we present a 3D integrated temperature actuator and sensor to demonstrate the performance and capabilities of our 3D systems and technology. The prototype was fabricated on a flavor of Silicon-on-Insulator (SOI) process: a 0.5μm Silicon-on-Sapphire (SOS) process.

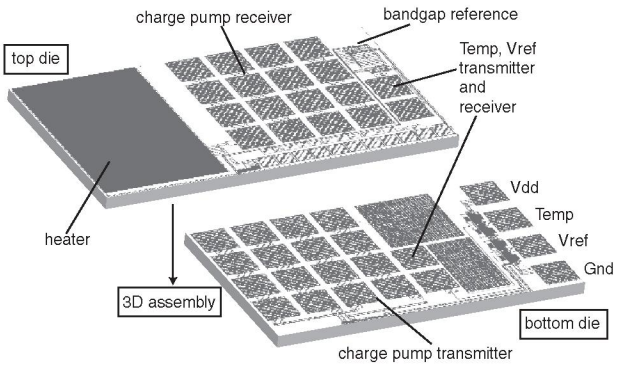

Fig. 1. Integration of the fabricated 3D integrated thermal actuator with digital temperature sensor. The bottom die transmits power to the top die. The top die contains a bandgap reference and two digital VCO converters. Notice that the die has no galvanic connection to the bottom die.

The advantage of our capacitive-coupling approach in SOS is its simplicity. Installation of a die in the package requires just an alignment of the die and the use of an adhesive. The alignment is unproblematic due to the transparency of the sapphire substrate. This is in contrast to the prevalent bump bond flip-chip techniques, where the yield of the multi-chip module is proportional to the number of bonds that have to be physically connected [10]. This technique can also be used to test dies before assembling them into a multi-chip module [10]. Capacitive coupling can provide high data throughput [8] while minimizing noise and parasitic inductance typical of wire-bonds. The reduction of the undesired inductance of the bonds can provide higher signal bandwidths, while the short interconnections by capacitive coupling reduce antenna effects and thermal noise. The combination of short interconnects and reduced parasitic capacitances relaxes the current requirements used by the interconnect's driver circuits, thus reducing the communication power consumption [11].

II. System Overview

In this paper we present a 3D integrated system capable of thermal actuation and digital temperature measurement using a bandgap reference. Figure 2 shows the organization of the prototype system. The bottom die transmits power to the top die using a four-stage Dickson charge pump and capacitive coupling [12]. The top die contains a bandgap reference and two digital VCO converters. These circuits convert a temperature dependent (*Vref*) and a temperature independent (*Temp*) signal from the bandgap reference into a square-wave digital signal. These two signals are communicated back to the bottom die again using capacitive coupling. Notice that the top die has no galvanic connection to the bottom die or the external world. Capacitive coupling and data and power allow the top die to be electrically *floating* [9].

The system contains a thermal heater implemented as a shunt silicon resistor of 100Ω between the power supplies of the top die. The heater shows the capabilities of the systems in actuation and is a fundamental components of chemicals and gas sensors. Having no direct galvanic connection to the power supply, the heater efficiency is much higher as no thermal loss occurs via the terminal's metal connections. The temperature measurement systems uses a VCO to converts the $Vref$ signal of the bandgap reference to the frequency of a digital square wave. An identical VCO is used to convert the reference signal $Temp$. These two signals can be used together to verify the functionality of the bandgap reference and also obtain a digital reading of the temperature of the top die.

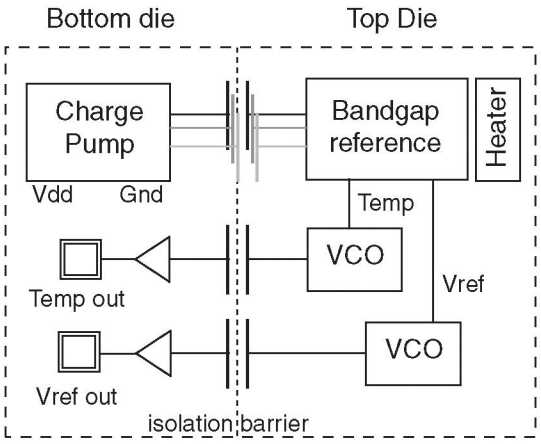

Fig. 2. System architecture.

Figure 1 shows the three-dimensional arrangement of the system. The bottom die couples with the bottom-facing top die by means of 18 bonding pads. The top die is flipped and aligned on top of the bottom die, so that the required capacitive connection are formed between the bonding pads metal plates of both dies. Sixteen pads are used to pump charge to the top die and supply current to its circuits. Two pads are used to communicate back the temperature and reference signals to the bottom die. The bottom die is placed and bonded into a common dual-in-line package. The alignment of the dies was performed manually under a microscope. The precision of the alignment was less than 10μm, and the dies have been bonded together using a layer of transparent varnish.

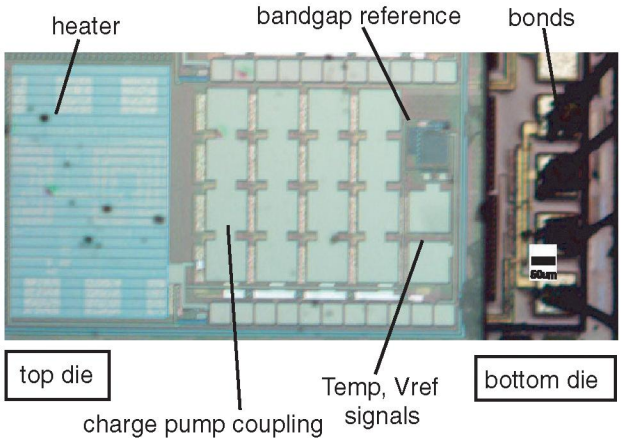

Fig. 3. Micrograph of the assembled multi chip module. The bottom die is bonded to a package through bonding wires visible on the right side of the figure. The top die, visible on the left side of the figure, is flipped so that its bonding pads are facing the bottom circuit's pads. This forms the capacitor for coupling the signal $(Temp, Vref)$ and power across the two dies (using a charge pump).

Figure 3 is a micrograph of the fabricated and assembled multi-chip module. The bottom die is bonded to a package through bonding wires visible on the right side of the figure. The top circuit, visible on the right side of the figure, is flipped so that its bonding pads are facing the bottom circuit's pads. This forms the capacitor for coupling the signal and power across the two dies. The capacitive coupling in air is about 8fF, with a plates distance of 10μm (3+3μm for the bond to passivation step and an estimated 4μm for the varnish layer).

III. System Components

The core circuitry of the 3D system is a CMOS bandgap reference with a sub-1-V output and implemented on the top die. Figure 4 represents a schematic caption of the bandgap reference. The circuit takes advantage of the multi-threshold MOS devices available in the SOS process [13]. Low-threshold PMOS (PL) are used as current sources for the entire bandgap circuit. The PL MOSFETs are all identical with a W/L = 10/2, unless specified in Figure 4. Notice also that the input NMOS of the 5-transistor transconductance amplifier are also low-threshold (NL type). The NL input transistors allow the transconductor to operate at low voltages and provide high-gain. The diodes are the SOS process native devices of the PG-type. The right diode is obtained as 8 diodes in parallel (8x). The resistor are SOS native high-resistivity silicon strips of the SN-type and the capacitor is a MIM type. The output of the charge pump is a $Temp$ signal based on the voltage Vbe in figure 4 of approximately 700mV and a $Vref$ signal of approximately 950mV.

The charge pump is based on the Dickson [14] charge pump design and it is composed by four stages. An eleven stages ring oscillator at the transmitter side produces a 350MHz

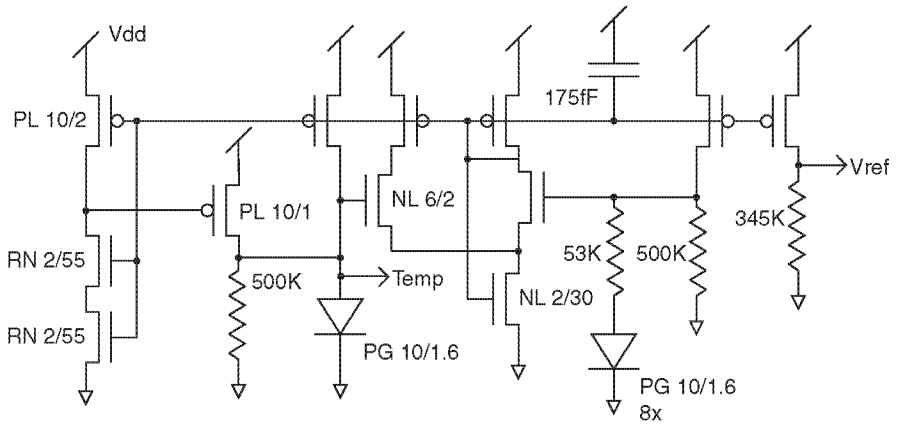

Fig. 4. Schematic caption of the circuit.

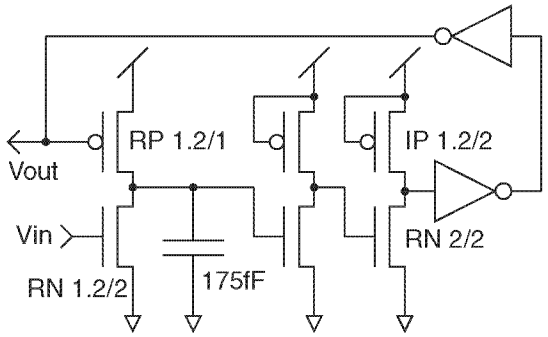

Fig. 5. Voltage controlled oscillator used to convert analog signal into a digital clock with varying frequency.

digital clock signal that controls the pump. The output of the oscillator is buffered to drive the isolation capacitances. The Dickson charge pump operates by pumping charge to the top die [12], [9]. The 16 coupling capacitors are organized to pump during the two phases of the clock cycles, in groups of 8 capacitors per phase.

The VCO circuit is presented in Figure 5. The circuit is a self-reset asynchronous oscillator that converts an input voltage into the frequency of a square digital wave. The core of the oscillator is an integrator based on capacitor discharge. The input transistor converts an input voltage into a non-linear current that discharges the capacitor. When the capacitor is discharged, a feedback loop composed of four inverters provides a delayed reset signal to restart the integration. Notice that we take advantage of the multiple threshold devices in the SOS process to design two of the inverters in the feedback loop. These self-biases inverters use a intrinsic transistor to self-bias. These first stages also provide a delay before communicating the reset signal to the integrator.

IV. Results

We measured the performance of the bandgap circuit by evaluating the temperature measurement capabilities and the stability of the output $Vref$ with a power supply of 2V. Figure 6 shows the dependance of signals $Temp$ and $Vref$ with temperature. The signal $Temp$ is derived from the Vbe voltage of the bandgap circuit and it is linearly and inversely proportional to temperature. The voltage $Vref$ was designed to be approximately 950mV. Notice that the $Vref$ signal is constant in the temperature range [20^{o}C, 80^{o}C] range. The $Vref$ ripple is approximately 6%, a very good result given the low reference voltage. Figure 7 represents the frequency of the square wave of signal $Temp$ as a function of temperature. This is the digital reading of the temperature. Notice the linearity of increase of the output frequency with temperature. A linear model of the frequency dependance predicts a conversion factor of 3.5kHz/^{o}C.

We successfully tested the functionality of the data communication and power transfer of the 3D integrated system. Figure 8 show screen frames from the oscilloscope verifying functionality of the prototype. The top and middle traces show the temperature digital signal $Temp$ obtained respectively with a 1V and 2V power supply and at a temperature of 25^{o}C. The bottom trace is the reference voltage $Vref$ signal with a 1V power supply. The current drawn was 2mA with a 3.3V supply and 1mA with a 1V supply.

V. Summary

We designed, fabricated and assembled a multi-chip sensor and actuation module that uses non-galvanic capacitive coupling to provide bi-directional communication and exchange power supply between two separate silicon-on-insulator dies. The prototype was fabricated on a conventional 0.5μm Silicon-on-Sapphire (SOS) process. We demonstrated that capacitive coupling is capable of transferring power to the receiver die, by employing a charge pump. We also show that communication can be achieved between the two dies by reading two digital signals coupled across the dies. One signal is the temperature reading of a thermometer circuit residing on the top die. A bandgap reference implements the temperature sensors and also provide a stable temperature-independent voltage that is also transmitted to the bottom die.

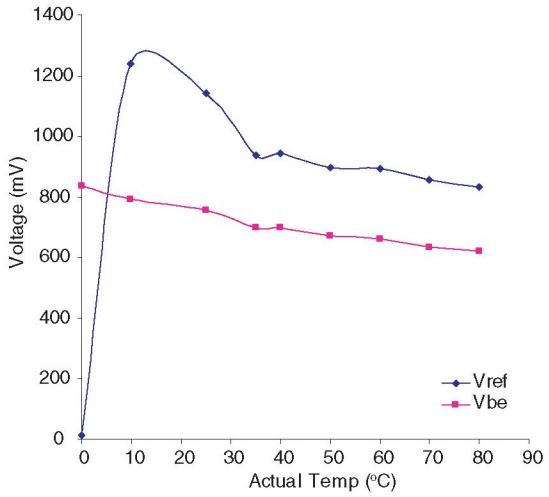

Fig. 6. Voltage reference output $Vref$ and $Temp$ as a function of the temperature.

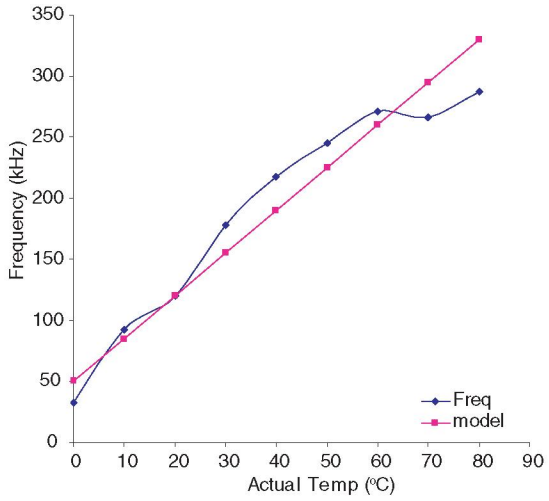

Fig. 7. Temp signal frequency versus temperature.

VI. Acknowledgements

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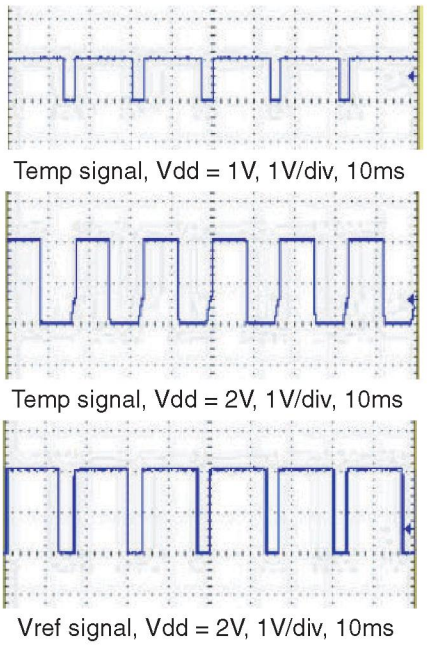

Fig. 8. Oscilloscope traces verifying functionality of the prototype. The top and middle traces show the temperature digital signal $Temp$ obtained respectively with a 1V and 2V power supply. The bottom trace is the reference voltage V_{ref} signal with a 1V power supply.

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