ALOHA CMOS IMAGER

Eugenio Culurciello and Andreas G. Andreou

Electrical & Computer Engineering, Johns Hopkins University, Baltimore Maryland 21218 USA

ABSTRACT

We report on a A 32 x 32 pixel CMOS imager with a digital pixel output fabricated in a 0.6μm CMOS process. The imager incorporates an embedded ALOHA MAC interface for unfettered self-timed pixel read-out in energy aware sensor network applications. Collision on the output is monitored using an analog contention detector. The imager has an unprecedented dynamic range of 240dB for an individual pixel with an array dynamic range of 180dB. The power consumption is 795μW for typical outdoor illumination conditions with a typical pixel mean event rate of 10K samples/s with frame rate updates of 4.88K frames/s.

1. INTRODUCTION

Synchronous quantization (data conversion), transmission, and processing of information are today common engineering practices. These practices have evolved in an era where system components were designed and optimized independently of each other but with a standard interface. This aids the rapid commercialization and adoption of new technologies: examples are the Universal Serial Bus, the Firewire and the NTSC video interface as standard interfaces for video technologies. However recent trends towards parallel and distributed processing in wireless sensor networks as well as high levels of system integration, necessitate the re-thinking of interfaces for sensor and sensory applications. The task in such networks is not necessarily the precise restitution of video or audio information but rather information extraction from an array of sensors. Often, computation and communication resources are shared by individual processor nodes.

In a distributed processing system, when there is a-priori knowledge that not all nodes are likely to require computation / communication resources at the same time, a fixed time-slot (synchronous) allocation of resources among all nodes is wasteful. If the demand for resources is bursty, computation / communication can be done asynchronously. Synchronous communication / computation as well as the additional complexity in the layered communication interfaces is also costly from a power dissipation perspective. This is the reason that a wealth of research is underway to develop new protocols for communication in wireless sensor networks that are energy aware [1]

In this paper we present a CMOS imager that incorporates an embedded ALOHA MAC digital interface for unfettered self-timed pixel read-out in energy aware sensor network applications. Collision on the output is monitored using an analog contention detector. The imager has an unprecedented dynamic range of 240dB for an individual pixel with an array dynamic range of 180dB. The available output bandwidth is allocated according to individual pixel demand.

Scanned image sensors [2, 3] use power very efficiently because externally driven, but do not make use of the available output bandwidth, since many pixels can be read before having integrated sufficient light. Arbitrated image sensors [4, 5] report excellent performance but with an overhead in terms of circuit components that results in a higher power budget. We thus propose to use the simplest access protocol, the ALOHA protocol [6], in conjunction with an efficient way to detect output bus contention. The marriage of these two techniques results in one of the lowest power, wide dynamic-range address-event image sensor reported in the literature. The power consumption is 795μW for typical outdoor illumination conditions with a typical pixel mean event rate of 10K samples/s with frame rate updates of 4.88K frames/s. The imager has a lower power budget with previously reported image sensor aimed at smart-dust networks [7] and remote smart sensors [8]. In addition it compares favorably to the lowest-power mass-produced digital image sensors as the Micron MT9C133 or the SMaL IM-001 models.

2. SYSTEM ARCHITECTURE

The proposed image sensor utilizes an event based digital representation of information originally proposed by Mahowald and Sivilotti [9, 10] and subsequently re-engineered by Boahen [4]. Several address-event image sensors have been reported in the literature [11, 12, 13, 5].

In the AER terminology, *events* are communication primitives sent from a sender to one or more receivers. For an image sensor, events are individual pixels reaching a threshold voltage and accessing the bus for communication with an outside receiver. An AER image sensor is composed of an array of pixels.

Representing intensity in the time domain allows each pixel to have large dynamic range [3, 14, 5, 15]. The integration time of each pixel varies in relation to the incident light intensity. Since the activity of the array is generated by the light intensity of the scene, and not an external scanning circuitry, the rate of collection of frames can be modulated by varying the *request-acknowledge* cycle time between the imager and the receiver circuitry. **Thus information can be extracted on demand from individual nodes in a wireless sensor network.**

3. DIGITAL PIXEL

The digital pixel employed in this design improves on the *integrate-and-fire pixel* [16] and on subsequent design [5]. The integrate-and-fire pixel operates by integrating the small photo currents on a capacitor, until the voltage exceeds a threshold. At that time, the pixel transmits an event at the periphery of the array. A disadvantage of this pixel is its high power consumption due to the input slew rate. If the input voltage changes slowly to external stimuli, it keeps the first amplification stage in the high-power regime, with large short-circuit currents and for a period of time equal to

the communication cycle time [5]. The new pixel used in this image sensor improves on the low power design [5] by eliminating two inverters in the digital circuitry. This improvement results in a even lower power consumption during event generation and in the silicon area used by individual pixels.

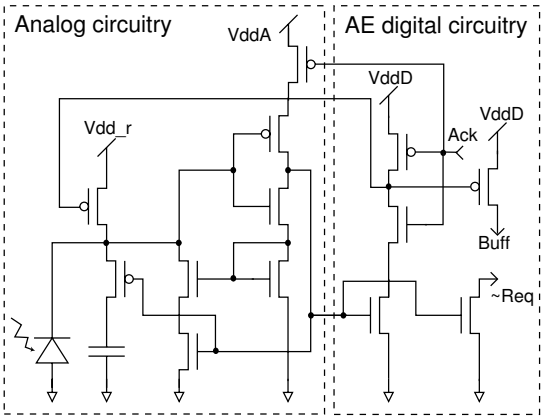

Fig. 1. Pixel Schematic

Active pixel or analog pixel sensor (APS) [17] have traditionally employed analog buffering and transmission of information from the pixel array to the periphery. In contrast digital pixel sensors (DPS) [18, 5] quantize the analog pixel value and provide data at the pixel level. Figure 1 shows the schematic of the pixel. It includes asynchronous circuitry that generates the address event request and resets the voltage on the capacitor when the request is acknowledged (AE digital circuitry). The operation of the pixel is divided into three main phases. First the light is converted into a current by the photodiode; this current discharges the integrating capacitor. The integrated voltage is then converted into a 1-b pixel request ($\sim$*Req*) signal and finally, after the communication cycle on the output bus, the pixel is acknowledged (*Ack*) and reset.

The photons collected by the n-type photodiode are integrated on a 120fF capacitor, resulting in a slew-rate of 0.083V/ms in typical indoor light conditions (0.1mW/cm^2). Because the slew-rate can be very small in presence of low lighting conditions, the comparator for generating the pixel request signal must have a fast switching time with low power consumption. The pixel uses an inverter with positive current feedback, shown in figure 1, to produce a digital pulse that activates the signal $\sim$*Req*. In analog pixel sensors most of the pixel's power consumption occurs during reset. To reduce reset power, the integration capacitor is disconnected from the comparator when a request is generated. The capacitor is then reset from $\sim$*(Vdd – Vtp)* to *Vdd* instead that from ground to *Vdd* [5].

The digital circuit that generates the pixel request and receives the acknowledge/reset signal is shown in the right part of figure 1. When the comparator is triggered, a row and column request ($\sim$*Req*) is generated to access the unfettered output bus.

No arbitration or external signal intervenes in the readout other than the receiver's *request* and *acknowledge* signals. The requesting pixel will immediately activate the row and column ROM that output its address on the bus. This output modality corresponds to a *row-column* organization. In other words the active pixel initiates communication on the output bus independently on both X and Y address buses. Row-column organization of the image sensor improves read-out speed by eliminating the large capacitance associated with the array common output bus lines. This capacitance is encountered when a request is performed within the whole array. Figure 2 shows the architecture of the row and column arbitration circuits in the unfettered ALOHA image sensor.

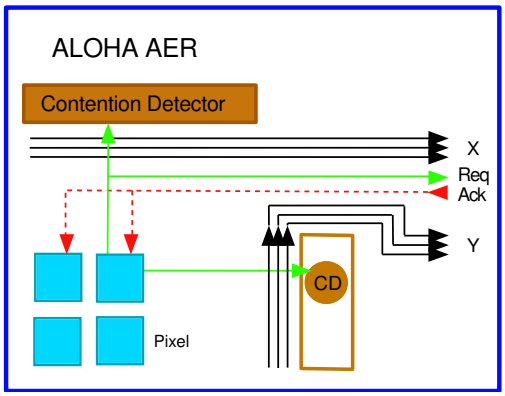

Fig. 2. Row and column ALOHA architecture

Data can be reconstructed in two possible ways; one is by counting events and reconstructing an histogram of the events in the array. Alternatively one can wait for two consecutive events for each pixel in the array and then compute the inter-event time between such two events [5]. An optional external timer can index each event and compare it with the last time an event at that pixel was recorded. The inter-event difference is inversely proportional to the light intensity. An external buffer must hold the latest pixel time index and the intensity value. Figure 3 shows example images recorded with the array and reconstructed using histogram normalization. Note that the quality of the images surpasses previous realization of address-event image sensors [19, 5].

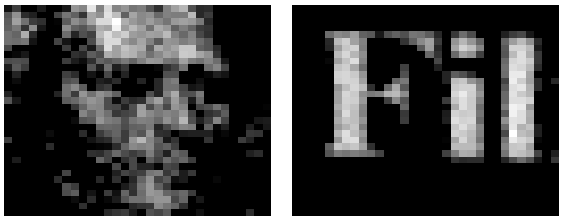

Fig. 3. Example images. President Jackson and text 'Fil'

3.1. CONTENTION DETECTOR

ALOHA is a simple and effective protocol for accessing a common bus from an array of sensory cells. On the other hand unfettered access can cause collision on the output bus, lowering the throughput [6]. The proposed image sensor employs a simple and effective way to detect contentions while multiple pixels access the channel at the same time. We use an analog circuit to detect multiple requests on the output bus control line, using the circuit in Figure 4, which is a modified multi-threshold digital NOR gate. The principle of operation is to size and bias the NOR circuit so that it

operates in analog mode. In a digital NOR every single one input being high will make the output commute to low. By creating two logic threshold in the NOR circuit, we can detect one or more input high. This is done sizing the transistors in the circuit so that if only one input is high, the output of the NOR will still be above the threshold of the following digital gates. If more that one input is high at a certain time, the output of the NOR will fall below the logic threshold and thus constitute a contention detection signal.

Referring to Figure 4, when a single pixel requests the bus with signal $e[a]$ the internal voltage of the contention detector *vcd* remains below the threshold of the following logic stages. As a second pixel request the bus before transmission of the previous one has been completed, signal $e[b]$ will bring *vcd* below the logic threshold and thus enable the output of the contention detector *cdout*.

Sizes of the realized contention detector circuit are: PMOS 95.4/2.4μm and pull-down NMOS 11.7/2.4 μm. An external bias (1V) to the PMOS pull-up transistor was provided.

The collision rate as a function of the event rate (also called *offered load*) is shown in figure 5, together with the theoretical limit. Data was collected by varying the uniform light intensity falling onto the image sensor. This corresponds to varying the event rate to the sensor. As a results of increasing the load, the collision rate increase as expected by the theory [6, 20, 21]. The collision rate data is higher than the theoretical limit because of the correlation between events due to the bursty read-out.

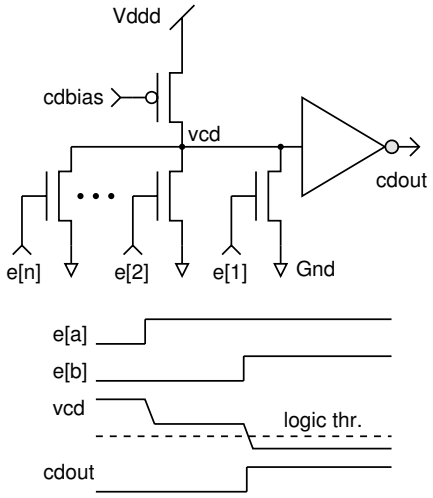

Fig. 4. Contention Detector circuit

4. RESULTS AND DISCUSSION

A die micrograph is reproduced in Figure 6. The sensor core size measures 1.2 x 1.2mm, excluded the pad frame. With the pad frame (21 pads) the image sensor occupies an area of 1.5 x 1.5mm. We measured the dynamic range of the image sensor by measuring the spike rate in the dark and with high illumination. In the dark the sensor produced a single event after 120s. The equivalent dark rate for a single pixel is thus 8.13μHz (since there are 32 x 32 pixels in the array). With very bright illumination, the image sensors minimum cycle time was 100ns, for a rate of 10MHz. Assuming a single pixel can fire at this rate if we focus light onto it, the measured dynamic range for an individual pixel is 240dB. Similarly, under uniform illumination, the array has a dynamic range of 180dB (8.33mHz – 10MHz). Table 6 summarizes the main characteristics of the array. The *sensitivity* is a cumulative performance metric of this image sensor [5]. Fixed pattern noise was measured in the dark as standard deviation to mean ratio of the array's histogram after collecting $100K$ samples. The maximum reported frame rate supposes the use of interevent-imaging technique [5].

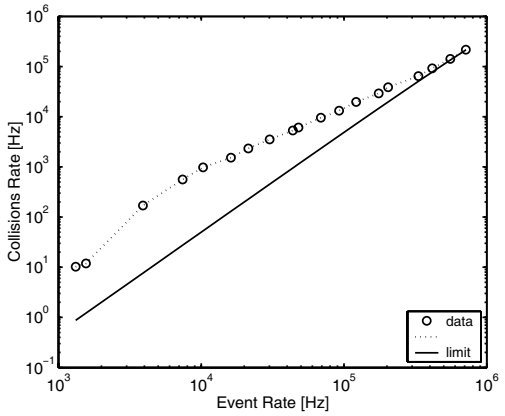

Fig. 5. Measured contention rate versus load and its ALOHA theoretical limit

With the rail voltage setting of: VddD = 3.3V, VddA = 3.3V, Vdd_r = 3.7V, the image quality and dynamic range was at its maximum. Power consumption of the image sensor in uniform room light ($\sim$0.1mW/cm^2) is 680μW for the analog supply and 115μW for the digital supply, at a rate of 10k events/s and cycle time of 350ns. This data was collected while imaging connected to a receiving computer. A great majority of the power dissipation is due to the pseudo-CMOS logic used in this design. The digital power consumption can be improved by removing all pseudo-MOS logic devices. At the maximum output event rate of 10MHz the sensor array provided an output aggregated address bandwidth of 110Mbits/s on the 5 X, 5 Y address lines and the request.

The image sensor is capable of updating its picture at a rate of 4.88K frames/s, and is one of the largest dynamic range [5, 2, 15], lowest power [3] and fastest [14] in the literature.

5. SUMMARY

We fabricated and tested a 32 x 32 pixels digital address-event imager with analog contention detection. The image sensor core size measures 1.2 x 1.2mm and provides a very large dynamic range of 240dB, a low power consumption of 795μW and is capable of updating its image at a rate of 4.88K frames/s.

6. ACKNOWLEDGEMENTS

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Performance Criteria, Resources Tradeoffs and Fundamental Limits, EIA-0130812.

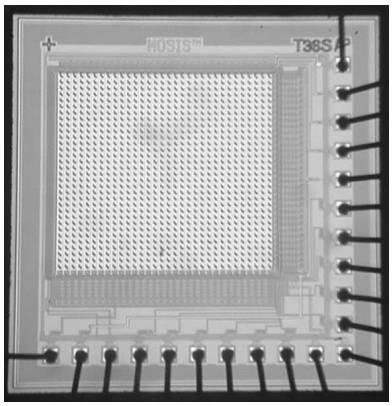

Fig. 6. Micrograph of the image sensor's die

Technology	0.6μm 3M CMOS
Array Size	32 x 32
Pixel Size	32.7μm x 29.7μm
Fill Factor	6.5%
Sensor Core Size	1.2 x 1.2mm
Bandwidth	8.13μHz - 10MHz (Pixel) 8.33mHz – 10MHz (Array)
Throughput	110Mbits/s (11bits)
Dynamic Range	241dB (Pixel) 181dB (Array)
Sensitivity [Hz/W/m^2]	1.7x10^3 (Array) 2.8 x10^9 (Pixel)
FPN	4.36% (dark)
Max. FPS	4.88K (effective)
Digital Power	115μW at 3.30V
Analog Power	680μW at 3.30V

Table 1. Summary of chip characteristics

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