Back-Illuminated Ultraviolet Image Sensor in Silicon-on-Sapphire

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Abstract— We present a back-illuminated 32 x 32 pixel SOI image sensor chip in 0.5- μ m silicon-on-sapphire process capable of ultraviolet imaging. The imager performs "snap-shot" image acquisition and analog readout at a continuous rate of a thousand frames/s and consumes as little as 650 μ W. Each pixel consists of a photodiode and a memory capacitor in 40 μ m x 40 μ m with a fill factor of 43%. The image sensor is suited for hyper-spectral imaging at high speeds.

I. INTRODUCTION

In recent years, silicon-on-insulator (SOI) circuits have been used for a variety of applications. Several groups have shown working photodetectors [1], [2]. However, there is no working sensor array in existence - only characterizations and simulations of full image arrays are available [3], [4], [5].

In this paper we present an image sensor array implemented in Peregrine Semiconductor's silicon-on-sapphire (SOS) technology [6]. As opposed to other SOI technologies, SOS features an insulating and transparent sapphire substrate that makes it ideal for optical applications.

The image sensor presented in this paper features the following innovations: (1) It is the first fully-functional array implemented in SOI/SOS technology, (2) it can be operated with back illumination, (3) the pixels feature a reflector that allows light to pass twice through the photodetector, (4) it was designed to be able to operate at 1000s of frames per second, (5) it is intrinsically radiation tolerant.

The sapphire substrate in SOS is optically transmissive from the UV (200 nm) to the infrared (5500 nm) spectrum [7], and makes this device favorable for hyper-spectral imaging in multiple bands with the use of back illumination. The back illumination also allows the pixels to have higher fill factors than traditional CMOS photodiodes because the metalization layer will not block the light. The tolerance to ionizing radiation makes this SOS image sensor suitable for outer-space instrumentation.

We engineered a fully-functional camera pictured in Figure 1 based on the SOS image sensor. The camera can be operated by any computer with an USB port.

The rest of the paper is organized as follows. In Section II, we describe the architecture and operation of the image sensor. In Section III, we describe the details of the complete camera system. In Section IV, we describe the test setup and chip characterization results including linearity, fixed pattern

noise, sample images, and power consumption. In Section V, we describe the results of imaging with a UV source.



Fig. 1. A camera designed for our SOS image sensor. The image sensor is mounted on a custom-built PCB with external components connected to the USB-based FPGA board.

II. SYSTEM OVERVIEW

The image sensor was designed in a 0.5- μ m silicon-on-sapphire process. The block diagram of the image sensor is shown in Figure 2. The array is composed of 32 x 32 pixels. A scan shift register is used to address individual pixels. A global operational amplifier is used as a buffer to convey the pixel integration voltages to the output.

The pixel is shown in Figure 3. The size of each pixel is $40 \mu m \times 40 \mu m$ with a fill factor of 43%. The capacitor is used as a memory element to store the integrated voltage. The *Read* signal connects/disconnects the photodiode from the rest of the pixel circuitry. SI and S2 signals connect the storage capacitor to the photodiode. The *Reset* signal shorts the capacitor, resetting the capacitor voltage to a pre-defined value (voltage at the *Bias* pin). *ColSel* is a signal from the scan shift register to connect the storage capacitor to the *Out* pin. The *Vdda* pin is set to 3.3V and *Out* is connected to the input pin of the global operational amplifier.

A normal pixel operation consists of three phases, as shown in Figure 4. First, the storage capacitor is reset to an initial value (voltage at the *Bias* pin) during the reset phase by setting the *Reset* pin to *VDD*, which shorts the storage capacitor. Then, during the integration phase, *Read* is set to *VDD*, connecting the photodiode to the rest of the pixel circuitry. *S1* is set to

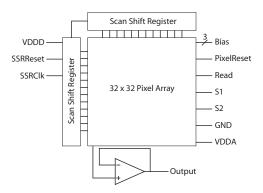


Fig. 2. Block diagram of the image sensor. The system is composed of a 32 x 32 photodiode array. The two scan shift registers are used to access the individual pixels. A global operational amplifier is used as a buffer to the output.

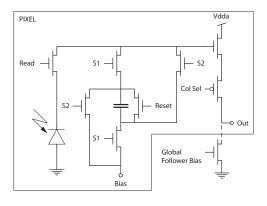


Fig. 3. Pixel schematic. The *Read* signal connects/disconnects the photodiode from the pixel. *Reset* switch shorts the storage capacitor to *Bias* voltage. *S1* and *S2* signals connect the capacitor to the photodiode and the output. *ColSel* is controlled by the scan shift registers to select the pixel.

VDD, S2 is set to GND, and Reset is set to GND, which connects the photodiode to the capacitor. The current from the photodiode discharges the capacitor as a function of the light intensity. Lastly, during the read out phase, Read is set to GND and the scan shift register sets ColSel to GND. This connects the storage capacitor to Out, which is connected to the global operational amplifier.

The S2 switch was designed to allow frame differencing on pixel. The first frame would be stored in the capacitor while S1 is set VDD and S2 to GND. Then, the second frame would be stored by setting S1 to GND and S2 to VDD. However, due to capacitive coupling between the capacitance of the photodetector and the storage capacitor during the switching, there is a voltage offset between the two frames related to light intensity and the frame subtraction feature cannot be used.

The image sensor performs a "snap-shot" image acquisition [8] because all the pixels are reset at the same time and integrate over the same interval before being read out. Unlike image sensors with rolling shutters [9], motion artifacts are not a problem for the image sensor.

The global operational amplifier in Figure 5 is connected in a feedback loop and has a gain of 1. The primary purpose of

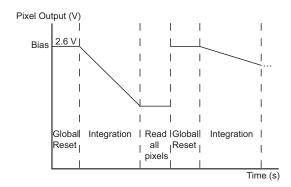


Fig. 4. The three phases during a normal operation of the pixel. (1) During Reset, the storage capacitor is set to the voltage at the *Bias* pin. (2) During Integration, *S1* is set to *VDD* and *S2* is set to *GND*, which discharges the storage capacitor relative to the light intensity at the photodiode. (3) During Read, the diode is disconnected by setting the *Read* signal to *GND* and the capacitor stops discharging. This process is repeated for video streams.

the operational amplifier is to act as a voltage buffer between the output of the pixel and the rest of the system circuitry.

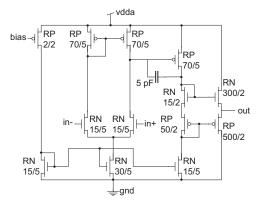


Fig. 5. The global operational amplifier is set up as a non-inverting amplifier with a gain of 1 (voltage buffer). The output of the amplifier is fed back into the negative input and the positive input is connected to the pixel output.

III. CAMERA SYSTEM

An OpalKelly XEM3001 FPGA integration module was used to measure the performance of individual photodiodes and the image sensor (Figure 1). The XEM3001 controlled a digital-to-analog converter (AD7304) to bias the image sensor and an analog-to-digital converter (AD7276) to convert the analog output of the image sensor for memory storage. The XEM3001 also provided the necessary digital signals to operate the image sensor. A graphical user interface was designed to control the whole system. The GUI has the ability to capture a still-frame from the camera as well as a continuous sequence of frames.

IV. TESTING AND CHARACTERIZATION

The time to integrate 1V at different intensities were measured to determine the integration characteristics of the photodiode. A dispersing filter was placed between a white light source (Genesys LS-150) and the image sensor. The light intensities were measured using a commercial photographic digital lux meter.

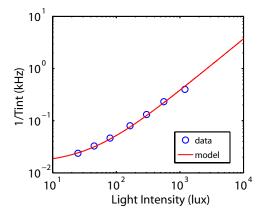


Fig. 6. Linearity of the photodiode and model fit. The data was gathered by measuring the integration time of 1 V at different light intensities. The equation of the linear model is $T_{int}^{-1} = 0.37 \cdot L_I + 15$.

The integration time (T_{int}) and the light intensity (L_I) have an inversely linear relationship for the photodiode as shown in Figure 6. Since the change in voltage (1 V) and the capacitance of the storage element (200 fF) is known, the current drawn by the photodiode relative to the light intensity can be calculated using the measured relationship between integration time and intensity (Eq. (3)). This relationship between the current drawn by the photodiode (I_{in}) and the intensity is shown in Eq. (4), where the coefficient is $7.4 \cdot 10^{-14} A/lux$ and the dark current is $3 \cdot 10^{-12} A$.

$$I_{in} = 200 f F \cdot \frac{1V}{T_{int}}$$

$$T_{int}^{-1} = \frac{I_{in}}{(200 f F)(1V)}$$

$$= 0.37 \cdot L_I + 15$$

$$I_{in} = (7.4 \cdot 10^{-14}) \cdot L_I + (3 \cdot 10^{-12})$$
(4)

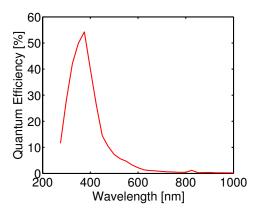
$$T_{int}^{-1} = \frac{I_{in}}{(200fF)(1V)} \tag{2}$$

$$= 0.37 \cdot L_I + 15 \tag{3}$$

$$I_{in} = (7.4 \cdot 10^{-14}) \cdot L_I + (3 \cdot 10^{-12})$$
 (4)

The quantum efficiency of the photodiode was measured by using the model derived from the integration characteristics (Eq. (1)). A HORIBA Jobin Yvon Fluoromax-3 generated wavelengths from 275 nm to 1000 nm. The calculated photocurrent from the SOS photodiode was compared to the output of a Newport 818-UV photodiode with known spectral responsivity under the same conditions. The quantum efficiency is shown in Figure 7. The SOS photodiode has a high quantum efficiency in near UV. However, at longer wavelengths, the quantum efficiency drops off because the thickness of silicon in the SOS process is 95 nm. This results in a depletion region thinner than traditional CMOS processes and photons at longer wavelengths do not generate electronhole pairs.

Various images were captured at different light intensities and frame rates to measure the properties of the system. A SUNEX DSL107 lens with F/# of 2.4 was used to focus the



Quantum efficiency of the photodiode. The peak occurs at 375 nm.

images when applicable. Sixty-four frames were captured at the different conditions, and the standard deviations of each pixel over the 64 frames were calculated to obtain the mean of the standard deviations of the 1024 pixels. The average standard deviation is 3 mV.

The output of the image sensor at different frames rates and power consumption are shown in Figure 8. The photodiode operates correctly with a F/# 2.4 lens even at 1000 frames per second (200 μ s integration time).

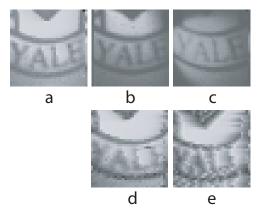


Fig. 8. Images captured with lens at various frame rates: a) 30 fps with 2.7 mW power consumption (reference), b) 500 fps, c) 1000 fps, d) 30 fps with 647 μ W power consumption, e) 30 fps with 181 μ W power consumption.

Another three sets of images (of 64 frames each) were captured to measure the fixed pattern noise of the image sensor. First, the image sensor was placed in the dark and the photodetector signal was integrated for 100 μ s to calculate the reset noise. Next, the image sensor was placed in the dark and the photodetector signal was integrated for 100 ms to measure the dark current. Lastly, light was focused on the image sensor and adjusted to be near saturation point for a given integration time for 30 fps to calculate the gain noise. For the noise calculations, the standard deviations of each pixel over the 64 frames were calculated and the mean of the standard deviations of the 1024 pixels were calculated for the above three cases. The standard deviation was 0.8 mV for a short integration time $(10 \ \mu s)$ in the dark with a swing of 3.8 mV, 2.2 mV for a long integration time (100 ms) in the dark with a 368 mV swing, and 3.8 mV when the image sensor was close to saturation while running at 30 fps with a 1.3 V swing. The signal-to-noise ratio was calculated by taking the mean swing of each pixel at near saturation over 64 frames and dividing it by the mean of the standard deviation of each pixel over 64 frames.

The power consumption was measured by observing how much current the image sensor was drawing through the VDDD and VDDA lines. The global operational amplifier and the pixels are powered by VDDA and the scan shift registers are powered by VDDD. A Keithley 2400 General-Purpose SourceMeter was used to measure the current. The scan shift register consumes 45 μ W, while the photodiode array and the global operational amplifier consume 200 μ W. The power consumption remained constant for all frame rates tested.

Although the data in Figure 8 shows the image sensor operating up to 1000 fps, the system is capable of much higher frame rates. The operational amplifier is able operate up to 10.5 MHz, or 10250 fps and is the limiting factor in the system. Also, the analog-to-digital converter used in the system is only capable of 3 MSPS, thus no images above 3000 fps can be obtained from the current setup unless we use a faster ADC.

V. ULTRAVIOLET TESTING

As seen from Figure 7, the back-illuminated photodiode has a high quantum efficiency in the near UV spectrum. Also, the integration of UV light by the image sensor was tested by using a 60-watt Hamamatsu Xenon Flash Lamp (L6604). A UV bandpass filter (Newport FSR-UG11) was placed on top of the image sensor. The light source saturated the image even at 500 μ s integration time. When a visible bandpass filter (Newport FSR-KG3) was used in conjunction with the UV bandpass filter with the same integration time, the image was dark as expected. No meaningful images are available, since we did not have access to a quartz lens.

VI. CONCLUSION

We have presented the first fully-working back-illuminated image sensor in SOS 0.5- μ m process that is also capable of detecting UV light. The image sensor has a resolution of 32 x 32 pixels. Each 40 μ m x 40 μ m pixel contains a photodiode and memory capacitor. Pixel reset, integration and output occur in full frame "snap-shot" fashion. The image sensor is able to achieve continuous 1000 frames/s operation and can consume as low as 650 μ W of power. A better operational amplifier and analog-to-digital converter will greatly improve both the analog read out and digital conversion speeds.

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TABLE I IMAGE SENSOR PROPERTIES

Technology	0.5-μm silicon-on-sapphire
Array Size	32 (H) x 32 (V)
Total Size	1.5mm x 1.5mm
Pixel Size	$40\mu \text{m x } 40\mu \text{m}$
Fill Factor	43%
Power Consumption	650 μW (@ 3.3V)
Fixed Pattern Noise	0.8 mV (dark, 10 μ s integration)
	2.2 mV (dark, 100 μ s integration)
	3.8 mV (light, before saturation)
Output Voltage Swing	1.5 V
Dark Current	3 pA
Conversion Gain	0.8 μV/e-
SNR	48 dB
Max Frame Rate	1000 fps

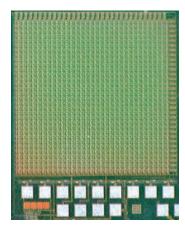


Fig. 9. Picture of the fabricated SOS image sensor die.

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