Electrical Noise Analysis of an Integrated Patch-Clamp Amplifier

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***Abstract*— This paper presents an evaluation of electrical noise sources and signal-to-noise limitations in a fabricated integrated patch-clamp amplifier. We also present numerical calculation of the theoretical noise of the patch-clamp system. Our fabricated device was measured to have less than 4pA of rms noise at 10kHz bandwidth, similar in performance to commercial bench-top systems. The integrated patch-clamp can accurately measure nano-Amperes of current and is intended for a high-throughput system that can screen a large number of cells in parallel. The fabricated device consumes 1480 by 1300μm of silicon area and 3.2mW at 3.3V of power. The device was fabricated using AMI 0.5 micron technology.**

I. Introduction

The advancements in medicine of the last century and the resulting benefits in disease diagnosis and patient recovery has been made possible by the availability of electrical biosensors. Electrophysiologists use patch-clamp biosensors to measure the currents flowing through membranes of living cells. The cell currents measured by the patch-clamp is used to study the effect medical compounds and to study the behavior of ion channels, the structures responsible for cell membrane conductivity [1].

The patch-clamp technique has the highest signal-to-noise ratios available in a biosensor, and patch-clamp designers pay considerable detail to sources of noise and their reduction [2]. Since patch-clamps are used extensively to test drugs, it would be beneficial for pharmaceutical companies to use high throughput screening instrumentation that would increase the number of recordings made per unit time. Such instrumentation would facilitate the introduction of safer and better drugs to the consumer market [3]. Other than minimizing the space requirements, an integrated patch-clamp amplifier reduces noise. It also offers better electrical performance by decreasing cabling and other parasitic capacitances that lower the measurement bandwidth. Therefore, it is prudent to analyze the noise performance of an integrated patch-clamp amplifier and thereby determine the feasibility of using an integrated patch-clamp amplifier to build the high-throughput system shown in Fig. 1. This system uses a low-noise integrated patch-clamp amplifier along with planar patch-clamp technology [4], [5], [6]. This system will be able to produce concurrent measurements from an entire 384 well plate in less than a minute protocol time. This design also differs from previous designs [7] because it has the capability to compensate for electrode parasitics [8].

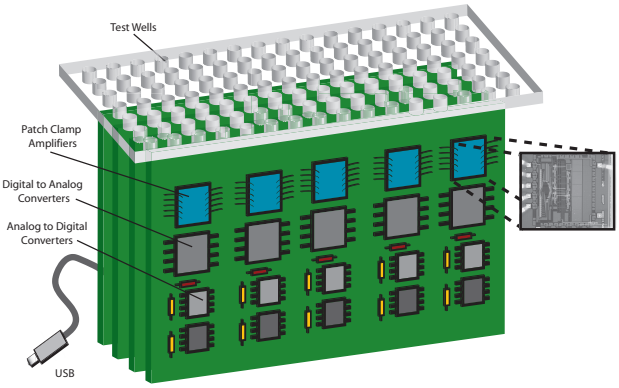

Fig. 1. A high-throughput patch-clamp system comprised of integrated patch-clamp amplifiers. This system allows to perform simultaneous patch-clamp recordings on an entire 384 well plate.

II. Patch-Clamp Design and Noise Limitations

During the design of an integrated patch-clamp amplifier, it is important to compute the input-referred electrical noise in order to quantify the minimum detectable signal and also compute the SNR. The SNR is a useful benchmark to evaluate the performance of the instrument. The SNR of patch-clamp amplifiers is affected by fundamental electrical noise sources and also by the desired input bandwidth.

A. Patch-Clamp Recording System Overview

Fig. 2 shows a block diagram of the patch-clamp headstage. The system consists of an input current-to-voltage trans-impedance amplifier that uses resistive feedback (R_f). A difference amplifier subtracts the command voltage from the tranimpedance amplifier's output. The resultant output voltage is proportional to the input current, as in equation 1.

$$V_{out} = I_{in} R_f \tag{1}$$

Command voltage steps (V_{com}) between 10mV and 100mV are applied to the cell membrane during experiments, in order to activate ion channel proteins and to permit ionic currents to flow across the membrane. Patch-clamp ionic currents are

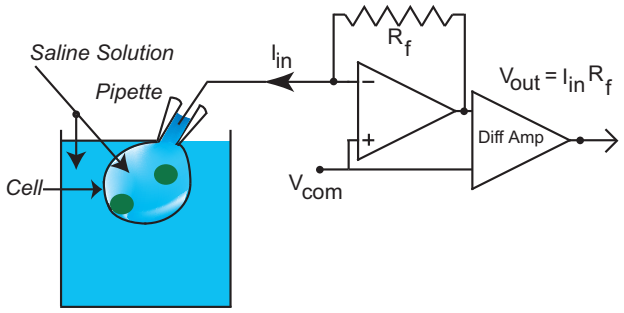

Fig. 2. Patch-clamp amplifier headstage. A trans-impedance amplifier followed by a difference amplifier produces an output proportional to the input current.

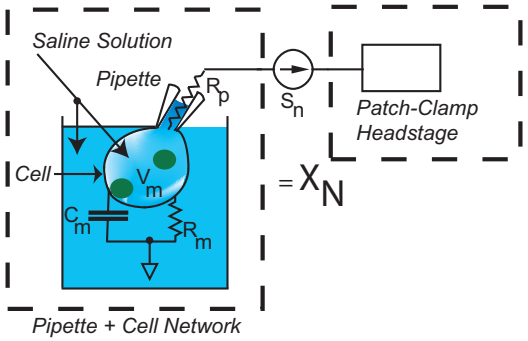

Fig. 3. Micropipette plus cell network. The noise level of this network limits the performance of the patch-recording system.

typically monitored at 1-10KHz. A whole-cell clamp reports the current across the entire cell membrane, as opposed to a patch of membrane. A pipette filled with a saline solution is used to adhere to the cell A whole-cell patch recording system typically measures currents in the range of a few nano-Amperes. Currents are bidirectional depending on the channel type and the membrane potential.

B. Current Noise Limits of the Patch-Clamp System

Low amplitude current measurements are often complicated by the presence of electronic noise. Electronic noise can be fundamental or man-made. Fundamental noise sources derive from the physical laws and the property of condensed matter. Man-made noise is induced by circuit design, layout, topological placement and system architecture. There are fundamental limits on the signal-to-noise ratio (SNR) that can be attained with biosensors measuring small currents. In this section we review these limitations so that designers can quickly assess the feasibility of measuring systems. The SNR physical limitations also allows us to compare the performance of our integrated patch-clamp system. Man-made noise source can be avoided with experienced and robust engineering and can ultimately approach the physical limits.

The noise level of a patch-clamp system is limited by the fundamental noise sources of the cell plus micropipette network shown in Fig. 3. The micropipette electrode can be modeled as a resistance R_p. The cell can be modeled as a membrane capacitance C_m in parallel with a membrane resistance R_m. Typical values for R_p, R_m and C_m are 4MΩ, 100MΩ and 20pF respectively. The noise level of cell plus micropipette network, S_n can be calculated using equation 2. Here, K is the boltzmann constant and T is the absolute temperature and X_N is the equivalent impedance of the pipette plus cell network. X_N can be calculated using equation 3. When designing a low-noise amplifier to measure low amplitude membrane current it is sufficient to ensure that the noise contribution of the amplifier is less than that of X_N.

$$S_n = \frac{4KT}{real(X_N)} \tag{2}$$

$$X_N = \frac{R_m}{1 + R_m C_m w j} + R_p \tag{3}$$

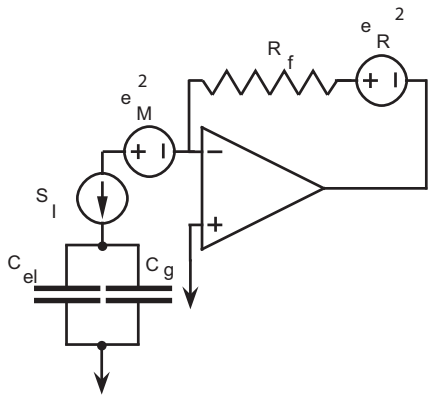

Fig. 4. The model used to calculate the noise of the patch-clamp headstage shown in Fig.3.

C. Calculation of Current Noise in the Patch-Clamp Amplifier

The patch-clamp technique is extremely sensitive to noise due to the low amplitude of the membrane current and hence low-noise amplification is critical to our design. The circuit model used to compute the input-referred current noise of the patch-clamp headstage in Fig.3 is reported in Fig. 4. The input-referred current noise of the patch-clamp amplifier can be calculated by by equation 4. e_M is the sum of the flicker noise and thermal noise components of the input transistor of the headstage and e_R is the thermal noise of the feedback resistor. C_{el} is the capacitance of the electrode and C_g is the gate capacitance of the input transistors. e_M and e_R can be calculated using equations 5 and 6 respectively.

$$S_I = \frac{e_M^2 + e_R^2}{{R_f}^2} + e_M^2 4\pi^2 (C_{el} + C_g)^2 \tag{4}$$

$$e_M^2 = \frac{8KT}{3g_m} + \frac{K_f g_m^2}{C_{OX} L^2 f} \tag{5}$$

$$e_R^2 = 4KTR_f \tag{6}$$

Here K_f is the process dependant flicker noise parameter and g_m is the transconductance of the input transistors. There-

fore, by combing equations 4, 5, and 6, we obtain equation 7.

$$S_I = \frac{4KT}{R_f} + \left[\frac{8KT}{3g_m} + \frac{K_f g_m^2}{C_{OX} L^2 f}\right] \frac{1}{R_f^2} + \left[\frac{8KT}{3g_m} + \frac{K_f g_m^2}{C_{OX} L^2 f}\right] 4\pi^2 (C_g + C_{el})^2 f^2 \quad (7)$$

D. Low-Noise Patch-Clamp Amplifier Design

All amplifiers are implemented using a low-noise three stage operational amplifier shown in Fig. 5. The input differential stage is followed by a second stage which allows for higher output swing. The third stage is an output stage. The input V_{bias} sets the quiescent point for the circuit and the inputs V_{cascP} and V_{cascN} provide biases to the cascode devices in the second stage that increases the bandwidth of the operational amplifier.

The input transistors are vital in establishing thse noise characteristics of the operational amplifier. The gate capacitance C_g of the input MOSFET is proportional to the area of the transistor, while the thermal noise e_n decreases as the square root of the area (assuming constant gate length). The noise of the recording system is proportional to $C_{in}e_n$ where the total input capacitance is C_{in} = C_g + C_{el}. By differentiating equation 4 with respect to C_g, the optimal gate can be shown to be the gate width corresponding to C_g = C_{el}. The flicker noise due to the trapping of charges below the gate of the transistor is a significant problem in making low-noise measurements using MOSFETs. This problem was alleviated using P-channel transistors which have been shown to have one or two orders lower K_f than n-channel devices [9]. As discussed in section II, the trans-impedance amplifier multiplies the input current by R_f to produce a voltage proportional to the input. The current noise at the input can be shown to be inversely proportional to R_f. However, the parasitic capacitance and the physical size of of R_f in layout as well the headroom limitations in the amplifier limits its value. A R_f of 25MΩ was chosen for our design.

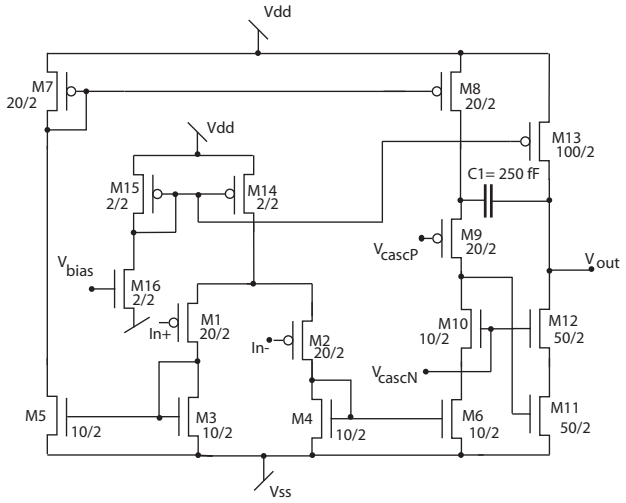

Fig. 5. The operational amplifier used in the design. The input stage was optimized for low-noise performance. All sizes [W/L] ratios are given in micro meters.

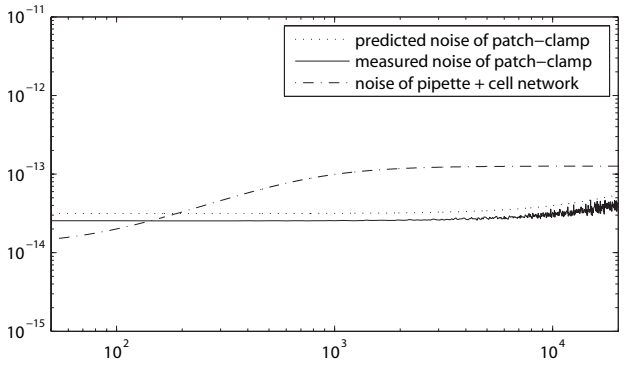

Fig. 6. The measured and simulated amplifier input-referred current noise spectrum compared with the noise contribution of the pipette plus cell network. The measured current noise is no greater than the noise level of the pipette plus cell network. Integration under this curve yields and rms noise current of 4 pA.

III. Experimental Results

Fig. 6 shows the measured input-referred current noise spectrum compared with the theoretical noise calculated using equation 4. The figure also shows that the input referred current noise of the low-noise amplifier is no greater than the noise contributed by the pipette electrode plus cell network calculated using equation 2. The flicker noise parameter K_{fp} was extracted as 10^{-25} V^2F. Integrating the input-referred noise yields an rms current noise of 4pA at 10kHz bandwidth. This corresponds to a signal to noise ratio of 250 or approximately 8 bits in whole-cell patch-clamp measurements. This result is comparable to state-of-the-art commercially available bench-top amplifiers. For example, the latest ionWorks amplifier from Molecular Devices has noise levels of 10pA of rms current at 10kHz bandwidth.

We tested the integrated patch-clamp amplifier by sourcing a range of inputs currents from a fraction of a nano-Ampere to a few nano-Amperes, while recording the output voltage. The amplifier was powered at 3.3V and the biases and the command voltage was provided by an Analog Instruments AD7304 digital to analog converter (DAC) controlled through an Opal Kelly 3010 FPGA board. The output of the amplifier was digitized using an Analog Instruments AD7475 analog to digital converter (12 bit resolution). The voltage noise on the current monitoring signal was measured as less than 10mV (corresponding to a 0.4nA rms of input-referred current noise). The excess noise is contributed by the testboard and the electrode compensation circuitry [8]. The input current was sourced by applying protocol corresponding to a bidirectional V_{com} of 10mV to 100mV across an Axon Instruments Patch-1U model cell. Fig. 7 shows the protocol used to evaluate the performance of the patch-clamp amplifier.

We obtained a linear dependency across the entire range of tested currents as shown in Fig. 8. The devices consumed

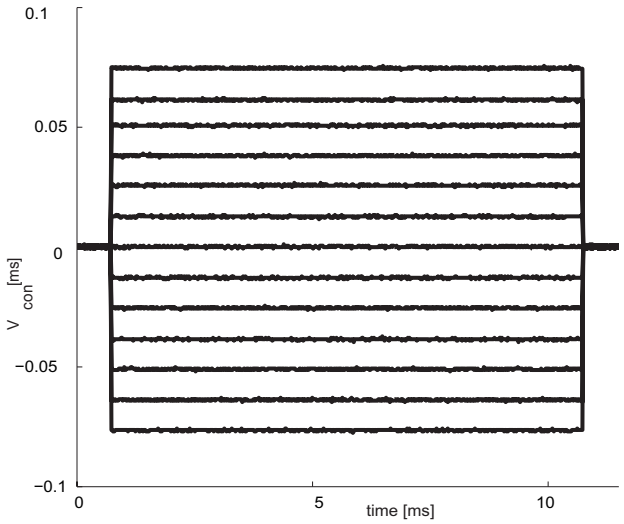

Fig. 7. The protocol used on the Patch-1U model cell to evaluate the patch-clamp amplifier.

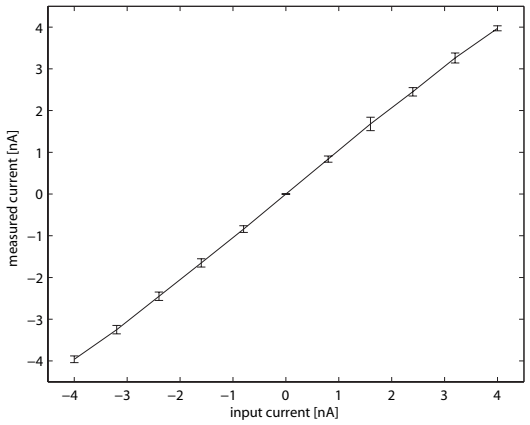

Fig. 8. The measured current from the integrated patch clamp amplifier as a function of input current.

3.2mW of power when operated with a 3.3V power supply. The slew rate of the operational amplifier was measured to be 1.5 $\mu V/s$. The input dynamic range of the amplifier was measured to be 2V pk-pk and the gain-bandwidth product was measured as 2MHz.

IV. Summary

We performed a noise analysis on a fabricated integrated patch-clamp system to investigate the feasibility employing the integrated circuitry to build high throughput patch-clamp systems. The prototype was fabricated on conventional AMI 0.5 micron technology. The low-noise amplifier used in the design produced less than 4pA of rms noise. The device is capable of measuring nano-amperes of current making it ideally suited to fabricate high-throughput whole-cell patch recordings arrays. The die size of the integrated patch clamp amplifier is

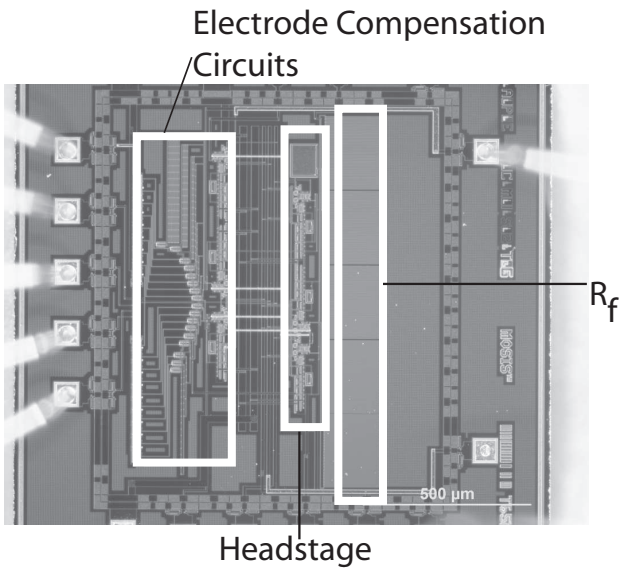

Fig. 9. Figure 7. Die micrograph of the integrated patch-clamp amplifier

$1480\mu m$ x $1300\mu m$. A micrograph of the fabricated die is shown in Fig. 9.

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