A Low-Power Silicon-On-Sapphire Tunable Ultra-Wideband Transmitter

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***Abstract*— A low-power tunable transmitter for ultra-wide band (UWB) radio was designed and fabricated. The design is based on a ring oscillator VCO, to produce short pulses. Both the pulse duration and frequency is controllable by two voltage biases. The transmitter can be used in both pulse-amplitude modulation (PAM) and pulse-position modulation (PPM). The circuit was fabricated on a 0.5μm silicon-on-sapphire CMOS process, and has been experimentally characterized with a transmitter and receiver module. The UWB transmitter produces monocycle pulses of 800ps duration. The power consumption is 75μW when the pulse frequency is 3MHz. The core pulse generator occupies 0.0091mm^2 of silicon area.**

***Index Terms*—Ultra-wide band radio (UWB), pulse generator, pulse modulation, UWB transmitter**

I. Introduction

In recent years, there has been a growing need for low-power, low-complexity short range wireless communication devices [1]. Battery-powered systems such as Wireless Sensor Networks (WSN), Body Area Networks (BAN), and biological applications, especially implantable biosensors [2], require wireless transmitters with reduced energy consumption (less than 1mW).

UWB radios have the potential to satisfy these requirements. Ultra-Wideband (UWB) radio is a kind of wireless transmission whose output occupies a wide frequency spectrum. A radio system is considered to be of UWB kind when its fractional bandwidth is greater than 0.25 or occupies a spectrum of 0.5GHz or more [3]. A UWB transmitter is based on the modulation of pulses and does not use a carrier. It can be designed with high-data rate low-complexity and provide low-power consumption [4]. For this reason, UWB is used in indoor communications, personal communications [1], wireless sensor networks [5] and body area networks [6] [7].

Though UWB transmitters are known as low-complexity and low-power circuits, in previous design, the oscillator, pulse generator and modulator is separated [4]. In [8] (with 0.13μm process) a transmitter consumes 350μW energy but occupies 0.48mm^2 chip area, and a pulse generator in [9] (with 0.18μm process) has 0.078mm^2 area with 18.33mW power consumption. Our design provides a low-power high-data rate transmitter with small silicon area. The oscillator, pulse generator and modulator are merged in a compact circuit, which can be easily adapted as a short-range wireless module.

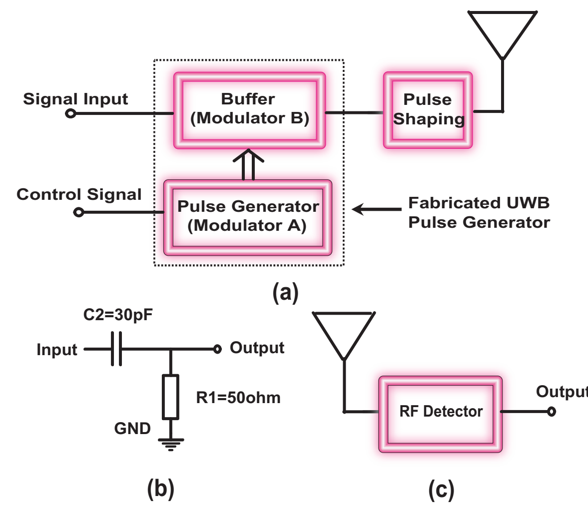

Fig. 1. Block diagram of the UWB transmission system. (a) The transmitter is composed of a pulse generator, a buffer, a pulse shaping circuit and an antenna. Both pulse generator and buffer can be used as pulse modulators. (b) Schematic of a pulse shaping circuit. (c) The receiver consists of antenna and a RF detector.

The transmitter was fabricated in a 0.5μm silicon-on-sapphire CMOS process. It consists a tunable pulse generator, occupying 0.0091mm^2 chip area and offers power consumptions of less than 1mW. This device is ideally suited to local personal communication system. We also instrumented a test platform for UWB transmission system based on our integrated circuit.

This paper is organized as follows. Section II describes the the pulse generator circuit and the architecture of the transmitter. Section III presents the test result from the fabricated integrated circuit, followed by Section IV, describing experimental results of wireless transmission. Finally, Section V summarizes the paper.

II. System Overview

The functional block diagram of the transmission system is shown in Fig. 1. The transmitter consists of a pulse generator, an amplitude modulator (buffer), a pulse shaping circuit and an antenna. In this prototype, the pulse generator is integrated on-chip. The receiver includes a commercial RF detector and an antenna. The pulses from the pulse generator are modulated

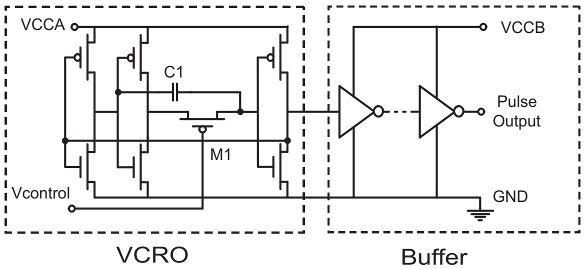

Fig. 2. Schematic of on-chip UWB pulse generator. It contains a *voltage controlled ring oscillator (VCRO)* and an output buffer. The MOSFETs in the *VCRO* are in the minimum size, the number of stages and transistor size in the buffer is designed to fit the load and power budget, 4 stages in our design.

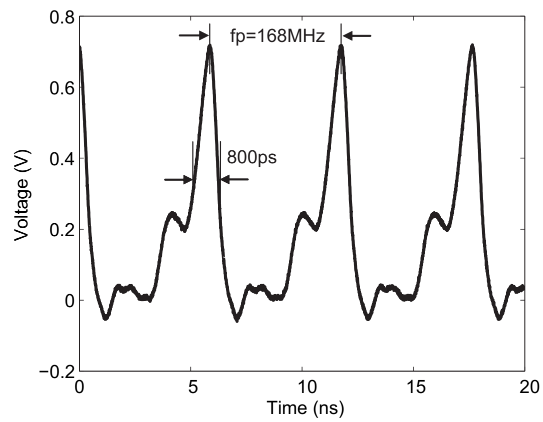

Fig. 3. Output pulses generated by our UWB transmitter. Here we show three pulses with amplitude of 0.7V. The duration of each pulse is 800ps. $V_{control}$ was set to 1.5V and the pulse frequency (f_p) is 168MHz.

and transmitted to the RF detector wirelessly through the antennas.

1) Pulse Generator: The pulse generator is the fundamental block of a UWB transmitter. The schematic of our pulse generator is shown in Fig. 2. It consists of 2 components: a *voltage control ring oscillator (VCRO)* and an output buffer. The *VCRO* is implemented with a 3-stage inverter-based ring oscillator. The output buffer is implemented with 4 inverters to buffer the *VCRO* output. The pulse frequency can be controlled by *VCCA* and $V_{control}$. *VCCA* controls the frequency by changing the supply voltage of the oscillator. $C1$ and $M1$ implement a variable delay that can change the oscillation frequency by means of $V_{control}$. The drain current of $M1$ charges $C1$, the charging and discharging time affect the oscillator frequency. *VCCB* can be used as a pulse output enable signal, as well as a bias to control the pulse amplitude and transmitted power. The number of the stages and size of each device in output buffer is designed to drive the pulse shaping circuit of Fig 1(b) and the antenna or a load of 50Ω. Output buffer dominates the power consumption of the integrated UWB pulse generator.

2) Transmitter Architecture: The transmitter is composed of the on-chip pulse generator, a pulse shaping circuit and an antenna. As shown in Fig. 1(b), the RC high-pass filter works as a pulse shaping circuit. It shapes the pulse by taking the derivative of the oscillator waveform and generates monocycle pulses. The value of $R1$ and $C2$ are chosen to match the impedance of the antenna to avoid signal reflection, this part should be designed to consist with antennas in different applications. The amplitude and duration of the pulses can also be controlled by $R1$ and $C2$. In the present prototype, the pulse shaping circuit is implemented off-chip for flexibility purposes, but can be easily integrated in future designs.

The antenna is another key component for the UWB transmission system [10]. It should be able to transmit wideband signal with minimum distortion in order to keep the pulse shape and amplitude in both the time and frequency domains [11]. In our design, we use a pair of planar triangular copper foil as antenna for both transmitter and receiver.

III. Integrated Circuit Test Result

Our prototype was fabricated on the Peregrine Semiconductor 0.5 micron silicon on sapphire (SOS) CMOS process. We choose the SOS technology for its speed and low power operation and its isolating substrate. This substrate offers lower parasitic capacitance than bulk CMOS circuit [12]. The total area of the integrated circuit without pads is 70μm x 130μm and 420μm x 420μm with pads. The power supply is 3.3V or 1.5V.

We tested the integrated UWB pulse generator with a Tektronic CSA 8000B Communication Signal Analyzer. The measured waveform is illustrated in Fig. 3, where 3 pulses are shown. Without pulse shaping circuit, the on-chip pulse generator generates pulses of 800ps duration (at 50% to 50% of the amplitude). The pulse amplitude is 0.7V. The frequency of the pulses (f_p) can be controlled by *VCCA* or $V_{control}$. The individual pulse shape does not vary from Fig. 3, which is guaranteed by pulse shaping circuit.

We measured the frequency and power consumption of the pulse generator in both 3.3V and 1.5V power supply, the results are shown in Fig. 4 and Fig. 5. In 3.3V power supply, the pulse frequency decreases from 70MHz to 25MHz as $V_{control}$ increases from 2.3V to 2.8V. The power consumption is 9mW when the pulse frequency is at 70MHz and 3.4mW at 25MHz. In 1.5V power supply, f_p increases from 3MHz to 44MHz when $V_{control}$ decreases from 1.02V to 0.15V. The power consumption is 1.3mW when f_p is at 44MHz and 75μW at 3MHz. The power consumption can be even lower by decreasing *VCCB* or using fewer stages in output buffer.

This UWB transmitter can provide high-datarate transmission with low power-consumption. For instance, when transmit 1 bit signal using 5 pulses, 1Mbps data rate needs pulse frequency of 5MHz, which means 0.14mW power consumption at 1.5V power supply. The power performance is much better than nowadays commercial RF transmitters, such as Zigbee [13](148.5mW at 250kbps), [14](16mW at 1Mbps)

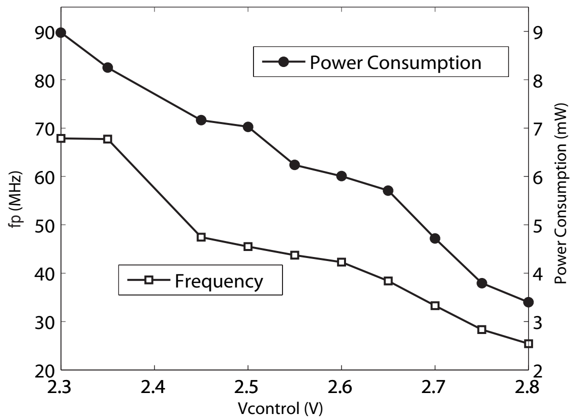

Fig. 4. Measured pulse frequency and power consumption as a function of $V_{control}$. *VCCA* and *VCCB* is set at 3.3V. The pulse frequency decreases from 70MHz to 25MHz when $V_{control}$ increases from 2.3V to 2.8V. The power consumption is between 3.4mW and 9mW

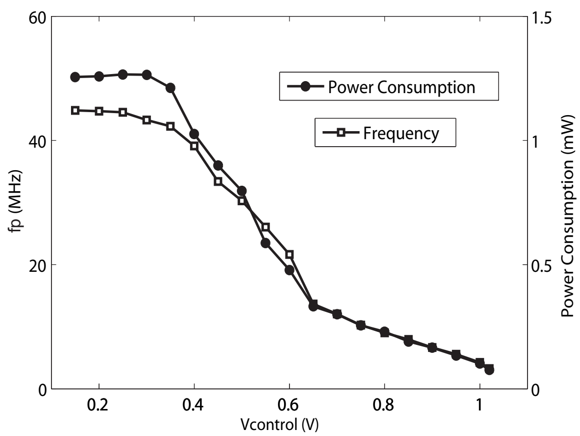

Fig. 5. Measured pulse frequency and power consumption as a function of $V_{control}$. *VCCA* and *VCCB* is set at 1.5V. The pulse frequency decreases from 44MHz to 3MHz when $V_{control}$ increases from 0.15V to 1.02V. The power consumption is between 75μW and 1.3mW

or Bluetooth transmitter (which usually consumes 30mW or more).

IV. Wireless Transmission Test Results

We designed a UWB transmitter using the SOS pulse generator. The power supply and input signals can be provided by an OpalKelly 3001v2 FPGA board (for 3.3V power supply). *VCCB* is used as digital input, to operate the transmitter in pulse amplitude modulation (PAM) mode (turning the pulse on and off, also known as On/Off Keying or OOK)[1].

We assembled two identical antennas for UWB transmitter and receiver by using triangular copper foil on a plastic sheet as illustrated in Fig. 9. We used a Analog Device AD8313 Logarithmic detector as the receiver. The output of the device is a function of the input RF signal power. The minimum receiver output amplitude is 500mV and this

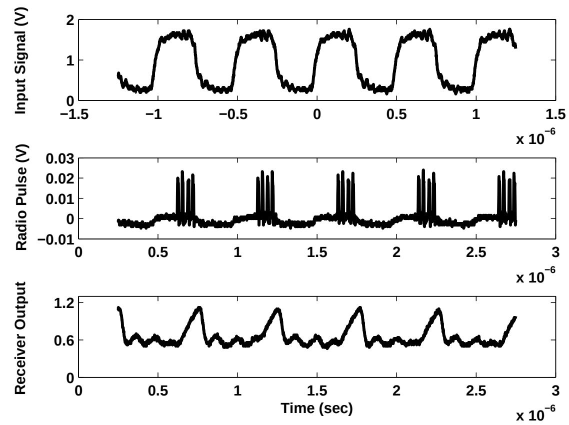

Fig. 6. Wireless communication test result in high data rate. Top: the 1.5V, 1.9MHz digital input signal modulates the amplitude of the pulses (PAM). Middle: the modulated UWB output pulses transmitted to antenna, in which 4 pulses are used to present 1 bit signal. Bottom: RF receiver output waveform showing the reconstructed signal from the received pulses.

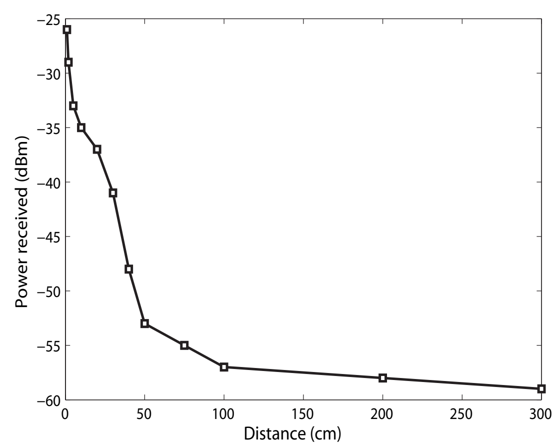

Fig. 7. Received power versus TX and RX distance. A commercial -70dBm wide-band RF power detector can receive the signal from our UWB transmitter in 300cm.

amplitude increases with higher RF input power. The receiver was designed to detect narrow-band signals with RF power of -70dBm or more. The maximum slew rate of the receiver evaluation board can reach at 5,500 V/μs, which results in a rise time of 545 ps, making it ideal as a pulse amplifier [15].

Fig. 6 shows the wireless transmission waveform. We used a 1.5V digital signal sequence as input signal to modulate the pulse amplitude. The UWB transmitter generates pulses for the input signal and transmits the pulses to TX antenna. The receiver collects data from RX antenna and reconstructs the waveform. The input digital signal is 1.9Mbps. We use 4 pulses to present 1 bit signal. The antenna distance between TX and RX is 15 cm.

The amplitude of the receiver output depends on both the orientation and distance between the antennas. Fig. 7 shows

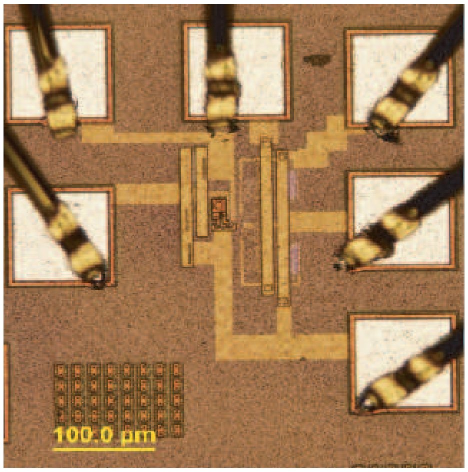

Fig. 8. Die micrograph of the integrated UWB pulse generator on a 0.5μm silicon-on-sapphire CMOS process

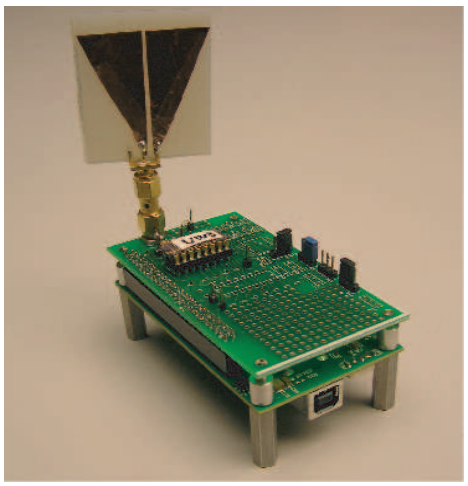

Fig. 9. Transmitter test system. An FPGA is connected to the transmitter and provides power supply and input signals. The input signal is delivered to the FPGA by means of a USB bus.

the received power as a function of the distance between antennas. The data in Fig. 7 is converted from output amplitude to received power according to the AD8313 data sheet. The transmitter and receiver antenna planes are facing each other, with the same height and the same orientation. Larger ranges can be attained with a more sensitive receiver.

V. Summary

We designed, fabricated and tested a silicon-on-sapphire low-power tunable UWB pulse generator which has the potential to be widely used in short-range low-power wireless applications. The circuit was fabricated on 0.5 micron SOS process. A micrograph of the integrated circuit is shown in Fig. 8. The whole transmitter test platform is illustrated in Fig. 9. The test result shows that our circuit consumes 75μW when f_p is at 3MHz, with 1.5V power supply. The core circuit occupies 0.0091mm^2 square. Table I summarizes the main results and

Process technology	SOS 0.5μm CMOS
Pulse Frequency f_p	2MHz-200MHz
Duration of Pulse	800ps
Amplitude of Pulse	0.7v
Power consumption	75μW (at f_p=3MHz)
Transmitting Distance	300cm (at -60dBm)
Chip Area (without pad)	70μm x 130μm
Chip Area (with pad)	420μm x 420μm

TABLE I
Summary of the UWB Transmitter Performance.

properties of our UWB transmitter circuit.

VI. Acknowledgements

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