CSE/EEE 120

Lab 4 Answer Sheet

The Complete Microprocessor

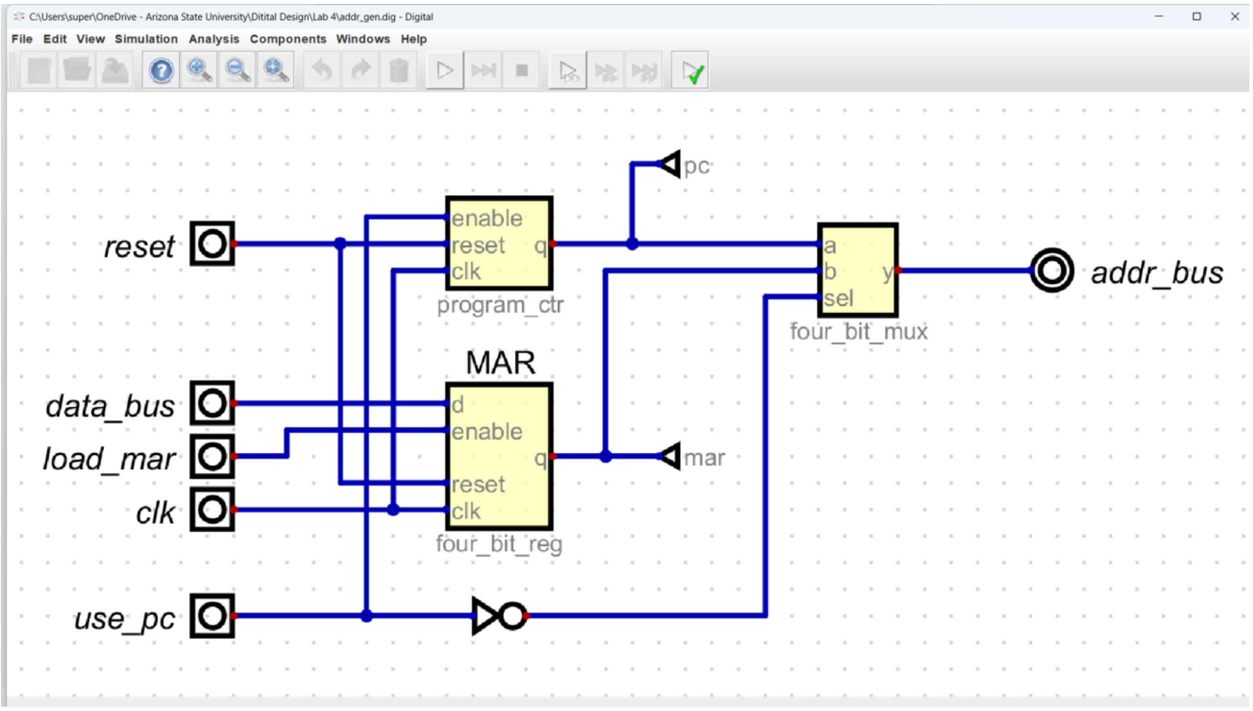
Name: ElHadji Omar Bane

Instructor/Time: Doctor Steve @ 10:30 Tuesday & Thursday

Date: 04/04/2024

Task 4-1: Build and Test the Memory-Address-Generation Circuit

Include a picture of your Digital circuit here:



C:\Users\super\OneDrive - Arizona State University\Ditital Design\Lab 4\addr_gen.dig - Digital

Please comment on the single biggest issue you were facing when designing the circuit.

The biggest issue I faced was understanding how the circuit contributed to the microprocessor.

Did the circuit behave as expected? If no, what was wrong?

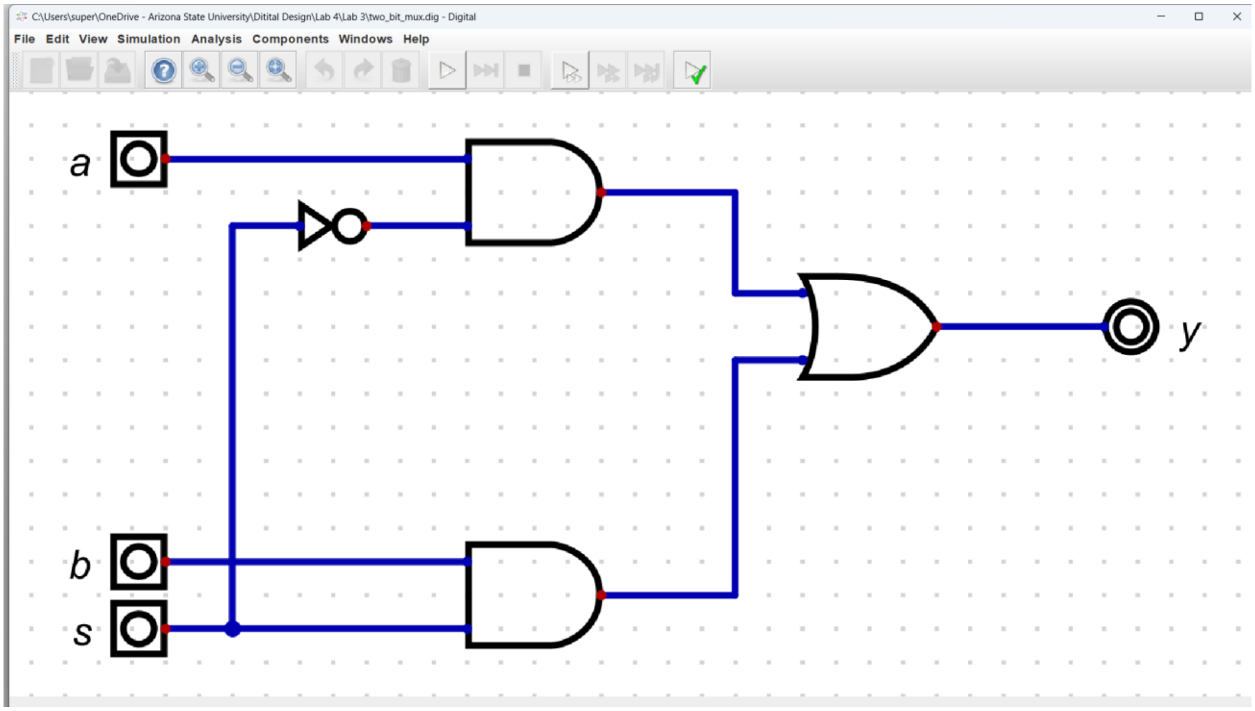
I did.

Please comment on the single biggest issue you were facing when simulating the circuit.

The biggest issue I faced was using the

Task 4-2: Build and Test the Controller Circuit

Include a picture of your two_bit_mux circuit here:


C:\Users\super\OneDrive - Arizona State University\Ditital Design\Lab 4\Lab 3\two_bit_mux.dig - Digital
File
Edit
View
Simulation
Analysis
Components
Windows
Help
a
b
s
y

Please comment on the single biggest issue you were facing when designing the circuit.

The biggest issue I faced was finding and dragging logic gates (The circuit wasn't complicated).

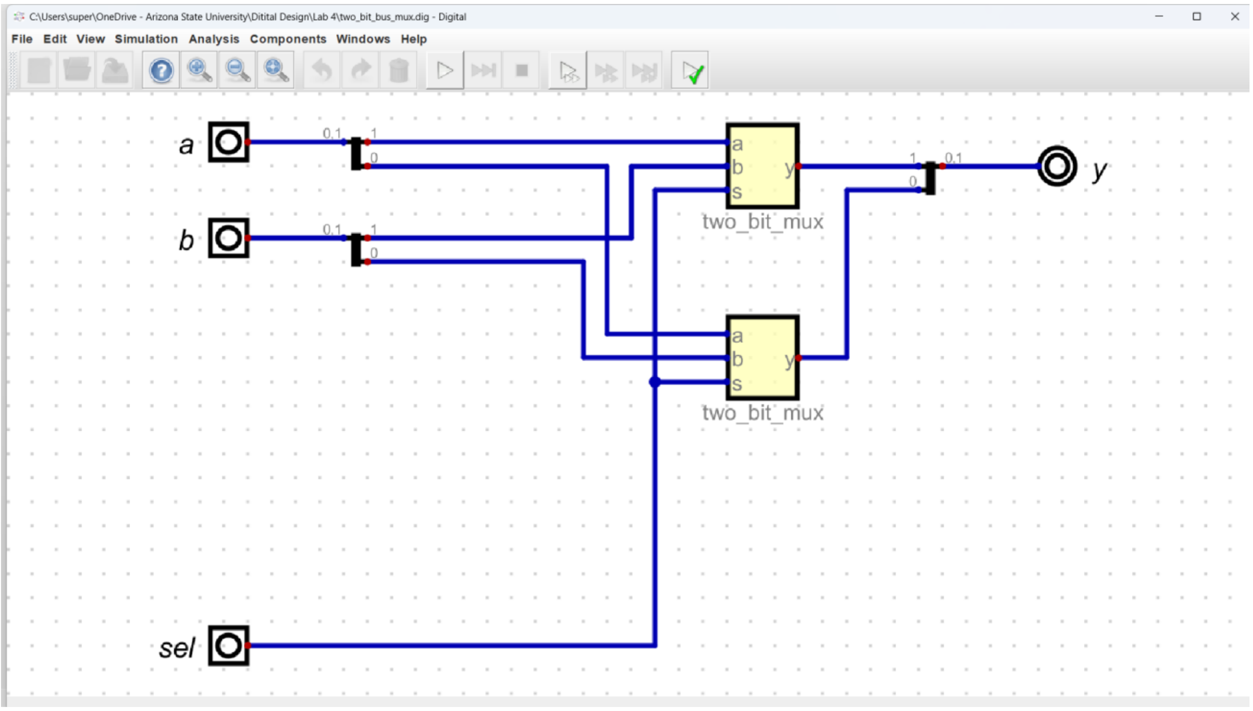
Did the circuit behave as expected? If no, what was wrong?

It did.

Please comment on the single biggest issue you were facing when simulating the circuit.

The biggest issue I faced was clicking the inputs (The circuit wasn't complicated).

Include a picture of your two_bit_reg circuit here:



Please comment on the single biggest issue you were facing when designing the circuit.

The biggest issue I faced was getting the correct values for the splitter/mergers.

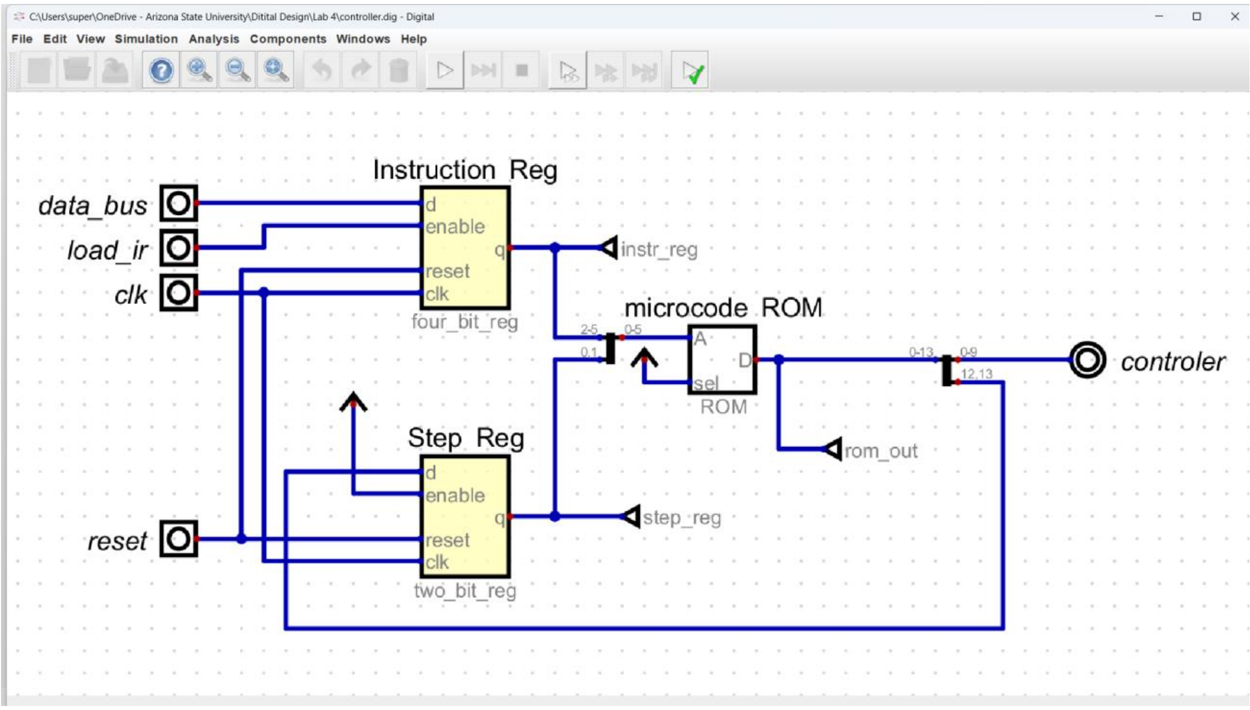
Did the circuit behave as expected? If no, what was wrong?

It did.

Please comment on the single biggest issue you were facing when simulating the circuit.

The biggest issue I faced was troubleshooting the splitter/mergers.

Include a picture of your controller circuit here:



Please comment on the single biggest issue you were facing when designing the circuit.

The biggest issue I faced was getting the correct values for the splitter/mergers.

Did the circuit behave as expected? If no, what was wrong?

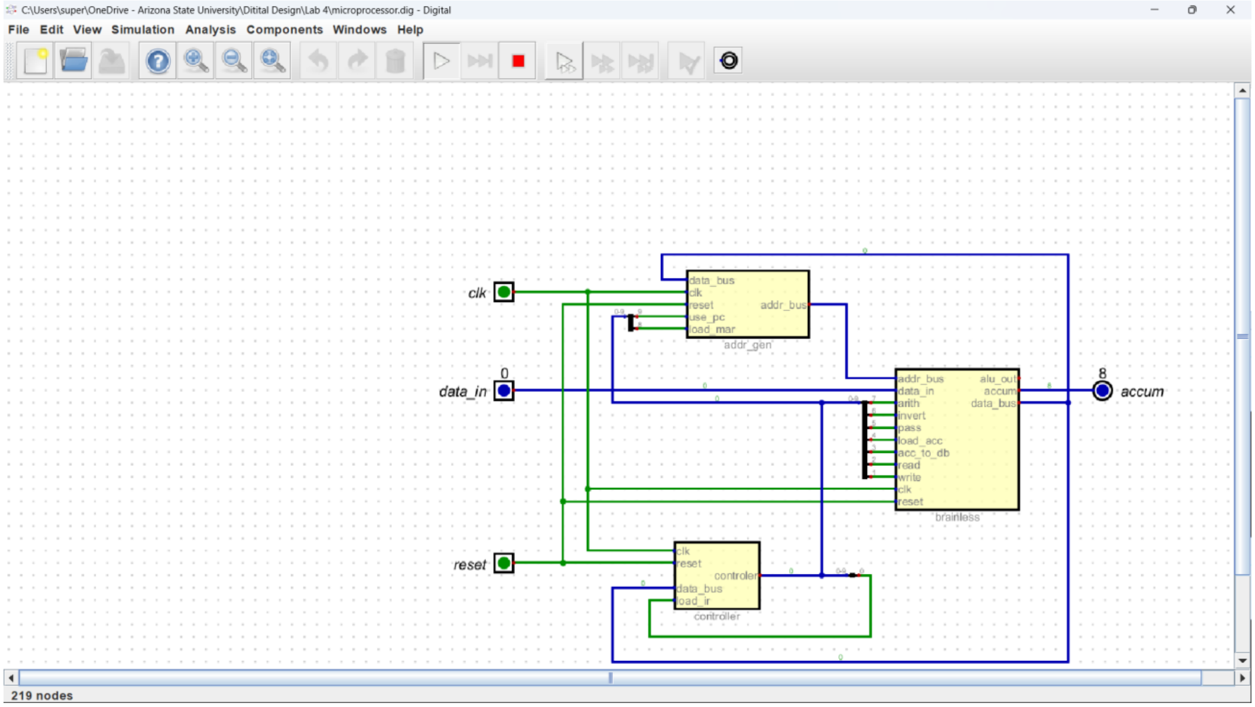
It did.

Please comment on the single biggest issue you were facing when simulating the circuit.

The biggest issue I faced was learning how to utilize the ROM and understanding the meaning of the output.

Task 4-3: Build the Complete Microprocessor Circuit

Include a picture of your Digital circuit here (make sure to show final values as shown in figure 17):


C:\Users\super\OneDrive - Arizona State University\Ditital Design\Lab 4\microprocessor.dig - Digital

Please comment on the single biggest issue you were facing when designing the circuit.

The biggest issue I faced was understanding where each wire should be connected to.

Did the circuit behave as expected? If no, what was wrong?

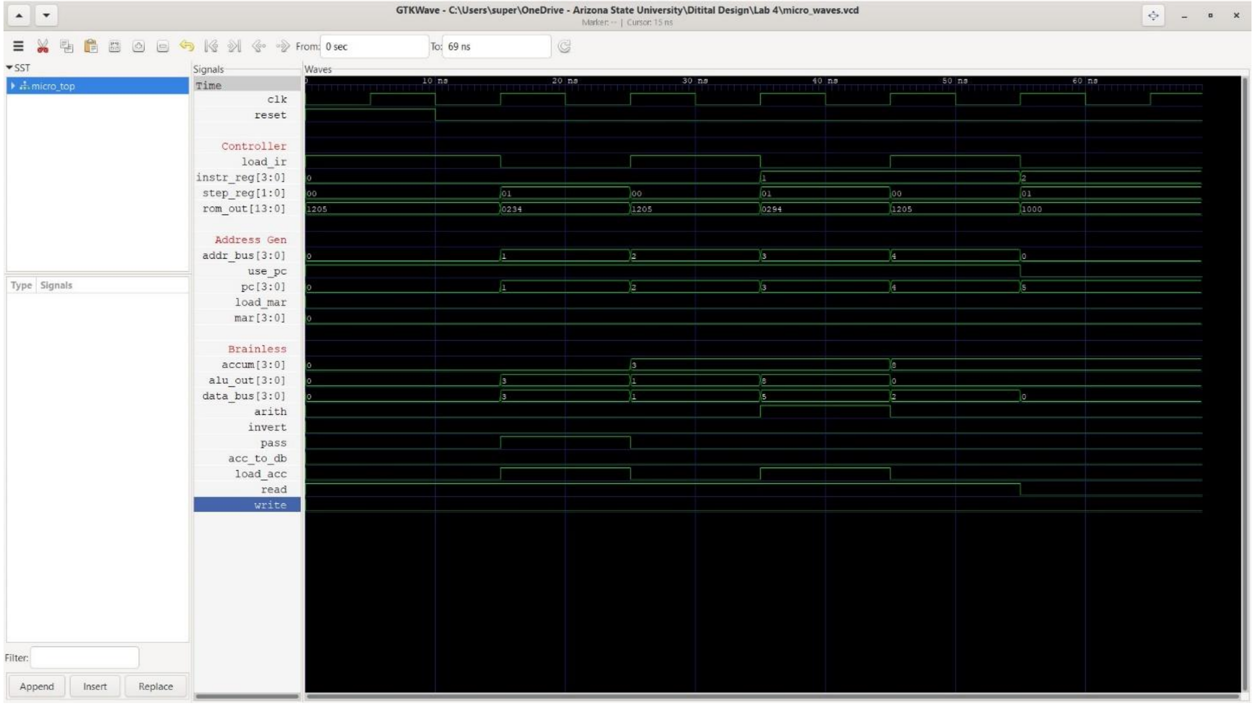
It did.

Please comment on the single biggest issue you were facing when simulating the circuit.

The biggest issue I faced was learning how to control values.

Task 4-4: Simulate the Design in Verilog

Include a picture of your waveforms here:



Please comment on the single biggest issue you were facing when simulating the processor.

The biggest issue I faced was learning how to program in the instructions.

Did the circuit behave as expected? If no, what was wrong?

It did.

Please comment on the single biggest issue you were facing when simulating the circuit.

The biggest issue I faced was displaying the Controller, Generator, and Brainless values.

Task 4-5: Add the AND, ZERO, SUB, and STORE ACC Instructions

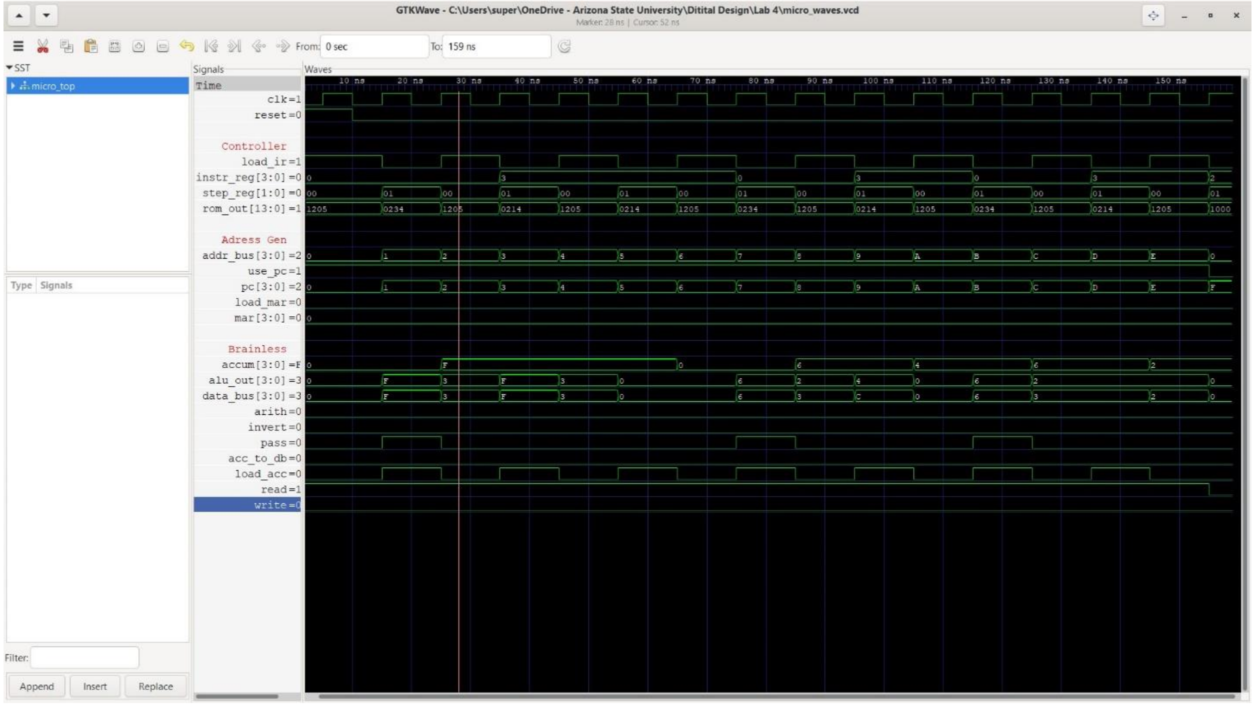
Paste the contents of your final rom_vals here:

```
v2.0 raw

1205 # LOAD ACC; Load IR (0)

0234 #  Load ACC

0000 #  unused

0000 #  unused

1205 # ADD ACC; Load IR (1)

0294 #  ADD

0000 #  unused

0000 #  unused

1205 # STOP; Load IR (2)

1000 #  stay here

0000 #  unused

0000 #  unused

1205 # AND; Load IR (3)

0214 #  Compairs value

0000 #  unused

0000 #  unused
```

```
1205 # ZERO; Load IR (4)
00D8 #  Uses the current acc for subtraction
0000 #  unused
0000 #  unused
1205 # SUB; Load IR (5)
02D4 # Uses the selected value for subtraction
0000 #  unused
0000 #  unused
1205 # STORE ACC; Load IR (6)
2304 #  Selects the desired address
000A #  Stores into ram
0000 #  unused
1205 # DOUBLE; Load IR (7)
0098 #  Adds the accumulation to itself
0000 #  unused
3FFF
```

Test your instructions by writing and executing programs. Paste the contents of your ram_vals.txt file for each program. Note which instruction or instructions each program tests.

Include a picture of your AND waveforms here:


GTKWave - C:\Users\super\OneDrive - Arizona State University\Ditital Design\Lab 4\micro_waves.vcd

Marker: 28 ns | Cursor: 52 ns

From: 0 sec To: 159 ns

0

F

3

F

3

0

0

6

3

C

0

6

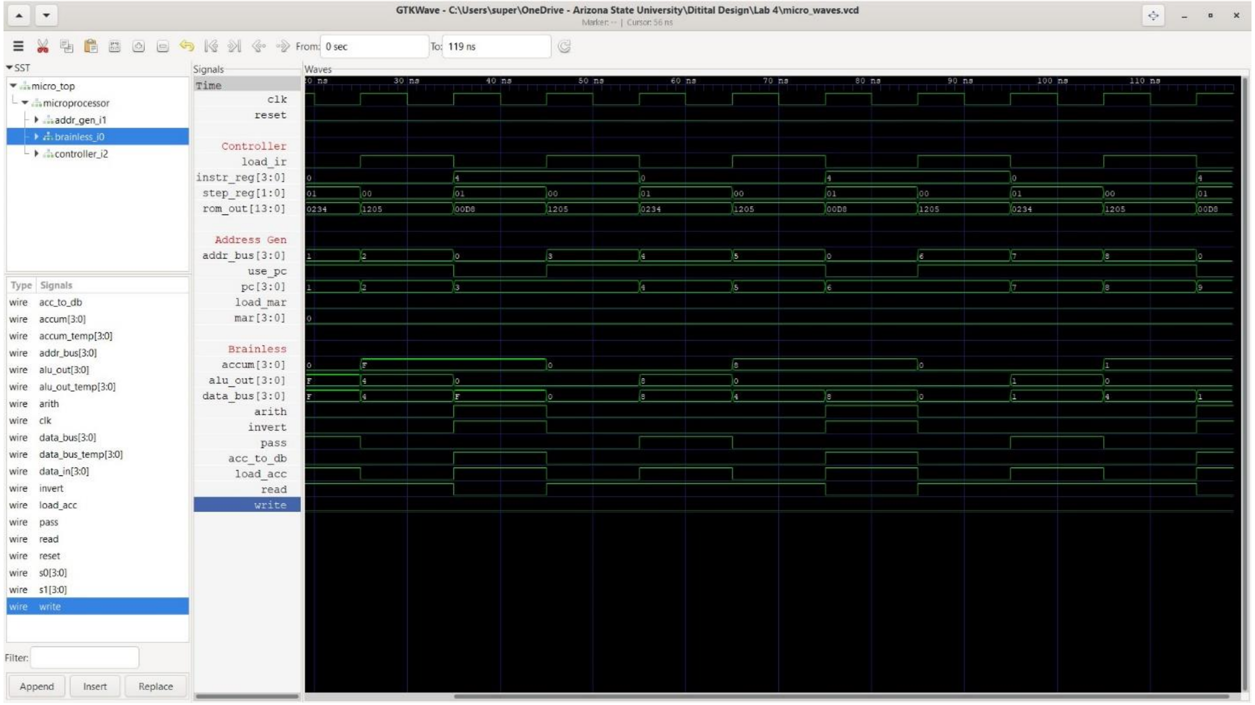
3

3

2

0

Include a picture of your ZERO waveforms here:



GTKWave - C:\Users\super\OneDrive - Arizona State University\Ditital Design\Lab 4\micro_waves.vcd

Marker: -- | Cursor: 56 ns

From: 0 sec To: 119 ns

0

F

4

0

8

4

0

1

4

2

0

0

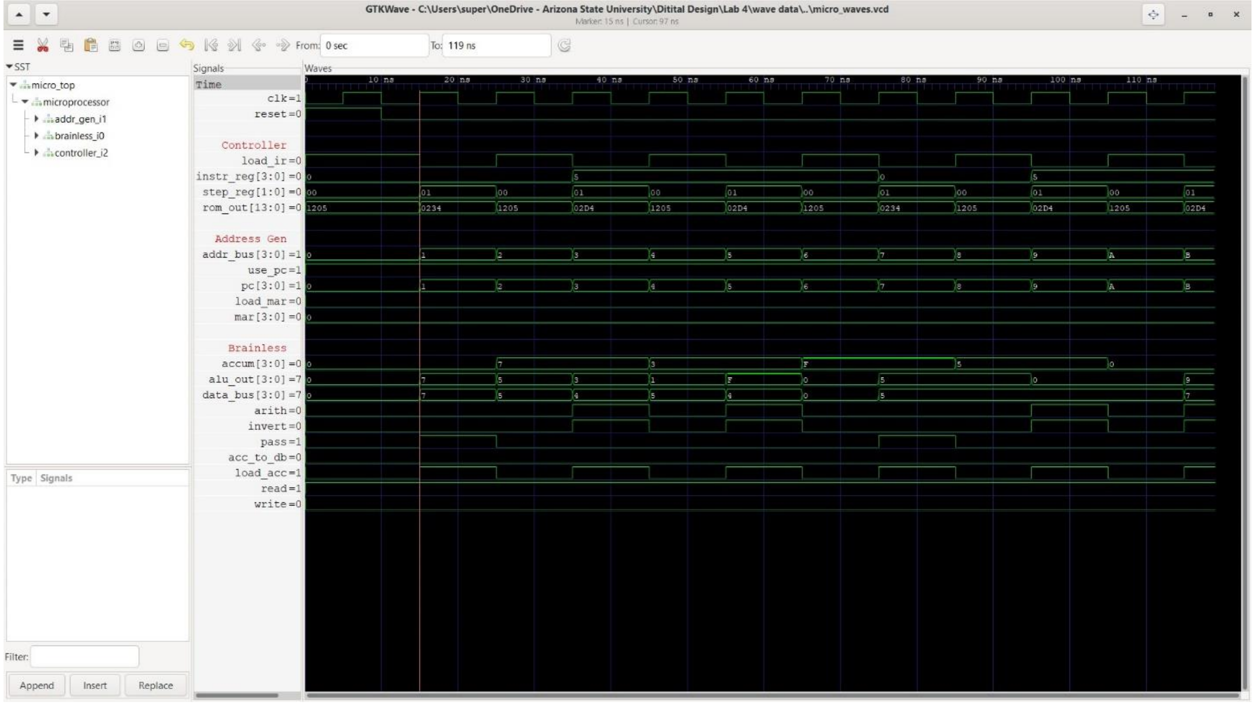
0

0

0

0

Include a picture of your SUB waveforms here:



GTKWave - C:\Users\super\OneDrive - Arizona State University\Ditital Design\Lab 4\wave data\..\micro_waves.vcd

Marker: 15 ns | Cursor: 97 ns

From: 0 sec To: 119 ns

clk=1
reset=0

Controller
load_ir=0
instr_reg[3:0]=0
step_reg[1:0]=0
rom_out[13:0]=0

Address Gen
addr_bus[3:0]=1
use_pc=1
pc[3:0]=1
load_mar=0
mar[3:0]=0

Brainless
accum[3:0]=0
alu_out[3:0]=7
data_bus[3:0]=7
arith=0
invert=0
pass=1
acc_to_db=0
load_acc=1
read=1
write=0

0

7

5

4

5

4

0

5

5

5

5

7

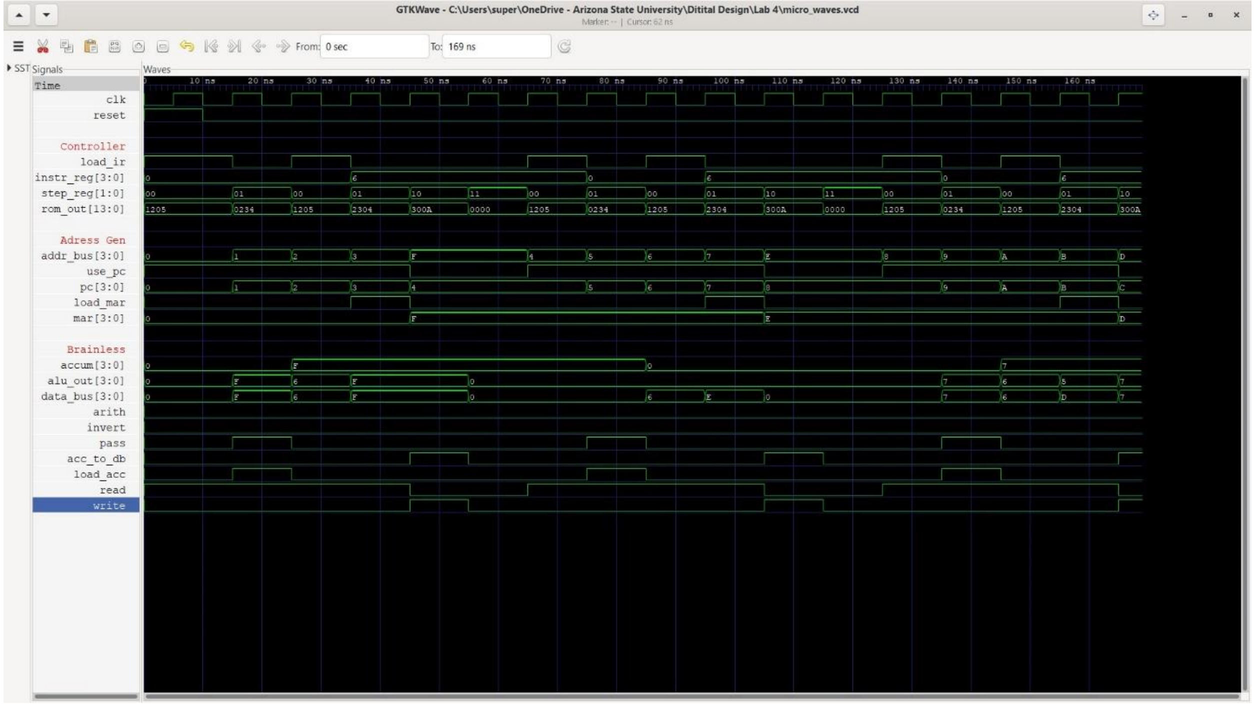
2

0

0

0

Include a picture of your STORE ACC waveforms here:



0

F

6

F

0

0

6

E

0

7

6

D

2

0

0

0

Did the circuit behave as expected? If no, what was wrong?

No, solely due to how I needed to spam the clock to get the results.

Please comment on the single biggest issue you were facing when simulating the circuit.

The biggest issue I had was keeping the ram text organized enough for me to read and alter.

Task 4-6: Invent Your Own Instruction (Extra Credit)

Place the contents of the rom_vals for the extra credit instruction here:

1205 # DOUBLE; Load IR (7)

0098 # Adds the accumulation to itself

0000 # unused

3FFF

Include your Verilog ram_vals.text program used to test the extra credit instruction here:

7

0

1

7

7

0

F

7

7

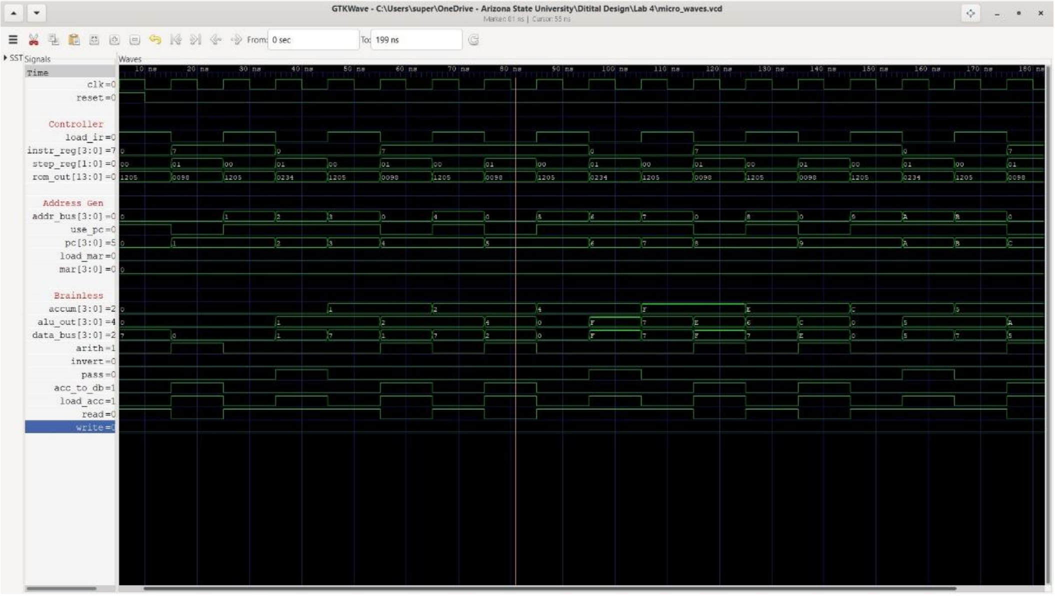
0

5

7

2

Include a picture of your waveforms here:

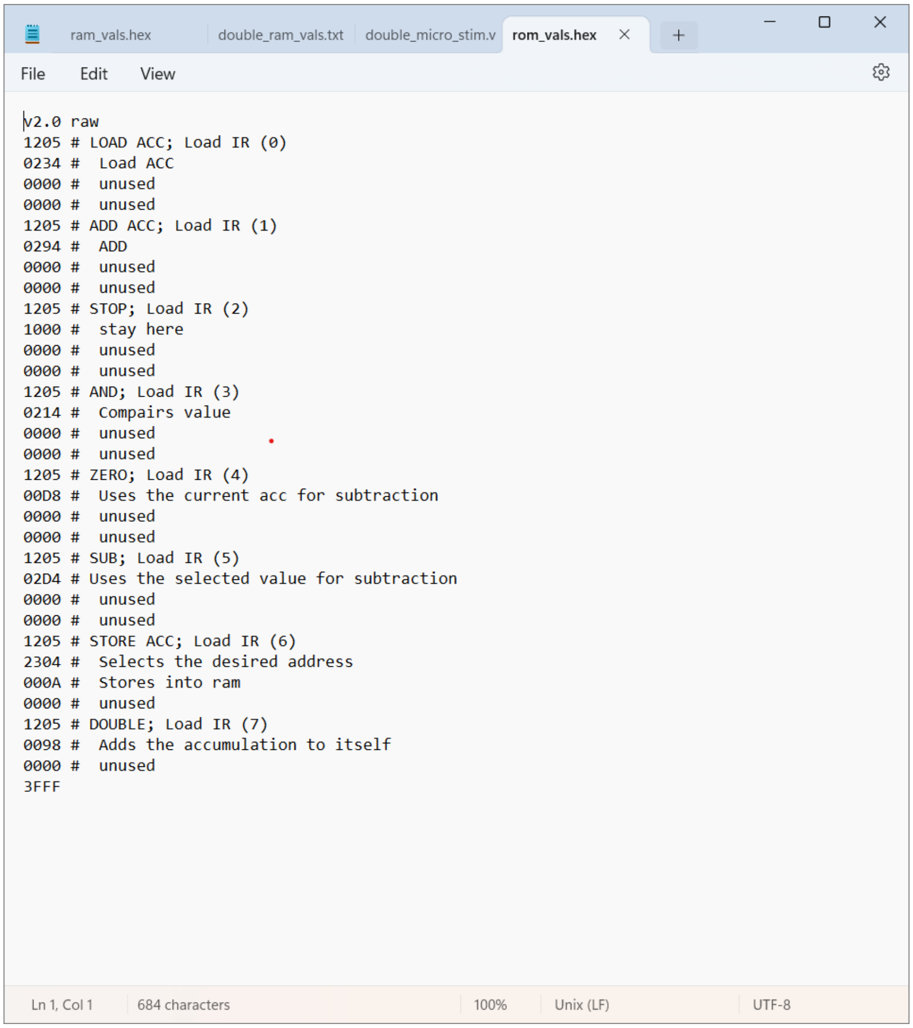


GTKWave - C:\Users\super\OneDrive - Arizona State University\Ditital Design\Lab 4\micro_waves.vcd

Marker: 81 ns | Cursor: 55 ns

From: 0 sec To: 199 ns

Include a picture of your ROM contents here:



```
v2.0 raw
1205 # LOAD ACC; Load IR (0)
0234 #  Load ACC
0000 #  unused
0000 #  unused
1205 # ADD ACC; Load IR (1)
0294 #  ADD
0000 #  unused
0000 #  unused
1205 # STOP; Load IR (2)
1000 #  stay here
0000 #  unused
0000 #  unused
1205 # AND; Load IR (3)
0214 #  Compairs value
0000 #  unused
0000 #  unused
1205 # ZERO; Load IR (4)
00D8 #  Uses the current acc for subtraction
0000 #  unused
0000 #  unused
1205 # SUB; Load IR (5)
02D4 # Uses the selected value for subtraction
0000 #  unused
0000 #  unused
1205 # STORE ACC; Load IR (6)
2304 #  Selects the desired address
000A #  Stores into ram
0000 #  unused
1205 # DOUBLE; Load IR (7)
0098 #  Adds the accumulation to itself
0000 #  unused
3FFF
```

Task 4-7: Create a video and submit your report

Record a short video showing your schematics in Digital and your waveforms in GTKWave. Be sure to show yourself in the video and show your screen. Explain how your circuit works – you need to convince the grader you did the lab and understand it! **Copy and paste the link to your video below. Make sure the link is working and pointing to the correct video. Remember to include the password if required. Do NOT upload your video to Canvas. It is recommended that you use Zoom to record to the cloud, pasting the link and password below.** If your circuit is not working as expected, explain in the video how it is not working and why you think it is not working.

Video Link: https://asu.zoom.us/rec/share/2MpQRPA8Sy-zobJMJvOi4_jfG1tu0tiwGMAvBFYqLIno1NK9Z63b2pqhX86q9CZ6.olGwhdNPu5lCAFRE?startTime=1712298602000

Passcode: 5@ZefQMT

At the beginning of your recording, say your name and the lab name. Be brief in your recording. Submit the completed template to Canvas.

Make sure all your files are in the Lab2 directory. Create a zip file of the Lab2 directory. Remember to turn in the zip file and your completed template on Canvas!

Do not include the video in the zip file! This makes the file very large and you run the risk of the zip file not uploading or taking so long to upload that your submission will be late. Remember that the submission is dated at the time the upload completes, not when it starts!

LAB 4: LAB REPORT GRADE SHEET

Name: ______________________________

NOTE: You submit the zip file in order to show your work.
If the zip file is not submitted there is a 5 point deduction!

Instructor Assessment

Grading Criteria	**Max Points**	**Points Lost**
Description of Assigned Tasks, Work Performed & Outcomes Met		
Task 4-1: Build and Test the Memory-Address-Generation Circuit	10	
Task 4-2: Build and Test the Controller Circuit	10	
Task 4-3: Build the Complete Microprocessor Circuit	10	
Task 4-4: Write and Execute a Simple Program for Your Microprocessor in Simulation	10	
Task 4-5: Add the 'AND', 'Zero', 'Subtract', and 'Store ACC' Instructions	30	
Task 4-6: Invent Your Own Instruction (Extra Credit)	10	
Task 4-7: Record your video	10	
Lab Score (80 points total)	**Points Lost**	
	Late Lab	
	Lab Score	