

CSE/EEE 120
Lab 1 Answer Sheet

Half Adder, Full Adder, 4-bit Incrementer and Adder

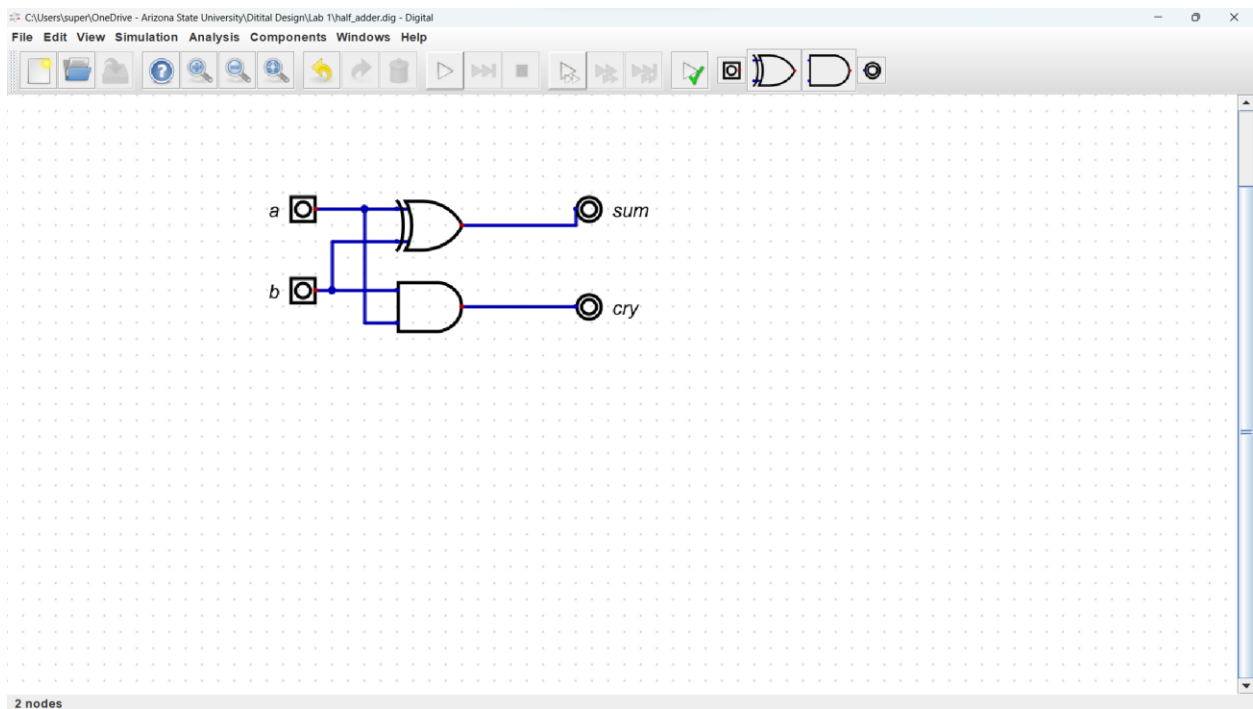
Name: El Hadji Bane

Instructor/Time: Doctor Steve @ 10:30 Tuesday & Thursday

Date: 02/08/2024

Task 1-1: Build and Test the 1-Bit Half-Adder

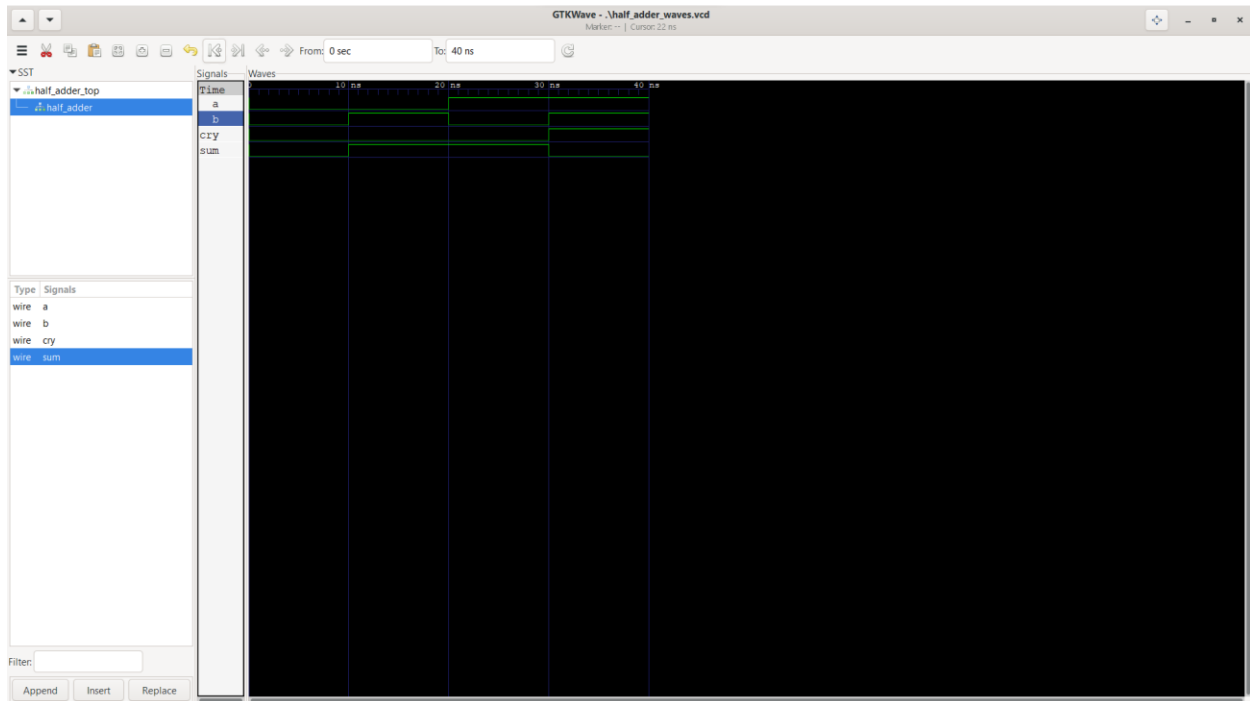
Include a picture of your circuit in Digital here:



Please comment on the single biggest issue you were facing when designing the circuit.

The biggest issue I faced with this design is understanding what gates I should use.

Include a picture of your waveform (timing diagram) here:



Did the circuit behave as expected? If no, what was wrong?

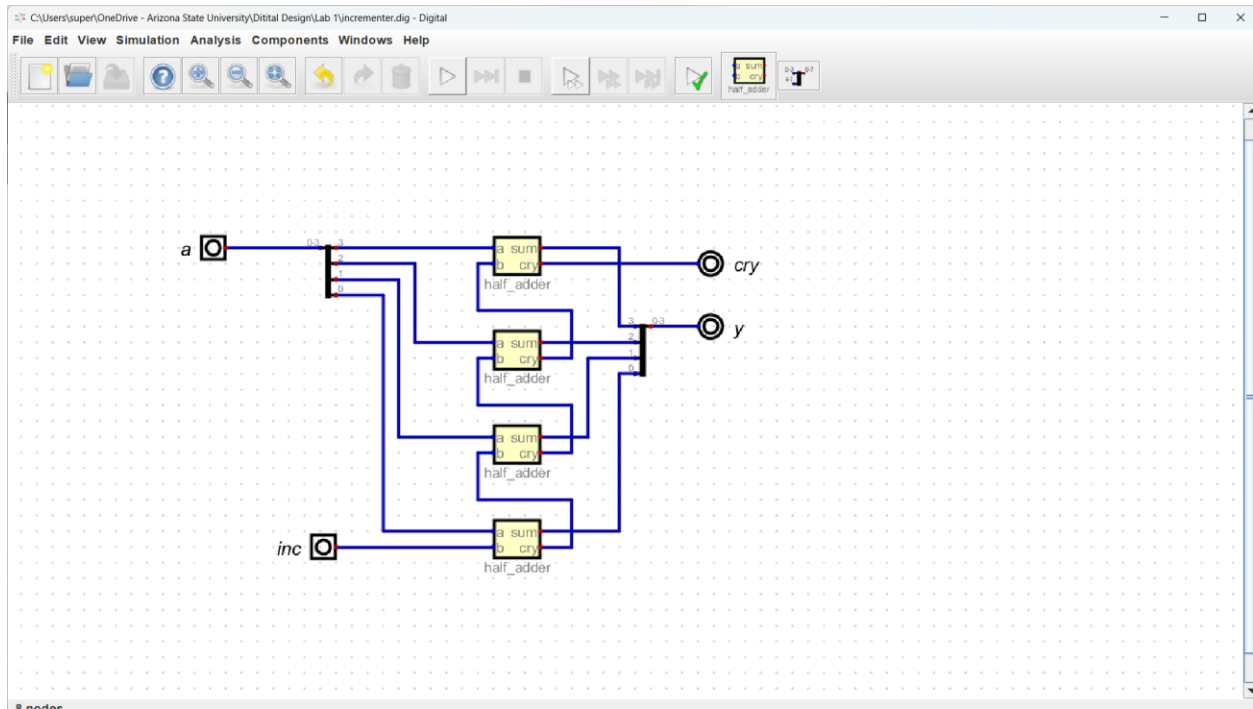
The circuit behaved as expected.

Please comment on the single biggest issue you were facing when simulating the circuit.

The biggest issue was trying to memorize the method to run the simulation.

Task 1-2: Build and Test a 4-Bit Increment Circuit

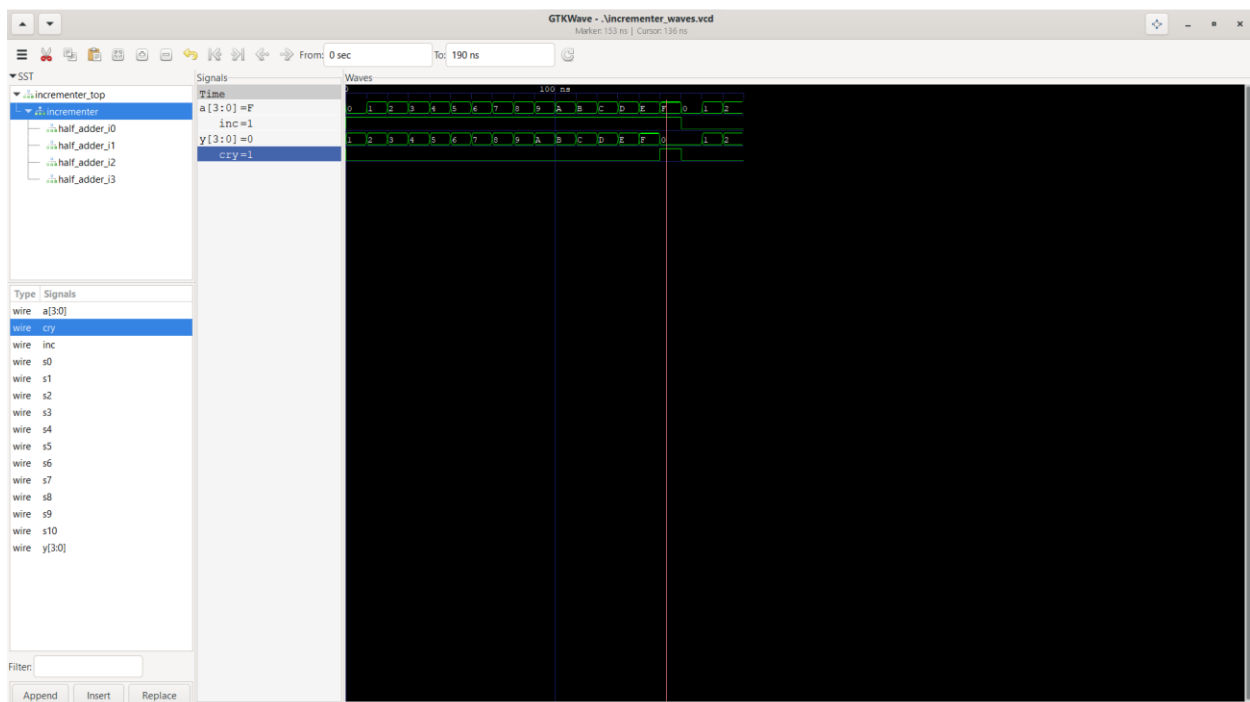
Include a picture of your circuit in Digital here:



Please comment on the single biggest issue you were facing when designing the circuit.

The biggest issue I faced was trying to understand how the splitter/merger works.

Include a picture of your waveform (timing diagram) here:



Did the circuit behave as expected? If no, what was wrong?

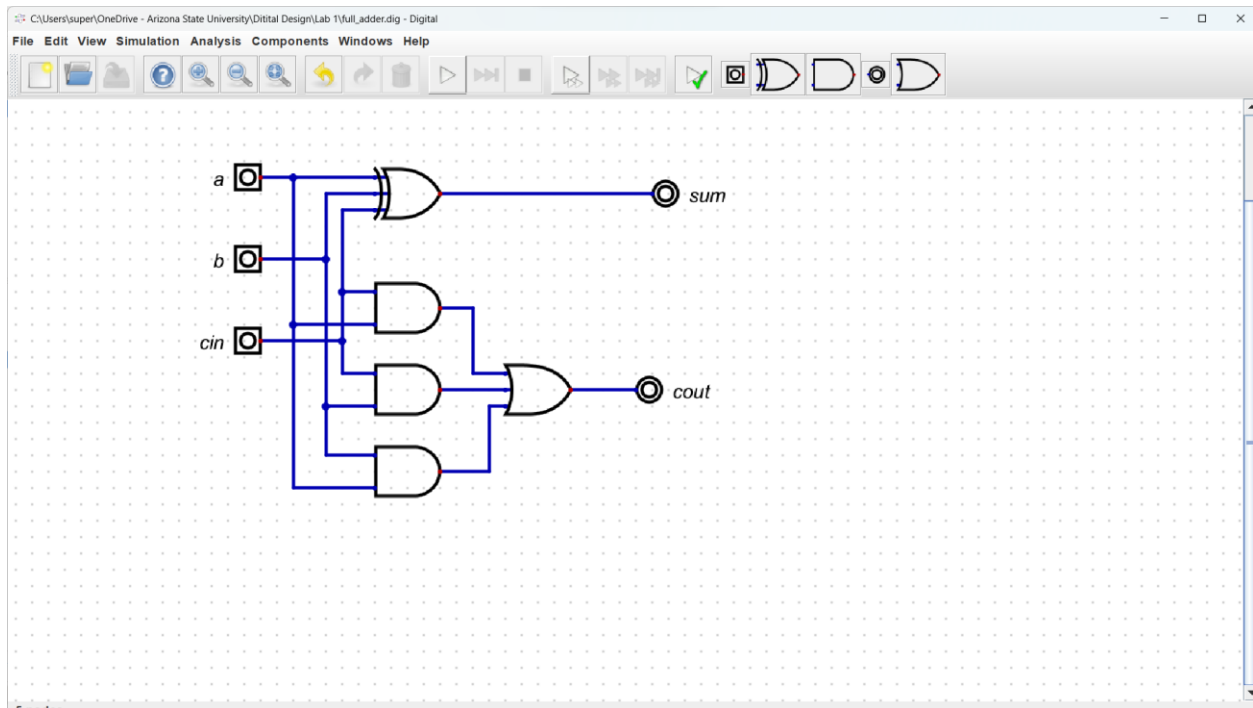
The circuit behaved as expected.

Please comment on the single biggest issue you were facing when simulating the circuit.

Like the wave simulation issues before, I still struggle with memorizing the commands and understanding what the commands specifically do.

Task 1-3: Build and Test a 1-bit Full Adder

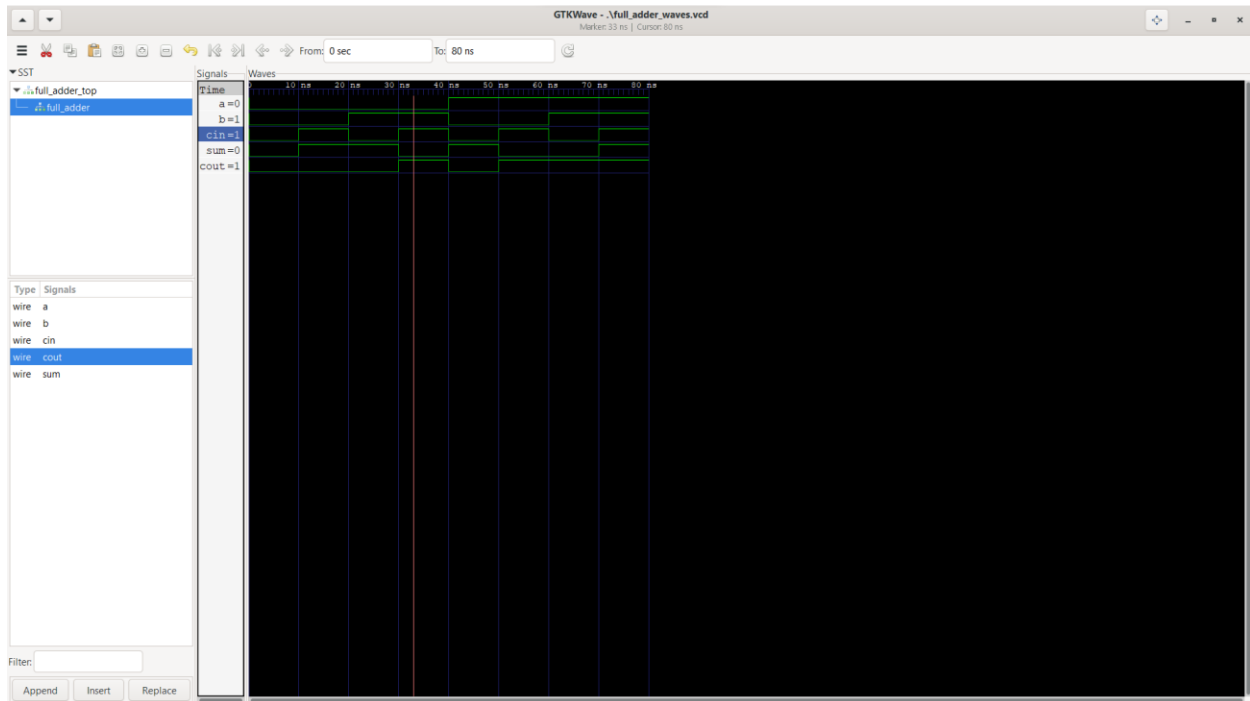
Include a picture of your circuit in Digital here:



Please comment on the single biggest issue you were facing when designing the circuit.

An issue I faced was keeping track of what should be connected to what.

Include a picture of your waveform (timing diagram) here:



Did the circuit behave as expected? If no, what was wrong?

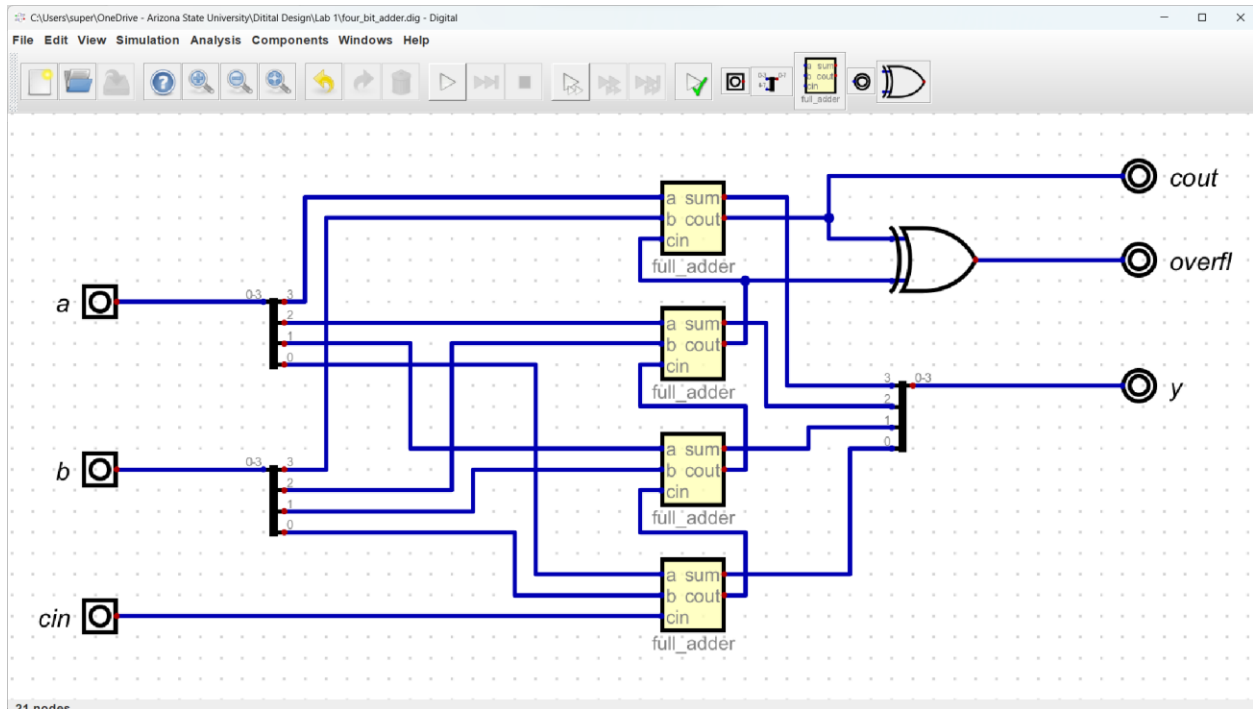
It behave as expected.

Please comment on the single biggest issue you were facing when simulating the circuit.

The issue I had was understanding the data since more inputs are getting involved.

Task 1-4: Build and Test a 4-Bit Full Adder

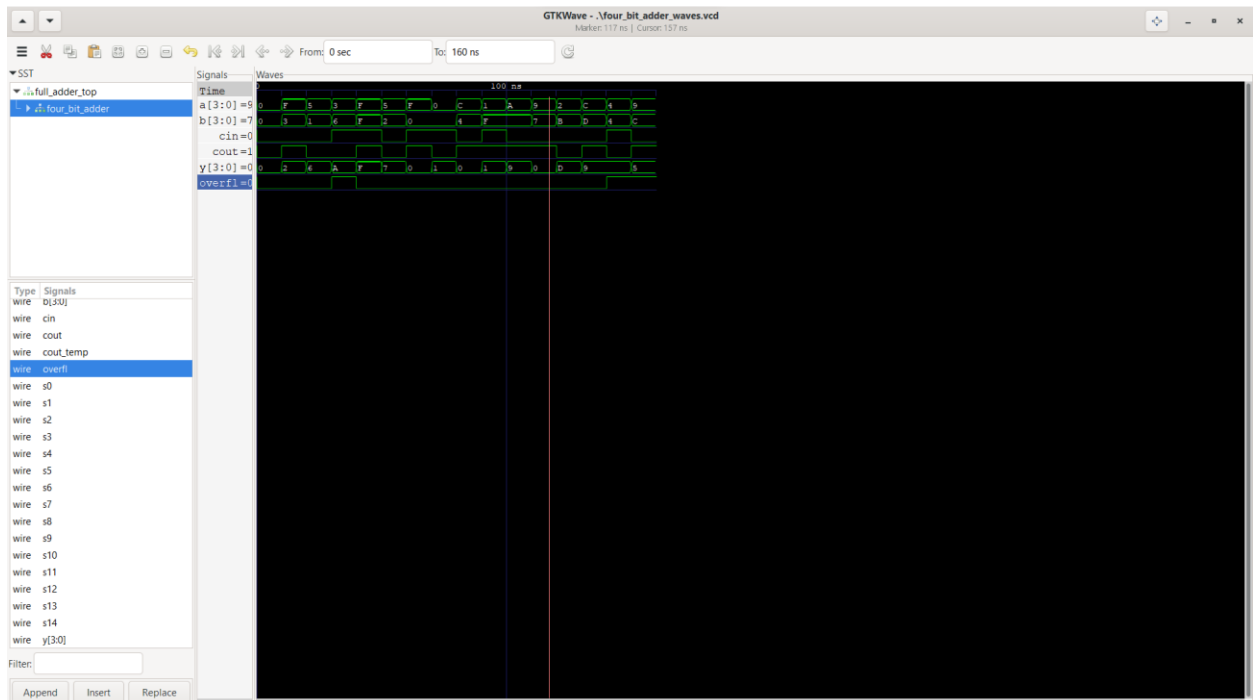
Include a picture of your circuit in Digital here:



Please comment on the single biggest issue you were facing when designing the circuit.

The biggest issue I had with making the design was making sure the components and wires were semi-uniform and neat.

Include a picture of your waveform (timing diagram) here:



Which tests did you perform and why? Use the following table to describe your test sequence. You need to make sure to perform a sufficient number of tests to check the circuit for eventual faults. Each row of the first column corresponds to a row of stimulus from your four_bit_adder_stim.txt file. Note that you only need to use as many tests as needed. Extra space is provided for enthusiastic students.

Test stimulus	Test motivation	Pass/Fail
0_0_0_0_0	Check for stuck-at-1 faults (this makes sure none of the wires were accidentally connected to power)	Pass
1_2_0_F_3	Determining if adding a larger positive number by a small negative number would result in the predicted sum.	Pass
0_6_0_5_1	Tests the design's ability to perform a standard addition problem.	Pass
2_A_1_3_6	Tests the design's ability to detect an overflow when there isn't a cout.	Pass
1_F_1_F_F	Tests the design's ability to add 2 negative numbers with a cin of 1 and get the appropriate sum.	Pass
0_7_0_5_2	Tests the design when the sum is almost an overflow.	Pass
1_0_1_F_0	Tests the design's ability to detect an overflow when 0 is an addon and cin is 1.	Pass
0_1_1_0_0	Tests the design's ability to get the appropriate sum when both addons are 0 and the cin is 1.	Pass
1_0_0_C_4	Tests the design's ability to get the appropriate sum when there's a cout.	Pass
1_1_1_1_F	Tests the design's ability to get the appropriate sum when the addons are complemented and the cin is 1.	Pass
1_9_0_A_F	Tests the design's ability to add 2 negative numbers with a cin of 0 and get the appropriate sum.	Pass
1_0_0_9_7	Tests the design's ability to get the appropriate sum when the addons are complemented and the cin is 0.	Pass

Test stimulus	Test motivation	Pass/Fail
0_D_0_2_B	Determining if adding a larger negative number by a small positive number would result in the predicted sum.	Pass
1_9_0_C_D	Tests the design's ability to produce the appropriate sum when adding 2 negative numbers that almost cause an overflow.	Pass
2_9_1_4_4	Tests the design's ability to detect an overflow with the predicted sum when cin is 1.	Pass
3_5_0_9_C	Tests the design's ability to detect an overflow despite their being a cout value.	Pass

Please comment on the single biggest issue you were facing when simulating the circuit.

The biggest issue I faced was creating a system for translating my test stimulus idea to the text file format.

Task 1-5: Create a video and submit your report.

Record a short video showing your schematics in Digital and your waveforms in GTKWave. Be sure to show yourself in the video and show your screen. Explain how your circuit works – you need to convince the grader you did the lab and understand it! **Copy and paste the link to your video below. Make sure the link is working and pointing to the correct video. Remember to include the password if required. Do NOT upload your video to Canvas. It is recommended that you use Zoom to record to the cloud, pasting the link and password below.** If your circuit is not working as expected, explain in the video how it is not working and why you think it is not working.

Video Link:

https://asu.zoom.us/rec/share/xDVNAnx9eD5i8NT2A2hSh4doNPWoP2fp9ZMg7rV7rD41X2a0eY1TK_tsXSl6abcx.RTzzM9YQDexd6LK0

Passcode: tHiJ2M?9

At the beginning of your recording, say your name and the lab name. Be brief in your recording. Submit the completed template to Canvas.

Make sure all your files are in the Lab1 directory. Create a zip file of the Lab1 directory. Remember to turn in the zip file and your completed template on Canvas!

Do not include the video in the zip file! This makes the file very large and you run the risk of the zip file not uploading or taking so long to upload that your submission will be late. Remember that the submission is dated at the time the upload completes, not when it starts!

LAB 1: LAB REPORT GRADE SHEET

Name _____

NOTE: You submit the zip file in order to show your work.

If the zip file is not submitted there is a 5 point deduction!

Instructor Assessment

Grading Criteria	Max Points	Points Lost
Description of Assigned Tasks, Work Performed & Outcomes Met		
Task 1-1: Build and Test a 1-Bit Half-Adder	10	
Task 1-2: Build and Test a 4-Bit Increment Circuit	10	
Task 1-3: Build and Test a 1-Bit Full Adder	10	
Task 1-4: Build and Test a 4-Bit Full Adder	10	
Task 1-5: Create a video and submit your report.	10	
Lab Score (50 points total)	Points Lost	
	Late Lab	
	Lab Score	