EEE/CSE 120

Capstone Design Project

Name:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Instructor:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Class Time:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Date:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**Task C-1: Planning the Synchronous Sequential Machines**

(5 pts) Interview at least 3 stakeholders, but 3 is preferred. Ask questions regarding the form, function, and features needed by potential customers for this design. Make sure to capture what the customer prefers from this type of solution, as well as what environment the customer plans to use this design. Summarize your findings here and document the names of who you interviewed.

1. **Questions**
   1. When the capstone key fob’s button is pressed while distant from your car, what do you expect the car to do?
   2. Would you rather have the key fob button presses override the auto-locking system or have the auto-locking system override the button presses.
   3. When the button is held for multiple clock cycles, what do you expect the car to do?
2. **Answers**
   1. **Annelise**
      1. beep and stay locked and not flashlights.
      2. button press override auto-locking.
      3. continue to beep or flash until not holding.
   2. **Siri**
      1. Do nothing when far.
      2. Key fob over auto-locking.
      3. Watch for pressing and release to continue normal functioning.
   3. **Aryan**
      1. Will lock.
      2. Button over auto.
      3. The state should be maintained.
   4. **Steve**
      1. do nothing.
      2. auto over button.
      3. register as a single button press.
3. **Findings**:
   1. When distant, the fob should be locked regardless of the button presses.
   2. The button presses should override the auto-locking system.
   3. Holding down the button and releasing should register as a single press.

(5 pts) Please include a comment on why your automation adds value from multiple perspectives (technological, societal, financial, environmental, etc.). (*What value does this add? What is the type of customer for whom this is designed? Where is this most needed? What couldn’t you do before?*)

(5 pts) It is allowable to continue to ask questions of stakeholders throughout the design process (and is preferred of a conscientious engineer). This can be done as you are designing, before you are designing if you need input and clarifications, or after you are done designing if you want feedback on improvements. Summarize any changes to your understanding or design based on the feedback you received during your initial interviews or continual interviews?

* The stakeholders don’t want the car to be unlockable when they press the button.
* The stakeholders want control over the auto-locking.
* The stakeholders consider the press and release as 1 button press.

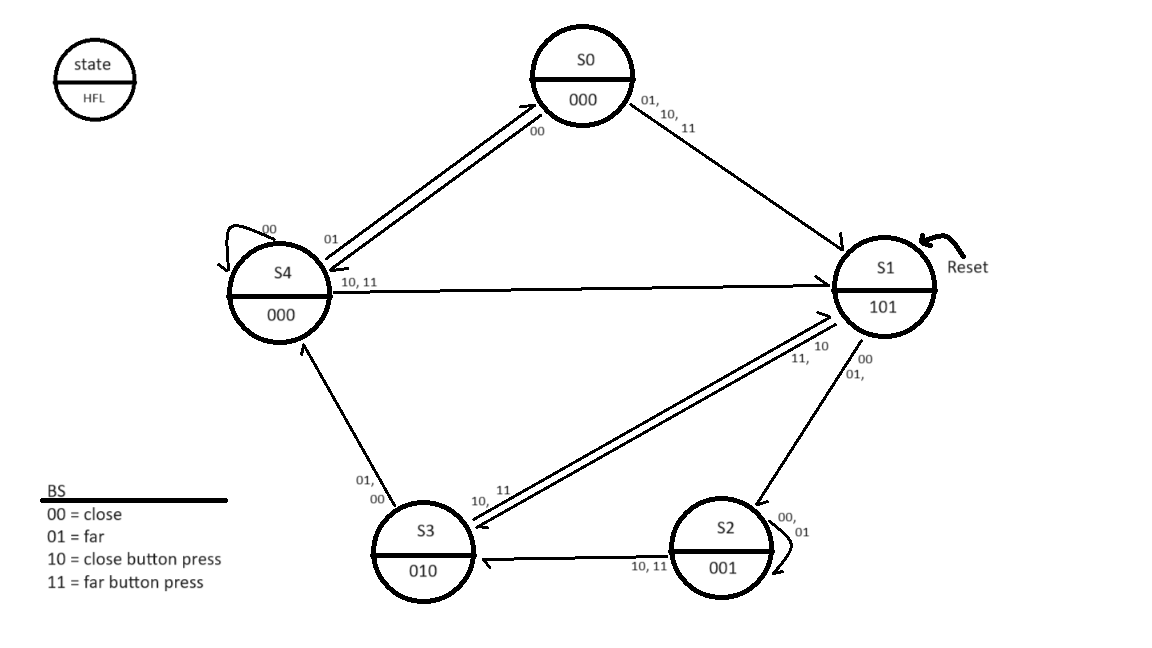
**Task C-2: Document the Synchronous Sequential Machines**

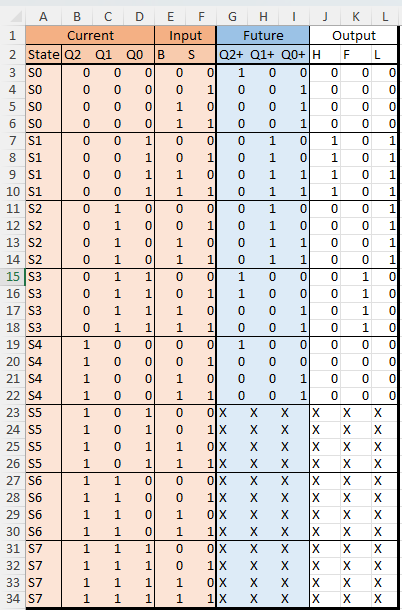
**Design #1:** (2 pts) What assumptions did you make in the design of this machine?

* The car can be unlocked regardless of the distance.
* Button presses are prioritized over the auto-locking.
* The car locks on reset.

(3 pts) Create a state definition table here that describes in plain English what each state in your machine means and what binary values you have assigned to represent each state, inputs, and outputs.

|  |  |  |  |
| --- | --- | --- | --- |
| State | Name | Definition | Binary |
| S0 | Wait | Keeps the car unlocked while watching for auto-locking conditions. | 000 |
| S1 | Locking | Locks and honks the car when the car is initially locked. | 001 |
| S2 | Locked | Keeps the car locked. | 010 |
| S3 | Unlocking | unlocks and flashes the car when the car is initially unlocked. | 011 |
| S4 | Unlocked | Keeps the car unlocked. | 100 |

(12 pts) Show your state diagrams, state transition tables and your circuit planning work (Karnaugh maps/equations/MUX/DEC/etc.) used in your design process. (You can do this by hand if you wish, do **not** show the full circuit schematic here.) 



Single table implicant =

Multi table implicant =

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Q0’ Q2+ | | | | Q0 Q2+ | | | |
| Q1Q2  B S | 00 | 01 | 11 | 10 | 00 | 01 | 11 | 10 |
| 00 | 1 |  | 1 |  | 1 | X | X | X |
| 01 |  |  | 1 |  |  | X | X | X |
| 11 |  |  |  |  |  | X | X | X |
| 10 |  |  |  |  |  | X | X | X |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Q0’ Q1+ | | | | Q0 Q1+ | | | |
| Q1Q2  B S | 00 | 01 | 11 | 10 | 00 | 01 | 11 | 10 |
| 00 |  | 1 |  | 1 |  | X | X | X |
| 01 |  | 1 |  | 1 |  | X | X | X |
| 11 |  | 1 |  | 1 |  | X | X | X |
| 10 |  | 1 |  | 1 |  | X | X | X |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Q0’ Q0+ | | | | Q0 Q0+ | | | |
| Q1Q2  B S | 00 | 01 | 11 | 10 | 00 | 01 | 11 | 10 |
| 00 |  |  |  |  |  | X | X | X |
| 01 | 1 |  |  |  |  | X | X | X |
| 11 | 1 | 1 | 1 | 1 | 1 | X | X | X |
| 10 | 1 | 1 | 1 | 1 | 1 | X | X | X |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Q0’ H | | | | Q0 H | | | |
| Q1Q2  B S | 00 | 01 | 11 | 10 | 00 | 01 | 11 | 10 |
| 00 |  | 1 |  |  |  | X | X | X |
| 01 |  | 1 |  |  |  | X | X | X |
| 11 |  | 1 |  |  |  | X | X | X |
| 10 |  | 1 |  |  |  | X | X | X |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Q0’ F | | | | Q0 F | | | |
| Q1Q2  B S | 00 | 01 | 11 | 10 | 00 | 01 | 11 | 10 |
| 00 |  |  | 1 |  |  | X | X | X |
| 01 |  |  | 1 |  |  | X | X | X |
| 11 |  |  | 1 |  |  | X | X | X |
| 10 |  |  | 1 |  |  | X | X | X |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Q0’ L | | | | Q0 L | | | |
| Q1Q2  B S | 00 | 01 | 11 | 10 | 00 | 01 | 11 | 10 |
| 00 |  | 1 |  | 1 |  | X | X | X |
| 01 |  | 1 |  | 1 |  | X | X | X |
| 11 |  | 1 |  | 1 |  | X | X | X |
| 10 |  | 1 |  | 1 |  | X | X | X |

(3 pts) List your final design equations and required logic gates (including types of Flip Flops) needed to complete this circuit.

* Equations
* Logic gates
  + XOR
  + AND
  + OR
  + D-FLIP FLOP, ASYNCHRONOUS

**Design #2:** (2 pts) What assumptions did you make in the design of this machine?

* The car can be unlocked regardless of the distance.
* The button press can override the wait.
* Holding the button doesn’t trigger a button press.
* The car locks on reset.

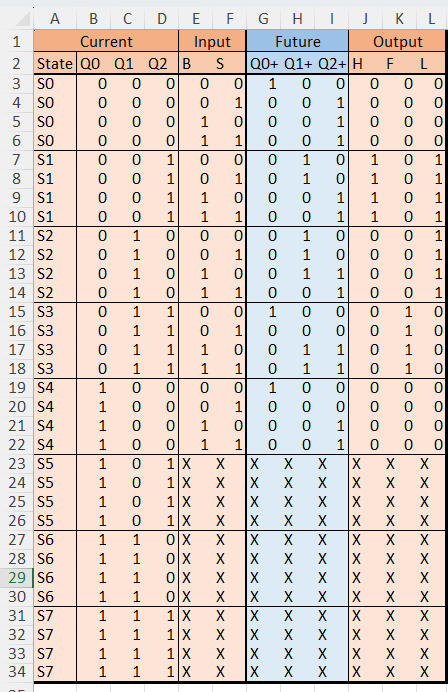
(3 pts) Create a state definition table here that describes in plain English what each state in your machine means and what binary values you have assigned to represent each state.

|  |  |  |  |
| --- | --- | --- | --- |
| State | Name | Definition | Binary |
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| S3 | Unlocking | unlocks and flashes the car when the car is initially unlocked. | 011 |
| S4 | Unlocked | Keeps the car unlocked. | 100 |

(12 pts) Show your state diagrams, state transition tables and your circuit planning work (Karnaugh maps/equations/MUX/DEC/etc.) used in your design process. (You can do this by hand if you wish, do **not** show the full circuit schematic here.)

A diagram of a diagram

Description automatically generated



Single table implicant =

Multi table implicant =

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Q0’ Q2+ | | | | Q0 Q2+ | | | |
| Q1Q2  B S | 00 | 01 | 11 | 10 | 00 | 01 | 11 | 10 |
| 00 |  |  |  |  |  | X | X | X |
| 01 | 1 |  |  |  |  | X | X | X |
| 11 | 1 | 1 | 1 | 1 | 1 | X | X | X |
| 10 | 1 | 1 | 1 | 1 | 1 | X | X | X |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Q0’ Q1+ | | | | Q0 Q1+ | | | |
| Q1Q2  B S | 00 | 01 | 11 | 10 | 00 | 01 | 11 | 10 |
| 00 |  | 1 |  | 1 |  | X | X | X |
| 01 |  | 1 |  | 1 |  | X | X | X |
| 11 |  |  | 1 |  |  | X | X | X |
| 10 |  |  | 1 | 1 |  | X | X | X |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Q0’ Q0+ | | | | Q0 Q0+ | | | |
| Q1Q2  B S | 00 | 01 | 11 | 10 | 00 | 01 | 11 | 10 |
| 00 | 1 |  |  |  |  | X | X | X |
| 01 |  |  |  |  |  | X | X | X |
| 11 |  |  | 1 |  |  | X | X | X |
| 10 |  |  | 1 |  |  | X | X | X |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Q0’ H | | | | Q0 H | | | |
| Q1Q2  B S | 00 | 01 | 11 | 10 | 00 | 01 | 11 | 10 |
| 00 |  | 1 |  |  |  | X | X | X |
| 01 |  | 1 |  |  |  | X | X | X |
| 11 |  | 1 |  |  |  | X | X | X |
| 10 |  | 1 |  |  |  | X | X | X |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Q0’ F | | | | Q0 F | | | |
| Q1Q2  B S | 00 | 01 | 11 | 10 | 00 | 01 | 11 | 10 |
| 00 |  |  | 1 |  |  | X | X | X |
| 01 |  |  | 1 |  |  | X | X | X |
| 11 |  |  | 1 |  |  | X | X | X |
| 10 |  |  | 1 |  |  | X | X | X |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Q0’ L | | | | Q0 L | | | |
| Q1Q2  B S | 00 | 01 | 11 | 10 | 00 | 01 | 11 | 10 |
| 00 |  | 1 |  | 1 |  | X | X | X |
| 01 |  | 1 |  | 1 |  | X | X | X |
| 11 |  | 1 |  | 1 |  | X | X | X |
| 10 |  | 1 |  | 1 |  | X | X | X |

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(3 pts) List your final design equations and required logic gates (including types of Flip Flops) needed to complete this circuit.

**Task C-3: Determine Criteria and Weighting for Judging Your Designs**

(5 pts) Using the guidelines in the laboratory FAQ’s, list your 5 criteria and associated weights here used to help decide between the two design models (weights should add to 100%):

Criteria Weight

**Task C-4: Apply the Criteria to Pick the Best Design**

(2 pts) Describe how you applied each of the criteria and weighting system in the above task to pick the best design. How did you choose these criteria (customer interviews, engineering preference)?

(3 pts) Which design is better based on your criteria and weighting system and why? Please explain how the winning design scored in each category and why (the winning design does not need to score the highest in every category, but it does need to score higher overall when applying the criteria weights).

**Task C-5: Build and Simulate Winning Design in Digital**

(15 pts) Insert a copy of your chosen Digital Schematic here. Please make sure that you have outputs or tunnels connected to each flip flop so that you can easily monitor your states. Make sure that the logic and equations match the final equations presented in either Design 1 or Design 2.

**Task C-6: Record a Video Demonstration of the Winning Design**

(15 pts) Record a video demonstration showing all positions being visited and various combinations of the inputs in Digital. For every clock cycle, explain the inputs, what current state you are in, and point out any outputs that should be noted. Be sure to show what happens for different input combinations at each position. That is, your demonstration should be able to showcase all possible states and transitions required to get there. If you include any asynchronous inputs, make sure to show those features as well. Add a link to your video below. Be sure to include any required password.

**Video link:**

**Task C-7: Fill Out the Self-Assessment and Turn in Your Design**

**There are two items to submit.** Turn in the zip file of your capstone project folder. Also turn in this template once it is filled out. There will be a deduction of 5 points if your template is only found inside the zip folder. The self-assessment is on the next page.

# Self-Assessment Worksheet

Put an ‘X’ in the table below indicating how strongly you agree or disagree that the outcomes of the assigned tasks were achieved. Use ‘5’ to indicate that you ‘strongly agree’ and ‘1’ to indicate that you ‘strongly disagree’. Use ‘NA’, Not Applicable, when the tasks you performed did not elicit this outcome. Credit will be given for including this worksheet with your lab report. However, your **responses will not be graded**, they are for your instructor’s information only.

**Table 1: Self-Assessment of Outcomes for the Capstone Design Project Lab.**

| **After completing the assigned tasks and report I am able to:** | **5** | **4** | **3** | **2** | **1** | **NA** |
| --- | --- | --- | --- | --- | --- | --- |
| Initiate a design process based on a value proposition and feedback from various stakeholders. |  |  |  |  |  |  |
| Make assumptions to complete an incomplete functional specification. |  |  |  |  |  |  |
| Use classical design techniques (i.e., state diagrams, state transition tables, and Karnaugh Maps), to design a synchronous sequential machine starting with a functional specification. |  |  |  |  |  |  |
| Build, and debug a synchronous sequential machine. |  |  |  |  |  |  |
| Develop reasonable engineering criteria for comparing different designs. |  |  |  |  |  |  |
| Apply engineering criteria to select a ‘best’ design. |  |  |  |  |  |  |

Write below any suggestions you have for improving this laboratory exercise so that the stated learning outcomes are achieved.

# Capstone Design Project: Lab Report Grade Sheet

**Name:**

| **Grading Criteria** | **Max Points** | **Points lost** |
| --- | --- | --- |
| **Template** |  |  |
| Neatness, Clarity, and Concision | 5 |  |
| **Description of Assigned Tasks, Work Performed & Outcomes Met** |  |  |
| Task C-1: Planning the Synchronous Sequential Machines | 15 |  |
| Task C-2: Document the Synchronous Sequential Machines | 40 |  |
| Task C-3: Determine Criteria and Weighting for Judging Your Designs | 5 |  |
| Task C-4: Apply the Criteria to Pick the Best Design | 5 |  |
| Task C-5: Build and Simulate Winning Design in Digital | 15 |  |
| Task C-6: Record a Video Demonstration of the Winning Design | 15 |  |
| **Self-Assessment Worksheet** (The content of the self-assessment worksheet will not be graded. Full credit is given for including the completed worksheet.) | (2 extra points) |  |
|  | **Points Lost** |  |
| **Lab Score** | **Late Lab** |  |
|  | **Lab Score** |  |