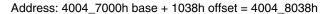
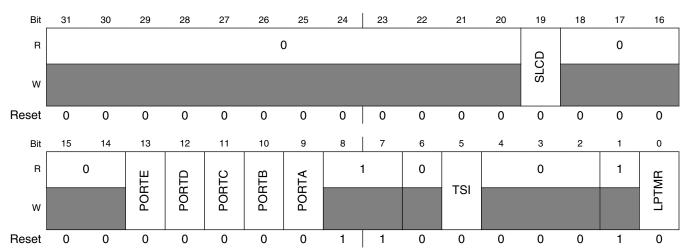


12.2.9 System Clock Gating Control Register 5 (SIM_SCGC5)





SIM_SCGC5 field descriptions

Field	Description
31–20 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
19 SLCD	Segment LCD Clock Gate Control This bit controls the clock gate to the Segment LCD module. Clock disabled Clock enabled
18–14 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
13 PORTE	Port E Clock Gate Control This bit controls the clock gate to the Port E module. O Clock disabled 1 Clock enabled
12 PORTD	Port D Clock Gate Control Controls the clock gate to the Port D module. 0 Clock disabled 1 Clock enabled
11 PORTC	Port C Clock Gate Control This bit controls the clock gate to the Port C module. 0 Clock disabled 1 Clock enabled

Table continues on the next page...



SIM_SCGC5 field descriptions (continued)

Field	Description
10 PORTB	Port B Clock Gate Control
-	Controls the clock gate to the Port B module.
	0 Clock disabled
	1 Clock enabled
9 PORTA	Port A Clock Gate Control
	Controls the clock gate to the Port A module.
	0 Clock disabled
	1 Clock enabled
8–7 Reserved	This field is reserved. This read-only field is reserved and always has the value 1.
6	This field is reserved.
Reserved	This read-only field is reserved and always has the value 0.
5 TSI	TSI Access Control
131	This bit controls software access to the TSI module.
	0 Access disabled
	1 Access enabled
4–2	This field is reserved.
Reserved 1	This read-only field is reserved and always has the value 0. This field is reserved.
Reserved	This field is reserved. This read-only field is reserved and always has the value 1.
0 LPTMR	Low Power Timer Access Control
	This bit controls software access to the Low Power Timer module.
	0 Access disabled
	1 Access enabled