

Chapter 31

Timer/PWM Module (TPM)

31.1 Introduction

The TPM (Timer/PWM Module) is a two to eight channel timer which supports input capture, output compare, and the generation of PWM signals to control electric motor and power management applications. The counter, compare and capture registers are clocked by an asynchronous clock that can remain enabled in low power modes.

31.1.1 TPM Philosophy

The TPM is built upon a very simple timer (HCS08 Timer PWM Module – TPM) used for many years on Freescale's 8-bit microcontrollers. The TPM extends the functionality to support operation in low power modes by clocking the counter, compare and capture registers from an asynchronous clock that can remain functional in low power modes.

31.1.2 Features

The TPM features include:

- TPM clock mode is selectable
 - Can increment on every edge of the asynchronous counter clock
 - Can increment on rising edge of an external clock input synchronized to the asynchronous counter clock
- Prescaler divide-by 1, 2, 4, 8, 16, 32, 64, or 128
- TPM includes a 16-bit counter

- It can be a free-running counter or modulo counter
- The counting can be up or up-down
- Includes 6 channels that can be configured for input capture, output compare, or edge-aligned PWM mode
 - In input capture mode the capture can occur on rising edges, falling edges or both edges
 - In output compare mode the output signal can be set, cleared, pulsed, or toggled on match
 - All channels can be configured for center-aligned PWM mode
- Support the generation of an interrupt and/or DMA request per channel
- Support the generation of an interrupt and/or DMA request when the counter overflows
- Support selectable trigger input to optionally reset or cause the counter to start incrementing.
 - The counter can also optionally stop incrementing on counter overflow
- Support the generation of hardware triggers when the counter overflows and per channel

31.1.3 Modes of Operation

During debug mode, the TPM can be configured to temporarily pause all counting until the core returns to normal user operating mode or to operate normally. When the counter is paused, trigger inputs and input capture events are ignored.

During doze mode, the TPM can be configured to operate normally or to pause all counting for the duration of doze mode. When the counter is paused, trigger inputs and input capture events are ignored.

During stop mode, the TPM counter clock can remain functional and the TPM can generate an asynchronous interrupt to exit the MCU from stop mode.

31.1.4 Block Diagram

The TPM uses one input/output (I/O) pin per channel, CH_n (TPM channel (n)) where n is the channel number.

The following figure shows the TPM structure. The central component of the TPM is the 16-bit counter with programmable final value and its counting can be up or up-down.

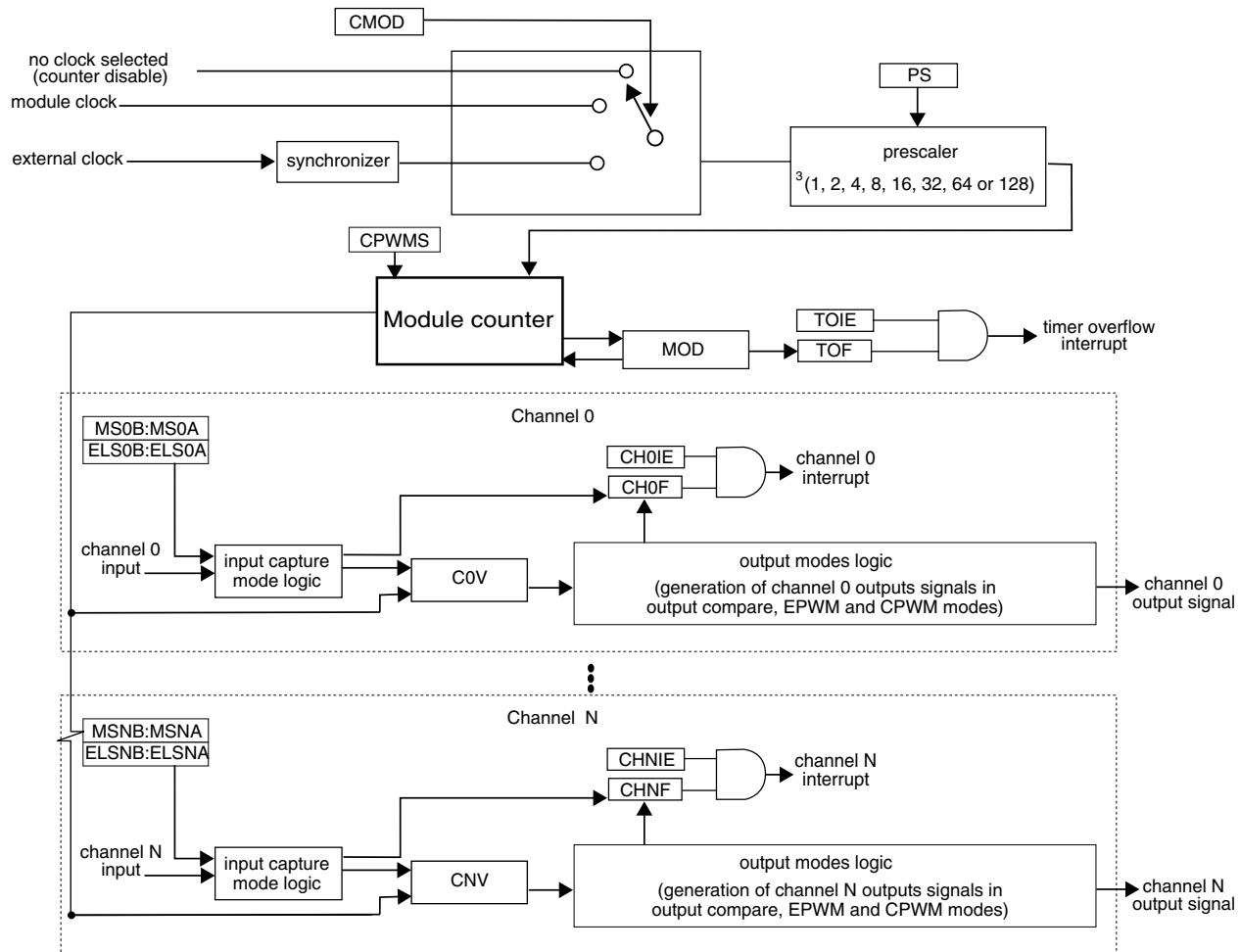


Figure 31-1. TPM block diagram

31.2 TPM Signal Descriptions

Table 31-1 shows the user-accessible signals for the TPM.

Table 31-1. TPM signal descriptions

Signal	Description	I/O
TPM_EXTCLK	External clock. TPM external clock can be selected to increment the TPM counter on every rising edge synchronized to the counter clock.	I
TPM_CHn	TPM channel (n = 5 to 0)	I/O

31.2.1 TPM_EXTCLK — TPM External Clock

The rising edge of the external input signal is used to increment the TPM counter if selected by CMOD[1:0] bits in the SC register. This input signal must be less than half of the TPM counter clock frequency. The TPM counter prescaler selection and settings are also used when an external input is selected.

31.2.2 TPM_CHn — TPM Channel (n) I/O Pin

Each TPM channel can be configured to operate either as input or output. The direction associated with each channel, input or output, is selected according to the mode assigned for that channel.

31.3 Memory Map and Register Definition

This section provides a detailed description of all TPM registers.

Attempting to access a reserved register location in the TPM memory map will generate a bus error.

TPM memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/page
4003_8000	Status and Control (TPM0_SC)	32	R/W	0000_0000h	31.3.1/566
4003_8004	Counter (TPM0_CNT)	32	R/W	0000_0000h	31.3.2/567
4003_8008	Modulo (TPM0_MOD)	32	R/W	0000_FFFFh	31.3.3/568
4003_800C	Channel (n) Status and Control (TPM0_C0SC)	32	R/W	0000_0000h	31.3.4/569
4003_8010	Channel (n) Value (TPM0_C0V)	32	R/W	0000_0000h	31.3.5/571
4003_8014	Channel (n) Status and Control (TPM0_C1SC)	32	R/W	0000_0000h	31.3.4/569
4003_8018	Channel (n) Value (TPM0_C1V)	32	R/W	0000_0000h	31.3.5/571
4003_801C	Channel (n) Status and Control (TPM0_C2SC)	32	R/W	0000_0000h	31.3.4/569
4003_8020	Channel (n) Value (TPM0_C2V)	32	R/W	0000_0000h	31.3.5/571
4003_8024	Channel (n) Status and Control (TPM0_C3SC)	32	R/W	0000_0000h	31.3.4/569
4003_8028	Channel (n) Value (TPM0_C3V)	32	R/W	0000_0000h	31.3.5/571
4003_802C	Channel (n) Status and Control (TPM0_C4SC)	32	R/W	0000_0000h	31.3.4/569
4003_8030	Channel (n) Value (TPM0_C4V)	32	R/W	0000_0000h	31.3.5/571
4003_8034	Channel (n) Status and Control (TPM0_C5SC)	32	R/W	0000_0000h	31.3.4/569
4003_8038	Channel (n) Value (TPM0_C5V)	32	R/W	0000_0000h	31.3.5/571
4003_8050	Capture and Compare Status (TPM0_STATUS)	32	R/W	0000_0000h	31.3.6/571
4003_8084	Configuration (TPM0_CONF)	32	R/W	0000_0000h	31.3.7/573

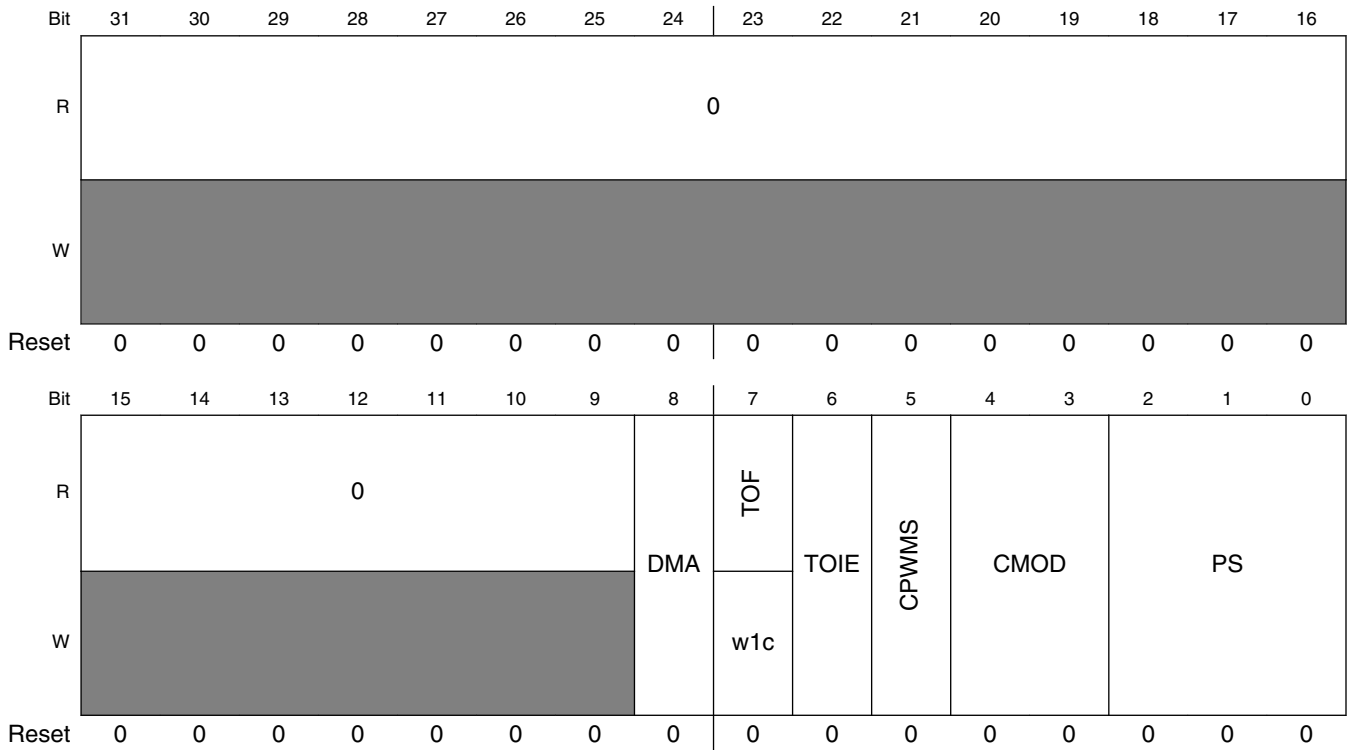
TPM memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4003_9000	Status and Control (TPM1_SC)	32	R/W	0000_0000h	31.3.1/566
4003_9004	Counter (TPM1_CNT)	32	R/W	0000_0000h	31.3.2/567
4003_9008	Modulo (TPM1_MOD)	32	R/W	0000_FFFFh	31.3.3/568
4003_900C	Channel (n) Status and Control (TPM1_C0SC)	32	R/W	0000_0000h	31.3.4/569
4003_9010	Channel (n) Value (TPM1_C0V)	32	R/W	0000_0000h	31.3.5/571
4003_9014	Channel (n) Status and Control (TPM1_C1SC)	32	R/W	0000_0000h	31.3.4/569
4003_9018	Channel (n) Value (TPM1_C1V)	32	R/W	0000_0000h	31.3.5/571
4003_901C	Channel (n) Status and Control (TPM1_C2SC)	32	R/W	0000_0000h	31.3.4/569
4003_9020	Channel (n) Value (TPM1_C2V)	32	R/W	0000_0000h	31.3.5/571
4003_9024	Channel (n) Status and Control (TPM1_C3SC)	32	R/W	0000_0000h	31.3.4/569
4003_9028	Channel (n) Value (TPM1_C3V)	32	R/W	0000_0000h	31.3.5/571
4003_902C	Channel (n) Status and Control (TPM1_C4SC)	32	R/W	0000_0000h	31.3.4/569
4003_9030	Channel (n) Value (TPM1_C4V)	32	R/W	0000_0000h	31.3.5/571
4003_9034	Channel (n) Status and Control (TPM1_C5SC)	32	R/W	0000_0000h	31.3.4/569
4003_9038	Channel (n) Value (TPM1_C5V)	32	R/W	0000_0000h	31.3.5/571
4003_9050	Capture and Compare Status (TPM1_STATUS)	32	R/W	0000_0000h	31.3.6/571
4003_9084	Configuration (TPM1_CONF)	32	R/W	0000_0000h	31.3.7/573
4003_A000	Status and Control (TPM2_SC)	32	R/W	0000_0000h	31.3.1/566
4003_A004	Counter (TPM2_CNT)	32	R/W	0000_0000h	31.3.2/567
4003_A008	Modulo (TPM2_MOD)	32	R/W	0000_FFFFh	31.3.3/568
4003_A00C	Channel (n) Status and Control (TPM2_C0SC)	32	R/W	0000_0000h	31.3.4/569
4003_A010	Channel (n) Value (TPM2_C0V)	32	R/W	0000_0000h	31.3.5/571
4003_A014	Channel (n) Status and Control (TPM2_C1SC)	32	R/W	0000_0000h	31.3.4/569
4003_A018	Channel (n) Value (TPM2_C1V)	32	R/W	0000_0000h	31.3.5/571
4003_A01C	Channel (n) Status and Control (TPM2_C2SC)	32	R/W	0000_0000h	31.3.4/569
4003_A020	Channel (n) Value (TPM2_C2V)	32	R/W	0000_0000h	31.3.5/571
4003_A024	Channel (n) Status and Control (TPM2_C3SC)	32	R/W	0000_0000h	31.3.4/569
4003_A028	Channel (n) Value (TPM2_C3V)	32	R/W	0000_0000h	31.3.5/571
4003_A02C	Channel (n) Status and Control (TPM2_C4SC)	32	R/W	0000_0000h	31.3.4/569
4003_A030	Channel (n) Value (TPM2_C4V)	32	R/W	0000_0000h	31.3.5/571
4003_A034	Channel (n) Status and Control (TPM2_C5SC)	32	R/W	0000_0000h	31.3.4/569
4003_A038	Channel (n) Value (TPM2_C5V)	32	R/W	0000_0000h	31.3.5/571
4003_A050	Capture and Compare Status (TPM2_STATUS)	32	R/W	0000_0000h	31.3.6/571
4003_A084	Configuration (TPM2_CONF)	32	R/W	0000_0000h	31.3.7/573

31.3.1 Status and Control (TPMx_SC)

SC contains the overflow status flag and control bits used to configure the interrupt enable, module configuration and prescaler factor. These controls relate to all channels within this module.

Address: Base address + 0h offset



TPMx_SC field descriptions

Field	Description
31–9 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
8 DMA	DMA Enable Enables DMA transfers for the overflow flag. 0 Disables DMA transfers. 1 Enables DMA transfers.
7 TOF	Timer Overflow Flag Set by hardware when the TPM counter equals the value in the MOD register and increments. The TOF bit is cleared by writing a 1 to TOF bit. Writing a 0 to TOF has no effect. If another LPTPM overflow occurs between the flag setting and the flag clearing, the write operation has no effect; therefore, TOF remains set indicating another overflow has occurred. In this case a TOF interrupt request is not lost due to a delay in clearing the previous TOF.

Table continues on the next page...

TPMx_SC field descriptions (continued)

Field	Description
	0 TPM counter has not overflowed. 1 TPM counter has overflowed.
6 TOIE	Timer Overflow Interrupt Enable Enables TPM overflow interrupts. 0 Disable TOF interrupts. Use software polling or DMA request. 1 Enable TOF interrupts. An interrupt is generated when TOF equals one.
5 CPWMS	Center-aligned PWM Select Selects CPWM mode. This mode configures the TPM to operate in up-down counting mode. This field is write protected. It can be written only when the counter is disabled. 0 TPM counter operates in up counting mode. 1 TPM counter operates in up-down counting mode.
4–3 CMOD	Clock Mode Selection Selects the TPM counter clock modes. When disabling the counter, this field remain set until acknowledged in the TPM clock domain. 00 TPM counter is disabled 01 TPM counter increments on every TPM counter clock 10 TPM counter increments on rising edge of TPM_EXTCLK synchronized to the TPM counter clock 11 Reserved
2–0 PS	Prescale Factor Selection Selects one of 8 division factors for the clock mode selected by CMOD. This field is write protected. It can be written only when the counter is disabled. 000 Divide by 1 001 Divide by 2 010 Divide by 4 011 Divide by 8 100 Divide by 16 101 Divide by 32 110 Divide by 64 111 Divide by 128

31.3.2 Counter (TPMx_CNT)

The CNT register contains the TPM counter value.

Reset clears the CNT register. Writing any value to COUNT also clears the counter.

When debug is active, the TPM counter does not increment unless configured otherwise.

Reading the CNT register adds two wait states to the register access due to synchronization delays.

memory Map and Register Definition

Address: Base address + 4h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																COUNT															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TPMx_CNT field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
15–0 COUNT	Counter value

31.3.3 Modulo (TPMx_MOD)

The Modulo register contains the modulo value for the TPM counter. When the TPM counter reaches the modulo value and increments, the overflow flag (TOF) is set and the next value of TPM counter depends on the selected counting method (see [Counter](#)).

Writing to the MOD register latches the value into a buffer. The MOD register is updated with the value of its write buffer according to [MOD Register Update](#) . Additional writes to the MOD write buffer are ignored until the register has been updated.

It is recommended to initialize the TPM counter (write to CNT) before writing to the MOD register to avoid confusion about when the first counter overflow will occur.

Address: Base address + 8h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																MOD															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

TPMx_MOD field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
15–0 MOD	Modulo value When writing this field, all bytes must be written at the same time.

31.3.4 Channel (n) Status and Control (TPMx_CnSC)

CnSC contains the channel-interrupt-status flag and control bits used to configure the interrupt enable, channel configuration, and pin function. When switching from one channel mode to a different channel mode, the channel must first be disabled and this must be acknowledged in the TPM counter clock domain.

Table 31-34. Mode, Edge, and Level Selection

CPWMS	MSnB:MSnA	ELSnB:ELSnA	Mode	Configuration
X	00	00	None	Channel disabled
X	01	00	Software compare	Pin not used for TPM
0	00	01	Input capture	Capture on Rising Edge Only
		10		Capture on Falling Edge Only
		11		Capture on Rising or Falling Edge
	01	01	Output compare	Toggle Output on match
		10		Clear Output on match
		11		Set Output on match
	10	10	Edge-aligned PWM	High-true pulses (clear Output on match, set Output on reload)
		X1		Low-true pulses (set Output on match, clear Output on reload)
	11	10	Output compare	Pulse Output low on match
		01		Pulse Output high on match
1	10	10	Center-aligned PWM	High-true pulses (clear Output on match-up, set Output on match-down)
		01		Low-true pulses (set Output on match-up, clear Output on match-down)

Address: Base address + Ch offset + (8d × i), where i=0d to 5d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Memory Map and Register Definition

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								CHF	CHIE	MSB	MSA	ELSB	ELSA	0	DMA
W									w1c							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TPMx_CnSC field descriptions

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7 CHF	Channel Flag Set by hardware when an event occurs on the channel. CHF is cleared by writing a 1 to the CHF bit. Writing a 0 to CHF has no effect. If another event occurs between the CHF sets and the write operation, the write operation has no effect; therefore, CHF remains set indicating another event has occurred. In this case a CHF interrupt request is not lost due to the delay in clearing the previous CHF. 0 No channel event has occurred. 1 A channel event has occurred.
6 CHIE	Channel Interrupt Enable Enables channel interrupts. 0 Disable channel interrupts. 1 Enable channel interrupts.
5 MSB	Channel Mode Select Used for further selections in the channel logic. Its functionality is dependent on the channel mode. When a channel is disabled, this bit will not change state until acknowledged in the TPM counter clock domain.
4 MSA	Channel Mode Select Used for further selections in the channel logic. Its functionality is dependent on the channel mode. When a channel is disabled, this bit will not change state until acknowledged in the TPM counter clock domain.
3 ELSB	Edge or Level Select The functionality of ELSB and ELSA depends on the channel mode. When a channel is disabled, this bit will not change state until acknowledged in the TPM counter clock domain.
2 ELSA	Edge or Level Select The functionality of ELSB and ELSA depends on the channel mode. When a channel is disabled, this bit will not change state until acknowledged in the TPM counter clock domain.
1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 DMA	DMA Enable Enables DMA transfers for the channel. 0 Disable DMA transfers. 1 Enable DMA transfers.

31.3.5 Channel (n) Value (TPMx_CnV)

These registers contain the captured TPM counter value for the input modes or the match value for the output modes.

In input capture mode, any write to a CnV register is ignored.

In compare modes, writing to a CnV register latches the value into a buffer. A CnV register is updated with the value of its write buffer according to [CnV Register Update](#) . Additional writes to the CnV write buffer are ignored until the register has been updated.

Address: Base address + 10h offset + (8d × i), where i=0d to 5d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																VAL															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TPMx_CnV field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
15–0 VAL	Channel Value Captured TPM counter value of the input modes or the match value for the output modes. When writing this field, all bytes must be written at the same time.

31.3.6 Capture and Compare Status (TPMx_STATUS)

The STATUS register contains a copy of the status flag CHnF bit (in CnSC) for each TPM channel, as well as the TOF bit (in SC), for software convenience.

Each CHnF bit in STATUS is a mirror of CHnF bit in CnSC. All CHnF bits can be checked using only one read of STATUS. All CHnF bits can be cleared by writing all ones to STATUS.

Hardware sets the individual channel flags when an event occurs on the channel. CHF is cleared by writing a 1 to the CHF bit. Writing a 0 to CHF has no effect.

If another event occurs between the flag setting and the write operation, the write operation has no effect; therefore, CHF remains set indicating another event has occurred. In this case a CHF interrupt request is not lost due to the clearing sequence for a previous CHF.

memory Map and Register Definition

Address: Base address + 50h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0							TOF	0		CH5F	CH4F	CH3F	CH2F	CH1F	CH0F
W								w1c			w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TPMx_STATUS field descriptions

Field	Description
31–9 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
8 TOF	Timer Overflow Flag See register description 0 TPM counter has not overflowed. 1 TPM counter has overflowed.
7–6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5 CH5F	Channel 5 Flag See the register description. 0 No channel event has occurred. 1 A channel event has occurred.
4 CH4F	Channel 4 Flag See the register description. 0 No channel event has occurred. 1 A channel event has occurred.
3 CH3F	Channel 3 Flag See the register description. 0 No channel event has occurred. 1 A channel event has occurred.

Table continues on the next page...

TPMx_STATUS field descriptions (continued)

Field	Description
2 CH2F	Channel 2 Flag See the register description. 0 No channel event has occurred. 1 A channel event has occurred.
1 CH1F	Channel 1 Flag See the register description. 0 No channel event has occurred. 1 A channel event has occurred.
0 CH0F	Channel 0 Flag See the register description. 0 No channel event has occurred. 1 A channel event has occurred.

31.3.7 Configuration (TPMx_CONF)

This register selects the behavior in debug and wait modes and the use of an external global time base.

Address: Base address + 84h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
R	0				TRGSEL					0					CROT	CSOO	CSOT
W																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0						GTBEEN	0	DBGMODE		DOZEEN	0				
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TPMx_CONF field descriptions

Field	Description
31–28 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

Table continues on the next page...

TPMx_CONF field descriptions (continued)

Field	Description
27–24 TRGSEL	<p>Trigger Select</p> <p>Selects the input trigger to use for starting the counter and/or reloading the counter. This field should only be changed when the TPM counter is disabled. See Chip configuration section for available options.</p>
23–19 Reserved	<p>This field is reserved.</p> <p>This read-only field is reserved and always has the value 0.</p>
18 CROT	<p>Counter Reload On Trigger</p> <p>When set, the TPM counter will reload with zero (and initialize PWM outputs to their default value) when a rising edge is detected on the selected trigger input.</p> <p>The trigger input is ignored if the TPM counter is paused during debug mode or doze mode. This field should only be changed when the TPM counter is disabled.</p> <p>0 Counter is not reloaded due to a rising edge on the selected input trigger 1 Counter is reloaded when a rising edge is detected on the selected input trigger</p>
17 CSOO	<p>Counter Stop On Overflow</p> <p>When set, the TPM counter will stop incrementing once the counter equals the MOD value and incremented (this also sets the TOF). Reloading the counter with zero due to writing to the counter register or due to a trigger input does not cause the counter to stop incrementing. Once the counter has stopped incrementing, the counter will not start incrementing unless it is disabled and then enabled again, or a rising edge on the selected trigger input is detected when CSOT set.</p> <p>This field should only be changed when the TPM counter is disabled.</p> <p>0 TPM counter continues incrementing or decrementing after overflow 1 TPM counter stops incrementing or decrementing after overflow.</p>
16 CSOT	<p>Counter Start on Trigger</p> <p>When set, the TPM counter will not start incrementing after it is enabled until a rising edge on the selected trigger input is detected. If the TPM counter is stopped due to an overflow, a rising edge on the selected trigger input will also cause the TPM counter to start incrementing again.</p> <p>The trigger input is ignored if the TPM counter is paused during debug mode or doze mode. This field should only be changed when the TPM counter is disabled.</p> <p>0 TPM counter starts to increment immediately, once it is enabled. 1 TPM counter only starts to increment when it a rising edge on the selected input trigger is detected, after it has been enabled or after it has stopped due to overflow.</p>
15–10 Reserved	<p>This field is reserved.</p> <p>This read-only field is reserved and always has the value 0.</p>
9 GTBEEN	<p>Global time base enable</p> <p>Configures the TPM to use an externally generated global time base counter. When an externally generated timebase is used, the internal TPM counter is not used by the channels but can be used to generate a periodic interruptor DMA request using the Modulo register and timer overflow flag.</p> <p>0 All channels use the internally generated TPM counter as their timebase 1 All channels use an externally generated global timebase as their timebase</p>
8 Reserved	<p>This field is reserved.</p> <p>This read-only field is reserved and always has the value 0.</p>
7–6 DBGMODE	<p>Debug Mode</p>

Table continues on the next page...

TPMx_CONF field descriptions (continued)

Field	Description
	Configures the TPM behavior in debug mode. All other configurations are reserved. 00 TPM counter is paused and does not increment during debug mode. Trigger inputs and input capture events are also ignored. 11 TPM counter continues in debug mode.
5 DOZEEN	Doze Enable Configures the TPM behavior in wait mode. 0 Internal TPM counter continues in Doze mode. 1 Internal TPM counter is paused and does not increment during Doze mode. Trigger inputs and input capture events are also ignored.
4–0 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

31.4 Functional Description

The following sections describe the TPM features.

31.4.1 Clock Domains

The TPM module supports two clock domains.

The bus clock domain is used by the register interface and for synchronizing interrupts and DMA requests.

The TPM counter clock domain is used to clock the counter and prescaler along with the output compare and input capture logic. The TPM counter clock is considered asynchronous to the bus clock, can be a higher or lower frequency than the bus clock and can remain operational in Stop mode. Multiple TPM instances are all clocked by the same TPM counter clock in support of the external timebase feature.

31.4.1.1 Counter Clock Mode

The CMOD[1:0] bits in the SC register either disable the TPM counter or select one of two possible clock modes for the TPM counter. After any reset, CMOD[1:0] = 0:0 so the TPM counter is disabled.

The CMOD[1:0] bits may be read or written at any time. Disabling the TPM counter by writing zero to the CMOD[1:0] bits does not affect the TPM counter value or other registers, but must be acknowledged by the TPM counter clock domain before they read as zero.

The external clock input passes through a synchronizer clocked by the TPM counter clock to assure that counter transitions are properly aligned to counter clock transitions. Therefore, to meet Nyquist criteria considering also jitter, the frequency of the external clock source must be less than half of the counter clock frequency.

31.4.2 Prescaler

The selected counter clock source passes through a prescaler that is a 7-bit counter. The value of the prescaler is selected by the PS[2:0] bits. The following figure shows an example of the prescaler counter and TPM counter.

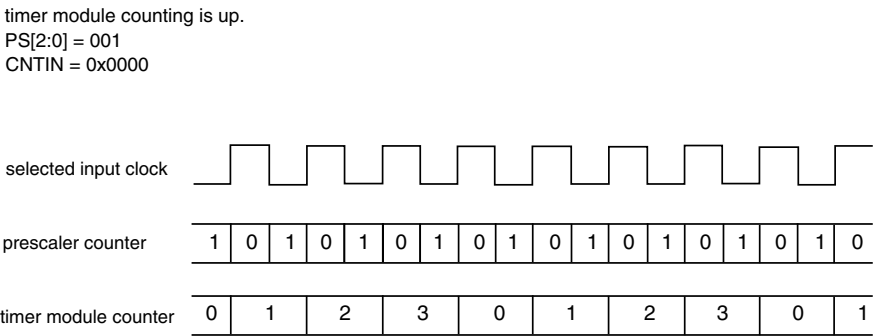


Figure 31-78. Example of the Prescaler Counter

31.4.3 Counter

The TPM has a 16-bit counter that is used by the channels either for input or output modes. The counter updates from the selected clock divided by the prescaler.

The TPM counter has these modes of operation:

- up counting (see [Up Counting](#))
- up-down counting (see [Up-Down Counting](#))

31.4.3.1 Up Counting

Up counting is selected when (CPWMS = 0)

The value of zero is loaded into the TPM counter, and the counter increments until the value of MOD is reached, at which point the counter is reloaded with zero.

The TPM period when using up counting is $(MOD + 0x0001) \times \text{period of the TPM counter clock}$.

The TOF bit is set when the TPM counter changes from MOD to zero.

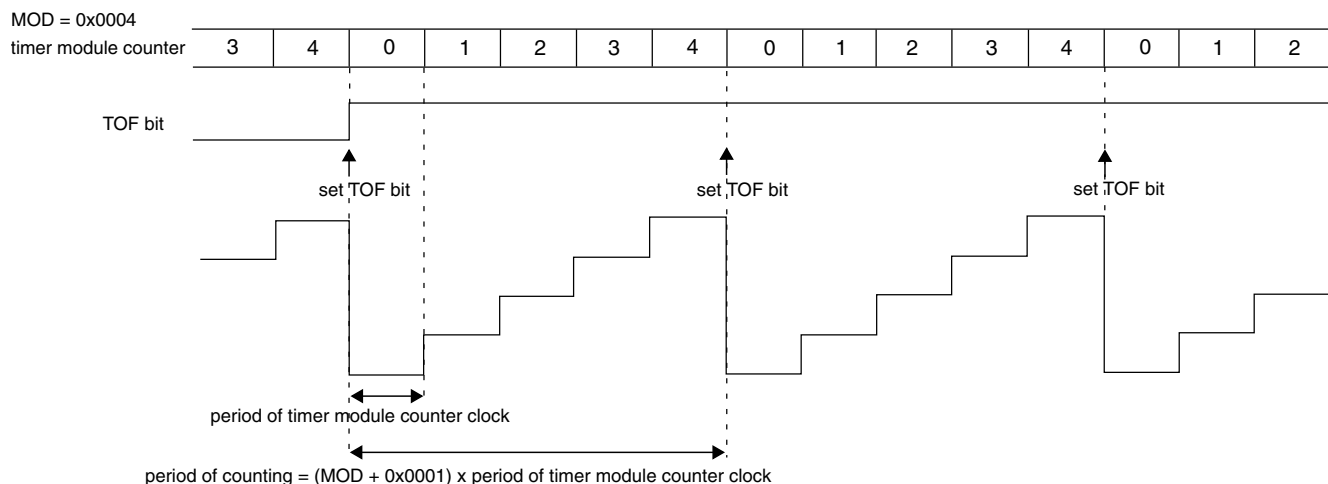


Figure 31-79. Example of TPM Up Counting

Note

- MOD = 0000 is a redundant condition. In this case, the TPM counter is always equal to MOD and the TOF bit is set in each rising edge of the TPM counter clock.

31.4.3.2 Up-Down Counting

Up-down counting is selected when (CPWMS = 1). When configured for up-down counting, configuring MOD to less than 2 is not supported.

The value of zero is loaded into the TPM counter, and the counter increments until the value of MOD is reached, at which point the counter is decremented until it returns to zero and the up-down counting restarts.

The TPM period when using up-down counting is $2 \times MOD \times \text{period of the TPM counter clock}$.

The TOF bit is set when the TPM counter changes from MOD to (MOD – 1).

Functional Description

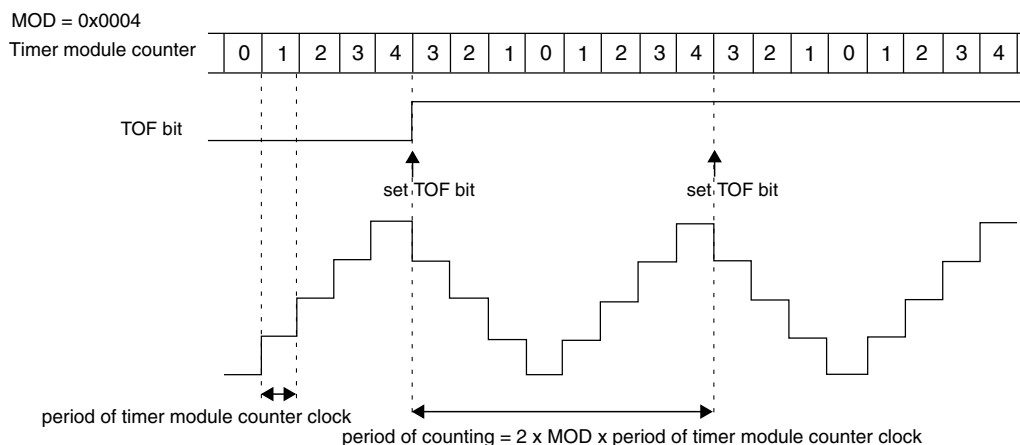


Figure 31-80. Example of Up-Down Counting

31.4.3.3 Counter Reset

Any write to CNT resets the TPM counter and the channel outputs to their initial values (except for channels in output compare mode).

31.4.3.4 Global time base (GTB)

The global time base (GTB) is a TPM function that allows multiple TPM modules to share the same timebase. When the global time base is enabled (GTBEEN = 1), the local TPM channels use the counter value, counter enable and overflow indication from the TPM generating the global time base. If the local TPM counter is not generating the global time base, then it can be used as an independent counter or pulse accumulator.

31.4.3.5 Counter trigger

The TPM counter can be configured to start, stop or reset in response to a hardware trigger input. The trigger input is synchronized to the asynchronous counter clock, so there is a 3 counter clock delay between the trigger assertion and the counter responding.

- When (CSOT = 1), the counter will not start incrementing until a rising edge is detected on the trigger input.
- When (CSOO = 1), the counter will stop incrementing whenever the TOF flag is set. The counter does not increment again unless it is disabled, or if CSOT = 1 and a rising edge is detected on the trigger input.
- When (CROT = 1), the counter will reset to zero as if an overflow occurred whenever a rising edge is detected on the trigger input.

31.4.4 Input Capture Mode

The input capture mode is selected when ($CPWMS = 0$), ($MSnB:MSnA = 0:0$), and ($ELSnB:ELSnA \neq 0:0$).

When a selected edge occurs on the channel input, the current value of the TPM counter is captured into the CnV register, at the same time the CHnF bit is set and the channel interrupt is generated if enabled by $CHnIE = 1$ (see the following figure).

When a channel is configured for input capture, the TPM_CHn pin is an edge-sensitive input. $ELSnB:ELSnA$ control bits determine which edge, falling or rising, triggers input-capture event. Note that the maximum frequency for the channel input signal to be detected correctly is counter clock divided by 4, which is required to meet Nyquist criteria for signal sampling.

Writes to the CnV register are ignored in input capture mode.

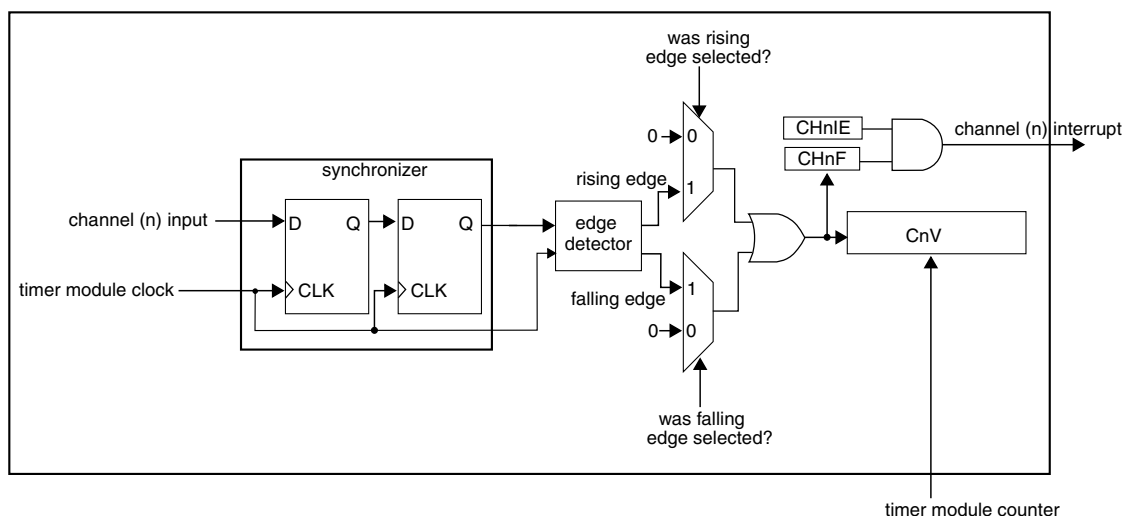


Figure 31-81. Input capture mode

The CHnF bit is set on the third rising edge of the counter clock after a valid edge occurs on the channel input.

31.4.5 Output Compare Mode

The output compare mode is selected when ($CPWMS = 0$), and ($MSnB:MSnA = X:1$).

Functional Description

In output compare mode, the TPM can generate timed pulses with programmable position, polarity, duration, and frequency. When the counter matches the value in the CnV register of an output compare channel, the channel (n) output can be set, cleared or toggled if MSnB is clear. If MSnB is set then the channel (n) output is pulsed high or low for as long as the counter matches the value in the CnV register.

When a channel is initially configured to output compare mode, the channel output updates with its negated value (logic 0 for set/toggle/pulse high and logic one for clear/pulse low).

The CHnF bit is set and the channel (n) interrupt is generated (if CHnIE = 1) at the channel (n) match (TPM counter = CnV).

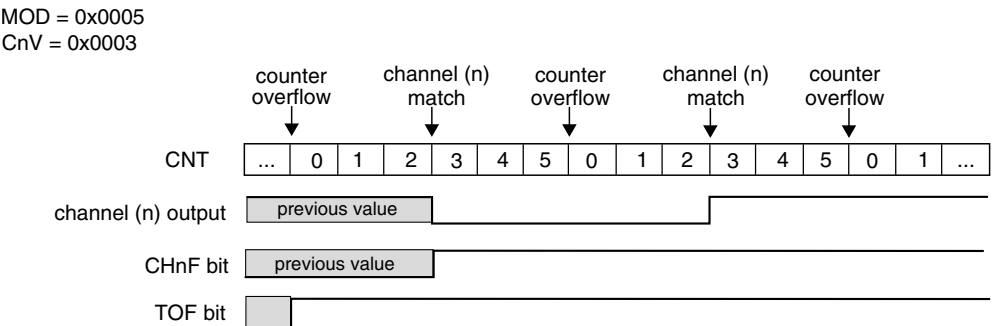


Figure 31-82. Example of the output compare mode when the match toggles the channel output

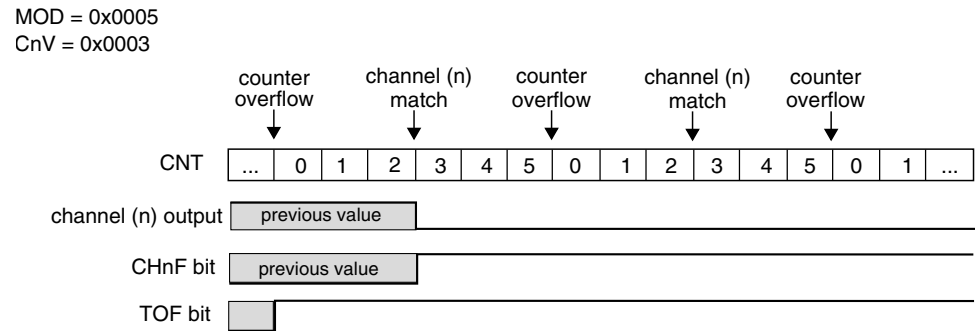


Figure 31-83. Example of the output compare mode when the match clears the channel output

MOD = 0x0005
CnV = 0x0003

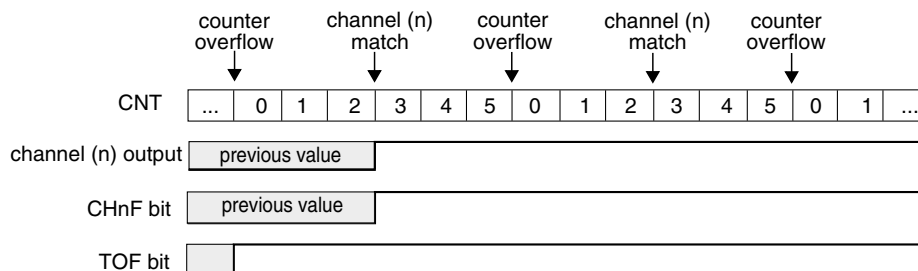


Figure 31-84. Example of the output compare mode when the match sets the channel output

It is possible to use the output compare mode with (ELSnB:ELSnA = 0:0). In this case, when the counter reaches the value in the CnV register, the CHnF bit is set and the channel (n) interrupt is generated (if CHnIE = 1), however the channel (n) output is not modified and controlled by TPM.

31.4.6 Edge-Aligned PWM (EPWM) Mode

The edge-aligned mode is selected when (CPWMS = 0), and (MSnB:MSnA = 1:0). The EPWM period is determined by (MOD + 0x0001) and the pulse width (duty cycle) is determined by CnV.

The CHnF bit is set and the channel (n) interrupt is generated (if CHnIE = 1) at the channel (n) match (TPM counter = CnV), that is, at the end of the pulse width.

This type of PWM signal is called edge-aligned because the leading edges of all PWM signals are aligned with the beginning of the period, which is the same for all channels within an TPM.

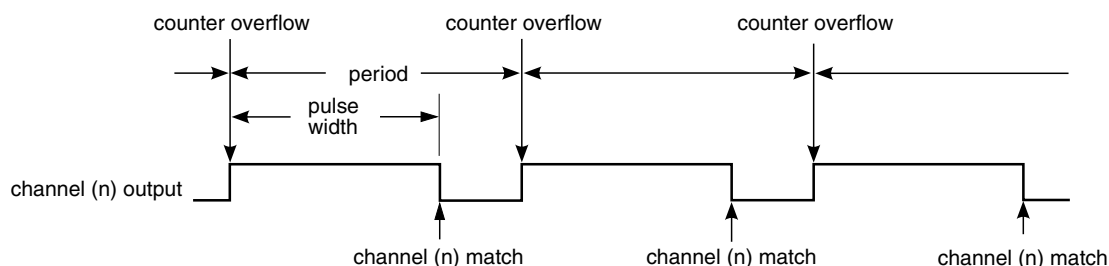


Figure 31-85. EPWM period and pulse width with ELSnB:ELSnA = 1:0

If (ELSnB:ELSnA = 0:0) when the counter reaches the value in the CnV register, the CHnF bit is set and the channel (n) interrupt is generated (if CHnIE = 1), however the channel (n) output is not controlled by TPM.

Functional Description

If (ELSnB:ELSnA = 1:0), then the channel (n) output is forced high at the counter overflow (when the zero is loaded into the TPM counter), and it is forced low at the channel (n) match (TPM counter = CnV) (see the following figure).

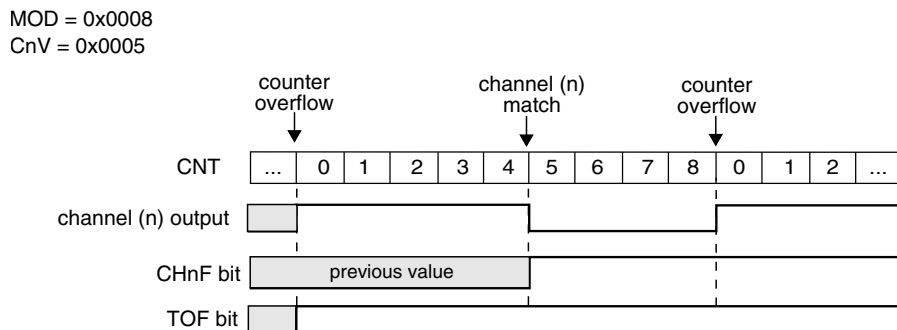


Figure 31-86. EPWM signal with ELSnB:ELSnA = 1:0

If (ELSnB:ELSnA = X:1), then the channel (n) output is forced low at the counter overflow (when zero is loaded into the TPM counter), and it is forced high at the channel (n) match (TPM counter = CnV) (see the following figure).

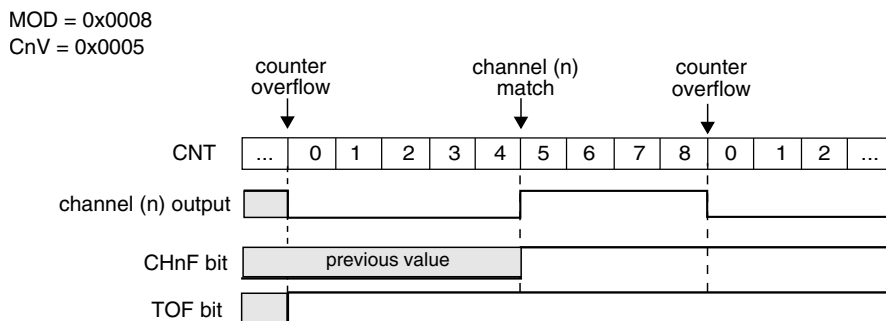


Figure 31-87. EPWM signal with ELSnB:ELSnA = X:1

If (CnV = 0x0000), then the channel (n) output is a 0% duty cycle EPWM signal. If (CnV > MOD), then the channel (n) output is a 100% duty cycle EPWM signal and CHnF bit is not set since there is never a channel (n) match. Therefore, MOD must be less than 0xFFFF in order to get a 100% duty cycle EPWM signal.

31.4.7 Center-Aligned PWM (CPWM) Mode

The center-aligned mode is selected when (CPWMS = 1) and (MSnB:MSnA = 1:0).

The CPWM pulse width (duty cycle) is determined by $2 \times \text{CnV}$ and the period is determined by $2 \times \text{MOD}$ (see the following figure). MOD must be kept in the range of 0x0001 to 0x7FFF because values outside this range can produce ambiguous results.

In the CPWM mode, the TPM counter counts up until it reaches MOD and then counts down until it reaches zero.

The CHnF bit is set and channel (n) interrupt is generated (if CHnIE = 1) at the channel (n) match (TPM counter = CnV) when the TPM counting is down (at the begin of the pulse width) and when the TPM counting is up (at the end of the pulse width).

This type of PWM signal is called center-aligned because the pulse width centers for all channels are when the TPM counter is zero.

The other channel modes are not designed to be used with the up-down counter (CPWMS = 1). Therefore, all TPM channels should be used in CPWM mode when (CPWMS = 1).

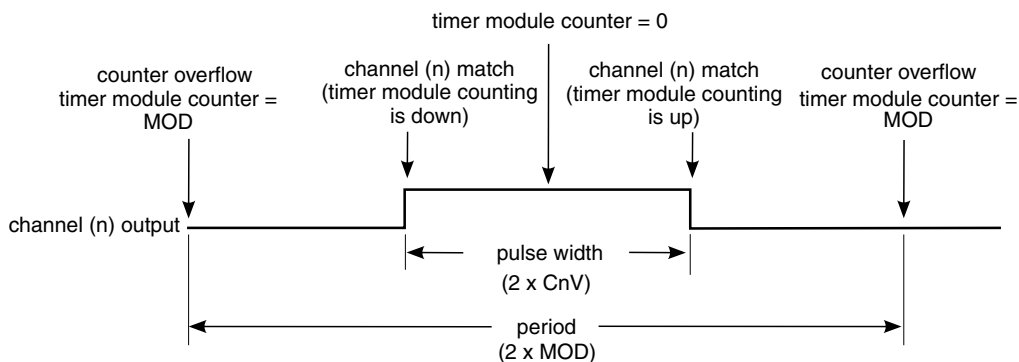


Figure 31-88. CPWM period and pulse width with ELSnB:ELSnA = 1:0

If (ELSnB:ELSnA = 0:0) when the TPM counter reaches the value in the CnV register, the CHnF bit is set and the channel (n) interrupt is generated (if CHnIE = 1), however the channel (n) output is not controlled by TPM.

If (ELSnB:ELSnA = 1:0), then the channel (n) output is forced high at the channel (n) match (TPM counter = CnV) when counting down, and it is forced low at the channel (n) match when counting up (see the following figure).

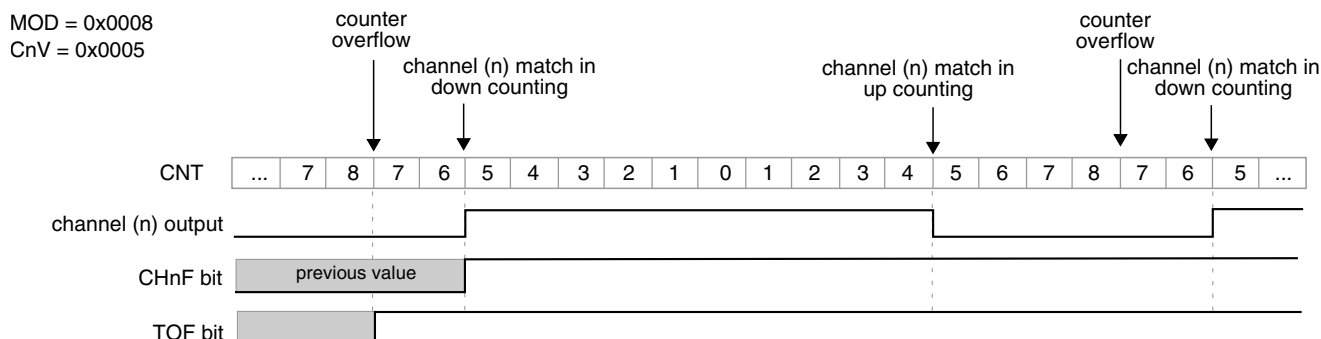


Figure 31-89. CPWM signal with ELSnB:ELSnA = 1:0

If (ELSnB:ELSnA = X:1), then the channel (n) output is forced low at the channel (n) match (TPM counter = CnV) when counting down, and it is forced high at the channel (n) match when counting up (see the following figure).

Functional Description

MOD = 0x0008
CnV = 0x0005

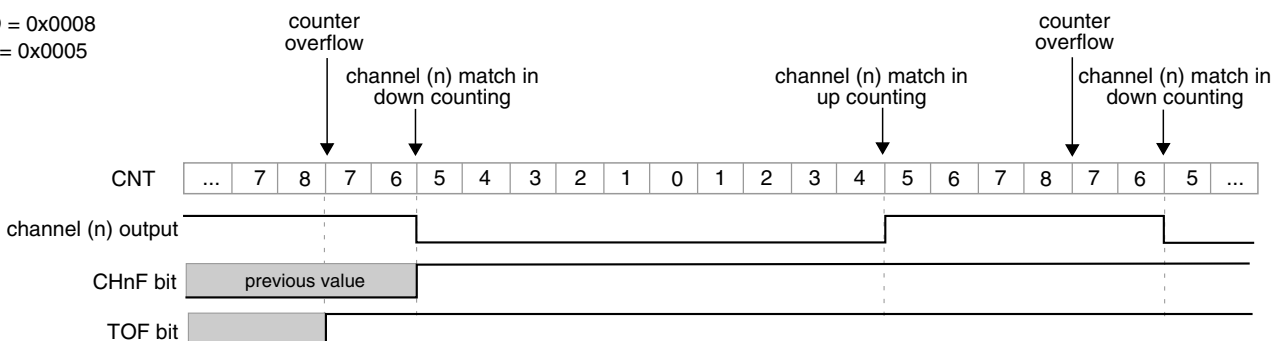


Figure 31-90. CPWM signal with ELSnB:ELSnA = X:1

If (CnV = 0x0000) then the channel (n) output is a 0% duty cycle CPWM signal.

If (CnV > MOD), then the channel (n) output is a 100% duty cycle CPWM signal, although the CHnF bit is set when the counter changes from incrementing to decrementing. Therefore, MOD must be less than 0xFFFF in order to get a 100% duty cycle CPWM signal.

31.4.8 Registers Updated from Write Buffers

31.4.8.1 MOD Register Update

If (CMOD[1:0] = 0:0) then MOD register is updated when MOD register is written.

If (CMOD[1:0] ≠ 0:0), then MOD register is updated according to the CPWMS bit, that is:

- If the selected mode is not CPWM then MOD register is updated after MOD register was written and the TPM counter changes from MOD to zero.
- If the selected mode is CPWM then MOD register is updated after MOD register was written and the TPM counter changes from MOD to (MOD – 1).

31.4.8.2 CnV Register Update

If (CMOD[1:0] = 0:0) then CnV register is updated when CnV register is written.

If (CMOD[1:0] ≠ 0:0), then CnV register is updated according to the selected mode, that is:

- If the selected mode is output compare then CnV register is updated on the next TPM counter increment (end of the prescaler counting) after CnV register was written.
- If the selected mode is EPWM then CnV register is updated after CnV register was written and the TPM counter changes from MOD to zero.
- If the selected mode is CPWM then CnV register is updated after CnV register was written and the TPM counter changes from MOD to (MOD – 1).

31.4.9 DMA

The channel generates a DMA transfer request according to DMA and CHnIE bits (see the following table).

Table 31-110. Channel DMA Transfer Request

DMA	CHnIE	Channel DMA Transfer Request	Channel Interrupt
0	0	The channel DMA transfer request is not generated.	The channel interrupt is not generated.
0	1	The channel DMA transfer request is not generated.	The channel interrupt is generated if (CHnF = 1).
1	0	The channel DMA transfer request is generated if (CHnF = 1).	The channel interrupt is not generated.
1	1	The channel DMA transfer request is generated if (CHnF = 1).	The channel interrupt is generated if (CHnF = 1).

If DMA = 1, the CHnF bit can be cleared either by channel DMA transfer done or writing a one to CHnF bit (see the following table).

Table 31-111. Clear CHnF Bit

DMA	How CHnF Bit Can Be Cleared
0	CHnF bit is cleared by writing a 1 to CHnF bit.
1	CHnF bit is cleared either when the channel DMA transfer is done or by writing a 1 to CHnF bit.

31.4.10 Output triggers

The TPM generates output triggers for the counter and each channel that can be used to trigger events in other peripherals. The counter trigger asserts whenever the TOF is set and remains asserted until the next increment.

Each TPM channel generates both a pre-trigger output and a trigger output. The pre-trigger output asserts whenever the CHnF is set, the trigger output asserts on the first counter increment after the pre-trigger asserts, and then both the trigger and pre-trigger negate on the first counter increment after the trigger asserts.

31.4.11 Reset Overview

The TPM is reset whenever any chip reset occurs.

When the TPM exits from reset:

- the TPM counter and the prescaler counter are zero and are stopped (CMOD[1:0] = 0:0);
- the timer overflow interrupt is zero;
- the channels interrupts are zero;
- the channels are in input capture mode;
- the channels outputs are zero;
- the channels pins are not controlled by TPM (ELS(n)B:ELS(n)A = 0:0).

31.4.12 TPM Interrupts

This section describes TPM interrupts.

31.4.12.1 Timer Overflow Interrupt

The timer overflow interrupt is generated when (TOIE = 1) and (TOF = 1).

31.4.12.2 Channel (n) Interrupt

The channel (n) interrupt is generated when (CHnIE = 1) and (CHnF = 1).