Table 10-2. Port control register configuration summary (continued)

This field of PORTx_PCRn	Generally resets to	Except for	Resets to	Configurability
IRQC	000	No exceptions—all are cleared on reset.	—	Only implemented for ports that support interrupt and DMA functionality.
ISF	0	No exceptions—all are cleared on reset.	—	Only implemented for ports that support interrupt and DMA functionality.

1. The RESET_b pin has the passive analog filter fixed enabled when functioning as the RESET_b pin (FOPT[RESET_PIN_CFG] = 1) and fixed disabled when configured for other shared functions.

10.2.2 Clock gating

The clock to the port control module can be gated on and off using the SCGC5[PORTx] bits in the SIM module. These bits are cleared after any reset, which disables the clock to the corresponding module to conserve power. Prior to initializing the corresponding module, set SIM_SCGC5[PORTx] to enable the clock. Before turning off the clock, make sure to disable the module. For more details, see the Clock distribution chapter.

10.2.3 Signal multiplexing constraints

1. A given peripheral function must be assigned to a maximum of one package pin. Do not program the same function to more than one pin.
2. To ensure the best signal timing for a given peripheral's interface, choose the pins in closest proximity to each other.
3. For normal operation of the LCD, use ALT0 LCD functions. The ALT7 LCD functions are only available for LCD fault detection.

10.3 Pinout

10.3.1 KL46 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

121 BGA	100 LQFP	64 BGA	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
E4	1	A1	1	PTE0	DISABLED	LCD_P48	PTE0	SPI1_MISO	UART1_TX	RTC_CLKOUT	CMP0_OUT	I2C1_SDA	LCD_P48
E3	2	B1	2	PTE1	DISABLED	LCD_P49	PTE1	SPI1_MOSI	UART1_RX		SPI1_MISO	I2C1_SCL	LCD_P49
E2	3	—	—	PTE2	DISABLED	LCD_P50	PTE2	SPI1_SCK					LCD_P50
F4	4	—	—	PTE3	DISABLED	LCD_P51	PTE3	SPI1_MISO			SPI1_MOSI		LCD_P51
H7	5	—	—	PTE4	DISABLED	LCD_P52	PTE4	SPI1_PCS0					LCD_P52
G4	6	—	—	PTE5	DISABLED	LCD_P53	PTE5						LCD_P53
F3	7	—	—	PTE6	DISABLED	LCD_P54	PTE6			I2S0_MCLK	audioUSB_ SOF_OUT		LCD_P54
E6	8	—	3	VDD	VDD	VDD							
G7	9	C4	4	VSS	VSS	VSS							
L6	—	—	—	VSS	VSS	VSS							
F1	10	E1	5	USB0_DP	USB0_DP	USB0_DP							
F2	11	D1	6	USB0_DM	USB0_DM	USB0_DM							
G1	12	E2	7	VOUT33	VOUT33	VOUT33							
G2	13	D2	8	VREGIN	VREGIN	VREGIN							
H1	14	—	—	PTE16	ADC0_DP1/ ADC0_SE1	LCD_P55/ ADC0_DP1/ ADC0_SE1	PTE16	SPI0_PCS0	UART2_TX	TPM_CLKIN0			LCD_P55
H2	15	—	—	PTE17	ADC0_DM1/ ADC0_SE5a	LCD_P56/ ADC0_DM1/ ADC0_SE5a	PTE17	SPI0_SCK	UART2_RX	TPM_CLKIN1		LPTMR0_ ALT3	LCD_P56
J1	16	—	—	PTE18	ADC0_DP2/ ADC0_SE2	LCD_P57/ ADC0_DP2/ ADC0_SE2	PTE18	SPI0_MOSI		I2C0_SDA	SPI0_MISO		LCD_P57
J2	17	—	—	PTE19	ADC0_DM2/ ADC0_SE6a	LCD_P58/ ADC0_DM2/ ADC0_SE6a	PTE19	SPI0_MISO		I2C0_SCL	SPI0_MOSI		LCD_P58
K1	18	G1	9	PTE20	ADC0_DP0/ ADC0_SE0	LCD_P59/ ADC0_DP0/ ADC0_SE0	PTE20		TPM1_CH0	UART0_TX			LCD_P59
K2	19	F1	10	PTE21	ADC0_DM0/ ADC0_SE4a	LCD_P60/ ADC0_DM0/ ADC0_SE4a	PTE21		TPM1_CH1	UART0_RX			LCD_P60
L1	20	G2	11	PTE22	ADC0_DP3/ ADC0_SE3	ADC0_DP3/ ADC0_SE3	PTE22		TPM2_CH0	UART2_TX			
L2	21	F2	12	PTE23	ADC0_DM3/ ADC0_SE7a	ADC0_DM3/ ADC0_SE7a	PTE23		TPM2_CH1	UART2_RX			
F5	22	F4	13	VDDA	VDDA	VDDA							
G5	23	G4	14	VREFH	VREFH	VREFH							
G6	24	G3	15	VREFL	VREFL	VREFL							
F6	25	F3	16	VSSA	VSSA	VSSA							
L3	26	H1	17	PTE29	CMP0_IN5/ ADC0_SE4b	CMP0_IN5/ ADC0_SE4b	PTE29		TPM0_CH2	TPM_CLKIN0			
K5	27	H2	18	PTE30	DAC0_OUT/ ADC0_SE23/ CMP0_IN4	DAC0_OUT/ ADC0_SE23/ CMP0_IN4	PTE30		TPM0_CH3	TPM_CLKIN1			

121 BGA	100 LQFP	64 BGA	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
L4	28	H3	19	PTE31	DISABLED		PTE31		TPM0_CH4				
L5	29	—	—	VSS	VSS	VSS							
K6	30	—	—	VDD	VDD	VDD							
H5	31	H4	20	PTE24	DISABLED		PTE24		TPM0_CH0		I2C0_SCL		
J5	32	H5	21	PTE25	DISABLED		PTE25		TPM0_CH1		I2C0_SDA		
H6	33	—	—	PTE26	DISABLED		PTE26		TPM0_CH5			RTC_CLKOUT	USB_CLKIN
J6	34	D3	22	PTA0	SWD_CLK	TSI0_CH1	PTA0		TPM0_CH5				SWD_CLK
H8	35	D4	23	PTA1	DISABLED	TSI0_CH2	PTA1	UART0_RX	TPM2_CH0				
J7	36	E5	24	PTA2	DISABLED	TSI0_CH3	PTA2	UART0_TX	TPM2_CH1				
H9	37	D5	25	PTA3	SWD_DIO	TSI0_CH4	PTA3	I2C1_SCL	TPM0_CH0				SWD_DIO
J8	38	G5	26	PTA4	NMI_b	TSI0_CH5	PTA4	I2C1_SDA	TPM0_CH1				NMI_b
K7	39	F5	27	PTA5	DISABLED		PTA5	USB_CLKIN	TPM0_CH2			I2S0_TX_BCLK	
E5	—	—	—	VDD	VDD	VDD							
G3	—	—	—	VSS	VSS	VSS							
K3	40	—	—	PTA6	DISABLED		PTA6		TPM0_CH3				
H4	41	—	—	PTA7	DISABLED		PTA7		TPM0_CH4				
K8	42	H6	28	PTA12	DISABLED		PTA12		TPM1_CH0			I2S0_TXD0	
L8	43	G6	29	PTA13	DISABLED		PTA13		TPM1_CH1			I2S0_TX_FS	
K9	44	—	—	PTA14	DISABLED		PTA14	SPI0_PCS0	UART0_TX			I2S0_RX_BCLK	I2S0_TXD0
L9	45	—	—	PTA15	DISABLED		PTA15	SPI0_SCK	UART0_RX			I2S0_RXD0	
J10	46	—	—	PTA16	DISABLED		PTA16	SPI0_MOSI			SPI0_MISO	I2S0_RX_FS	I2S0_RXD0
H10	47	—	—	PTA17	DISABLED		PTA17	SPI0_MISO			SPI0_MOSI	I2S0_MCLK	
L10	48	G7	30	VDD	VDD	VDD							
K10	49	H7	31	VSS	VSS	VSS							
L11	50	H8	32	PTA18	EXTAL0	EXTAL0	PTA18		UART1_RX	TPM_CLKIN0			
K11	51	G8	33	PTA19	XTAL0	XTAL0	PTA19		UART1_TX	TPM_CLKIN1		LPTMR0_ALT1	
J11	52	F8	34	PTA20	RESET_b		PTA20						RESET_b
G11	53	F7	35	PTB0/ LLWU_P5	LCD_P0/ ADC0_SE8/ TSI0_CH0	LCD_P0/ ADC0_SE8/ TSI0_CH0	PTB0/ LLWU_P5	I2C0_SCL	TPM1_CH0				LCD_P0
G10	54	F6	36	PTB1	LCD_P1/ ADC0_SE9/ TSI0_CH6	LCD_P1/ ADC0_SE9/ TSI0_CH6	PTB1	I2C0_SDA	TPM1_CH1				LCD_P1
G9	55	E7	37	PTB2	LCD_P2/ ADC0_SE12/ TSI0_CH7	LCD_P2/ ADC0_SE12/ TSI0_CH7	PTB2	I2C0_SCL	TPM2_CH0				LCD_P2
G8	56	E8	38	PTB3	LCD_P3/ ADC0_SE13/ TSI0_CH8	LCD_P3/ ADC0_SE13/ TSI0_CH8	PTB3	I2C0_SDA	TPM2_CH1				LCD_P3
E11	57	—	—	PTB7	LCD_P7	LCD_P7	PTB7						LCD_P7
D11	58	—	—	PTB8	LCD_P8	LCD_P8	PTB8	SPI1_PCS0	EXTRG_IN				LCD_P8

121 BGA	100 LQFP	64 BGA	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
E10	59	—	—	PTB9	LCD_P9	LCD_P9	PTB9	SPI1_SCK					LCD_P9
D10	60	—	—	PTB10	LCD_P10	LCD_P10	PTB10	SPI1_PCS0					LCD_P10
C10	61	—	—	PTB11	LCD_P11	LCD_P11	PTB11	SPI1_SCK					LCD_P11
B10	62	E6	39	PTB16	LCD_P12/ TSI0_CH9	LCD_P12/ TSI0_CH9	PTB16	SPI1_MOSI	UART0_RX	TPM_CLKIN0	SPI1_MISO		LCD_P12
E9	63	D7	40	PTB17	LCD_P13/ TSI0_CH10	LCD_P13/ TSI0_CH10	PTB17	SPI1_MISO	UART0_TX	TPM_CLKIN1	SPI1_MOSI		LCD_P13
D9	64	D6	41	PTB18	LCD_P14/ TSI0_CH11	LCD_P14/ TSI0_CH11	PTB18		TPM2_CH0	I2S0_TX_ BCLK			LCD_P14
C9	65	C7	42	PTB19	LCD_P15/ TSI0_CH12	LCD_P15/ TSI0_CH12	PTB19		TPM2_CH1	I2S0_TX_FS			LCD_P15
F10	66	—	—	PTB20	LCD_P16	LCD_P16	PTB20					CMP0_OUT	LCD_P16
F9	67	—	—	PTB21	LCD_P17	LCD_P17	PTB21						LCD_P17
F8	68	—	—	PTB22	LCD_P18	LCD_P18	PTB22						LCD_P18
E8	69	—	—	PTB23	LCD_P19	LCD_P19	PTB23						LCD_P19
B9	70	D8	43	PTC0	LCD_P20/ ADC0_SE14/ TSI0_CH13	LCD_P20/ ADC0_SE14/ TSI0_CH13	PTC0		EXTRG_IN	audioUSB_ SOF_OUT	CMP0_OUT	I2S0_TXD0	LCD_P20
D8	71	C6	44	PTC1/ LLWU_P6/ RTC_CLKIN	LCD_P21/ ADC0_SE15/ TSI0_CH14	LCD_P21/ ADC0_SE15/ TSI0_CH14	PTC1/ LLWU_P6/ RTC_CLKIN	I2C1_SCL		TPM0_CH0		I2S0_TXD0	LCD_P21
C8	72	B7	45	PTC2	LCD_P22/ ADC0_SE11/ TSI0_CH15	LCD_P22/ ADC0_SE11/ TSI0_CH15	PTC2	I2C1_SDA		TPM0_CH1		I2S0_TX_FS	LCD_P22
B8	73	C8	46	PTC3/ LLWU_P7	LCD_P23	LCD_P23	PTC3/ LLWU_P7		UART1_RX	TPM0_CH2	CLKOUT	I2S0_TX_ BCLK	LCD_P23
F7	74	E3	47	VSS	VSS	VSS							
E7	—	E4	—	VDD	VDD	VDD							
A11	75	C5	48	VLL3	VLL3	VLL3							
A10	76	A6	49	VLL2	VLL2	VLL2/ LCD_P4	PTC20						LCD_P4
A9	77	B5	50	VLL1	VLL1	VLL1/ LCD_P5	PTC21						LCD_P5
B11	78	B4	51	VCAP2	VCAP2	VCAP2/ LCD_P6	PTC22						LCD_P6
C11	79	A5	52	VCAP1	VCAP1	VCAP1/ LCD_P39	PTC23						LCD_P39
A8	80	B8	53	PTC4/ LLWU_P8	LCD_P24	LCD_P24	PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	TPM0_CH3	I2S0_MCLK		LCD_P24
D7	81	A8	54	PTC5/ LLWU_P9	LCD_P25	LCD_P25	PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ ALT2	I2S0_RXD0		CMP0_OUT	LCD_P25
C7	82	A7	55	PTC6/ LLWU_P10	LCD_P26/ CMP0_IN0	LCD_P26/ CMP0_IN0	PTC6/ LLWU_P10	SPI0_MOSI	EXTRG_IN	I2S0_RX_ BCLK	SPI0_MISO	I2S0_MCLK	LCD_P26
B7	83	B6	56	PTC7	LCD_P27/ CMP0_IN1	LCD_P27/ CMP0_IN1	PTC7	SPI0_MISO	audioUSB_ SOF_OUT	I2S0_RX_FS	SPI0_MOSI		LCD_P27
A7	84	—	—	PTC8	LCD_P28/ CMP0_IN2	LCD_P28/ CMP0_IN2	PTC8	I2C0_SCL	TPM0_CH4	I2S0_MCLK			LCD_P28

121 BGA	100 LQFP	64 BGA	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
D6	85	—	—	PTC9	LCD_P29/ CMP0_IN3	LCD_P29/ CMP0_IN3	PTC9	I2C0_SDA	TPM0_CH5	I2S0_RX_ BCLK			LCD_P29
C6	86	—	—	PTC10	LCD_P30	LCD_P30	PTC10	I2C1_SCL		I2S0_RX_FS			LCD_P30
C5	87	—	—	PTC11	LCD_P31	LCD_P31	PTC11	I2C1_SDA		I2S0_RXD0			LCD_P31
B6	88	—	—	PTC12	LCD_P32	LCD_P32	PTC12			TPM_CLKIN0			LCD_P32
A6	89	—	—	PTC13	LCD_P33	LCD_P33	PTC13			TPM_CLKIN1			LCD_P33
D5	90	—	—	PTC16	LCD_P36	LCD_P36	PTC16						LCD_P36
C4	91	—	—	PTC17	LCD_P37	LCD_P37	PTC17						LCD_P37
B4	92	—	—	PTC18	LCD_P38	LCD_P38	PTC18						LCD_P38
D4	93	C3	57	PTD0	LCD_P40	LCD_P40	PTD0	SPI0_PCS0		TPM0_CH0			LCD_P40
D3	94	A4	58	PTD1	LCD_P41/ ADC0_SE5b	LCD_P41/ ADC0_SE5b	PTD1	SPI0_SCK		TPM0_CH1			LCD_P41
C3	95	C2	59	PTD2	LCD_P42	LCD_P42	PTD2	SPI0_MOSI	UART2_RX	TPM0_CH2	SPI0_MISO		LCD_P42
B3	96	B3	60	PTD3	LCD_P43	LCD_P43	PTD3	SPI0_MISO	UART2_TX	TPM0_CH3	SPI0_MOSI		LCD_P43
A3	97	A3	61	PTD4/ LLWU_P14	LCD_P44	LCD_P44	PTD4/ LLWU_P14	SPI1_PCS0	UART2_RX	TPM0_CH4			LCD_P44
A2	98	C1	62	PTD5	LCD_P45/ ADC0_SE6b	LCD_P45/ ADC0_SE6b	PTD5	SPI1_SCK	UART2_TX	TPM0_CH5			LCD_P45
B2	99	B2	63	PTD6/ LLWU_P15	LCD_P46/ ADC0_SE7b	LCD_P46/ ADC0_SE7b	PTD6/ LLWU_P15	SPI1_MOSI	UART0_RX		SPI1_MISO		LCD_P46
A1	100	A2	64	PTD7	LCD_P47	LCD_P47	PTD7	SPI1_MISO	UART0_TX		SPI1_MOSI		LCD_P47
J3	—	—	—	NC	NC	NC							
H3	—	—	—	NC	NC	NC							
K4	—	—	—	NC	NC	NC							
L7	—	—	—	NC	NC	NC							
J9	—	—	—	NC	NC	NC							
J4	—	—	—	NC	NC	NC							
H11	—	—	—	NC	NC	NC							
F11	—	—	—	NC	NC	NC							
A5	—	—	—	NC	NC	NC							
B5	—	—	—	NC	NC	NC							
A4	—	—	—	NC	NC	NC							
B1	—	—	—	NC	NC	NC							
C2	—	—	—	NC	NC	NC							
C1	—	—	—	NC	NC	NC							
D2	—	—	—	NC	NC	NC							
D1	—	—	—	NC	NC	NC							
E1	—	—	—	NC	NC	NC							

10.3.2 KL46 pinouts

The following figures show the pinout diagrams for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see KL46 Signal Multiplexing and Pin Assignments.

	1	2	3	4	5	6	7	8	9	10	11	
A	PTD7	PTD5	PTD4/ LLWU_P14	NC	NC	PTC13	PTC8	PTC4/ LLWU_P8	VLL1	VLL2	VLL3	A
B	NC	PTD6/ LLWU_P15	PTD3	PTC18	NC	PTC12	PTC7	PTC3/ LLWU_P7	PTC0	PTB16	VCAP2	B
C	NC	NC	PTD2	PTC17	PTC11	PTC10	PTC6/ LLWU_P10	PTC2	PTB19	PTB11	VCAP1	C
D	NC	NC	PTD1	PTD0	PTC16	PTC9	PTC5/ LLWU_P9	PTC1/ LLWU_P6/ RTC_CLKIN	PTB18	PTB10	PTB8	D
E	NC	PTE2	PTE1	PTE0	VDD	VDD	VDD	PTB23	PTB17	PTB9	PTB7	E
F	USB0_DP	USB0_DM	PTE6	PTE3	VDDA	VSSA	VSS	PTB22	PTB21	PTB20	NC	F
G	VOUT33	VREGIN	VSS	PTE5	VREFH	VREFL	VSS	PTB3	PTB2	PTB1	PTB0/ LLWU_P5	G
H	PTE16	PTE17	NC	PTA7	PTE24	PTE26	PTE4	PTA1	PTA3	PTA17	NC	H
J	PTE18	PTE19	NC	NC	PTE25	PTA0	PTA2	PTA4	NC	PTA16	PTA20	J
K	PTE20	PTE21	PTA6	NC	PTE30	VDD	PTA5	PTA12	PTA14	VSS	PTA19	K
L	PTE22	PTE23	PTE29	PTE31	VSS	VSS	NC	PTA13	PTA15	VDD	PTA18	L
	1	2	3	4	5	6	7	8	9	10	11	

Figure 10-2. KL46 121-pin BGA pinout diagram

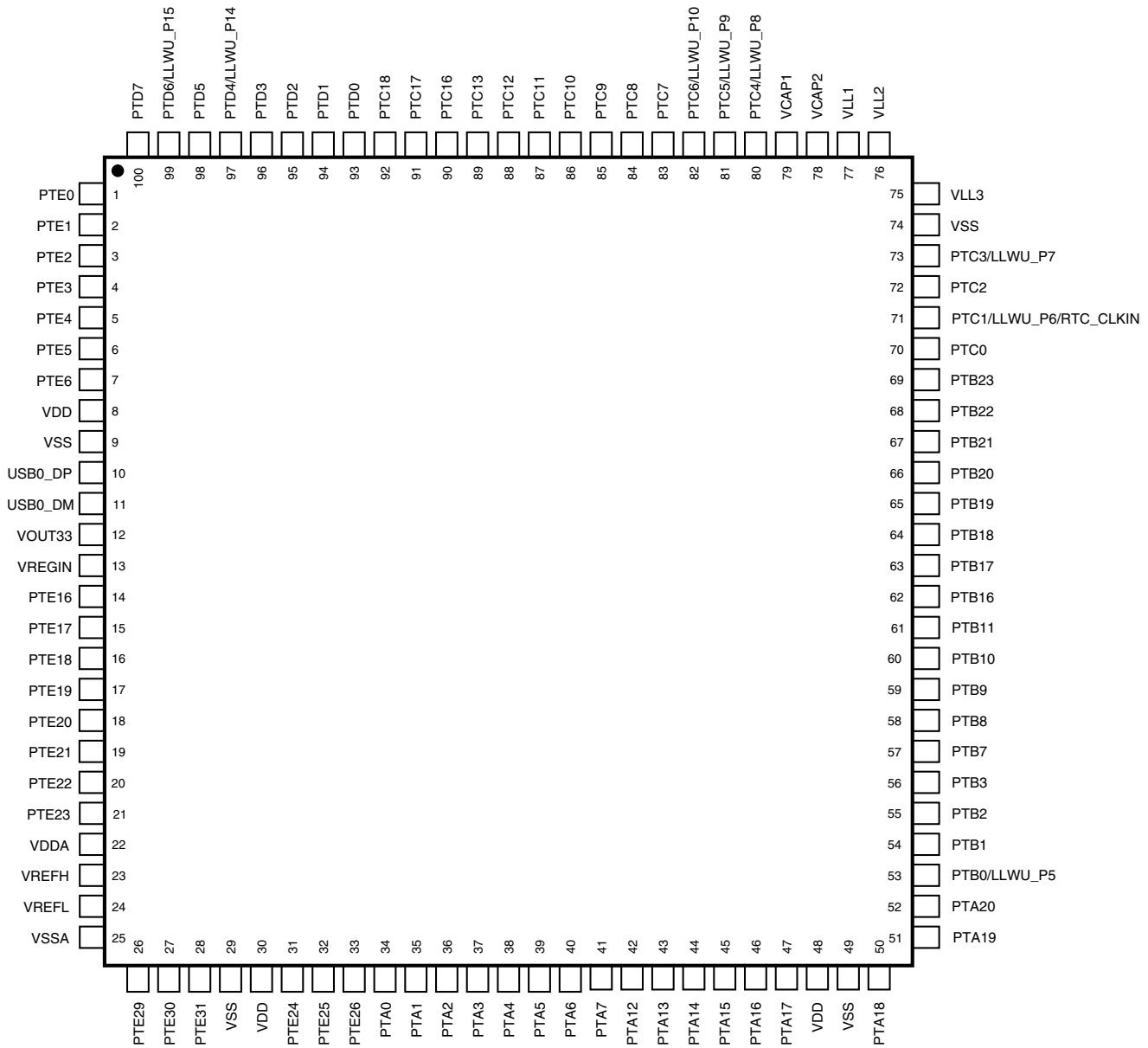
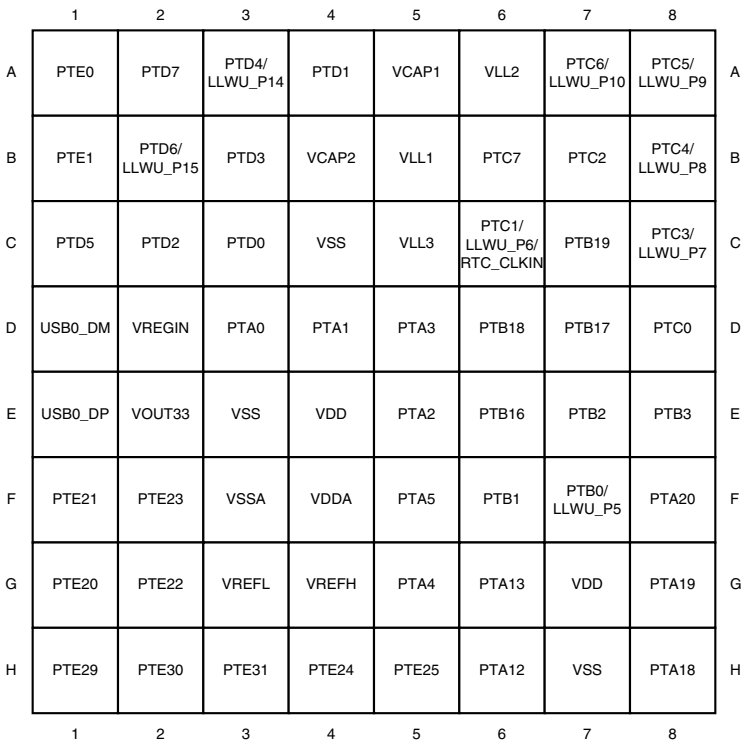


Figure 10-3. KL46 100-pin LQFP pinout diagram



	1	2	3	4	5	6	7	8	
A	PTE0	PTD7	PTD4/ LLWU_P14	PTD1	VCAP1	VLL2	PTC6/ LLWU_P10	PTC5/ LLWU_P9	A
B	PTE1	PTD6/ LLWU_P15	PTD3	VCAP2	VLL1	PTC7	PTC2	PTC4/ LLWU_P8	B
C	PTD5	PTD2	PTD0	VSS	VLL3	PTC1/ LLWU_P6/ RTC_CLKIN	PTB19	PTC3/ LLWU_P7	C
D	USB0_DM	VREGIN	PTA0	PTA1	PTA3	PTB18	PTB17	PTC0	D
E	USB0_DP	VOUT33	VSS	VDD	PTA2	PTB16	PTB2	PTB3	E
F	PTE21	PTE23	VSSA	VDDA	PTA5	PTB1	PTB0/ LLWU_P5	PTA20	F
G	PTE20	PTE22	VREFL	VREFH	PTA4	PTA13	VDD	PTA19	G
H	PTE29	PTE30	PTE31	PTE24	PTE25	PTA12	VSS	PTA18	H
	1	2	3	4	5	6	7	8	

Figure 10-4. KL46 64-pin BGA pinout diagram

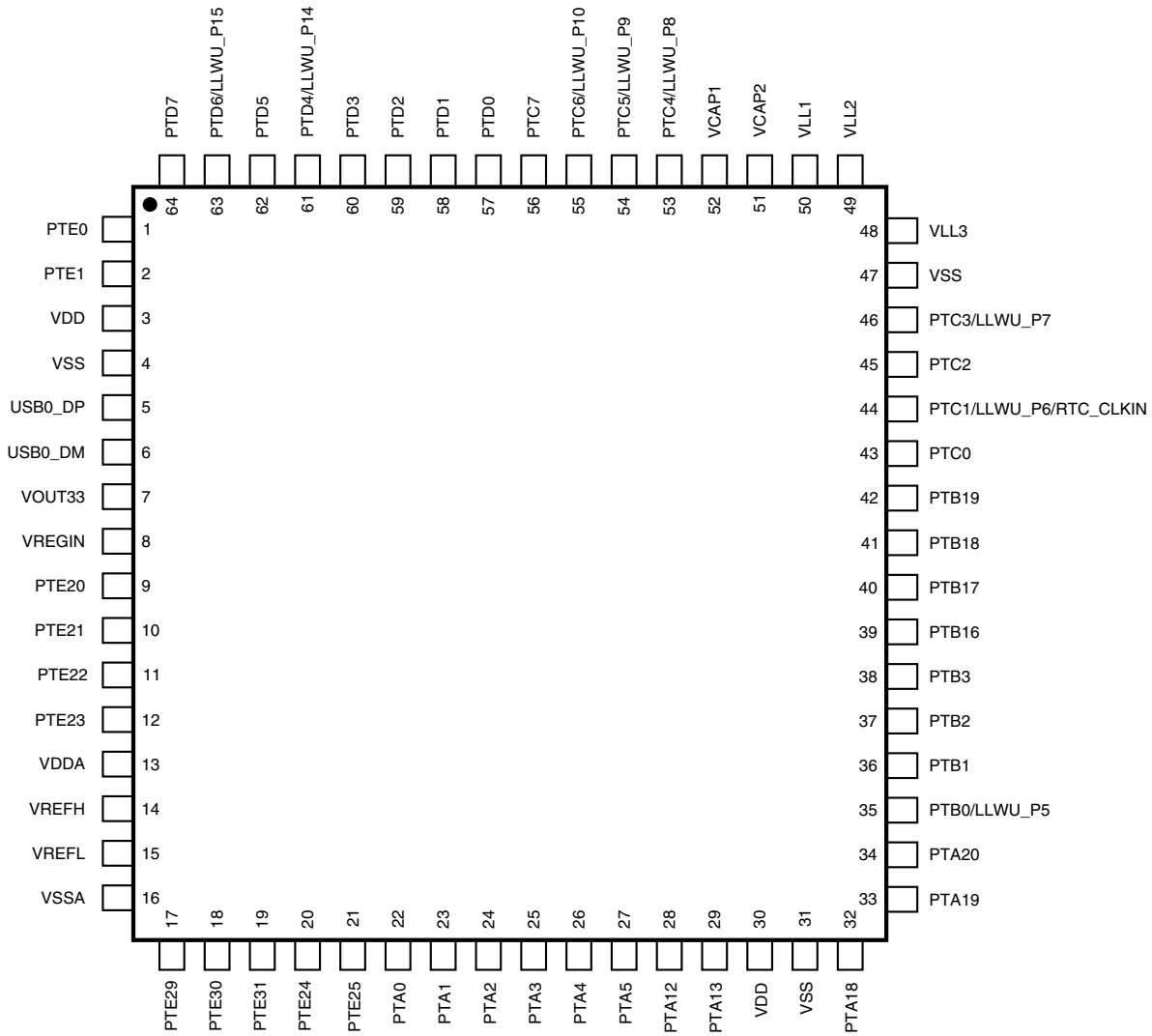


Figure 10-5. KL46 64-pin LQFP pinout diagram

10.4 Module Signal Description Tables

The following sections correlate the chip-level signal name with the signal name used in the module's chapter. They also briefly describe the signal function and direction.