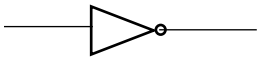
CO221: Digital Design Lab 03 - Pre-lab

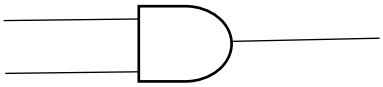
1.

a) NOT Gate (Inverter)



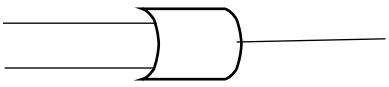
Input	Output
1	0
0	1

b) 2 input AND Gate



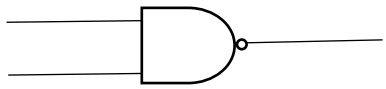
Input 1	Input 2	Output
0	0	0
0	1	0
1	0	0
1	1	1

c) 2 input OR Gate



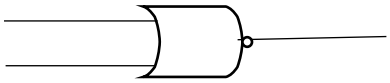
Input 1	Input 2	Output
0	0	0
0	1	1
1	0	1
1	1	1

d) 2 input NAND Gate



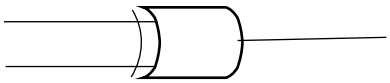
Input 1	Input 2	Output
0	0	1
0	1	1
1	0	1
1	1	0

e) 2 input NOR Gate



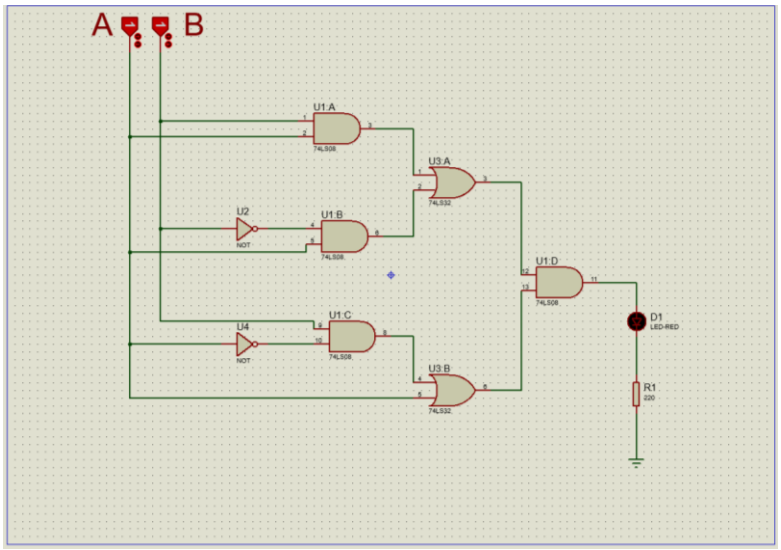
Input 1	Input 2	Output
0	0	1
0	1	0
1	0	0
1	1	0

f) 2 input XOR Gate



Input 1	Input 2	Output
0	0	0
0	1	1
1	0	1
1	1	0

2.



A	B	AB	AB’	AB + AB’	A’B	A + A’B	F
0	0	0	0	0	1	1	0
0	1	0	0	0	1	1	0
1	0	0	1	1	0	1	1
1	1	1	0	1	1	1	1

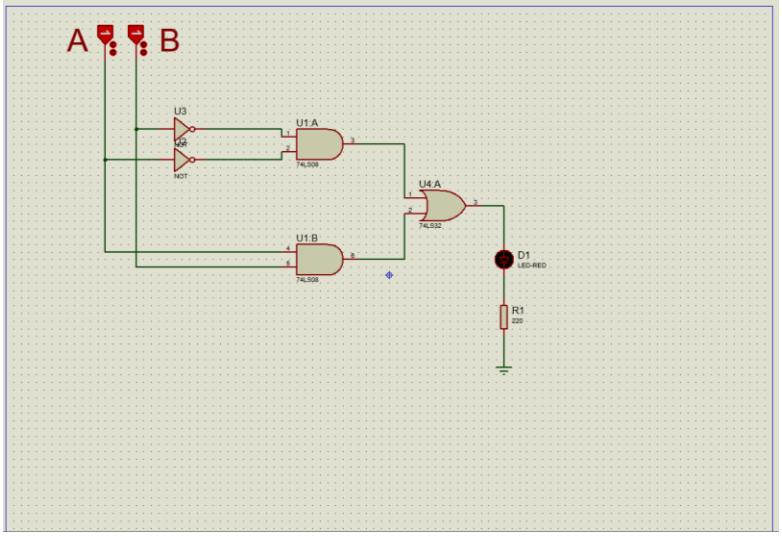
3.

A	B	F
0	0	1
0	1	0
1	0	0
1	1	1

Boolean Equation:

F = A'B' + AB

a)



A	B	F
0	0	1
0	1	0
1	0	0
1	1	1

b)

NOT XOR

A	B	OUTPUT
0	0	1
0	1	0
1	0	0
1	1	1

According to the tables 3(a) & 3(b) the circuit obtained is equivalent to NOT(XOR)

4.

KARNAUGH MAP

BC A	00	01	11	10
0	0	0	0	1
1	1	1	1	1

a)

Boolean Expression:

F = A + BC’

b)