SPI

- Reading: Mazidi -- SPI
- Physical characterstics
    - Type
        - Full-duplex protocol
        - Bus protocol
    - Wires/Connectivity
        - 4 wire protocol
            - MOSI/SDO
            - MISO/SDI
            - SCLK/SCK
            - SS/CE
    - Internal block diagram
        - Single shift register is used for full duplex communication
    - Voltage levels
        - TTL voltage
            - 0 V = Logic 0
            - 3/5 V = Logic 1
    - Frequency
        - High speed
- Logical characterstics
    - Data bit transfer
        - CPOL --> Clock Base
        - CPHA --> Leading/Trailing Edge
    - Data frame
        - Single byte transfer
            - Slave selection is responsibility of the master.
            - SS=0 + MOSI --> 8 Data Bits --> MISO + SS=1
            - SS=0 + MISO <-- 8 Data Bits <-- MOSI + SS=1
        - Multi-byte write

        - Master sends internal address (1-byte or 2-byte) followed by Number of data bytes.
        - SS=0 + Master --> Addr1, Addr2, Byte1, Byte2, ..., Byten --> Slave + SS=1
    - Multi-byte read
        - Master sends internal address (1-byte or 2-byte) and then Slave send Number of data bytes.
        - SS=0 + Master --> Addr1, Addr2 --> Slave + Slave --> Byte1, Byte2, ..., Byten --> Master + SS=1

Applications/Devices

- SD card
- Accelerometer
- EEPROM
- LCD Display
- 7-Segment Display
- RTC
- ...

LIS3DSH (datasheet)

- Introduction
- SPI interface
    - Multi-byte read operation
    - Multi-byte write operation
- Registers
    - CTRL4 -- Data Rate + Axis Enable
    - OUT_X_L & OUT_X_H, OUT_Y_L & OUT_Y_H, OUT_Z_L & OUT_Z_H
    - STATUS

LIS3DSH Library Code - Reference

- https://github.com/MYaqoobEmbedded/STM32-Tutorials/tree/master/Tutorial%2027%20-%20Motion%203-Axis%20Accelerometer%20LIS3DSH

Error conditions

- Read overrun: Before reading received data the next data arrives and overwrite the old one. Thus old data is lost.
- Write collision: Before transmitting current data, new data is overwritten on it. Thus last data is not transmitted correctly.
- Mode fault: When SPI device is in master mode and other SPI device force it to become slave, then Mode fault occurs.
- Slave abort: If SPI master is communicating with a SPI slave and that slave stop responding suddenly, then this error is raised.
- STM32 -- CRC Error: STM32 SPI has CRC calculate & checking hardware in SPI. If CRC is not matching, then this error is raised.

Daisy chaining

- SPI Master select the slave using Slave Select pin. For multiple slaves it (master device) use multiple GPIO pins.
- The number of pins can be reduced using Mux circuit. In this case 3 GPIO pins will be needed to select one of the max 8 slave devices from SPI bus.
- Daisy chaining enables using single GPIO pin of master device to enable all the slaves and transfer data to them.
- https://www.maximintegrated.com/en/design/technical-documents/app-notes/3/3947.html
- https://www.best-microcontroller-projects.com/spi-interface.html

3-wire SPI

- Tie DOUT and DIN pin together.