



# Advanced Micro-controllers - ARM

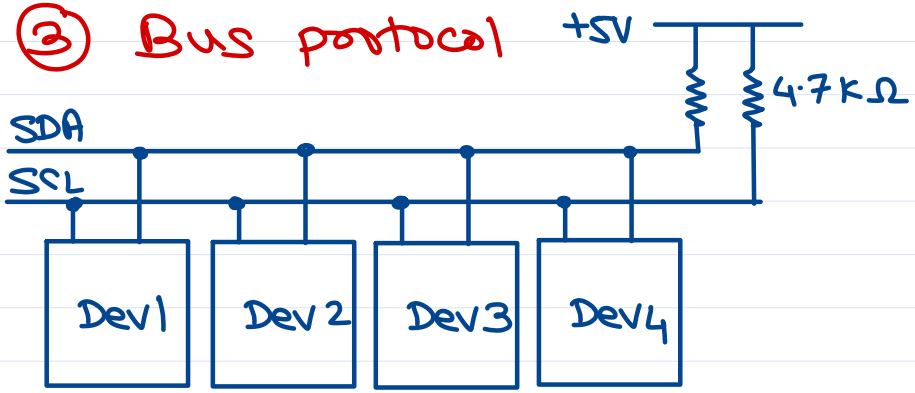
*DESD @ Sunbeam Infotech*

# I2C → Inter IC Communication.

① Philips

② Short distance comm$^{n}$

③ Bus protocol




④ Two wire (TWI)

⑤ Synchronous protocol

⑥ Half duplex

⑦ Wired AND
if any device pulls line to low level, effective line level will be low.

⑧ TTL level

⑨ Frequency
100 kHz - standard
400 kHz - Fast
1 MHz - Fast Plus

⑩ Applications
RTC, EEPROM, LCD, 7-seg Display, Accel, ...

⑪ Device addr → 7-bit
- by manfacturer
- in datasheet.
- max addresses = $2^7$ = 128
- 120 devices on a bus
- few addr reserved
  e.g. 0000 0000: general call

⑫ master-slave arch. → multi-master bus
- clock generation
- control (start/stop) comm$^{n}$
- multiple devices are capable of becoming master on a bus
- Only one master at a time.

⑬ bit format

⑭ packet/frame format
- data packet
- addr packet

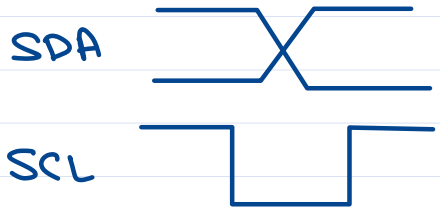
⑮ multi byte write

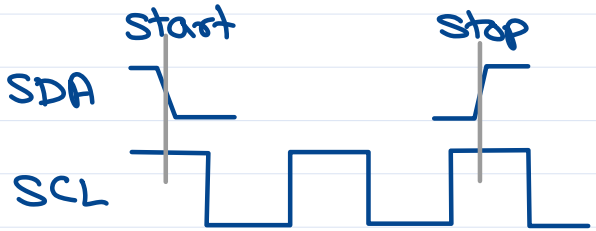
⑯ multi byte read

⑰ error conditions

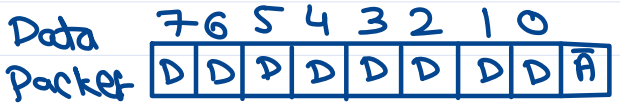
⑱ I2C is a state machine

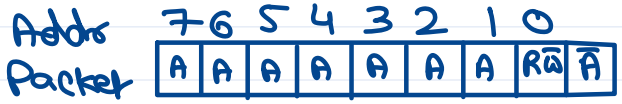
## 13) bit format



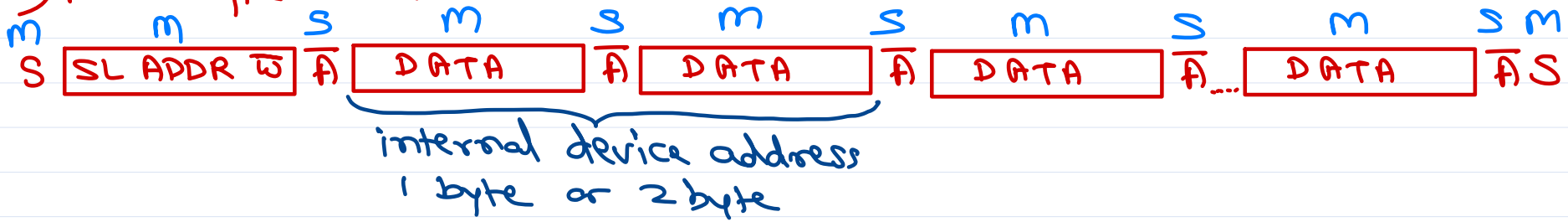

## 14) Packet format



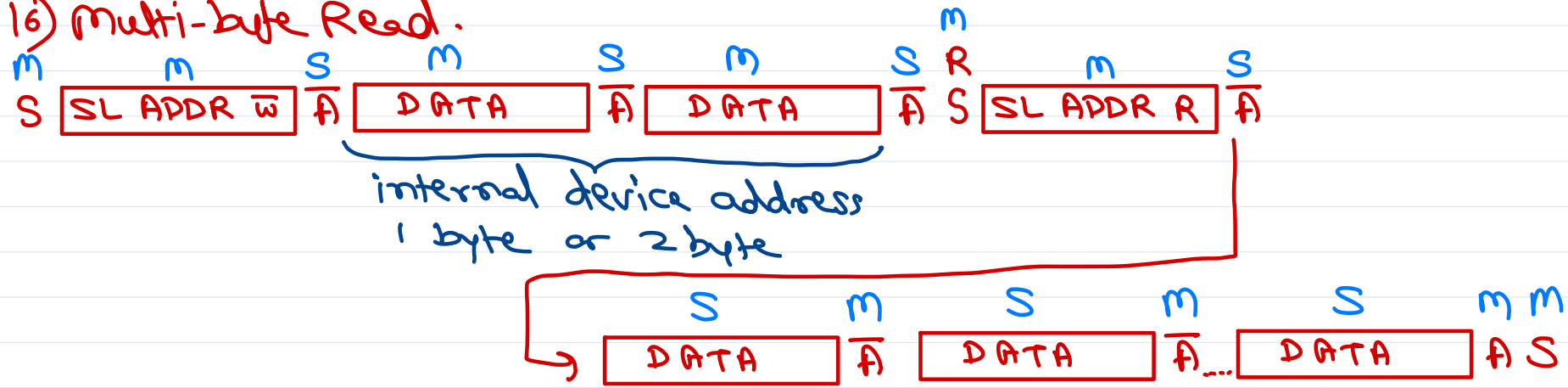




↳ sent immediately after start bit.

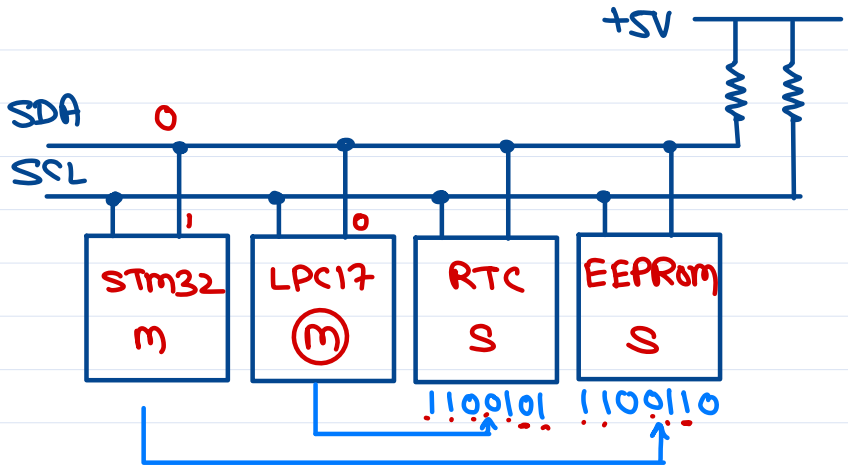
## 15) Multi-byte write.

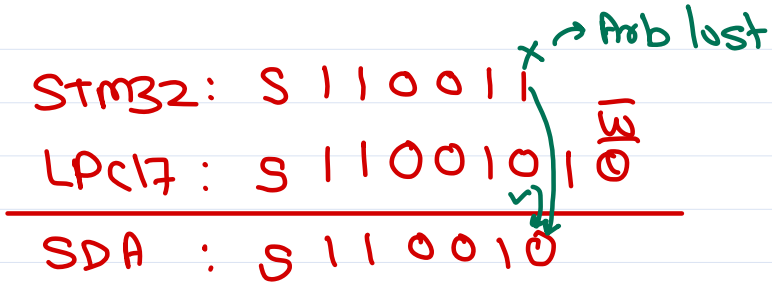



## 16) Multi-byte Read.

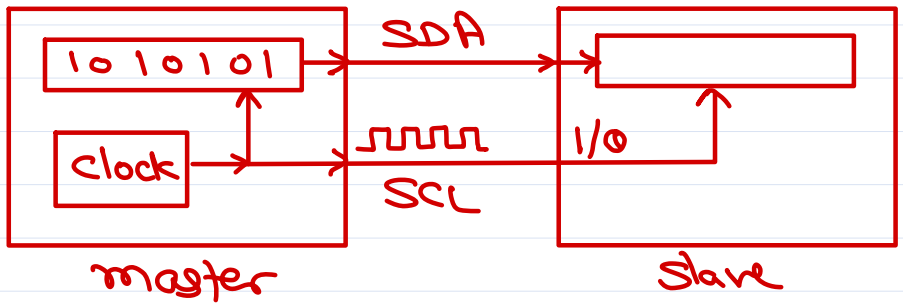


## ⊛ Bus Arbitration




## ⊛ Clock stretching



(19) I2C device is a state machine.

(20) Each operation success/failure is represented by 5-bit status.

(21) Error conditions

- (a) bus error
- (b) ack error
- (c) arbitration lost
- (d) read overrun

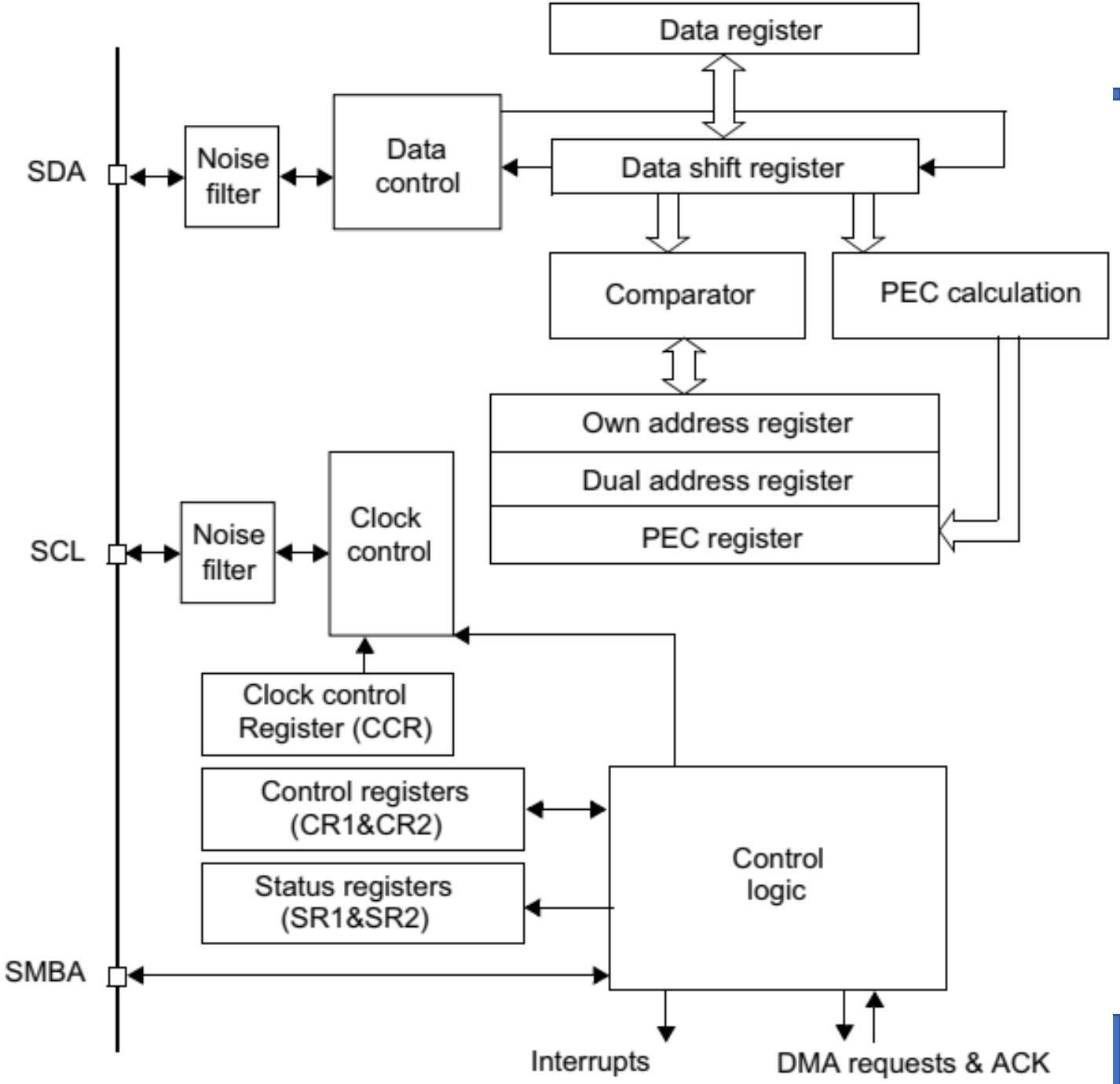
# STM32 I2C

- Multi-master capability: the same interface can act as Master or Slave
- I2C Master features: Clock generation, Start and Stop generation
- I2C Slave features: Dual Addressing Capability, Stop bit detection
- Generation and detection of 7-bit addressing and General Call
- Supports different communication speeds: 100 kHz and 400 kHz
- Status flags: Transmitter/Receiver mode flag, End-of-Byte transmission flag, I2C busy
- Error flags:
  - Arbitration lost condition for master mode
  - Acknowledgment failure after address/ data transmission
  - Detection of misplaced start or stop condition
  - Overrun/Underrun if clock stretching is disabled
- 2 Interrupt vectors: Successful Address/Data communication, Error
- Clock stretching

I2C address
① 7-bit addr
② 10-bit addr

# STM32 I2C

* I2C is a state machine.
* State change after each operation/ error.
* State change is represented in status regr. I2C status is 5 bits.




*Thank you!*

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