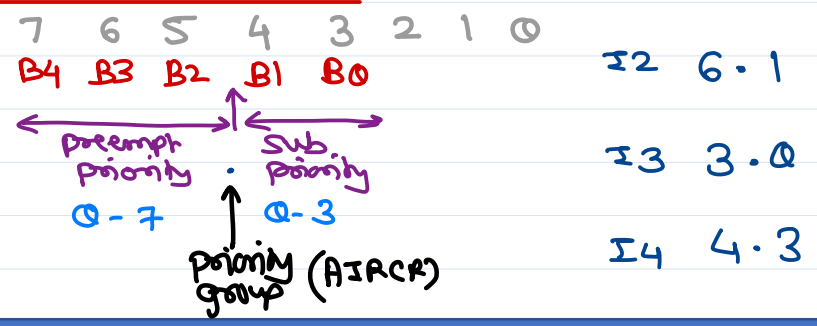
ARM Cortex-M architecture

DESD @ Sunbeam Infotech

Interrupt priority

- Three fixed priority levels i.e. -3 (highest), -2 & -1.
- Up to 256 levels of programmable priority (if 8 bits are used per interrupt).
- More the priority bits increase gate count and hence power consumption.
- Most of chips use 5 bits priority per interrupt (upper 5 bits i.e. [7:3]) in IPR. e.g. LPC17xx
- It enable 32 priority levels.
- Priority levels are divided into two parts
  - ***Pre-emption priority***: Higher pre-emption priority pre-empts current handler.
  - ***Sub priority***: Interrupt handlers are executed in this order, if multiple are pending (of same pre-emption priority).
- Number of bits in pre-emption priority and sub-priority is adjustable via Priority Group setting in NVIC register AIRCR [bits 10:8].
  - PRIGROUP=2 → all 5 bits [7:3] for pre-emption priority.
  - PRIGROUP=4 → 3 bits [7:5] for pre-emption priority and 2 bits [4:3] for sub priority.
  - PRIGROUP=7 → all 5 bits [7:3] for sub priority.
- Refer section 34.4.3.6.1 from LPC1768 user manual.



Thank you!

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