Advanced Micro-controllers - ARM

DESD @ Sunbeam Infotech
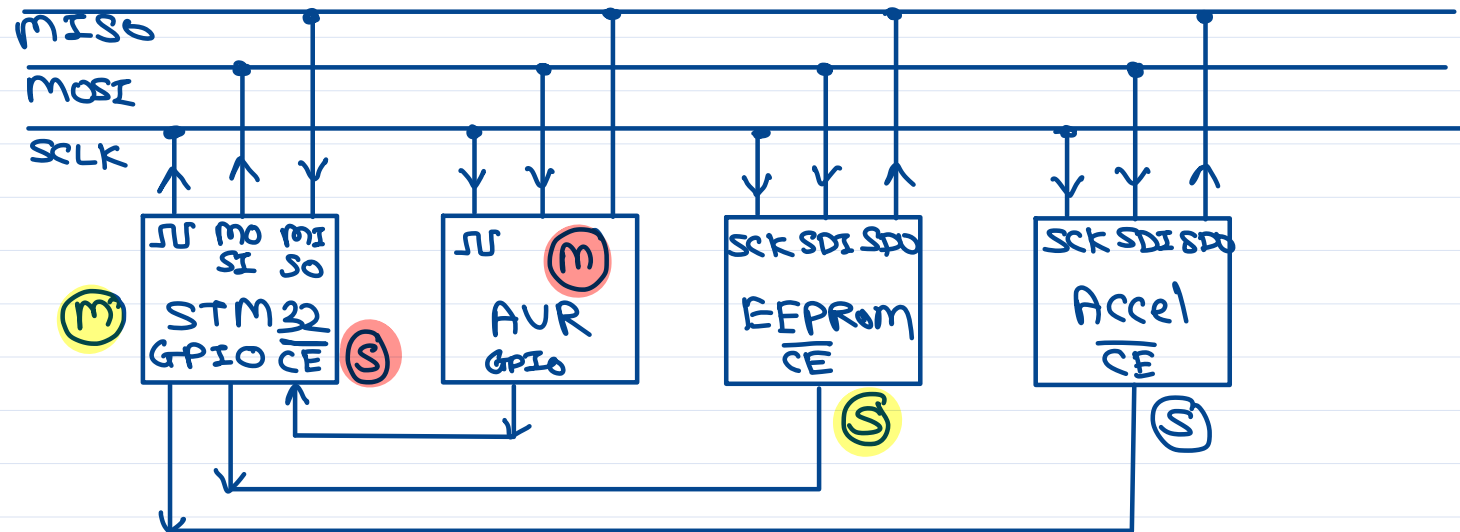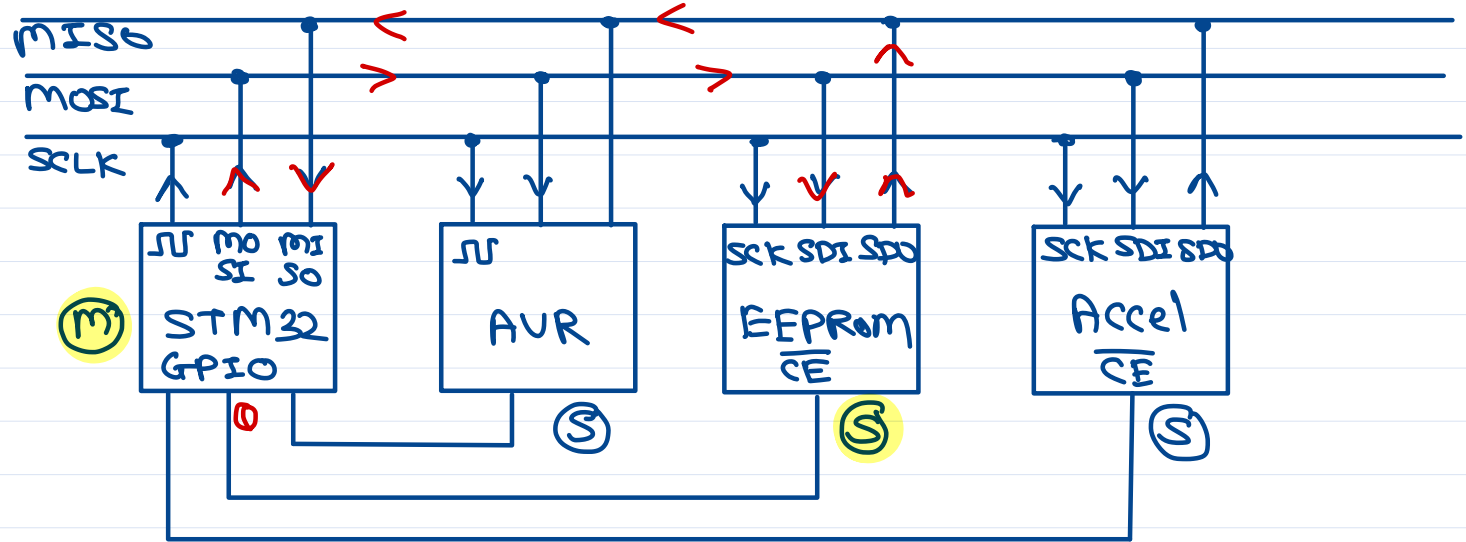
SPI Error Conditions

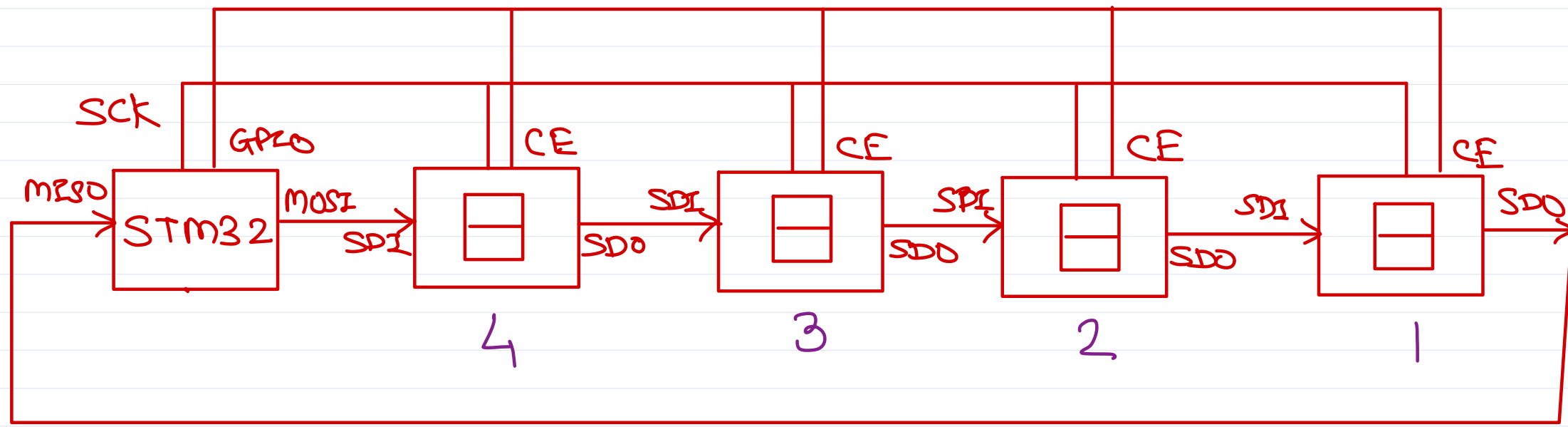① write collision

② read overrun

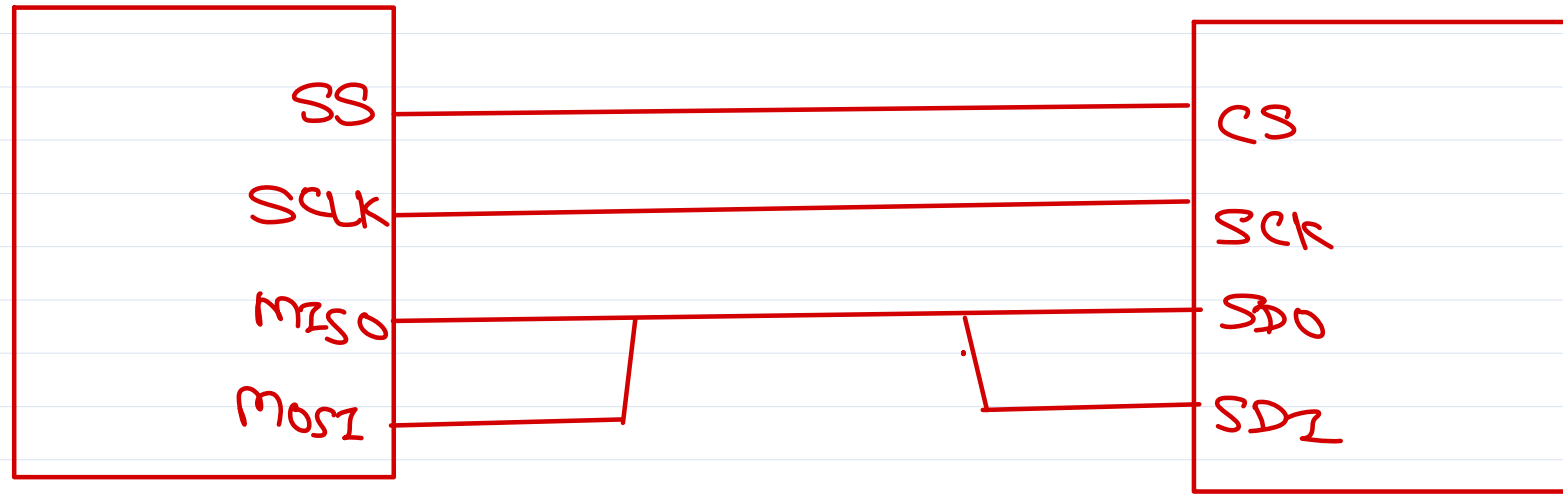③ slave abort
   - error occured in slave device.

④ mode fault
   - when current master device is forced to become slave, by other SPI master.

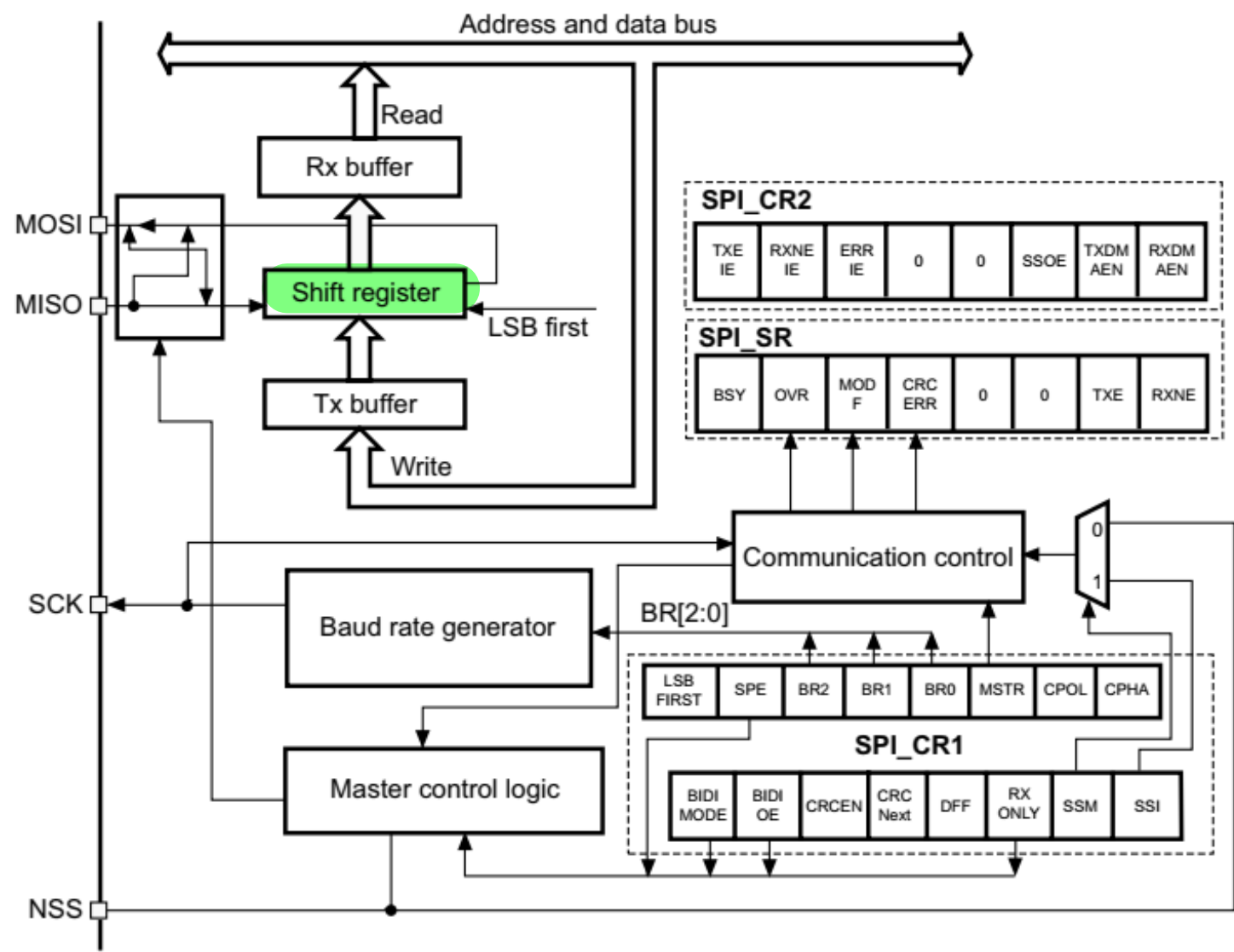# SPI daisy chain

3-wire SPI — Half duplex

STM32 SPI

- 3 SPI ports
- Full-duplex synchronous transfers on three lines
- 8 or 16 bit transfer frame format selection
- Master or slave operation
- Multi-master mode capability
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Dedicated transmission and reception flags with interrupt capability
- SPI bus busy status flag
- Hardware CRC feature for reliable communication:
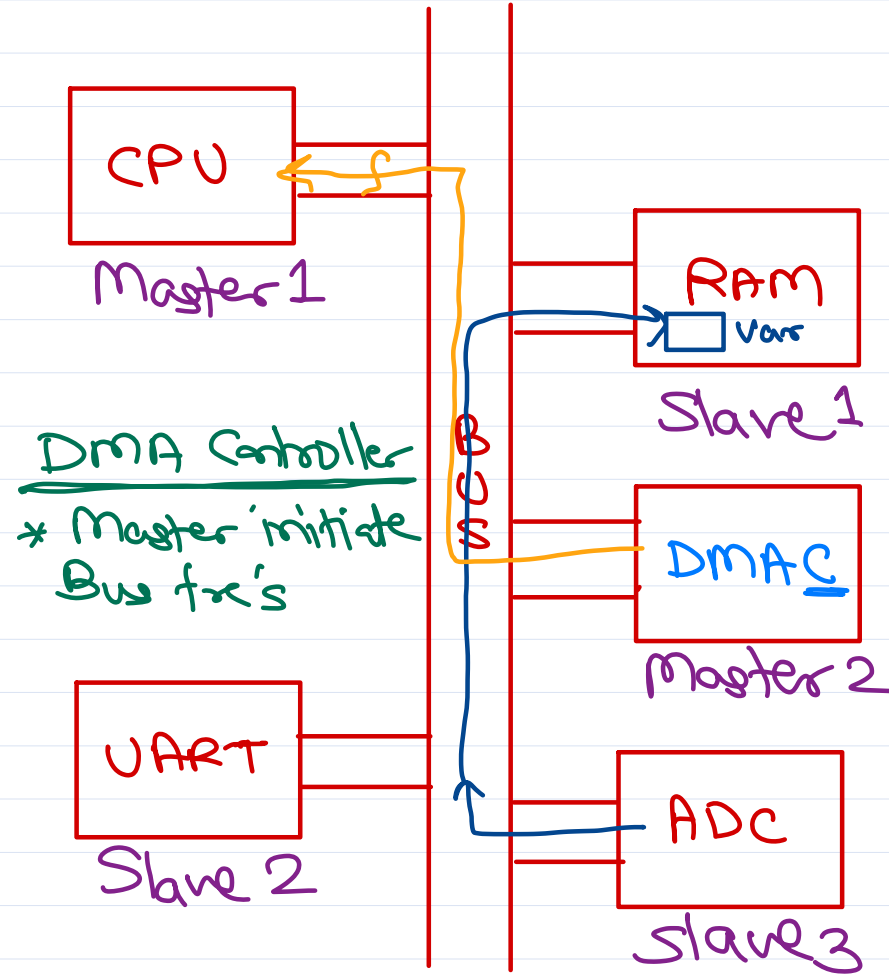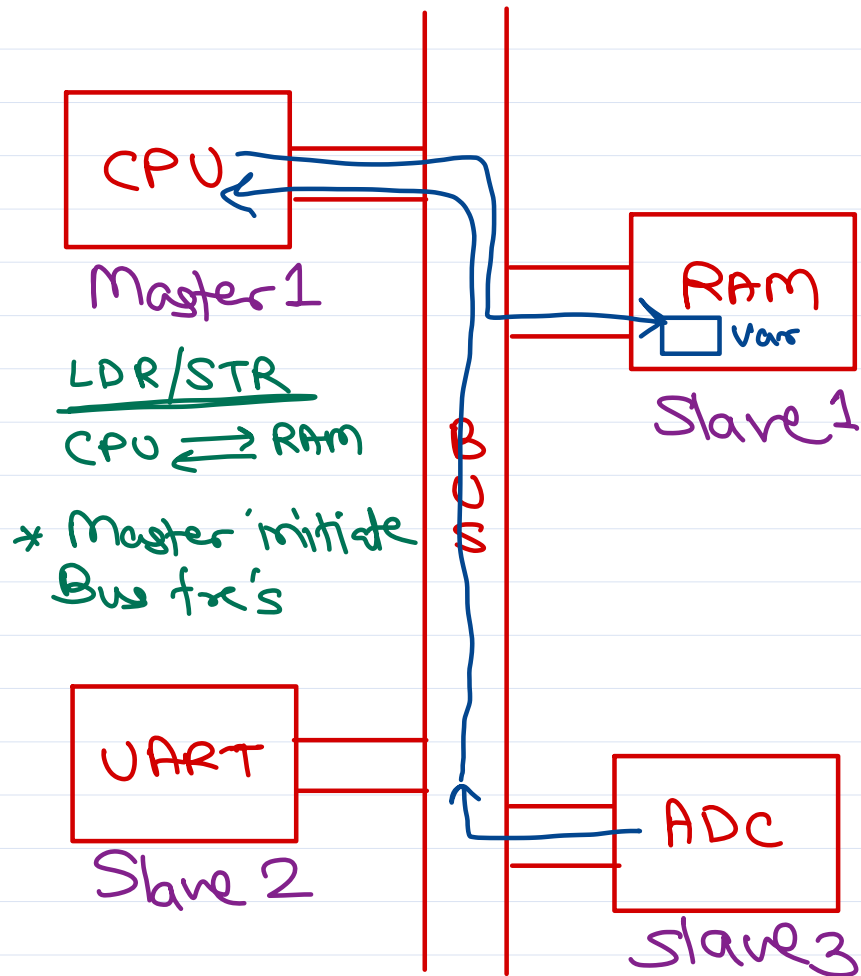- Master mode fault, overrun and CRC error flags with interrupt capability

STM32 SPI

DMA - Direct Memory Access

Bus - Master & Slave

Master 1

LDR/STR
CPU ⇌ RAM

* Master initiate
Bus trx's

Slave 2

Slave 1

Slave 3

Master 1

DMA Controller
* Master initiate
Bus trx's

Slave 2
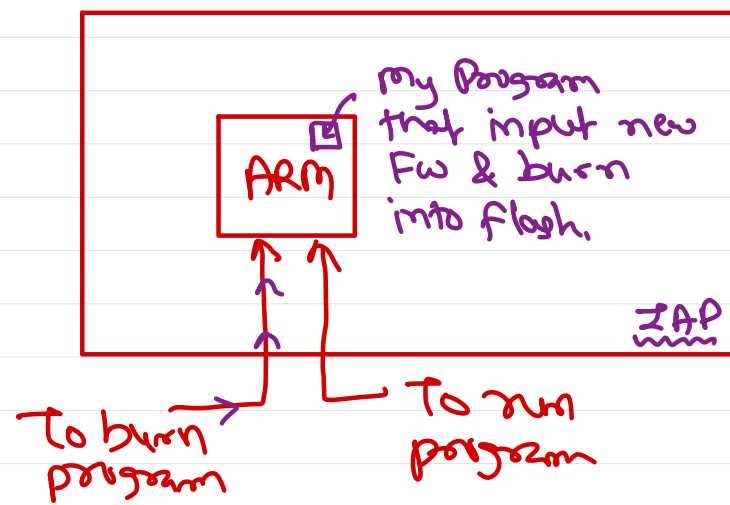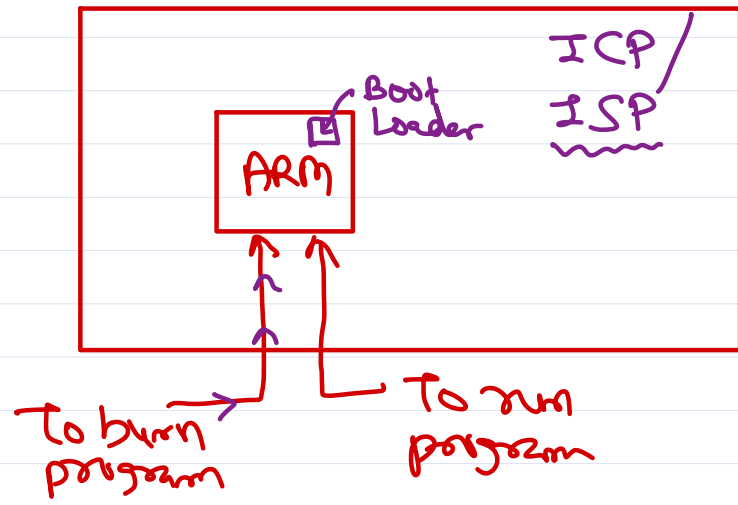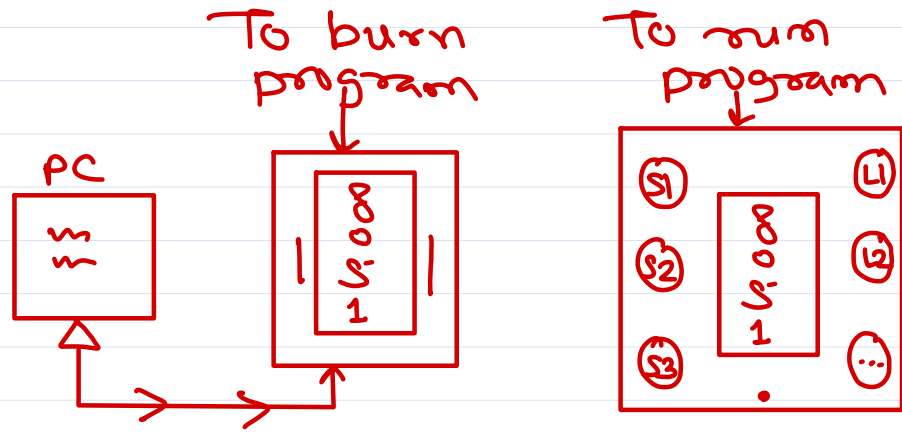
Slave 1

Master 2

Slave 3

DMA controller is responsible for data transfer between memory and peripherals without intervention of CPU.

DMA
1. P2M : Peri → Mem
2. M2P : Mem → Peri
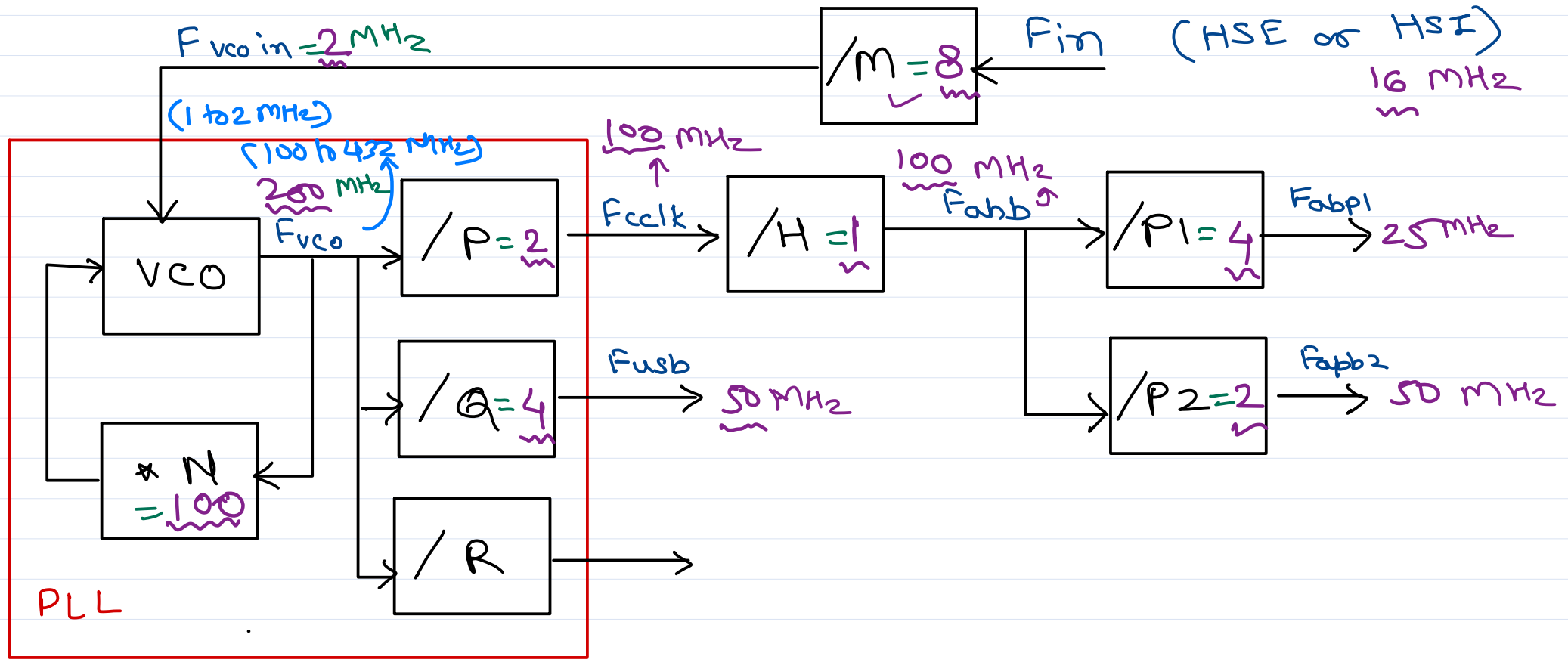3. M2M : Mem → Mem
4. P2P : Peri → Peri

ISP vs IAP

STM32 PLL 100 MHz Config

F vco in = 2 MHz

(1 to 2 MHz)

(100 to 432 MHz)

200 MHz

Fvco

VCO

* N = 100

/P = 2

/Q = 4

/R

PLL

Fcclk

Fusb

100 MHz

/H = 1

50 MHz

100 MHz
Fahb

Fin (HSE or HSI)

/M = 8

16 MHz

/P1 = 4

/P2 = 2

Fabp1

Fabp2

25 MHz

50 MHz

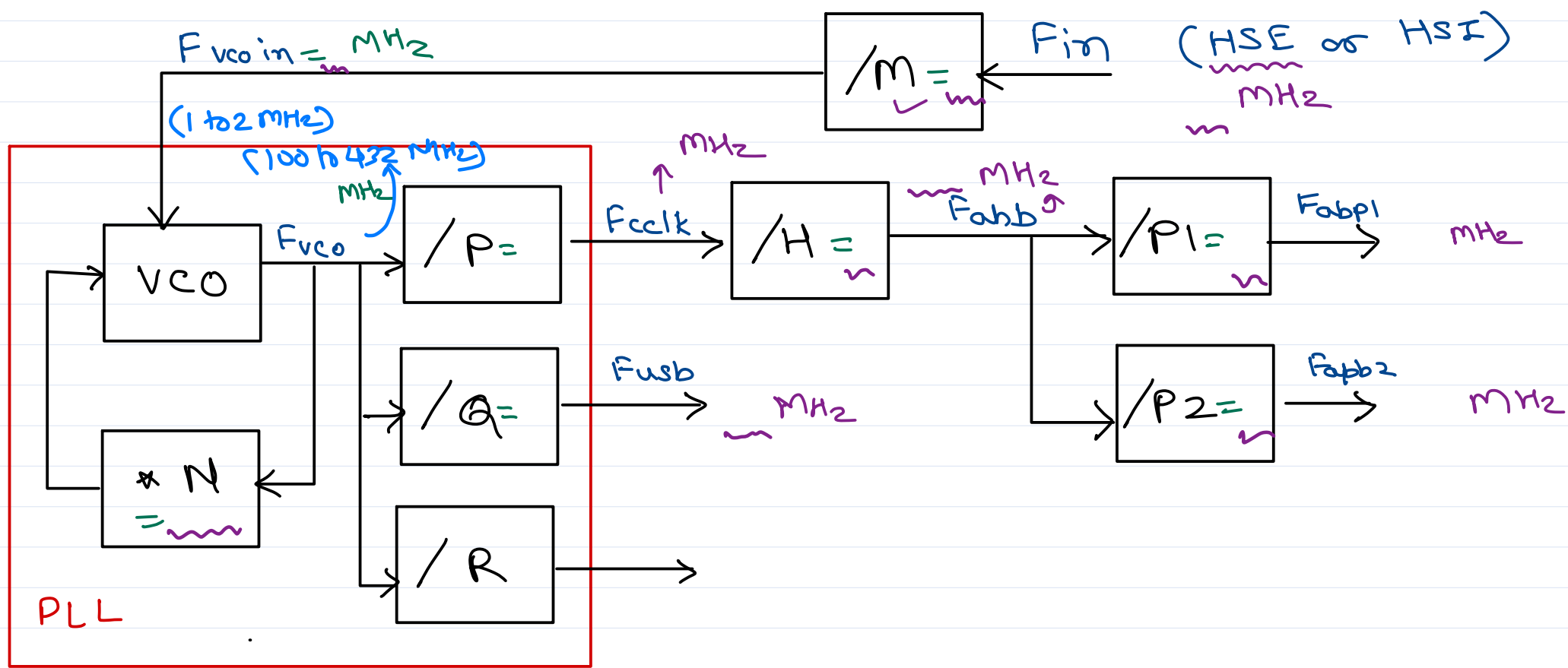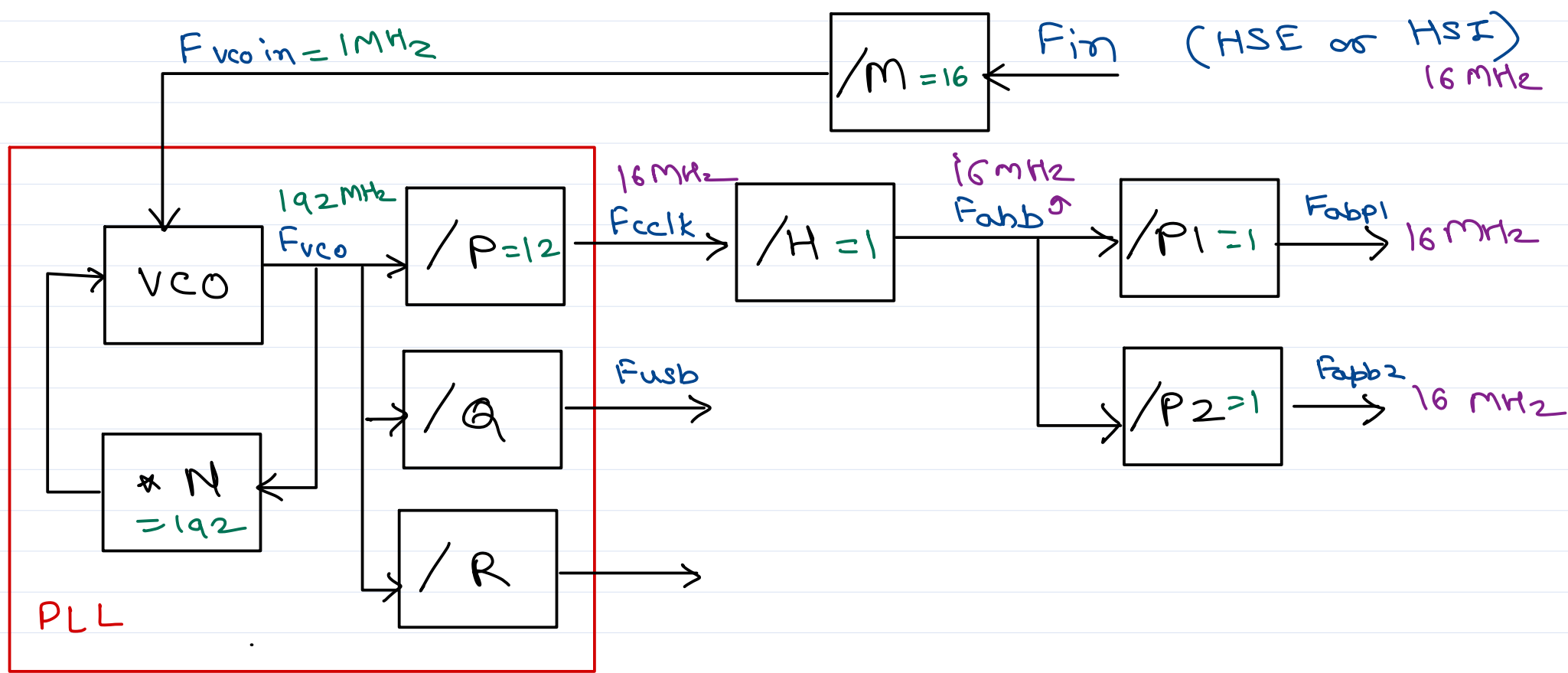# STM32 PLL 168 MHz Config

STM32 PLL Default Config

Thank you!

Nilesh Ghule <nilesh@sunbeaminfo.com>