

The ARM logo consists of the letters "ARM" in a bold, white, sans-serif font, followed by a registered trademark symbol (®). The logo is centered within a solid blue rectangular box.

ARM®

Advanced Micro-controllers - ARM

DESD @ Sunbeam Infotech

struct test {

int a;

char b;

};



struct test2 {

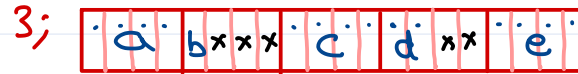
int a;

char b;

int c;

short d;

int e;



ARMv4

100				
104				
108			44	33
112	22	11		
116				

int a = 0x11223344;

&a = 110.

pf("iX", a);

↳ mm 4433

char c1 = 0x44, c2 = 0x33,
c3 = 0x22, c4 = 0x11;

int x = (c1 | (c2 << 8) |
(c3 << 16) | (c4 << 24));

RAM

100				
104	44	33	22	11
108				
112			40	30
116	20	10		
120				

int a = 0x11223344;

addr

data

reg

40	30	20	10
----	----	----	----

addr

data

addr

data

x	x	40	30
---	---	----	----

r1

20	10	x	x
----	----	---	---

r2

int b = 0x10203040;

ARM Ltd

Acorn Computers (UK)
↳ New processor → RISC → 32-bit CPU
↳ ARM
↳ Acorn RISC Machine

- ARM founded in November 1990
 - Advanced RISC Machines
- Company headquarters in Cambridge, UK
 - Processor design centers in Cambridge, Austin, and Sophia Antipolis
 - Sales, support, and engineering offices all over the world
- Best known for its range of RISC processor cores designs
 - Other products – fabric IP, software tools, models, cell libraries - to help partners develop and ship ARM-based SoCs
- ARM does *not* manufacture silicon
- More information about ARM and our offices on our web site:
 - <http://www.arm.com/aboutarm/>



ARM Offices Worldwide



ARM Connected Community – 900+



Connect, Collaborate, Create – accelerating innovation



ISA vs Core

ISA = Instruction Set Architecture.

- ISA → Instruction Execution Engine
 - ↳ Opcode + operand
- Executes machine level instructions.
- Versions: v1, v2, v3, v4, v5, v6, v7, v8.
- a.k.a. micro-architecture.
- Doesn't include Flash, RAM, Cache, MPU/MMU.

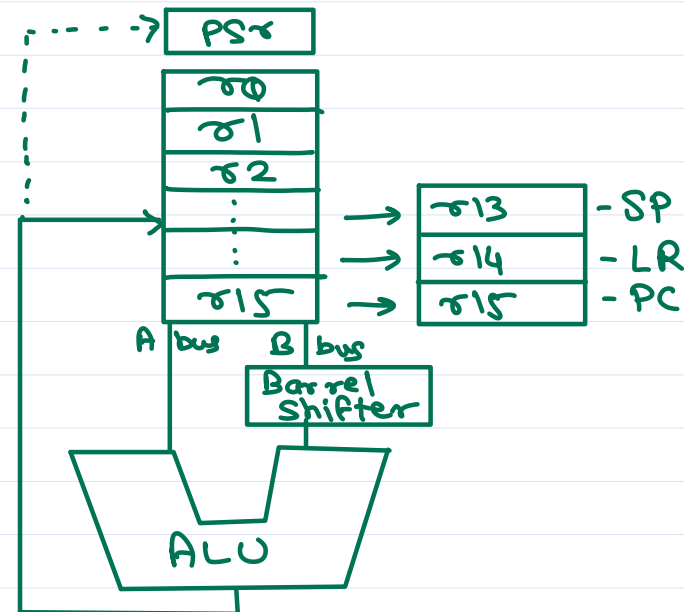
Core = ISA + Cache + MPU/MMU +
Debug facility + buses + ...

- based on some ISA.
- versions: ARM7, ARM9, ARM10, ARM11,
Cortex-A8, Cortex-M3, Cortex-M4, ...
- ARM v4 → ARM7 and ARM9
(~~MMU~~) (MMU)

MC = Core + Flash + SRAM + Peripherals.

- ✓ e.g. STM32F407VG (CM4)
- LPC1768 (CM3)
- LPC2148 (ARM7)
- AM335x (CA8)

In general, ARM core (basic).



ARM arch

word = 32 bit

half-word = 16 bit

byte = 8 bit

ARM Instructions

① ARM Instruction Set

- each instruction is 32-bit

→ $ADDEQ\ R0, R1, R2$ | $ADD\ R0, R1, R2, \#2$

② Thumb Instruction Set

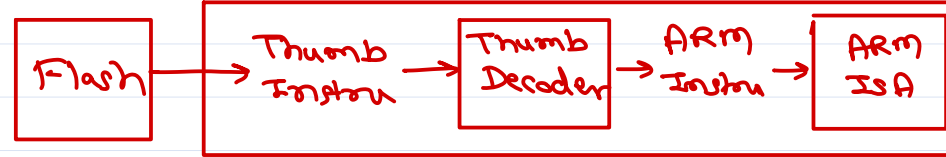
- each instruction is 16-bit
- increased code density

- Thumb limitations:

- ① cannot used for exception handling
- ② cannot manipulate status register
- ③ not all instrn can access all registers (limited regs: r0-r7)
- ④ Conditional exec not possible.
- ⑤ Inline barrel shift not supported.

- Needs 70% less code space.

ARM v4 T



SLAS: Thumb encoding / ARM encoding

ARM processor state

① ARM state

- fetch 4 byte instrn from flash

- $PC = PC + 4$

- PC is multiple of 4 $[31 \dots 2 \overset{1}{0} \overset{0}{0}]$

② Thumb state

- fetch 2 byte instrn from flash

- $PC = PC + 2$

- PC is multiple of 2 $[31 \dots 1 \overset{0}{0}]$

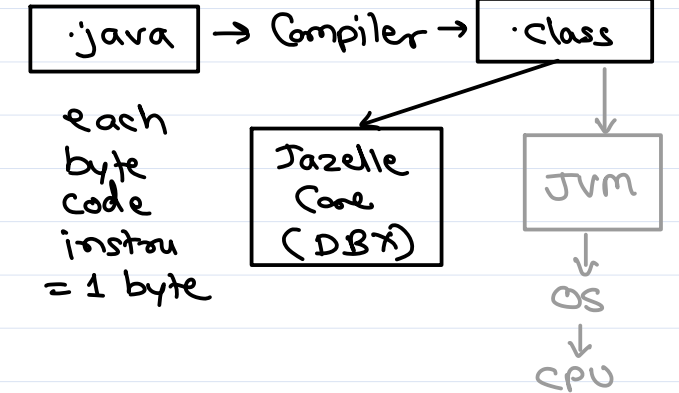
ARM - Thumb interworking: Instructions to switch from ARM to Thumb state & vice versa - BX label, BLX func

label/func → addr → is loaded in PC

& last bit (0) indicate state

0: ARM state
1: Thumb state

③ Jazelle state



✓ PC is multiple of 4.
✓ each time 4 instrns (4 bytes) are fetched from code memory.

Development of the ARM Architecture

ARM modes

- ① SVC
- ② IRQ
- ③ FIQ
- ④ Undef
- ⑤ Abt
- ⑥ User



Early ARM architectures

Apple Newton PDA

Halfword and signed halfword / byte support



(Intel) Strong ARM

SA-110

SA-1110

System mode

Thumb instruction set



LPC2148

ARM7TDMI

ARM9TDMI

ARM720T

ARM940T

+ mmu

Improved ARM/Thumb Interworking



Enhanced DSP

CLZ
Count leading zero.

Saturated maths - USAT, SSAT

DSP multiply-accumulate instructions

MLA
($w = x \times y + z$)

ARM1020E

XScale

Motorola
FreeScale

ARM9E-S

ARM966E-S

Jazelle

Java bytecode execution (PBT)



ARM9EJ-S

ARM926EJ-S

ARM7EJ-S

ARM1026EJ-S

Single Instru Multiple Data
SIMD Instructions
e.g. QADD8, ...

Multi-processing

V6 Memory architecture (VMSA)

Multi-Core
Virtual memory System Architecture



Unaligned data support

ARM1136EJ-S



Thank you!

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