

E2-63170-Vaibhav Lohar

Q. What is difference between microcontroller and microprocessor?

### Microcontroller

- Dedicated processing chip.
- It contains CPU, RAM, ROM, peripherals (timers, gpio, adc, dac, spi, i2c, can etc) on same chip.
- Usually works on lower clock speed & hence lower power consumption.
- Require less space & cost.
- Cannot customize a controller but can choose from variety of controller as per need.
- Used in application-specific systems.

### Microprocessor

- General purpose computing machine / chip.
- It contains CPU [ALU, registers], cache & MMU.
- usually works on higher clock speed & hence higher power consumption.
- Require more space & cost.
- Designer can choose required amount of RAM, ROM & peripheral.
- Used for general purpose applications.

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Q2. What is difference between I/O mapped I/O & Memory mapped I/O ?

### Memory Mapped I/O

- I/O Devices (SFRs) are mapped as memory addresses (in memory address space). Memory and I/O addresses are not overlapping.
- I/O registers are accessed with same instructions as of memory e.g. MOV, LD/ST
- There is no differentiation between memory locations & I/O registers, except by address.
- e.g.: ARM

### I/O Mapped I/O

- I/O devices (SFRs) are mapped as separate I/O addresses (in different space). Memory & I/O addresses may be overlapping.
- I/O registers are accessed with special instruction e.g. IN/OUT
- Memory locations & I/O registers are differentiated by different buses or control signal e.g. IO/M
- e.g.: X86 architecture

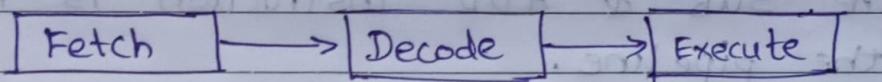
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3. What is pipeline? What are limitations? Explain pipeline in ARM architecture.

A pipeline is the mechanism used by RISC processors to execute instructions by speeding up the execution by fetching in instruction while other 3 instructions are being decoded and executed simultaneously.

Limitations :-

- ① Designing of the pipeline process is complex.
- ② Instruction latency increases.
- ③ Longer the pipeline, the problem of hazard for branch instruction.



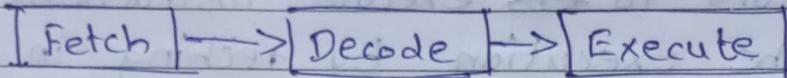
- Fetch loads an instruction from memory.
- Decode identifies the instruction to be executed.
- Execute processes the instruction & writes the result back to register.

: Pipeline, is a design technique or a process which plays an important role in increasing the efficiency of data processing in the processor of computer & microcontroller. By keeping the processor in continuous process of fetching, decoding & executing...

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4 What is ARM 7 Pipeline? What are limitations of pipeline.

ARM 7 Pipeline : Three stage pipeline.



- The three instruction are placed into the pipeline sequentially
- In the first cycle the core fetches the ADD instruction from memory.
- In second cycle the core fet feches the SUB instruction & decodes the ADD instruction
- In the third instruction cycle, both the SUB & ADD instruction is moved along the pipeline.
- The ADD instruction is executed the SUB instruction is decoded , and the CMP instruction is fetched . This processor is called as pipeline.

Time	Cycle 1	ADD		
	Cycle 2	SUB	ADD	
	Cycle 3	CMP	SUB	ADD

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5 What is difference between Fast GPIO and Legacy GPIO?

### Legacy GPIO

### Fast GPIO

- Connected to peripheral BUS (APB).
  - Work at lower speed i.e. peripheral speed.
  - Word (32-bit) accessible.
  - No Mask/lock feature.
- Connected to ARM core BUS (AHB).
  - Work at higher speed i.e. ARM core speed.
  - Word (32 bit), Half word(16-bit), or byte (8 bit) accessible.
  - Mask/lock feature to avoid accidental changes in GPIO pins.

6 What is difference between Von-Neumann & Harvard Architecture.

### Von-Neumann

### Harvard

- Address & Data bus is common for program memory (ROM) and data memory (RAM).
- Separate address & data buses for program memory ROM and data memory (RAM).

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<ul style="list-style-type: none"> <li>Instruction &amp; data cannot be fetched simultaneously.</li> <li>Op code &amp; operands are not fetched in single cycle so slower execution.</li> <li>Unified Cache (i.e common cache for instruction &amp; data)</li> </ul>	<p>Instruction &amp; Data can be fetched simultaneously.</p> <p>Op code &amp; operands are fetched in single cycle so faster execution.</p> <p>seperate cache for instruction &amp; data.</p>
e.g X86 architecture.	AVR architecture.

7 Explain ARM cortex M Modes ? Explain Register banking Why FIQ is faster than IRQ?

→

ARM cortex M supports ~~two~~ following two modes

- Thread Mode
- Handler Mode.

• Thread Mode :

- User program or embedded os execution mode.

- It uses privileged or Non-privileged access level .

• Privileged level - embedded os.

• Non-privileged level - user program.

• While using cortex M as a bare metal programming , only privileged access level is used.

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- Handler mode :
  - When exception/interrupt occurs, core enters in handler mode.
  - Exception Handler is executed in this mode.
  - After handler completion, it returns to thread mode.
  - It uses privileged access level.

### \* Register Banking :

- ALL 37 registers in the register file, of those 20 registers are hidden from a program at different times. These are called banked registers.
- They These registers are available only when the processor is in a particular mode.

\* If FIQ & IRQ raised at same time, FIQ will be handled first, Because FIQ has higher priority.

- FIQ mode has separate set of General purpose register (r8 - r12), No need to save
- Last entry in EVT (Exception Vector Table) is FIQ. So instead of jump instruction we can place FIQ handler directly from that address.
- Usually single peripheral is configured as FIQ.
- FIQ handler can directly start handling the interrupt.

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8 Explain protocols in detail : RS232, I2C, SPI, PS2

- RS232 :

- RS stands for Recommended standard.
- To allow compatibility among data communication equipment made by various manufacturers, an interfacing standard called RS232 was set by the Electronics Industries standard in 1960.
- Today RS232 is one of the most widely used serial I/O interfacing standards. This standard is used in PC's & numerous types of equipment.

- Physical characteristics :

- Types

- Full-duplex communication.
    - peer to peer.
    - Connection wires

• There are three wires used to connect devices.

• Tx - Transmit, Rx - Receive, GND.

• Connectors - DB-25 and DB-9.

• In old times DB-25 is used.

• Standard DB-9 connector.

• Half serial cable : only 3 wires connected Rx, Tx, Ground.

• Full serial cable : 9 wires connected.

• Rx, Tx, Ground.

• CTS, RTS

-- Handshaking signal

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- Voltage & current levels
  - NRZ (Not Returning zero)
  - CMOS voltage levels.
    - +3V to +25V -- Logic 0 -- Space.
    - -3V to -25V -- Logic 1 -- Mark.
  - TTL Voltage (0V=0 and 5V=1) → RS 232 Line Driver → CMOS' Voltage levels.
  - TTL ↔ MAX 232 → CMOS.
- Bit Rate / Baud Rate.  
standard baud rate : 9600, 38400, 115200, ...

Logical characteristics :

Data frames

Start bit → Always 0.

Data bits → 5 to 9 bits -- LSB Tx First.

Parity bits → Even / Odd / 1 / 0 / No.

stop bits → always 1.

I<sub>2</sub>C

The I<sub>2</sub>C (Inter Integrated Circuit) is a bus interface connection incorporated into many devices such as sensors, RTC & EEPROM.

• Types

- It is a bus protocol (Master slave).
- It uses Half duplex communication.

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- Wires / connectivity  
2 wired protocol.  
SDA - Serial Data.  
SCL - Serial clock.
- It uses TTL voltage level.
- Frequency
  - 100 kHz - standard mode.
  - 400 kHz - Fast Mode.
  - 1 MHz - Fast plus mode.

### I2C Device modes.

Master Transmitter.

Master Receiver.

Slave transmitter.

Slave Receiver.

### • Data frame

- 8 bit Data bits + Acknowledgment.
- Transmitter  $\rightarrow$  8 bits Data bits + (Ack=1)  
-- Receiver.

### • Address frame

- 7 I2C Addr bits + Read/Write + ACK.
- Master  $\rightarrow$  7 I2C - Addr bits + Read/Write  
+ (ACK=1)  $\rightarrow$  slave
- Slave  $\rightarrow$  (ACK=0) + Acknowledge  $\rightarrow$  Master

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## SPI :

The SPI (Serial Peripheral interface) is a bus interface connection incorporated into many devices such as ADC, DAC and EEPROM.

### Types

Uses full Duplex protocol.

Bus Protocol.

Wires / connectivity

4 wire protocol

MOSI

MISO

SCLK

Internal block diagram

single shift register is used for full duplex communication.

### Voltage levels

TTL voltage - 0V = Logic 0      3.5V = logic 1

Frequency - High Speed

### Logical Characteristics

Data bit transfer.

C POL --> Clock Base

C PHA --> Leading / Trailing Edge.

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### Data frame :

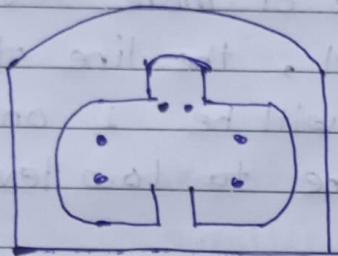
- Single byte transfer
  - slave selection is responsibility of the master.
  - $SS = 0 + MOSI \rightarrow 8$  Data bits  $\rightarrow MISO + SS = 1$ .
  - $SS = 0 + MOSI \Leftarrow 8$  Data bits  $\Leftarrow MISO + SS = 1$ .
- Multi - byte Write
  - Master sends internal address (1 byte or 2 byte) followed by number of data bytes.
  - $SS = 0 +$  Master  $\rightarrow Addr1, Addr2, Byte1, Byte2,$   
 $\dots$   $ByteN \rightarrow$  Slave  $+ SS = 1$
- Multi - byte Read
  - Master sends internal address (1 byte or 2 byte) and then slave send number of data bytes.
  - $SS = 0 +$  Master  $\rightarrow Addr1, Addr2 \rightarrow$  Slave + slave  
 $\rightarrow Byte1, Byte2, \dots, ByteN \rightarrow$  Master  $+ SS = 1$

### PS2 :

- The PS2 Port is used for connecting keyboard & mic to a PC. It is introduced in 1987 by IBM. The main purpose of replacing the serial keyboard & mouse.
- In our days PS2 port was replaced by USB port, which is more easy to implement on a PC even though PS2 offers more capability & greater speed.

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- PS2 Connector color code.
- PS2 Mini-DIN connector has 6 pin & carries a serial signal at frequency starting from 10 upto 16 KHz with one start bit, one stop bit & one parity bit



Pin 1 - Data

Pin 2 - Not connected

Pin 3 - Ground

Pin 4 - VDC +5V at 275mA

Pin 5 - clock

Pin 6 - Not connected

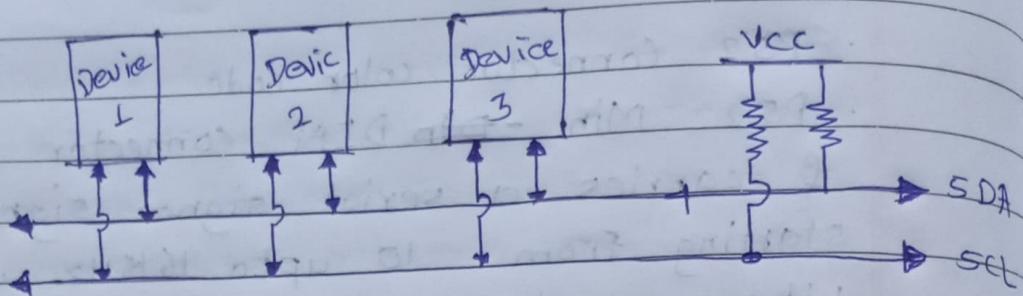
- PS2 Protocol is a Bi-directional serial synchronous protocol.
- When the data & clock lines are High the bus is idle & the keyboard / mouse can begin transmitting data.

9. What is wired AND in I2C? What is clock stretching? What is bus arbitration?

Wired AND:

- I2C devices use only 2 bidirectional open-drain pins for data communication.
- To implement I2C, only a 4.7 kilohm pull-up resistors for each of bus lines is needed.
- This implements a wired AND, which is needed to implement I2C protocols.

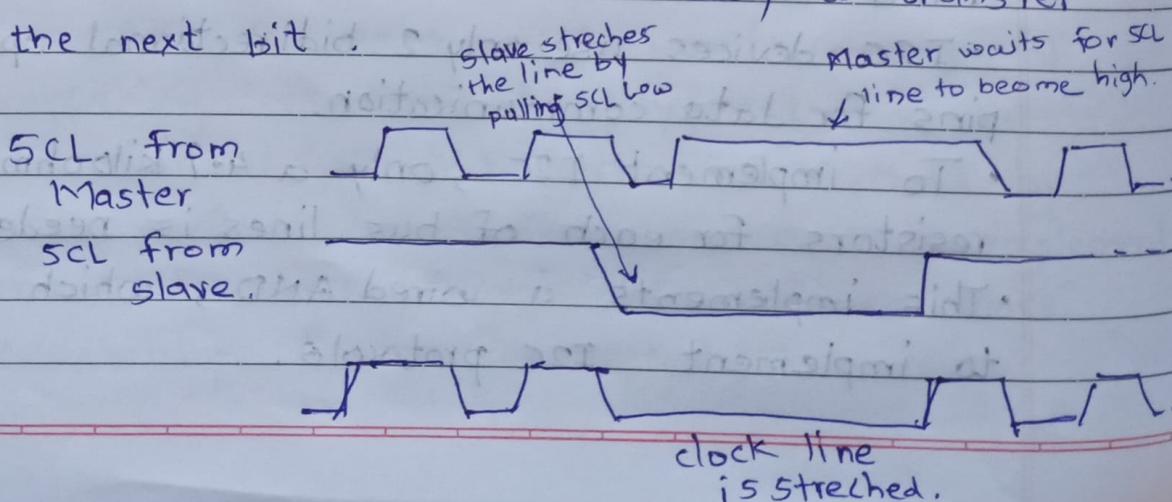
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- This means that if one or more devices pull the line to low (zero) level, the line state is zero and the level of line will be 1 only if none of devices pull the line to low level.

### clock stretching :

- One of the features of the I2C protocol is clock stretching.
- It is kind of flow control.
- If an addressed slave device is not ready to process more data it will stretch the clock by holding the clock line (SCL) low after receiving (or sending) a bit of data.
- Thus the master will not be able to raise the clock line (because devices are wire anded) and will wait until the slave releases the SCL line to show it is ready to transfer the next bit.



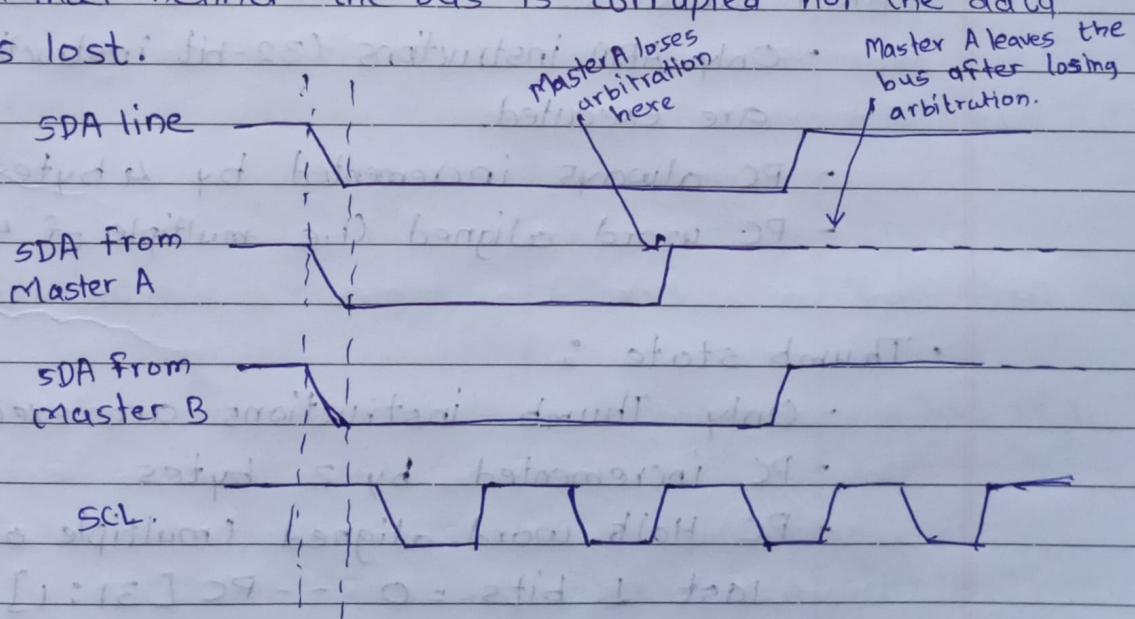
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## Arbitration :

I<sup>2</sup>C protocol supports a multimaster bus system. This doesn't mean that more than one master can use the bus at the same time. Rather, each master waits for the current transmission to finish & then starts to use the bus.

But it is impossible that two or more masters initiate a transmission at about the same time. In this case the arbitration happens.

- Each transmitter has to check the level of the bus & compare it with the level it expects, if it doesn't match, that the transmitter has lost the arbitration and will switch to slave mode.
- In case of arbitration, the winning master will continue its job.
- In that neither the bus is corrupted nor the data is lost.



1-2-3-0-T = what all goes?

what is going happening?

what happens to the slave?

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10 Which Programmer you have used for ARM?

We used ST-LINK/V2 is an In circuit debugger & programmer for STM32 micro-controller.

- The single wire interface module and JTAG/serial/wire debugging interface are used to communicate with STM32 mcu located on application board.

11 What are ARM Processor states?

There are Three state in ARM.

- ARM state

- Thumb state

- Jazelle state

• ARM state :

- Only ARM instructions (32-bit instruction) are executed.

- PC always incremented by 4 bytes.

- PC word aligned (i.e. multiple of 4bytes)

• Thumb state :

- Only Thumb instructions are executed.

- PC incremented by 2 bytes

- PC Half word aligned (multiple of 2 bytes)  
last 1 bits = 0 -- PC [31:1].

• Jazelle state = T=0 & S=1

- PC incremented by 4 bytes

- Multiple bytecode instructions are fetched at once

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12. Compare ARM, AVR, PIC & 8051 controllers.

	8051	PIC	AVR	ARM
① Bus width	8 bit	8/16/32 bit	8/32 bit	32/64 bit
② Comm' protocol	VART, USART SPI, I2C	PIC, VART, USART LIN, CAN, SPI	VART, USART, SPI, I2C, CAN	UART, USART, LIN, I2C, SPI, USB, Ethernet, I2S, DSR
③ speed	12 clock instruction cycle	4 clock instruction cycle	1 clock instruction cycle	1 clock instruction cycle.
④ Memory	ROM, SRAM, FLASH	SRAM, FLASH	Flash, SRA, EEPROM	Flash, SDRAM, EEPROM.
Power consumption	Average	Low	Low	Low
Families	8051	PIC 16, PIC 18, PIC 24	Tiny, Atmega	ARM V4, 5, 6, 7
Manufacturer	INTEL, Atmel	Microchip	Atmel	Apple, Qualcomm
Cost	Very low	Average	Average	High

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13. IN 8086 Architecture What is difference in SP, BP and SS registers?

• Stack Pointer :

- stack pointer pointing to the program stack.
- It is usually used to store information about the memory segment. SP points current stack top.

• Base pointer :

- This is base pointer register pointing to data in stack segment.
- Base pointer access data in the other segment.

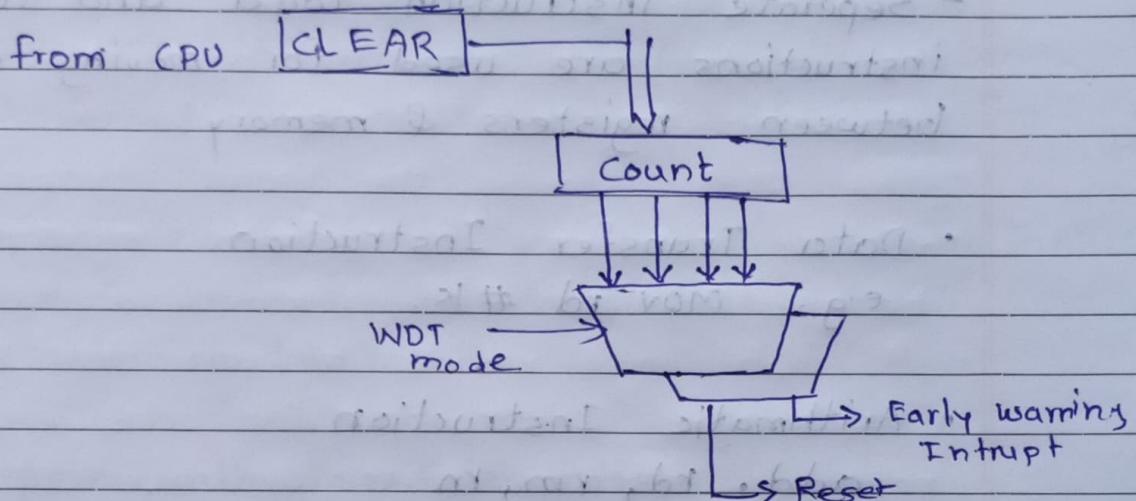
• Stack Segment (SS) :

- The stack segment register (SS) is usually used to store information about the memory segment that stores the call stack of the current executed program.

14 Explain watch dog timer & brown out detection

- A watchdog timer (WDT) is an embedded timing device. A software hang or is lost, WDT reset the system microcontroller via a 16 bit counter.
- A WDT is also known as computer operating property (COP) timer.

- WDT are widely used in computers to facilitate automatic correction of temporary hardware fault.
- WDT microcontroller to recover from catastrophic software errors such as a run-away code or a dead deadlock condition.



If the WDT **CLEAR** register is not updated by the application within the allocated time then reset signal is generated.

### Brown Out Detection

In Brown out is used to describe a dip or drop in voltage supply. A black out is when there is a total voltage loss.

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15 Explain the instruction set for ARM in detail.

- The ARM has a load store architecture means that all arithmetic and logical instruction take only register operands.

- Separate instruction load and store instructions are used for moving data between registers & memory.

- Data Transfer Instruction.

e.g.:  $\text{Mov rd} \#k$ .

- Arithmetic Instruction.

add, rd, rm, rn

- Logical Instruction.

$\text{ANA } B \rightarrow A \leftarrow A \text{ AND } B$

- Conditional branching

$\text{cmp rm, rn}$

- Thumb-2 If then instruction.

$\text{movgt rd, rm}$

- Barrel shifter

LSL, ASR, LSR, ROR, RRX.

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17 What is the use of AMBA interface & explain it in detail?

- AMBA (Advanced Microcontroller Bus Architecture).
- It is freely available, open standard for the connection & management of the functional blocks in a system-on-chip (soc)
- Advanced Extensible Interface.
- Advanced High performance bus.

18 What are the types of addressing modes in ARM?

→ ① Register Indirect Addressing Mode;

LDR R0, [R1]

② Register with immediate offset

LDR R0, [R1], #20

③ Pre - Index Addressing Mode.

LDR R0, [R1, #4]

④ ARM's Auto indexing Post - Index

LDR R0, [R1], #4

⑤ PC Relative A.M.

LDR R0, [R15, #24]

⑥ ARM's Load & Store Encoding

LDREQ R3, [R4]

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19 What is translation lookaside buffer (TLB) ?

Translation Lookaside Buffer (TLB):

- A translation lookaside Buffer (TLB) is a memory cache that is used to reduce time taken to access a user memory location.
- It is a part of the chip's memory management unit (MMU).
- The TLB stores the recent translations of virtual memory to physical memory and can be called an address - translation cache.
- A TLB may reside between the CPU & the CPU cache , between CPU cache & the main memory or between the different levels of the ~~the~~ multi-level cache.

20 What is single issue multiple data (SIMD) processing ?

- Single instruction , multiple data (SIMD) is a type of parallel processing in Flynn's taxonomy.
- ARM NEON technology is an advanced single instruction multiple data (SIMD) architecture extension for the ARM Cortex -A & Cortex -R series processors.

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- Neon registers are considered as vectors of elements of the same data type, with Neon instructions operating on multiple elements simultaneously.
- NEON is a wide SIMD data processing architecture.
- Extension of the ARM instruction set (V7-A)
- $32 \times 64$  bit wide registers.
- NEON instruction perform "Packed SIMD" processing.

21. How will you allow Thumb code to call the ARM assembly code?

- Thumb code together for both assembly & C/C++.
- To call thumb routine from ARM routine. The core has to change its state. This state change is shown in the T bit of the CPSR.
- The BX & BLX instruction caused a switch between ARM & Thumb state while branching to routine.
- The Thumb BX instruction does the same syntax -  $\text{BX Rm}$

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22. What is the use of 'SWI' in ARM assembly?

- The SWI instruction causes a SWI exception.
- This means that the process state changes to ARM.
- The processor mode changes to supervisor, the CPSR is saved to the supervisor mode SPSR, & execution branches to the SWI vector.
- Syntax :

SWI {cond} imm32

cond : is an optional condition code.  
imm32 : is an expression evaluating to an integer in the range.

23. Tell about the Exception Handling in ARM processor. What does the ARM core do automatically for every exception?

Exception types :

Reset

Non Maskable Interrupt (NMI)

Fault

PendSV

SVCALL

External Interrupt

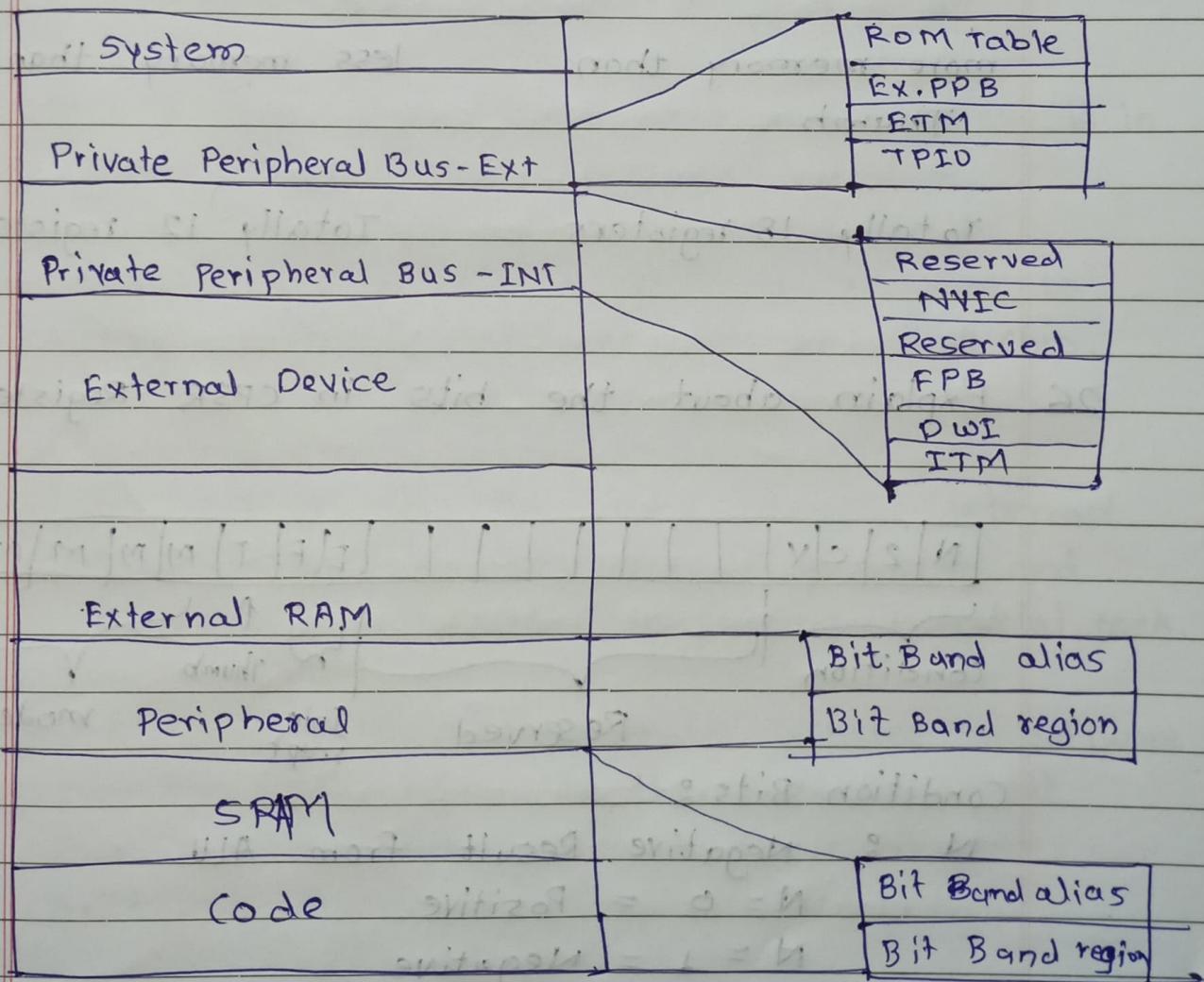
Systick Interrupt

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## 24 Explain Memory map in ARM architecture.

The predefined memory map also allows the cortex - m3 processor to be highly optimized for speed ease of integration in system-on-a-chip (soc design).

Overall the 4GB memory space can be divided into range as shown in picture.



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25 Explain difference between ARM or Thumb Mode.

ARM Mode

Thumb Mode

ARM Mode is states  
that T bit of CPSR  
is 0.

Thumb mode is status  
that T bit of CPSR is 1.

ARM provide 32 bit  
instruction set

Thumb mode fetches  
instruction by 2 byte.

more memory than

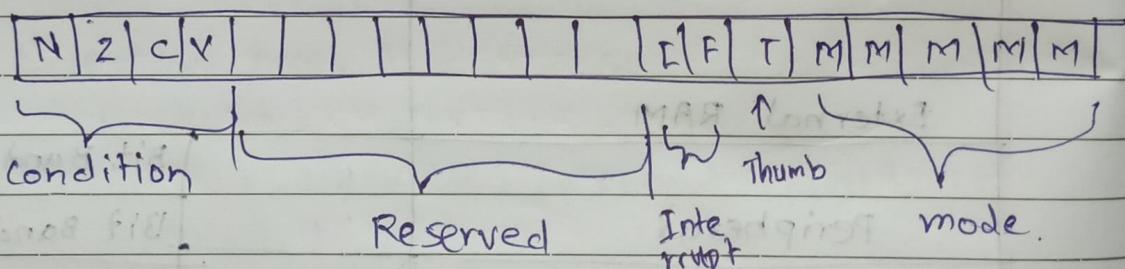
less memory than ARM.

Thumb

Totally 18 registers

Totally 12 registers.

26. Explain about the bits in CPSR Registers.



Condition Bits:

N : Negative Result from ALU.

N = 0 = Positive.

N = 1 = Negative.

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$Z$  : zero result from ALU

$Z = 1$  Result is zero.

$C$  : ALU operation carried out.

$C = 1 \rightarrow$  Addition product a carry.

$C = 0 \rightarrow$  Subtraction produced, Borrow.

$V$  : ALU operation overflow.

$V = 1 \rightarrow$  signed overflow occurred.

$I$  = Disable IRQ interrupt when it is set.

$F$  = Disable FIQ interrupt when it is set

$T$  = Thumb mode.

$M$  = 5 bits that control what mode the CPU is in.

Q. 27. What is an interrupt? Write a cprogram to handle external interrupt for an ARM chip.

\* Interrupt :

An interrupt as the name suggest interrupt the CPU from whatever it is doing and draws the attention to perform a special task.

\* An interrupt is the automatic transfer of software execution in response to the hardware event that is asynchronous with the current software execution.

\* An interrupt is a computer or Arch signal that tells the computer to stop running the current program to the new one can be started or by circuit that corners such signal.

Header file

```
#ifndef EXTI_H_
#define EXTI_H_

#include "stm32f4xx.h"
#include "RCC_AHBLIFNR.h"
#define SWITCH_EXTI_O 0
#define SWITCH_EXTI IRQnEXTIO_IRQn
#define SWITCH_CLOCK_EN RCC_AHB1ENR_GPIOAEN
#define SWITCH_GPIO GPIOA
#define SWITCH_PIN 0.
```

```
#define SWITCH_EXTICR SYSEFFQ[4] → EXTIICR[0]
#define SWITCH_EXTIIR_MSK (BV(3) | BV(2) | BV(1) | BV(0))
```

```
void switchExtiInit(void);
```

```
#endif .
```

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Source file :

```
# include "Exti.h"
# include "led.h"
Void switch_ExtiInit(Void)
{
```

```
RCC ->AHB1ENR |= BV(switch_CKEN);
SWITCH-GPIO -> MODE &= ~BV(switchpin+2)+
| BV(switchpin+2);
```

```
switch-GPIO ->PUPDR &= ~
(BV(switchpin+2)-1)
```

```
SWITCH-GPIO ->PUPDR &= ~BV(switchpin+2*1)|
BV(switchpin+2));
```

RCC -> APB2 = BV(RCC ->APB2ENR ->SYSCFG EN-POS)

SD card no board in R, A2T found

switch -> exti pin did not work

```
EXTI -> FISR |= BV(SWITCH-EXTI);
```

```
EXTI -> RTISR &= ~BV(SWITCH-EXTI);
```

```
EXTI -> IMR, |= BW(SWITCH-EXTI);
```

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NVIC\_Enable\_IRQ(SWITCH\_EXTI\_IRQn);

}

Void EXTI0\_IRQHandler(void)

EXIT → PR1 = BV(SWITCH\_EXTI);

28. Explain Cortex M3 architecture.

Cortex M3 Architecture

- Cortex M3 use a 32 bit architecture.
- The ISA in the Cortex M processor is called the Thumb ISA & is based on Thumb2 Technology which supports a mixture of 16 bit & 32 bit architectures.
- 3 stage pipeline.
- Harvard bus architecture.
- 32 bit addressing, supporting 4GB of memory space.

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- on chip bus interface based on ARM AMBA
- AHB Lite BUS interface
- Fixed Memory MAP.
- 1 - 240 interrupts.
  
- configurable priority levels.
- Non maskable interrupt.
- Debug & sleep control.
  
- \* serial wire or JTAG debug.
- \* optional EIM.