جامعة القاهرة الجديدة التكنولوجية NEW CAIRO TECHNOLOGICAL UNIVERSITY

Sub.	Re-Sub

Assignment Brief Submission&Resub

LOs	LO3	
Grade " Sub"	LO3	
Grade"Resub"	P	Not Achieved " repeat unit"

Student Name:		ID Number	
Unit Number and Title:	ICT 215	Digital Engineering	
Qualification	Higher National Diploma in Information and Communications Technology (ICT) (Y2).		
Academic Year:	2023/2024	Assessor Name:	Dr. Hatem Yousry
Assignment Title:	Class Work - Combinational and Sequential logic	Internal Verifier Name:	Dr. Rasha Stohy
Assignment No.	2	Issue Date:	19 /12 /2023
Submission Format: Type of Evidence	Document	Submission Date:	26 /12 /2023

STUDENT DECLARATION

Plagiarism

Plagiarism is a particular form of cheating. Plagiarism must be avoided at all costs and students who break the rules, however innocently, may be penalised. It is your responsibility to ensure that you understand correct referencing practices. As a university level student, you are expected to use appropriate references throughout and keep carefully detailed notes of all your sources of materials for material you have used in your work, including any material downloaded from the Internet. Please consult the relevant unit lecturer or your course tutor if you need any further advice.

Student Declaration

Student declaration

I certify that the assignment submission is entirely my own work and I fully understand the consequences of plagiarism. I understand that making a false declaration is a form of malpractice.

Also, I acknowledge that I have received the feedback about my work from the assessor.

Student signature: Date: / /2023

FORMATIVE FEEDBACK	
Assessor's Formative Feedback:	**Confirm action completed:**
Assessor Signature:	**Date:**

IV assessment brief approval

IV's signature: Rasha Date: /12/2023

Learning Outcomes and Assessment Criteria:			
Learning Outcome	**Pass**	**Merit**	**Distinction**
LO3 Understand the basic logic components of combinational and sequential logic systems.	**P7** Identify the main components of the given combinational logic system, such as adders, decoders, encoders, multiplexers, etc. **P8** Explore the main components of sequential logic system such as Latches and Flip Flops. **P9** Explain the operation of the given combinational or sequential logic system, make a good use of Truth Tables and Karnaugh Map (K-Map). **P10** Use appropriate software simulator to simulate and test the operation of a combinational or sequential logic system.	**M3** Analyze the logic operation for a combinational or sequential logic system in the given real life application scenario.	**D3** Design a hardware implementation schematic diagram for a combinational or sequential logic system in the given real life application scenario.

Scenario

You are a Digital logic designer, who is responsible for designing digital hardware products. Your job duties include creating the digital hardware design with User Interface (UI), working with marketing to determine the type of digital products needed, and troubleshooting errors in existing products. A binary multiplier is an arithmetic circuit used in digital electronics, such as a Calculators, Computers, etc., to multiply two binary numbers. A binary or an array Multiplier is a digital combinational circuit used for multiplying two binary numbers by employing an array of full adders and half adders. For implementation of array multiplier with a combinational circuit, consider the multiplication of two 2-bit numbers as shown in figure 1. The multiplicand bits are b1 and b0, the multiplier bits are a1 and a0, and the product is c3c2c1c0. The multiplication of two bits such as A0 and B0 produces a 1 if both bits are 1; otherwise, it produces a 0, this is identical to an AND operation. The two partial products are added with two half-adder (HA) circuits (if there are more than two bits, we must use full adder (FA)).

For a Binary logic calculator consists of Decimal to Binary encoder input and 4-bit Adder, logic gates and Binary to Decimal decoder output as shown in Figure 1.

For the **two 2-bits binary inputs** A and B. The value of A and B can vary from 00 to 11 in binary using two bits' logic switch as an input to the system. The binary multiplication output from that combinational logic system is stored in a memory to be displayed on **two Seven segment displays to represent the units and tens as decimal number**. As in Binary Coded Decimal (BCD) encoding scheme each of the decimal numbers (0-9) is represented by its equivalent binary pattern (which is generally of 4-bits output).

Whereas, **Seven segment display** is an electronic device which consists of seven Light Emitting Diodes (LEDs) arranged in some definite pattern (common cathode or common anode

type), which is used to display **Decimal numbers, as input is BCD i.e., 0-9).**

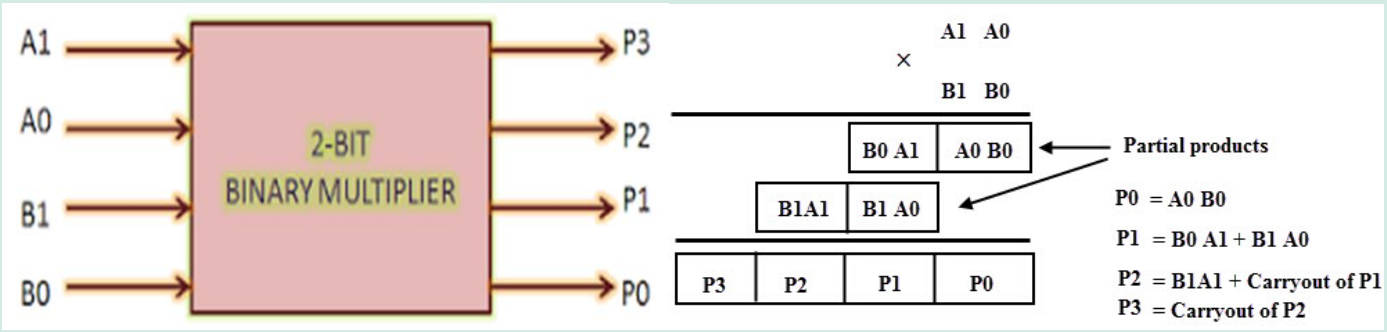

Figure 1. 2-Bits Multiplication

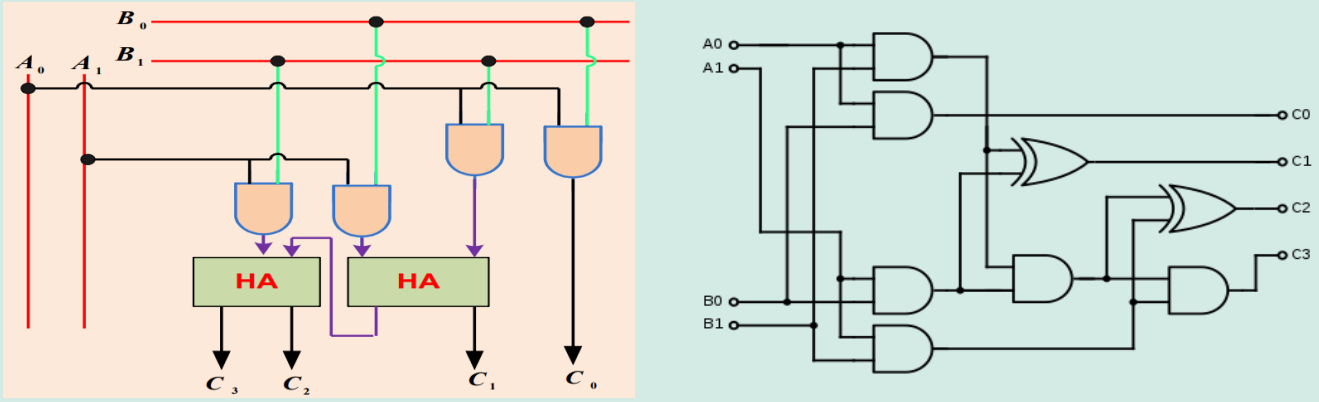

Figure 2. 2-Bits Multiplier (a) Structural Design (b) Behaviour Design

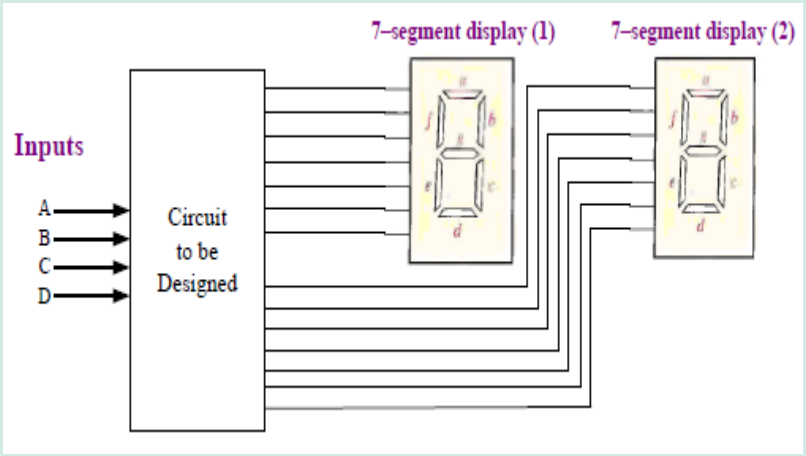

Figure 3. The End-User Product Design

Do the following Tasks:

Task 1:

1. **Identify the main components** of the given combinational logic system and extract the relations between each block.
2. **Define the different types of logic components** in the given combinational logic system.
3. **Explain the operation** of the given combinational logic system as shown in Figure 1 , make a good use of Truth Tables and Karnaugh Map (K-Map).

4. **Explain and Sketch** the logic gates diagram of the **2-bits binary multiplier for Structural Design. and compare it with the Behaviour Design.**
5. **Analyze the main differences between Structural Design and Behaviour Design for 2-bits binary multiplier as shown in Figure 2**.
6. **Design a hardware implementation schematic** and define the **number of IC chips** requirements for a **Binary 2-bits binary multiplier with Binary to Decimal Converter** to Drive Two Seven-Segment Indicators. The Four Inputs to the Converter Circuit (A, B, C, D) as in the **Figure 3**. Then, examine the suitable number of the **Seven segment displays**.

Task 2:

1. **From your exploration of the sequential logic systems,** Explain the logic operation of **two Master-Slave D Flip-Flop** which is a sequential logic system with two stable states that can be used to store binary data. **Analyze** the system for **logic gates, truth table, and Timing Diagram.**

Task 3: (In Lab Task)

1. Use **Multisim simulator** to simulate the given **combinational logic system** and to test its operation.
2. Use **Multisim simulator** to simulate the **Master-Slave D Flip-Flop** and show its **clock** and **Timing Diagram**.

- **Printout the Logic and its output.**

Sources of information

- Class handouts and learning materials.
- Individual research.
- Lab ……..
- https://learnabout-electronics.org/Digital/dig44.php

Higher Nationals - Summative Assignment Feedback Form

Student Name		Student ID	
Unit Title	**ICT215- Digital Engineering**		
Assignment Number(x of y)	**2**	Assignment Title	Classwork

Assessor Summative Feedback: Feedback should be against the learning outcomes and assessment criteria to help students understand how these inform the process of judging the overall grade. *should be constructive and useful including:

- Feedback should give full guidance to the students on how they have met the learning outcomes and assessment criteria

a) Strengths of performance

b) Limitations of performance

c) Any improvements needed in future assessments

Assessor Signature:	Date: / /2023

Re-submission Date	/ /2023	Actual Date Received Re-submission	/ /2023

Resubmission Feedback:

*Please note resubmission feedback is focussed only on the resubmitted work

Assessor Signature:	Date: / /2023
Internal Verifier's Comments:	
Signature:	Date: / /2023

* Please note that grade decisions are provisional. They are only confirmed once internal and external moderation has taken place and grades decisions have been agreed at the assessment board.

Observation Sheet

Student Name:			
Unit Number and Title:	ICT215	**Digital Engineering**	
Qualification	Higher National Diploma in ICT		
Assignment No.	2	Assignment Title:	**Class Work - Combinational and Sequential logic**

Description of the activity undertaken

- **Use Multisim simulator to simulate the given combinational logic system and to test its operation.**
- **Use Multisim simulator to simulate the Master-Slave D Flip-Flop and show its clock and Timing Diagram.**
- **Use the combinational logic system as described in Assignment (2).**

Observation Checklist

The Observer will observe the student perform the following operation independently.

Use Multisim simulator to do the following:

Criteria Ref.	Task No.	Task Description	Tick if met
P10 M3 P3	**3**	Navigate in Multisim Program and its Libraries for combinational and sequential logic simulation.	☐
		Identify the suitable logic gates and Logic Blocks for the given combinational logic system	☐
		Select the appropriate inputs, and outputs according to the combinational logic system.	☐
		Construct the combinational logic system as shown in Figure 1, and 2 - assignment (2) and show the output for each input operation.	☐
		Identify the suitable Logic Blocks for the Master-Slave D Flip-Flop.	☐
		Select the appropriate inputs, clock and outputs according to Master-Slave D Flip-Flop.	☐
		Construct the Master-Slave D Flip-Flop.and show the output Timing Diagram.	☐

Observer Signature		Date	