جامعة القاهرة الجديدة التكنولوجية NEW CAIRO TECHNOLOGICAL UNIVERSITY

Sub.	Re-Sub

Assignment Brief Submission&Resub

LOs	LO1 and LO2			
Grade " Sub"	LO1		LO2	
Grade"Resub"	LO1 P	Not Achieved " repeat unit"	LO2 P	Not Achieved " repeat unit"

Student Name:		ID Number	
Unit Number and Title:	ICT 215	Digital Engineering	
Qualification	Higher National Diploma in ICT program		
Academic Year:	2023/2024	Assessor Name:	Dr. Hatem Yousry
Assignment Title:	Mid-Term LO1 and LO2	Internal Verifier Name:	Dr. Rasha
Assignment No.	1	Issue Date:	9 /11 /2023
Submission Format: Type of Evidence	Document	Submission Date:	23 /11 /2023

STUDENT DECLARATION

Plagiarism

Plagiarism is a particular form of cheating. Plagiarism must be avoided at all costs and students who break the rules, however innocently, may be penalised. It is your responsibility to ensure that you understand correct referencing practices. As a university level student, you are expected to use appropriate references throughout and keep carefully detailed notes of all your sources of materials for material you have used in your work, including any material downloaded from the Internet. Please consult the relevant unit lecturer or your course tutor if you need any further advice.

Student Declaration

Student declaration

I certify that the assignment submission is entirely my own work and I fully understand the consequences of plagiarism. I understand that making a false declaration is a form of malpractice.

Also, I acknowledge that I have received the feedback about my work from the assessor.

Student signature: Date: / /2023

FORMATIVE FEEDBACK	
Assessor's Formative Feedback:	**Confirm action completed:**
Assessor Signature:	**Date:**

IV assessment brief approval		
IV's signature:	Rasha	Date: 7/11/2023

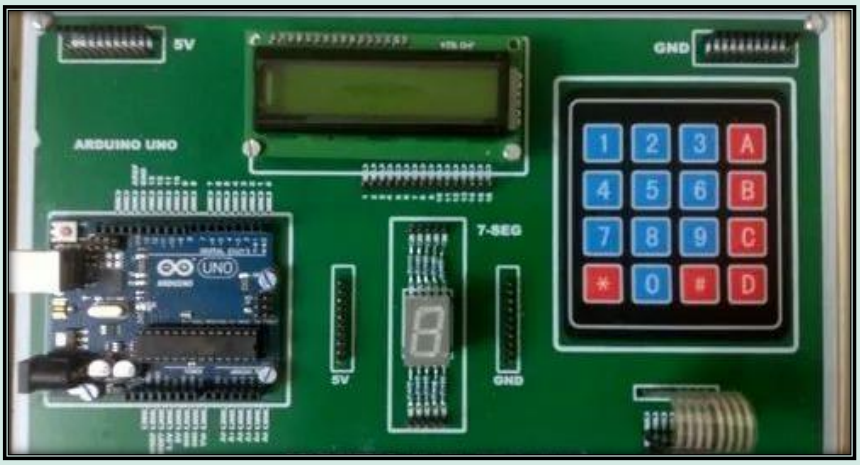
Learning Outcomes and Assessment Criteria:			
Learning Outcome	**Pass**	**Merit**	**Distinction**
LO1 Understand the operation of logic function at the gate level.	**P1** Identify the main components of a given digital logic system. **P2** Convert between numbers system showing the type of digital system conversion. **P3** Explain the operation of a logic function, in a given digital logic system.	**M1** Analyze the Boolean expression for a logic function in a real life application.	**D1** Design a hardware implementation schematic diagram in a real life application.
LO2 Express and simplify logic functions using Boolean rules and logic simplification methods.	**P4** Simplify logic function using different simplification methods. **P5** Represent logic function in terms of the POS or SOP expressions. **P6** Use appropriate software simulator to simulate a logic function and to test its operation.	**M2** Use advanced input or output methods to simulate a logic function and test its operation in each case using the software simulator.	**D2** Evaluate the simplification method according to most important or worst case simplification scenario.

Scenario

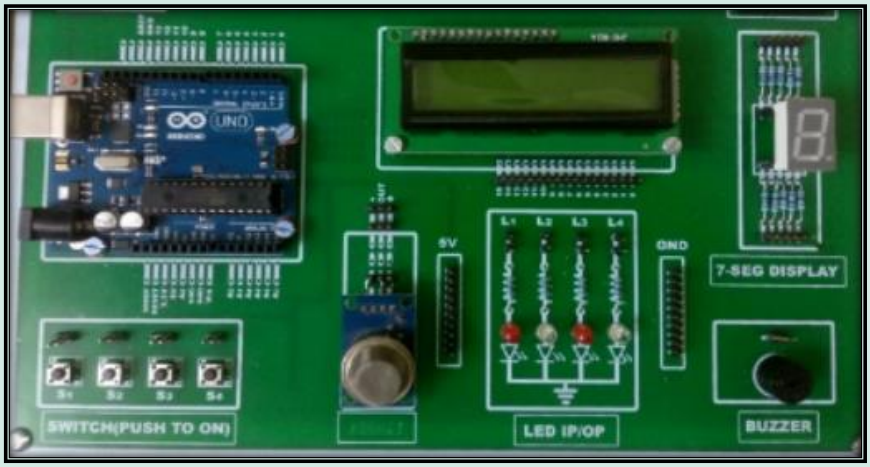
You are a digital circuits designer, who is responsible for designing digital Training Kits for education. Your job duties include creating the logic system design, working with market customers to determine the type of digital modules needed in the kits, and troubleshooting errors in existing kit or products.

For a Digital Kit Product as shown in Figure (1). One kit model consists of a 4x4 Matrix Keypad, which receives code or sequence numbers (decimal numbers) from the trainee and converts outputs to binary output number. This output (binary) is then connected to a Digital Logic Processor (DLP), DLP is a specialized Microcontroller chip, with its architecture is optimized for carrying out logic functions. For a logic function takes three binary inputs named A, B, and C as input sequence with Least Significant Bit (LSB) for input A to the Most Significant Bit (MSB) for input C to that logic function. The output generates one-bit binary output Q. The output Q is stored in a memory one by one as a binary word or one byte (The Least Significant Bit (LSB) is at first). The binary output Q is processed by an arithmetic or logic process to displayed on LCD screen as a hexadecimal code as shown in the kit model.

- The input sequence is **6325** decimal number.
- Each decimal number is processed to three logic inputs A, B, and C respectively.
- The logic function is **Q = (A'BC' + A'B'C)' .**



Model (A)



Model (B)

Figure 1 Digital Kit Product

Do the following Tasks:

Task 1:

1. Identify the main components of the given Digital Kit Products model (A) and Model (B) as shown in Figure (1), Compare and contrast between the two models, which one is described in the scenario.
2. For the given logic function, explain its operation, make a good use of Boolean algebra and Truth Tables. And, sketch the logic diagram of the given logic function.
3. Convert the decimal input to the binary format. And the output to hexadecimal format.

4. Critically analyze the input and output methods for the Boolean expression of the given logic function when it has been processed using kit model (A) and model (B) in terms of component blocks in each kit as shown in Figure (1).

Task 2:

1. Simplify the given logic function and write a step by step simplification process with Logic Rules. Then, check the simplified with the given function.
2. Identify the Minterm and Maxterm terms of the given logic function.
3. Represent the given logic function in terms of the Sum of Product (SOP) expression.
4. Use Karnaugh Map (K-Map) to simplify the given logic function. Then, check the simplified with the given function output.
5. Evaluate the simplification method according to the worst-case simplification scenario.

Task 3: (In Lab Task)

1. Use Multisim simulator to simulate the given logic function and to test its operation.
2. Use advanced input methods to simulate the given logic function and test its operation in each case using Multisim simulator.
3. Design a hardware implementation schematic and define the number of IC chips requirements for a Logic function implementation process in the given application scenario.

- Printout the Logic diagram and its output.

Sources of information

- Class handouts and learning materials.
- Individual research.
- Lab .....
- https://www.ekb.eg/

Higher Nationals - Summative Assignment Feedback Form

Student Name		Student ID	
Unit Title			
Assignment Number (1)		Assignment Title	

Assessor Summative Feedback: Feedback should be against the learning outcomes and assessment criteria to help students understand how these inform the process of judging the overall grade. *should be constructive and useful including:

- Feedback should give full guidance to the students on how they have met the learning outcomes and assessment criteria

a) Strengths of performance

b) Limitations of performance

c) Any improvements needed in future assessments

Assessor Signature:	Date: / /2023

Re-submission Date	/ /2023	Actual Date Received Re-submission	/ /2023

Resubmission Feedback:

*Please note resubmission feedback is focussed only on the resubmitted work

Assessor Signature:	Date: / /2023

Internal Verifier's Comments:

Signature:	Date: / /2023

* Please note that grade decisions are provisional. They are only confirmed once internal and external moderation has taken place and grades decisions have been agreed at the assessment board.

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Observation Sheet

Student Name and ID:			
Unit Number and Title:		**Digital Engineering**	
Qualification	Higher National Diploma in Information and Communications Technology (ICT)		
Assignment No.	1	Assignment Title:	**Midterm - LO1 and LO2**

Description of the activity undertaken

- **Use Multisim simulator to simulate the given logic function and to test its operation.**
- **Use advanced input methods to simulate the given logic function and test its operation in each case using Multisim simulator.**
- **Design a hardware implementation schematic and define the number of IC chips requirements for a Logic function implementation process in the given application scenario.**

Observation Checklist

The Observer will observe the student perform the following operation independently.

Use Multisim simulator to do the following:

Criteria Ref.	Task No.	Task Description	Tick if met
P6 M2 D1	3	Navigate in Multisim Program and its Libraries for Logic gate simulation.	☐
		Identify the suitable logic gates for the given logic function simulation.	☐
		Select the appropriate inputs and outputs according to the logic function.	☐
		Construct the complete logic and test the output for each input logic combination.	☐
		Use advanced input methods to simulate the given logic function and test its operation in each case.	☐
		Design a hardware implementation schematic and define the number of IC chips requirements for a Logic function implementation process in the given application scenario.	☐

Observer Signature		Date	

Rasha