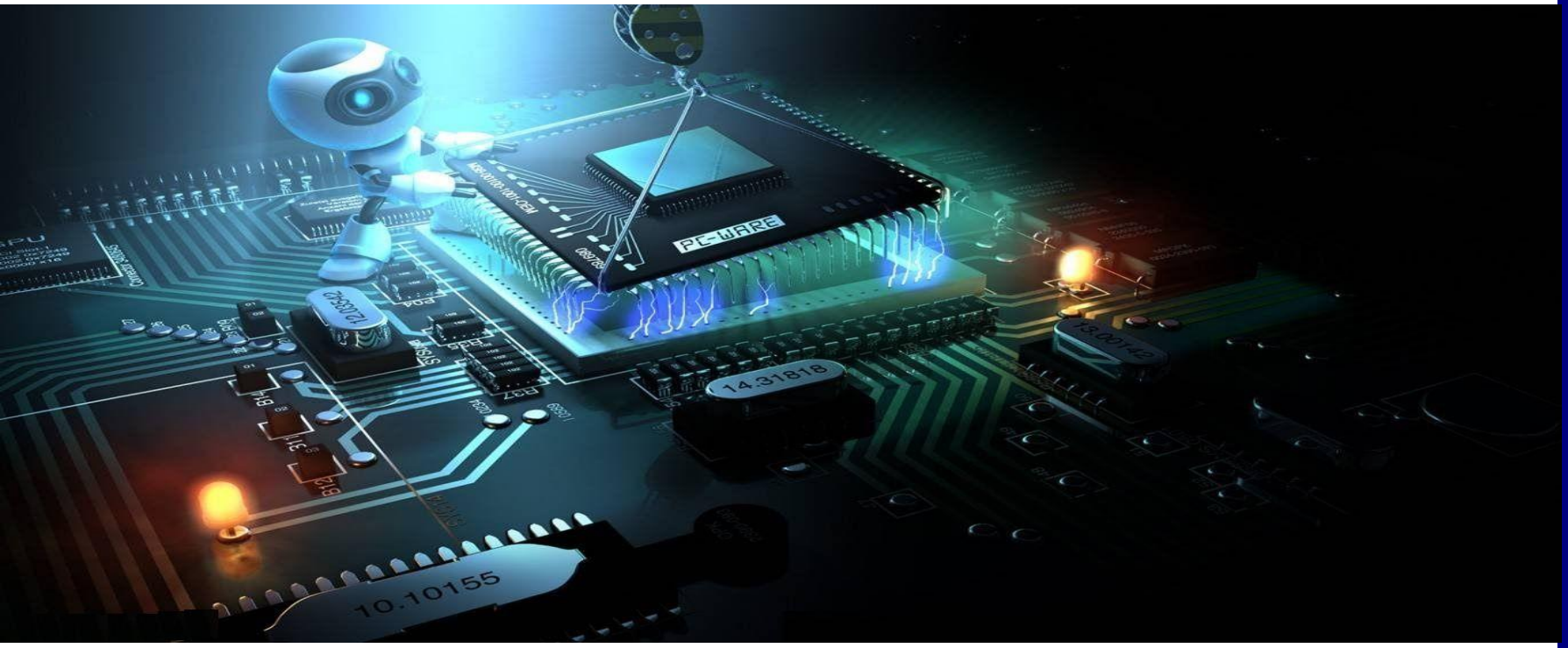
جامعة القاهرة الجديدة التكنولوجية

Fall 2023

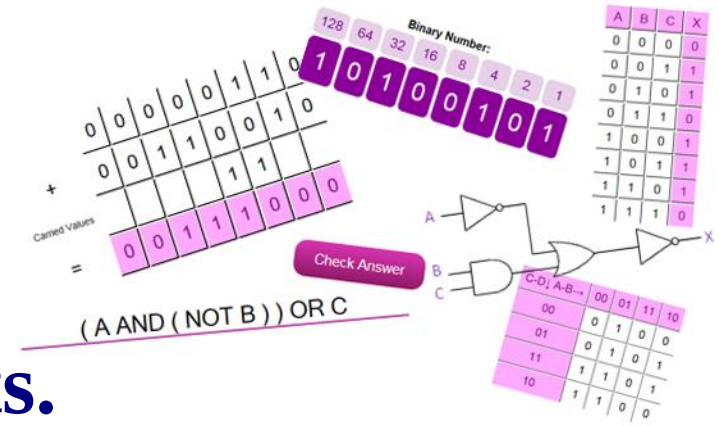
(8)



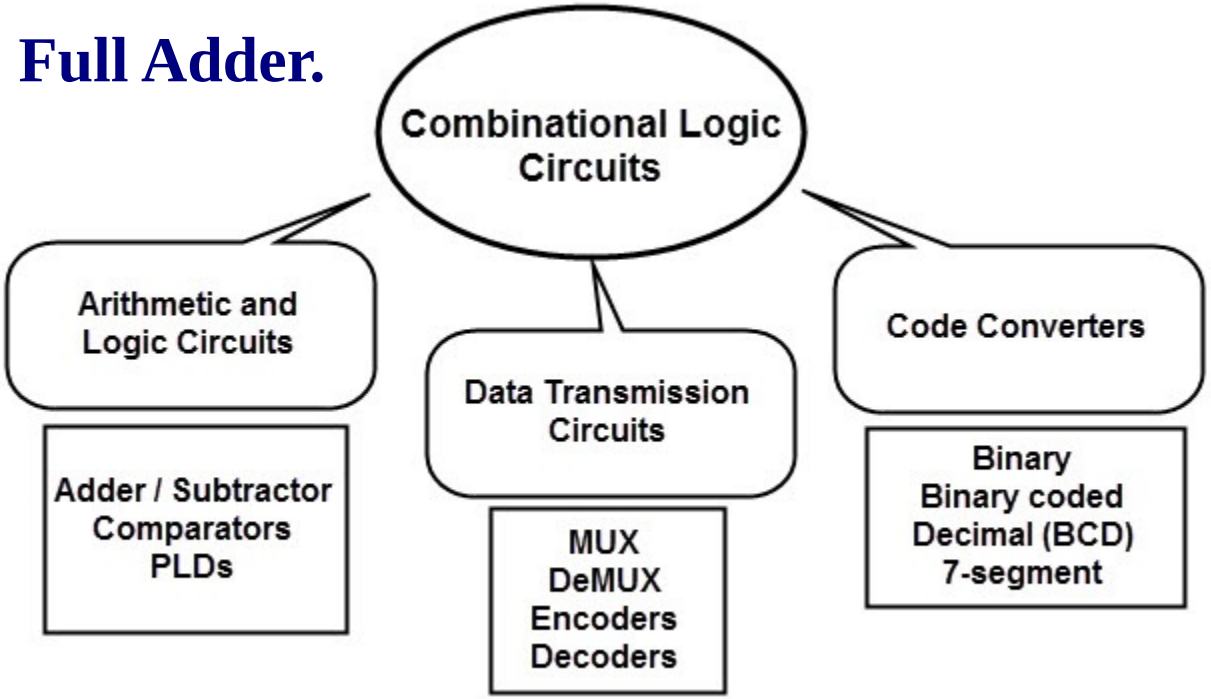
Digital Engineering

Dr. Hatem Yousry

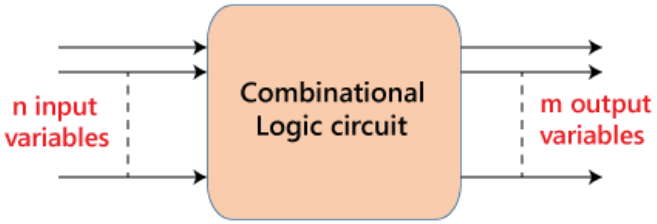
Agenda



- **Combinational Circuits.**
  - **Binary Adder.**
    - **Half Adder.**
    - **Full Adder.**

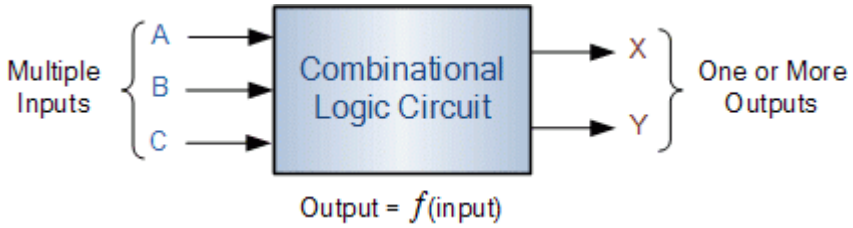


Combinational Circuits



Block diagram of a combinational circuit

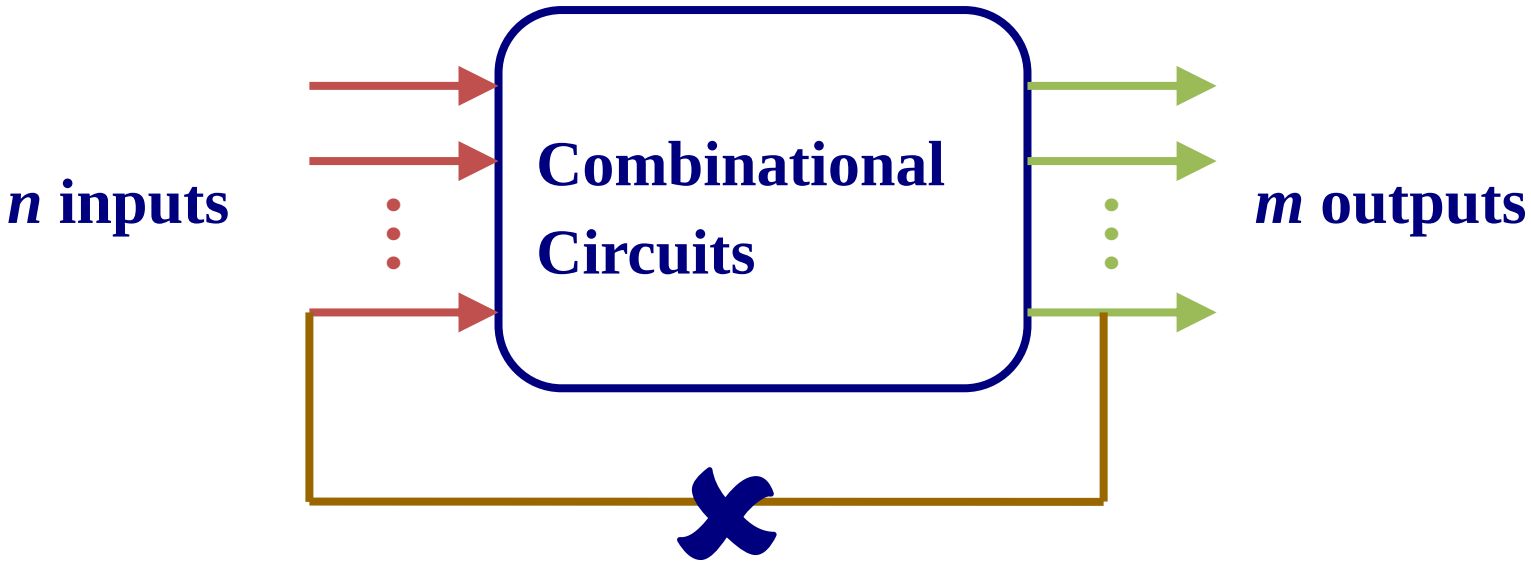
- A combinational logic circuit is a circuit **whose outputs only depend on the current state of its inputs.** In mathematical terms, the each output is a function of the inputs.
- Combinational circuit is a circuit in which we **combine the different gates in the circuit,** for example encoder, decoder, multiplexer and demultiplexer.
- Some of the characteristics of combinational circuits are following −
  - The **output** of combinational circuit at any instant of time, depends only on the levels present at input terminals.
  - The combinational circuit do **not use any memory**. The previous state of input does not have any effect on the present state of the circuit.
  - A combinational circuit can have an **n number of inputs and m number of outputs**



Combinational Circuits

- **Output is function of input only**

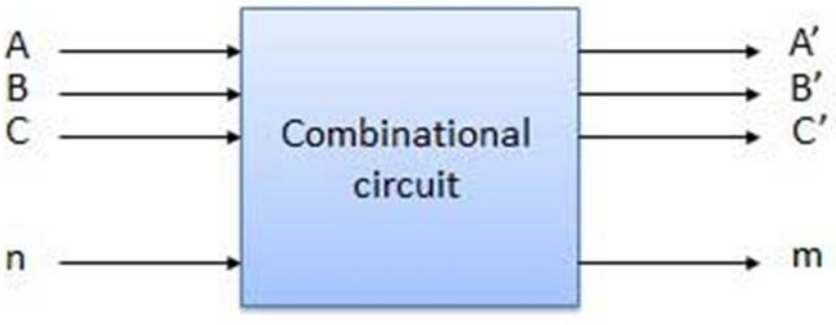
  i.e. **no feedback**

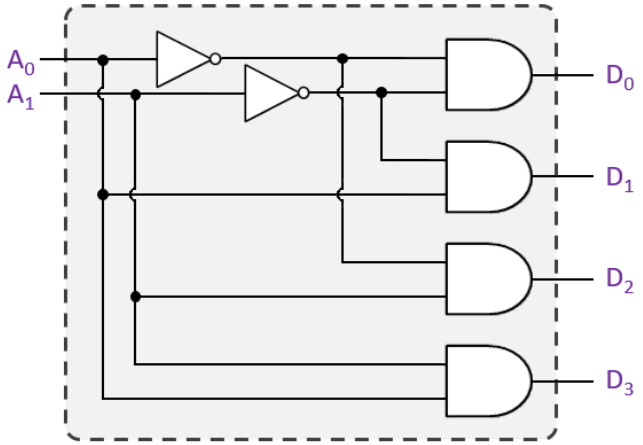


When input changes, output may change (after a delay)

Combinational Circuits

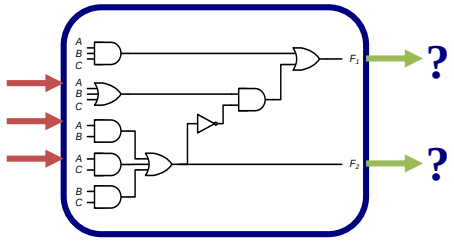
- Combinational circuits are used in a wide variety **applications** including calculators, digital measuring techniques, computers, digital processing, automatic control of machines, industrial processing, digital communications, etc.
- Combinational logic is used in computer circuits **to perform Boolean algebra on input signals and on stored data.** Practical computer circuits normally contain a mixture of combinational and sequential logic.





Combinational Circuits

- **Analysis**
  - Given a circuit, find out its *function*
  - Function may be expressed as:
    - Boolean function
    - Truth table



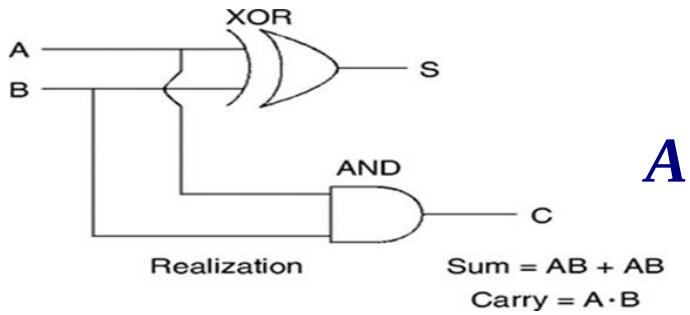
- **Design**
  - Given a desired function, determine its *circuit*
  - Function may be expressed as:
    - Boolean function
    - Truth table

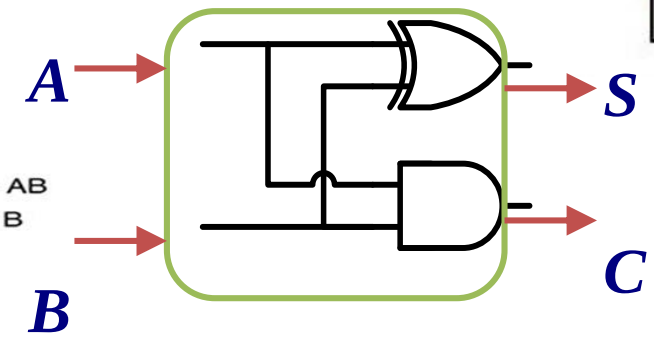
Reverse Engineering

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

- Get the Logic Operation.
- Define the inputs and outputs.
- Construct the truth table of the logic function.
- Use K-Map based on Minterm (SOP) to get the logic function.
- Design the Combinational Circuits.

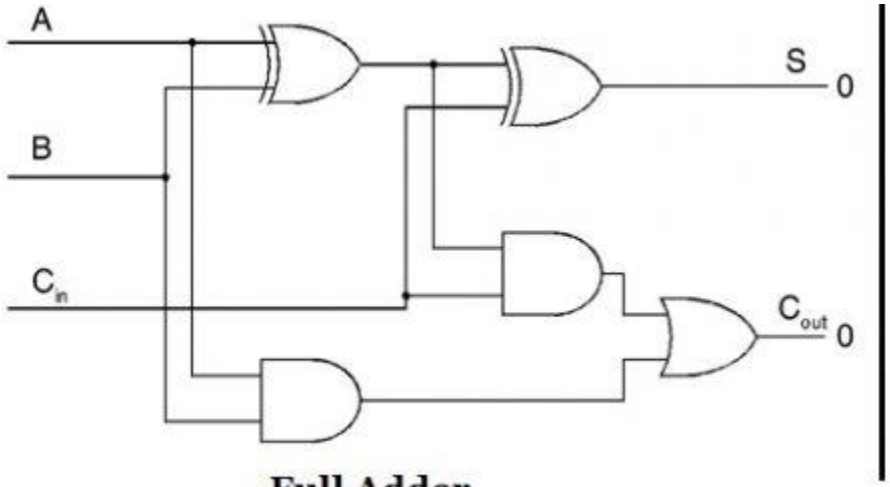
A \ B	0	1
0	0	1
1	1	0



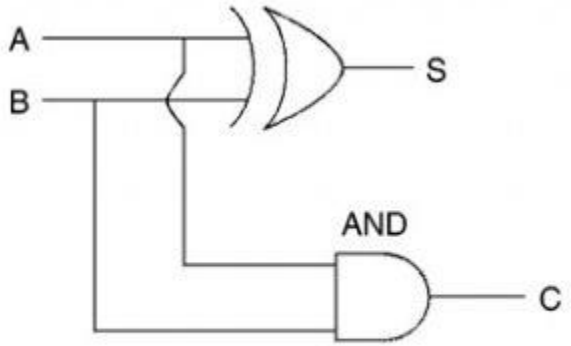


Binary Adder

- The binary adder is a combinational circuit that can perform **summation of the input binary numbers**. The most common or basic arithmetic operation is **the addition of binary digits**.
- A combination circuit which performs the additions **of two bits is a called a half adder while that performs the addition of three bits is a full adder.**

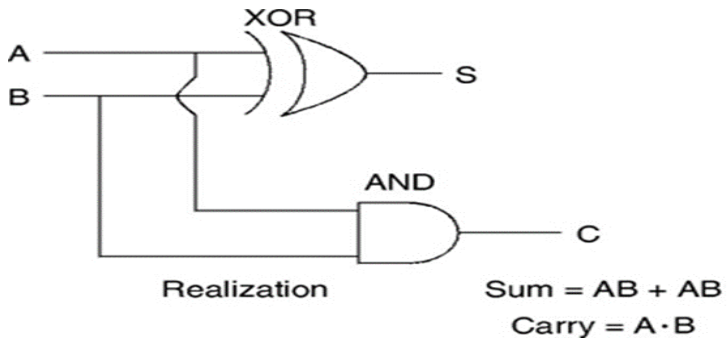


Full Adder

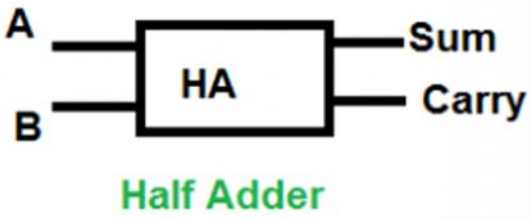


Half Adder

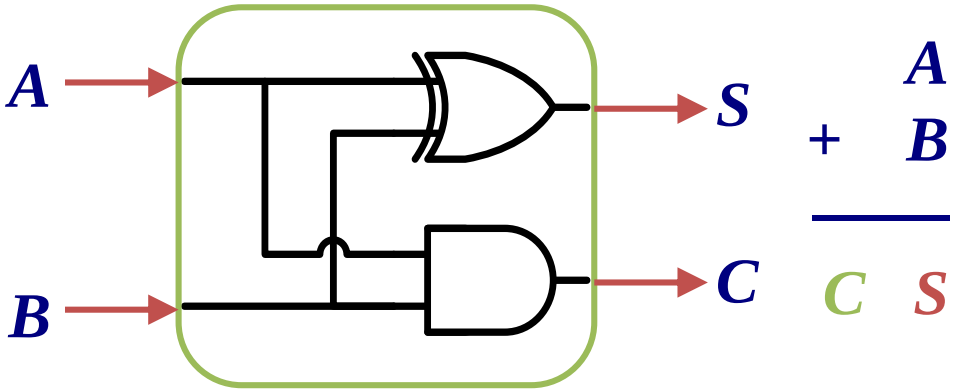
Half Adder



- The Half adder is the simplest of all adder circuits. **Half adder is a combinational arithmetic circuit that adds two numbers and produces a sum bit (S) and carry bit (C) both as the output.** Let us consider two inputs bits A and B, then sum bit (S) is the **X-OR** of A and B and the carry bit (C) will be the **AND** of A and B. It is evident from the function of a half adder that it requires one **X-OR gate and one AND gate** for its construction. Let us first consider the addition of single bits.



Adds 1-bit plus 1-bit
Produces Sum and Carry



Half Adder

- 0 + 0 = 0
- 0 + 1 = 1
- 1 + 0 = 1
- 1 + 1 = 10

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

for Sum:

A \ B	0	1
0	0	1
1	1	0

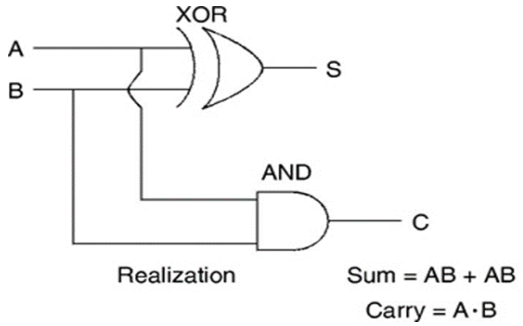
(A XOR B)

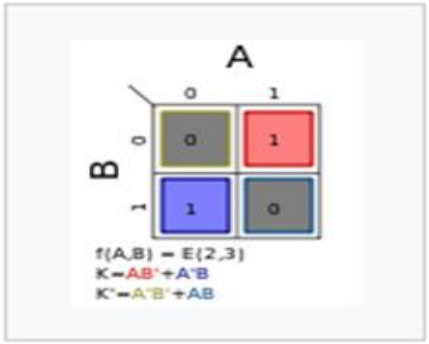
for Carry:

A \ B	0	1
0	0	0
1	0	1

(A and B)

- Here we perform two operations Sum and Carry, thus we need two **K-maps** one for each to derive the expression.
- Thus, the above equations can be written as
- 0 + 0 = 00
- 0 + 1 = 01
- 1 + 0 = 01
- 1 + 1 = 10





$\Sigma m(2,3);\ K = AB' + A'B$

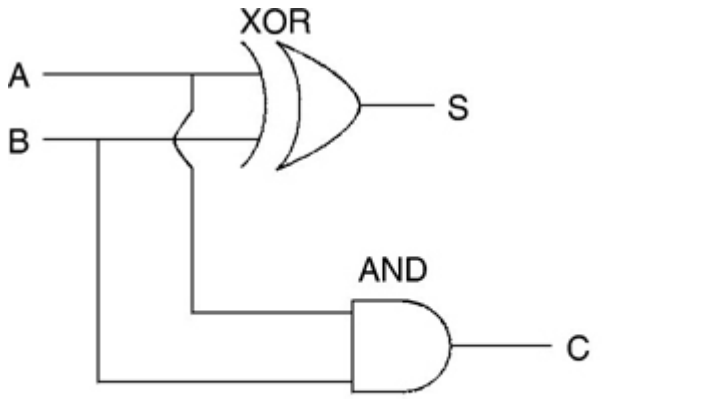
- Here the output “1” of “10” becomes the **carry-out.**

Half Adder

- The “SUM” is the normal output and “CARRY” is the carry-out. Though the half adder is the simplest adder circuit, it has a major disadvantage**. A half adder can add only two input bits (A and B) and is not affected by the carry of the input.**
- As a result, if the input that is given to a half adder has a carry, then it will be neglected and it adds only the bits A and B. But this results in **an incomplete binary addition** and hence it gets its name a half adder. The truth table of half adder is shown in the above table.

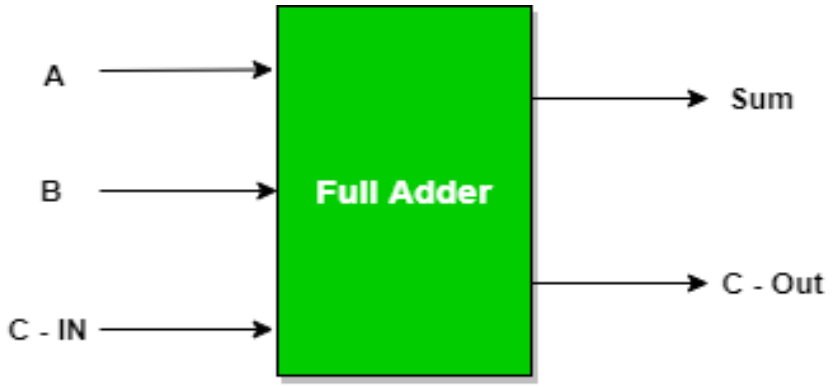
Truth Table

Input		Output	
A	B	S	C
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1

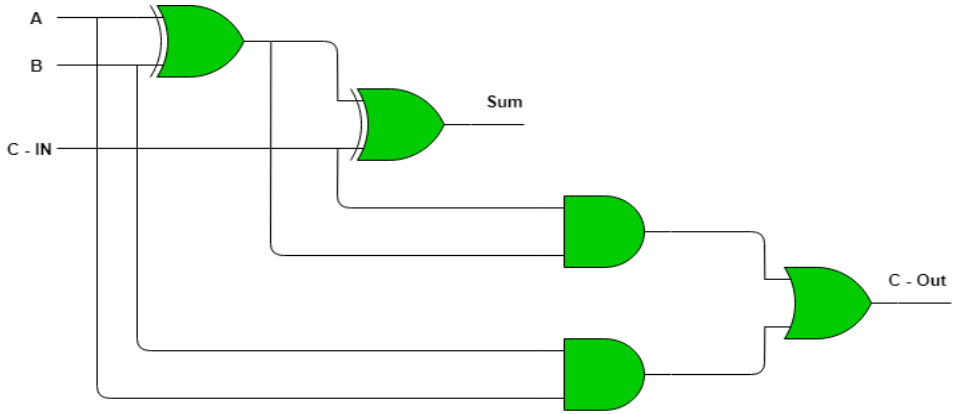


Full Adder

- Full Adder is the adder which adds **three inputs and produces two outputs.** The first two inputs are A and B and the third input is an **input carry as C-IN.**
- The **output carry** is designated as **C-OUT** and the normal output is designated as **S which is SUM.**
- A full adder logic is designed in such a manner that can take eight inputs together to create a byte-wide adder and cascade the carry bit from one adder to the another.



Full Adder



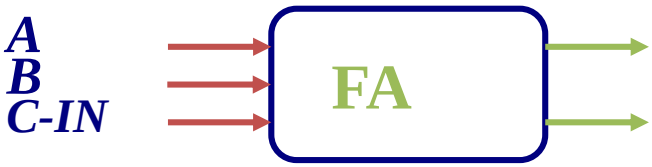
- **Logical Expression for SUM:**
- = A' B' C-IN + A' B C-IN' + A B' C-IN' + A B C-IN
- = C-IN (A' B' + A B) + C-IN' (A' B + A B')
- = C-IN XOR (A XOR B)
- **= (1,2,4,7)**

- **Logical Expression for C-OUT:**
- = A' B C-IN + A B' C-IN + A B C-IN' + A B C-IN
- = A B + B C-IN + A C-IN
- **= (3,5,6,7)**

Full Adder Truth Table:

Inputs			Outputs	
A	B	C – IN	Sum	C - Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Full Adder

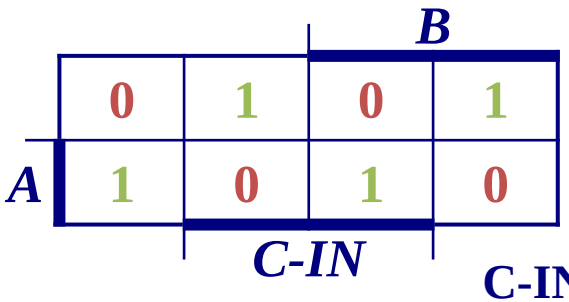


$$\begin{array}{rr} & A \\ + & B \\ + & C\text{-}IN \\ \hline C & S \end{array}$$

- **Full Adder**
  - Adds 1-bit plus 1-bit plus 1-bit
  - Produces **Sum** and **Carry**

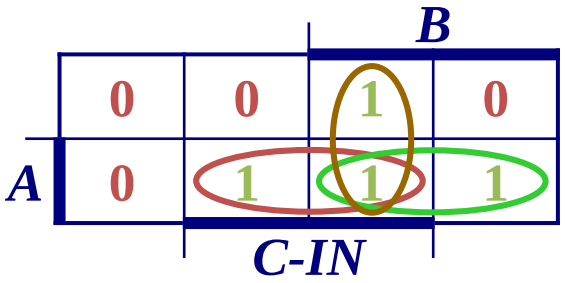
	B'	B'	B	B
A'	mo	m1	m3	m2
A	m4	m5	m7	m6
	C'	C	C	C'

A	B	C-IN	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



S= (1,2,4,7)

C-IN XOR (A XOR B)



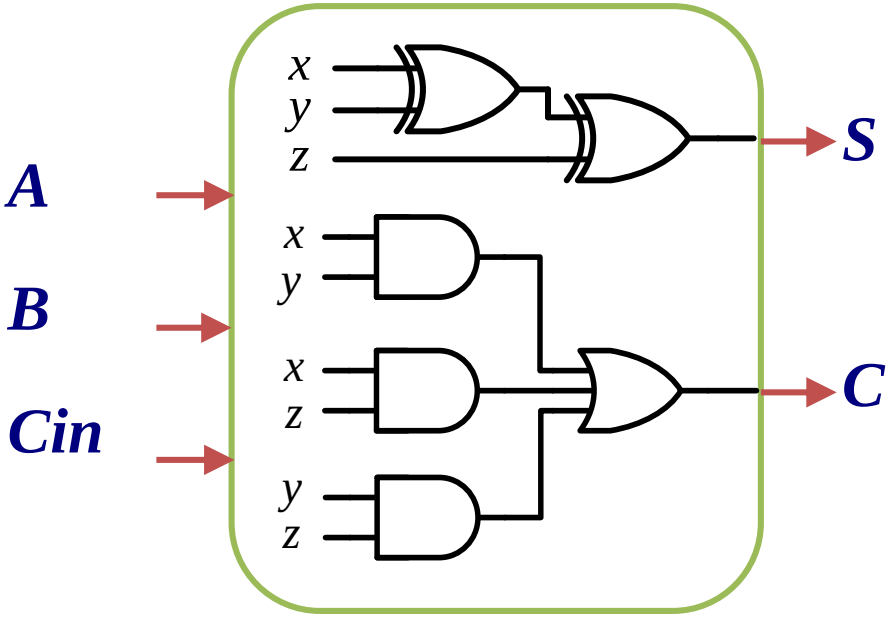
C= (3,5,6,7)

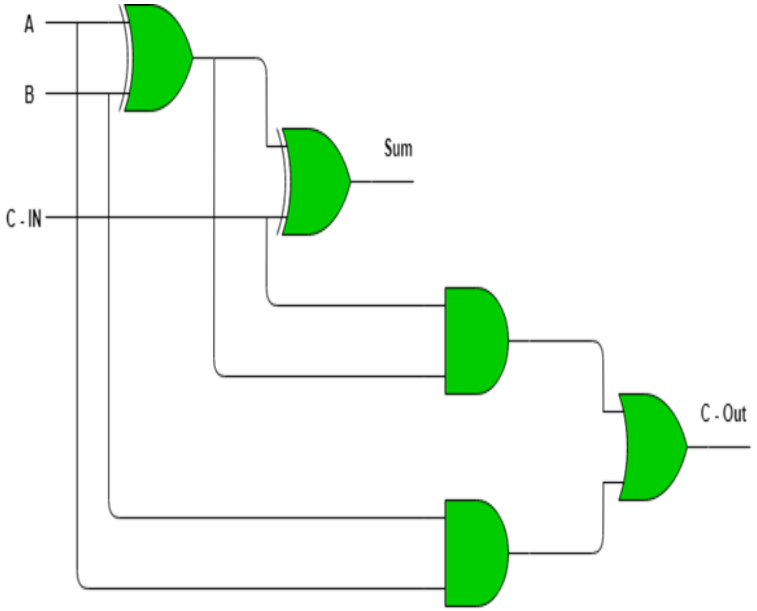
A B + B C-IN + A C-IN

Implementation of Full Adder

$S = AB'$ C-IN $'+A'B$ C-IN $'+A'B'$ C-IN $+ABC\text{-IN} = A \oplus B \oplus$ C-IN

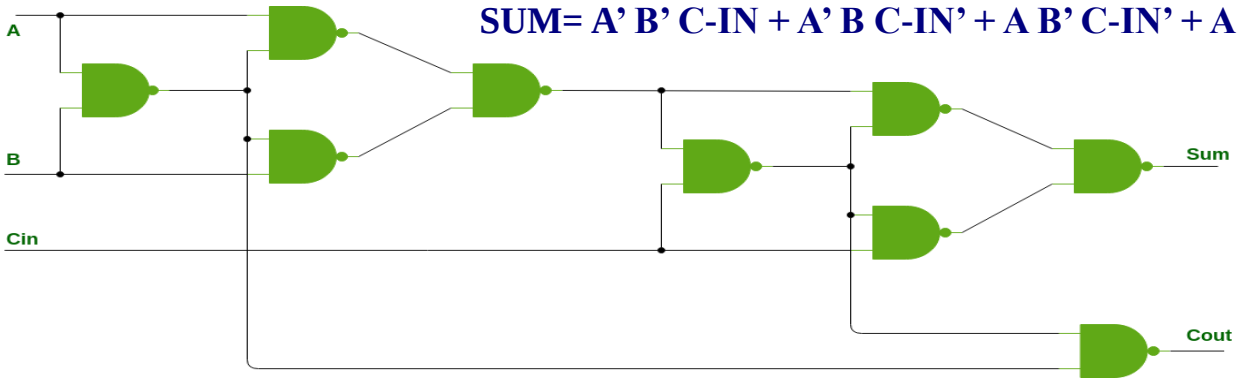
$C = AB + AC\text{-IN} + BC\text{-IN}$



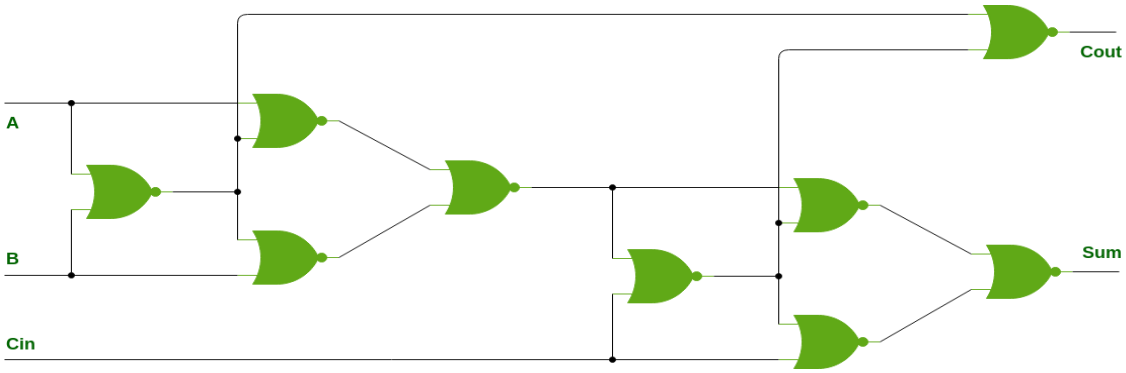


Implementation of Full Adder

- Implementation of Full Adder using **NAND** gates:



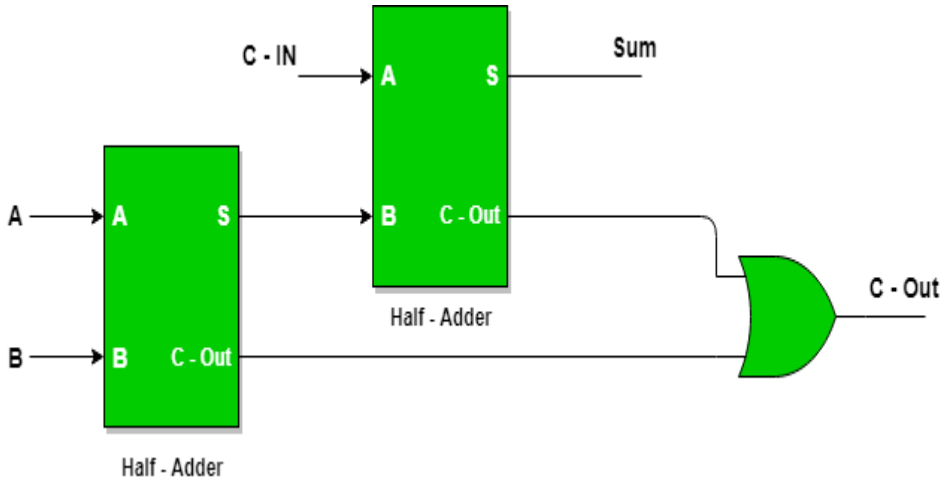
- Implementation of Full Adder using **NOR** gates:
- Total 9 NOR gates are required to implement a Full Adder.



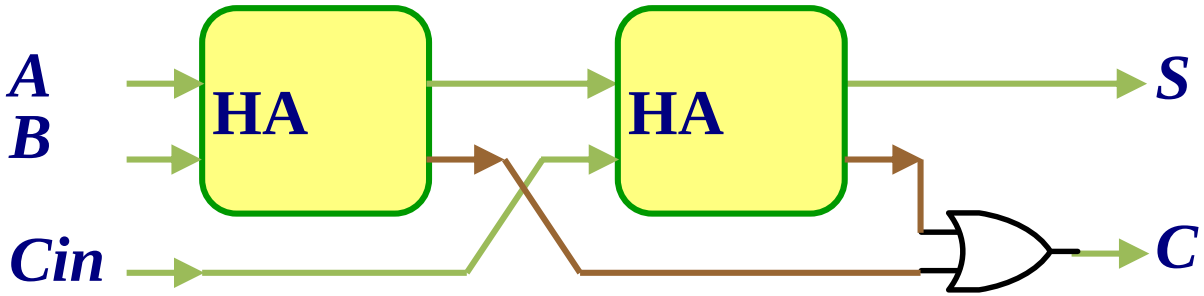
Implementation of Full Adder using Half Adders

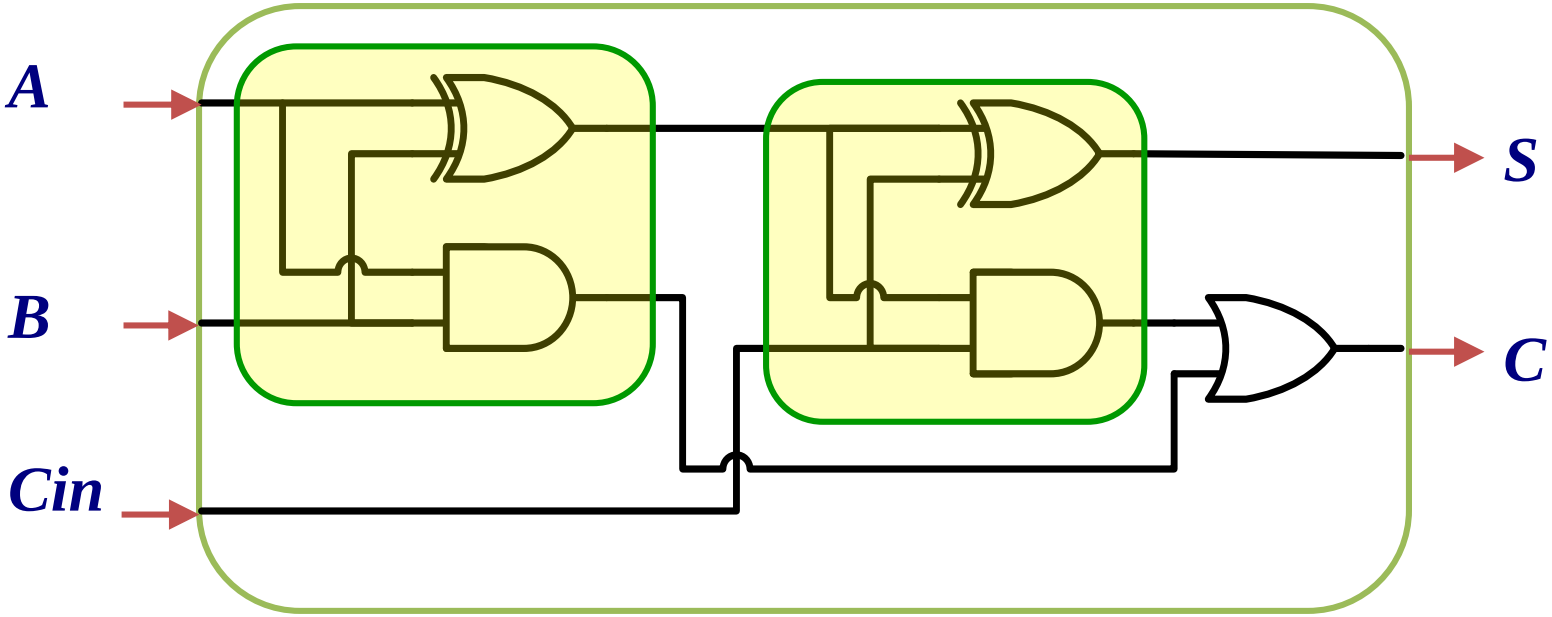
- **2 Half Adders** and a OR gate is required to implement a Full Adder.
- With this logic circuit, two bits can be added together, **taking a carry from the next lower order of magnitude, and sending a carry to the next higher order of magnitude.**

Inputs			Outputs	
A	B	C_{IN}	C_{OUT}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



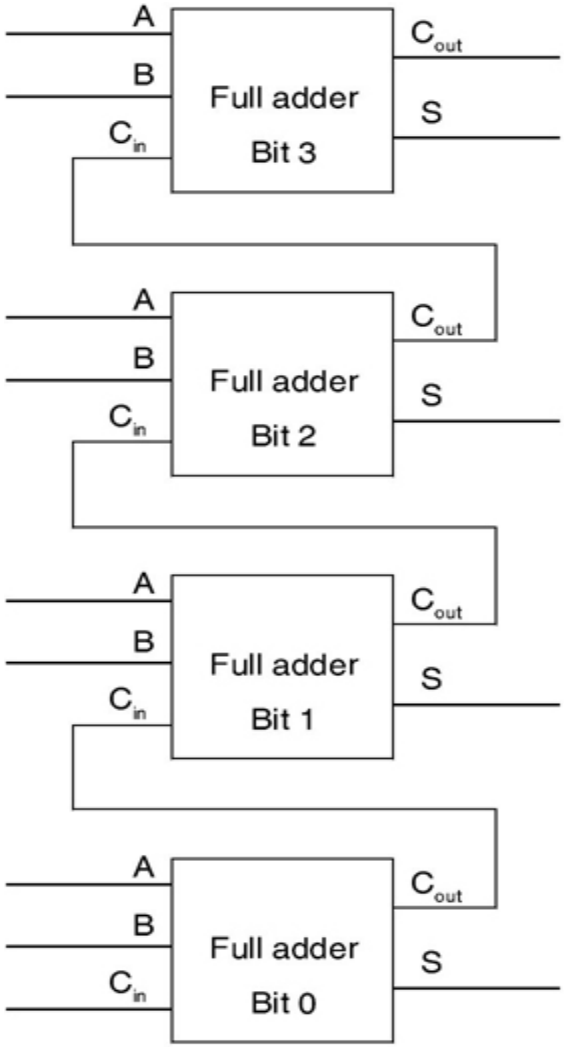
Implementation of Full Adder using Half Adders



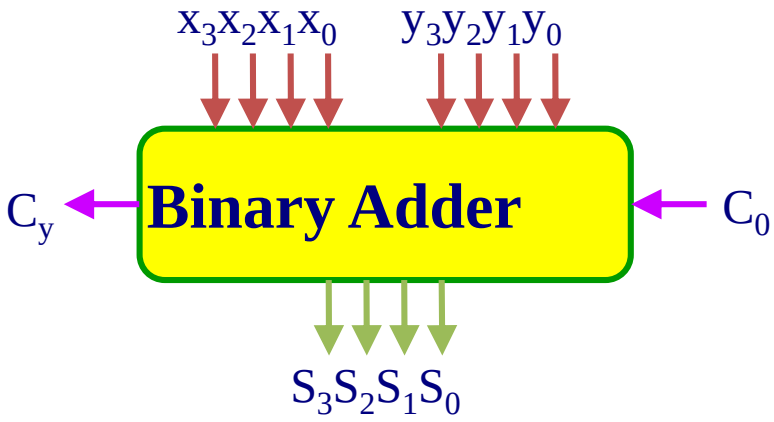


Multi-bit Adder using Full Adder

- The above-mentioned adder is used to sum up to 2 bits together taking a carry from the next lower order of magnitude and sending a carry to the next higher order of magnitude.
- For a **multi-bit operation**, each bit must be represented by a full adder and all the bits must be **added simultaneously.**
- Thus**, to add two 8-bit numbers**, we need 8 full adders which can be formed by cascading two of the 4-bit blocks.
- The addition of two 4-bit numbers is shown.

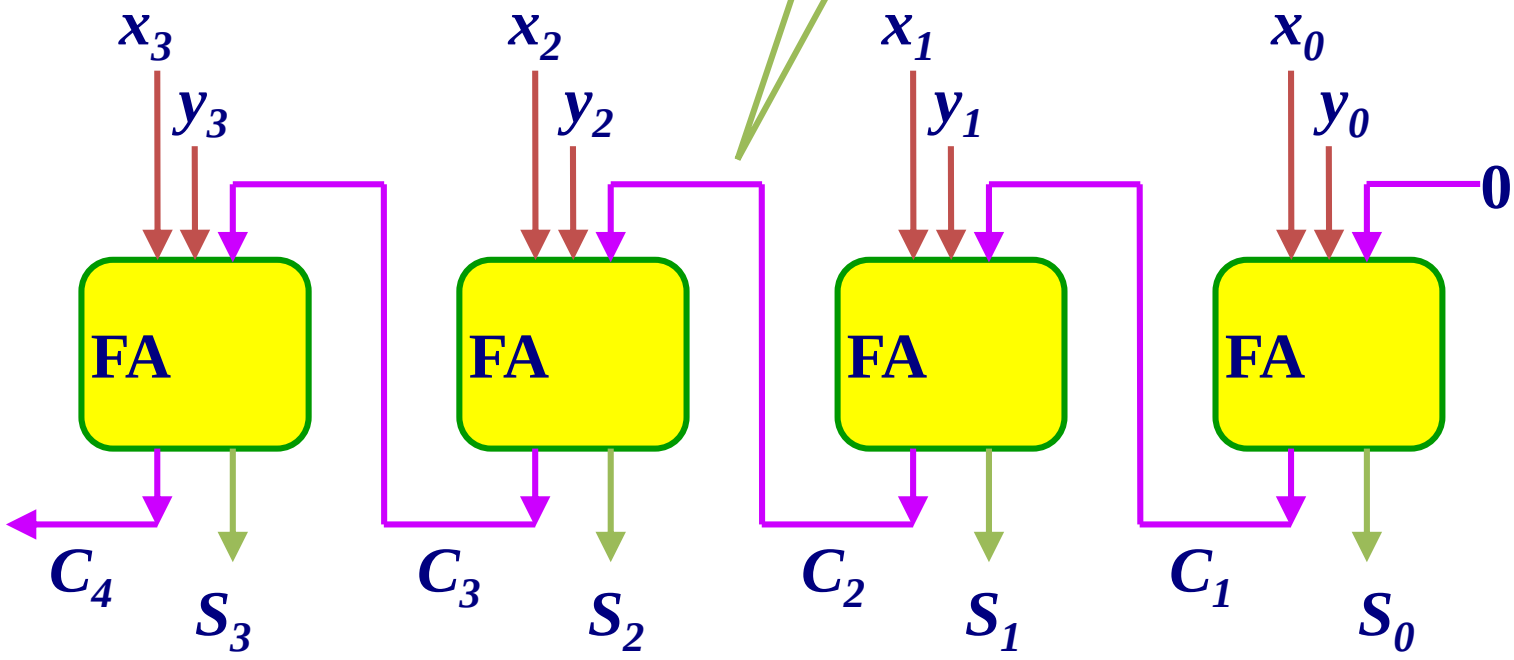


Binary Adder

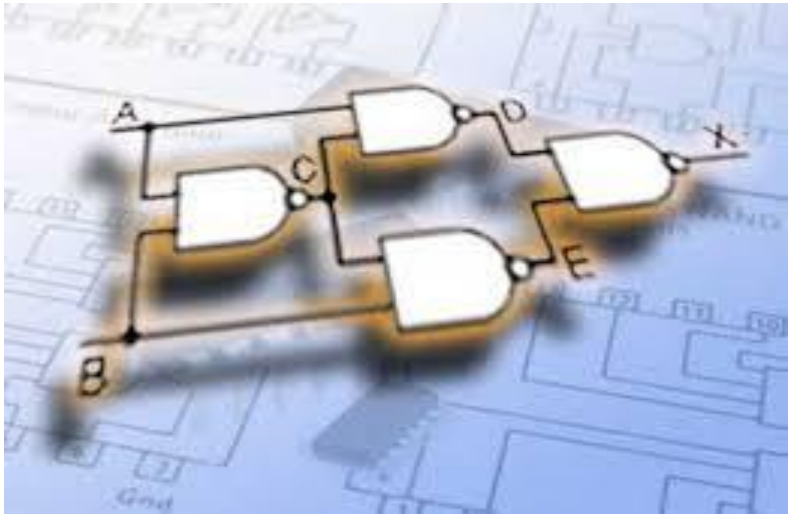


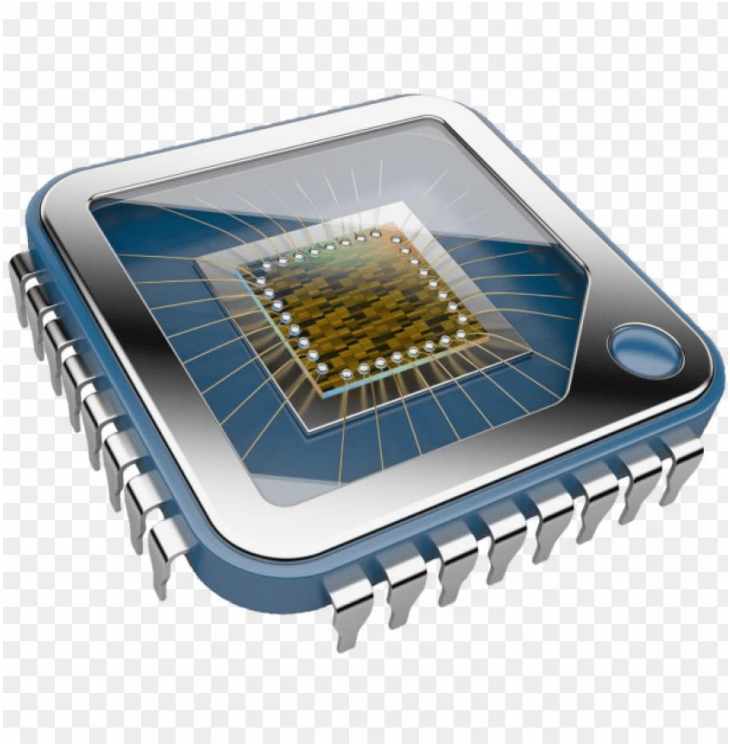
Carry Propagate Addition

$$\begin{array}{rcccc} & c_3 & c_2 & c_1 & \\ + & x_3 & x_2 & x_1 & x_0 \\ + & y_3 & y_2 & y_1 & y_0 \\ \hline Cy & S_3 & S_2 & S_1 & S_0 \end{array}$$



Thank You





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