

Discrete Mathematics 4

Applications of Logic

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Applications of Logic

1. Bitwise operations

A **bitwise operation** is a *Boolean operation* that operates on the individual bits (0s, or 1s) of the operand(s) and are summarized

Bitwise Operations

- a. The **bitwise AND**, denoted by "&", applies the *and* \wedge to the corresponding bits of each operand.
- b. The **bitwise OR**, denoted by "|", applies the *or* \vee to the corresponding bits of each operand.
- c. The **bitwise XOR**, denoted by "^", applies the disjunctive or \oplus to the corresponding bits of each operand.
- d. The **bitwise NOT**, denoted by "!", applies the negation \neg (flips 0 \longleftrightarrow 1), to the corresponding bits of each operand.

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1. Bitwise operations

We summarize the truth tables for the bitwise boolean operators.

p	q	AND &	OR	XOR \wedge	IF \Rightarrow	IFF \Leftrightarrow
1	1	1	1	0	1	1
1	0	0	1	1	0	0
0	1	0	1	1	1	0
0	0	0	0	0	1	1

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Example 24 - Bitwise Operations

Find the bitwise *AND*, *OR*, *XOR* for the following binary numbers,

$$A = 111101$$

$$B = 001111$$

Solution

Using the truth tables for Boolean operators, where the results are noted in the bottom row, we have

Bitwise AND	Bitwise OR	Bitwise XOR
111101	111101	111101
001111	001111	001111
001101	111111	110010

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Logic Circuits

Logic circuits are important in designing the arithmetic and logic units of a computer processor. Consider the problem of adding two 8-bit numbers in binary. In binary $0 + 0 = 0$, and $1 + 0 = 0 + 1 = 1$, but, as in decimal addition, in binary $1 + 1 = 2$, which in binary will be a sum of 0 and a carry of 1 to the next significant column on the left. Thinking then of adding a specific column of two binary digits, say A and B , involves as input the digits A , B and the carry in from the previous column say C_{in} . The output will be the sum S and the carry out to the next column, say C_{out} . These are the basic components of what is called a binary adder.



Figure 10. A Binary adder

The logic table for binary addition based on the digital inputs A , B , C_{in} , and digital outputs S and C_{out} is summarized in the table.

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Table 2. Truth table for Binary adder

A	B	C_{in}	S	C_{out}
1	1	1	1	1
1	1	0	0	1
1	0	1	0	1
1	0	0	1	0
0	1	1	0	1
0	1	0	1	0
0	0	1	1	0
0	0	0	0	0

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It can be shown that the logic for the outputs S , and C_{out} is given by the following propositions

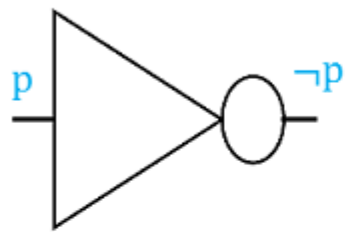
$$C_{out} = (A \wedge B) \vee (B \wedge C_{in}) \vee (A \wedge C_{in})$$

$$S = (\sim A \wedge \sim B \wedge C_{in}) \vee (\sim A \wedge B \wedge \sim C_{in}) \vee (A \wedge \sim B \wedge \sim C_{in}) \vee (A \wedge B \wedge C_{in})$$

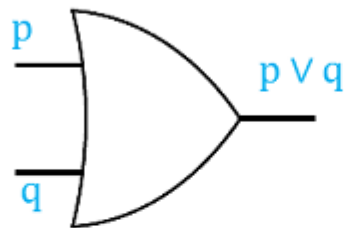
Implementing these logical outputs based on the inputs (A, B, C_{in}) , is through the use of electronic circuits called logic gates.

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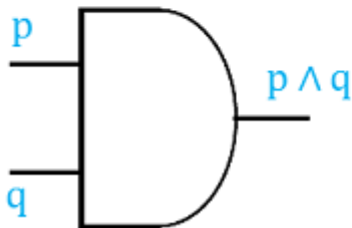
The basic logic gates, are the **Inverter** or *Not* gate, the **And** gate, the **Or** gate and the **Xor** gate. The graphical representation for each is shown below.



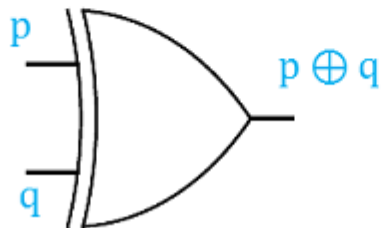
Inverter



Or gate



And gate

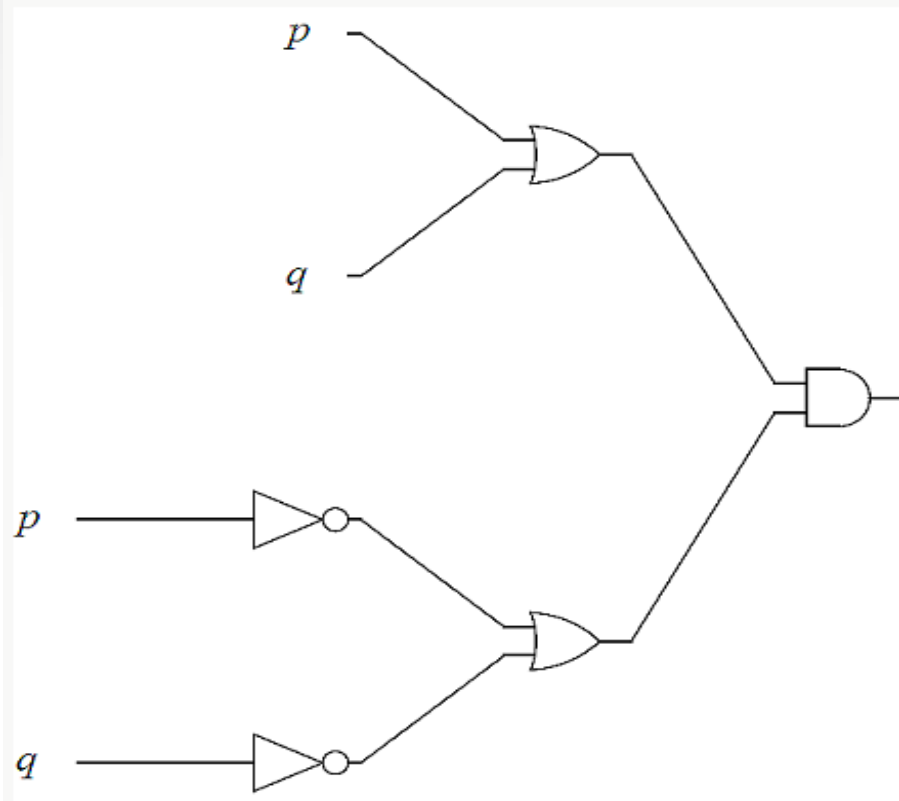


Xor gate

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Example 25 - Output of a logic circuit in terms Input

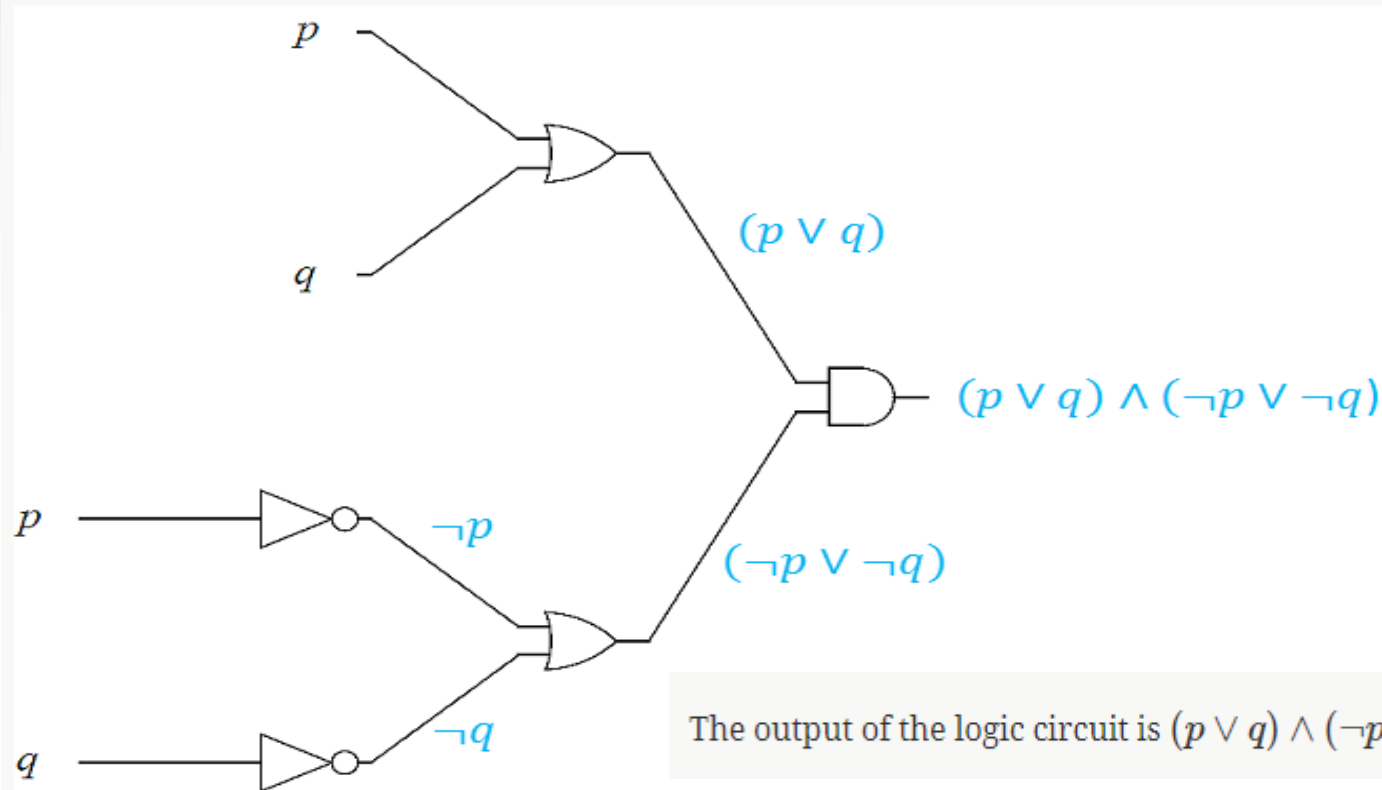
Determine the output of the following logic circuit in terms of the input variables, p , q , and r .



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Solution

Proceeding left to right, determine the output of the leftmost gates first using the basic gate outputs.



The output of the logic circuit is $(p \vee q) \wedge (\neg p \vee \neg q)$

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Example 26 - Design a Logic Circuit

Design a logic circuit for $(p \vee \neg q) \wedge \neg p$.

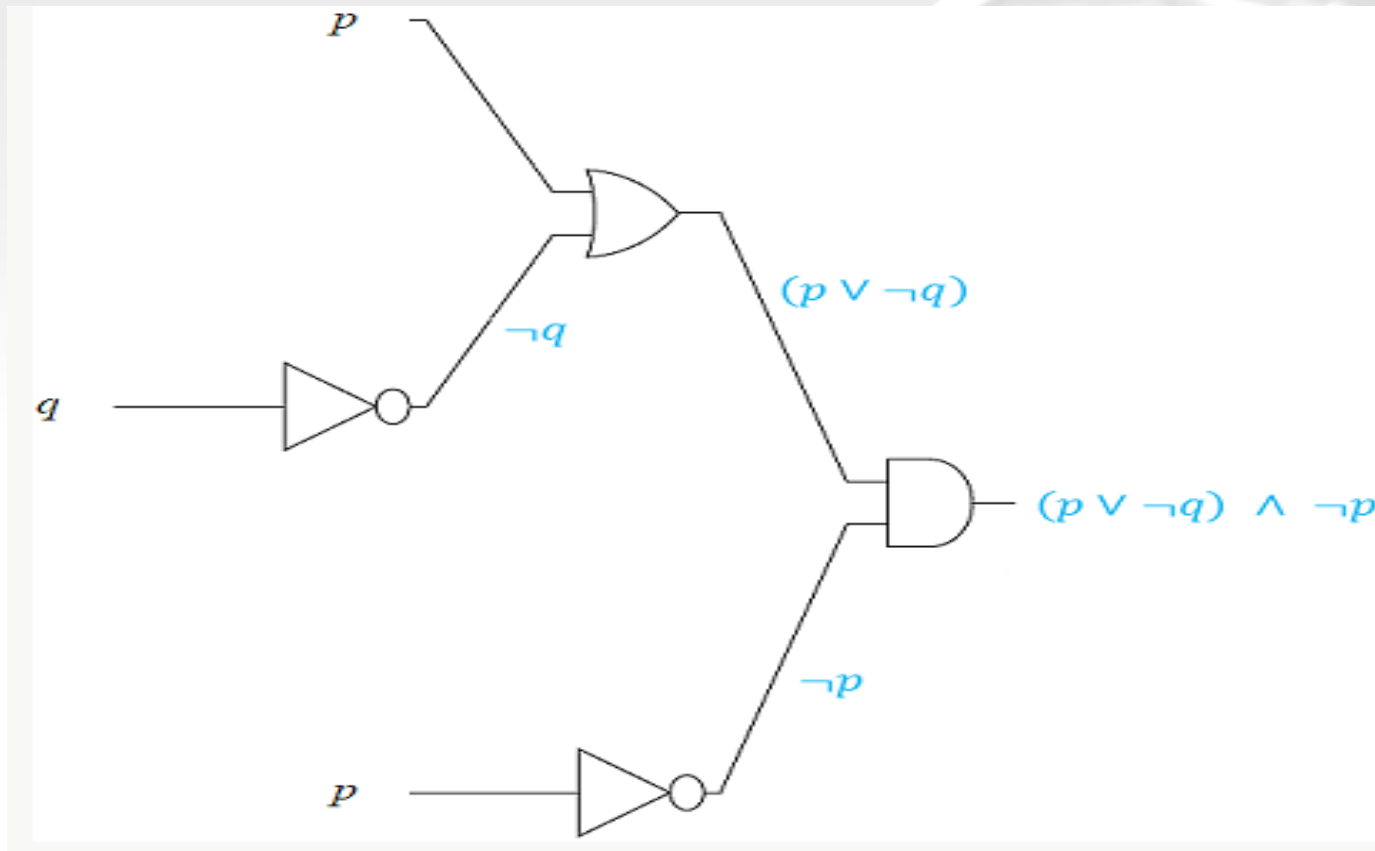
Solution

Working backwards from right to left we have the following sequence of gates

- 1) An **AND** gate $(p \vee \neg q) \wedge \neg p$.
- 2) The inputs to the **AND** gate are $(p \vee \neg q)$ and $\neg p$.
- 3) These inputs come from the output of an **INVERTER**, for $\neg p$ and an **OR** gate $(p \vee \neg q)$.
- 4) There are two inputs to the **OR** gate $(p \vee \neg q)$, being p , and the output of an **INVERTER**, $\neg q$.

Putting these now in left to right order we obtain the following logic circuit.

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Example 27 - Design a Logic Circuit

Design a logic circuit for $r \wedge (p \vee (r \wedge \neg q))$.

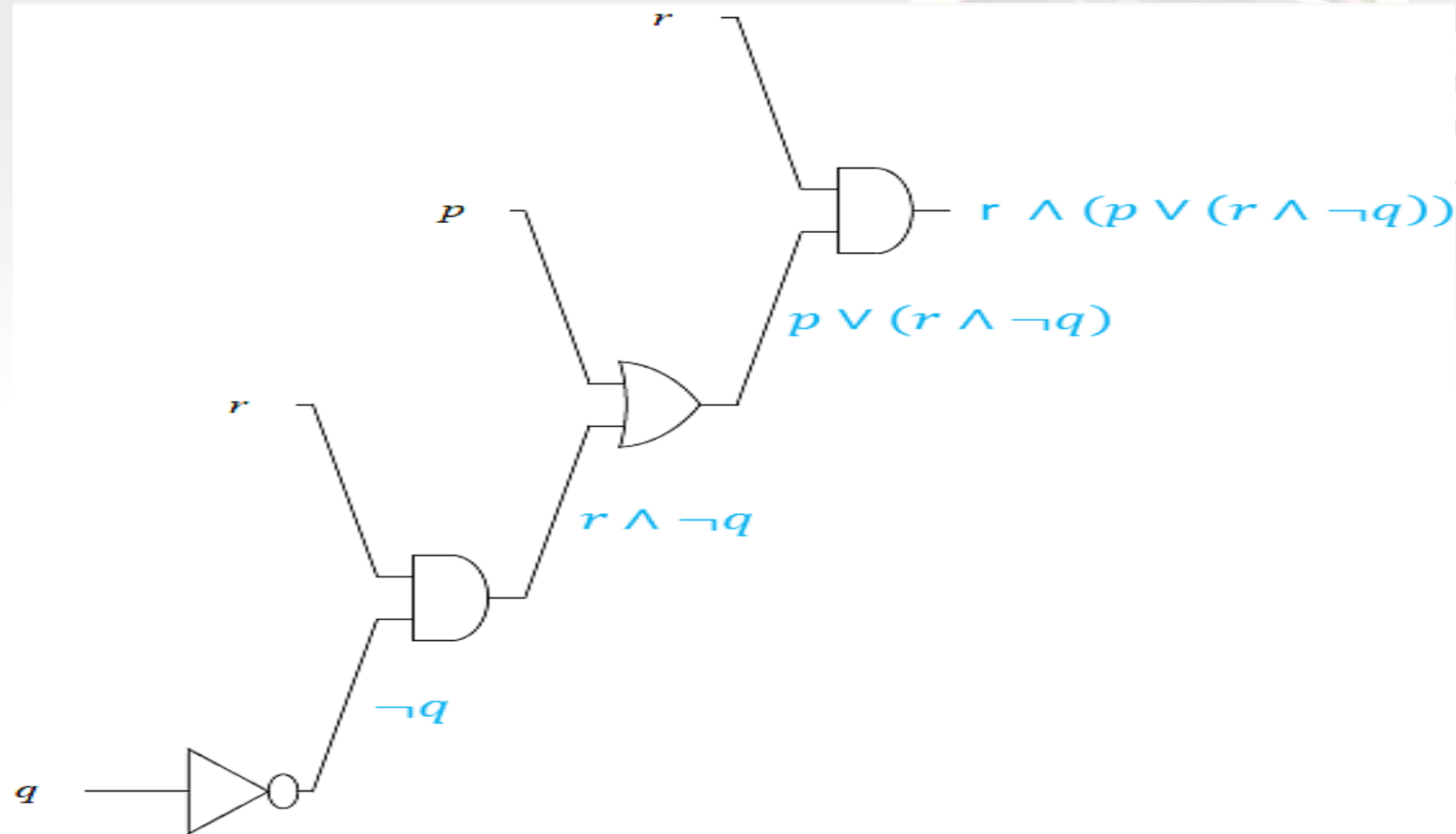
Solution

Working backwards from right to left we have the following sequence of gates

- 1) An **AND** gate $r \wedge (p \vee (r \wedge \neg q))$.
- 2) The inputs to the **AND** gate are r and $p \vee (r \wedge \neg q)$.
- 3) The input, $p \vee (r \wedge \neg q)$, comes from the output of an **OR** gate for $p \vee (r \wedge \neg q)$.
- 4) The inputs to the **OR** gate, $p \vee (r \wedge \neg q)$, are p and $(r \wedge \neg q)$, which is an **AND** gate.
- 5) The inputs to the **AND** , gate, $r \wedge \neg q$, are r and the output of an **INVERTER** , $\neg q$.

Putting these now in left to right order we obtain the following logic circuit.

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