Design, Analysis and Simulation of an I/O Link Second interim report

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Index Terms

High-Speed Data Links, Low-Power 10Gb/s link.

1 Choice of RX topology

For the receiver we made several choices with regard to what topology and types of elements to use. The general topology we chose to use for the receiver is depicted in figure 1.

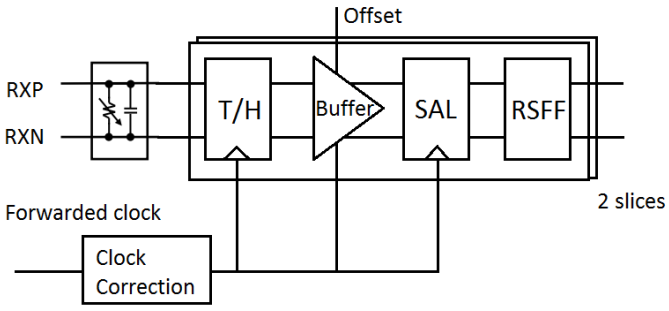

Fig. 1: Transmitter top level topology

The choice of topology is based on the work in [1].
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2 Performance results

Todo write sth here!
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3 Receiver schematics

The top-level schematic of our receiver is shown in figure 2. It conists of two of the receiver slices shown in figure 4 and an input impedance tuning circuit shown in figure 3. Each slice consists of a track-and-hold (simply a transistor together with the input capacitance of the next stage), a variable offset amplifier (figure 5), a strongARM latch (figure 6) and a RS-flipflop like in figure 7 as final stage.
The input impedance tuning circuit consists of a fixed portion and switched resistors which are doubled in size between each bit. Same is true for the tuneable load in the voltage amplifier, here also each transistor width is doubled for the next bit.
The final used transistor scalings and control voltages are shown in table 1.

type	value
termination resistor (fixed, parallel)	131 Ω
termination resistor (switched, smallest)	220 Ω
termination nmos switch	20 μm
track-and-hold pmos	20 μm
VOA differential nmos	2 μm
VOA nmos current source	16 μm
VOA load pmos (smallest)	400 nm
VOA pctl pass	10 μm
pctl	757 mV
nctl	320 mV
strongARM clk nmos	2 μm
strongARM input nmos	2 μm
strongARM inverter nmos	300 nm
strongARM inverter pmos	600 nm
strongARM reset pmos (output pull)	750 nm
strongARM reset pmos (sense short)	1 μm
RS-flipflop nmos	2 μm
RS-flipflop pmos	2 μm

TABLE 1: Used transistor sizes

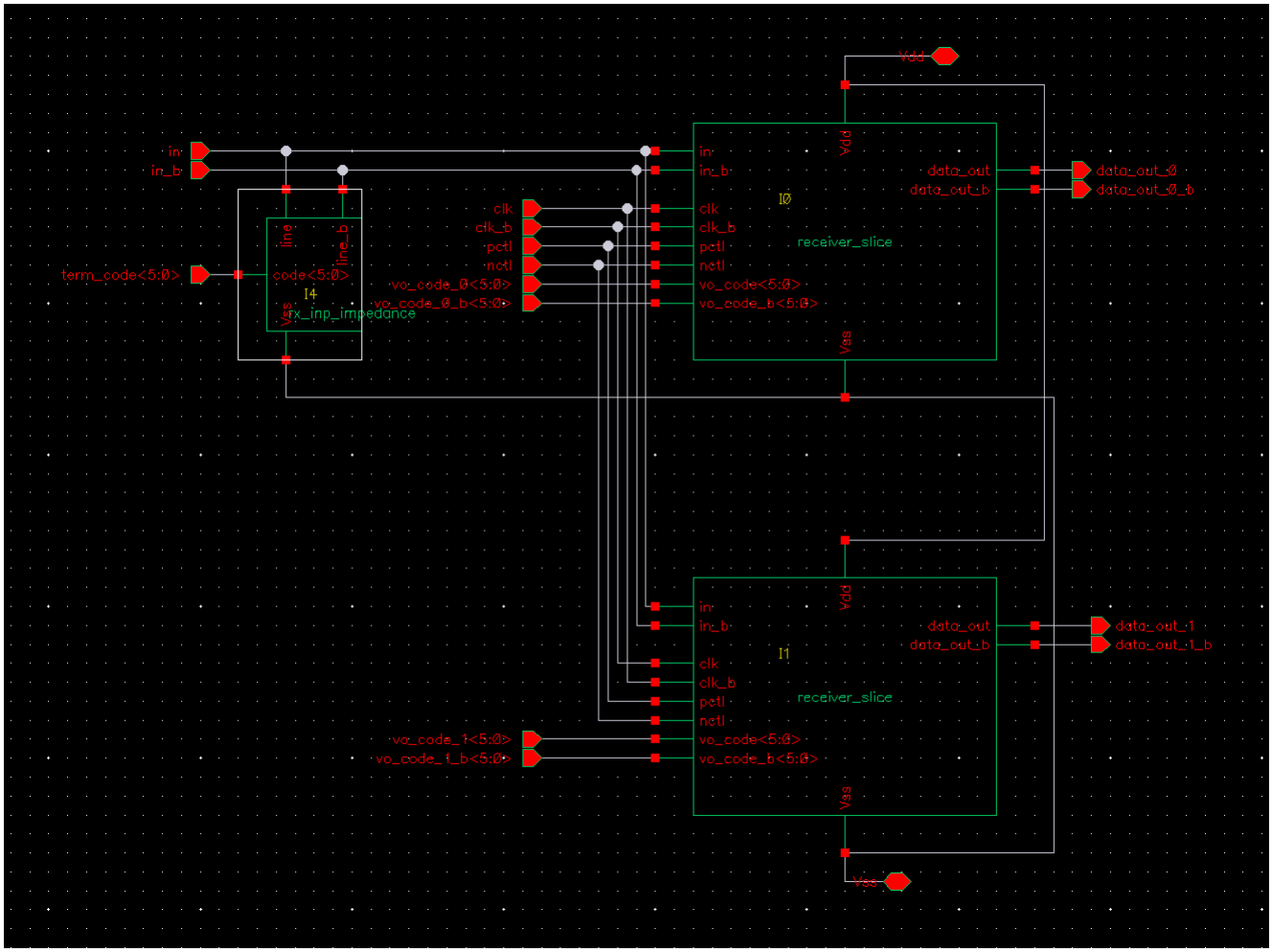


Fig. 2: Receiver top level circuit

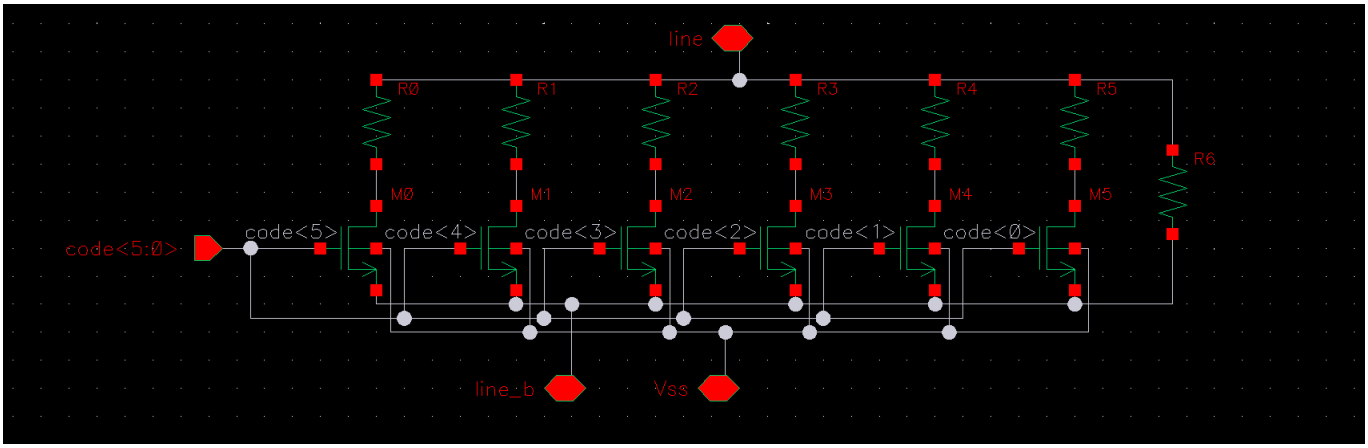


Fig. 3: Receiver input impedance tuning circuit

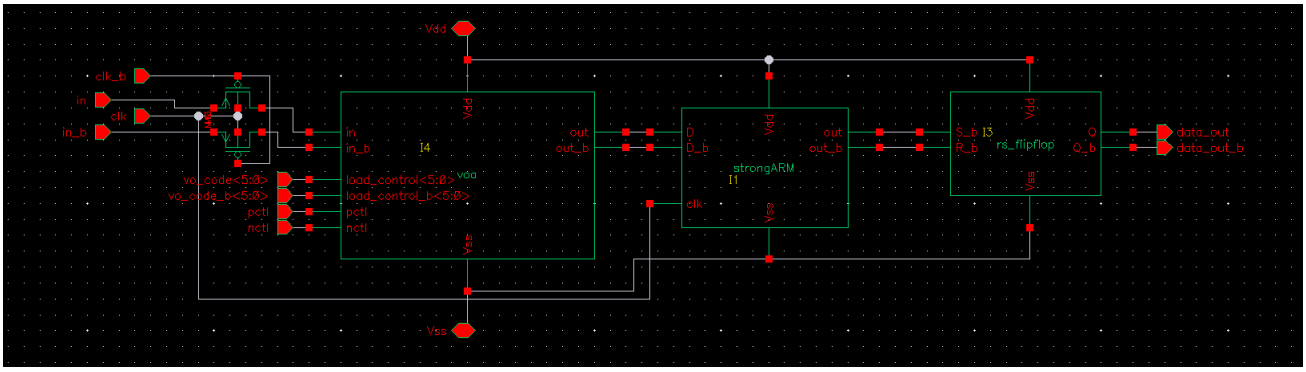
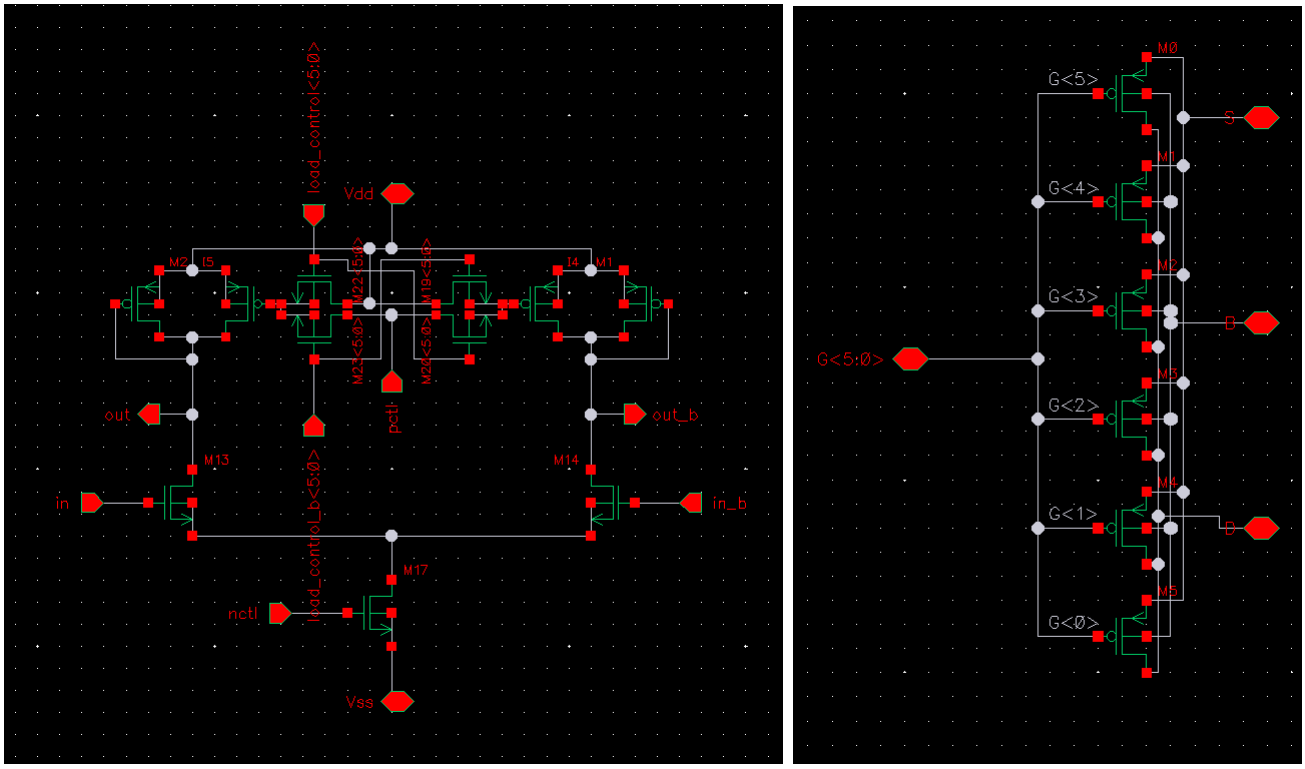


Fig. 4: Receiver slice circuit



(a) Variable offset amplifier

(b) scaled p-channel devices

Fig. 5: Variable offset amplifier (buffer). The devices I4 and I5 are multiple p-channel transistors scaled in size connected like shown in part (b).

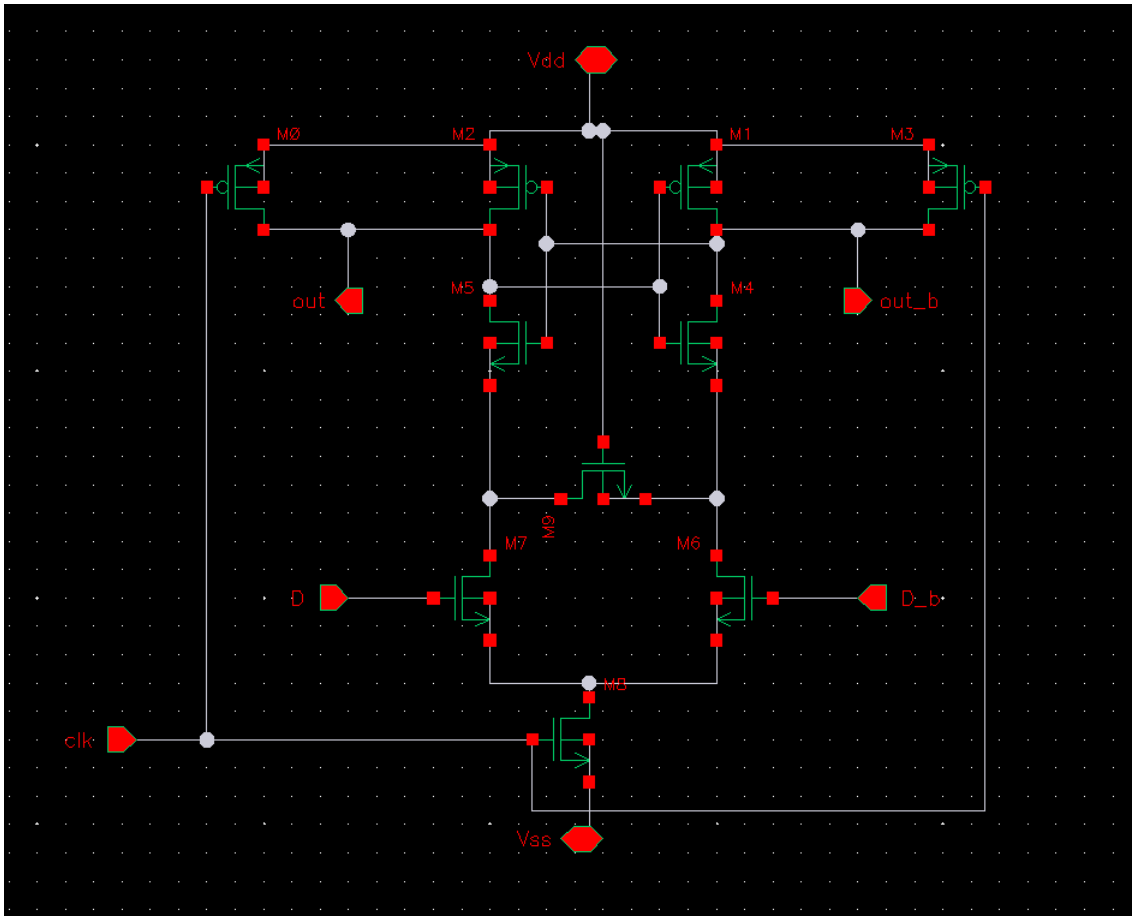


Fig. 6: StrongARM latch

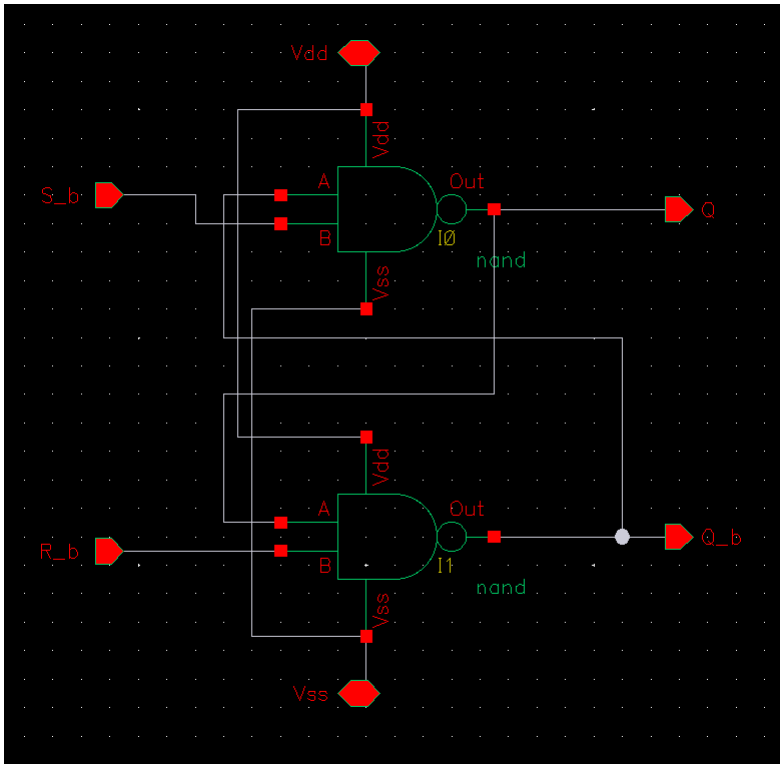


Fig. 7: RS-FlipFlop

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4 Performance results

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5 Performance results

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6 Performance results

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8 Performance results

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9 Performance results

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10 Performance results

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11 Performance results

TODO write sth here!

12 Performance results

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13 Bibliography

References

[1] Frank OMahony.... A 47 10 Gb/s 1.4 mW/Gb/s Parallel Interface in 45 nm CMOS, 2010.