Design, Analysis and Simulation of an I/O Link Second interim report

Carsten Bruns & Jakob Toft

Index Terms

High-Speed Data Links, Low-Power 10Gb/s link.

1 Choice of RX topology

For the receiver we made several choices with regard to what topology and types of elements to use. The general topology we chose to use for the receiver is depicted in figure 1.

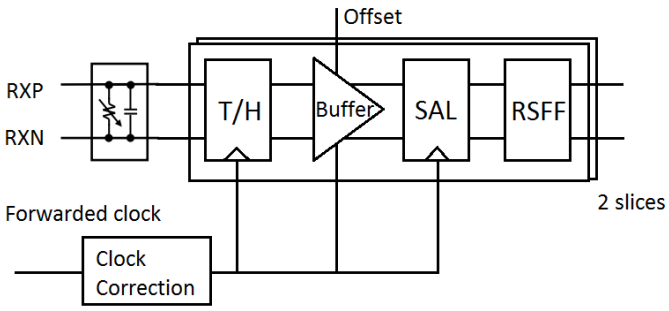


Fig. 1: Transmitter top level topology

The overall transceiver was to be a low-power 10 Gb/s link, and as such the receiver part of the link has to be power efficient like the transmitter. Thus we choose to base our topology on the design used in [1], as this design implements a half-rate low-power link. As we chose to design our transmitter using half-rate clocking, it makes sense to implement a receiver with the same clock-rate, such that the clock can be forwarded to the receiver. We could have chosen not to forward the clock, but this would have generated the need to implement another clock-generator, which would add to the total power consumption.

Tuning of the termination impedance is done in the beginning of the receiver using several transistors and resistors in parallel, giving the possibility of tuning the impedance with a certain resolution.

The receiver is a 2-slice design as each slice is clocked at half-rate of the data, this introduces the need to implement a synchronizer after the slices but this can hopefully be implemented in low-power CMOS technology.

Each slice has a Track and Hold (sometimes called Sample and Hold) switch, depicted as ”T/H” in figure 1.

For the buffer we chose to implement a VOA-3 amplifier as this should have a lower power penalty than a VOA-1 or VOA-2, and it is simpler than the VOA-4 amplifier.

For the strong-arm latch we chose to try and do our implementation with only one SAL instead of the two the use in [1], in the hope of reducing the power consumption. If the load

that the SAL needs to drive is too big to obtain the desired BW, we may need to introduce another SAL or re-think our receiver design.

We decided to not use CTLE nor DFE in the initial topology as these increase the power complexity of the receiver, we may need to add one or both of these later on if our signal needs more equalization.

2 RECEIVER SCHEMATICS

The top-level schematic of our receiver is shown in figure 2. It conists of two of the receiver slices shown in figure 4 and an input impedance tuning circuit shown in figure 3. Each slice consists of a track-and-hold (simply a transistor together with the input capacitance of the next stage), a variable offset amplifier (figure 5), a strongARM latch (figure 6) and a RS-flipflop like in figure 7 as final stage.
The input impedance tuning circuit consists of a fixed portion and switched resistors which are doubled in size between each bit. Same is true for the tuneable load in the voltage amplifier, here also each transistor width is doubled for the next bit.
The final used transistor scalings and control voltages are shown in table 1.

type	value
termination resistor (fixed, parallel)	131 Ω
termination resistor (switched, smallest)	220 Ω
termination nmos switch	20 μm
track-and-hold pmos	20 μm
VOA differential nmos	2 μm
VOA nmos current source	16 μm
VOA load pmos (smallest)	400 nm
VOA pctl pass	10 μm
pctl	757 mV
nctl	320 mV
strongARM clk nmos	2 μm
strongARM input nmos	2 μm
strongARM inverter nmos	300 nm
strongARM inverter pmos	600 nm
strongARM reset pmos (output pull)	750 nm
strongARM reset pmos (sense short)	200 nm
RS-flipflop nmos	2 μm
RS-flipflop pmos	2 μm

TABLE 1: Used transistor sizes

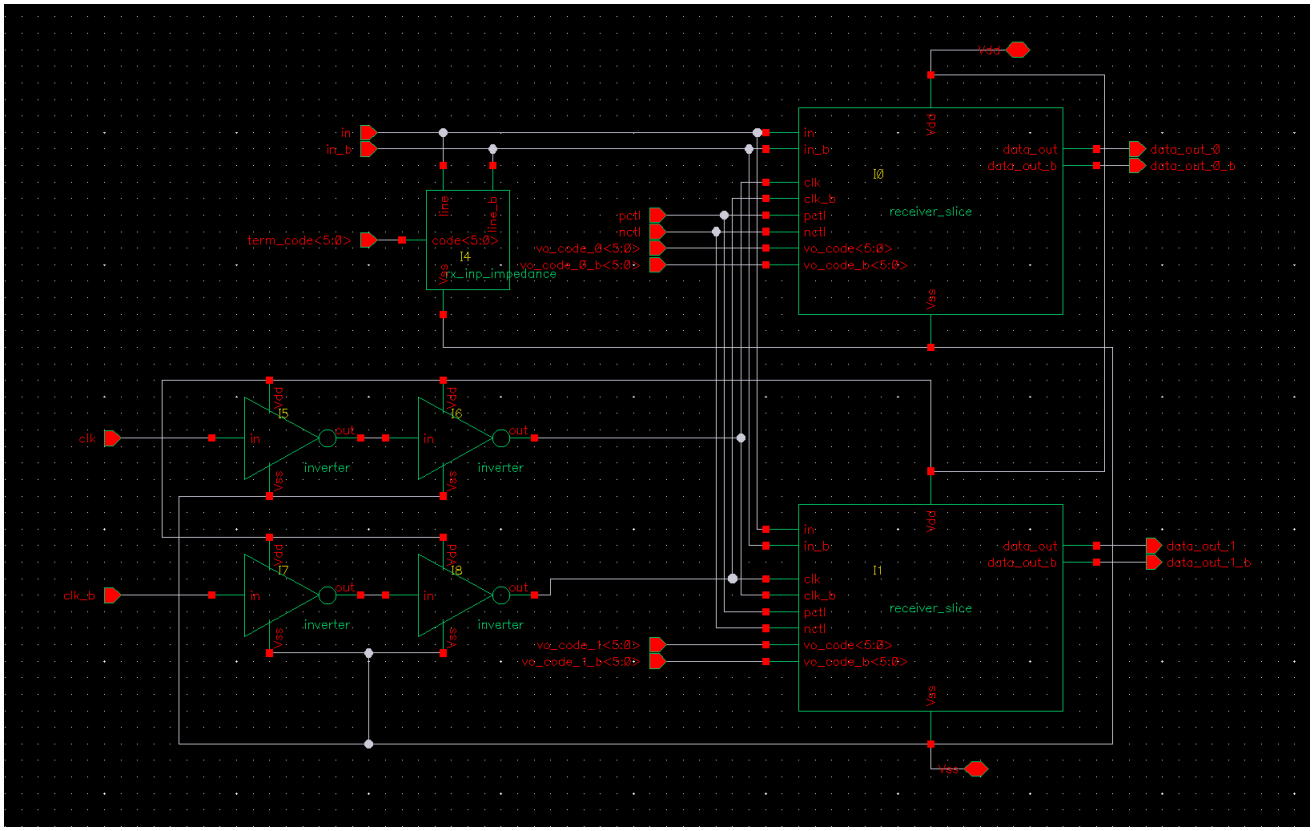


Fig. 2: Receiver top level circuit

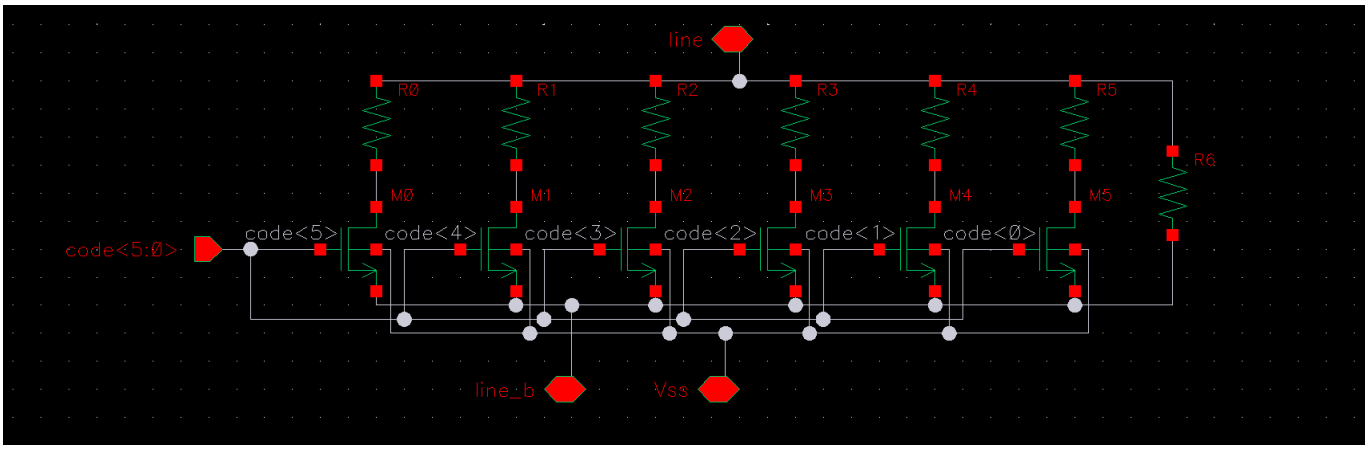


Fig. 3: Receiver input impedance tuning circuit

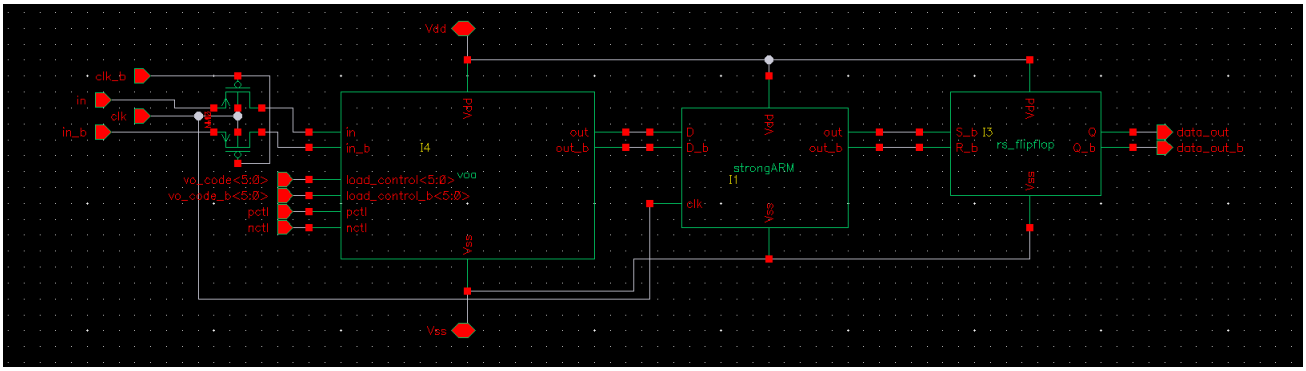
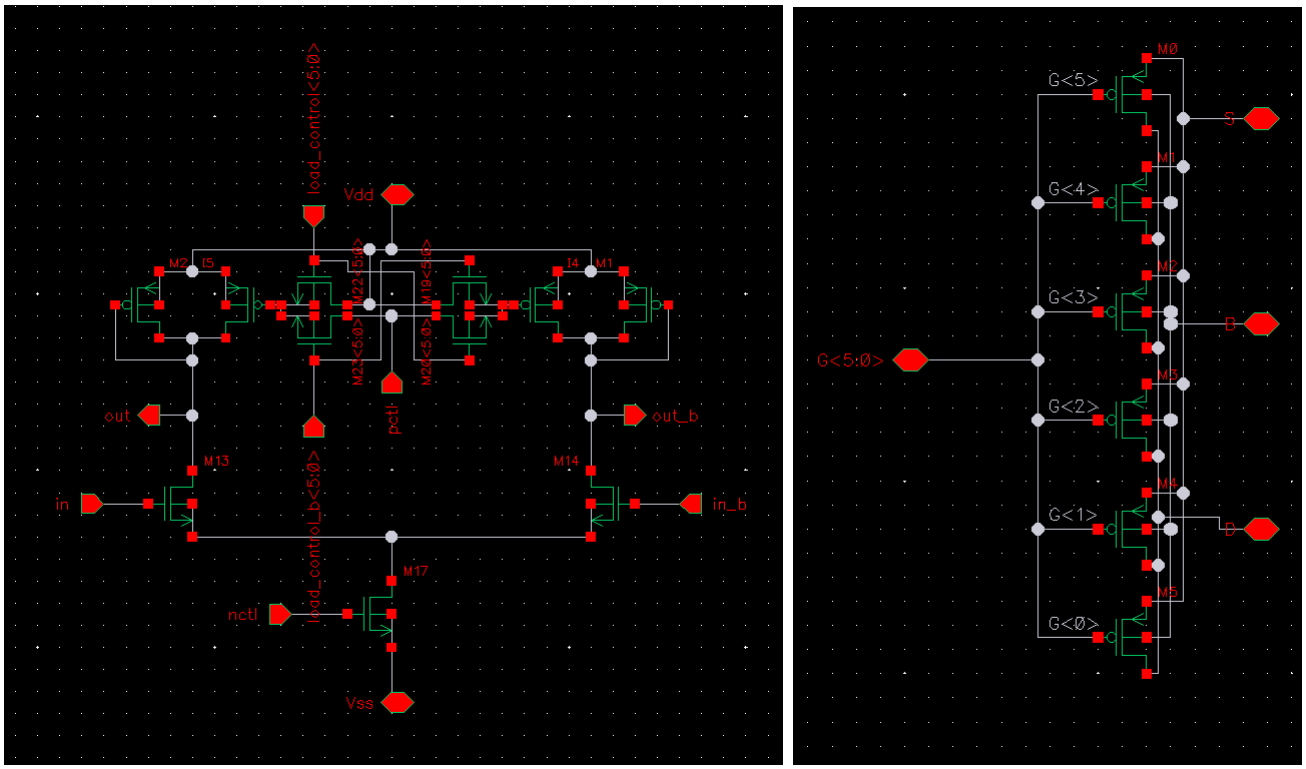


Fig. 4: Receiver slice circuit



(a) Variable offset amplifier

(b) scaled p-channel devices

Fig. 5: Variable offset amplifier (buffer). The devices I4 and I5 are multiple p-channel transistors scaled in size connected like shown in part (b).

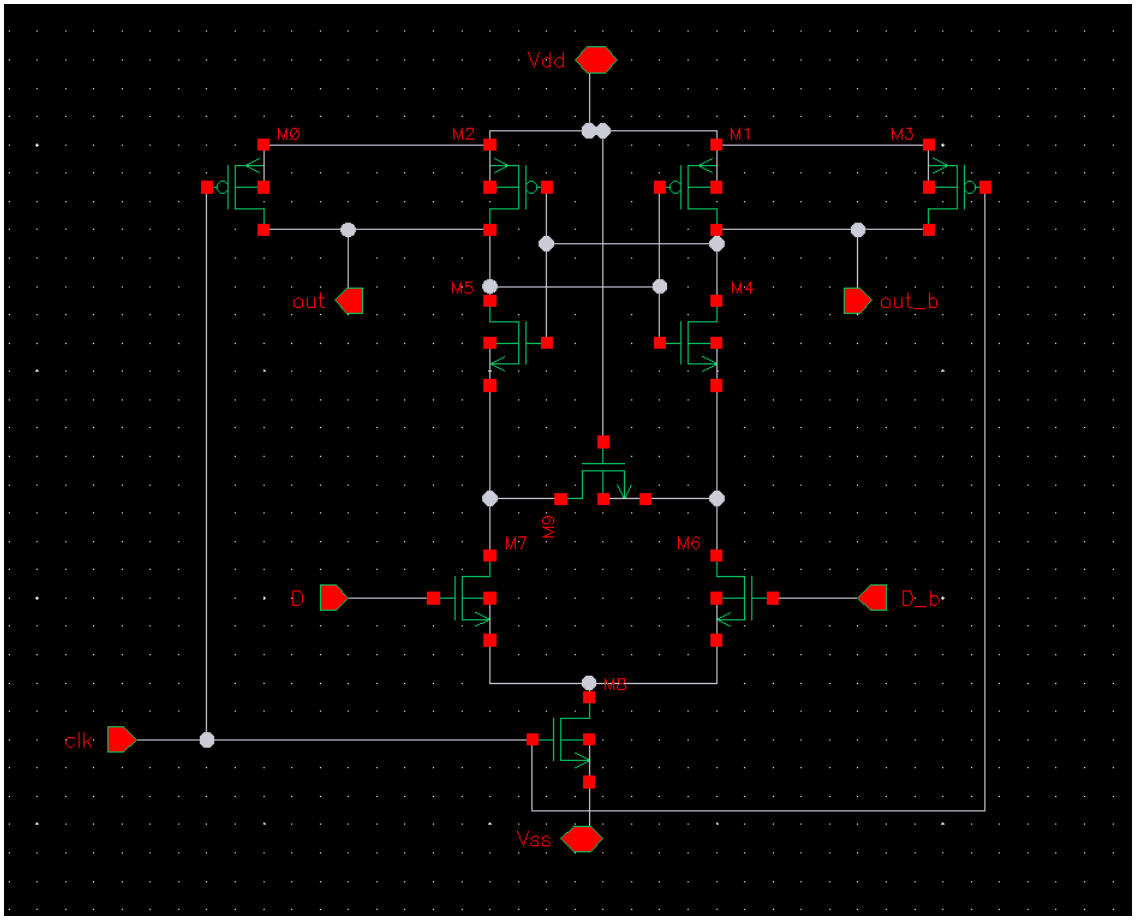


Fig. 6: StrongARM latch

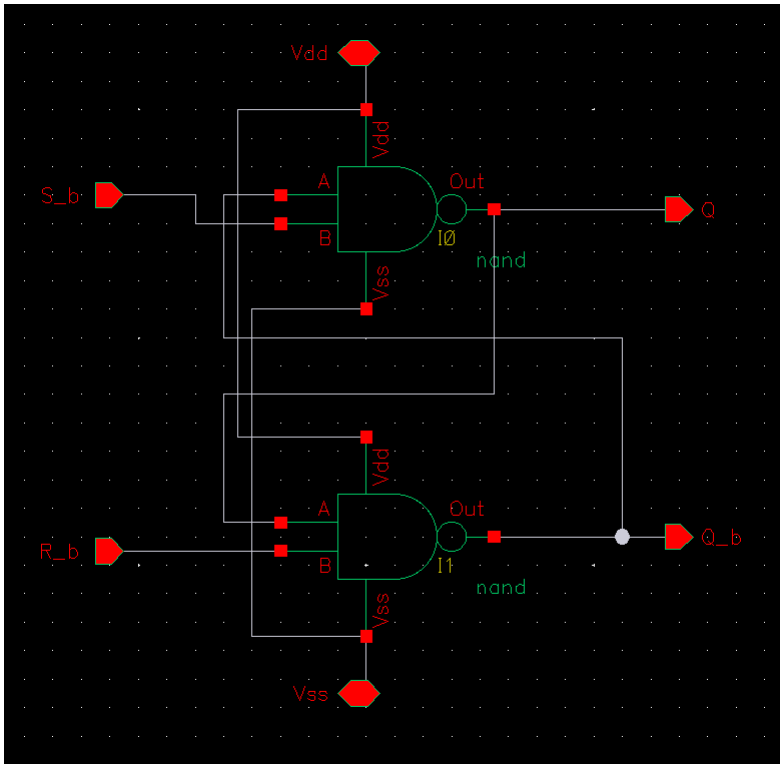


Fig. 7: RS-FlipFlop

3 Performance results

TODO write sth here!

4 Performance results

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5 Performance results

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6 Performance results

TODO write sth here!

7 Performance results

TODO write sth here!

8 Performance results

TODO write sth here!

9 Performance results

TODO write sth here!

10 Performance results

TODO write sth here!

11 Performance results

TODO write sth here!

12 Bibliography

References

[1] Frank OMahony.... A 47 10 Gb/s 1.4 mW/Gb/s Parallel Interface in 45 nm CMOS, 2010.