Design, Analysis and Simulation of an I/O Link Second interim report

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Index Terms

High-Speed Data Links, Low-Power 10Gb/s link.

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1 Choice of RX topology

For the receiver we made several choices with regard to what topology and types of elements to use. The general topology we chose to use for the receiver is depicted in figure 1.

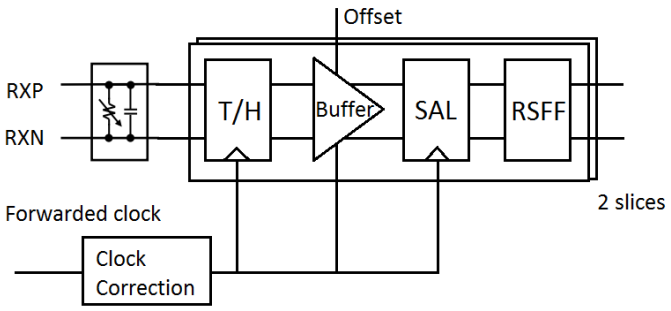


Fig. 1: Transmitter top level topology

The overall transceiver was to be a low-power 10 Gb/s link, and as such the receiver part of the link has to be power efficient like the transmitter. Thus we choose to base our topology on the design used in [1], as this design implements a half-rate low-power link. As we chose to design our transmitter using half-rate clocking, it makes sense to implement a receiver with the same clock-rate, such that the clock can be forwarded to the receiver. We could have chosen not to forward the clock, but this would have generated the need to implement another clock-generator, which would add to the total power consumption.

Tuning of the termination impedance is done in the beginning of the receiver using several transistors and resistors in parallel, giving the possibility of tuning the impedance with a certain resolution.

The receiver is a 2-slice design as each slice is clocked at half-rate of the data, this introduces the need to implement a synchronizer after the slices but this can hopefully be implemented in low-power CMOS technology.

Each slice has a Track and Hold (sometimes called Sample and Hold) switch, depicted as ”T/H” in figure 1.

For the buffer we chose to implement a VOA-3 amplifier as this should have a lower power penalty than a VOA-1 or VOA-2, and it is simpler than the VOA-4 amplifier.

For the strong-arm latch we chose to try and do our implementation with only one SAL instead of the two the use in [1], in the hope of reducing the power consumption. If the load that the SAL needs to drive is too big to obtain the desired BW, we may need to introduce another SAL or re-think our receiver design.

We decided to not use CTLE nor DFE in the initial topology as these increase the power complexity of the receiver, we may need to add one or both of these later on if our signal needs more equalization.

2 RECEIVER SCHEMATICS

The top-level schematic of our receiver is shown in figure 2. It conists of two of the receiver slices shown in figure 4 and an input impedance tuning circuit shown in figure 3. Each slice consists of a track-and-hold (simply a transistor together with the input capacitance of the next stage), a variable offset amplifier (figure 5), a strongARM latch (figure 6) and a RS-flipflop like in figure 7 as final stage.
The input impedance tuning circuit consists of a fixed portion and switched resistors which are doubled in size between each bit. Same is true for the tuneable load in the voltage amplifier, here also each transistor width is doubled for the next bit.

Scaling of transistors in the receiver was done element-wise. We started by sizing the RS-flipflop as we knew this needed to be able to drive a load of 20fF. Sizing of the RS-flipflop was done by estimating the required output resistance that would result in the desired bandwidth (5Gb/s), then simulating with the estimated values and then monkey-tuning the sizes until the wave-forms seemed acceptable.

From the RS-flipflop we went backwards in the receiver, sizing the strongARM-latch afterwards, then the buffer, then the T/H, and finally the impedance tuning of the receiver.

The sizing was done for one slice, and the second slice will use the same parameters, as they should experience the same load.

The final used transistor scalings and control voltages are shown in table 1.

type	value
termination resistor (fixed, parallel)	131 Ω
termination resistor (switched, smallest)	220 Ω
termination nmos switch	20 μm
track-and-hold pmos	20 μm
VOA differential nmos	2 μm
VOA nmos current source	16 μm
VOA load pmos (smallest)	400 nm
VOA pctl pass	10 μm
pctl	757 mV
nctl	320 mV
strongARM clk nmos	2 μm
strongARM input nmos	2 μm
strongARM inverter nmos	300 nm
strongARM inverter pmos	600 nm
strongARM reset pmos (output pull)	750 nm
strongARM reset pmos (sense short)	200 nm
RS-flipflop nmos	2 μm
RS-flipflop pmos	2 μm

TABLE 1: Used transistor sizes

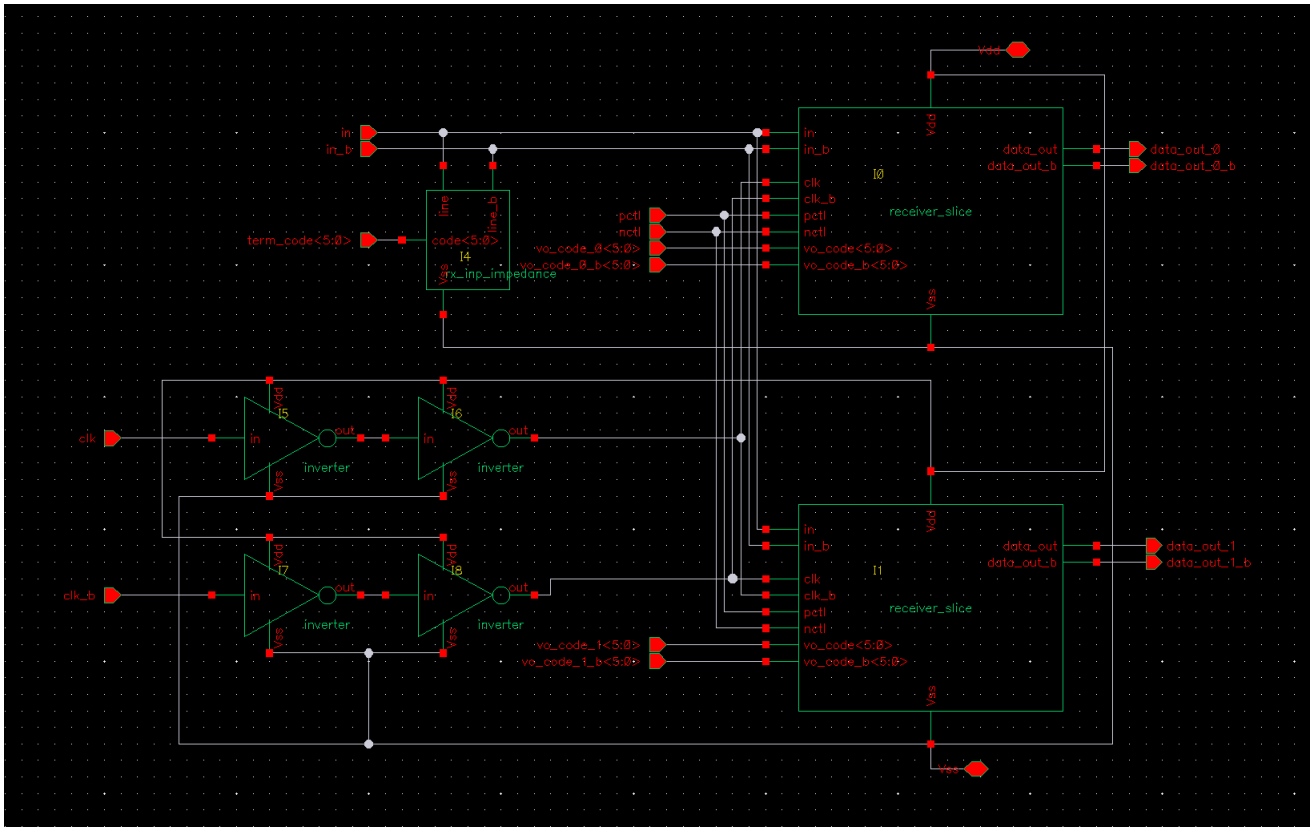


Fig. 2: Receiver top level circuit

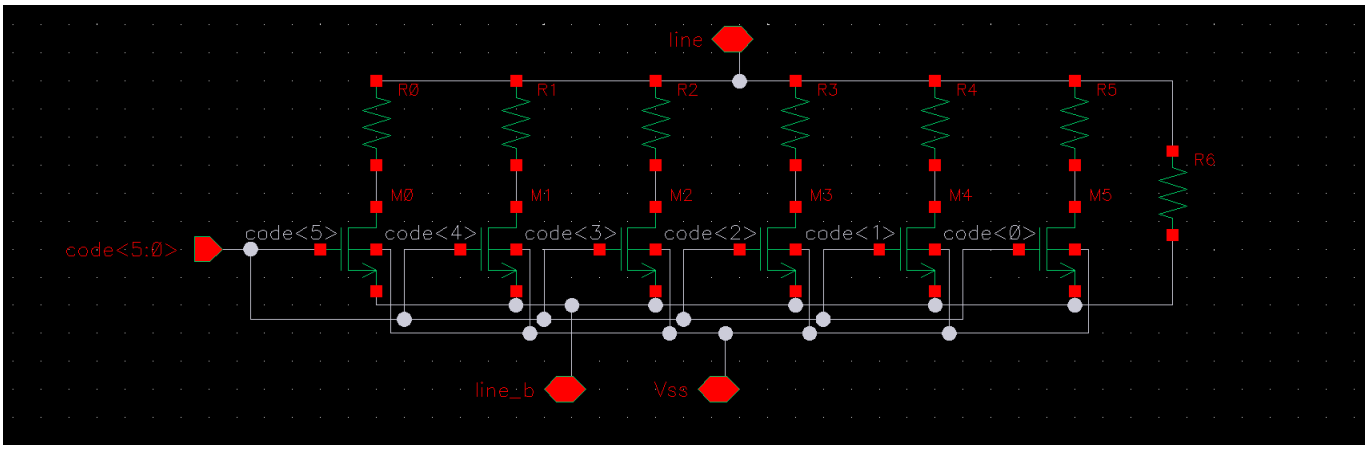


Fig. 3: Receiver input impedance tuning circuit

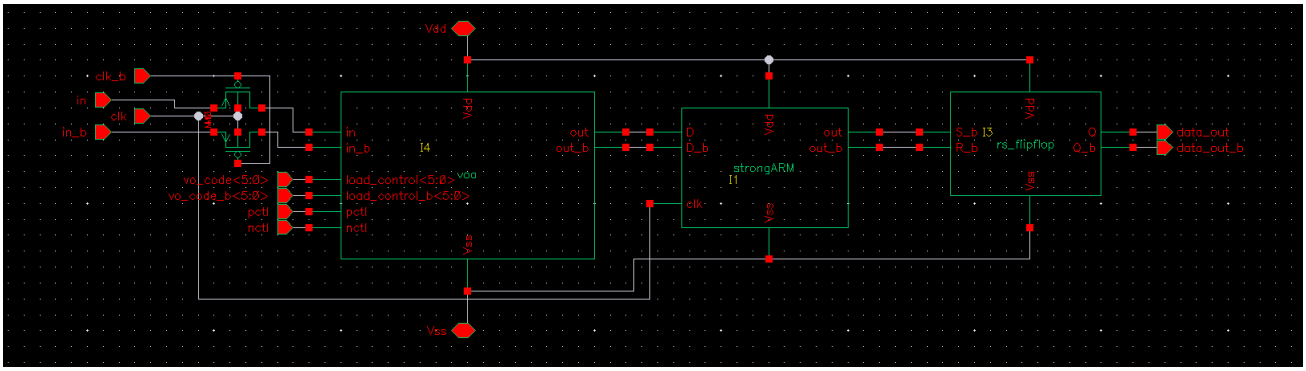
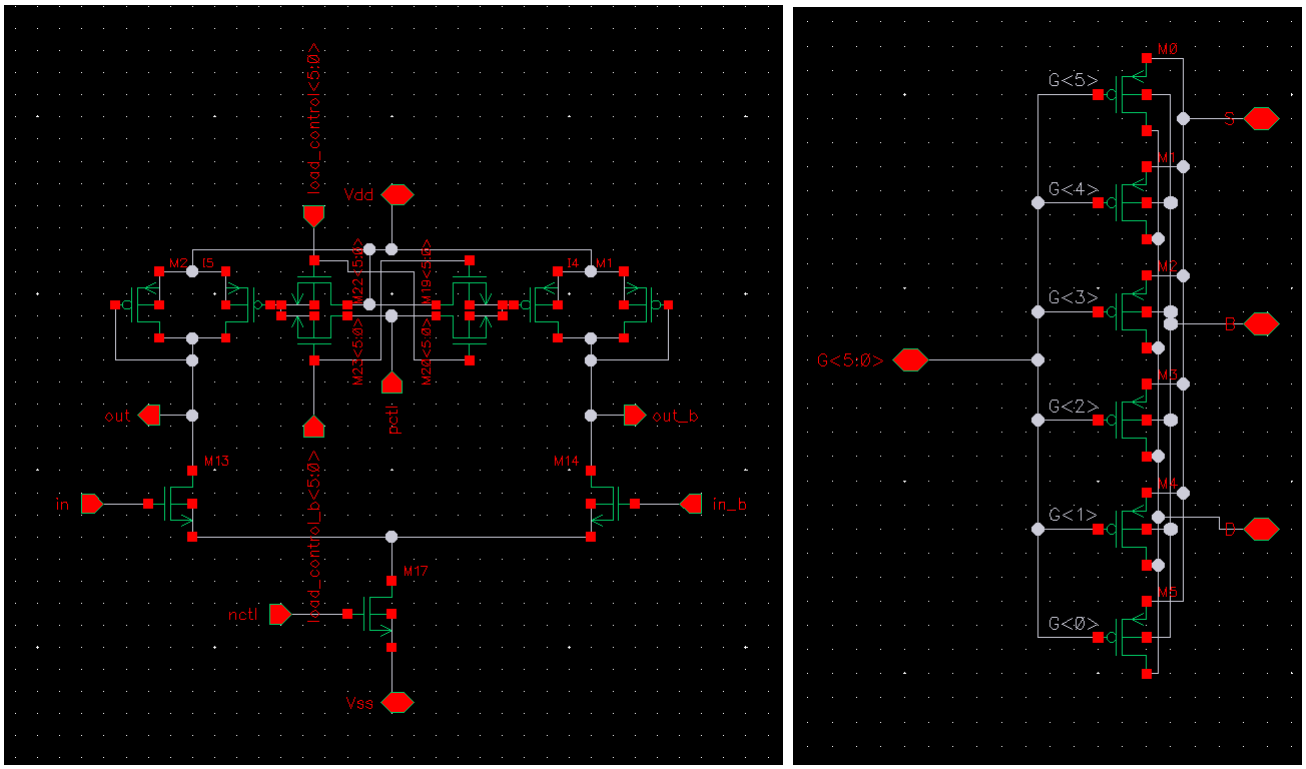


Fig. 4: Receiver slice circuit



(a) Variable offset amplifier

(b) scaled p-channel devices

Fig. 5: Variable offset amplifier (buffer). The devices I4 and I5 are multiple p-channel transistors scaled in size connected like shown in part (b).

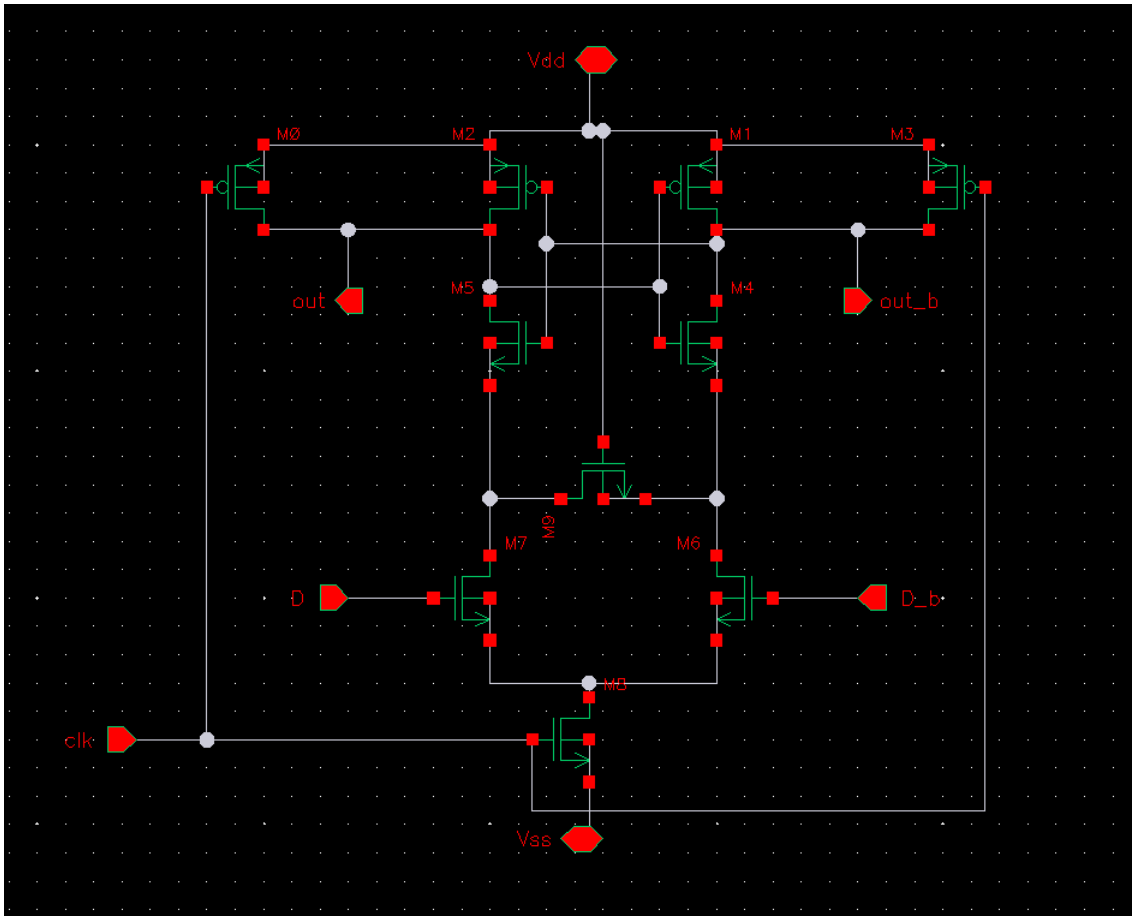


Fig. 6: StrongARM latch

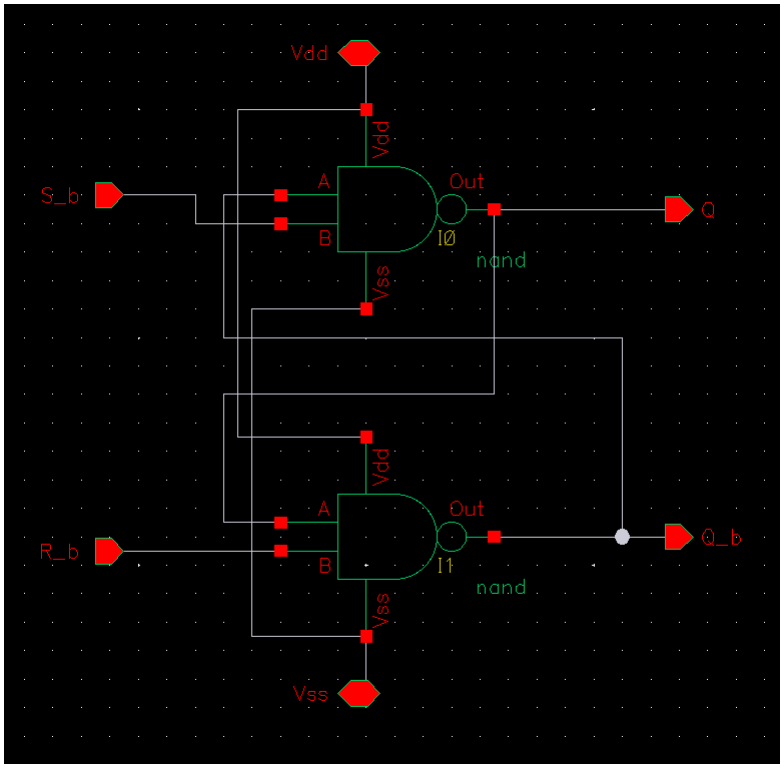


Fig. 7: RS-FlipFlop

3 SIMULATIONS

Figure 10 shows the output of the stongARM latch for alternating data at the input for 6 UI. For the simulation a data pattern of 11001100 was feed into the input of the receiver. As we have two slices with half-rate clocking this results in alternating data for one of the slices. To degenerate the signal and take the limited bandwith of the channel into account a RC circuit was used at the receiver input resulting in the *in+* and *in-* signals. The *set* and *reset* signals are the direct outputs of the strongARM circuit and the *RS_out* signal is one of the RS-FlipFlop outputs.

The frequency response of the variable offset amplifier (VOA) is shown in figure 8 and its ac noise response is drawn in figure 9.

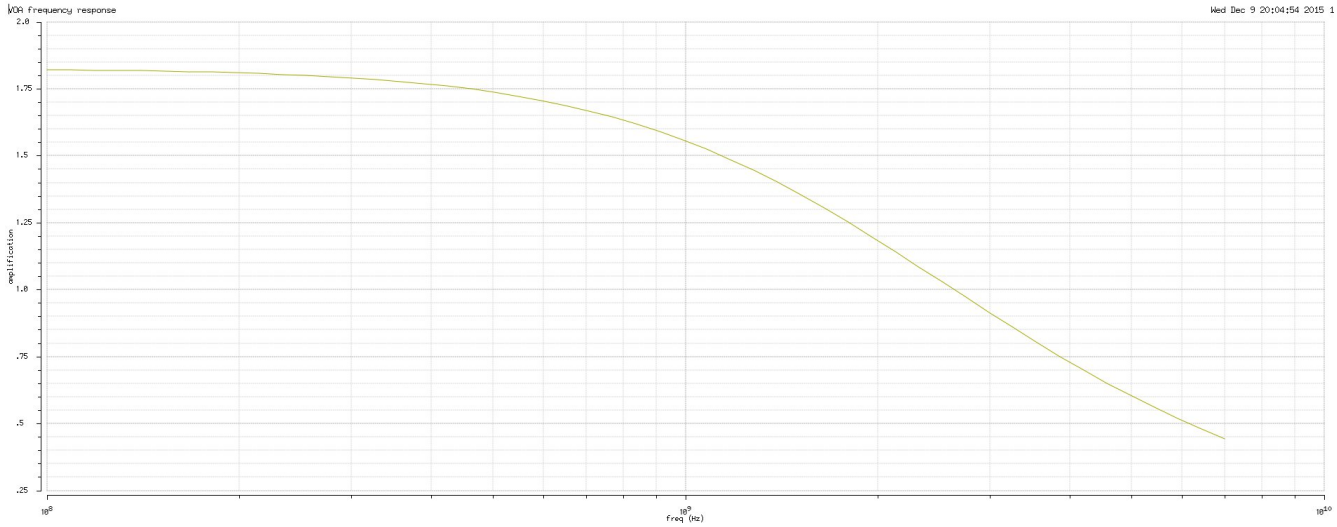


Fig. 8: VOA frequency response

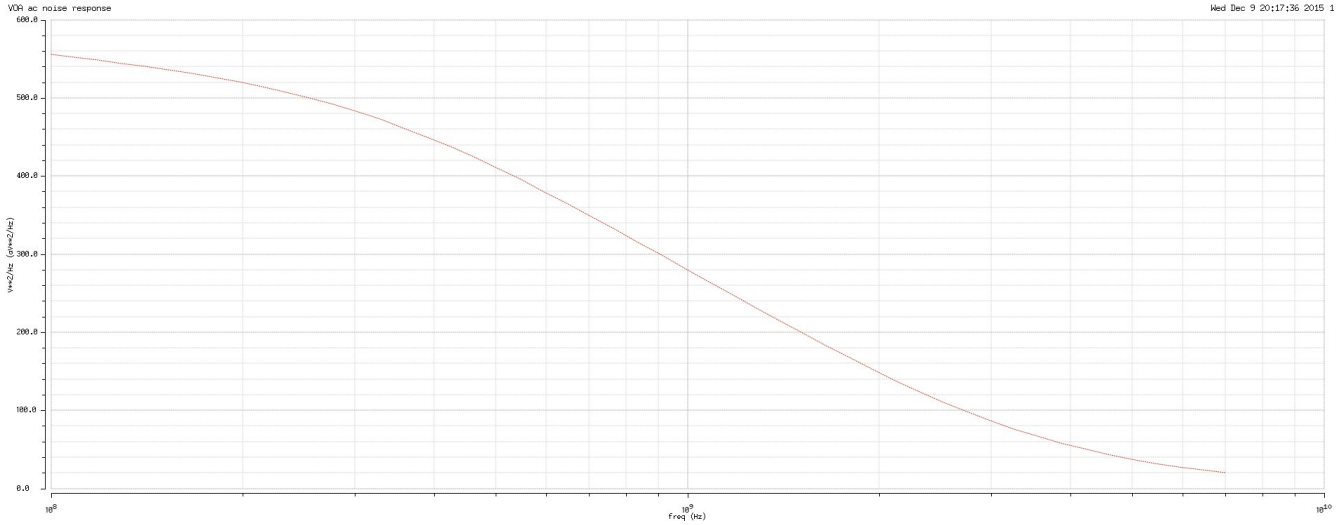


Fig. 9: VOA ac noise response

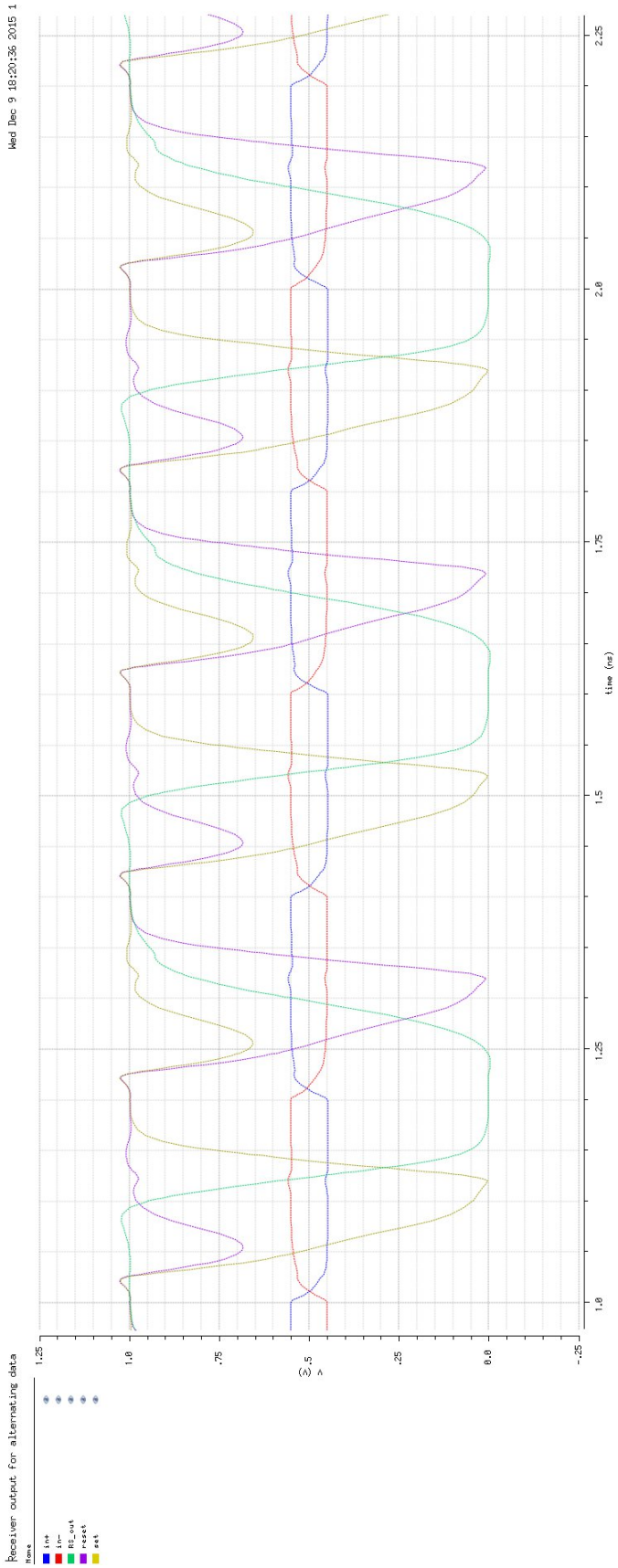


Fig. 10: Transient waveform for alternating data at the output of the strongARM latch

4 Performance Results

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5 Performance results

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6 Impedance and offset tuning

To tune the input impedance of the receiver the input consists of a fixed portion and six resistors which can be switched on, doubled in size between each of them (see section 2). The resulting input impedance values for different codes are shown in figure 11. The tuning ranges from 70 Ω to 130 Ω. Note that this tuning is not linear but as the best code has to be searched for the running link anyway, this leads only to small performance degradation as the tuning is more coarse for higher impedance values as for lower values.

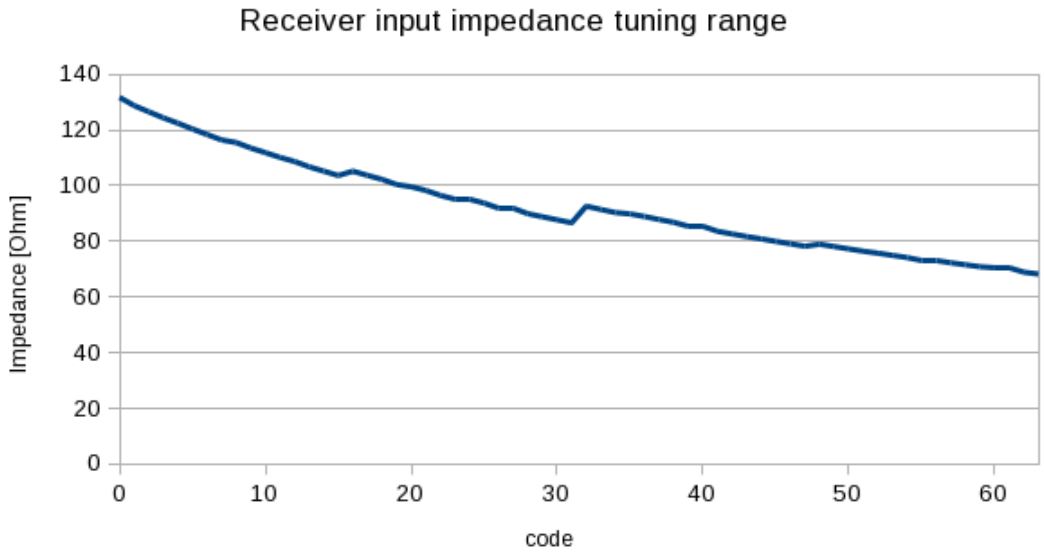

Fig. 11: Receiver input impedance tuning range

The variable offset voltage amplifier enables cancellation of offset voltages (e.g. due to mismatch in the differential pair of the strongARM latch). The achieved offset voltage over input code is shown in figure 12. It ranges from -100 mV to 100 mV and is pretty much linear.

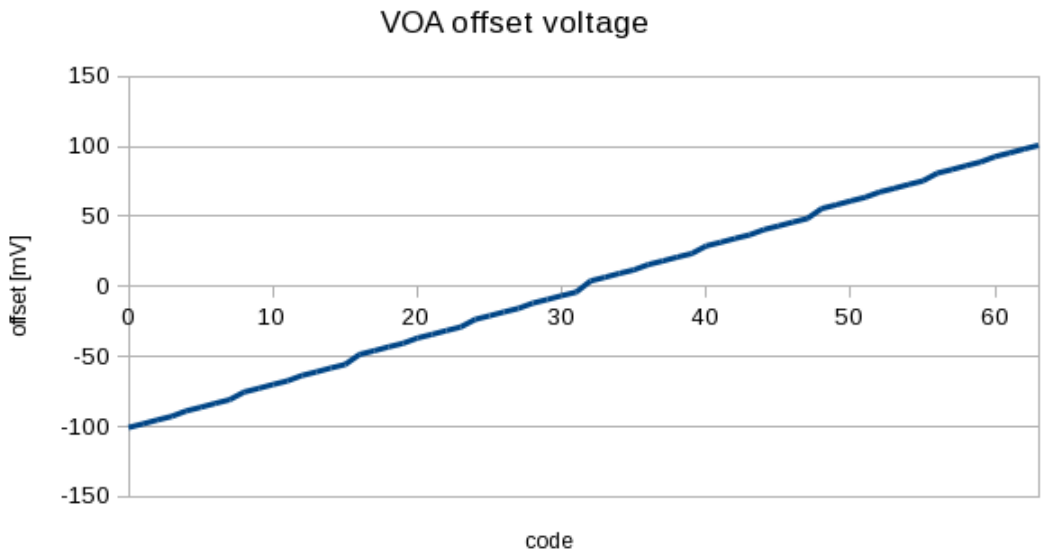

Fig. 12: VOA offset voltage tuning range

7 Power consumption

The power consumption at 10 Gb/s PRBS15 data and 1 V power supply is shown in table 2. The complete receiver consists of two receiver slices, each of them of VOA, strongARM and RS-FlipFlop (see section 2).

component	consumed power
complete receiver	2104 μW
clock buffers	1814 μW
receiver slice	136,3 μW
VOA	32,58 μW
strongARM	46,07 μW
RS-FlipFlop	57,66 μW

TABLE 2: Receiver power consumption at 10 Gb/s PRBS15 data and 1 V power supply

8 Performance results

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9 BIBLIOGRAPHY

REFERENCES

[1] Frank OMahony.... A 47 10 Gb/s 1.4 mW/Gb/s Parallel Interface in 45 nm CMOS, 2010.