ⓘ Dashed red lines indicate isolation barriers between TS and LV.

ⓘ Cyan areas indicate GLVS and cyan nets indicate signals from/to GLVS.

ⓘ Orange areas indicate TS and orange nets indicate high power TS.

Specifications:

f_sw = 40 kHz

V_in, max = 600 VDC
V_out, max = 245 V,RMS,ph-n (SVPWM)
I_out, max = 80 A,RMS
I_out, cont = 32 A,RMS

P_out, max = 53 kW
P_out, cont = 23.5 kW

Liquid cooled with water at 50ºC max

Changelog:

Version 1.0: (sent to production 15-02-2024)
- Base version

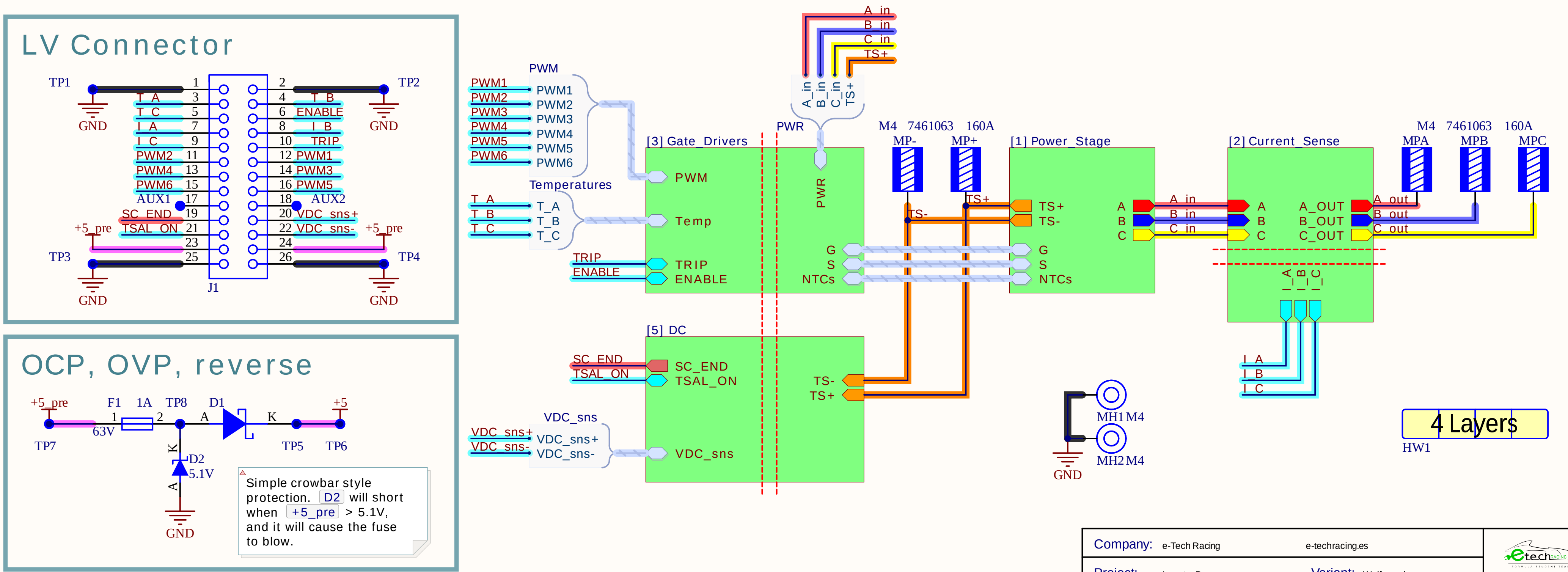
Version 1.1: (sent to production 28-03-2024)
- Added 5V supply protections
- Swapped pins 4 and 5 in gate drivers' LDOs
- Swapped MP+ and MP-, and their silkscreen
- Added testpoints for current sensors' reference
- Added testpoints for VDC_sns+ and VDC_sns-
- Renamed testpoints in [3]
- Added various silkscreen texts and indications
- Added layer physical logo

Changes in SCH but not in PCB:

19-04-2024: Added decoupling capacitors to semiconductor terminals (TS+ / TS-).

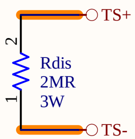
Known issues:

- D1 is not correctly rated. Replace with appropiate PMOS or beefier Schottky (beware the voltage drop)
- Rdis does practically nothing compared to R504 .. R510 and could be eliminated.
- R301 can be of lower value.
- Most DNP caps are actually needed.
- D501 failed once, but cause remains unknown.
- R501 should have a bigger value.
- R511 and R512 should have a small tolerance, and it should be specified in the schematic.
- 10uF 50V 0805 caps are expensive and should be replaced with 10uF 50V 1206 or 10uF 50V 1210.

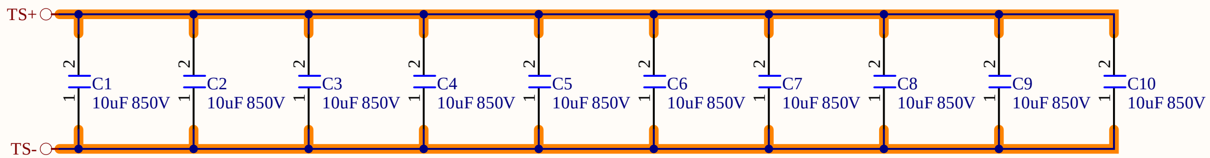


Company: e-Tech Racing	e-techracing.es		
Project: Inverter Power	Variant: Wolfspeed		
Size: -	Page Contents: Inverter_Power.SchDoc	Version: 1.1	
		Department: Powertrain	
Author: David Redondo	dredondovinolo@gmail.com	Sheet 1 of 5	
Checked by: -		Date: 29/05/2024	

Passive discharge



DC Bus capacitors, 100uF, Murata FHA85Y106KS



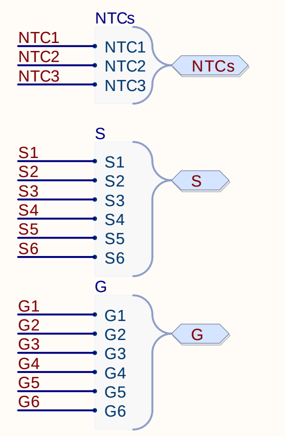
DC Link design considerations:

V_C > 1.1 · Vmax = 1.1 · 600 V = 660 V → 850 V

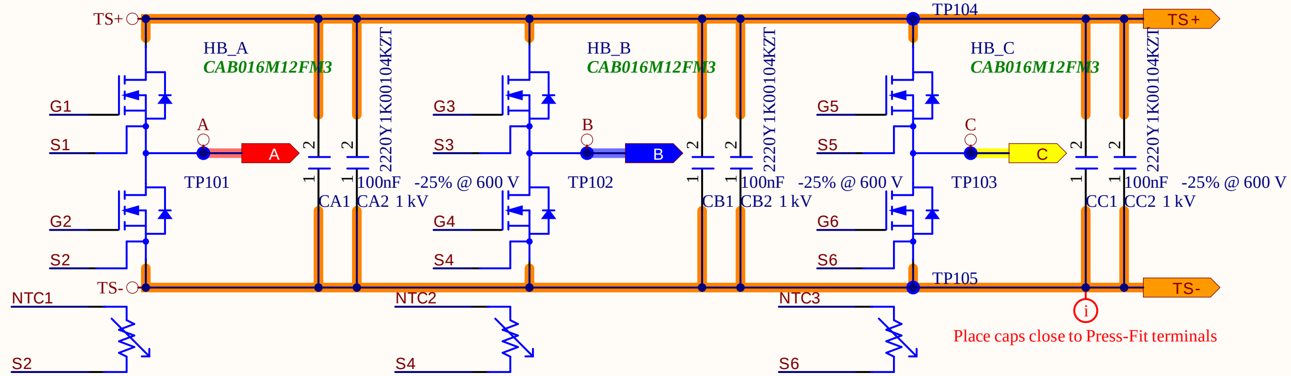
I_C,RMS ≈ 0.65 · I_phase,RMS = 0.65 · 80 A,RMS = 52 A,RMS → 10 x 5 A,RMS (ΔT = 10 ºC)
C > I_C,RMS / (V_ripple · f_sw) = 52 A,RMS / (15V · 40 kHz) ≈ 87 μF → 10 x 10 μF

Check:
https://www.specterengineering.com/blog/2019/9/7/dc-link-capacitor-selection-for-y

INPUTS/OUTPUTS

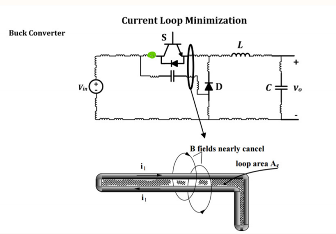


SiC Half-Bridges



Semiconductor details:

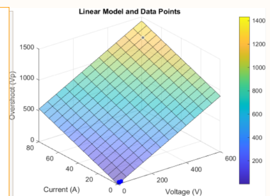
V_DSS(breakdown) = 1200 V // 1200 V
Ron = 5.5 .. 13 mΩ // 16.0 .. 28.8mΩ
Vf_D = 3.3 .. 4 V // 4.9 .. 5.5 V
T_rr = 41.5 .. 45 ns // 20.0 ns
Q_rr = 2.19 .. 3.94 μC // 1.30 μC
R_th_jc = 0.12 .. 0.15 K/W // 0.543 K/W
Q_G = 520 nC / 236 nC
C_in = 14.5 nF // 6.6 nF
R_G(int) = 1.9 Ω // 2.4 Ω
V_GS(th) = 2.8 .. 4.8 V // 1.8 .. 3.6 V



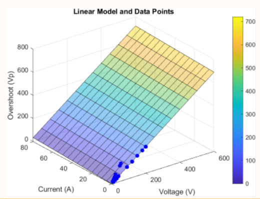
CA1, CA2, CB1, CB2, CC1, CC2

Current loop between top and bottom MOSFETs will cause excessive overshoot due to parasitic inductance and low parasitic capacitance. Increasing capacitance to hundreds of nF mitigates the effect. The capacitors essentially work as a switching decoupling. MLCCs with low DC bias or film, but MLCCs are way more compact. Place as close as possible to semiconductor terminals.

Overshoot analysis can be performed using a linear model proportional to DC bus voltage and output current. Easiest way to do it is using only one half bridge as a synchronous buck and varying input voltage with a fixed duty cycle and a R or RL load.



No C leads to 1430 Vp at max. specs.



C brings it down to 720 Vp at max. specs.

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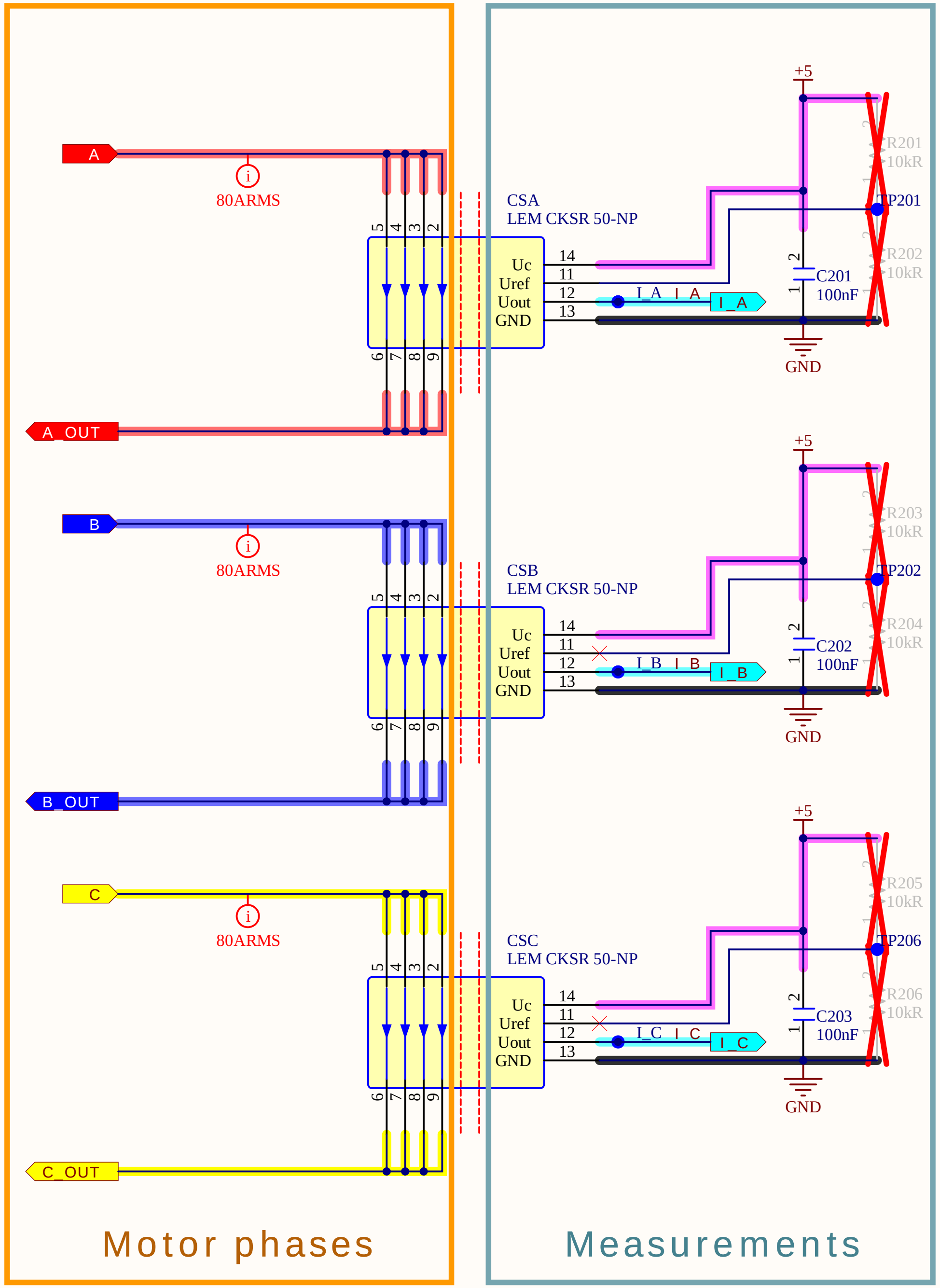
Project: Inverter Power	Variant: Wolfspeed		
Size: -	Page Contents: [1] Power_Stage.SchDoc	Version: 1.1	Department: Powertrain
Author: David Redondo	dredondovinolo@gmail.com	Sheet 2 of 5	
Checked by: -		Date: 29/05/2024	

CSA , CSB , CSC

CKSR 50-NP/SP1 configured with Number of primary turns = 1 (R_phase-connector = 0.18 mΩ)



CSA , CSB , CSC

CKSR 50-NP/SP1 2.5V internal reference is used in order to have equal measuring range for positive and negative values. Voltage divider implemented just in case.

I_A , I_B , I_C

U_meas = (12.5mV/A · I_meas + Uref)

For ±150Apk:
V_meas_pk+ = 4.375V
V_meas_pk- = 0.625V

C201 , C202 , C203

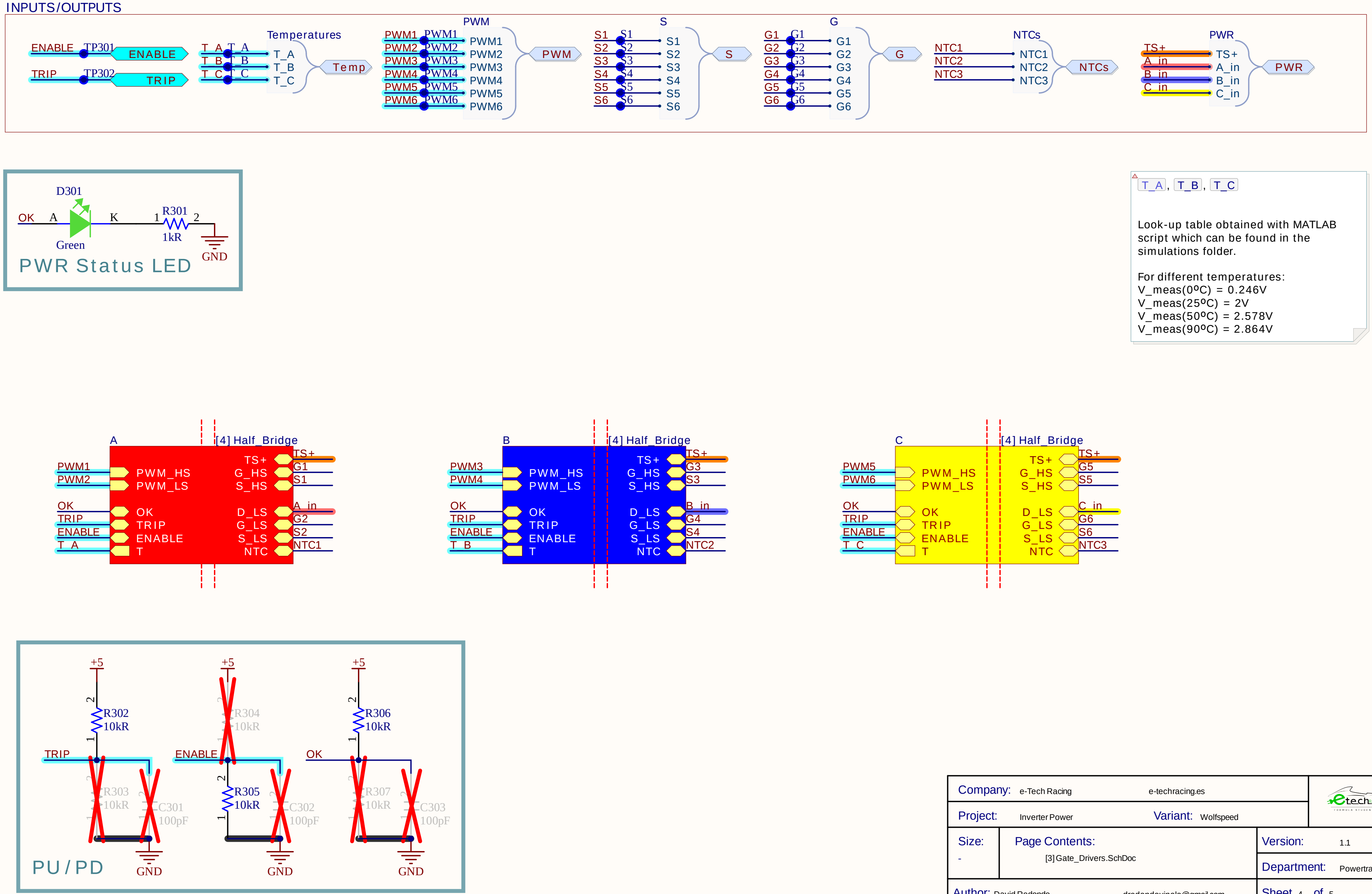
The fluxgate oscillator draws current pulses of up to 30 mA at a rate of ca. 900 kHz. In the case of a power supply with high impedance, it is advised to provide local decoupling (100 nF or more, located close to the transducer).

CSA , CSB , CSC

AC insulation test
RMS voltage, 50 Hz, 1 min:

Ud = 4.3 kV > 3*V_max = 1.8 kV

Company: e-Tech Racing	e-techracing.es		
Project: Inverter Power	Variant: Wolfspeed		
Size: -	Page Contents: [2] Current_Sense.SchDoc	Version: 1.1	
		Department: Powertrain	
Author: David Redondo	dredondovinolo@gmail.com	Sheet 3 of 5	
Checked by: _		Date: 29/05/2024	



Company: e-Tech Racing	e-techracing.es		
Project: Inverter Power	Variant: Wolfspeed		
Size: -	Page Contents: [3] Gate_Drivers.SchDoc	Version: 1.1	Department: Powertrain
Author: David Redondo	dredondovinolo@gmail.com	Sheet 4 of 5	
Checked by: _		Date: 29/05/2024	

U_HS, U_LS

1. TRIP and OK signals are in open drain configuration, so they can be paralleled.
2. IN- is not used and tied to GND.
3. ENABLE to be given by MCU in active-high mode. When set to low for more than 1 µs, TRIP is reset.
4. Temperature sensing using low-side drivers. Ain outputs a current of 200 µA. PWM to analog using a RC filter, to be fed directly to MCU ADC. R405, R406 and C411 from SPICE simulation.
5. Miller clamp protection is used.
6. RGS_HS, RGS_LS: External gate pull-down is implemented even though the gate drivers implement an active pull-down.
7. Overcurrent detection is not implemented.

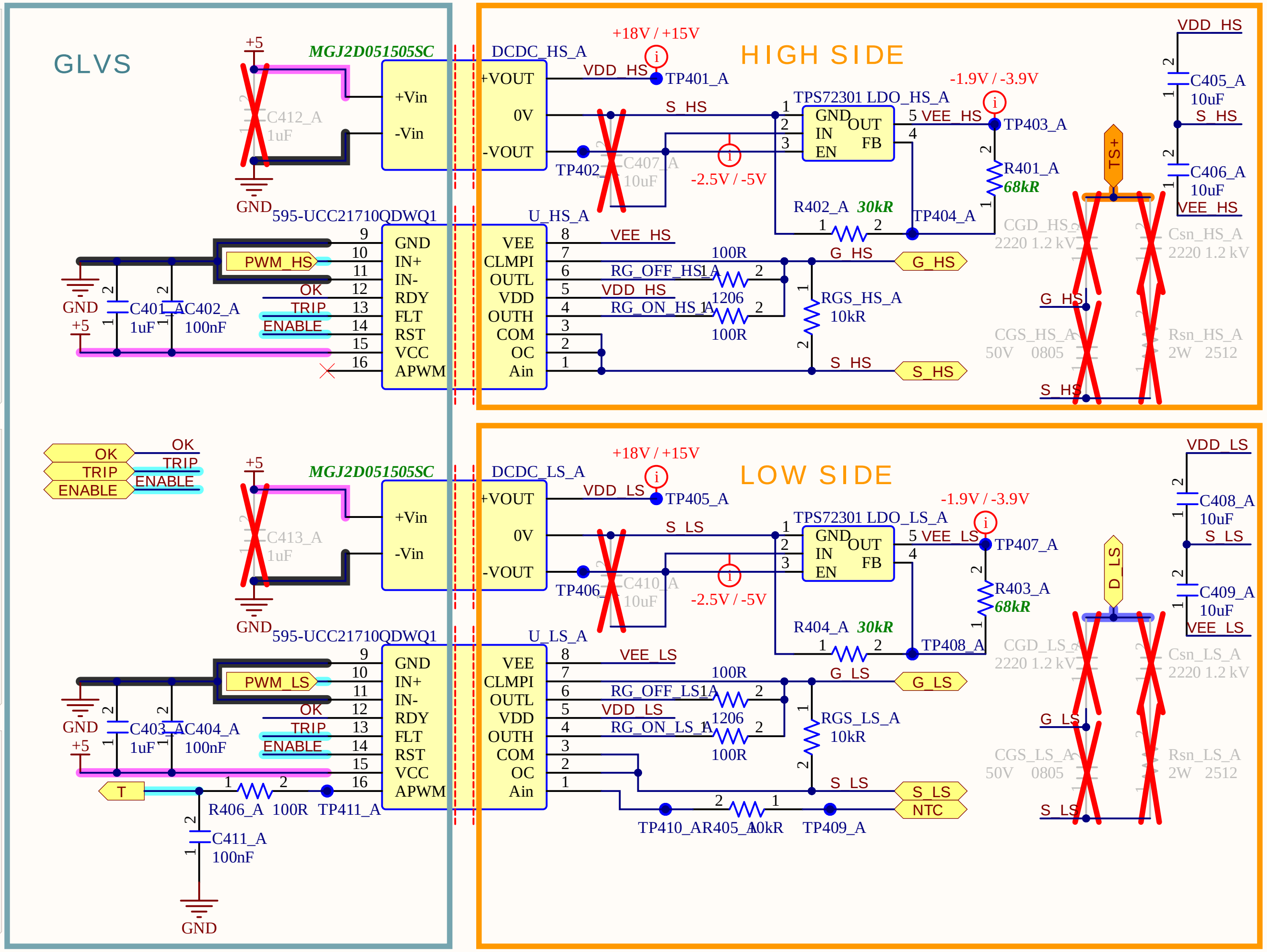
LDO_HS, LDO_LS

An LDO is implemented to trim VEE_HS_A and VEE_LS_A during testing to fine tune the necessary negative gate voltage. Feedback voltage divider adjusted with a Python script which can be found in the simulations folder.

VEE = - 1.186 · (1 + R1/R2)
R1 + R2 ≈ 100 kΩ
Leapers → R1 = 36 kΩ, R2 = 56 kΩ
Wolfspeed → R1 = 68 kΩ, R2 = 30 kΩ

DCDC_HS, DCDC_LS
Isolation test voltage (Qualification tested for 1 minute): 5200 VDC

U_HS, U_LS
VIOTM (t = 60 s (qualification test)): 8000 VPK



V_GS values:

The values can be modified by replacing DCDC_HS and DCDC_LS with one from the following list: MGJ2D051505SC, MGJ2D051509SC, MGJ2D051515SC, MGJ2D051802SC, MGJ2D052003SC, MGJ2D052005SC. LDO voltages must also be adjusted.

Minimum gate driver current and power:
I_GD(min) = f_sw · Q_G = 40 kHz · 520 nC = 20.8 mA
P_min = ΔV_GS · I_GD(min) = 20 V · 20.8 mA = 0.416 W → 2 W

RG_ON_HS, RG_OFF_HS, RG_ON_LS, RG_OFF_LS

Essentially, a lower value for the gate resistors will reduce switching losses as the MOSFETs will switch faster and thus spend less time switching. Switching faster also means that the dV/dt will be higher, which can be responsible of EMI increase. The considered values of 3.3 Ω are recommended by the datasheet.

CGS_HS, CGS_LS, CGD_HS, CGD_LS, Csn_HS, Csn_LS, Rsn_HS, Rsn_LS

DNP, but they could be useful with EMI related issues to decrease dV/dt. Implementing them could result in further issues with the power limit for DCDC_HS and DCDC_LS, as the gate charge would increase significantly. The maximum allowed capacitance would be:

CGS_max = 2 · P_DCDC / (ΔV_GS ^2 · f_sw) = 2 · 2 W / ((20 V)^2) · 40 kHz) = 250 nF

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Project: Inverter Power	Variant: Wolfspeed		
Size: -	Page Contents: [4] Half_Bridge.SchDoc	Version: 1.1	
		Department: Powertrain	
Author: David Redondo	dredondovinolo@gmail.com	Sheet 5 of 5	
Checked by: _		Date: 29/05/2024	

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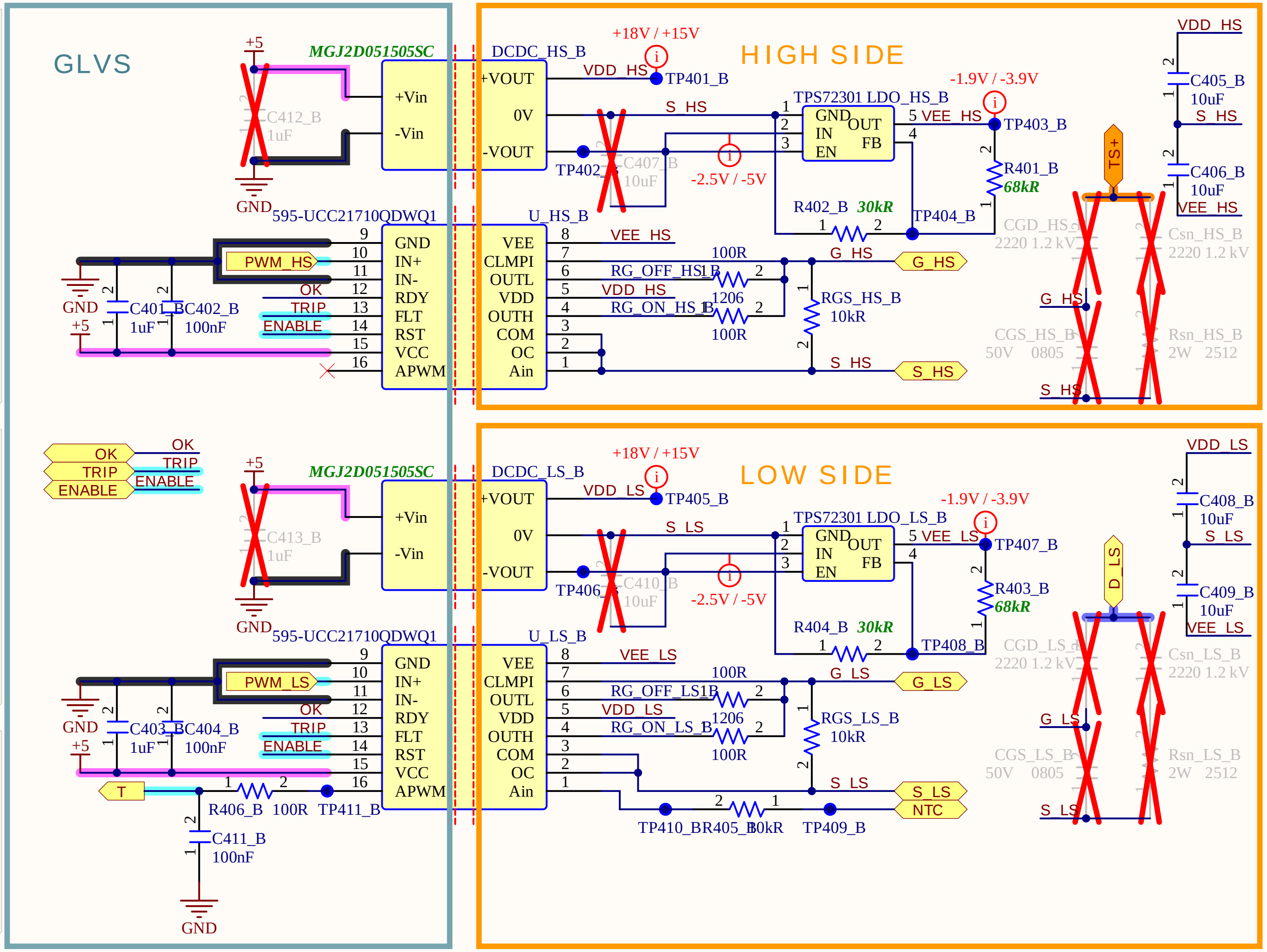
U_HS, U_LS
VIOTM (t = 60 s (qualification test)): 8000 VPK



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Project: Inverter Power	Variant: Wolfspeed		
Size: -	Page Contents: [4] Half_Bridge.SchDoc	Version: 1.1	
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Author: David Redondo	dredondovinolo@gmail.com	Sheet 5 of 5	
Checked by: _		Date: 29/05/2024	

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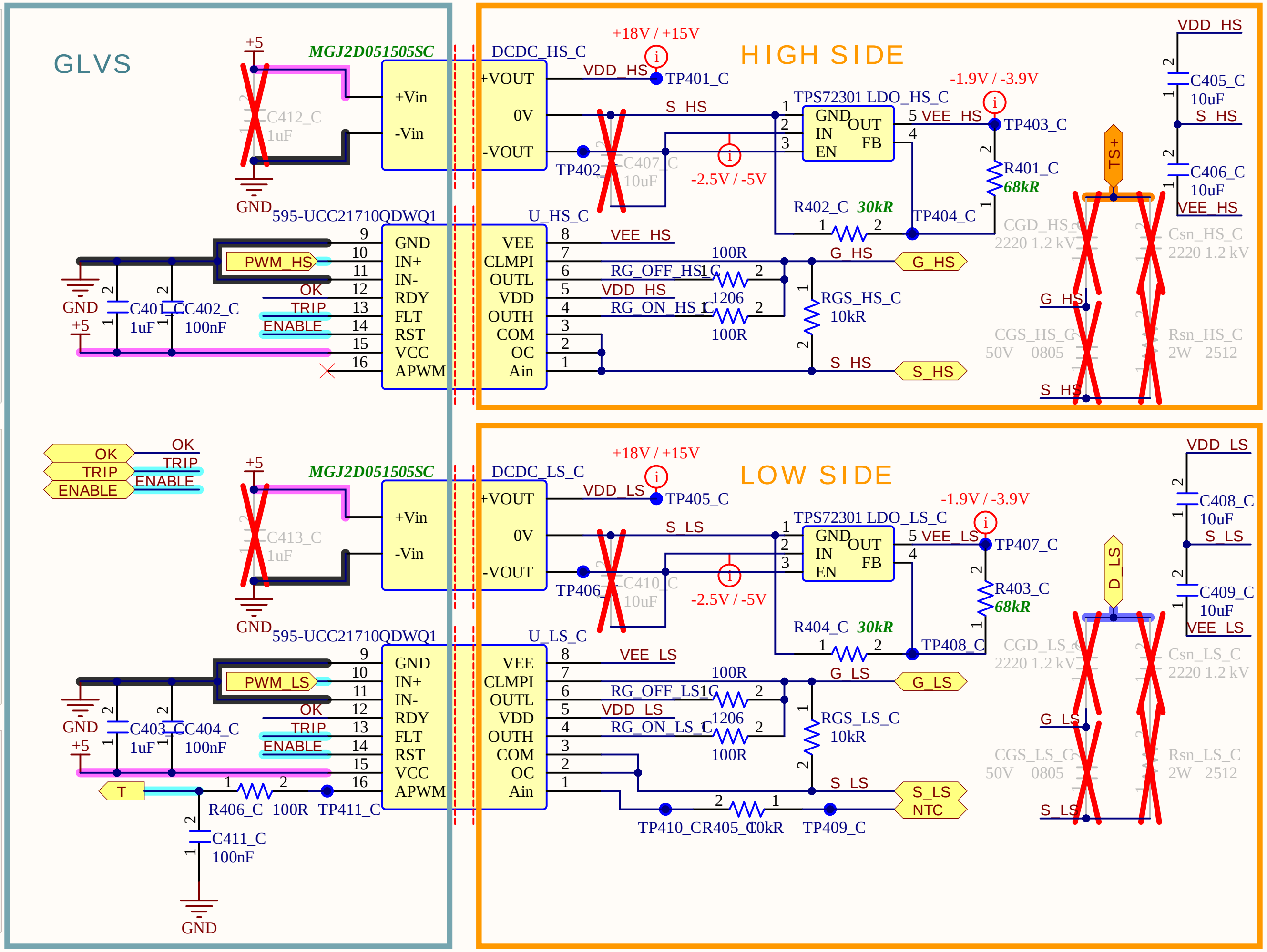

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Size: -	Page Contents: [4] Half_Bridge.SchDoc	Version: 1.1	Department: Powertrain
Author: David Redondo	dredondovinolo@gmail.com	Sheet 5 of 5	
Checked by: _		Date: 29/05/2024	

Discharge resistors:

$t_{dis} = R_{dis} \cdot C \cdot \ln(V_{initial}/V_{final}) = (470\ k\Omega / 24) \cdot (100\ \mu F) \cdot \ln(600\ V / 60\ V) = 4.509\ s$

$P(R_{dis,max}) = V_{max}^2 / R_{dis} = 600\ V^2 / 470\ k\Omega = 0.766\ W < 1\ W$

$\Delta T \sim 110^{o}C/W \cdot 0.766\ W = 85\ ^{o}C$

$I_{dis,max} = 600\ V / (470\ k\Omega / 24) = 30.64\ mA$

U503

Single supply configuration as per datasheet.

Maximum differential input voltage = 6.833 V - 677 mV = 6.156 V < 30 V

$VDC\_div = (TS+ - TS-) \cdot 4.7\ k\Omega / (4.7\ k\Omega + 6 \cdot 68\ k\Omega)$

$600\ V \cdot 4.7\ k\Omega / (4.7\ k\Omega + 6 \cdot 68\ k\Omega) = 6.833\ V$

$60\ V \cdot 4.7\ k\Omega / (4.7\ k\Omega + 6 \cdot 68\ k\Omega) = 683\ mV$

$P_{R4} = I_{R4}^2 \cdot R4 = ((600\ V / (4.7\ k\Omega + 6 \cdot 68\ k\Omega)) / 68\ k\Omega)^2 \cdot 68\ k\Omega = 144\ mW \rightarrow$ 1206 package

$V\_TSAL = 5\ V \cdot 4.7\ k\Omega / (4.7\ k\Omega + 30\ k\Omega) = 677\ mV \equiv 59.46\ V$ in TS+ - TS-

R501

For U501 , the recommended diode forward current is 10 mA. SC_END can be between 20 V and 30 V.

$I_{min} = 20\ V / 2.2\ k\Omega = 9.1\ mA$

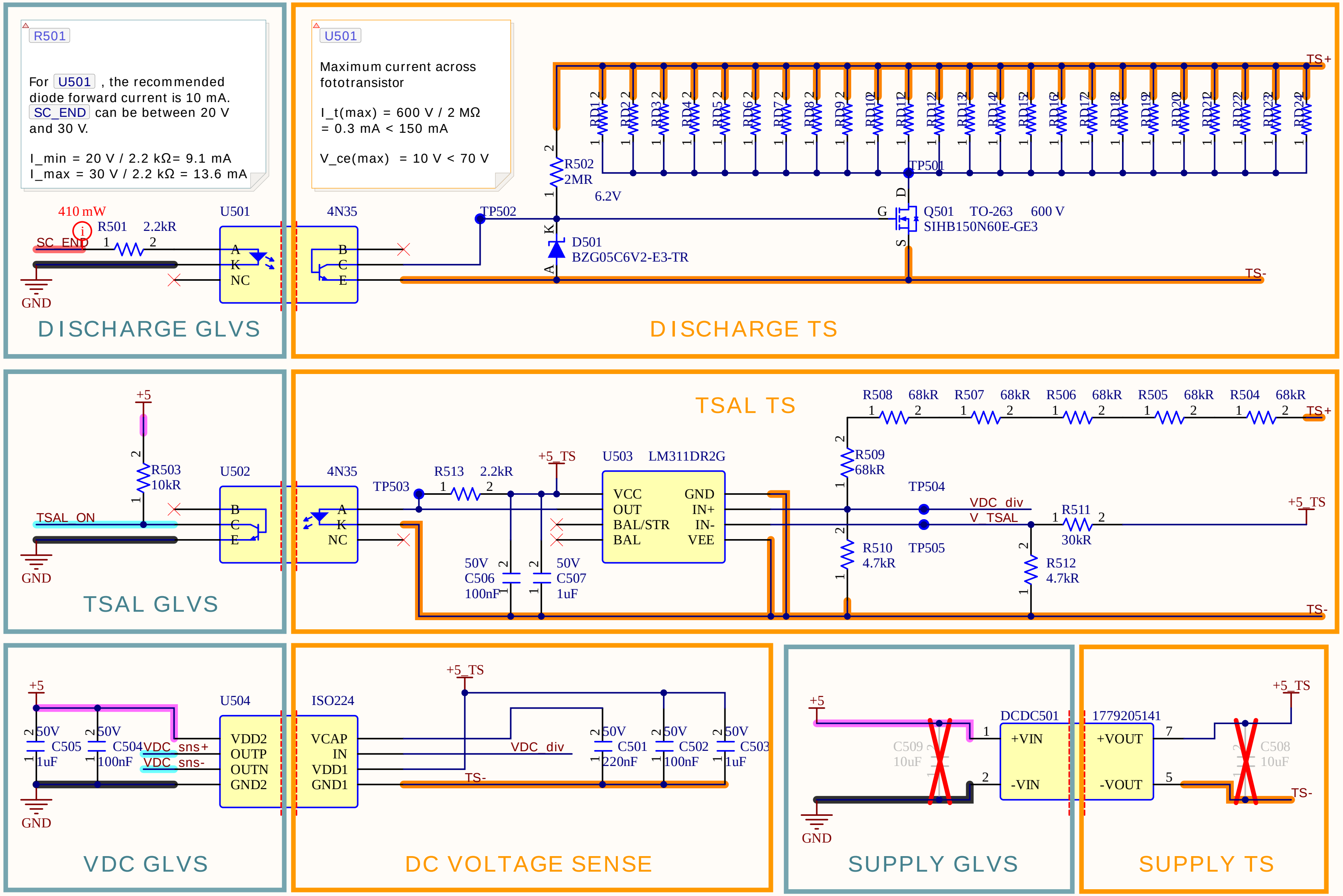
$I_{max} = 30\ V / 2.2\ k\Omega = 13.6\ mA$

U501

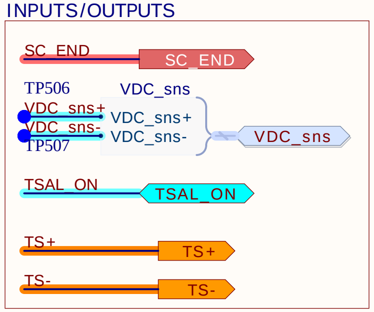
Maximum current across fototransistor

$I_{t(max)} = 600\ V / 2\ M\Omega = 0.3\ mA < 150\ mA$

$V_{ce(max)} = 10\ V < 70\ V$



INPUTS/OUTPUTS



$(TS+ - TS-) > 60V \rightarrow TSAL\_ON = 0V$

$(TS+ - TS-) < 60V \rightarrow TSAL\_ON = 5V$

U504

$(VDC\_sns+ - VDC\_sns-) = 1/3 \cdot VDC\_div = 1/3 \cdot ((TS+ - TS-) \cdot 4.7\ k\Omega / (4.7\ k\Omega + 6 \cdot 68\ k\Omega)) = 1/3 \cdot 0.011388 \cdot (TS+ - TS-)$

$(VDC\_sns+ - VDC\_sns-) = 1/3 \cdot 0.011388 \cdot 600\ V = 2.278\ V$

U501 , U502

Isolation Voltage: AC For 1 Minute, R.H. = 40 ~ 60% Viso = 5000 Vrms

U504

Maximum transient isolation voltage: VTEST = VIOTM, t = 60 s (qualification test) VIOTM = 7071 Vpk

DCDC501

Isolation voltage input to output, tested 100% for 60s(2) VISO = 3000 V

Company: e-Tech Racing	e-techracing.es		
Project: Inverter Power	Variant: Wolfspeed		
Size: -	Page Contents: [5] DC.SchDoc	Version: 1.1	Department: Powertrain
Author: David Redondo	dredondovinolo@gmail.com	Sheet * of *	
Checked by: _		Date: 29/05/2024	


ID:
Variant:
A
B
C
REV 1.1 - MARCH 2024
David Redondo
LV
TS
GND GND
+5V +5V
TSAL VDC+
SC VDC-
AUX1 AUX2
PWM6 PWM5
PWM4 PWM3
PWM2 PWM1
I_C TRIP
I_A I_B
T_C ENA
T_A T_B
GND GND
MPA
MPB
MPC
CSA
CSB
CSC
HB_A
HB_B
HB_C
DIN912
M2.5x08
0.4 N·m
DIN912
M4x06
2 N·m
DIN912 M4x16
DIN980 M4
DIN125 M4
Warning
High voltage
Warning
High temperatures
Rdis

A
B
C
ID:
Variant:
LV
TS
GND GND
+5V +5V
TSAL VDC+
SC VDC-
AUX1 AUX2
PWM6 PWM5
PWM4 PWM3
PWM2 PWM1
I_C TRIP
I_A I_B
T_C ENA
T_A T_B
GND GND
MPA
MPB
MPC
CSA
CSB
CSC
HB_A
HB_B
HB_C
VDD VEE1
VEE2
S1
S2
S3
S4
S5
S6
G1
G2
G3
G4
G5
G6
DIN912
M2.5x08
0.4 N·m
DIN912
M4x06
2 N·m
DIN912 M4x16
DIN980 M4
DIN125 M4
Warning
High voltage
Warning
High temperatures
DC501
David Redondo
Layers

A
B
C
ID:
Variant:
LV
TS
GND GND
+5V +5V
TSAL VDC+
SC VDC-
AUX1 AUX2
PWM6 PWM5
PWM4 PWM3
PWM2 PWM1
I_C TRIP
I_A I_B
T_C ENA
T_A T_B
GND GND
Warning
High voltage
Warning
High temperatures
DIN912
M2.5x08
0.4 N·m
DIN912
M4x06
2 N·m
DIN912 M4x16
DIN980 M4
DIN125 M4
Layers
David Redondo


A
B
C
ID:
Variant:
GND GND
+5V +5V
TSAL VDC+
SC VDC-
AUX1 AUX2
PWM6 PWM5
PWM4 PWM3
PWM2 PWM1
I_C TRIP
I_A I_B
T_C ENA
T_A T_B
GND GND
LV
TS
MPA
MPB
MPC
HB_A
HB_B
HB_C
DIN912
M2.5x08
0.4 N·m
DIN912
M4x06
2 N·m
DIN912 M4x16
DIN980 M4
DIN125 M4
Warning
High voltage
Warning
High temperatures
DC501
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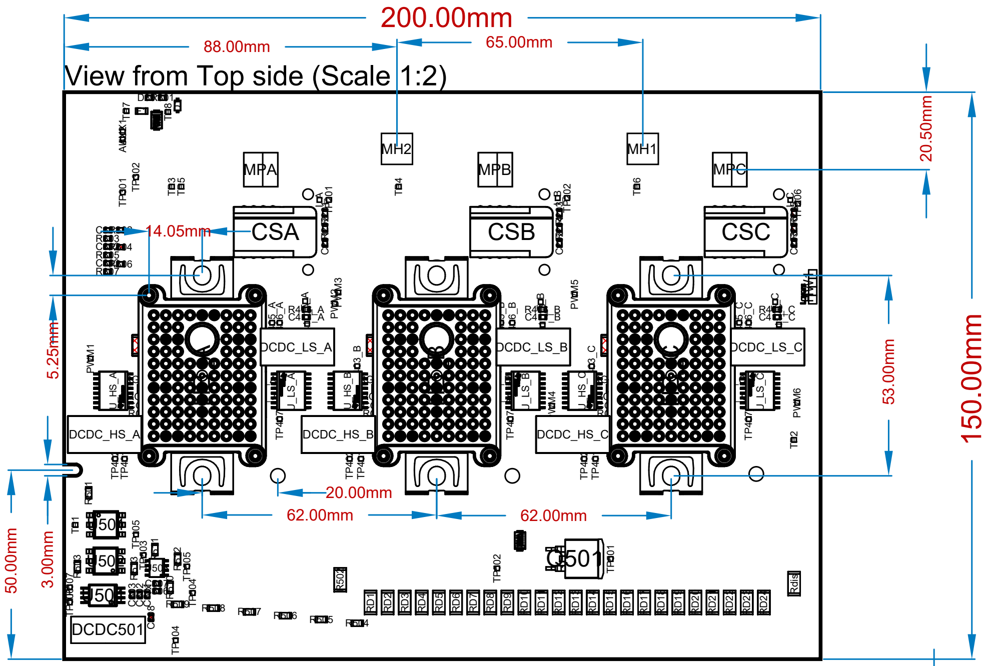
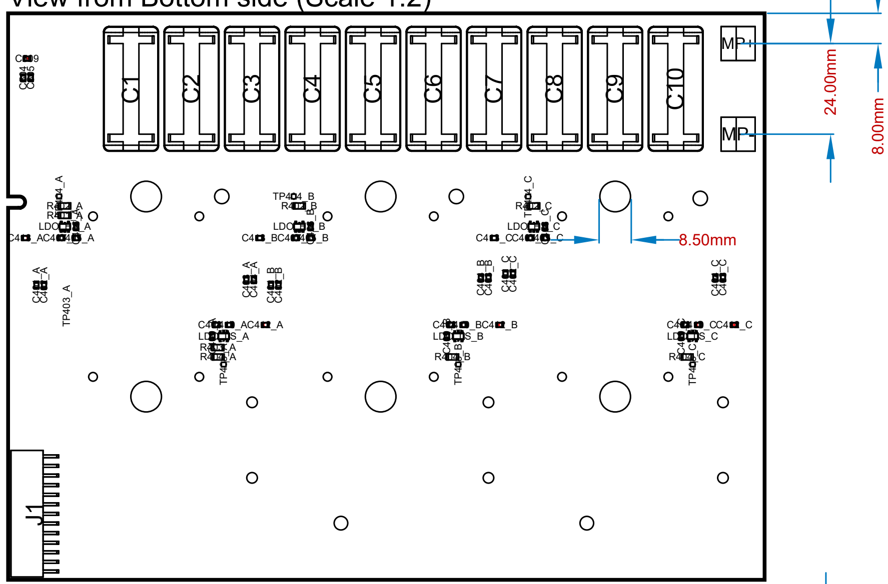
Redondo
Layers

Inverter Power

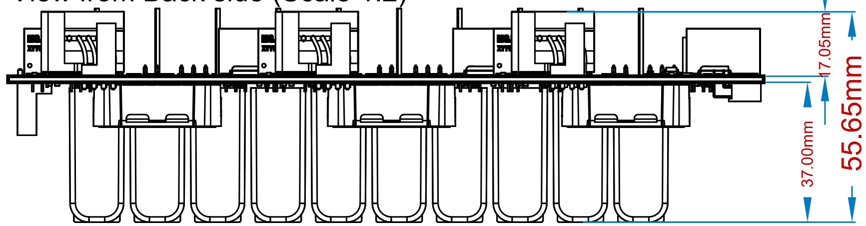
View from Top side (Scale 1:2)



View from Bottom side (Scale 1:2)



View from Back side (Scale 1:2)

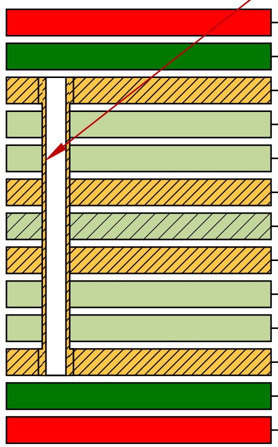


Bill Of Materials

Designator	Name	Quantity
C405_A, C405_B, C405_C, C406_A, C406_B, C406_C, C408_A, C408_B, C408_C, C409_A, C409_B, C409_C	10uF	12
C1, C2, C3, C4, C5, C6, C7, C8, C9, C10	10uF 850V	10
CA1, CA2, CB1, CB2, CC1, CC2	2220Y1K00104KZT	6
F1	0437001.WRA	1
DCDC501	1779205141	1
J1	613026243121	1
D2	BZG05C5V1-E3-TR	1
HB_A, HB_B, HB_C	CAB016M12FM3	3
R402_A, R402_B, R402_C, R404_A, R404_B, R404_C	CR1206-JW-303ELF	6
R401_A, R401_B, R401_C, R403_A, R403_B, R403_C	CR1206-JW-683ELF	6
R503	CRCW120610K0FKEA	1
R511	CRCW120630K0FKEA	1
HW1	LOGO CAPAS (4)	1
MP-, MP+, MPA, MPB, MPC	M4	5
D1	MBR0530	1
DCDC_HS_A, DCDC_HS_B, DCDC_HS_C, DCDC_LS_A, DCDC_LS_B, DCDC_LS_C	MGJ6-series	6
MH1, MH2	Mounting_Hole_M4	2
RD1, RD2, RD3, RD4, RD5, RD6, RD7, RD8, RD9, RD10, RD11, RD12, RD13, RD14, RD15, RD16, RD17, RD18, RD19, RD20, RD21, RD22, RD23, RD24	RCV2512470KFKEG	24
R406_A, R406_B, R406_C	CR0805-FX-1000ELF	3
R301	CR0805-JW-102ELF	1
R302, R305, R306, R405_A, R405_B, R405_C, RGS_HS_A, RGS_HS_B, RGS_HS_C, RGS_LS_A, RGS_LS_B, RGS_LS_C	CR0805-JW-103ELF	12
R504, R505, R506, R507, R508, R509	CR1206AFX-6802EAS	6
R501, R513	CR1206-FX-2201ELF	2
R510, R512	CRS1206-FX-4701ELF	2
CSA, CSB, CSC	LEM CKSR 50-NP	3
U503	LM311DR2G	1
C501	885012208058	1
RG_OFF_HS_A, RG_OFF_HS_B, RG_OFF_HS_C, RG_OFF_LS_A, RG_OFF_LS_B, RG_OFF_LS_C, RG_ON_HS_A, RG_ON_HS_B, RG_ON_HS_C, RG_ON_LS_A, RG_ON_LS_B, RG_ON_LS_C	CRG1206F100R	12
U504	ISO224	1
LDO_HS_A, LDO_HS_B, LDO_HS_C, LDO_LS_A, LDO_LS_B, LDO_LS_C	TPS72301	6
U_HS_A, U_HS_B, U_HS_C, U_LS_A, U_LS_B, U_LS_C	UCC21710	6
Q501	SIHB150N60E-GE3	1
R502, Rdis	R2M-2512FTK	2
U501, U502	4N35	2
D501	BZG05C6V2-E3-TR	1
D301	150080GS75000	1
C201, C202, C203, C402_A, C402_B, C402_C, C404_A, C404_B, C404_C, C411_A, C411_B, C411_C, C502, C504, C506	885012207098	15
C401_A, C401_B, C401_C, C403_A, C403_B, C403_C, C503, C505, C507	885012207103	9

Copper thickness in hole 25-50um, watch out for 1.10mm holes
Chemical tin 1-15um

Layer Stack Legend



Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay			Legend	GTO
Surface Material	Top Solder	0.01mm	Solder Resist	Solder Mask	GTS
CF-004	**TOP**	**0.07mm**		**Signal**	**GTL**
Prepreg		*0.10mm*	*PP-006*	*Dielectric*	
Prepreg		*0.10mm*	*PP-006*	*Dielectric*	
Copper	**GND**	**0.07mm**		**Signal**	**G1**
		0.90mm	*FR-4*	*Dielectric*	
Copper	**PWR**	**0.07mm**		**Signal**	**G2**
Prepreg		*0.10mm*	*PP-006*	*Dielectric*	
Prepreg		*0.10mm*	*PP-006*	*Dielectric*	
CF-004	**BOT**	**0.07mm**		**Signal**	**GBL**
Surface Material	Bottom Solder	0.01mm	Solder Resist	Solder Mask	GBS
	Bottom Overlay			Legend	GBO

Total thickness: 1.60mm