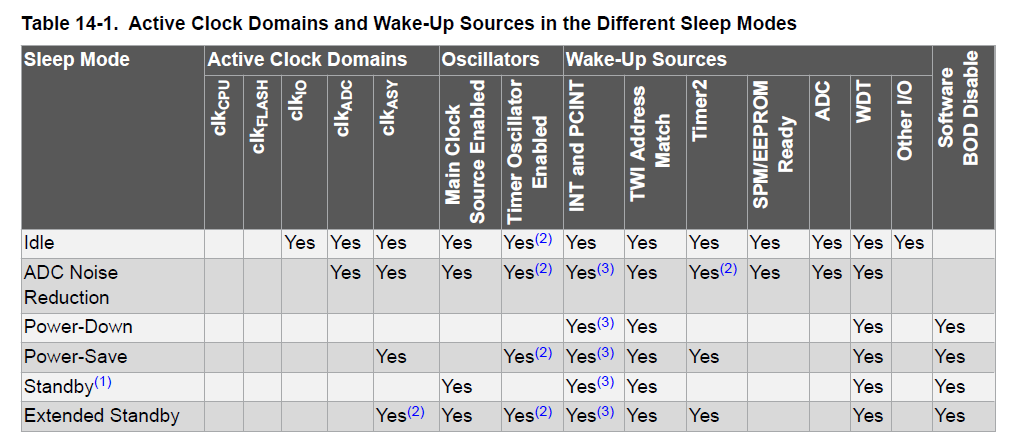
LPM in Atmega328p



1. IDLE mode (SM[2:0] bits are written to '000')

his Sleep mode basically halts clkCPU and clkFLASH, while allowing the other clocks to run.

2. **ADC Noise Reduction Mode (SM[2:0] bits are written to '001')**

This sleep mode basically halts clkI/O, clkCPU, and clkFLASH, while allowing the other clocks to run.

Wake up sources

• External Reset

• Watchdog System Reset

• Watchdog Interrupt

• Brown-out Reset

• Two-wire Serial Interface Address Match

• Timer/Counter Interrupt

• SPM/EEPROM Ready Interrupt

• External Level Interrupt on INT

• Pin Change Interrupt

3. **Power-Down Mode (SM[2:0]=010)**

The external oscillator is stopped, This sleep mode basically halts all generated clocks, allowing operation of asynchronous modules only.

4. **Power-Save Mode (SM[2:0]=011)**

Same as power down **EXCEPT:** If timer/counter2 is enabled, it will keep running during sleep. The device can wake-up from either timer overflow or output compare event from timer/counter2 if the corresponding timer/counter2 interrupt enable bits are set in TIMSK2, and the global interrupt enable bit in SREG is set.

5. **Standby mode (SM[2:0]=110)**

This mode is identical to the Power-Down mode with the exception that the oscillator is kept running. From Standby mode, the device wakes up in six clock cycles.

6. **Extended** **Standby mode (SM[2:0]=111)**

This mode is identical to Power-Save mode with the exception that the oscillator is kept running. From Extended Standby mode, the device wakes up in six clock cycles.

**Watchdog timer :**

**Features**

**• Clocked from Separate On-chip Oscillator**

**• Three Operating modes:**

**– Interrupt**

**– System Reset**

**– Interrupt and System Reset**

**• Selectable Time-out Period from 16 ms to 8s**

**• Possible Hardware Fuse Watchdog Always ON (WDTON) for Fail-safe mode**