



eYs3D

Flash Protection APN

FW Div.

V2.0
20210906

Version.	Date	Description
V1.0	20210824	• Initial release
V2.0	20210906	• Create user file id as the shadow of factory file id, p.19 • Add file id 201 as a backup of UNP, p.20

1. Flash type we use is MX25R series
 - a. MX25R2035F, 2M bits (256K Bytes)
 - b. MX25R4035F, 4M bits (512K Bytes)
 - c. MX25R8035F, 8M bits (1M Bytes)
2. Flash protection is block base. Each block is **64KB**.
3. Flash protection scheme is separated as program data and user data.
 - a. Program data and protected parameters need to be protected by flash chip level.
 - b. User data is unprotected.
4. Flash protection blocks must start at lowest address and the size must be able to store all protected data, item 2.a. (See p.9)
5. $BP_{3\sim0}$ is protection bits in flash. BP stands for Block Protection. There are 4 bits for this setting. $BP_{3\sim0}$ determines protection blocks (See pp.10 - 12).
6. Numbers of protection blocks, $N = BPX > 0 ? 2^{BPX-1} : 0$, $BPX = BP_{3\sim0}$, ($N = 0, 1, 2, 4, 8, \dots$), $N \leq \text{Total blocks}$

1. TB bit sets protection block from top to bottom or bottom to top.

Protected Area Sizes (TB bit = 0)

Status bit				Protect Level
BP3	BP2	BP1	BP0	
0	0	0	0	0 (none)
0	0	0	1	1 (1block, block 3rd)
0	0	1	0	2 (2blocks, block 2nd~3rd)
0	0	1	1	3 (4blocks, protect all)
0	1	0	0	4 (4blocks, protect all)
0	1	0	1	5 (4blocks, protect all)
0	1	1	0	6 (4blocks, protect all)
0	1	1	1	7 (4blocks, protect all)
1	0	0	0	8 (4blocks, protect all)
1	0	0	1	9 (4blocks, protect all)
1	0	1	0	10 (4blocks, protect all)
1	0	1	1	11 (4blocks, protect all)
1	1	0	0	12 (4blocks, protect all)
1	1	0	1	13 (4blocks, protect all)
1	1	1	0	14 (4blocks, protect all)
1	1	1	1	15 (4blocks, protect all)

High

Low

Protected Area Sizes (TB bit = 1)

Status bit				Protect Level
BP3	BP2	BP1	BP0	
0	0	0	0	0 (none)
0	0	0	1	1 (1block, block 0th)
0	0	1	0	2 (2blocks, block 0th~1st)
0	0	1	1	3 (4blocks, protect all)
0	1	0	0	4 (4blocks, protect all)
0	1	0	1	5 (4blocks, protect all)
0	1	1	0	6 (4blocks, protect all)
0	1	1	1	7 (4blocks, protect all)
1	0	0	0	8 (4blocks, protect all)
1	0	0	1	9 (4blocks, protect all)
1	0	1	0	10 (4blocks, protect all)
1	0	1	1	11 (4blocks, protect all)
1	1	0	0	12 (4blocks, protect all)
1	1	0	1	13 (4blocks, protect all)
1	1	1	0	14 (4blocks, protect all)
1	1	1	1	15 (4blocks, protect all)

Low

High

- To meet the criteria, MX25R2035F (2Mb/256KB), can be configured as lower 2 blocks (0th ~ 1st /128KB) are protected, higher 2 blocks (2nd ~ 3rd /128KB) are unprotected.

Protected Area Sizes (TB bit = 1)

Status bit				Protect Level
BP3	BP2	BP1	BP0	
0	0	0	0	0 (none)
0	0	0	1	1 (1block, block 0th)
0	0	1	0	2 (2blocks, block 0th-1st)
0	0	1	1	3 (4blocks, protect all)
0	1	0	0	4 (4blocks, protect all)
0	1	0	1	5 (4blocks, protect all)
0	1	1	0	6 (4blocks, protect all)
0	1	1	1	7 (4blocks, protect all)
1	0	0	0	8 (4blocks, protect all)
1	0	0	1	9 (4blocks, protect all)
1	0	1	0	10 (4blocks, protect all)
1	0	1	1	11 (4blocks, protect all)
1	1	0	0	12 (4blocks, protect all)
1	1	0	1	13 (4blocks, protect all)
1	1	1	0	14 (4blocks, protect all)
1	1	1	1	15 (4blocks, protect all)

2. If 128KB protected size is not enough, it can upgrade to 4Mb, MX25R4035F (4Mb/512KB). This part number can be configured as lower 4 blocks (0th ~ 3rd /256KB) are protected, higher 4 blocks (4th ~ 7th /256KB) are unprotected.

Protected Area Sizes (TB bit = 1)

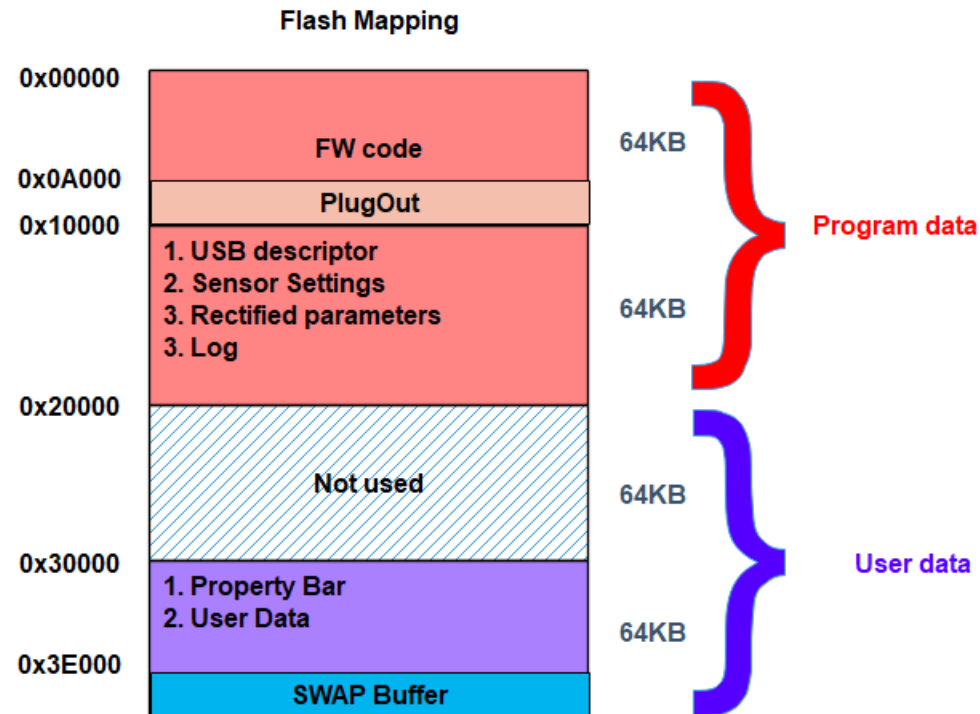
Status bit				Protect Level
BP3	BP2	BP1	BP0	
0	0	0	0	0 (none)
0	0	0	1	1 (1block, block 0th)
0	0	1	0	2 (2blocks, block 0th-1st)
0	0	1	1	3 (4blocks, block 0th-3th)
0	1	0	0	4 (8blocks, protect all)
0	1	0	1	5 (8blocks, protect all)
0	1	1	0	6 (8blocks, protect all)
0	1	1	1	7 (8blocks, protect all)
1	0	0	0	8 (8blocks, protect all)
1	0	0	1	9 (8blocks, protect all)
1	0	1	0	10 (8blocks, protect all)
1	0	1	1	11 (8blocks, protect all)
1	1	0	0	12 (8blocks, protect all)
1	1	0	1	13 (8blocks, protect all)
1	1	1	0	14 (8blocks, protect all)
1	1	1	1	15 (8blocks, protect all)

3. This is 8Mb(1MB), MX25R8035F, configuration.

Protected Area Sizes (TB bit = 1)

Status bit				Protect Level
BP3	BP2	BP1	BP0	8Mb
0	0	0	0	0 (none)
0	0	0	1	1 (1block, block 0th)
0	0	1	0	2 (2blocks, block 0th-1st)
0	0	1	1	3 (4blocks, block 0th-3rd)
0	1	0	0	4 (8blocks, block 0th-7th)
0	1	0	1	5 (16blocks, protect all)
0	1	1	0	6 (16blocks, protect all)
0	1	1	1	7 (16blocks, protect all)
1	0	0	0	8 (16blocks, protect all)
1	0	0	1	9 (16blocks, protect all)
1	0	1	0	10 (16blocks, protect all)
1	0	1	1	11 (16blocks, protect all)
1	1	0	0	12 (16blocks, protect all)
1	1	0	1	13 (16blocks, protect all)
1	1	1	0	14 (16blocks, protect all)
1	1	1	1	15 (16blocks, protect all)

1. Protected parameters:
 1. File table structure
 2. Sensor settings
 3. USB description table
 4. Y-offset (file id 3x)
 5. Rectify table (file id 4x)
 6. ZD Table (file 5x)
 7. Log file (file 24x)
2. Property bar locates at unprotected lock area.



Status Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRWD (status register write protect)	QE (Quad Enable)	BP3 (level of protected block)	BP2 (level of protected block)	BP1 (level of protected block)	BP0 (level of protected block)	WEL (write enable latch)	WIP (write in progress bit)
1=status register write disable	1=Quad Enable 0=not Quad Enable	(note 1)	(note 1)	(note 1)	(note 1)	1=write enable 0=not write enable	1=write operation 0=not in write operation
Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

1. Check BP status by CapW:
 1. Set ASIC type
 2. Use Batch Write to load script file, RD_Flash_STS_(SPI_RDSR_CMD).txt, to read status register
 3. Set the address to 0xF0A6 to read the content
 1. [0xF0A6] = 0x88 >> BPX = 0010.
2. Refer to slide: Improvement 2/6, Improvement 3/6
3. Note: It needs to reload script file to read the register again

Etron [New] WebCam Extension Un... □ ×

☒ ASIC ☐ ISP ☐ FW ☐ I2C ☐ EI2C

1 ID: 0x76 ☒ SensorA ☐ SensorB ☐ SensorBoth

☒ Addr2Byte ☐ Value2Byte Read HW All

Sensor Addr From 0x0000 To 0x00ff Read Sensor All

3 ☐ SlaveIC Addr Mode ☒ Hex ☒ Auto Read

Address: 0xf0a6 Read Batch Read

Value: 0x0088 Write Batch Write

Small 7 6 5 4 3 2 1 0 15 14 13 12 11 10 9 8

Batch 2 10 ms

Write Command History:

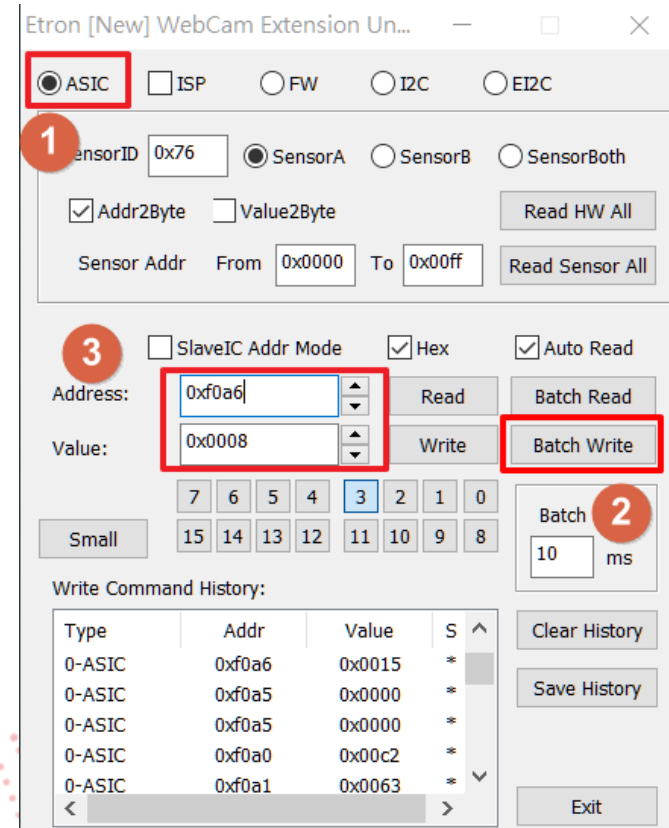
Type	Addr	Value	S
0-ASIC	0xf0a6	0x0005	*
0-ASIC	0xf0a5	0x0000	*
0-ASIC	0xf0a5	0x0000	*
0-ASIC	0xf0a0	0x00c2	*
0-ASIC	0xf0a1	0x0063	*

Clear History Save History Exit

Configuration Register - 1

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Reserved	DC (Dummy Cycle)	Reserved	Reserved	TB (top/bottom selected)	Reserved	Reserved	Reserved
x	2READ/4READ Dummy Cycle	x	x	0=Top area protect 1=Bottom area protect (Default=0)	x	x	x
x	Volatile bit	x	x	OTP	x	x	x

1. Check Top/Bottom setting by CapW
 1. Set ASIC type
 2. Use Batch Write to load script file, RD_Flash_Configuration_(SPI_RDCR_CMD).txt, to read configuration register
 3. Set the address to 0xF0A6 to read the content
 1. [0xF0A6] = 0x08 >> bottom area
2. Refer to slide: Improvement 2/6, Improvement 3/6
3. Note: It needs to reload script file to read the register again



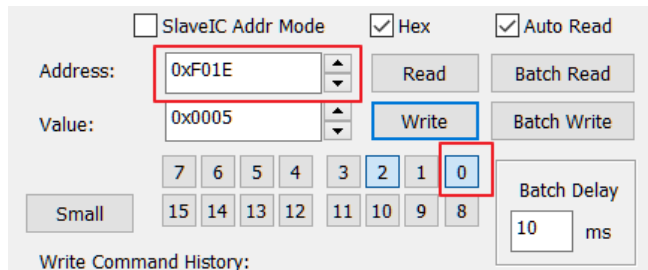
The screenshot shows the Etron [New] WebCam Extension Un... software interface. The following steps are highlighted with red boxes and numbers:

- 1**: Select **ASIC** as the device type.
- 2**: Set the **Batch** time to **10 ms**.
- 3**: Set the **Address** to **0xf0a6** and the **Value** to **0x0008**. The **Batch Write** button is also highlighted.

The interface includes fields for SensorID (0x76), Sensor selection (SensorA, SensorB, SensorBoth), Addr2Byte/Value2Byte checkboxes, Sensor Addr range (From 0x0000 To 0x00ff), and a Write Command History table.

Type	Addr	Value	S
0-ASIC	0xf0a6	0x0015	*
0-ASIC	0xf0a5	0x0000	*
0-ASIC	0xf0a5	0x0000	*
0-ASIC	0xf0a0	0x00c2	*
0-ASIC	0xf0a1	0x0063	*

1. Do the following steps to unprotect flash
 1. Set GPIO23 from UART RX to GPIO mode
 1. Set bit 0 of 0xF01E to 1



SlaveIC Addr Mode ☐ Hex ☒ Auto Read ☒

Address: 0xF01E Read Batch Read

Value: 0x0005 Write Batch Write

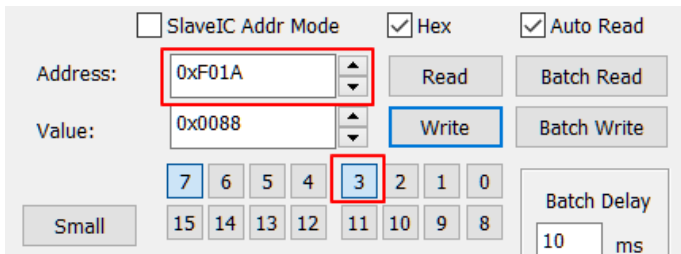
7 6 5 4 3 2 1 0

Small 15 14 13 12 11 10 9 8

Batch Delay 10 ms

Write Command History:

2. Set GPIO23 as output
 1. Set bit 3 of 0xF01A to 1
 2. Set bit 3 of 0xF019 to 1



SlaveIC Addr Mode ☐ Hex ☒ Auto Read ☒

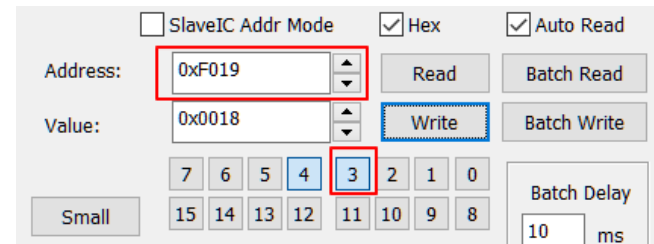
Address: 0xF01A Read Batch Read

Value: 0x0088 Write Batch Write

7 6 5 4 3 2 1 0

Small 15 14 13 12 11 10 9 8

Batch Delay 10 ms



SlaveIC Addr Mode ☐ Hex ☒ Auto Read ☒

Address: 0xF019 Read Batch Read

Value: 0x0018 Write Batch Write

7 6 5 4 3 2 1 0

Small 15 14 13 12 11 10 9 8

Batch Delay 10 ms

3. Use batch write to load script file, Flash_Wr_Protect_None -00.txt, to unprotect flash.
4. Read BPX to check the status. BP_{3~0} should be cleared.

1. If you find you can't write to flash as you want like calibration, please run unprotect flash procedure.
2. Run your tool like calibration to do your job.

Note: *Don't remove the module after you unprotect flash. Or, the flash will be protected again when the module is powered on.*

	Protected Flash	Unprotected Flash
Property Bar/ User Data	V	V
Calibration / Program Data	X	V



D:_M\019 BETA01 FP\YX8059-B01-CH65M-BL60U-019-BETA01-256K-FP.bin	D:\X8059\ROM\019 BETA01 FP\after K\20210806-02-after-K-on-protected.bin	D:\eYs3D\Projects\PIEX8059\ROM\019 BETA01 FP\after K\20210809-after-K-
18610 03 05 f5 04 d0 f5 05 02 f5 06 00 f5 07 04 f5 08	18610 03 05 f5 04 d0 f5 05 02 f5 06 00 f5 07 04 f5 08	18610 03 05 f5 04 d0 f5 05 02 f5 06 41 f5 07 0f f5 08
18620 00 f5 09 00 f5 0a 00 f5 0b 00 f5 0c 1f f5 0d 00	18620 00 f5 09 00 f5 0a 00 f5 0b 00 f5 0c 1f f5 0d 00	18620 fd f5 09 07 f5 0a 2d f5 0b 9c f5 0c 05 f5 0d 03
18630 f5 0e 00 f5 0f 00 f5 10 04 f5 11 00 f5 12 80 f5	18630 f5 0e 00 f5 0f 00 f5 10 04 f5 11 00 f5 12 80 f5	18630 f5 0e 00 f5 0f 41 f5 10 0f f5 11 46 f5 12 9d f5
18640 13 1f f5 14 00 f5 15 00 f5 16 00 f5 17 00 f5 18	18640 13 1f f5 14 00 f5 15 00 f5 16 00 f5 17 00 f5 18	18640 13 06 f5 14 1c f5 15 00 f5 16 fa f5 17 03 f5 18
18650 00 f5 19 00 f5 1a 02 f5 1b 00 f5 1c 00 f5 1d 80	18650 00 f5 19 00 f5 1a 02 f5 1b 00 f5 1c 00 f5 1d 80	18650 26 f5 19 fc f5 1a 01 f5 1b 00 f5 1c 00 f5 1d 80
18660 f5 1e 02 f5 1f 00 f5 20 00 f5 21 68 f5 22 01 f5	18660 f5 1e 02 f5 1f 00 f5 20 00 f5 21 68 f5 22 01 f5	18660 f5 1e 02 f5 1f 00 f5 20 00 f5 21 68 f5 22 01 f5
18670 40 00 f5 42 00 f5 44 00 f5 45 00 f5 46 00 f5 47	18670 40 00 f5 42 00 f5 44 00 f5 45 00 f5 46 00 f5 47	18670 40 03 f5 42 7f f5 44 6a f5 45 ff f5 46 0a f5 47
18680 00 f5 48 00 f5 49 00 f5 4a 00 f5 4b 00 f5 4c 00	18680 00 f5 48 00 f5 49 00 f5 4a 00 f5 4b 00 f5 4c 00	18680 00 f5 48 02 f5 49 00 f5 4a 00 f5 4b 00 f5 4c 00
18690 f5 4d 00 f5 4e 00 f5 4f 00 f5 50 00 f5 51 10 f5	18690 f5 4d 00 f5 4e 00 f5 4f 00 f5 50 00 f5 51 10 f5	18690 f5 4d 00 f5 4e 00 f5 4f 00 f5 50 1d f5 51 0a f5
186a0 52 00 f5 53 08 f5 54 00 f5 55 40 f5 56 00 f5 57	186a0 52 00 f5 53 08 f5 54 00 f5 55 40 f5 56 00 f5 57	186a0 52 ce f5 53 05 f5 54 60 f5 55 11 f5 56 00 f5 57
186b0 00 f5 58 40 f5 59 00 f5 73 02 f5 74 00 f5 75 02	186b0 00 f5 58 40 f5 59 00 f5 73 02 f5 74 00 f5 75 02	186b0 56 f5 58 11 f5 59 00 f5 23 41 f5 24 0f f5 25 fb
186c0 f5 76 00 f5 77 00 f5 78 00 f5 79 02 f5 7a 80 f5	186c0 f5 76 00 f5 77 00 f5 78 00 f5 79 02 f5 7a 80 f5	186c0 f5 26 07 f5 27 05 f5 28 9f f5 29 05 f5 2a 05 f5
186d0 7b 00 f5 7c 00 f5 7d 01 f5 7e 68 f5 23 00 f5 24	186d0 7b 00 f5 7c 00 f5 7d 01 f5 7e 68 f5 23 00 f5 24	186d0 2b 00 f5 2c 41 f5 2d 0f f5 2e 43 f5 2f 9b f5 30
186e0 04 f5 25 00 f5 26 00 f5 27 00 f5 28 00 f5 29 1f	186e0 04 f5 25 00 f5 26 00 f5 27 00 f5 28 00 f5 29 1f	186e0 06 f5 31 08 f5 32 00 f5 33 06 f5 34 00 f5 35 26
186f0 f5 2a 00 f5 2b 00 f5 2c 00 f5 2d 04 f5 2e 00 f5	186f0 f5 2a 00 f5 2b 00 f5 2c 00 f5 2d 04 f5 2e 00 f5	186f0 f5 36 fe f5 37 01 f5 38 00 f5 39 00 f5 3a 80 f5
18700 2f 80 f5 30 1f f5 31 00 f5 32 00 f5 33 00 f5 34	18700 2f 80 f5 30 1f f5 31 00 f5 32 00 f5 33 00 f5 34	18700 3b 02 f5 3c 00 f5 3d 00 f5 3e 68 f5 3f 01 f5 5a
18710 00 f5 35 00 f5 36 00 f5 37 02 f5 38 00 f5 39 00	18710 00 f5 35 00 f5 36 00 f5 37 02 f5 38 00 f5 39 00	18710 fe f5 5b 01 f5 5c 6c f5 5d ff f5 5e 07 f5 5f 00
18720 f5 3a 80 f5 3b 02 f5 3c 00 f5 3d 00 f5 3e 68 f5	18720 f5 3a 80 f5 3b 02 f5 3c 00 f5 3d 00 f5 3e 68 f5	18720 f5 60 04 f5 61 00 f5 62 00 f5 63 00 f5 64 00 f5
18730 3f 01 f5 5a 00 f5 5b 00 f5 5c 00 f5 5d 00 f5 5e	18730 3f 01 f5 5a 00 f5 5b 00 f5 5c 00 f5 5d 00 f5 5e	18730 65 00 f5 66 00 f5 67 00 f5 68 0e f5 69 0a f5 6a
18740 00 f5 5f 00 f5 60 00 f5 61 00 f5 62 00 f5 63 00	18740 00 f5 5f 00 f5 60 00 f5 61 00 f5 62 00 f5 63 00	18740 d4 f5 6b 05 f5 6c 65 f5 6d 11 f5 6e 00 f5 6f 5b
18750 f5 64 00 f5 65 00 f5 66 00 f5 67 00 f5 68 00 f5	18750 f5 64 00 f5 65 00 f5 66 00 f5 67 00 f5 68 00 f5	18750 f5 70 11 f5 71 00 f5 72 00 f5 73 02 f5 74 00 f5
18760 69 10 f5 6a 00 f5 6b 08 f5 6c 00 f5 6d 40 f5 6e	18760 69 10 f5 6a 00 f5 6b 08 f5 6c 00 f5 6d 40 f5 6e	18760 75 02 f5 76 00 f5 77 00 f5 78 00 f5 79 00 f5 7c
18770 00 f5 6f 00 f5 70 40 f5 71 00 f5 7a 00 f5 7b 02	18770 00 f5 6f 00 f5 70 40 f5 71 00 f5 7a 00 f5 7b 02	18770 00 f5 7b 00 f5 7c 00 f5 7d 00 f5 7e 00 f5 7f 00 f5
18780 f5 bc 00 f5 bd 02 f5 be 00 f5 bf 20 f5 c0 80 f5	18780 f5 bc 00 f5 bd 02 f5 be 00 f5 bf 20 f5 c0 80 f5	18780 f5 bb 00 f5 bc 00 f5 bd 00 f5 be 00 f5 bf 00 f5 c0 f5
18790 c1 00 f5 c2 10 f5 c3 68 f5 72 07 f5 7f 00 f5	18790 c1 00 f5 c2 10 f5 c3 68 f5 72 07 f5 7f 00 f5	18790 bf 00 f5 c1 00 f5 c2 00 f5 c3 00 f5 c4 00 f5 c5 00 f5
187a0 10 f5 af f8 f5 83 80 f5 84 20 f5 b0 10 f5 b1 20	187a0 10 f5 af f8 f5 83 80 f5 84 20 f5 b0 10 f5 b1 20	187a0 00 f5 af ff f5 7f 40 f5 83 50 f5 84 10 f5 b0 10
187b0 f5 b2 00 f5 b3 0a f5 c8 ff f5 c9 00 00 00 00 00	187b0 f5 b2 00 f5 b3 0a f5 c8 ff f5 c9 00 00 00 00 00	187b0 f5 b1 20 f5 b2 00 f5 b3 0a f5 c4 14 f5 c5 05 f5
187c0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	187c0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	187c0 c6 00 f5 c7 00 f5 c8 ff f5 c9 00 f4 2b 80 f4 2c
187d0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	187d0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	187d0 04 f4 2b 81 f4 2c 04 f4 2b 82 f4 2c 08 f4 2b 83
187e0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	187e0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	187e0 f4 2c 0c f4 2b 84 f4 2c 10 f4 2b 85 f4 2c 18 f4
187f0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	187f0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	187f0 2b 86 f4 2c 20 f4 2b 87 f4 2c 30 f4 2b 88 f4 2c
18800 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	18800 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	18800 40 f4 2b 89 f4 2c 50 f4 2b 8a f4 2c 60 f4 2b 8b
18810 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	18810 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	18810 f4 2b 8c f4 2c 60 f4 2b 8d f4 2c 70 f4 2c 80 f4 2c
18820 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	18820 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	18820 2b 8e f4 2c 80 f4 2c 90 f4 2c 9a f4 2c 9b f4 2c
18830 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	18830 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	18830 c0 f4 2b 90 f4 2b 91 f4 2b 92 f4 2b 93 f4 2b 94 f4 2b
18840 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	18840 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	18840 f4 2b 95 f4 2b 96 f4 2b 97 f4 2b 98 f4 2b 99 f4 2b
18850 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	18850 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	18850 af 10 f4 02 ef f4 03 14 f4 04 ff f4 09 45 f4 10
18860 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	18860 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	18860 07 f4 32 09 f4 33 05 f4 34 0a f4 36 05 f4 39 0a
18870 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	18870 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	18870 f4 3a 05 f4 3b 00 f4 3c 00 f4 3d 0a f4 3e 01 f4
18880 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	18880 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	18880 3f 03 f4 40 01 f4 41 00 f4 42 01 f4 4f 06 00 00

Original ROM

Calibrated on Protected Flash

Calibrated on Unprotected Flash

2. Header

Offset	Field	Size	Description
0x00	Signature	8	String "AXES-CFG"
0x08	Version	2	1 for initial release.
0x0A	STI_Offset	2	Offset of "Storage Type Information" 0xFFFF means use default SPI Flash Storage

- Find the STI offset from header table illustrated at the left table, and check the StructLen value.

New structure

3. Storage Type Information

Old structure

11 Storage Type Information

Offset	Field	Size	Description
0	StructLen	1	Struct Length of Storage Information(不包含長度欄位本身，因此目前為 11)
1	SpiPageShift	1	Power of SPI Page Size. (Page: minimal writing size) It should be 8 (256) now
2	SpiSecShift	1	Power of SPI Sector Size. (Sector: minimal erasing size)
3	Reserved	1	Always set as 32
4	SpiTotalSec	2	SPI Total Sector Number.
6	UserAreaStartSec	2	Start Sector Number of User Area. Set as 0 to Disabled User Area.
8	UserAreaEndSec	2	End Sector Number of User Area
10	SpiWpGpioNum	1	SPI Flash Write Protection GPIO Register (Low Byte)
11	SpiWpGpioPin	1	SPI Flash Write Protection GPIO Pin
...	...		

Offset	Field	Size	Description
0	StructLen	1	Struct Length of Storage Information(不包含長度欄位本身，因此目前為 17)
1	SpiPageShift	1	Power of SPI Page Size. (Page: minimal writing size) It should be 8 (256) now
2	SpiSecShift	1	Power of SPI Sector Size. (Sector: minimal erasing size)
3	Reserved	1	Always set as 32
4	SpiTotalSec	2	SPI Total Sector Number.
6	UserAreaStartSec	2	Start Sector Number of User Area. Set as 0 to Disabled User Area.
8	UserAreaEndSec	2	End Sector Number of User Area
10	SpiWpGpioNum	1	SPI Flash Write Protection GPIO Register (Low Byte)
11	SpiWpGpioPin	1	SPI Flash Write Protection GPIO Pin
12	UnpAreaStartSec	2	UnProtection Area Start Sector Set as 0 to Disabled UNP Area
14	UnpAreaSizeShift	1	Power of UnProtection Area Size (Ex. 16=64K)
15	SpiWpSts	1	SPI Flash Write Protection Status
16	SpiInitCfg	2	SPI Flash Initial Config Value
...	...		

1. If the StructLen is 0x0B, this bin file doesn't support flash protection.
2. If it is other than 0x0B, 0x11 for current case, this bin file supports flash protection.
 1. The first 128KB is protected.
 2. If UnpAreaStartSec is 0, this bin file doesn't have unprotected area. If it is not 0, the unprotected address starts at $N * 4096$. N is UnpAreaStartSec value.
3. For example, the current setting is $48 \times 4096 = 196608 = 0x30000$. The UNP starts at address 0x30000.

Without flash protection scheme

With flash protection scheme

Header

Offset(h)	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
00010000	41	58	45	53	2D	43	46	47	00	19	0D	12	00	20	01	00
00010010	0C	DC	08	DE	7A	A0	7A	84	FF	FF	0D	1E	00	00	00	00
00010020	03	02	01	0F	08	00	00	00	09	00	00	00	01	00	00	00
00010030	08	00	00	00	03	01	03	00	00	00	00	01	00	00	00	00
00010040	00	00	00	01	00	00	00	04	0F	01	00	00	00	01	00	00

Storage Type Information

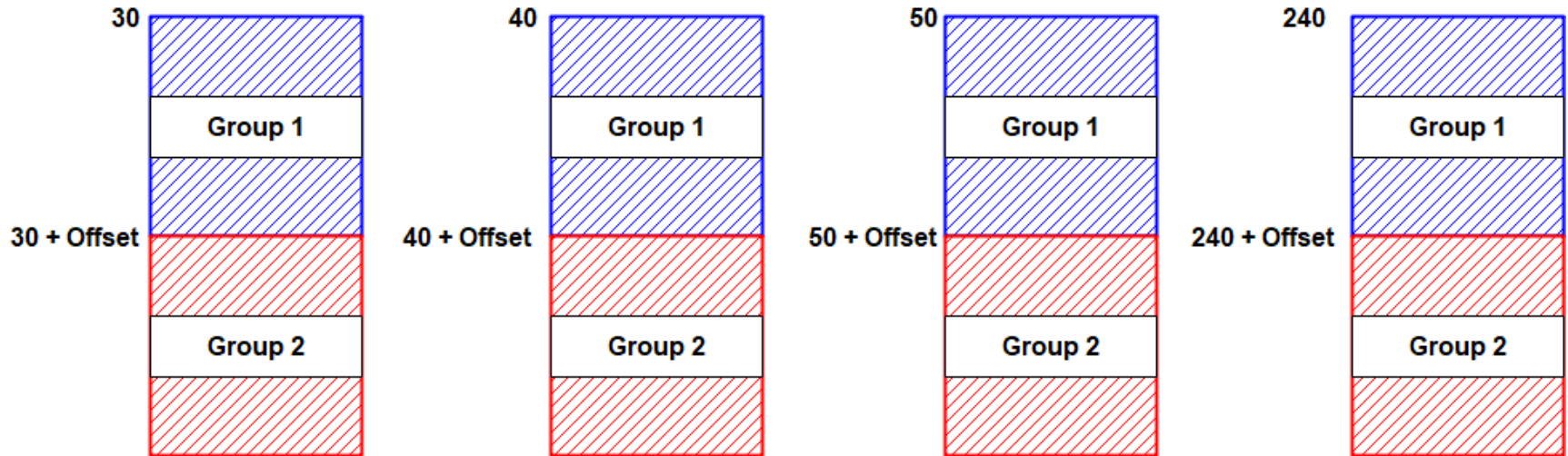
Offset(h)	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
00010D10	0D	12	0B	08	0C	20	00	20	00	00	00	00	19	03	36	00
00010D20	00	00	00	EC	01	00	EC	02	CA	02	03	B6	01	F3	03	05
00010D30	A9	00	E4	04	06	8D	03	9F	05	0A	2C	03	A8	06	0D	D4
00010D40	06	6E	07	14	42	02	99	08	16	DB	03	97	09	1A	72	01
00010D50	0E	0A	1B	80	00	E5	0B	1C	65	02	93	0C	1E	F8	01	C4

Header

Offset(h)	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
00010000	41	58	45	53	2D	43	46	47	00	1C	0D	44	00	20	01	00
00010010	0D	0E	09	10	7C	D6	7C	BA	FF	FF	0D	56	00	00	00	00
00010020	03	02	01	0F	08	00	00	00	09	00	00	00	01	00	00	00
00010030	08	00	00	00	03	01	03	00	00	00	00	01	00	00	00	00
00010040	00	00	00	01	00	00	00	04	04	0F	01	00	00	00	01	00

Storage Type Information

Offset(h)	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
00010D40	00	00	0D	44	11	08	0C	20	00	40	00	00	00	00	19	03
00010D50	00	30	10	88	00	08	36	00	00	00	00	EC	01	00	EC	02
00010D60	CA	02	03	B6	01	F3	03	05	A9	00	E4	04	06	8D	03	9F
00010D70	05	0A	2C	03	A8	06	0D	D4	06	6E	07	14	42	02	99	08
00010D80	16	DB	03	97	09	1A	72	01	0E	0A	1B	80	00	E5	0B	1C



1. The group 1 is the factory settings which are calibrated before shipment. The group 2 is user settings which are the shadow of factory settings after post calibration.
2. FW Register 0xF6 is the offset.
3. The final file ID is loaded = file id + offset which is stored at 0xF6.
4. The default offset is set as 5 which means 10 is divided by 2 (groups) = 5
5. For example, 30/40/50/240 are factory settings, 35/45/55/245 are user settings
6. File ID:
 - 030 ~ 039: Y-Offset
 - 040 ~ 049: Rectification
 - 050 ~ 059: ZD table
 - 240 ~ 249: Log

1. The UNP (**UN**Protect ion) area still has a chance to be destroyed. Hence, data in this area will be compressed and saved in the file id 201.
2. If the application needs to restore to factory settings for UNP area, it can get UNP backup from file id 201 and restore to UNP area.
3. Default length of file id 201 is 512 bytes.



Flash_Wr_Protect_None -00.txt



RD_Flash_Configuration_(SPI_RDCCR_CMD).txt



RD_Flash_STS_(SPI_RDSR_CMD).txt

1. Axes Plugin Data Binary File Format.doc

*Thanks for your attention.
Any comment is sincerely appreciated.*