**Group 27**
**Loren Lugosch 260404057**
**Lulan Shen 260449509**

## Part 2: Envelope Circuit

### Building and Testing

The envelope circuit generates a rising and falling logarithmic waveform. It makes this waveform by keeping track of what values it has outputted and increasing accordingly. Hence we need memory elements like flip-flops, and indeed the circuit has a single register after a set of combinational logic blocks.

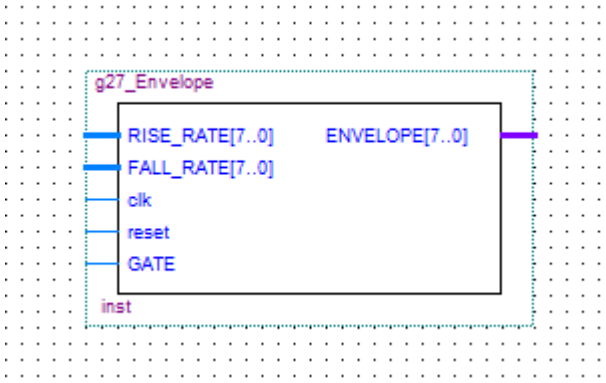



*Figure 1- Symbol for Envelope*

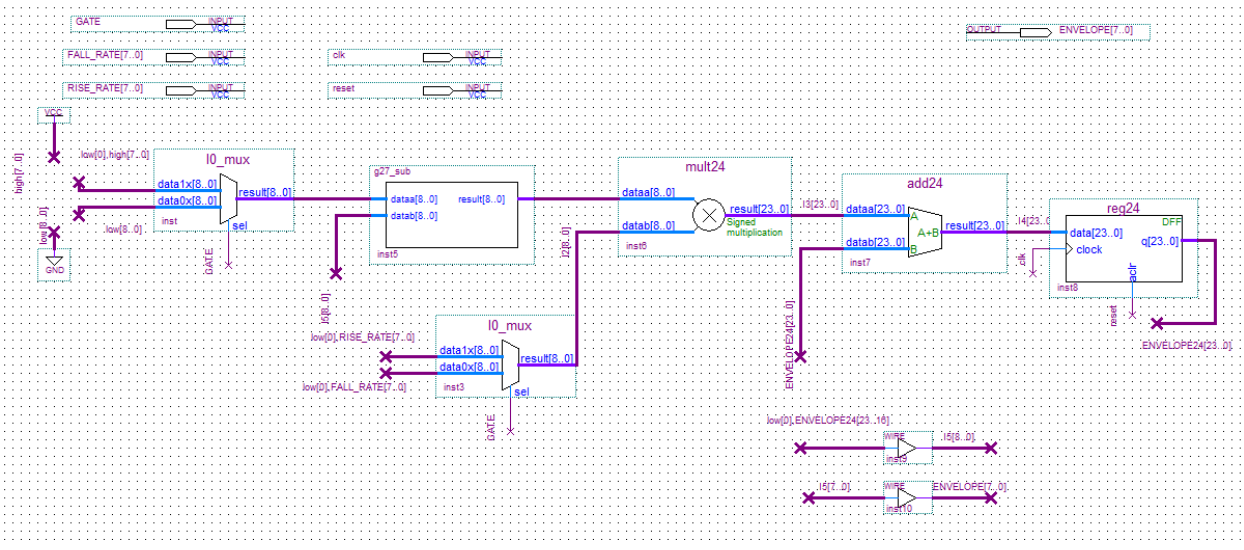



*Figure 2- Interior of Envelope Circuit*

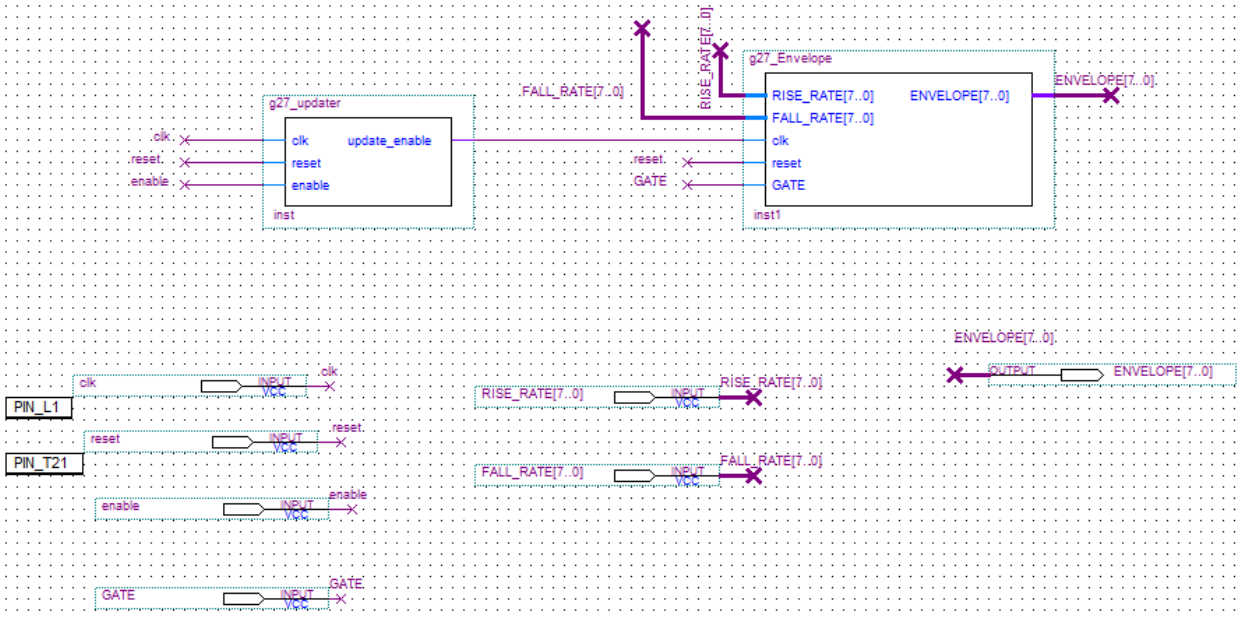



*Figure 3- without LEDs*

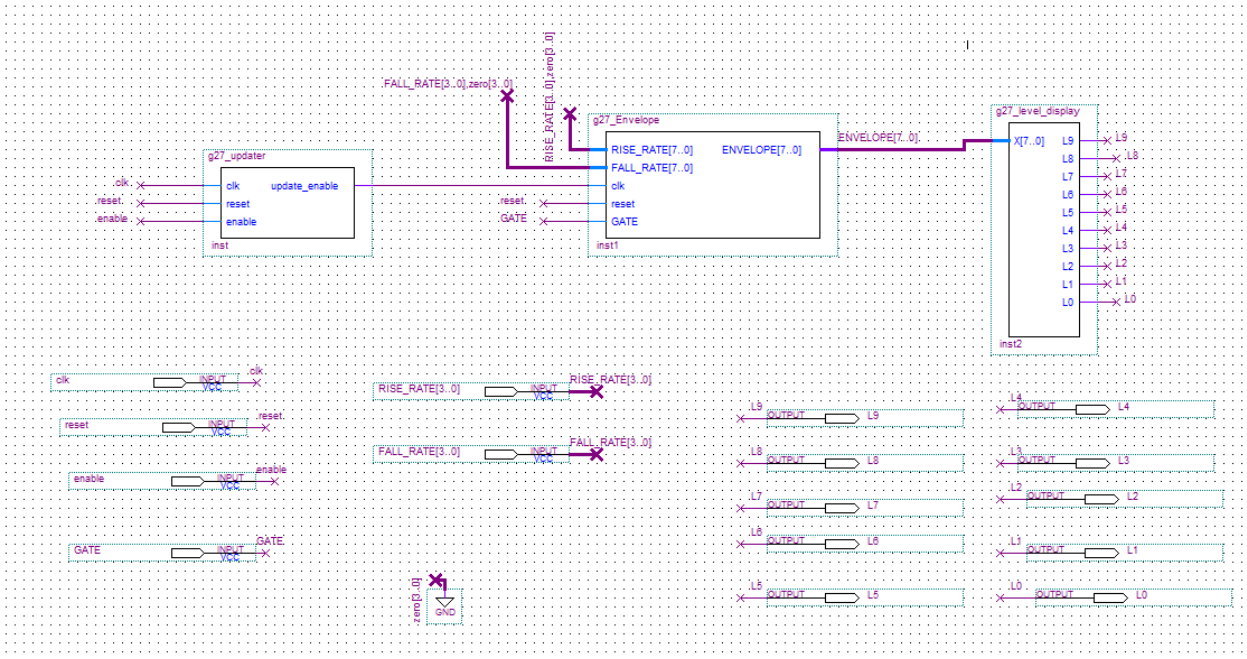



*Figure 4-Testbed with LEDs*

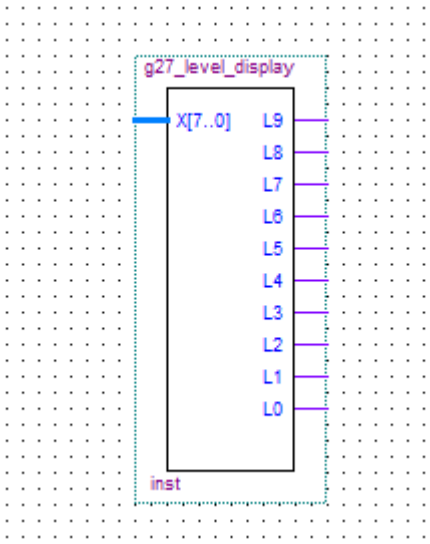



*Figure 5- Symbol for LED computation*

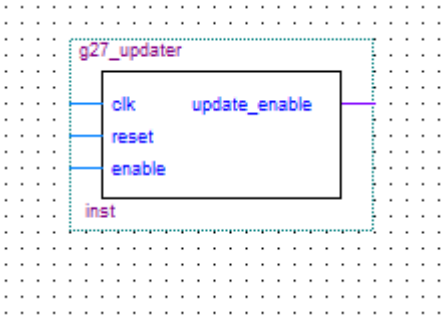



*Figure 6- Symbol for frequency divider*

To check that our circuit was increments ENVELOPE correctly, we calculate what the value ought to be after the first UPDATE_ENABLE given RISE_RATE = 11111111:

> ENVELOPE24 at **time 1** (i.e. after the first UPDATE_ENABLE)= RISE_RATE * [255 – ENVELOPE at time 0] + ENVELOPE24 at time 0
>
> = 11111111*[11111111 – 00000000] + 000000000000000000000000
>
> = 00000000 11111110 00000001
>
> ENVELOPE at time 1 = ENVELOPE24(23 downto 16) at time 1 = **00000000**

Looking at the simulation, the value after one UPDATE_ENABLE period (20.8 us) is 0 as we expect. (Hence the envelope = 0 for **two** UPDATE_ENABLE periods.)

We repeat the calculation to find the value after the first UPDATE_ENABLE:

> ENVELOPE24 at **time 2** = RISE_RATE * [255 – ENVELOPE at time 1] + ENVELOPE24 at time 1
>
> = 11111111*[11111111 – 00000000] + 000000001111111000000001
>
> = 000000001111111000000001 * 2

= 00000001 11111100 00000010

ENVELOPE at time 2 = ENVELOPE24(23 downto 16) at time 2 = **00000001**

These two values match what we see in the simulation.

The maximum time needed for the envelope to rise from 0 to 100 (0% to 39 %) depends on the minimum rise rate. If rise rate = 00000001, this time is about 200 ms. The minimum time, 5 ms, occurs when rate = 11111111.

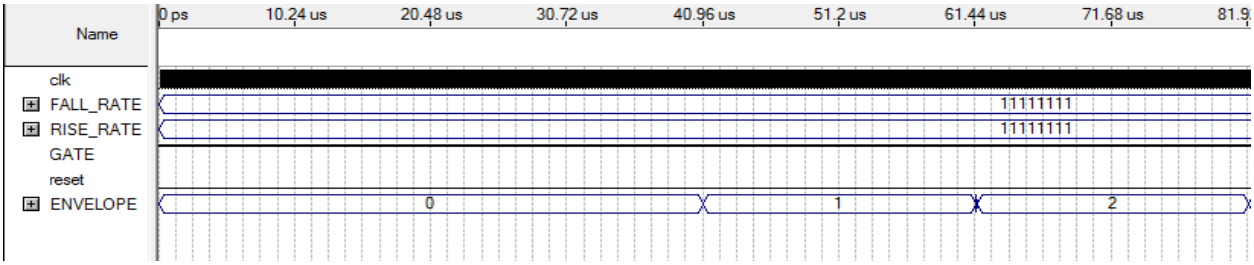



*Figure 7- ENVELOPE increments to 0 after one period, 1 after two periods, 2 after three periods*

We check the envelope over 80 us given a fast rise rate/fall rate (11111111) and a slow rise rate/fall rate (01000000).

For an envelope with RISE_RATE high, the output reaches 255 quickly and plateaus at around 30 ms; hence the output remains at 254 for a long time before switching to 255. The same applies for the falling part of the envelope.

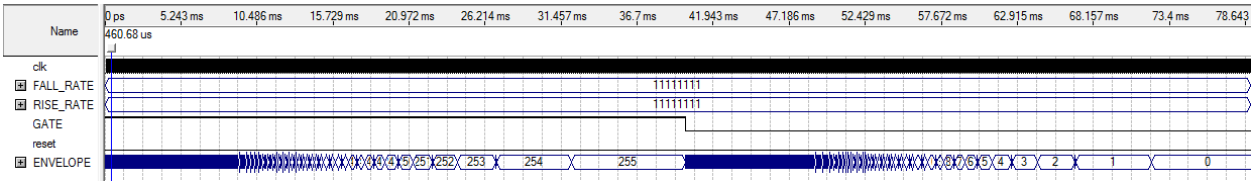



*Figure 8- ENVELOPE with RISE_RATE = FALL_RATE = 11111111*

For an envelope with RISE_RATE low, the output reaches 255 more slowly and thus does not plateau the way a fast envelope does. (As shown in the closeups below, the envelope at 40 ms only reaches 216 in the rising state and 34 in the falling state.)

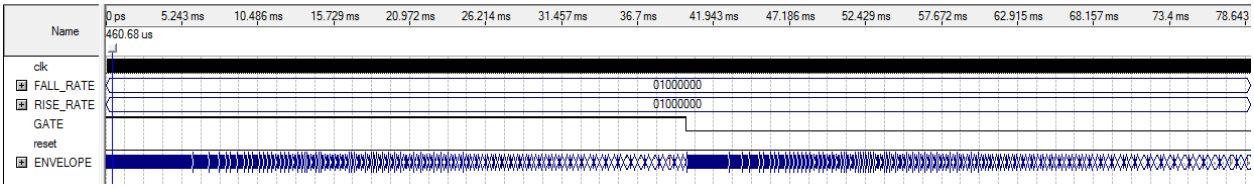



*Figure 9- ENVELOPE with RISE_RATE = 01000000*

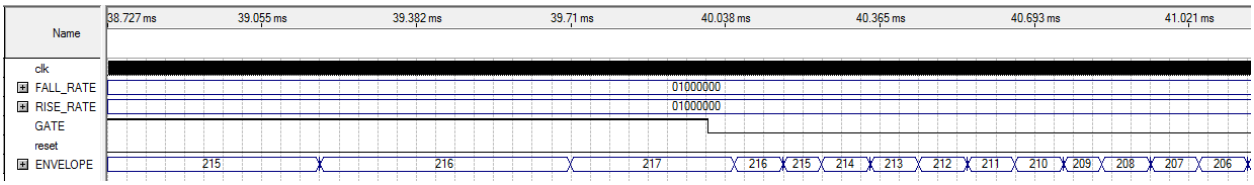



*Figure 10- Closeup of value at end of rising state*

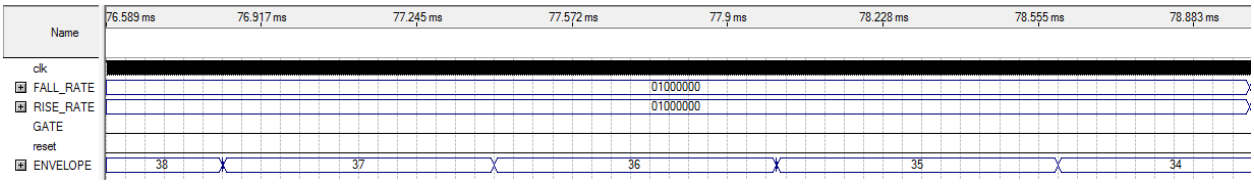



*Figure 11- Closeup of value at end of falling state*

Using Signal Tap, we look at the value of envelope inside the running circuit. Signal tap samples for 128 clock cycles and displays the state of the chosen wires.

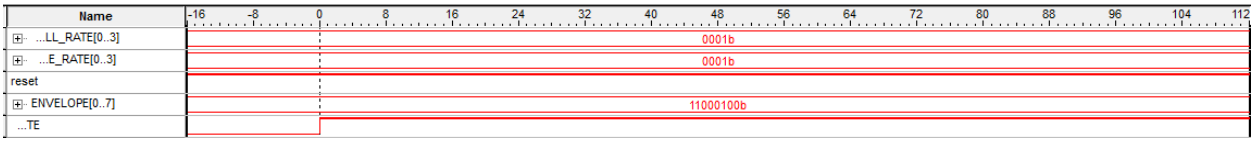



*Figure 12-rise slow*

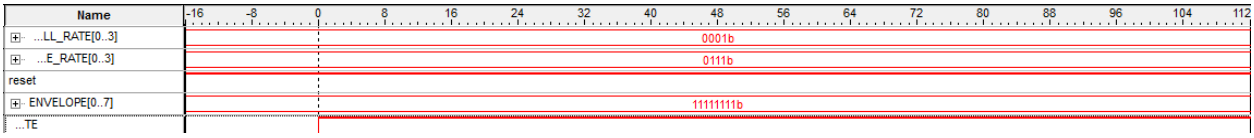
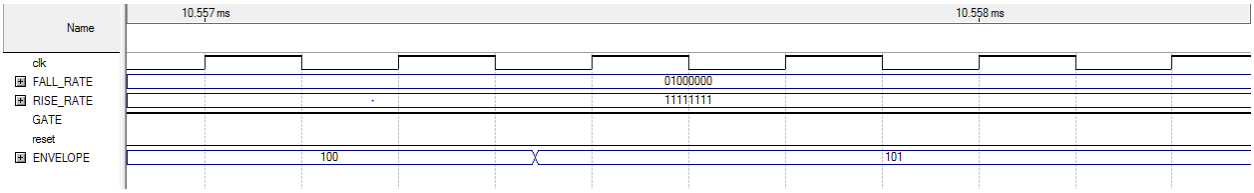



*Figure 13- rise fast*

## Timing Analysis

There is a 4.23 ns delay.



## FPGA Utilization

| | |
|---|---|
| Flow Status | Successful - Fri Nov 08 20:43:50 2013 |
| Quartus II 64-Bit Version | 9.1 Build 350 03/24/2010 SP 2 SJ Full Version |
| Revision Name | g27_lab3 |
| Top-level Entity Name | g27_Envelope |
| Family | Cyclone II |
| Device | EP2C20F484C7 |
| Timing Models | Final |
| Met timing requirements | N/A |
| Total logic elements | 650 / 18,752 ( 3 % ) |
| Total combinational functions | 405 / 18,752 ( 2 % ) |
| Dedicated logic registers | 524 / 18,752 ( 3 % ) |
| Total registers | 524 |
| Total pins | 27 / 315 ( 9 % ) |
| Total virtual pins | 0 |
| Total memory bits | 2,304 / 239,616 ( < 1 % ) |
| Embedded Multiplier 9-bit elements | 1 / 52 ( 2 % ) |
| Total PLLs | 0 / 4 ( 0 % ) |