ECSE 323 Digital System Design

Lab #4 – VHDL for Sequential Circuit Design

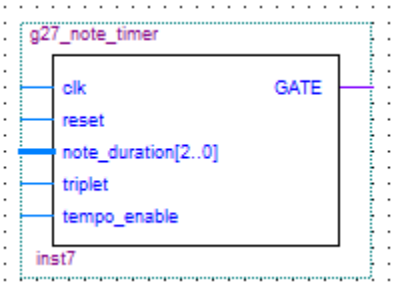
Group 27

Lulan Shen (260449509)
Loren Lugosch (260404057)

Part 2: Note Timer Circuit

Circuit Description and Design

The square wave circuit takes as input a 50MHz clock, a reset signal, a note duration (000 = 1 32nd-note, 111 = 4 whole-notes), a triplet indicator, and a tempo enable.



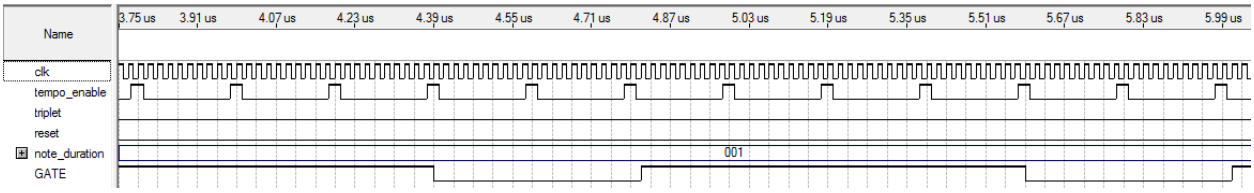
When tempo_enable is high, a counter in the circuit increments; when the count hits half of the note duration (translated into clock cycles), GATE goes low: this gives a staccato output for the appropriate duration.

Testing and Simulation

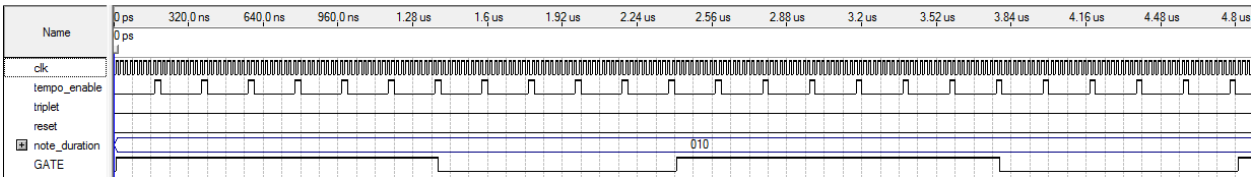
We simulated the timer circuit alone by clocking tempo enable at a fraction of the clock rate with a small duty cycle.

note_duration = 1 and triplet = 0

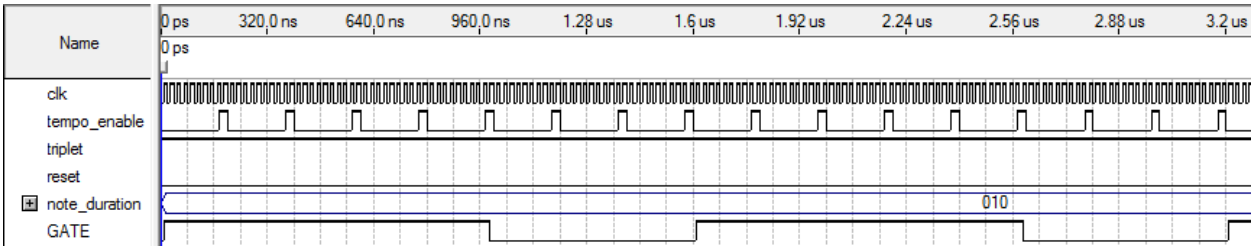
Corresponding number of tempo pluses per note should be 6. Gate is high for first 4 pulses and low for the rest.



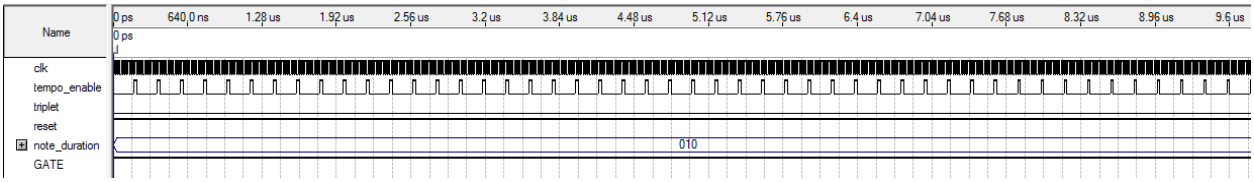
- note_duration = 2 and triplet = 0
  Corresponding number of tempo pluses per note should be 12. Gate is high for first 7 pulses and low for the rest.



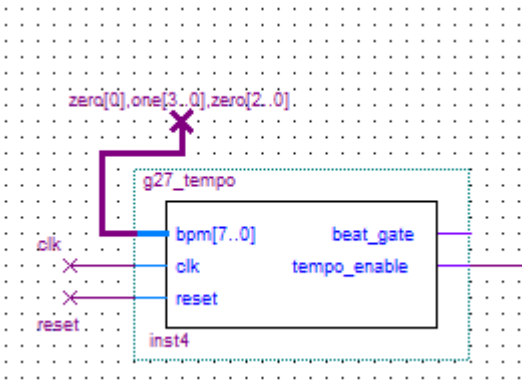
- note_duration = 2 and triplet = 1
  Corresponding number of tempo pluses per note should be 8. Gate is high for first 5 pulses and low for the rest.



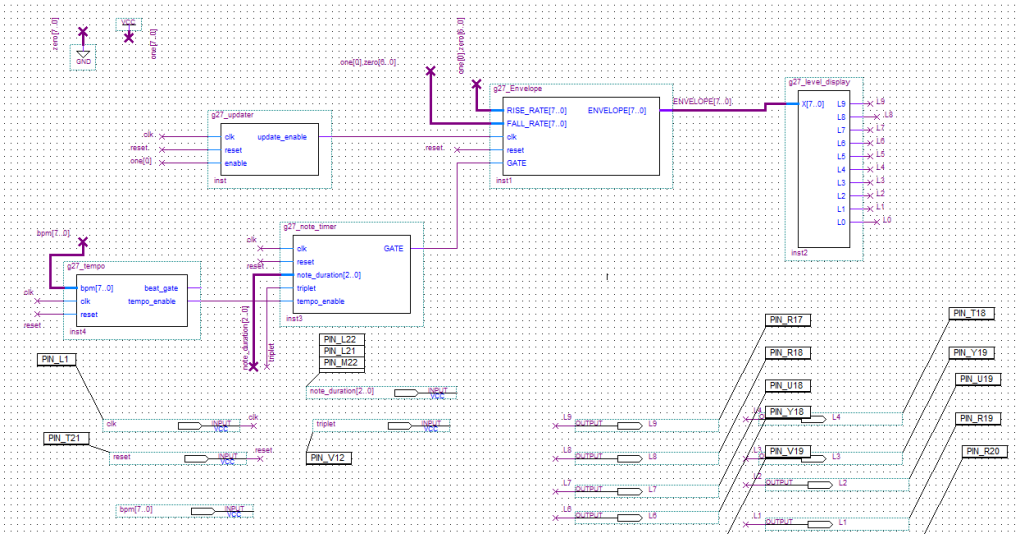
- reset = 1
  Upon reset set an internal count signal to zero, the GATE output signal will be high.



We tested the complete timer circuit at 120 bpm by fixing the input to 01110000, as seen below:



We programmed the board and found that the beats were 120 bpm (for quarter notes, and 60 bpm for half notes, 240 bpm for eighth notes, etc.). Then we connected the switches to the tempo enabler:



We tested the circuit for various tempi and note durations successfully.

Timing Analysis

Timing Analyzer Summary

	Type	Slack	Required Time	Actual Time	From	To	From Clock	To Clock	Failed Paths
1	Worst-case tsu	N/A	None	3.126 ns	triplet	g27_note_timer:inst3|GATE	--	clk	0
2	Worst-case tco	N/A	None	19.764 ns	g27_Envelope:inst1|lpm_ff:reg|dffs[17]	L5	clk	--	0
3	Worst-case th	N/A	None	-0.887 ns	note_duration[2]	g27_note_timer:inst3|GATE	--	clk	0
4	Clock Setup: 'clk'	N/A	None	97.00 MHz (period = 10.309 ns)	g27_Envelope:inst1|lpm_ff:reg|dffs[16]	g27_Envelope:inst1|lpm_ff:reg|dffs[23]	clk	clk	0
5	Total number of failed paths								0

The combinational delay is worryingly large. Our clock cycle is 20 ns, and the combinational delay is 19.764 ns, so we may need to improve some part of our circuit later.

FPGA Resouce Utilization

The large number of registers in our resource utilization makes sense, as the circuit uses a ROM to store the appropriate period in 50 MHz clock cycles for lookup.

Flow Status	Successful - Fri Nov 22 20:06:37 2013
Quartus II 64-Bit Version	9.1 Build 350 03/24/2010 SP 2 SJ Full Version
Revision Name	g27_lab4
Top-level Entity Name	g27_squarewave_generator_testbed
Family	Cyclone II
Device	EP2C20F484C7
Timing Models	Final
Met timing requirements	Yes
Total logic elements	1,020 / 18,752 (5 %)
Total combinational functions	624 / 18,752 (3 %)
Dedicated logic registers	836 / 18,752 (4 %)
Total registers	836
Total pins	43 / 315 (14 %)
Total virtual pins	0
Total memory bits	0 / 239,616 (0 %)
Embedded Multiplier 9-bit elements	0 / 52 (0 %)
Total PLLs	0 / 4 (0 %)