Test Systems Suitability Assessment Report

TO :

CUSTOMER :

FROM : GP Synergia Technologies Corp.

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DATE :

SUBJECT : **CTS5400 to STS GP3 Migration**

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1. Executive Summary

The Test Systems Suitability Assessment report assesses the compatibility of the NI STS GP3 (National Instruments STS GP3) as a substitute for the CTS5400 in testing the AD5750, Industrial Current/Voltage Output Driver with Programmable Ranges. The assessment compared the functionality, performance, and scalability of both systems. Following the evaluation, it is recommended that the NI STS GP3 is a suitable option for testing the device on up to 4 sites.

2. Introduction

The objective of this Test Systems Suitability Assessment is to evaluate the potential of the NI STS GP3 as a replacement for the outdated CTS5400 System currently used to test the AD5750. The CTS5400 system is encountering difficulties in terms of performance, maintenance, and productivity. The primary goal of this assessment is to ascertain whether the NI STS GP3 is capable of effectively substituting the CTS5400 for testing the AD5750.

3. Assessment Methodology

The assessment methodology included conducting a functional and performance analysis of both the legacy system and the new target system. The customer was assumed to have already completed the criteria of scalability, maintainability, reliability, and cost. The assessment team extensively analyzed the known capabilities of each tester, considering factors such as instrument accuracy, resolution, range, speed, and sensitivity.

The core of the assessment methodology relied on comparative analysis, which served as the foundation for evaluating the suitability of the new target system. By carefully examining and contrasting the functional and performance aspects of both the legacy and new systems, the team was able to identify potential improvements or limitations offered by the new system. This analysis was firmly grounded in the collected DUT data and the team's knowledge of the capabilities of each tester, ensuring a comprehensive and objective evaluation. Key factors such as instrument accuracy, resolution, range, speed, and sensitivity were thoroughly examined, as they play a critical role in semiconductor testing, directly influencing the precision, reliability, and quality of measurements obtained.

The primary goal of this assessment methodology was to facilitate informed decision-making regarding the selection of the most suitable measuring instrument for testing the device. By following this methodology, the assessment team ensured a thorough and systematic evaluation, considering vital factors necessary for accurate and reliable measurements.

4. Overview

PRODUCT DESCRIPTION

The AD5750/AD5750-1/AD5750-2 are single-channel, low cost, precision voltage/current output drivers with hardware- or software-programmable output ranges. The software ranges are configured via an SPI-/MICROWIRE-compatible serial interface. The AD5750/AD5750-1/AD5750-2 target applications in PLC and industrial process control. The analog input to the AD5750/ AD5750-1/AD5750-2 is provided from a low voltage, single-supply digital-to-analog converter (DAC) and is internally conditioned to provide the desired output current/voltage range. Analog input ranges available are 0 V to 2.5 V (AD5750-1/AD5750-2) or 0 V to 4.096 V (AD5750).

PIN CONFIGURATION

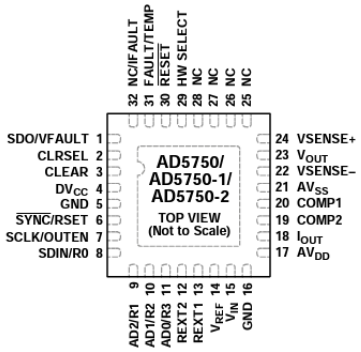


Table 1. Pin Function Description

Pin	Mnemonic	Function
1	SDO/VFAULT	Serial Data Output (SDO). In software mode, this pin is used to clock data from the input shift register in readback mode. Data is clocked out on the rising edge of SCLK and is valid on the falling edge of SCLK. This pin is a CMOS output.
2	CLRSEL	In hardware or software mode, this pin selects the clear value, either zero-scale or midscale code. In software mode, this pin is implemented as a logic OR with the internal CLRSEL bit.
3	CLEAR	Active High Input. Asserting this pin sets the output current/voltage to zero-scale code or midscale code of the range selected (user selectable). CLEAR is a logic OR with the internal clear bit. In software mode, during power-up, the CLEAR pin level determines the power-on condition of the voltage channel, which can be active 0 V or tristate. See the Asynchronous Clear (CLEAR) section for more details.
4	DVCC	Digital Power Supply.
5	GND	Ground Connection.
6	SYNC/RSET	Positive Edge Sensitive Latch (SYNC). In software mode, a rising edge parallel loads the input shift register data into the AD5750/AD5750-1/AD5750-2, also updating the output. Resistor Select (RSET). In hardware mode, this pin selects whether the internal or the external current sense resistor is used. If RSET = 0, the external sense resistor is chosen, and if RSET = 1, the internal sense resistor is chosen.
7	SCLK/OUTEN	Serial Clock Input (SCLK). In software mode, data is clocked into the input shift register on the falling edge of SCLK. This pin operates at clock speeds up to 50 MHz. Output Enable (OUTEN). In hardware mode, this pin acts as an output enable pin.
8	SDIN/R0	Serial Data Input (SDIN). In software mode, data must be valid on the falling edge of SCLK. Range Decode Bit (R0). In hardware mode, this pin, in conjunction with R1, R2, and R3, selects the output current/voltage range setting on the part.
9	AD2/R1	Device Addressing Bit (AD2). In software mode, this pin, in conjunction with AD1 and AD0, allows up to eight devices to be addressed on one bus. Range Decode Bit (R1). In hardware mode, this pin, in conjunction

		with R0, R2, and R3, selects the output current/voltage range setting on the part.
10	AD1/R2	Device Addressing Bit (AD1). In software mode, this pin, in conjunction with AD2 and AD0, allows up to eight devices to be addressed on one bus. Range Decode Bit (R2). In hardware mode, this pin, in conjunction with R0, R1, and R3, selects the output current/voltage range setting on the part.
11	AD0/R3	Device Addressing Bit (AD0). In software mode, this pin, in conjunction with AD1 and AD2, allows up to eight devices to be addressed on one bus. Range Decode Bit (R3). In hardware mode, this pin, in conjunction with R0, R1, and R2, selects the output current/voltage range setting on the part.
12,13	REXT2, REXT1	A 15 kΩ external current setting resistor can be connected between the REXT1 and REXT2 pins to improve the IOUT temperature drift performance.
14	VREF	Buffered Reference Input.
15	VIN	Buffered Analog Input (0 V to 4.096 V).
16	GND	Ground Connection.
17	AVDD	Positive Analog Supply.
18	IOUT	Current Output.
19, 20	COMP2, COMP1	Optional Compensation Capacitor Connections for the Voltage Output Buffer. These pins are used to drive higher capacitive loads on the output. They also reduce overshoot on the output. Care should be taken when choosing the value of the capacitor connected between the COMP1 and COMP2 pins because it has a direct influence on the settling time of the output. See the Driving Large Capacitive Loads section for further details.
21	AVSS	Negative Analog Supply
22	VSENSE−	Sense Connection for the Negative Voltage Output Load Connection. This pin must stay within ±3.0 V of ground for correct operation.
23	VOUT	Buffered Analog Output Voltage.
24	VSENSE+	Sense Connection for the Positive Voltage Output Load Connection.
25, 26, 27, 28	NC	No Connect. Can be tied to GND.
29	HW SELECT	This pin is used to configure the part to hardware or software mode. HW SELECT = 0 selects software control, and HW SELECT = 1 selects hardware control.
30	RESET	Resets the part to its power-on state.
31	FAULT/TEMP	Fault Alert (FAULT). In software mode, this pin acts as a general fault alert pin. It is asserted low when an open circuit error, short-circuit error, overtemperature error, or PEC interface error is detected. This pin is an open- drain output and must be connected to a pull-up resistor. Overtemperature Fault (TEMP). In hardware mode, this pin acts as an overtemperature fault pin. It is asserted low when an overtemperature error is detected. This pin is an open-drain output and must be connected to a pull-up resistor.
32	NC/IFAULT	No Connect (NC). In software mode, this pin is a no connect. Instead, tie this pin to GND. Open-Circuit Fault Alert (IFAULT). In hardware mode, this pin acts as an open-circuit fault alert pin. It is asserted low when an open-circuit error is detected. This pin is an open-drain output and must be connected to a pullup resistor.
33	EPAD	The exposed paddle is tied to AVSS.

5. Analysis

1. Manufacturing analysis:

This table summarizes the manufacturing details for current and proposed test solutions.

	Current	Proposed
Platform	CTS5400_B	STS GP3
Number of Sites	4	4
Handler	SEIKO EPSON	TBD
Performance Board	GTL-50202	TBD
Contactor	GTP-00306	TBD
Index Time	TBD	TBD
Test Time (Per device)	TBD	TBD

2. List of Affected T-Part/s

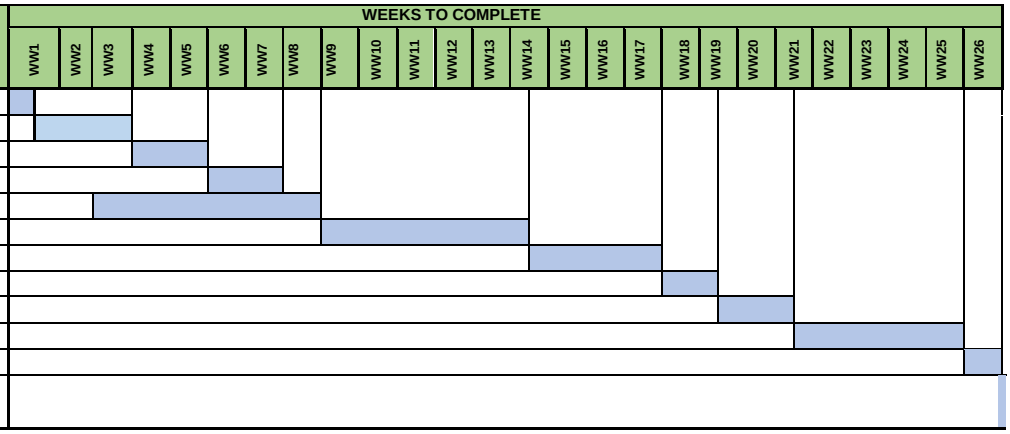
GENERIC	PARTNAME AFFECTED	No. of Leads	Package	Current Platform	Number of Test Pass
AD5750	AD5750-1ACPCT-T0Z.30	32	LFCSP	CTS5400_B	25C
	AD5750-1ACPCT-TEZ.12				
	AD5750-1ACPCT-TNZ.05				
	AD5750-1BCPCT-TNZ.05				
	AD5750-1BCPCT-TQZ.14				

3. Qualification Plan

Qualification will adhere to the specifications stated in TST00095 (Test Platform Migration/Conversion Flow) and TST00094 (Qualification Requirements for the Release of Test Application Hardware and Software to Manufacturing)

4. Test Migration/Development Schedule

Item	ACTIVITY	WEEKS TO COMPLETE
1	FEASIBILITY	
2	SCHEMATIC GENERATION	
3	HW LAYOUT	
4	ASSEMBLY	
5	TEST PROGRAM DEVELOPMENT	
6	TEST FLOW DEBUG	
7	CORRELATION	
8	ENGINEERING VERIFICATION	
9	BULK CORRELATION	
10	YIELD VALIDATION	
11	REJECT VERIFICATION	
12	FINAL TEST PROGRAM RELEASE/ SAFE LAUNCH	



A total of 26 working weeks is needed for this project development (working weeks does not include weekend or holidays).

5. Contingency Plan

The migration project from CTS5400 to NI_GP3 of AD5750 provides new platform capability which will be a help to free up constraint of CTS5400 testers. The planning forecast for the next upcoming four quarters needs to have materials ahead of qualification lot. In worst cases that no materials are available for test, setup verifiers (SUV) run will be done to both tester platforms to validate tester/handler interfacing.

6. Tester Technical Resource Mapping

DUT PIN	Pin Name	CTS5400 Resource	STS GP3 Resource
1	SDO/VFAULT	PINCARD D	PXIe-6571
2	CLRSEL	PINCARD D	PXIe-6571
3	CLEAR	PINCARD D	PXIe-6571
4	DVCC	PINCARD D	PXIe-6571
		V/I TYPE F	PXIe-4162
5	GND	GND	GND
		GND	GND
6	SYNC/RSET	PINCARD D	PXIe-6571
7	SCLK/OUTEN	PINCARD D	PXIe-6571
8	SDIN/R0	PINCARD D	PXIe-6571
9	AD2/R1	PINCARD D	PXIe-6571
10	AD1/R2	PINCARD D	PXIe-6571
11	AD0/R3	PINCARD D	PXIe-6571
12, 13	REXT2, REXT1	PINCARD D	PXIe-6571
		V/I TYPE F	PXIe-4162
14	VREF	PINCARD D	PXIe-6571
		DC SOURCE	PVS
		MEASURE MATRIX (DMM)	DMM4081
15	VIN	PINCARD D	PXIe-6571
		DC SOURCE	PVS
			PXIe-6368
		MEASURE MATRIX (DMM)	DMM4081
16	GND	GND	GND
		GND	GND
17	AVDD	PINCARD D	PXIe-6571
		USER POWER CARD	PXIe-4137
18	IOUT	PINCARD D	PXIe-6571
		LF Digitizer	PXIe-6368
		MEASURE MATRIX (DMM)	DMM4081
19, 20	COMP2, COMP1	PINCARD D	PXIe-6571
21	AVSS	PINCARD D	PXIe-6571
		ANALOG MATRIX	PXIe-4137
22	VSENSE−	PINCARD D	PXIe-6571
		MEASURE MATRIX (DMM)	DMM4081
		V/I TYPE F	PXIe-4162
		LF Digitizer	PXIe-6368
23	VOUT	PINCARD D	PXIe-6571
		MEASURE MATRIX (DMM)	DMM4081
		LF Digitizer	PXIe-6368
24	VSENSE+	PINCARD D	PXIe-6571
		MEASURE MATRIX (DMM)	DMM4081
		LF Digitizer	PXIe-6368
25, 26, 27, 28	NC	PINCARD D	PXIe-6571
29	HW SELECT	PINCARD D	PXIe-6571
30	RESET	PINCARD D	PXIe-6571
31	FAULT/TEMP	PINCARD D	PXIe-6571
32	NC/IFAULT	PINCARD D	PXIe-6571
		MEASURE MATRIX (DMM)	DMM4081

7. Summary of Utilized NI STS GP3

Resource	Capability	# Channels Available in GP3	# Channels Required total	% Used
Source Measure Units				
PXIe-4137	±200V, 20W/1A max	8	8	100%
PXIe-4139	±60V, 20W/3A max	1	0	0%
PXIe-4147	±8V, 24W/3A max	4	0	0%
PXIe-4162	±24V@100mA	36	12	33.33%
PXIe-4163	±24V@50mA	72	0	0%
Programmable Power Supplies				
PXI - 4110	6 V/20 V/-20 V, 1 A/20 mA	3 Channels (1 set of each)	TBD	TBD
Auxiliary Power Supplies				
12 V, 12 A		1 Channel	TBD	TBD
20 V, 6 A		2 Channels	TBD	TBD
48V, 3 A		1 Channel	TBD	TBD
Digital Multimeter				
PXIe-4081	7.5 digit, ±60 VDC, ±3 A, 1.8 MS/s	4 Channels	4	100%
Oscilloscope				
PXIe-5172	100MHz,14-Bit, 50/1M Ohm, 80Vpp, Oscilloscope	8	0	0%
Multifunction I/O				
PXIe-6368	AI (±10 V, 2 MS/s/ch), AO (±10 V, 3.3 MS/s), DIO	16 AI 4 AO 48 DIO	16(Al) 4(AO)	100% 100%
Precision AC Source				
PXIe-4467	24 bits	2	0	0%
Digital Pattern				
PXIe-6571	128M Vectors LVM, 100 MVectors/s, -2 V to 6 V	160 Channels	100	62.5%
Relay Driver				
PXI - 2567	50 VDC, 600 mA/ch, 10 A/block, 60 µs	64 Channels	TBD	TBD
Synchronization				
PXIe-6674T	OCXO, ±1 PPM	2 CLKIN 2 CLKOUT 12 PFI	0%	0%

8. Assessment

Based on a preliminary evaluation of the schematic and device requirements, it is evident that the resource capabilities of STS GP3 align with the necessary specifications for conducting tests on AD5750 on four sites. Adequate sources are available to achieve the required voltage or current ranges for this device with the capabilities of the NI STS Instruments, migrating the AD5750 from CTS5400 to STS GP3 is feasible.

9. Stakeholder Approval Required

Technical council approval	Name of Approver	Signature of Approver
Product Line		
Capacity Planning		
Cost Representative		
Development Engineer		
Central Applications Group		
ADGT Clearing House		