Ewen Crawford

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EDUCATION

Queen's University Expected Graduation: April 2024
Bachelor of Applied Science, Computer Engineering

- Coursework: Digital Design, Computer Networks, Data Structures, Signals and Systems

WORK EXPERIENCE

Trend Micro – Vulnerability Research Intern May 2022 – Aug. 2022

- Developed a practical understanding of vulnerability research concepts such as network protocol structures, memory buffer overflows, and reverse engineering.
- Authored reports for 0-day and N-day security flaws, which included creating functional proof-of-concepts to demonstrate attacks on the reported vulnerabilities.
- Produced regex-based network filters for use as attack detection guidance by vendors.
- Worked with colleagues to improve the learning resources for future internship terms.

PROJECTS

FPGA Lava Lamp Aug. 2022 – Jan. 2023

- Designed a digital replica of a lava lamp on a Xilinx Artix-7 FPGA using SystemVerilog.
- Implemented the metaball algorithm in hardware with fixed-point arithmetic to describe simulation behaviour.
- Wrote a display controller to drive an LED matrix panel with the simulation output.
- Code and demonstration available at *https://github.com/eacrawford02/lava-lamp*

Meal Planner App May 2021 – June 2022

- A simple Android app for planning meals and indexing recipes.
- Written in Dart using the Flutter mobile framework for UI and an SQLite API for data storage.
- Code available at *https://github.com/eacrawford02/meal-planner-app/tree/develop*

OpenJGE2D – Open-Source Game Engine May 2019 – Jan. 2020

- Designed and implemented a rudimentary 2D game engine, consisting of core facilities, a multithreaded scheduler, and a rendering system.
- Written in Java using a wrapper for the OpenGL API.
- Documentation available at *https://openjge.github.io/OpenJGE2D-Website/*

SKILLS & INTERESTS

Technologies: Vivado, OpenGL, Git, SQL, HTML & CSS, Linux

Languages: C/C++, Verilog/SystemVerilog, Python, Java, Dart, x86 Assembly, Tcl

Interests: FPGAs, graphics programming, applied probability, reverse engineering