Ewen Crawford

eacrawford02@gmail.com
416-278-9886
www.ewencrawford.com

EDUCATION

Queen's University Expected Graduation: April 2024
Bachelor of Applied Science, Computer Engineering

- Coursework: Digital Design, Computer Networks, Data Structures, Signals and Systems.

WORK EXPERIENCE

Marvell – Design Verification Intern May 2023 – Present

- Working alongside Marvell's Ethernet IP division to further support implementation of the IEEE 802.1AE (MACsec) standard.
- Responsible for verifying a low-latency statistics engine used to provide general channelized accounting across large counter domains.
- Leveraged formal verification methodologies to exhaustively prove design correctness against a reference model.

Trend Micro – Vulnerability Research Intern May 2022 – Aug. 2022

- Developed a practical understanding of vulnerability research concepts such as network protocol structures, memory buffer overflows, and reverse engineering.
- Authored reports for 0-day and N-day security flaws, which included creating functional proof-of-concepts to demonstrate attacks on the reported vulnerabilities.
- Produced regex-based network filters for use as attack detection guidance by vendors.
- Worked with colleagues to improve the learning resources for future intern cohorts.

PROJECTS

Ethernet MAC July 2023 – Present

- Currently working on a SystemVerilog implementation of an IEEE 802.3 compliant MAC.
- Designed and verified an asynchronous FIFO to cross data between L3 and L2 clock domains.
- Code available at *https://github.com/eacrawford02/eth-mac*

FPGA Lava Lamp Aug. 2022 – Mar. 2023

- Designed a digital replica of a lava lamp on a Xilinx Artix-7 FPGA using SystemVerilog.
- Implemented the metaball algorithm in hardware with fixed-point arithmetic to describe simulation behaviour.
- Wrote a display controller to drive an LED matrix panel with the simulation output.
- Code and demonstration available at *https://github.com/eacrawford02/lava-lamp*

SKILLS & INTERESTS

Technologies: Vivado, Cadence JasperGold, Git, SQL, HTML & CSS, Linux

Languages: Verilog/SystemVerilog, C/C++, Python, Java, Dart, Tcl

Interests: FPGAs, graphics programming, applied probability, reverse engineering