

Ultra-Small, Ultra-Low Power MEMS Oscillator

Features

- Wide Frequency Range: 2 kHz to 100 MHz
- Ultra-Low Power Consumption: 3 mA/12 μ A (Active/Standby)
- Ultra-Small Footprints
 - 1.6 mm \times 1.2 mm
 - 2.0 mm \times 1.6 mm
 - 2.5 mm \times 2.0 mm
 - 3.2 mm \times 2.5 mm
- Frequency Select Input Supports Two Pre-Defined Frequencies
- High Stability: ± 25 ppm, ± 50 ppm
- Wide Temperature Range
 - Industrial: -40°C to 85°C
 - Ext. Commercial: -20° to 70°C
- Excellent Shock and Vibration Immunity
 - Qualified to MIL-STD-883
- High Reliability
 - 20x Better MTF Than Quartz Oscillators
- Supply Range of 1.71V to 3.63V
- Short Sample Lead Time: <2 weeks
- Lead Free & RoHS Compliant

Applications

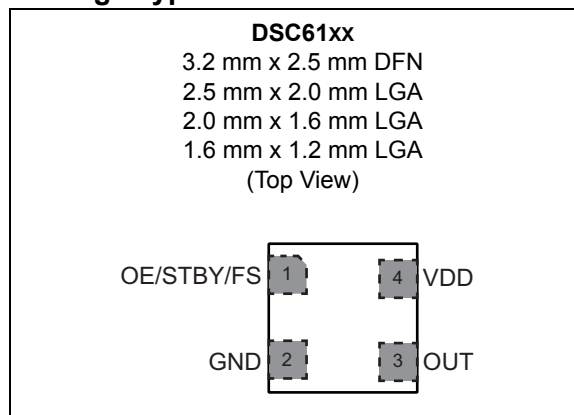
- Low Power/Portable Applications: IoT, Embedded/Smart Devices
- Consumer: Home Healthcare, Fitness Devices, Home Automation
- Automotive: Rear View/Surround View Cameras, Infotainment System
- Industrial: Building/Factory Automation, Surveillance Camera

General Description

The DSC61xx family of MEMS oscillators combines the industry leading low power consumption and ultra-small packages with exceptional frequency stability and jitter performance over temperature. The single-output DSC61xx MEMS oscillators are excellent choices for use as clock references in small, battery-powered devices such as wearable and Internet of Things (IoT) devices in which small size, low power consumption, and long-term reliability are paramount. They also meet the stringent mechanical durability and reliability requirements within Automotive Electronics Council standard Q100 (AEC-Q100), so they are well suited for under-hood applications as well.

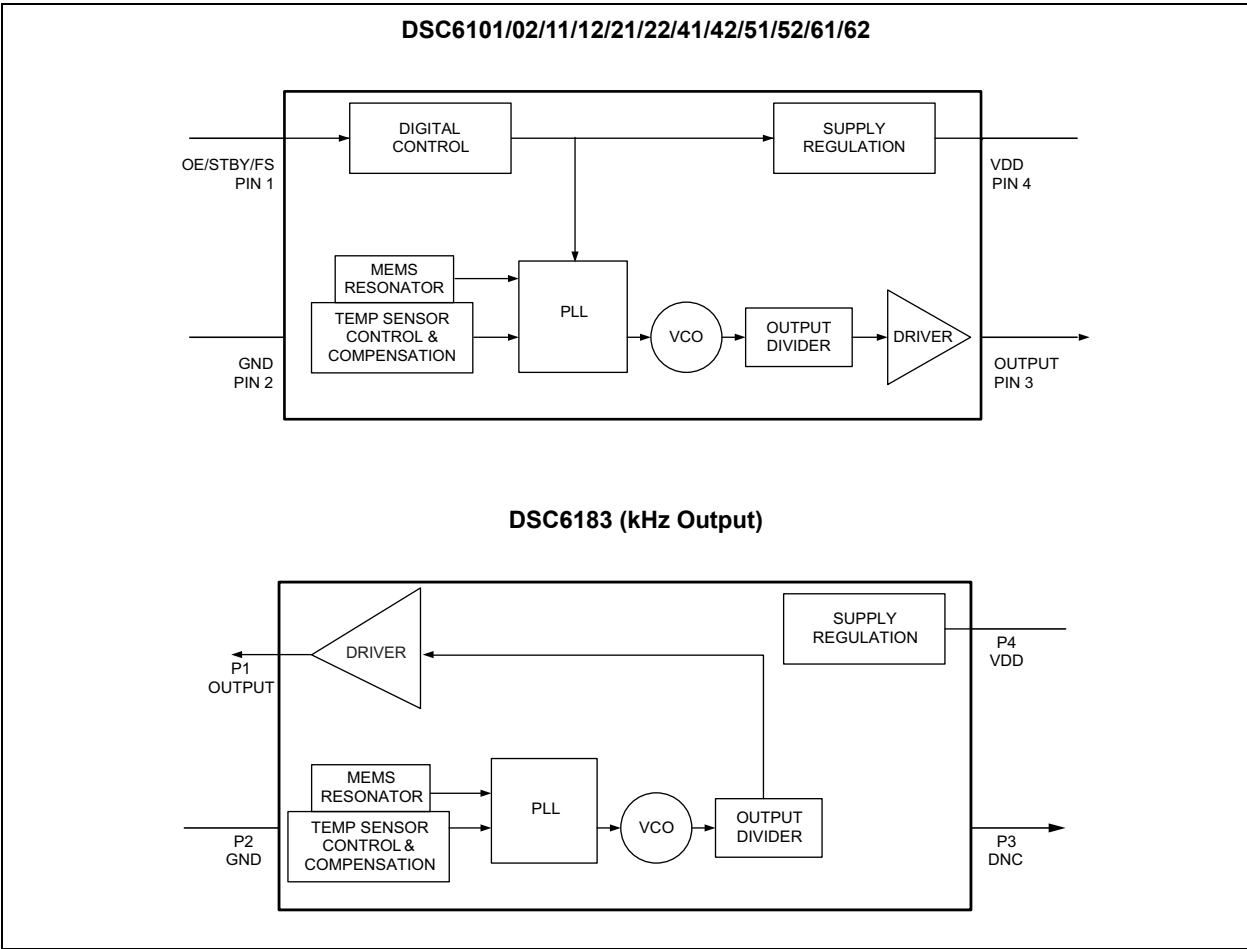
The DSC61xx family is available in ultra-small 1.6 mm \times 1.2 mm and 2.0 mm \times 1.6 mm packages. Other package sizes include: 2.5 mm \times 2.0 mm and 3.2 mm \times 2.5 mm. These packages are “drop-in” replacements for standard 4-pin CMOS quartz crystal oscillators.

Package Types



DSC61XX

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

| | |
|----------------------------------|-----------------------------|
| Supply Voltage | –0.3V to +4.0V |
| Input Voltage (V_{IN}) | –0.3V to $V_{DD}+0.3V$ |
| ESD Protection | 4 kV HBM, 400V MM, 2 kV CDM |

ELECTRICAL CHARACTERISTICS

| Electrical Characteristics: Unless otherwise indicated, $V_{DD} = 1.8V -5\%$ to $3.3V +10\%$, $T_A = -40^{\circ}C$ to $85^{\circ}C$. | | | | | | |
|---|------------|---------------------|------|----------------------|------------|--|
| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
| Supply Voltage, Note 1 | V_{DD} | 1.71 | — | 3.63 | V | — |
| Power Supply Ramp | t_{PU} | 0.1 | — | 100 | ms | Note 8 |
| Active Supply Current | I_{DD} | — | 3.0 | — | mA | $F_{OUT} = 27\text{ MHz}$, $V_{DD} = 1.8V$, No Load |
| Standby Supply Current Note 2 | I_{STBY} | — | 12 | — | μA | $V_{DD} = 1.8/2.5V$ |
| | | — | 80 | — | | $V_{DD} = 3.3V$ |
| Frequency Stability Note 3 | Δf | — | — | ± 25 ± 50 | ppm | All temp ranges |
| Aging | Δf | — | — | ± 5 | ppm | 1st year @ $25^{\circ}C$ |
| | | — | — | ± 1 | | Per year after first year |
| Startup Time | t_{SU} | — | — | 1.3 | ms | From 90% V_{DD} to valid clock output, $T = 25^{\circ}C$ |
| Input Logic Levels Note 4 | V_{IH} | $0.7 \times V_{DD}$ | — | — | V | Input Logic High |
| | V_{IL} | — | — | $0.3 \times V_{DD}$ | V | Input Logic Low |
| Output Disable Time Note 5 | t_{DA} | — | — | 200+Period | ns | — |
| Output Enable Time Note 6 | t_{EN} | — | — | 1 | μs | — |
| Enable Pull-up Resistor Note 7 | — | — | 300 | — | k Ω | If configured |
| Output Logic Levels | V_{OH} | $0.8 \times V_{DD}$ | — | — | V | Output Logic High, $I = 3\text{ mA}$, Std. Drive |
| | | | | | | Output Logic High, $I = 6\text{ mA}$, High Drive |
| | V_{OL} | — | — | $0.2 \times V_{DD}$ | V | Output Logic Low, $I = -3\text{ mA}$, Std. Drive |
| | | | | | | Output Logic Low, $I = -3\text{ mA}$, High Drive |

- Note 1:** Pin 4 V_{DD} should be filtered with 0.1 μF capacitor.
- 2:** Not including current through pull-up resistor on EN pin (if configured). Higher standby current seen at $>3.3V V_{DD}$.
- 3:** Includes frequency variations due to initial tolerance, temp. and power supply voltage.
- 4:** Input waveform must be monotonic with rise/fall time $< 10\text{ ms}$
- 5:** Output Disable time takes up to one period of the output waveform + 200 ns.
- 6:** For parts configured with OE, not Standby.
- 7:** Output is enabled if pad is floated or not connected.
- 8:** Time to reach 90% of target V_{DD} . Power ramp rise must be monotonic.

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ELECTRICAL CHARACTERISTICS (CONTINUED)

| Electrical Characteristics: Unless otherwise indicated, $V_{DD} = 1.8V -5\%$ to $3.3V +10\%$, $T_A = -40^{\circ}C$ to $85^{\circ}C$. | | | | | | | |
|--|-----------------|-------|------|------|------------|---|----------------------|
| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions | |
| Output Transition Time Rise Time/Fall Time | t_{RX}/t_{FX} | — | 1 | 1.5 | ns | DSC61x2 High Drive, 20% to 80% $C_L = 15$ pF | $V_{DD} = 1.8V$ |
| | | — | 0.5 | 1.0 | ns | | $V_{DD} = 2.5V/3.3V$ |
| | t_{RY}/t_{FY} | — | 1.2 | 2.0 | ns | DSC61x1 Std Drive, 20% to 80% $C_L = 10$ pF | $V_{DD} = 1.8V$ |
| | | — | 1.5 | 2.2 | ns | | $V_{DD} = 2.5V/3.3V$ |
| Frequency | f_0 | 0.002 | — | 100 | MHz | Output on Pin 1 for < 1 MHz | |
| Output Duty Cycle | SYM | 45 | — | 55 | % | — | |
| Period Jitter, RMS | J_{PER} | — | 9.5 | 11 | ps_{RMS} | $F_{OUT} = 27$ MHz | $V_{DD} = 1.8V$ |
| | | — | 7.5 | 9 | | | $V_{DD} = 2.5V/3.3V$ |
| Cycle-to-Cycle Jitter (peak) | J_{Cy-Cy} | — | 50 | 70 | ps | $F_{OUT} = 27$ MHz | $V_{DD} = 1.8V$ |
| | | — | 35 | 60 | | | $V_{DD} = 2.5V/3.3V$ |

- Note 1:** Pin 4 V_{DD} should be filtered with 0.1 μF capacitor.
- 2:** Not including current through pull-up resistor on EN pin (if configured). Higher standby current seen at $>3.3V$ V_{DD} .
- 3:** Includes frequency variations due to initial tolerance, temp. and power supply voltage.
- 4:** Input waveform must be monotonic with rise/fall time < 10 ms
- 5:** Output Disable time takes up to one period of the output waveform + 200 ns.
- 6:** For parts configured with OE, not Standby.
- 7:** Output is enabled if pad is floated or not connected.
- 8:** Time to reach 90% of target V_{DD} . Power ramp rise must be monotonic.

TEMPERATURE SPECIFICATIONS (Note 1)

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|-----------------------------------|-------|------|------|------|-------|---------------------|
| Temperature Ranges | | | | | | |
| Junction Operating Temperature | T_J | — | — | +150 | °C | — |
| Ambient Operating Temperature | T_A | −40 | — | +85 | °C | Industrial |
| Ambient Operating Temperature | T_A | −20 | — | +70 | °C | Extended Commercial |
| Storage Ambient Temperature Range | T_A | −55 | — | +150 | °C | — |
| Soldering Temperature | T_S | — | +260 | — | °C | 40 sec. max. |

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A , T_J , θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +150°C rating. Sustained junction temperatures above +150°C can impact the device reliability.

DSC61XX

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 2-1](#) and [Table 2-2](#).

TABLE 2-1: DSC6101/02/11/12/21/22/41/42/51/52/61/62 PIN FUNCTION TABLE (OUTPUT FREQUENCY ≥ 1 MHZ)

| Pin Number | Pin Name | Pin Type | Description |
|------------|----------|----------|---|
| 1 | OE | I | Output Enable: H = Specified Frequency Output, Note 1 L = Output is high impedance |
| | STBY | | Standby: H = Specified Frequency Output, Note 1 L = Output is high impedance. Device is in low power mode, supply current is at I_{STBY} |
| | FS | | Frequency Select: H = Output Frequency 1, Note 2 L = Output Frequency 2 |
| 2 | GND | Power | Power supply ground |
| 3 | Output | O | Oscillator clock output |
| 4 | VDD | Power | Power supply |

Note 1: DSC610x/1x/2x has 300 k Ω internal pull-up resistor on pin1. DSC614x/5x/6x has no internal pull-up resistor on pin1 and needs external pull-up or being driven by other chip.

2: Two pre-programmed frequencies can be configured at <http://clockworks.microchip.com/timing/>

3: Bypass with 0.1 μ F capacitor placed as close to V_{DD} pin as possible.

TABLE 2-2: DSC6183 PIN FUNCTION TABLE (OUTPUT FREQUENCY < 1 MHZ)

| Pin Number | Pin Name | Pin Type | Description |
|------------|----------|----------|--------------------------------------|
| 1 | Output | O | Kilohertz Oscillator clock output |
| 2 | GND | Power | Power supply ground |
| 3 | DNC | DNC | Do Not Connect |
| 4 | VDD | Power | Power supply, Note 1 |

Note 1: Bypass with 0.1 μ F capacitor placed as close to V_{DD} pin as possible.

2.1 Output Buffer Options

DSC61xx family is available in multiple output driver configurations.

The standard-drive (61x1) and high-drive (61x2) deliver respective output currents of greater than 3 mA and 6 mA at 20%/80% of the supply voltage. For heavy loads of 15 pF or higher, the high-drive option is recommended.

3.0 DIAGRAMS

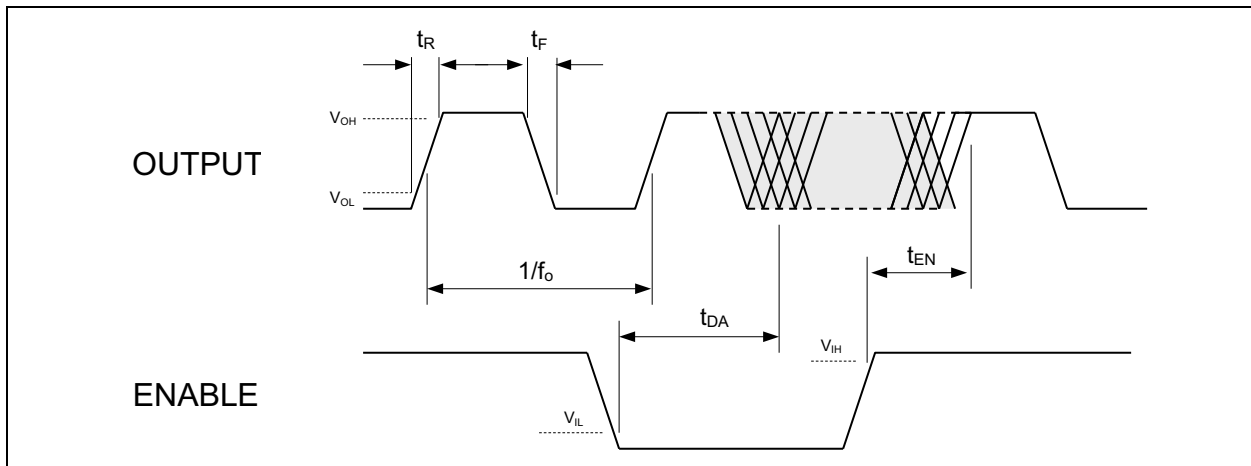


FIGURE 3-1: Output Waveform.

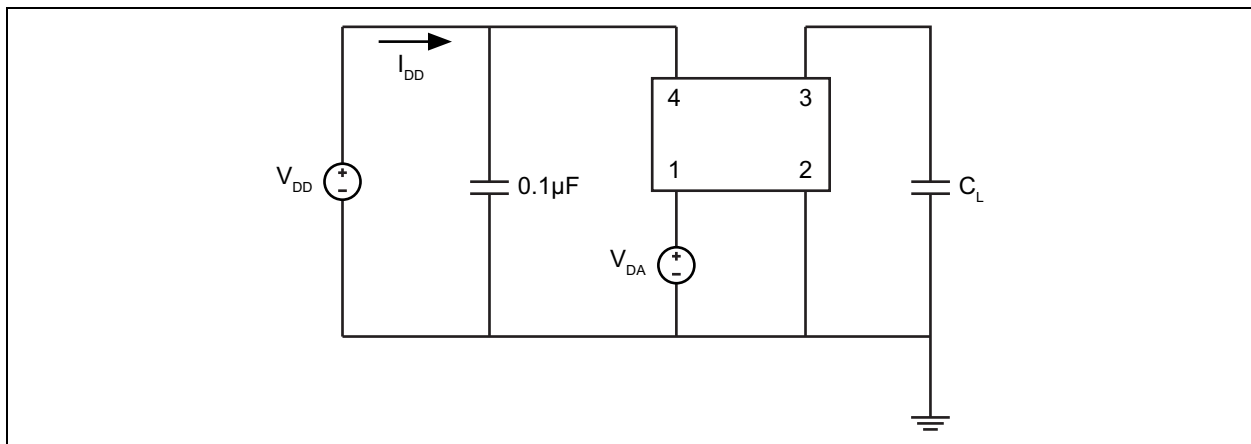


FIGURE 3-2: Test Circuit.

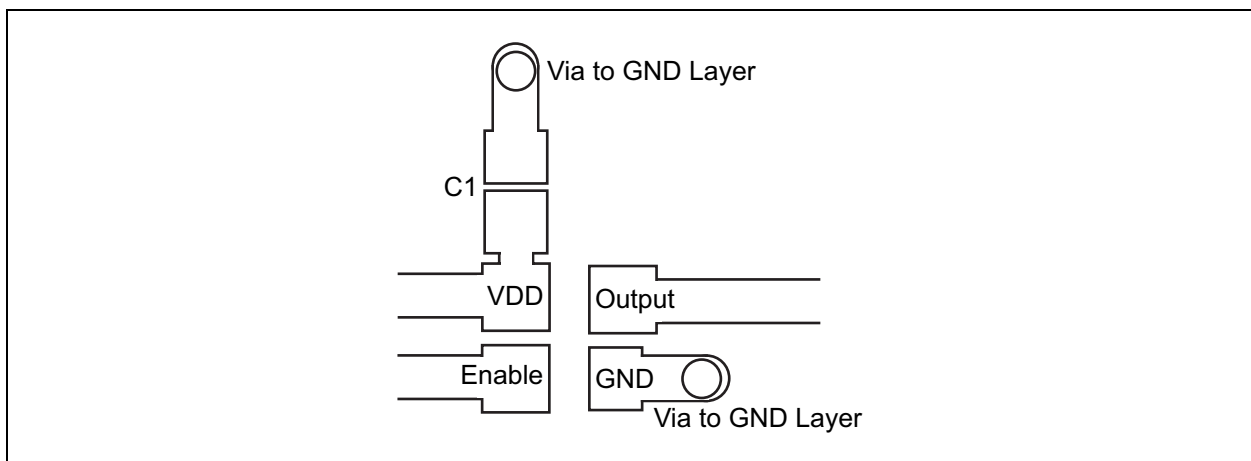


FIGURE 3-3: Recommended Board Layout.

4.0 SOLDER REFLOW PROFILE

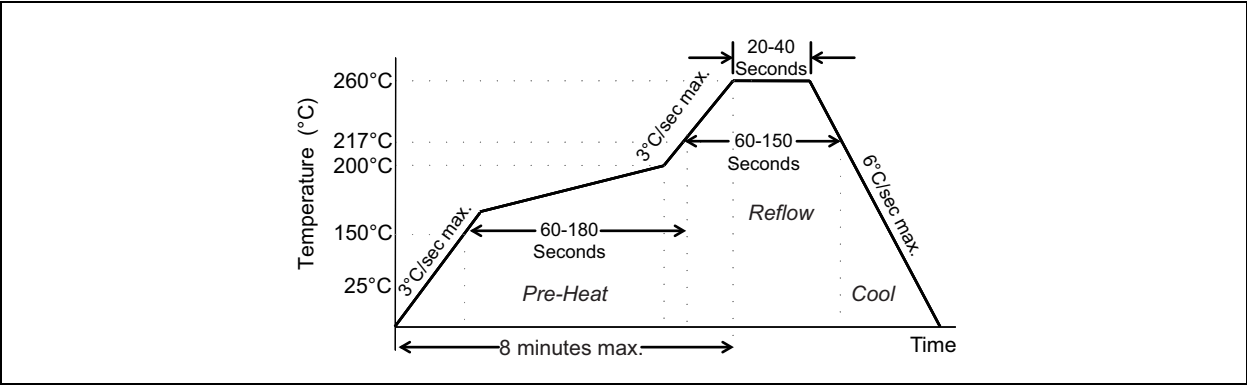


FIGURE 4-1: Solder Reflow Profile.

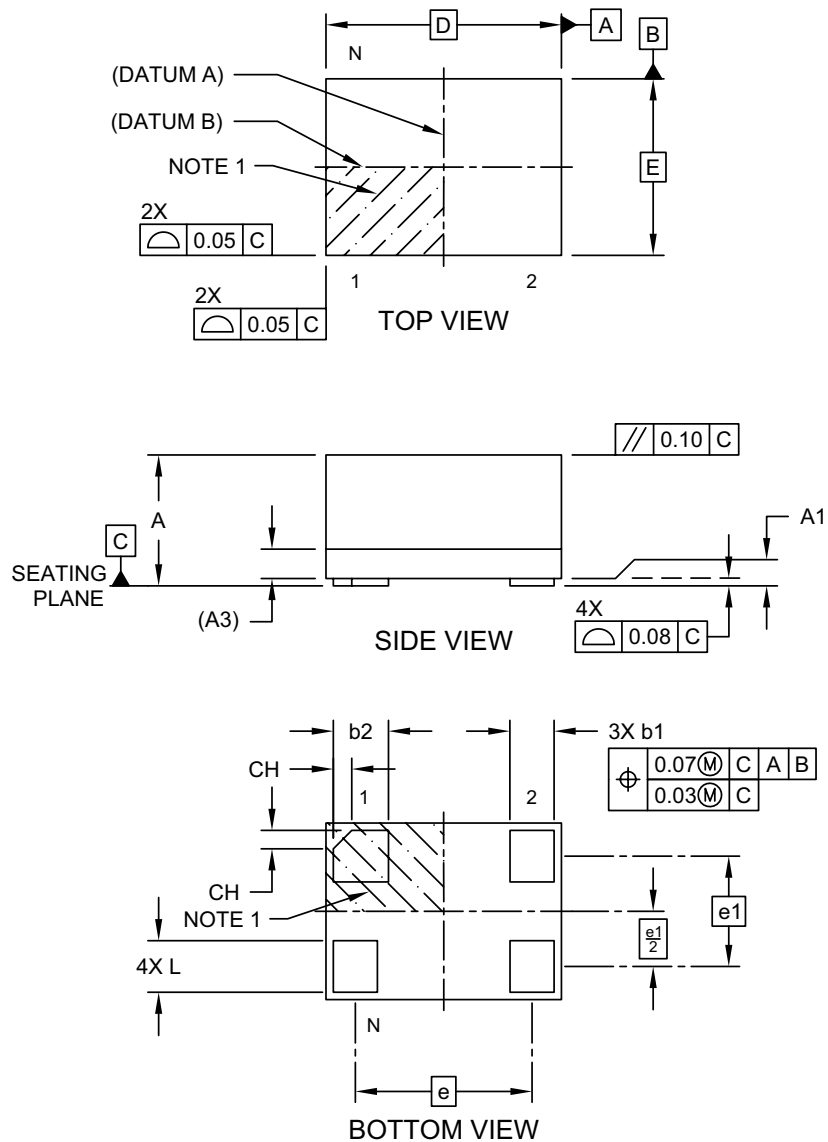
| MSL 1 @ 260°C refer to JSTD-020C | |
|-----------------------------------|----------------|
| Ramp-Up Rate (200°C to Peak Temp) | 3°C/sec. max. |
| Preheat Time 150°C to 200°C | 60 to 180 sec. |
| Time maintained above 217°C | 60 to 150 sec. |
| Peak Temperature | 255°C to 260°C |
| Time within 5°C of actual Peak | 20 to 40 sec. |
| Ramp-Down Rate | 6°C/sec. max. |
| Time 25°C to Peak Temperature | 8 minutes max. |

5.0 PACKAGING INFORMATION

4-Lead VFLGA 1.6 mm x 1.2 mm Package Outline

4-Lead Very Thin Fine Pitch Land Grid Array (ARA) - 1.6x1.2 mm Body [VFLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

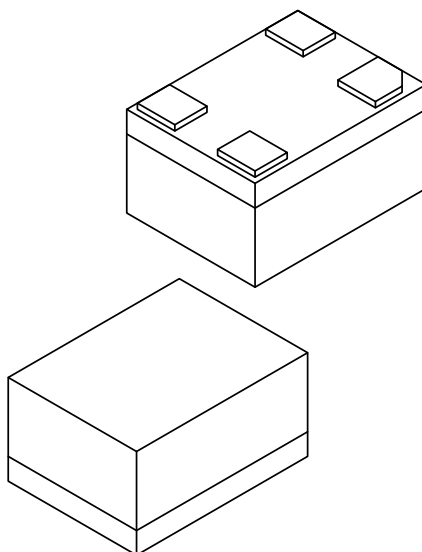


Microchip Technology Drawing C04-1199A Sheet 1 of 2

4-Lead VFLGA 1.6 mm x 1.2 mm Package Outline

4-Lead Very Thin Fine Pitch Land Grid Array (ARA) - 1.6x1.2 mm Body [VFLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Units | | MILLIMETERS | | |
|--------------------------------------|----|-------------|-------|-------|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | 4 | | |
| Terminal Pitch | e | 1.20 BSC | | |
| Terminal Pitch | e1 | 0.75 BSC | | |
| Overall Height | A | 0.79 | 0.84 | 0.89 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Substrate Thickness (with Terminals) | A3 | 0.20 REF | | |
| Overall Length | D | 1.60 BSC | | |
| Overall Width | E | 1.20 BSC | | |
| Terminal Width | b1 | 0.25 | 0.30 | 0.35 |
| Terminal Width | b2 | 0.325 | 0.375 | 0.425 |
| Terminal Length | L | 0.30 | 0.35 | 0.40 |
| Terminal 1 Index Chamfer | CH | - | 0.125 | - |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

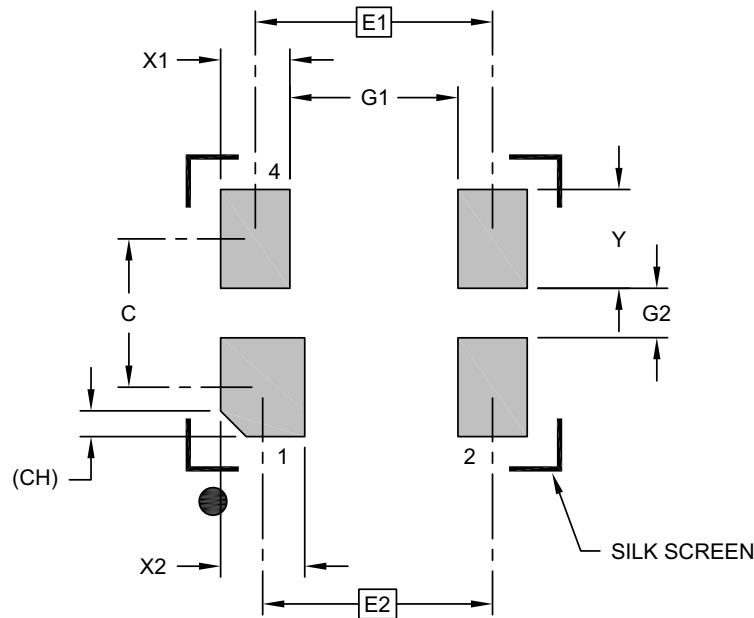
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1199A Sheet 2 of 2

4-Lead VFLGA 1.6 mm x 1.2 mm Recommended Land Pattern

4-Lead Very Thin Fine Pitch Land Grid Array (ARA) - 1.6x1.2 mm Body [VFLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Dimension Limits | Units | MILLIMETERS | | |
|-----------------------------|-------|----------------|----------|------|
| | | MIN | NOM | MAX |
| Contact Pitch | E1 | | 1.20 BSC | |
| Contact Pitch | E2 | | 1.16 BSC | |
| Contact Spacing | C | | 0.75 | |
| Contact Width (X3) | X1 | | | 0.35 |
| Contact Width | X2 | | | 0.43 |
| Contact Pad Length (X6) | Y | | | 0.50 |
| Space Between Contacts (X4) | G1 | 0.85 | | |
| Space Between Contacts (X3) | G2 | 0.25 | | |
| Contact 1 Index Chamfer | CH | 0.13 X 45° REF | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

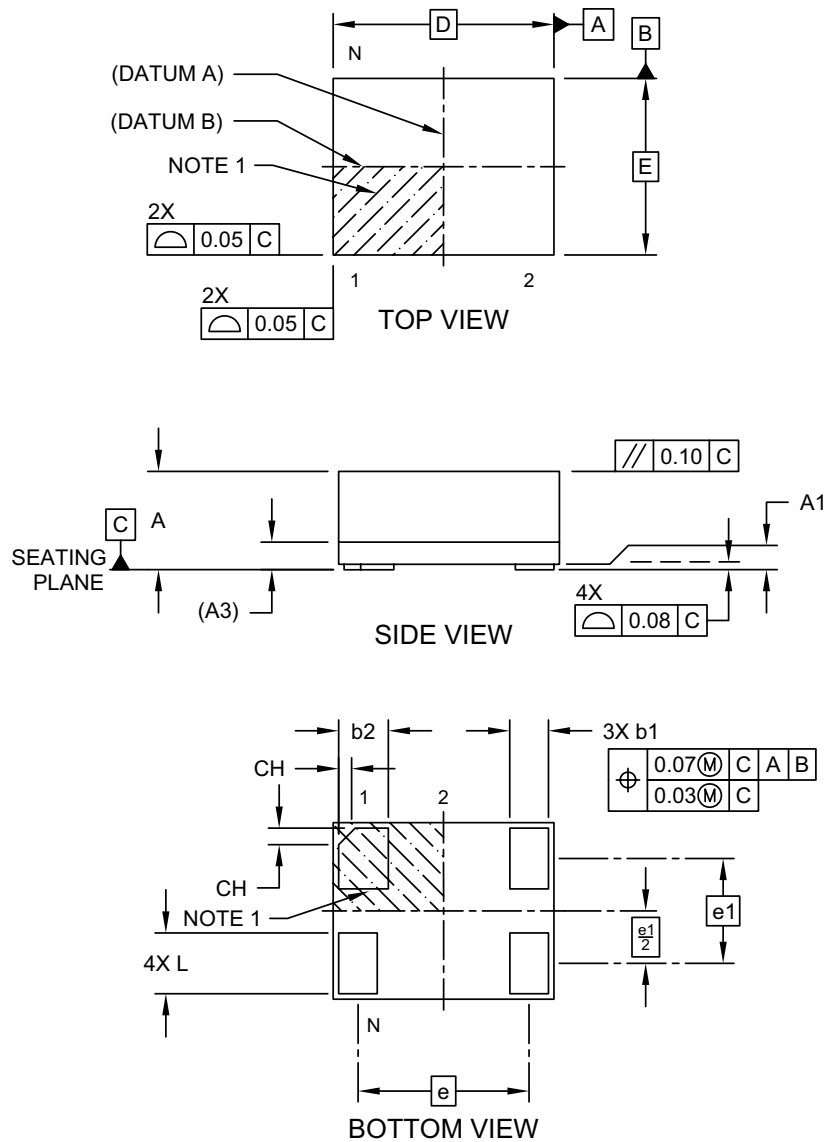
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3199A

4-Lead VFLGA 2.0 mm x 1.6 mm Package Outline

4-Lead Very Thin Fine Pitch Land Grid Array (ASA) - 2.0x1.6 mm Body [VFLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

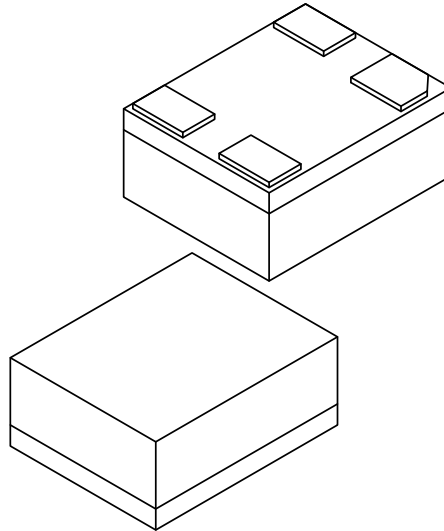


Microchip Technology Drawing C04-1200A Sheet 1 of 2

4-Lead VFLGA 2.0 mm x 1.6 mm Package Outline

4-Lead Very Thin Fine Pitch Land Grid Array (ASA) - 2.0x1.6 mm Body [VFLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Units | | MILLIMETERS | | |
|--------------------------------------|----|-------------|------|------|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | 6 | | |
| Terminal Pitch | e | 1.55 BSC | | |
| Terminal Pitch | e1 | 0.95 BSC | | |
| Overall Height | A | 0.79 | 0.84 | 0.89 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Substrate Thickness (with Terminals) | A3 | 0.20 REF | | |
| Overall Length | D | 2.00 BSC | | |
| Overall Width | E | 1.60 BSC | | |
| Terminal Width | b1 | 0.30 | 0.35 | 0.40 |
| Terminal Width | b2 | 0.40 | 0.45 | 0.50 |
| Terminal Length | L | 0.50 | 0.55 | 0.60 |
| Terminal 1 Index Chamfer | CH | - | 0.15 | - |

Notes:

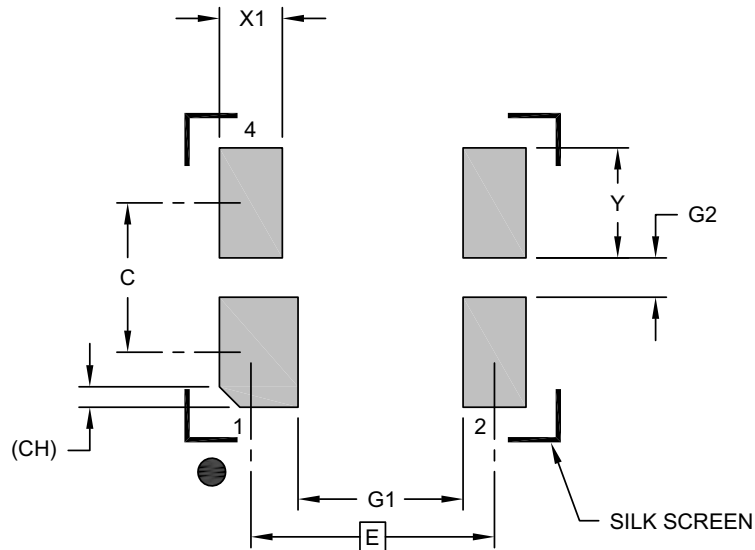
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1200A Sheet 2 of 2

4-Lead VFLGA 2.0 mm x 1.6 mm Package Outline

4-Lead Very Thin Fine Pitch Land Grid Array (ASA) - 2.0x1.6 mm Body [VFLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|-----------------------------|----|----------------|------|------|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 1.55 BSC | | |
| Contact Spacing | C | | 0.95 | |
| Contact Width (X4) | X1 | | | 0.50 |
| Contact Width (X2) | X2 | | | 0.40 |
| Contact Pad Length (X6) | Y | | | 0.70 |
| Space Between Contacts (X4) | G1 | 1.05 | | |
| Space Between Contacts (X3) | G2 | 0.25 | | |
| Contact 1 Index Chamfer | CH | 0.13 X 45° REF | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

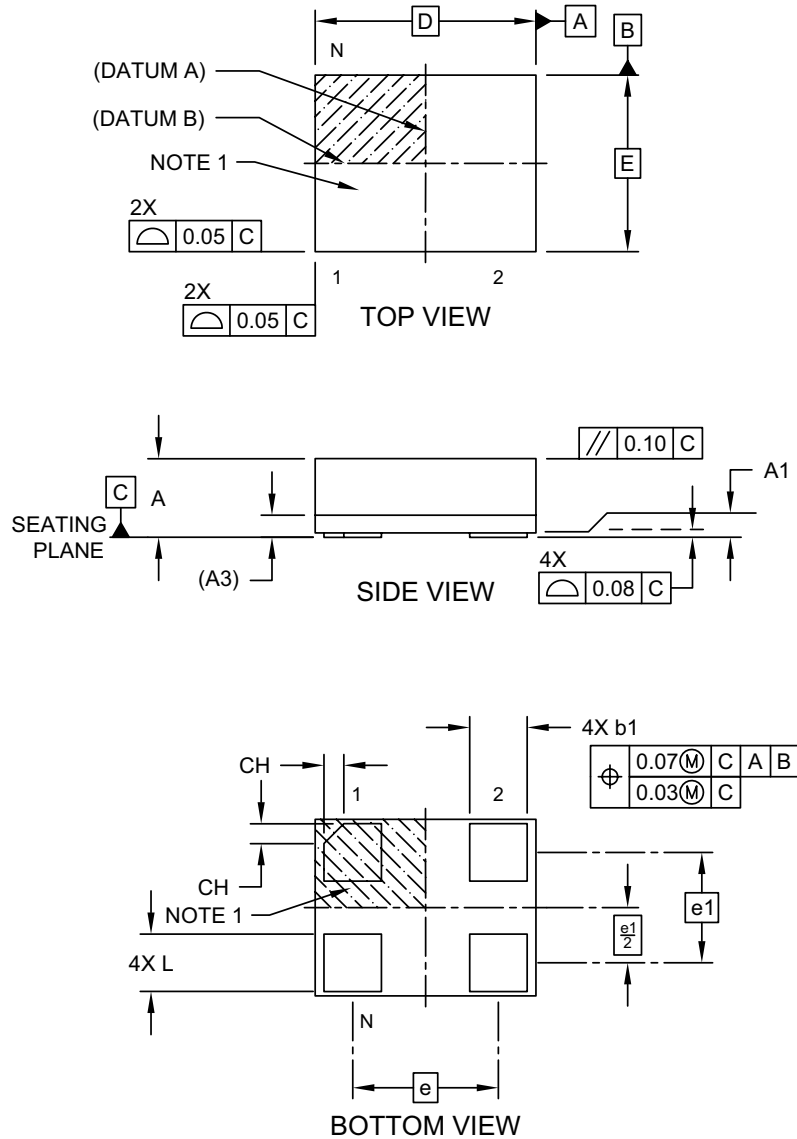
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3200A

4-Lead VLGA 2.5 mm x 2.0 mm Package Outline

4-Lead Very Thin Land Grid Array (AUA) - 2.5x2.0 mm Body [VLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

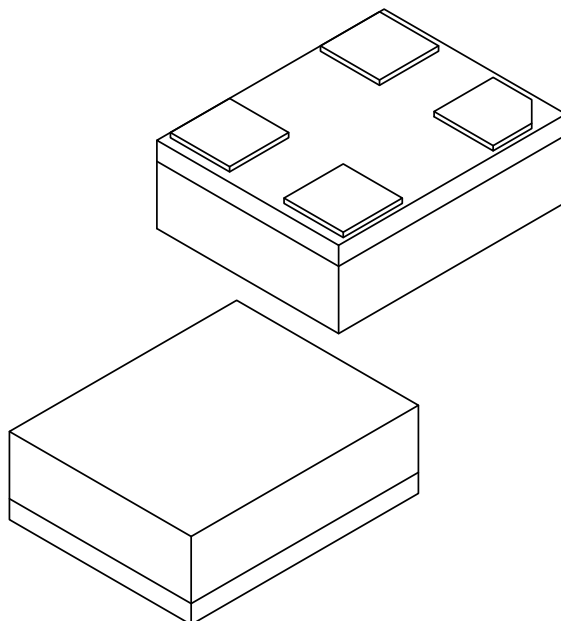


Microchip Technology Drawing C04-1202A Sheet 1 of 2

4-Lead VLGA 2.5 mm x 2.0 mm Package Outline

4-Lead Very Thin Land Grid Array (AUA) - 2.5x2.0 mm Body [VLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Units | | MILLIMETERS | | |
|--------------------------------------|----|-------------|-------|------|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | 4 | | |
| Terminal Pitch | e | 1.65 BSC | | |
| Terminal Pitch | e1 | 1.25 BSC | | |
| Overall Height | A | 0.79 | 0.84 | 0.89 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Substrate Thickness (with Terminals) | A3 | 0.20 REF | | |
| Overall Length | D | 2.50 BSC | | |
| Overall Width | E | 2.00 BSC | | |
| Terminal Width | b1 | 0.60 | 0.65 | 0.70 |
| Terminal Length | L | 0.60 | 0.65 | 0.70 |
| Terminal 1 Index Chamfer | CH | - | 0.225 | - |

Notes:

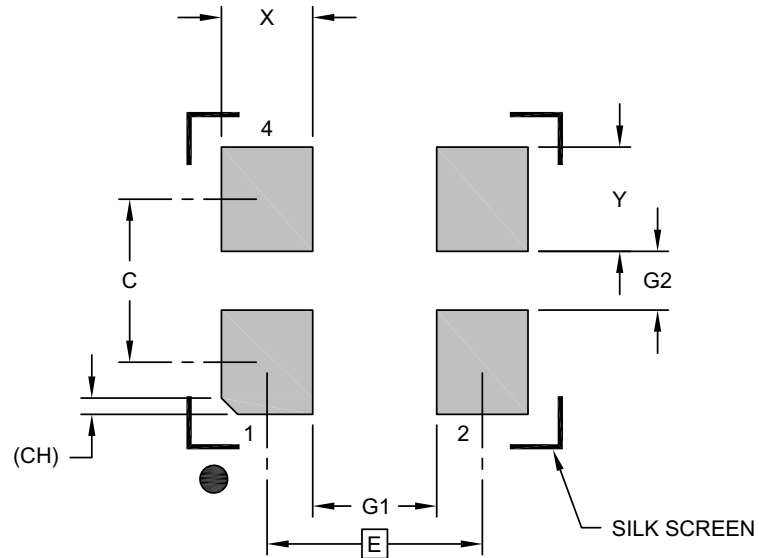
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1202A Sheet 2 of 2

4-Lead VLGA 2.5 mm x 2.0 mm Recommended Land Pattern

4-Lead Very Thin Land Grid Array (AUA) - 2.5x2.0 mm Body [VLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|-----------------------------|----|----------------|------|------|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 1.65 BSC | | |
| Contact Spacing | C | | 1.25 | |
| Contact Width (X4) | X | | | 0.70 |
| Contact Pad Length (X6) | Y | | | 0.80 |
| Space Between Contacts (X4) | G1 | 0.95 | | |
| Space Between Contacts (X3) | G2 | 0.45 | | |
| Contact 1 Index Chamfer | CH | 0.13 X 45° REF | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3202A

DSC61XX

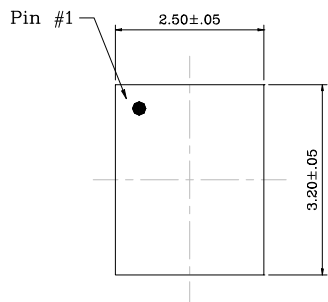
4-Lead CDFN 3.2 mm x 2.5 mm Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

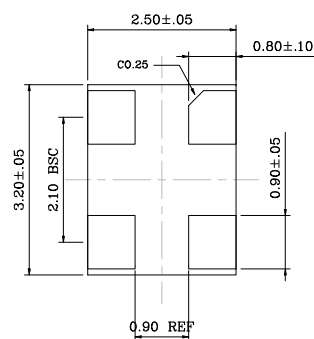
TITLE

4 LEAD CDFN 3.2x2.5mm COL PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

| DRAWING # | CDFN3225-4LD-PL-1 | UNIT | MM |
|-----------|-------------------|------|----|
|-----------|-------------------|------|----|



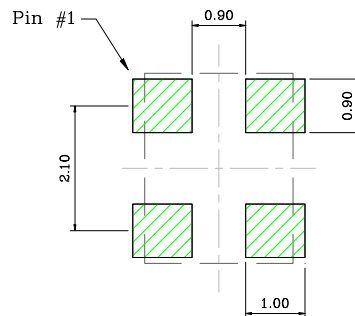
Top View



Bottom View



Side View



Recommended Land Pattern

NOTE:

1. Green shaded rectangles in Recommended Land Pattern are solder stencil opening.

APPENDIX A: REVISION HISTORY

Revision A (September 2016)

- Initial release of DSC61xx Microchip data sheet DS20005624A.

Revision B (September 2017)

- Added Power Supply Ramp value in [Electrical Characteristics](#) table.
- Redrew diagrams for clarity. No technical content affected.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO. X X X X X X - XXX.XXXX X
 Device Pin 1 Output Package Temperature Frequency Revision Frequency Tape
 Definition Drive Strength Range Stability and Reel

| | | |
|-------------------------------|------------------|--|
| Device: | DSC61xx: | Ultra-Low Power MEMS Oscillator |
| Pin Definition: | Selection | Pin 1 Internal Pull-Up Register |
| | 0 | OE Pull-up |
| | 1 | STBY Pull-up |
| | 2 | FS Pull-up |
| | 4 | OE None |
| | 5 | STBY None |
| | 6 | FS None |
| | 8 | kHz None |
| | | Output |
| Output Drive Strength: | 1 | Standard |
| | 2 | High |
| Packages: | C | = 4-Lead 3.2 mm x 2.5 mm DFN |
| | J | = 4-Lead 2.5 mm x 2.0 mm VLGA |
| | M | = 4-Lead 2.0 mm x 1.6 mm VFLGA |
| | H | = 4-Lead 1.6 mm x 1.2 mm VFLGA |
| Temperature Range: | E | = -20°C to +70°C (Extended Commercial) |
| | I | = -40°C to +85°C (Industrial) |
| Frequency Stability: | 1 | = ± 50 ppm |
| | 2 | = ± 25 ppm |
| Revision: | A | = Revision A |
| Frequency: | xxx.xxxx | = User-Defined Frequency between 001.0000 MHz and 100.0000 MHz |
| | xxxkxxx | = User-Defined Frequency between 002.000 kHz and 999.999 kHz |
| | xxxx | = Frequency configuration code when pin 1 = FS. Configure the part online through ClockWorks |
| Tape and Reel: | <blank> | = 100/Bag |
| | T | = 1,000/Reel |

Examples:

- a) DSC6112JI2A-100.0000:
 Ultra-Low Power MEMS Oscillator, Pin1 = Standby with Internal Pull-Up, High Drive Strength, 4-Lead 2.5 mm x 2.0 mm VLGA, Industrial Temperature, ±25 ppm Stability, Revision A, 100 MHz Frequency, 100/Bag
- b) DSC6101HE1A-016.0000T:
 Ultra-Low Power MEMS Oscillator, Pin1 = OE with Internal Pull-Up, Standard Drive Strength, 4-Lead 1.6 mm x 1.2 mm VFLGA, Extended Commercial Temp., ±50 ppm Stability, Revision A, 16 MHz Frequency, 1,000/Reel
- c) DSC6121MI2A-005Q:
 Ultra-Low Power MEMS Oscillator, Pin1 = Freq. Select with Internal Pull-Up, Standard Drive Strength, 4-Lead 2.0 mm x 1.6 mm VFLGA, Industrial Temperature, ±25 ppm Stability, Revision A, Two Frequencies Configured through ClockWorks, 100/Bag

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

Note 1: Please visit Microchip ClockWorks® Configurator Website to configure the part number for customized frequency. <http://clockworks.microchip.com/timing/>.

NOTES:

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ISBN: 978-1-5224-0961-8

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