instruction page	variant	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UNALLOCATED					**0**	**0**																											
Branch,exception generation and system Instruction					**1**	**0**	**1**																										
Compare & Branch (immediate)		**sf**	**0**	**1**	**1**	**0**	**1**	**0**	**op**	**imm19**																			**Rt**				
CBZ	32-bit	0	0	1	1	0	1	0	0	imm19																			Rt				
CBNZ	32-bit	0	0	1	1	0	1	0	1	imm19																			Rt				
CBZ	64-bit	1	0	1	1	0	1	0	0	imm19																			Rt				
CBNZ	64-bit	1	0	1	1	0	1	0	1	imm19																			Rt				
Test & branch (immediate)		**b5**	**0**	**1**	**1**	**0**	**1**	**1**	**op**	**b40**					**imm14**														**Rt**				
TBZ	-	b5	0	1	1	0	1	1	0	b40					imm14														Rt				
TBNZ	-	b5	0	1	1	0	1	1	1	b40					imm14														Rt				
Conditional branch (immediate)		**0**	**1**	**0**	**1**	**0**	**1**	**0**	**o1**	**imm19**																			**o0**	**cond**			
B.cond	-	0	1	0	1	0	1	0	0	imm19																			0	cond			
Exception generation		**1**	**1**	**0**	**1**	**0**	**1**	**0**	**0**	**opc**			**imm16**																**op2**		**LL**		
SVC	-	1	1	0	1	0	1	0	0	0	0	0	imm16																0	0	0	0	1
HVC	-	1	1	0	1	0	1	0	0	0	0	0	imm16																0	0	0	1	0
SMC	-	1	1	0	1	0	1	0	0	0	0	0	imm16																0	0	0	1	1
BRK	-	1	1	0	1	0	1	0	0	0	0	1	imm16																0	0	0	0	0
HLT	-	1	1	0	1	0	1	0	0	0	1	0	imm16																0	0	0	0	0
DCPS1	-	1	1	0	1	0	1	0	0	1	0	1	imm16																0	0	0	0	1
DCPS2	-	1	1	0	1	0	1	0	0	1	0	1	imm16																0	0	0	1	0
DCPS3	-	1	1	0	1	0	1	0	0	1	0	1	imm16																0	0	0	1	1
System		**1**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**0**	**L**	**op0**		**op1**			**CRn**				**CRm**				**op2**			**Rt**				
MSR(immediate)	-	1	1	0	1	0	1	0	1	0	0	0	0	0	op1			0	1	0	0	CR_m				op2			1	1	1	1	1
HINT	-	1	1	0	1	0	1	0	1	0	0	0	0	0	0	1	1	0	0	1	0	CR_m				op2			1	1	1	1	1
CLREX	-	1	1	0	1	0	1	0	1	0	0	0	0	0	0	1	1	0	0	1	1	CR_m			0	1	0		1	1	1	1	1
DSB	-	1	1	0	1	0	1	0	1	0	0	0	0	0	0	1	1	0	0	1	1	CR_m			1	0	0		1	1	1	1	1
DMB	-	1	1	0	1	0	1	0	1	0	0	0	0	0	0	1	1	0	0	1	1	CR_m			1	0	1		1	1	1	1	1
ISB	-	1	1	0	1	0	1	0	1	0	0	0	0	0	0	1	1	0	0	1	1	CR_m			1	1	0		1	1	1	1	1
SYS	-	1	1	0	1	0	1	0	1	0	0	0	0	1	op1			CR_n				CR_m				op2			Rt				
MSR(register)	-	1	1	0	1	0	1	0	1	0	0	0	1		op1			CR_n				CR_m				op2			Rt				
SYSL	-	1	1	0	1	0	1	0	1	0	0	1	0	1	op1			CR_n				CR_m				op2			Rt				
MRS	-	1	1	0	1	0	1	0	1	0	0	1	1		op1			CR_n				CR_m				op2			Rt				
Unconditional branch (register)		**1**	**1**	**0**	**1**	**0**	**1**	**1**	**opc**				**op2**					**op3**						**Rn**					**op4**				
BR	-	1	1	0	1	0	1	1	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	Rn					0	0	0	0	0
BLR	-	1	1	0	1	0	1	1	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	Rn					0	0	0	0	0
RET	-	1	1	0	1	0	1	1	0	0	1	0	1	1	1	1	1	0	0	0	0	0	0	Rn					0	0	0	0	0
ERET	-	1	1	0	1	0	1	1	0	1	0	0	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0
DRPS	-	1	1	0	1	0	1	1	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0
Unconditional branch (immediate)		**op**	**0**	**0**	**1**	**0**	**1**	**imm26**																									
B	-	0	0	0	1	0	1	imm26																									
BL	-	1	0	0	1	0	1	imm26																									
Loads and stores						**1**		**0**																									
Load/store exclusive		**size**		**0**	**0**	**1**	**0**	**0**	**0**	**o2**	**L**	**o1**	**Rs**					**o0**	**Rt2**					**Rn**					**Rt**				

instruction page	variant	31	30	29	28	27	26	25	24	23	22	21	20 19 18 17 16	15	14 13 12 11 10	9 8 7 6 5	4 3 2 1 0
STXRB	-	0	0	0	0	1	0	0	0	0	0	0	Rs	0	Rt2	Rn	Rt
STLXRB	-	0	0	0	0	1	0	0	0	0	0	0	Rs	1	Rt2	Rn	Rt
LDXRB	-	0	0	0	0	1	0	0	0	0	1	0	Rs	0	Rt2	Rn	Rt
LDAXRB	-	0	0	0	0	1	0	0	0	0	1	0	Rs	1	Rt2	Rn	Rt
STLRB	-	0	0	0	0	1	0	0	0	1	0	0	Rs	1	Rt2	Rn	Rt
LDARB	-	0	0	0	0	1	0	0	0	1	1	0	Rs	1	Rt2	Rn	Rt
STXRH	-	0	1	0	0	1	0	0	0	0	0	0	Rs	0	Rt2	Rn	Rt
STLXRH	-	0	1	0	0	1	0	0	0	0	0	0	Rs	1	Rt2	Rn	Rt
LDXRH	-	0	1	0	0	1	0	0	0	0	1	0	Rs	0	Rt2	Rn	Rt
LDAXRH	-	0	1	0	0	1	0	0	0	0	1	0	Rs	1	Rt2	Rn	Rt
STLRH	-	0	1	0	0	1	0	0	0	1	0	0	Rs	1	Rt2	Rn	Rt
LDARH	-	0	1	0	0	1	0	0	0	1	1	0	Rs	1	Rt2	Rn	Rt
STXR	32-bit	1	0	0	0	1	0	0	0	0	0	0	Rs	0	Rt2	Rn	Rt
STLXR	32-bit	1	0	0	0	1	0	0	0	0	0	0	Rs	1	Rt2	Rn	Rt
STXP	32-bit	1	0	0	0	1	0	0	0	0	0	1	Rs	0	Rt2	Rn	Rt
STLXP	32-bit	1	0	0	0	1	0	0	0	0	0	1	Rs	1	Rt2	Rn	Rt
LDXR	32-bit	1	0	0	0	1	0	0	0	0	1	0	Rs	0	Rt2	Rn	Rt
LDAXR	32-bit	1	0	0	0	1	0	0	0	0	1	0	Rs	1	Rt2	Rn	Rt
LDXP	32-bit	1	0	0	0	1	0	0	0	0	1	1	Rs	0	Rt2	Rn	Rt
LDAXP	32-bit	1	0	0	0	1	0	0	0	0	1	1	Rs	1	Rt2	Rn	Rt
STLR	32-bit	1	0	0	0	1	0	0	0	1	0	0	Rs	1	Rt2	Rn	Rt
LDAR	32-bit	1	0	0	0	1	0	0	0	1	1	0	Rs	1	Rt2	Rn	Rt
STXR	64-bit	1	1	0	0	1	0	0	0	0	0	0	Rs	0	Rt2	Rn	Rt
STLXR	64-bit	1	1	0	0	1	0	0	0	0	0	0	Rs	1	Rt2	Rn	Rt
STXP	64-bit	1	1	0	0	1	0	0	0	0	0	1	Rs	0	Rt2	Rn	Rt
STLXP	64-bit	1	1	0	0	1	0	0	0	0	0	1	Rs	1	Rt2	Rn	Rt
LDXR	64-bit	1	1	0	0	1	0	0	0	0	1	0	Rs	0	Rt2	Rn	Rt
LDAXR	64-bit	1	1	0	0	1	0	0	0	0	1	0	Rs	1	Rt2	Rn	Rt
LDXP	64-bit	1	1	0	0	1	0	0	0	0	1	1	Rs	0	Rt2	Rn	Rt
LDAXP	64-bit	1	1	0	0	1	0	0	0	0	1	1	Rs	1	Rt2	Rn	Rt
STLR	64-bit	1	1	0	0	1	0	0	0	1	0	0	Rs	1	Rt2	Rn	Rt
LDAR	64-bit	1	1	0	0	1	0	0	0	1	1	0	Rs	1	Rt2	Rn	Rt
Load register (literal)		**opc**		**0**	**1**	**1**	**V**	**0**	**0**					**imm19**			**Rt**
LDR(literal)	32-bit	0	0	0	1	1	0	0	0					imm19			Rt
LDR(literal,SIMD&FP)	32-bit	0	0	0	1	1	1	0	0					imm19			Rt
LDR(literal)	64-bit	0	1	0	1	1	0	0	0					imm19			Rt
LDR(literal,SIMD&FP)	64-bit	0	1	0	1	1	1	0	0					imm19			Rt
LDRSW(literal)	-	1	0	0	1	1	0	0	0					imm19			Rt
LDR(literal,SIMD&FP)	128-bit	1	0	0	1	1	1	0	0					imm19			Rt
PRFM(literal)	-	1	1	0	1	1	0	0	0					imm19			Rt
Load/store no-allocate pair (offset)		**opc**		**1**	**0**	**1**	**V**	**0**	**0**	**0**	**L**	**imm7**			**Rt2**	**Rn**	**Rt**
STNP	32-bit	0	0	1	0	1	0	0	0	0	0	imm7			Rt2	Rn	Rt

instruction page	variant	31	30	29	28	27	26	25	24	23	22	21 20 19 18 17 16 15	14 13 12 11 10	9 8 7 6 5	4 3 2 1 0
LDNP	32-bit	0	0	1	0	1	0	0	0	0	1	imm7	Rt2	Rn	Rt
STNP(SIMD&FP)	32-bit	0	0	1	0	1	1	0	0	0	0	imm7	Rt2	Rn	Rt
LDNP(SIMD&FP)	32-bit	0	0	1	0	1	1	0	0	0	1	imm7	Rt2	Rn	Rt
STNP(SIMD&FP)	64-bit	0	1	1	0	1	1	0	0	0	0	imm7	Rt2	Rn	Rt
LDNP(SIMD&FP)	64-bit	0	1	1	0	1	1	0	0	0	1	imm7	Rt2	Rn	Rt
STNP64-bit	64-bit	1	0	1	0	1	0	0	0	0	0	imm7	Rt2	Rn	Rt
LDNP64-bit	64-bit	1	0	1	0	1	0	0	0	0	1	imm7	Rt2	Rn	Rt
STNP(SIMD&FP)	128-bit	1	0	1	0	1	1	0	0	0	0	imm7	Rt2	Rn	Rt
LDNP(SIMD&FP)	128-bit	1	0	1	0	1	1	0	0	0	1	imm7	Rt2	Rn	Rt
Load/store register pair (post-indexed)		**opc**		**1**	**0**	**1**	**V**	**0**	**0**	**1**	**L**	**imm7**	**Rt2**	**Rn**	**Rt**
STP	32-bit	0	0	1	0	1	0	0	0	1	0	imm7	Rt2	Rn	Rt
LDP	32-bit	0	0	1	0	1	0	0	0	1	1	imm7	Rt2	Rn	Rt
STP(SIMD&FP)	32-bit	0	0	1	0	1	1	0	0	1	0	imm7	Rt2	Rn	Rt
LDP(SIMD&FP)	32-bit	0	0	1	0	1	1	0	0	1	1	imm7	Rt2	Rn	Rt
LDPSW	Post-index	0	1	1	0	1	0	0	0	1	1	imm7	Rt2	Rn	Rt
STP(SIMD&FP)	64-bit	0	1	1	0	1	1	0	0	1	0	imm7	Rt2	Rn	Rt
LDP(SIMD&FP)	64-bit	0	1	1	0	1	1	0	0	1	1	imm7	Rt2	Rn	Rt
STP	64-bit	1	0	1	0	1	0	0	0	1	0	imm7	Rt2	Rn	Rt
LDP	64-bit	1	0	1	0	1	0	0	0	1	1	imm7	Rt2	Rn	Rt
STP(SIMD&FP)	128-bit	1	0	1	0	1	1	0	0	1	0	imm7	Rt2	Rn	Rt
LDP(SIMD&FP)	128-bit	1	0	1	0	1	1	0	0	1	1	imm7	Rt2	Rn	Rt
Load/store register pair (offset)		**opc**		**1**	**0**	**1**	**V**	**0**	**1**	**0**	**L**	**imm7**	**Rt2**	**Rn**	**Rt**
STP	32-bit	0	0	1	0	1	0	0	1	0	0	imm7	Rt2	Rn	Rt
LDP	32-bit	0	0	1	0	1	0	0	1	0	1	imm7	Rt2	Rn	Rt
STP(SIMD&FP)	32-bit	0	0	1	0	1	1	0	1	0	0	imm7	Rt2	Rn	Rt
LDP(SIMD&FP)	32-bit	0	0	1	0	1	1	0	1	0	1	imm7	Rt2	Rn	Rt
LDPSWSigned	offset	0	1	1	0	1	0	0	1	0	1	imm7	Rt2	Rn	Rt
STP(SIMD&FP)	64-bit	0	1	1	0	1	1	0	1	0	0	imm7	Rt2	Rn	Rt
LDP(SIMD&FP)	64-bit	0	1	1	0	1	1	0	1	0	1	imm7	Rt2	Rn	Rt
STP	64-bit	1	0	1	0	1	0	0	1	0	0	imm7	Rt2	Rn	Rt
LDP	64-bit	1	0	1	0	1	0	0	1	0	1	imm7	Rt2	Rn	Rt
STP(SIMD&FP)	128-bit	1	0	1	0	1	1	0	1	0	0	imm7	Rt2	Rn	Rt
LDP(SIMD&FP)	128-bit	1	0	1	0	1	1	0	1	0	1	imm7	Rt2	Rn	Rt
Load/store register pair (pre-indexed)		**opc**		**1**	**0**	**1**	**V**	**0**	**1**	**1**	**L**	**imm7**	**Rt2**	**Rn**	**Rt**
STP	32-bit	0	0	1	0	1	0	0	1	1	0	imm7	Rt2	Rn	Rt
LDP	32-bit	0	0	1	0	1	0	0	1	1	1	imm7	Rt2	Rn	Rt
STP(SIMD&FP)	32-bit	0	0	1	0	1	1	0	1	1	0	imm7	Rt2	Rn	Rt
LDP(SIMD&FP)	32-bit	0	0	1	0	1	1	0	1	1	1	imm7	Rt2	Rn	Rt
LDPSW	Pre-index	0	1	1	0	1	0	0	1	1	1	imm7	Rt2	Rn	Rt
STP(SIMD&FP)	64-bit	0	1	1	0	1	1	0	1	1	0	imm7	Rt2	Rn	Rt
LDP(SIMD&FP)	64-bit	0	1	1	0	1	1	0	1	1	1	imm7	Rt2	Rn	Rt
STP	64-bit	1	0	1	0	1	0	0	1	1	0	imm7	Rt2	Rn	Rt

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LDP	64-bit	1	0	1	0	1	0	0	1	1	1	imm7							Rt2					Rn					Rt				
STP(SIMD&FP)	128-bit	1	0	1	0	1	1	0	1	1	0	imm7							Rt2					Rn					Rt				
LDP(SIMD&FP)	128-bit	1	0	1	0	1	1	0	1	1	1	imm7							Rt2					Rn					Rt				
Load/store register (unscaled immediate)		**size**		**1**	**1**	**1**	**V**	**0**	**0**	**opc**		**0**	**imm9**									**0**	**0**	**Rn**					**Rt**				
STURB	-	0	0	1	1	1	0	0	0	0	0	0	imm9									0	0	Rn					Rt				
LDURB	-	0	0	1	1	1	0	0	0	0	1	0	imm9									0	0	Rn					Rt				
LDURSB	64-bit	0	0	1	1	1	0	0	0	1	0	0	imm9									0	0	Rn					Rt				
LDURSB	32-bit	0	0	1	1	1	0	0	0	1	1	0	imm9									0	0	Rn					Rt				
STUR(SIMD&FP)	8-bit	0	0	1	1	1	1	0	0	0	0	0	imm9									0	0	Rn					Rt				
LDUR(SIMD&FP)	8-bit	0	0	1	1	1	1	0	0	0	1	0	imm9									0	0	Rn					Rt				
STUR(SIMD&FP)	128-bit	0	0	1	1	1	1	0	0	1	0	0	imm9									0	0	Rn					Rt				
LDUR(SIMD&FP)	128-bit	0	0	1	1	1	1	0	0	1	1	0	imm9									0	0	Rn					Rt				
STURH	-	0	1	1	1	1	0	0	0	0	0	0	imm9									0	0	Rn					Rt				
LDURH	-	0	1	1	1	1	0	0	0	0	1	0	imm9									0	0	Rn					Rt				
LDURSH	64-bit	0	1	1	1	1	0	0	0	1	0	0	imm9									0	0	Rn					Rt				
LDURSH	32-bit	0	1	1	1	1	0	0	0	1	1	0	imm9									0	0	Rn					Rt				
STUR(SIMD&FP)	16-bit	0	1	1	1	1	1	0	0	0	0	0	imm9									0	0	Rn					Rt				
LDUR(SIMD&FP)	16-bit	0	1	1	1	1	1	0	0	0	1	0	imm9									0	0	Rn					Rt				
STUR	32-bit	1	0	1	1	1	0	0	0	0	0	0	imm9									0	0	Rn					Rt				
LDUR	32-bit	1	0	1	1	1	0	0	0	0	1	0	imm9									0	0	Rn					Rt				
LDURSW	-	1	0	1	1	1	0	0	0	1	0	0	imm9									0	0	Rn					Rt				
STUR(SIMD&FP)	32-bit	1	0	1	1	1	1	0	0	0	0	0	imm9									0	0	Rn					Rt				
LDUR(SIMD&FP)	32-bit	1	0	1	1	1	1	0	0	0	1	0	imm9									0	0	Rn					Rt				
STUR	64-bit	1	1	1	1	1	0	0	0	0	0	0	imm9									0	0	Rn					Rt				
LDUR	64-bit	1	1	1	1	1	0	0	0	0	1	0	imm9									0	0	Rn					Rt				
PRFUM	-	1	1	1	1	1	0	0	0	1	0	0	imm9									0	0	Rn					Rt				
STUR(SIMD&FP)	64-bit	1	1	1	1	1	1	0	0	0	0	0	imm9									0	0	Rn					Rt				
LDUR(SIMD&FP)	64-bit	1	1	1	1	1	1	0	0	0	1	0	imm9									0	0	Rn					Rt				
Load/store register (immediate post-indexed)		**size**		**1**	**1**	**1**	**V**	**0**	**0**	**opc**		**0**	**imm9**									**0**	**1**	**Rn**					**Rt**				
STRB(immediate)	Post-index	0	0	1	1	1	0	0	0	0	0	0	imm9									0	1	Rn					Rt				
LDRB(immediate)	Post-index	0	0	1	1	1	0	0	0	0	1	0	imm9									0	1	Rn					Rt				
LDRSB(immediate)	64-bit	0	0	1	1	1	0	0	0	1	0	0	imm9									0	1	Rn					Rt				
LDRSB(immediate)	32-bit	0	0	1	1	1	0	0	0	1	1	0	imm9									0	1	Rn					Rt				
STR(immediate,SIMD&	8-bit	0	0	1	1	1	1	0	0	0	0	0	imm9									0	1	Rn					Rt				
LDR(immediate,SIMD&	8-bit	0	0	1	1	1	1	0	0	0	1	0	imm9									0	1	Rn					Rt				
STR(immediate,SIMD&	128-bit	0	0	1	1	1	1	0	0	1	0	0	imm9									0	1	Rn					Rt				
LDR(immediate,SIMD&	128-bit	0	0	1	1	1	1	0	0	1	1	0	imm9									0	1	Rn					Rt				
STRH(immediate)	Post-index	0	1	1	1	1	0	0	0	0	0	0	imm9									0	1	Rn					Rt				
LDRH(immediate)	Post-index	0	1	1	1	1	0	0	0	0	1	0	imm9									0	1	Rn					Rt				
LDRSH(immediate)	64-bit	0	1	1	1	1	0	0	0	1	0	0	imm9									0	1	Rn					Rt				
LDRSH(immediate)	32-bit	0	1	1	1	1	0	0	0	1	1	0	imm9									0	1	Rn					Rt				
STR(immediate,SIMD&	16-bit	0	1	1	1	1	1	0	0	0	0	0	imm9									0	1	Rn					Rt				
LDR(immediate,SIMD&	16-bit	0	1	1	1	1	1	0	0	0	1	0	imm9									0	1	Rn					Rt				

instruction page	variant	31	30	29	28	27	26	25	24	23	22	21	20 19 18 17 16 15 14 13 12	11	10	9 8 7 6 5	4 3 2 1 0
STR(immediate)	32-bit	1	0	1	1	1	0	0	0	0	0	0	imm9	0	1	Rn	Rt
LDR(immediate)	32-bit	1	0	1	1	1	0	0	0	0	1	0	imm9	0	1	Rn	Rt
LDRSW(immediate)	Post-index	1	0	1	1	1	0	0	0	1	0	0	imm9	0	1	Rn	Rt
STR(immediate,SIMD&	32-bit	1	0	1	1	1	1	0	0	0	0	0	imm9	0	1	Rn	Rt
LDR(immediate,SIMD&	32-bit	1	0	1	1	1	1	0	0	0	1	0	imm9	0	1	Rn	Rt
STR(immediate)	64-bit	1	1	1	1	1	0	0	0	0	0	0	imm9	0	1	Rn	Rt
LDR(immediate)	64-bit	1	1	1	1	1	0	0	0	0	1	0	imm9	0	1	Rn	Rt
STR(immediate,SIMD&	64-bit	1	1	1	1	1	1	0	0	0	0	0	imm9	0	1	Rn	Rt
LDR(immediate,SIMD&	64-bit	1	1	1	1	1	1	0	0	0	1	0	imm9	0	1	Rn	Rt
Load/store register (unprivileged)		**size**		**1**	**1**	**1**	**V**	**0**	**0**	**opc**		**0**	**imm9**	**1**	**0**	**Rn**	**Rt**
STTRB	-	0	0	1	1	1	0	0	0	0	0	0	imm9	1	0	Rn	Rt
LDTRB	-	0	0	1	1	1	0	0	0	0	1	0	imm9	1	0	Rn	Rt
LDTRSB	64-bit	0	0	1	1	1	0	0	0	1	0	0	imm9	1	0	Rn	Rt
LDTRSB	32-bit	0	0	1	1	1	0	0	0	1	1	0	imm9	1	0	Rn	Rt
STTRH	-	0	1	1	1	1	0	0	0	0	0	0	imm9	1	0	Rn	Rt
LDTRH	-	0	1	1	1	1	0	0	0	0	1	0	imm9	1	0	Rn	Rt
LDTRSH	64-bit	0	1	1	1	1	0	0	0	1	0	0	imm9	1	0	Rn	Rt
LDTRSH	32-bit	0	1	1	1	1	0	0	0	1	1	0	imm9	1	0	Rn	Rt
STTR	32-bit	1	0	1	1	1	0	0	0	0	0	0	imm9	1	0	Rn	Rt
LDTR	32-bit	1	0	1	1	1	0	0	0	0	1	0	imm9	1	0	Rn	Rt
LDTRSW	-	1	0	1	1	1	0	0	0	1	0	0	imm9	1	0	Rn	Rt
STTR	64-bit	1	1	1	1	1	0	0	0	0	0	0	imm9	1	0	Rn	Rt
LDTR	64-bit	1	1	1	1	1	0	0	0	0	1	0	imm9	1	0	Rn	Rt
Load/store register (immediate pre-indexed)		**size**		**1**	**1**	**1**	**V**	**0**	**0**	**opc**		**0**	**imm9**	**1**	**1**	**Rn**	**Rt**
STRB(immediate)	Pre-index	0	0	1	1	1	0	0	0	0	0	0	imm9	1	1	Rn	Rt
LDRB(immediate)	Pre-index	0	0	1	1	1	0	0	0	0	1	0	imm9	1	1	Rn	Rt
LDRSB(immediate)	64-bit	0	0	1	1	1	0	0	0	1	0	0	imm9	1	1	Rn	Rt
LDRSB(immediate)	32-bit	0	0	1	1	1	0	0	0	1	1	0	imm9	1	1	Rn	Rt
STR(immediate,SIMD&	8-bit	0	0	1	1	1	1	0	0	0	0	0	imm9	1	1	Rn	Rt
LDR(immediate,SIMD&	8-bit	0	0	1	1	1	1	0	0	0	1	0	imm9	1	1	Rn	Rt
STR(immediate,SIMD&	128-bit	0	0	1	1	1	1	0	0	1	0	0	imm9	1	1	Rn	Rt
LDR(immediate,SIMD&	128-bit	0	0	1	1	1	1	0	0	1	1	0	imm9	1	1	Rn	Rt
STRH(immediate)	Pre-index	0	1	1	1	1	0	0	0	0	0	0	imm9	1	1	Rn	Rt
LDRH(immediate)	Pre-index	0	1	1	1	1	0	0	0	0	1	0	imm9	1	1	Rn	Rt
LDRSH(immediate)	64-bit	0	1	1	1	1	0	0	0	1	0	0	imm9	1	1	Rn	Rt
LDRSH(immediate)	32-bit	0	1	1	1	1	0	0	0	1	1	0	imm9	1	1	Rn	Rt
STR(immediate,SIMD&	16-bit	0	1	1	1	1	1	0	0	0	0	0	imm9	1	1	Rn	Rt
LDR(immediate,SIMD&	16-bit	0	1	1	1	1	1	0	0	0	1	0	imm9	1	1	Rn	Rt
STR(immediate)	32-bit	1	0	1	1	1	0	0	0	0	0	0	imm9	1	1	Rn	Rt
LDR(immediate)	32-bit	1	0	1	1	1	0	0	0	0	1	0	imm9	1	1	Rn	Rt
LDRSW(immediate)	Pre-index	1	0	1	1	1	0	0	0	1	0	0	imm9	1	1	Rn	Rt
STR(immediate,SIMD&	32-bit	1	0	1	1	1	1	0	0	0	0	0	imm9	1	1	Rn	Rt
LDR(immediate,SIMD&	32-bit	1	0	1	1	1	1	0	0	0	1	0	imm9	1	1	Rn	Rt

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STR(immediate)	64-bit	1	1	1	1	1	0	0	0	0	0	0	imm9									1	1	Rn					Rt				
LDR(immediate)	64-bit	1	1	1	1	1	0	0	0	0	1	0	imm9									1	1	Rn					Rt				
STR(immediate,SIMD&	64-bit	1	1	1	1	1	1	0	0	0	0	0	imm9									1	1	Rn					Rt				
LDR(immediate,SIMD&	64-bit	1	1	1	1	1	1	0	0	0	1	0	imm9									1	1	Rn					Rt				
Load/store register (register offset)		**size**		**1**	**1**	**1**	**v**	**0**	**0**	**opc**		**1**	**Rm**					**option**			**S**	**1**	**0**	**Rn**					**Rt**				
STRB(register)	-	0	0	1	1	1	0	0	0	0	0	1	Rm					-	-	-	S	1	0	Rn					Rt				
LDRB(register)	-	0	0	1	1	1	0	0	0	0	1	1	Rm					-	-	-	S	1	0	Rn					Rt				
LDRSB(register)	64-bit	0	0	1	1	1	0	0	0	1	0	1	Rm					-	-	-	S	1	0	Rn					Rt				
LDRSB(register)	32-bit	0	0	1	1	1	0	0	0	1	1	1	Rm					-	-	-	S	1	0	Rn					Rt				
STR(register,SIMD&FP	8-bit	0	0	1	1	1	1	0	0	0	0	1	Rm					-	-	-	S	1	0	Rn					Rt				
LDR(register,SIMD&FP	8-bit	0	0	1	1	1	1	0	0	0	1	1	Rm					-	-	-	S	1	0	Rn					Rt				
STR(register,SIMD&FP	128-bit	0	0	1	1	1	1	0	0	1	0	1	Rm					-	-	-	S	1	0	Rn					Rt				
LDR(register,SIMD&FP	128-bit	0	0	1	1	1	1	0	0	1	1	1	Rm					-	-	-	S	1	0	Rn					Rt				
STRH(register)	-	0	1	1	1	1	0	0	0	0	0	1	Rm					-	-	-	S	1	0	Rn					Rt				
LDRH(register)	-	0	1	1	1	1	0	0	0	0	1	1	Rm					-	-	-	S	1	0	Rn					Rt				
LDRSH(register)	64-bit	0	1	1	1	1	0	0	0	1	0	1	Rm					-	-	-	S	1	0	Rn					Rt				
LDRSH(register)	32-bit	0	1	1	1	1	0	0	0	1	1	1	Rm					-	-	-	S	1	0	Rn					Rt				
STR(register,SIMD&FP	16-bit	0	1	1	1	1	1	0	0	0	0	1	Rm					-	-	-	S	1	0	Rn					Rt				
LDR(register,SIMD&FP	16-bit	0	1	1	1	1	1	0	0	0	1	1	Rm					-	-	-	S	1	0	Rn					Rt				
STR(register)	32-bit	1	0	1	1	1	0	0	0	0	0	1	Rm					-	-	-	S	1	0	Rn					Rt				
LDR(register)	32-bit	1	0	1	1	1	0	0	0	0	1	1	Rm					-	-	-	S	1	0	Rn					Rt				
LDRSW(register)	-	1	0	1	1	1	0	0	0	1	0	1	Rm					-	-	-	S	1	0	Rn					Rt				
STR(register,SIMD&FP	32-bit	1	0	1	1	1	1	0	0	0	0	1	Rm					-	-	-	S	1	0	Rn					Rt				
LDR(register,SIMD&FP	32-bit	1	0	1	1	1	1	0	0	0	1	1	Rm					-	-	-	S	1	0	Rn					Rt				
STR(register)	64-bit	1	1	1	1	1	0	0	0	0	0	1	Rm					-	-	-	S	1	0	Rn					Rt				
LDR(register)	64-bit	1	1	1	1	1	0	0	0	0	1	1	Rm					-	-	-	S	1	0	Rn					Rt				
PRFM(register)	-	1	1	1	1	1	0	0	0	1	0	1	Rm					-	-	-	S	1	0	Rn					Rt				
STR(register,SIMD&FP	64-bit	1	1	1	1	1	1	0	0	0	0	1	Rm					-	-	-	S	1	0	Rn					Rt				
LDR(register,SIMD&FP	64-bit	1	1	1	1	1	1	0	0	0	1	1	Rm					-	-	-	S	1	0	Rn					Rt				
Load/store register (unsigned immediate)		**size**		**1**	**1**	**1**	**v**	**0**	**1**	**opc**			**imm12**											**Rn**					**Rt**				
STRB (immediate)	Unsigned offset	0	0	1	1	1	0	0	1	0	0		imm12											Rn					Rt				
LDRB (immediate)	Unsigned offset	0	0	1	1	1	0	0	1	0	1		imm12											Rn					Rt				
LDRSB (immediate)	64-bit	0	0	1	1	1	0	0	1	1	0		imm12											Rn					Rt				
LDRSB (immediate)	32-bit	0	0	1	1	1	0	0	1	1	1		imm12											Rn					Rt				
STR (immediate, SIMD&	8-bit	0	0	1	1	1	1	0	1	0	0		imm12											Rn					Rt				
LDR (immediate, SIMD&	8-bit	0	0	1	1	1	1	0	1	0	1		imm12											Rn					Rt				
STR (immediate, SIMD&	128-bit	0	0	1	1	1	1	0	1	1	0		imm12											Rn					Rt				
LDR (immediate, SIMD&	128-bit	0	0	1	1	1	1	0	1	1	1		imm12											Rn					Rt				
STRH (immediate)	Unsigned offset	0	1	1	1	1	0	0	1	0	0		imm12											Rn					Rt				
LDRH (immediate	Unsigned offset	0	1	1	1	1	0	0	1	0	1		imm12											Rn					Rt				
LDRSH (immediate)	64-bit	0	1	1	1	1	0	0	1	1	0		imm12											Rn					Rt				
LDRSH (immediate)	32-bit	0	1	1	1	1	0	0	1	1	1		imm12											Rn					Rt				
STR (immediate, SIMD&	16-bit	0	1	1	1	1	1	0	1	0	0		imm12											Rn					Rt				

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LDR (immediate, SIMD&	16-bit	0	1	1	1	1	1	0	1	0	1	imm12												Rn					Rt				
STR (immediate)	32-bit	1	0	1	1	1	0	0	1	0	0	imm12												Rn					Rt				
LDR (immediate)	32-bit	1	0	1	1	1	0	0	1	0	1	imm12												Rn					Rt				
LDRSW (immediate)	Unsigned offset	1	0	1	1	1	0	0	1	1	0	imm12												Rn					Rt				
STR (immediate, SIMD&	32-bit	1	0	1	1	1	1	0	1	0	0	imm12												Rn					Rt				
LDR (immediate, SIMD&	32-bit	1	0	1	1	1	1	0	1	0	1	imm12												Rn					Rt				
STR (immediate)	64-bit	1	1	1	1	1	0	0	1	0	0	imm12												Rn					Rt				
LDR (immediate)	64-bit	1	1	1	1	1	0	0	1	0	1	imm12												Rn					Rt				
PRFM (immediate)	-	1	1	1	1	1	0	0	1	1	0	imm12												Rn					Rt				
STR (immediate, SIMD&	64-bit	1	1	1	1	1	1	0	1	0	0	imm12												Rn					Rt				
LDR (immediate, SIMD&	64-bit	1	1	1	1	1	1	0	1	0	1	imm12												Rn					Rt				
AdvSIMD load/store multiple structures		**0**	**Q**	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**L**	**0**	**0**	**0**	**0**	**0**	**0**	**opcode**				**size**		**Rn**					**Rt**				
ST4(multiple structures)	No offset	0	Q	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	size		Rn					Rt				
ST1(multiple structures)	Four registers	0	Q	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	size		Rn					Rt				
ST3(multiple structures)	No offset	0	Q	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	size		Rn					Rt				
ST1(multiple structures)	Three registers	0	Q	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	size		Rn					Rt				
ST1(multiple structures)	One register	0	Q	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	size		Rn					Rt				
ST2(multiple structures)	No offset	0	Q	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	size		Rn					Rt				
ST1(multiple structures)	Two registers	0	Q	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	0	size		Rn					Rt				
LD4(multiple structures)	No offset	0	Q	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	size		Rn					Rt				
LD1(multiple structures)	Four registers	0	Q	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	1	0	size		Rn					Rt				
LD3(multiple structures)	No offset	0	Q	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	1	0	0	size		Rn					Rt				
LD1(multiple structures)	Three registers	0	Q	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	1	1	0	size		Rn					Rt				
LD1(multiple structures)	One register	0	Q	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	1	1	1	size		Rn					Rt				
LD2(multiple structures)	No offset	0	Q	0	0	1	1	0	0	0	1	0	0	0	0	0	0	1	0	0	0	size		Rn					Rt				
LD1(multiple structures)	Two registers	0	Q	0	0	1	1	0	0	0	1	0	0	0	0	0	0	1	0	1	0	size		Rn					Rt				
AdvSIMD load/store multiple structures (post-indexed)		**0**	**Q**	**0**	**0**	**1**	**1**	**0**	**0**	**1**	**L**	**0**	**Rm**					**opcode**				**size**		**Rn**					**Rt**				
ST4 (multiple structures	Register offset	0	Q	0	0	1	1	0	0	1	0	0	!= 11111					0	0	0	0	size		Rn					Rt				
ST1 (multiple structures	Four registers, register offset	0	Q	0	0	1	1	0	0	1	0	0	!= 11111					0	0	1	0	size		Rn					Rt				
ST3 (multiple structures	Register offset	0	Q	0	0	1	1	0	0	1	0	0	!= 11111					0	1	0	0	size		Rn					Rt				
ST1 (multiple structures	Three registers, register offset	0	Q	0	0	1	1	0	0	1	0	0	!= 11111					0	1	1	0	size		Rn					Rt				
ST1 (multiple structures	One register, register offset	0	Q	0	0	1	1	0	0	1	0	0	!= 11111					0	1	1	1	size		Rn					Rt				
ST2 (multiple structures	Register offset	0	Q	0	0	1	1	0	0	1	0	0	!= 11111					1	0	0	0	size		Rn					Rt				
ST1 (multiple structures	Two registers, register offset	0	Q	0	0	1	1	0	0	1	0	0	!= 11111					1	0	1	0	size		Rn					Rt				
ST4 (multiple structures	Immediate offset	0	Q	0	0	1	1	0	0	1	0	0	1	1	1	1	1	0	0	0	0	size		Rn					Rt				
ST1 (multiple structures	Four registers, immediate offset	0	Q	0	0	1	1	0	0	1	0	0	1	1	1	1	1	0	0	1	0	size		Rn					Rt				
ST3 (multiple structures	Immediate offset	0	Q	0	0	1	1	0	0	1	0	0	1	1	1	1	1	0	1	0	0	size		Rn					Rt				
ST1 (multiple structures	Three registers, immediate offset	0	Q	0	0	1	1	0	0	1	0	0	1	1	1	1	1	0	1	1	0	size		Rn					Rt				
ST1 (multiple structures	One register, immediate offset	0	Q	0	0	1	1	0	0	1	0	0	1	1	1	1	1	0	1	1	1	size		Rn					Rt				
ST2 (multiple structures	Immediate offset	0	Q	0	0	1	1	0	0	1	0	0	1	1	1	1	1	1	0	0	0	size		Rn					Rt				
ST1 (multiple structures	Two registers, immediate offset	0	Q	0	0	1	1	0	0	1	0	0	1	1	1	1	1	1	0	1	0	size		Rn					Rt				
LD4 (multiple structures	Register offset	0	Q	0	0	1	1	0	0	1	1	0	!= 11111					0	0	0	0	size		Rn					Rt				
LD1 (multiple structures	Four registers, register offset	0	Q	0	0	1	1	0	0	1	1	0	!= 11111					0	0	1	0	size		Rn					Rt				

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LD3 (multiple structures	Register offset	0	Q	0	0	1	1	0	0	1	1	0	!= 11111					0	1	0	0	size		Rn					Rt				
LD1 (multiple structures	Three registers, register offset	0	Q	0	0	1	1	0	0	1	1	0	!= 11111					0	1	1	0	size		Rn					Rt				
LD1 (multiple structures	One register, register offset	0	Q	0	0	1	1	0	0	1	1	0	!= 11111					0	1	1	1	size		Rn					Rt				
LD2 (multiple structures	Register offset	0	Q	0	0	1	1	0	0	1	1	0	!= 11111					1	0	0	0	size		Rn					Rt				
LD1 (multiple structures	Two registers, register offset	0	Q	0	0	1	1	0	0	1	1	0	!= 11111					1	0	1	0	size		Rn					Rt				
LD4 (multiple structures	Immediate offset	0	Q	0	0	1	1	0	0	1	1	0	1	1	1	1	1	0	0	0	0	size		Rn					Rt				
LD1 (multiple structures	Four registers, immediate offset	0	Q	0	0	1	1	0	0	1	1	0	1	1	1	1	1	0	0	1	0	size		Rn					Rt				
LD3 (multiple structures	Immediate offset	0	Q	0	0	1	1	0	0	1	1	0	1	1	1	1	1	0	1	0	0	size		Rn					Rt				
LD1 (multiple structures	Three registers, immediate offset	0	Q	0	0	1	1	0	0	1	1	0	1	1	1	1	1	0	1	1	0	size		Rn					Rt				
LD1 (multiple structures	One register, immediate offset	0	Q	0	0	1	1	0	0	1	1	0	1	1	1	1	1	0	1	1	1	size		Rn					Rt				
LD2 (multiple structures	Immediate offset	0	Q	0	0	1	1	0	0	1	1	0	1	1	1	1	1	1	0	0	0	size		Rn					Rt				
LD1 (multiple structures	Two registers, immediate offset	0	Q	0	0	1	1	0	0	1	1	0	1	1	1	1	1	1	0	1	0	size		Rn					Rt				
AdvSIMD load/store single structure		**0**	**Q**	**0**	**0**	**1**	**1**	**0**	**1**	**0**	**L**	**R**	**0**	**0**	**0**	**0**	**0**	**opcode**			**S**	**size**		**Rn**					**Rt**				
ST1 (single structure)	8-bit	0	Q	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	-	-	-	Rn					Rt				
ST3 (single structure)	8-bit	0	Q	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	1	-	-	-	Rn					Rt				
ST1 (single structure)	16-bit	0	Q	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	1	0	-	x	0	Rn					Rt				
ST3 (single structure)	16-bit	0	Q	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	1	1	-	x	0	Rn					Rt				
ST1 (single structure)	32-bit	0	Q	0	0	1	1	0	1	0	0	0	0	0	0	0	0	1	0	0	-	0	0	Rn					Rt				
ST1 (single structure)	64-bit	0	Q	0	0	1	1	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	1	Rn					Rt				
ST3 (single structure)	32-bit	0	Q	0	0	1	1	0	1	0	0	0	0	0	0	0	0	1	0	1	-	0	0	Rn					Rt				
ST3 (single structure)	64-bit	0	Q	0	0	1	1	0	1	0	0	0	0	0	0	0	0	1	0	1	0	0	1	Rn					Rt				
ST2 (single structure)	8-bit	0	Q	0	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	-	-	-	Rn					Rt				
ST4 (single structure)	8-bit	0	Q	0	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	1	-	-	-	Rn					Rt				
ST2 (single structure)	16-bit	0	Q	0	0	1	1	0	1	0	0	1	0	0	0	0	0	0	1	0	-	x	0	Rn					Rt				
ST4 (single structure)	16-bit	0	Q	0	0	1	1	0	1	0	0	1	0	0	0	0	0	0	1	1	-	x	0	Rn					Rt				
ST2 (single structure)	32-bit	0	Q	0	0	1	1	0	1	0	0	1	0	0	0	0	0	1	0	0	-	0	0	Rn					Rt				
ST2 (single structure)	64-bit	0	Q	0	0	1	1	0	1	0	0	1	0	0	0	0	0	1	0	0	0	0	1	Rn					Rt				
ST4 (single structure)	32-bit	0	Q	0	0	1	1	0	1	0	0	1	0	0	0	0	0	1	0	1	-	0	0	Rn					Rt				
ST4 (single structure)	64-bit	0	Q	0	0	1	1	0	1	0	0	1	0	0	0	0	0	1	0	1	0	0	1	Rn					Rt				
LD1 (single structure)	8-bit	0	Q	0	0	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	-	-	-	Rn					Rt				
LD3 (single structure)	8-bit	0	Q	0	0	1	1	0	1	0	1	0	0	0	0	0	0	0	0	1	-	-	-	Rn					Rt				
LD1 (single structure)	16-bit	0	Q	0	0	1	1	0	1	0	1	0	0	0	0	0	0	0	1	0	-	x	0	Rn					Rt				
LD3 (single structure)	16-bit	0	Q	0	0	1	1	0	1	0	1	0	0	0	0	0	0	0	1	1	-	x	0	Rn					Rt				
LD1 (single structure)	32-bit	0	Q	0	0	1	1	0	1	0	1	0	0	0	0	0	0	1	0	0	-	0	0	Rn					Rt				
LD1 (single structure)	64-bit	0	Q	0	0	1	1	0	1	0	1	0	0	0	0	0	0	1	0	0	0	0	1	Rn					Rt				
LD3 (single structure)	32-bit	0	Q	0	0	1	1	0	1	0	1	0	0	0	0	0	0	1	0	1	-	0	0	Rn					Rt				
LD3 (single structure)	64-bit	0	Q	0	0	1	1	0	1	0	1	0	0	0	0	0	0	1	0	1	0	0	1	Rn					Rt				
LD1R	No offset	0	Q	0	0	1	1	0	1	0	1	0	0	0	0	0	0	1	1	0	0	-	-	Rn					Rt				
LD3R	No offset	0	Q	0	0	1	1	0	1	0	1	0	0	0	0	0	0	1	1	1	0	-	-	Rn					Rt				
LD2 (single structure)	8-bit	0	Q	0	0	1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	-	-	-	Rn					Rt				
LD4 (single structure)	8-bit	0	Q	0	0	1	1	0	1	0	1	1	0	0	0	0	0	0	0	1	-	-	-	Rn					Rt				
LD2 (single structure)	16-bit	0	Q	0	0	1	1	0	1	0	1	1	0	0	0	0	0	0	1	0	-	x	0	Rn					Rt				
LD4 (single structure)	16-bit	0	Q	0	0	1	1	0	1	0	1	1	0	0	0	0	0	0	1	1	-	x	0	Rn					Rt				

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LD2 (single structure)	32-bit	0	Q	0	0	1	1	0	1	0	1	1	0	0	0	0	0	1	0	0	-	0	0	Rn					Rt				
LD2 (single structure)	64-bit	0	Q	0	0	1	1	0	1	0	1	1	0	0	0	0	0	1	0	0	0	0	1	Rn					Rt				
LD4 (single structure)	32-bit	0	Q	0	0	1	1	0	1	0	1	1	0	0	0	0	0	1	0	1	-	0	0	Rn					Rt				
LD4 (single structure)	64-bit	0	Q	0	0	1	1	0	1	0	1	1	0	0	0	0	0	1	0	1	0	0	1	Rn					Rt				
LD2R	No offset	0	Q	0	0	1	1	0	1	0	1	1	0	0	0	0	0	1	1	0	0	-	-	Rn					Rt				
LD4R	No offset	0	Q	0	0	1	1	0	1	0	1	1	0	0	0	0	0	1	1	1	0	-	-	Rn					Rt				
AdvSIMD load/store single structure (post-indexed)		**0**	**Q**	**0**	**0**	**1**	**1**	**0**	**1**	**1**	**L**	**R**	**Rm**					**opcode**			**S**	**size**		**Rn**					**Rt**				
ST1 (single structure)	8-bit, register offset	0	Q	0	0	1	1	0	1	1	0	0	!=11111					0	0	0	-	-	-	Rn					Rt				
ST3 (single structure)	8-bit, register offset	0	Q	0	0	1	1	0	1	1	0	0	!=11111					0	0	1	-	-	-	Rn					Rt				
ST1 (single structure)	16-bit, register offset	0	Q	0	0	1	1	0	1	1	0	0	!=11111					0	1	0	-	x	0	Rn					Rt				
ST3 (single structure)	16-bit, register offset	0	Q	0	0	1	1	0	1	1	0	0	!=11111					0	1	1	-	x	0	Rn					Rt				
ST1 (single structure)	32-bit, register offset	0	Q	0	0	1	1	0	1	1	0	0	!=11111					1	0	0	-	0	0	Rn					Rt				
ST1 (single structure)	64-bit, register offset	0	Q	0	0	1	1	0	1	1	0	0	!=11111					1	0	0	0	0	1	Rn					Rt				
ST3 (single structure)	32-bit, register offset	0	Q	0	0	1	1	0	1	1	0	0	!=11111					1	0	1	-	0	0	Rn					Rt				
ST3 (single structure)	64-bit, register offset	0	Q	0	0	1	1	0	1	1	0	0	!=11111					1	0	1	0	0	1	Rn					Rt				
ST1 (single structure)	8-bit, immediate offset	0	Q	0	0	1	1	0	1	1	0	0	1	1	1	1	1	0	0	0	-	-	-	Rn					Rt				
ST3 (single structure)	8-bit, immediate offset	0	Q	0	0	1	1	0	1	1	0	0	1	1	1	1	1	0	0	1	-	-	-	Rn					Rt				
ST1 (single structure)	16-bit, immediate offset	0	Q	0	0	1	1	0	1	1	0	0	1	1	1	1	1	0	1	0	-	x	0	Rn					Rt				
ST3 (single structure)	16-bit, immediate offset	0	Q	0	0	1	1	0	1	1	0	0	1	1	1	1	1	0	1	1	-	x	0	Rn					Rt				
ST1 (single structure)	32-bit, immediate offset	0	Q	0	0	1	1	0	1	1	0	0	1	1	1	1	1	1	0	0	-	0	0	Rn					Rt				
ST1 (single structure)	64-bit, immediate offset	0	Q	0	0	1	1	0	1	1	0	0	1	1	1	1	1	1	0	0	0	0	1	Rn					Rt				
ST3 (single structure)	32-bit, immediate offset	0	Q	0	0	1	1	0	1	1	0	0	1	1	1	1	1	1	0	1	-	0	0	Rn					Rt				
ST3 (single structure)	64-bit, immediate offset	0	Q	0	0	1	1	0	1	1	0	0	1	1	1	1	1	1	0	1	0	0	1	Rn					Rt				
ST2 (single structure)	8-bit, register offset	0	Q	0	0	1	1	0	1	1	0	1	!=11111					0	0	0	-	-	-	Rn					Rt				
ST4 (single structure)	8-bit, register offset	0	Q	0	0	1	1	0	1	1	0	1	!=11111					0	0	1	-	-	-	Rn					Rt				
ST2 (single structure)	16-bit, register offset	0	Q	0	0	1	1	0	1	1	0	1	!=11111					0	1	0	-	x	0	Rn					Rt				
ST4 (single structure)	16-bit, register offset	0	Q	0	0	1	1	0	1	1	0	1	!=11111					0	1	1	-	x	0	Rn					Rt				
ST2 (single structure)	32-bit, register offset	0	Q	0	0	1	1	0	1	1	0	1	!=11111					1	0	0	-	0	0	Rn					Rt				
ST2 (single structure)	64-bit, register offset	0	Q	0	0	1	1	0	1	1	0	1	!=11111					1	0	0	0	0	1	Rn					Rt				
ST4 (single structure)	32-bit, register offset	0	Q	0	0	1	1	0	1	1	0	1	!=11111					1	0	1	-	0	0	Rn					Rt				
ST4 (single structure)	64-bit, register offset	0	Q	0	0	1	1	0	1	1	0	1	!=11111					1	0	1	0	0	1	Rn					Rt				
ST2 (single structure)	8-bit, immediate offset	0	Q	0	0	1	1	0	1	1	0	1	1	1	1	1	1	0	0	0	-	-	-	Rn					Rt				
ST4 (single structure)	8-bit, immediate offset	0	Q	0	0	1	1	0	1	1	0	1	1	1	1	1	1	0	0	1	-	-	-	Rn					Rt				
ST2 (single structure)	16-bit, immediate offset	0	Q	0	0	1	1	0	1	1	0	1	1	1	1	1	1	0	1	0	-	x	0	Rn					Rt				
ST4 (single structure)	16-bit, immediate offset	0	Q	0	0	1	1	0	1	1	0	1	1	1	1	1	1	0	1	1	-	x	0	Rn					Rt				
ST2 (single structure)	32-bit, immediate offset	0	Q	0	0	1	1	0	1	1	0	1	1	1	1	1	1	1	0	0	-	0	0	Rn					Rt				
ST2 (single structure)	64-bit, immediate offset	0	Q	0	0	1	1	0	1	1	0	1	1	1	1	1	1	1	0	0	0	0	1	Rn					Rt				
ST4 (single structure)	32-bit, immediate offset	0	Q	0	0	1	1	0	1	1	0	1	1	1	1	1	1	1	0	1	-	0	0	Rn					Rt				
ST4 (single structure)	64-bit, immediate offset	0	Q	0	0	1	1	0	1	1	0	1	1	1	1	1	1	1	0	1	0	0	1	Rn					Rt				
LD1 (single structure)	8-bit, register offset	0	Q	0	0	1	1	0	1	1	1	0	!=11111					0	0	0	-	-	-	Rn					Rt				
LD3 (single structure)	8-bit, register offset	0	Q	0	0	1	1	0	1	1	1	0	!=11111					0	0	1	-	-	-	Rn					Rt				
LD1 (single structure)	16-bit, register offset	0	Q	0	0	1	1	0	1	1	1	0	!=11111					0	1	0	-	x	0	Rn					Rt				
LD3 (single structure)	16-bit, register offset	0	Q	0	0	1	1	0	1	1	1	0	!=11111					0	1	1	-	x	0	Rn					Rt				

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LD1 (single structure)	32-bit, register offset	0	Q	0	0	1	1	0	1	1	1	0	!=11111					1	0	0	-	0	0	Rn					Rt				
LD1 (single structure)	64-bit, register offset	0	Q	0	0	1	1	0	1	1	1	0	!=11111					1	0	0	0	0	1	Rn					Rt				
LD3 (single structure)	32-bit, register offset	0	Q	0	0	1	1	0	1	1	1	0	!=11111					1	0	1	-	0	0	Rn					Rt				
LD3 (single structure)	64-bit, register offset	0	Q	0	0	1	1	0	1	1	1	0	!=11111					1	0	1	0	0	1	Rn					Rt				
LD1R	Register offset	0	Q	0	0	1	1	0	1	1	1	0	!=11111					1	1	0	0	-	-	Rn					Rt				
LD3R	Register offset	0	Q	0	0	1	1	0	1	1	1	0	!=11111					1	1	1	0	-	-	Rn					Rt				
LD1 (single structure)	8-bit, immediate offset	0	Q	0	0	1	1	0	1	1	1	0	1	1	1	1	1	0	0	0	-	-	-	Rn					Rt				
LD3 (single structure)	8-bit, immediate offset	0	Q	0	0	1	1	0	1	1	1	0	1	1	1	1	1	0	0	1	-	-	-	Rn					Rt				
LD1 (single structure)	16-bit, immediate offset	0	Q	0	0	1	1	0	1	1	1	0	1	1	1	1	1	0	1	0	-	x	0	Rn					Rt				
LD3 (single structure)	16-bit, immediate offset	0	Q	0	0	1	1	0	1	1	1	0	1	1	1	1	1	0	1	1	-	x	0	Rn					Rt				
LD1 (single structure)	32-bit, immediate offset	0	Q	0	0	1	1	0	1	1	1	0	1	1	1	1	1	1	0	0	-	0	0	Rn					Rt				
LD1 (single structure)	64-bit, immediate offset	0	Q	0	0	1	1	0	1	1	1	0	1	1	1	1	1	1	0	0	0	0	1	Rn					Rt				
LD3 (single structure)	32-bit, immediate offset	0	Q	0	0	1	1	0	1	1	1	0	1	1	1	1	1	1	0	1	-	0	0	Rn					Rt				
LD3 (single structure)	64-bit, immediate offset	0	Q	0	0	1	1	0	1	1	1	0	1	1	1	1	1	1	0	1	0	0	1	Rn					Rt				
LD1R	Immediate offset	0	Q	0	0	1	1	0	1	1	1	0	1	1	1	1	1	1	1	0	0	-	-	Rn					Rt				
LD3R	Immediate offset	0	Q	0	0	1	1	0	1	1	1	0	1	1	1	1	1	1	1	1	0	-	-	Rn					Rt				
LD2 (single structure)	8-bit, register offset	0	Q	0	0	1	1	0	1	1	1	1	!=11111					0	0	0	-	-	-	Rn					Rt				
LD4 (single structure)	8-bit, register offset	0	Q	0	0	1	1	0	1	1	1	1	!=11111					0	0	1	-	-	-	Rn					Rt				
LD2 (single structure)	16-bit, register offset	0	Q	0	0	1	1	0	1	1	1	1	!=11111					0	1	0	-	x	0	Rn					Rt				
LD4 (single structure)	16-bit, register offset	0	Q	0	0	1	1	0	1	1	1	1	!=11111					0	1	1	-	x	0	Rn					Rt				
LD2 (single structure)	32-bit, register offset	0	Q	0	0	1	1	0	1	1	1	1	!=11111					1	0	0	-	0	0	Rn					Rt				
LD2 (single structure)	64-bit, register offset	0	Q	0	0	1	1	0	1	1	1	1	!=11111					1	0	0	0	0	1	Rn					Rt				
LD4 (single structure)	32-bit, register offset	0	Q	0	0	1	1	0	1	1	1	1	!=11111					1	0	1	-	0	0	Rn					Rt				
LD4 (single structure)	64-bit, register offset	0	Q	0	0	1	1	0	1	1	1	1	!=11111					1	0	1	0	0	1	Rn					Rt				
LD2R	Register offset	0	Q	0	0	1	1	0	1	1	1	1	!=11111					1	1	0	0	-	-	Rn					Rt				
LD4R	Register offset	0	Q	0	0	1	1	0	1	1	1	1	!=11111					1	1	1	0	-	-	Rn					Rt				
LD2 (single structure)	8-bit, immediate offset	0	Q	0	0	1	1	0	1	1	1	1	1	1	1	1	1	0	0	0	-	-	-	Rn					Rt				
LD4 (single structure)	8-bit, immediate offset	0	Q	0	0	1	1	0	1	1	1	1	1	1	1	1	1	0	0	1	-	-	-	Rn					Rt				
LD2 (single structure)	16-bit, immediate offset	0	Q	0	0	1	1	0	1	1	1	1	1	1	1	1	1	0	1	0	-	x	0	Rn					Rt				
LD4 (single structure)	16-bit, immediate offset	0	Q	0	0	1	1	0	1	1	1	1	1	1	1	1	1	0	1	1	-	x	0	Rn					Rt				
LD2 (single structure)	32-bit, immediate offset	0	Q	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	0	0	-	0	0	Rn					Rt				
LD2 (single structure)	64-bit, immediate offset	0	Q	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	1	Rn					Rt				
LD4 (single structure)	32-bit, immediate offset	0	Q	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	0	1	-	0	0	Rn					Rt				
LD4 (single structure)	64-bit, immediate offset	0	Q	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	0	1	0	0	1	Rn					Rt				
LD2R	Immediate offset	0	Q	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	0	0	-	-	Rn					Rt				
LD4R	Immediate offset	0	Q	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	0	-	-	Rn					Rt				
Data processing – Immediate					**1**	**0**	**0**																										
PC-rel. addressing		**op**	**immlo**		**1**	**0**	**0**	**0**	**0**	**immhi**																				**Rd**			
ADR	-	0	immlo		1	0	0	0	0	immhi																				Rd			
ADRP	-	1	immlo		1	0	0	0	0	immhi																				Rd			
Add/subtract (immediate)		**sf**	**op**	**S**	**1**	**0**	**0**	**0**	**1**	**shift**		**imm12**														**Rn**				**Rd**			
ADD (immediate)	32-bit	0	0	0	1	0	0	0	1	-	-	imm12														Rn				Rd			
ADDS (immediate)	32-bit	0	0	1	1	0	0	0	1	-	-	imm12														Rn				Rd			

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SUB (immediate)	32-bit	0	1	0	1	0	0	0	1	-	-	imm12														Rn					Rd		
SUBS (immediate)	32-bit	0	1	1	1	0	0	0	1	-	-	imm12														Rn					Rd		
ADD (immediate)	64-bit	1	0	0	1	0	0	0	1	-	-	imm12														Rn					Rd		
ADDS (immediate)	64-bit	1	0	1	1	0	0	0	1	-	-	imm12														Rn					Rd		
SUB (immediate)	64-bit	1	1	0	1	0	0	0	1	-	-	imm12														Rn					Rd		
SUBS (immediate)	64-bit	1	1	1	1	0	0	0	1	-	-	imm12														Rn					Rd		
Logical (immediate)		**sf**		**opc**	**1**	**0**	**0**	**1**	**0**	**0**	**N**	**immr**						**imms**							**Rn**					**Rd**		
AND (immediate)	32-bit	0	0	0	1	0	0	1	0	0	0	immr						imms								Rn					Rd		
ORR (immediate)	32-bit	0	0	1	1	0	0	1	0	0	0	immr						imms								Rn					Rd		
EOR (immediate)	32-bit	0	1	0	1	0	0	1	0	0	0	immr						imms								Rn					Rd		
ANDS (immediate)	32-bit	0	1	1	1	0	0	1	0	0	0	immr						imms								Rn					Rd		
AND (immediate)	64-bit	1	0	0	1	0	0	1	0	0	-	immr						imms								Rn					Rd		
ORR (immediate)	64-bit	1	0	1	1	0	0	1	0	0	-	immr						imms								Rn					Rd		
EOR (immediate)	64-bit	1	1	0	1	0	0	1	0	0	-	immr						imms								Rn					Rd		
ANDS (immediate)	64-bit	1	1	1	1	0	0	1	0	0	-	immr						imms								Rn					Rd		
Move wide (immediate)		**sf**		**opc**	**1**	**0**	**0**	**1**	**0**	**1**	**hw**			**imm16**																	**Rd**		
MOVN	32-bit	0	0	0	1	0	0	1	0	1	-	-		imm16																	Rd		
MOVZ	32-bit	0	1	0	1	0	0	1	0	1	-	-		imm16																	Rd		
MOVK	32-bit	0	1	1	1	0	0	1	0	1	-	-		imm16																	Rd		
MOVN	64-bit	1	0	0	1	0	0	1	0	1	-	-		imm16																	Rd		
MOVZ	64-bit	1	1	0	1	0	0	1	0	1	-	-		imm16																	Rd		
MOVK	64-bit	1	1	1	1	0	0	1	0	1	-	-		imm16																	Rd		
Bitfield		**sf**		**opc**	**1**	**0**	**0**	**1**	**1**	**0**	**N**			**immr**						**imms**						**Rn**					**Rd**		
SBFM	32-bit	0	0	0	1	0	0	1	1	0	0			immr						imms						Rn					Rd		
BFM	32-bit	0	0	1	1	0	0	1	1	0	0			immr						imms						Rn					Rd		
UBFM	32-bit	0	1	0	1	0	0	1	1	0	0			immr						imms						Rn					Rd		
SBFM	64-bit	1	0	0	1	0	0	1	1	0	1			immr						imms						Rn					Rd		
BFM	64-bit	1	0	1	1	0	0	1	1	0	1			immr						imms						Rn					Rd		
UBFM	64-bit	1	1	0	1	0	0	1	1	0	1			immr						imms						Rn					Rd		
Extract		**sf**		**op21**	**1**	**0**	**0**	**1**	**1**	**1**	**N**	**o0**		**Rm**						**imms**						**Rn**					**Rd**		
EXTR	32-bit	0	0	0	1	0	0	1	1	1	0	0		Rm				0	x	x	x	x	x			Rn					Rd		
EXTR	64-bit	1	0	0	1	0	0	1	1	1	1	0		Rm				-	-	-	-	-	-			Rn					Rd		
Data Processing – register						**1**	**0**	**1**																									
Logical (shifted register)		**sf**		**opc**	**0**	**1**	**0**	**1**	**0**	**shift**	**N**			**Rm**						**imm6**						**Rn**					**Rd**		
AND (shifted register)	32-bit	0	0	0	0	1	0	1	0	shift	0			Rm				-	-	-	-	-	-			Rn					Rd		
BIC (shifted register)	32-bit	0	0	0	0	1	0	1	0	shift	1			Rm				-	-	-	-	-	-			Rn					Rd		
ORR (shifted register)	32-bit	0	0	1	0	1	0	1	0	shift	0			Rm				-	-	-	-	-	-			Rn					Rd		
ORN (shifted register)	32-bit	0	0	1	0	1	0	1	0	shift	1			Rm				-	-	-	-	-	-			Rn					Rd		
EOR (shifted register)	32-bit	0	1	0	0	1	0	1	0	shift	0			Rm				-	-	-	-	-	-			Rn					Rd		
EON (shifted register)	32-bit	0	1	0	0	1	0	1	0	shift	1			Rm				-	-	-	-	-	-			Rn					Rd		
ANDS (shifted register)	32-bit	0	1	1	0	1	0	1	0	shift	0			Rm				-	-	-	-	-	-			Rn					Rd		
BICS (shifted register)	32-bit	0	1	1	0	1	0	1	0	shift	1			Rm				-	-	-	-	-	-			Rn					Rd		
AND (shifted register)	64-bit	1	0	0	0	1	0	1	0	shift	0			Rm				-	-	-	-	-	-			Rn					Rd		

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BIC (shifted register)	64-bit	1	0	0	0	1	0	1	0	shift		1		Rm				-	-	-	-	-	-		Rn				Rd				
ORR (shifted register)	64-bit	1	0	1	0	1	0	1	0	shift		0		Rm				-	-	-	-	-	-		Rn				Rd				
ORN (shifted register)	64-bit	1	0	1	0	1	0	1	0	shift		1		Rm				-	-	-	-	-	-		Rn				Rd				
EOR (shifted register)	64-bit	1	1	0	0	1	0	1	0	shift		0		Rm				-	-	-	-	-	-		Rn				Rd				
EON (shifted register)	64-bit	1	1	0	0	1	0	1	0	shift		1		Rm				-	-	-	-	-	-		Rn				Rd				
ANDS (shifted register)	64-bit	1	1	1	0	1	0	1	0	shift		0		Rm				-	-	-	-	-	-		Rn				Rd				
BICS (shifted register)	64-bit	1	1	1	0	1	0	1	0	shift		1		Rm				-	-	-	-	-	-		Rn				Rd				
Add/subtract (shifted register)		**sf**	**op**	**S**	**0**	**1**	**0**	**1**	**1**	**shift**		**0**		**Rm**				**imm6**							**Rn**				**Rd**				
ADD (shifted register)	32-bit	0	0	0	0	1	0	1	1	-	-	0		Rm				-	-	-	-	-	-		Rn				Rd				
ADDS (shifted register)	32-bit	0	0	1	0	1	0	1	1	-	-	0		Rm				-	-	-	-	-	-		Rn				Rd				
SUB (shifted register)	32-bit	0	1	0	0	1	0	1	1	-	-	0		Rm				-	-	-	-	-	-		Rn				Rd				
SUBS (shifted register)	32-bit	0	1	1	0	1	0	1	1	-	-	0		Rm				-	-	-	-	-	-		Rn				Rd				
ADD (shifted register)	64-bit	1	0	0	0	1	0	1	1	-	-	0		Rm				-	-	-	-	-	-		Rn				Rd				
ADDS (shifted register)	64-bit	1	0	1	0	1	0	1	1	-	-	0		Rm				-	-	-	-	-	-		Rn				Rd				
SUB (shifted register)	64-bit	1	1	0	0	1	0	1	1	-	-	0		Rm				-	-	-	-	-	-		Rn				Rd				
SUBS (shifted register)	64-bit	1	1	1	0	1	0	1	1	-	-	0		Rm				-	-	-	-	-	-		Rn				Rd				
Add/subtract (extended register)		**sf**	**op**	**S**	**0**	**1**	**0**	**1**	**1**	**opt**		**1**		**Rm**				**option**			**imm3**				**Rn**				**Rd**				
ADD (extended register	32-bit	0	0	0	0	1	0	1	1	0	0	1		Rm				option			-	-	-		Rn				Rd				
ADDS (extended registe	32-bit	0	0	1	0	1	0	1	1	0	0	1		Rm				option			-	-	-		Rn				Rd				
SUB (extended register	32-bit	0	1	0	0	1	0	1	1	0	0	1		Rm				option			-	-	-		Rn				Rd				
SUBS (extended registe	32-bit	0	1	1	0	1	0	1	1	0	0	1		Rm				option			-	-	-		Rn				Rd				
ADD (extended register	64-bit	1	0	0	0	1	0	1	1	0	0	1		Rm				option			-	-	-		Rn				Rd				
ADDS (extended registe	64-bit	1	0	1	0	1	0	1	1	0	0	1		Rm				option			-	-	-		Rn				Rd				
SUB (extended register	64-bit	1	1	0	0	1	0	1	1	0	0	1		Rm				option			-	-	-		Rn				Rd				
SUBS (extended registe	64-bit	1	1	1	0	1	0	1	1	0	0	1		Rm				option			-	-	-		Rn				Rd				
Add/subtract (with carry)		**sf**	**op**	**S**	**1**	**1**	**0**	**1**	**0**	**0**	**0**	**0**						**opcode2**							**Rn**				**Rd**				
ADC	32-bit	0	0	0	1	1	0	1	0	0	0	0		Rm				0	0	0	0	0	0		Rn				Rd				
ADCS	32-bit	0	0	1	1	1	0	1	0	0	0	0		Rm				0	0	0	0	0	0		Rn				Rd				
SBC	32-bit	0	1	0	1	1	0	1	0	0	0	0		Rm				0	0	0	0	0	0		Rn				Rd				
SBCS	32-bit	0	1	1	1	1	0	1	0	0	0	0		Rm				0	0	0	0	0	0		Rn				Rd				
ADC	64-bit	1	0	0	1	1	0	1	0	0	0	0		Rm				0	0	0	0	0	0		Rn				Rd				
ADCS	64-bit	1	0	1	1	1	0	1	0	0	0	0		Rm				0	0	0	0	0	0		Rn				Rd				
SBC	64-bit	1	1	0	1	1	0	1	0	0	0	0		Rm				0	0	0	0	0	0		Rn				Rd				
SBCS	64-bit	1	1	1	1	1	0	1	0	0	0	0		Rm				0	0	0	0	0	0		Rn				Rd				
Conditional compare (register)		**sf**	**op**	**S**	**1**	**1**	**0**	**1**	**0**	**0**	**1**	**0**		**imm5**				**cond**				**0**	**o2**		**Rn**				**o3**	**nzcv**			
CCMN (register)	32-bit	0	0	1	1	1	0	1	0	0	1	0		imm5				cond				0	0		Rn				0	nzcv			
CCMP (register)	32-bit	0	1	1	1	1	0	1	0	0	1	0		imm5				cond				0	0		Rn				0	nzcv			
CCMN (register)	64-bit	1	0	1	1	1	0	1	0	0	1	0		imm5				cond				0	0		Rn				0	nzcv			
CCMP (register)	64-bit	1	1	1	1	1	0	1	0	0	1	0		imm5				cond				0	0		Rn				0	nzcv			
Conditional compare (immediate)		**sf**	**op**	**S**	**1**	**1**	**0**	**1**	**0**	**0**	**1**	**0**		**imm5**				**cond**				**1**	**o2**		**Rn**				**o3**	**nzcv**			
CCMN (immediate)	32-bit	0	0	1	1	1	0	1	0	0	1	0		imm5				cond				1	0		Rn				0	nzcv			
CCMP (immediate)	32-bit	0	1	1	1	1	0	1	0	0	1	0		imm5				cond				1	0		Rn				0	nzcv			
CCMN (immediate)	64-bit	1	0	1	1	1	0	1	0	0	1	0		imm5				cond				1	0		Rn				0	nzcv			

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CCMP (immediate)	64-bit	1	1	1	1	1	0	1	0	0	1	0	imm5					cond				1	0	Rn					0	nzcv			
Conditional select		**sf**	**op**	**S**	**1**	**1**	**0**	**1**	**0**	**1**	**0**	**0**	**Rm**					**cond**				**op2**		**Rn**					**Rd**				
CSEL	32-bit	0	0	0	1	1	0	1	0	1	0	0	Rm					cond				0	0	Rn					Rd				
CSINC	32-bit	0	0	0	1	1	0	1	0	1	0	0	Rm					cond				0	1	Rn					Rd				
CSINV	32-bit	0	1	0	1	1	0	1	0	1	0	0	Rm					cond				0	0	Rn					Rd				
CSNEG	32-bit	0	1	0	1	1	0	1	0	1	0	0	Rm					cond				0	1	Rn					Rd				
CSEL	64-bit	1	0	0	1	1	0	1	0	1	0	0	Rm					cond				0	0	Rn					Rd				
CSINC	64-bit	1	0	0	1	1	0	1	0	1	0	0	Rm					cond				0	1	Rn					Rd				
CSINV	64-bit	1	1	0	1	1	0	1	0	1	0	0	Rm					cond				0	0	Rn					Rd				
CSNEG	64-bit	1	1	0	1	1	0	1	0	1	0	0	Rm					cond				0	1	Rn					Rd				
Data-processing (3 source)		**sf**	**op54**		**1**	**1**	**0**	**1**	**1**	**op31**			**Rm**					**o0**	**Ra**					**Rn**					**Rd**				
MADD	32-bit	0	0	0	1	1	0	1	1	0	0	0	Rm					0	Ra					Rn					Rd				
MSUB	32-bit	0	0	0	1	1	0	1	1	0	0	0	Rm					1	Ra					Rn					Rd				
MADD	64-bit	1	0	0	1	1	0	1	1	0	0	0	Rm					0	Ra					Rn					Rd				
MSUB	64-bit	1	0	0	1	1	0	1	1	0	0	0	Rm					1	Ra					Rn					Rd				
SMADDL	-	1	0	0	1	1	0	1	1	0	0	1	Rm					0	Ra					Rn					Rd				
SMSUBL	-	1	0	0	1	1	0	1	1	0	0	1	Rm					1	Ra					Rn					Rd				
SMULH	-	1	0	0	1	1	0	1	1	0	1	0	Rm					0	Ra					Rn					Rd				
UMADDL	-	1	0	0	1	1	0	1	1	1	0	1	Rm					0	Ra					Rn					Rd				
UMSUBL	-	1	0	0	1	1	0	1	1	1	0	1	Rm					1	Ra					Rn					Rd				
UMULH	-	1	0	0	1	1	0	1	1	1	1	0	Rm					0	Ra					Rn					Rd				
Data-processing (2 source)		**sf**	**0**	**S**	**1**	**1**	**0**	**1**	**0**	**1**	**1**	**0**	**Rm**					**opcode**						**Rn**					**Rd**				
UDIV	32-bit	0	0	0	1	1	0	1	0	1	1	0	Rm					0	0	0	0	1	0	Rn					Rd				
SDIV	32-bit	0	0	0	1	1	0	1	0	1	1	0	Rm					0	0	0	0	1	1	Rn					Rd				
LSLV	32-bit	0	0	0	1	1	0	1	0	1	1	0	Rm					0	0	1	0	0	0	Rn					Rd				
LSRV	32-bit	0	0	0	1	1	0	1	0	1	1	0	Rm					0	0	1	0	0	1	Rn					Rd				
ASRV	32-bit	0	0	0	1	1	0	1	0	1	1	0	Rm					0	0	1	0	1	0	Rn					Rd				
RORV	32-bit	0	0	0	1	1	0	1	0	1	1	0	Rm					0	0	1	0	1	1	Rn					Rd				
CRC32B, CRC32H, CR	CRC32B	0	0	0	1	1	0	1	0	1	1	0	Rm					0	1	0	0	0	0	Rn					Rd				
CRC32B, CRC32H, CR	CRC32H	0	0	0	1	1	0	1	0	1	1	0	Rm					0	1	0	0	0	1	Rn					Rd				
CRC32B, CRC32H, CR	CRC32W	0	0	0	1	1	0	1	0	1	1	0	Rm					0	1	0	0	1	0	Rn					Rd				
CRC32CB, CRC32CH,	CRC32CB	0	0	0	1	1	0	1	0	1	1	0	Rm					0	1	0	1	0	0	Rn					Rd				
CRC32CB, CRC32CH,	CRC32CH	0	0	0	1	1	0	1	0	1	1	0	Rm					0	1	0	1	0	1	Rn					Rd				
CRC32CB, CRC32CH,	CRC32CW	0	0	0	1	1	0	1	0	1	1	0	Rm					0	1	0	1	1	0	Rn					Rd				
UDIV	64-bit	1	0	0	1	1	0	1	0	1	1	0	Rm					0	0	0	0	1	0	Rn					Rd				
SDIV	64-bit	1	0	0	1	1	0	1	0	1	1	0	Rm					0	0	0	0	1	1	Rn					Rd				
LSLV	64-bit	1	0	0	1	1	0	1	0	1	1	0	Rm					0	0	1	0	0	0	Rn					Rd				
LSRV	64-bit	1	0	0	1	1	0	1	0	1	1	0	Rm					0	0	1	0	0	1	Rn					Rd				
ASRV	64-bit	1	0	0	1	1	0	1	0	1	1	0	Rm					0	0	1	0	1	0	Rn					Rd				
RORV	64-bit	1	0	0	1	1	0	1	0	1	1	0	Rm					0	0	1	0	1	1	Rn					Rd				
CRC32B, CRC32H, CR	CRC32X	1	0	0	1	1	0	1	0	1	1	0	Rm					0	1	0	0	1	1	Rn					Rd				
CRC32CB, CRC32CH,	CRC32CX	1	0	0	1	1	0	1	0	1	1	0	Rm					0	1	0	1	1	1	Rn					Rd				
Data-processing (1 source)		**sf**	**1**	**S**	**1**	**1**	**0**	**1**	**0**	**1**	**1**	**0**	**opcode2**					**opcode**						**Rn**					**Rd**				

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RBIT	32-bit	0	1	0	1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0			Rn					Rd		
REV16	32-bit	0	1	0	1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1			Rn					Rd		
REV	32-bit	0	1	0	1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0			Rn					Rd		
CLZ	32-bit	0	1	0	1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0			Rn					Rd		
CLS	32-bit	0	1	0	1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	1	0	1			Rn					Rd		
RBIT	64-bit	1	1	0	1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0			Rn					Rd		
REV16	64-bit	1	1	0	1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1			Rn					Rd		
REV32	-	1	1	0	1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0			Rn					Rd		
REV	64-bit	1	1	0	1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	1	1			Rn					Rd		
CLZ	64-bit	1	1	0	1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0			Rn					Rd		
CLS	64-bit	1	1	0	1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	1	0	1			Rn					Rd		
Data Processing – SIMD and floating point						**1**	**1**	**1**																									
Floating-point<->fixed-point conversions		**sf**	**0**	**S**	**1**	**1**	**1**	**1**	**0**	**type**		**0**	**rmode**		**opcode**			**scale**								**Rn**					**Rd**		
SCVTF (scalar, fixed-pc	32-bit to single-precision	0	0	0	1	1	1	1	0	0	0	0	0	0	0	1	0	-	-	-	-	-	-			Rn					Rd		
UCVTF (scalar, fixed-pc	32-bit to single-precision	0	0	0	1	1	1	1	0	0	0	0	0	0	0	1	1	-	-	-	-	-	-			Rn					Rd		
FCVTZS (scalar, fixed-p	Single-precision to 32-bit	0	0	0	1	1	1	1	0	1	1	0	1	1	0	0	0	-	-	-	-	-	-			Rn					Rd		
FCVTZU (scalar, fixed-p	Single-precision to 32-bit	0	0	0	1	1	1	1	0	1	1	0	1	1	0	0	1	-	-	-	-	-	-			Rn					Rd		
SCVTF (scalar, fixed-pc	32-bit to double-precision	0	0	0	1	1	1	1	0	0	0	0	0	0	0	1	0	-	-	-	-	-	-			Rn					Rd		
UCVTF (scalar, fixed-pc	32-bit to double-precision	0	0	0	1	1	1	1	0	0	0	0	0	0	0	1	1	-	-	-	-	-	-			Rn					Rd		
FCVTZS (scalar, fixed-p	Double-precision to 32-bit	0	0	0	1	1	1	1	0	1	1	0	1	1	0	0	0	-	-	-	-	-	-			Rn					Rd		
FCVTZU (scalar, fixed-p	Double-precision to 32-bit	0	0	0	1	1	1	1	0	1	1	0	1	1	0	0	1	-	-	-	-	-	-			Rn					Rd		
SCVTF (scalar, fixed-pc	64-bit to single-precision	1	0	0	1	1	1	1	0	0	0	0	0	0	0	1	0	-	-	-	-	-	-			Rn					Rd		
UCVTF (scalar, fixed-pc	64-bit to single-precision	1	0	0	1	1	1	1	0	0	0	0	0	0	0	1	1	-	-	-	-	-	-			Rn					Rd		
FCVTZS (scalar, fixed-p	Single-precision to 64-bit	1	0	0	1	1	1	1	0	1	1	0	1	1	0	0	0	-	-	-	-	-	-			Rn					Rd		
FCVTZU (scalar, fixed-p	Single-precision to 64-bit	1	0	0	1	1	1	1	0	1	1	0	1	1	0	0	1	-	-	-	-	-	-			Rn					Rd		
SCVTF (scalar, fixed-pc	64-bit to double-precision	1	0	0	1	1	1	1	0	0	0	0	0	0	0	1	0	-	-	-	-	-	-			Rn					Rd		
UCVTF (scalar, fixed-pc	64-bit to double-precision	1	0	0	1	1	1	1	0	0	0	0	0	0	0	1	1	-	-	-	-	-	-			Rn					Rd		
FCVTZS (scalar, fixed-p	Double-precision to 64-bit	1	0	0	1	1	1	1	0	1	1	0	1	1	0	0	0	-	-	-	-	-	-			Rn					Rd		
FCVTZU (scalar, fixed-p	Double-precision to 64-bit	1	0	0	1	1	1	1	0	1	1	0	1	1	0	0	1	-	-	-	-	-	-			Rn					Rd		
Floating-point conditional compare		**M**	**0**	**S**	**1**	**1**	**1**	**1**	**0**	**type**		**1**			**Rm**			**cond**				**0**	**1**			**Rn**			**op**		**nzcv**		
FCCMP	Single-precision	0	0	0	1	1	1	1	0	0	0	1			Rm			cond				0	1			Rn			0		nzcv		
FCCMPE	Single-precision	0	0	0	1	1	1	1	0	0	0	1			Rm			cond				0	1			Rn			1		nzcv		
FCCMP	Double-precision	0	0	0	1	1	1	1	0	0	1	1			Rm			cond				0	1			Rn			0		nzcv		
FCCMPE	Double-precision	0	0	0	1	1	1	1	0	0	1	1			Rm			cond				0	1			Rn			1		nzcv		
Floating-point data-processing (2 source)		**M**	**0**	**S**	**1**	**1**	**1**	**1**	**0**	**type**		**1**			**Rm**			**opcode**				**1**	**0**			**Rn**					**Rd**		
FMUL (scalar)	Single-precision	0	0	0	1	1	1	1	0	0	0	1			Rm			0	0	0	0	1	0			Rn					Rd		
FDIV (scalar)	Single-precision	0	0	0	1	1	1	1	0	0	0	1			Rm			0	0	0	1	1	0			Rn					Rd		
FADD (scalar)	Single-precision	0	0	0	1	1	1	1	0	0	0	1			Rm			0	0	1	0	1	0			Rn					Rd		
FSUB (scalar)	Single-precision	0	0	0	1	1	1	1	0	0	0	1			Rm			0	0	1	1	1	0			Rn					Rd		
FMAX (scalar)	Single-precision	0	0	0	1	1	1	1	0	0	0	1			Rm			0	1	0	0	1	0			Rn					Rd		
FMIN (scalar)	Single-precision	0	0	0	1	1	1	1	0	0	0	1			Rm			0	1	0	1	1	0			Rn					Rd		
FMAXNM (scalar)	Single-precision	0	0	0	1	1	1	1	0	0	0	1			Rm			0	1	1	0	1	0			Rn					Rd		
FMINNM (scalar)	Single-precision	0	0	0	1	1	1	1	0	0	0	1			Rm			0	1	1	1	1	0			Rn					Rd		

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FNMUL	Single-precision	0	0	0	1	1	1	1	0	0	0	1			Rm			1	0	0	0	1	0			Rn					Rd		
FMUL (scalar)	Double-precision	0	0	0	1	1	1	1	0	0	1	1			Rm			0	0	0	0	1	0			Rn					Rd		
FDIV (scalar)	Double-precision	0	0	0	1	1	1	1	0	0	1	1			Rm			0	0	0	1	1	0			Rn					Rd		
FADD (scalar)	Double-precision	0	0	0	1	1	1	1	0	0	1	1			Rm			0	0	1	0	1	0			Rn					Rd		
FSUB (scalar)	Double-precision	0	0	0	1	1	1	1	0	0	1	1			Rm			0	0	1	1	1	0			Rn					Rd		
FMAX (scalar)	Double-precision	0	0	0	1	1	1	1	0	0	1	1			Rm			0	1	0	0	1	0			Rn					Rd		
FMIN (scalar)	Double-precision	0	0	0	1	1	1	1	0	0	1	1			Rm			0	1	0	1	1	0			Rn					Rd		
FMAXNM (scalar)	Double-precision	0	0	0	1	1	1	1	0	0	1	1			Rm			0	1	1	0	1	0			Rn					Rd		
FMINNM (scalar)	Double-precision	0	0	0	1	1	1	1	0	0	1	1			Rm			0	1	1	1	1	0			Rn					Rd		
FNMUL	Double-precision	0	0	0	1	1	1	1	0	0	1	1			Rm			1	0	0	0	1	0			Rn					Rd		
Floating-point conditional select		**M**	**0**	**S**	**1**	**1**	**1**	**1**	**0**	**type**		**1**			**Rm**			**cond**				**1**	**1**			**Rn**					**Rd**		
FCSEL	Single-precision	0	0	0	1	1	1	1	0	0	0	1			Rm			cond				1	1			Rn					Rd		
FCSEL	Double-precision	0	0	0	1	1	1	1	0	0	1	1			Rm			cond				1	1			Rn					Rd		
Floating-point immediate		**M**	**0**	**S**	**1**	**1**	**1**	**1**	**0**	**type**		**1**			**imm8**						**1**	**0**	**0**			**imm5**					**Rd**		
FMOV (scalar, immedia	Single-precision	0	0	0	1	1	1	1	0	0	0	1			imm8						1	0	0	0	0	0	0	0			Rd		
FMOV (scalar, immedia	Double-precision	0	0	0	1	1	1	1	0	0	1	1			imm8						1	0	0	0	0	0	0	0			Rd		
Floating-point compare		**M**	**0**	**S**	**1**	**1**	**1**	**1**	**0**	**type**		**1**			**Rm**			**op**		**1**	**0**	**0**	**0**			**Rn**			**opcode2**				
FCMP	Single-precision	0	0	0	1	1	1	1	0	0	0	1			Rm			0	0	1	0	0	0			Rn			0	0	0	0	0
FCMP	Single-precision, zero	0	0	0	1	1	1	1	0	0	0	1			Rm			0	0	1	0	0	0			Rn			0	1	0	0	0
FCMPE	Single-precision	0	0	0	1	1	1	1	0	0	0	1			Rm			0	0	1	0	0	0			Rn			1	0	0	0	0
FCMPE	Single-precision, zero	0	0	0	1	1	1	1	0	0	0	1			Rm			0	0	1	0	0	0			Rn			1	1	0	0	0
FCMP	Double-precision	0	0	0	1	1	1	1	0	0	1	1			Rm			0	0	1	0	0	0			Rn			0	0	0	0	0
FCMP	Double-precision, zero	0	0	0	1	1	1	1	0	0	1	1			Rm			0	0	1	0	0	0			Rn			0	1	0	0	0
FCMPE	Double-precision	0	0	0	1	1	1	1	0	0	1	1			Rm			0	0	1	0	0	0			Rn			1	0	0	0	0
FCMPE	Double-precision, zero	0	0	0	1	1	1	1	0	0	1	1			Rm			0	0	1	0	0	0			Rn			1	1	0	0	0
Floating-point data-processing (1 source)		**M**	**0**	**S**	**1**	**1**	**1**	**1**	**0**	**type**		**1**			**opcode**					**1**	**0**	**0**	**0**			**Rn**					**Rd**		
FMOV (register)	Single-precision	0	0	0	1	1	1	1	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0			Rn					Rd		
FABS (scalar)	Single-precision	0	0	0	1	1	1	1	0	0	0	1	0	0	0	0	0	1	1	0	0	0	0			Rn					Rd		
FNEG (scalar)	Single-precision	0	0	0	1	1	1	1	0	0	0	1	0	0	0	0	1	0	1	0	0	0	0			Rn					Rd		
FSQRT (scalar)	Single-precision	0	0	0	1	1	1	1	0	0	0	1	0	0	0	0	1	1	1	0	0	0	0			Rn					Rd		
FCVT	Single-precision to double-precision	0	0	0	1	1	1	1	0	0	0	1	0	0	0	1	0	1	1	0	0	0	0			Rn					Rd		
FCVT	Single-precision to half-precision	0	0	0	1	1	1	1	0	0	0	1	0	0	0	1	1	1	1	0	0	0	0			Rn					Rd		
FRINTN (scalar)	Single-precision	0	0	0	1	1	1	1	0	0	0	1	0	0	1	0	0	0	1	0	0	0	0			Rn					Rd		
FRINTP (scalar)	Single-precision	0	0	0	1	1	1	1	0	0	0	1	0	0	1	0	0	1	1	0	0	0	0			Rn					Rd		
FRINTM (scalar)	Single-precision	0	0	0	1	1	1	1	0	0	0	1	0	0	1	0	1	0	1	0	0	0	0			Rn					Rd		
FRINTZ (scalar)	Single-precision	0	0	0	1	1	1	1	0	0	0	1	0	0	1	0	1	1	1	0	0	0	0			Rn					Rd		
FRINTA (scalar)	Single-precision	0	0	0	1	1	1	1	0	0	0	1	0	0	1	1	0	0	1	0	0	0	0			Rn					Rd		
FRINTX (scalar)	Single-precision	0	0	0	1	1	1	1	0	0	0	1	0	0	1	1	1	0	1	0	0	0	0			Rn					Rd		
FRINTI (scalar)	Single-precision	0	0	0	1	1	1	1	0	0	0	1	0	0	1	1	1	1	1	0	0	0	0			Rn					Rd		
FMOV (register)	Double-precision	0	0	0	1	1	1	1	0	0	1	1	0	0	0	0	0	0	1	0	0	0	0			Rn					Rd		
FABS (scalar)	Double-precision	0	0	0	1	1	1	1	0	0	1	1	0	0	0	0	0	1	1	0	0	0	0			Rn					Rd		
FNEG (scalar)	Double-precision	0	0	0	1	1	1	1	0	0	1	1	0	0	0	0	1	0	1	0	0	0	0			Rn					Rd		
FSQRT (scalar)	Double-precision	0	0	0	1	1	1	1	0	0	1	1	0	0	0	0	1	1	1	0	0	0	0			Rn					Rd		

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FCVT	Double-precision to single-precision	0	0	0	1	1	1	1	0	0	1	1	0	0	0	1	0	1	1	0	0	0	0	Rn					Rd				
FCVT	Double-precision to half-precision	0	0	0	1	1	1	1	0	0	1	1	0	0	0	1	1	1	1	0	0	0	0	Rn					Rd				
FRINTN (scalar)	Double-precision	0	0	0	1	1	1	1	0	0	1	1	0	0	1	0	0	0	1	0	0	0	0	Rn					Rd				
FRINTP (scalar)	Double-precision	0	0	0	1	1	1	1	0	0	1	1	0	0	1	0	0	1	1	0	0	0	0	Rn					Rd				
FRINTM (scalar)	Double-precision	0	0	0	1	1	1	1	0	0	1	1	0	0	1	0	1	0	1	0	0	0	0	Rn					Rd				
FRINTZ (scalar)	Double-precision	0	0	0	1	1	1	1	0	0	1	1	0	0	1	0	1	1	1	0	0	0	0	Rn					Rd				
FRINTA (scalar)	Double-precision	0	0	0	1	1	1	1	0	0	1	1	0	0	1	1	0	0	1	0	0	0	0	Rn					Rd				
FRINTX (scalar)	Double-precision	0	0	0	1	1	1	1	0	0	1	1	0	0	1	1	1	0	1	0	0	0	0	Rn					Rd				
FRINTI (scalar)	Double-precision	0	0	0	1	1	1	1	0	0	1	1	0	0	1	1	1	1	1	0	0	0	0	Rn					Rd				
FCVT	Half-precision to single-precision	0	0	0	1	1	1	1	0	1	1	1	0	0	0	1	0	0	1	0	0	0	0	Rn					Rd				
FCVT	Half-precision to double-precision	0	0	0	1	1	1	1	0	1	1	1	0	0	0	1	0	1	1	0	0	0	0	Rn					Rd				
Floating-point<->integer conversions		**sf**	**0**	**S**	**1**	**1**	**1**	**1**	**0**	**type**		**1**	**rmode**		**opcode**			**0**	**0**	**0**	**0**	**0**	**0**	**Rn**					**Rd**				
FCVTNS (scalar)	Single-precision to 32-bit	0	0	0	1	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	Rn					Rd				
FCVTNU (scalar)	Single-precision to 32-bit	0	0	0	1	1	1	1	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	Rn					Rd				
SCVTF (scalar, integer)	32-bit to single-precision	0	0	0	1	1	1	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	Rn					Rd				
UCVTF (scalar, integer)	32-bit to single-precision	0	0	0	1	1	1	1	0	0	0	1	0	0	0	1	1	0	0	0	0	0	0	Rn					Rd				
FCVTAS (scalar)	Single-precision to 32-bit	0	0	0	1	1	1	1	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	Rn					Rd				
FCVTAU (scalar)	Single-precision to 32-bit	0	0	0	1	1	1	1	0	0	0	1	0	0	1	0	1	0	0	0	0	0	0	Rn					Rd				
FMOV (general)	Single-precision to 32-bit	0	0	0	1	1	1	1	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	Rn					Rd				
FMOV (general)	32-bit to single-precision	0	0	0	1	1	1	1	0	0	0	1	0	0	1	1	1	0	0	0	0	0	0	Rn					Rd				
FCVTPS (scalar)	Single-precision to 32-bit	0	0	0	1	1	1	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	Rn					Rd				
FCVTPU (scalar)	Single-precision to 32-bit	0	0	0	1	1	1	1	0	0	0	1	0	1	0	0	1	0	0	0	0	0	0	Rn					Rd				
FCVTMS (scalar)	Single-precision to 32-bit	0	0	0	1	1	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	Rn					Rd				
FCVTMU (scalar)	Single-precision to 32-bit	0	0	0	1	1	1	1	0	0	0	1	1	0	0	0	1	0	0	0	0	0	0	Rn					Rd				
FCVTZS (scalar, intege	Single-precision to 32-bit	0	0	0	1	1	1	1	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	Rn					Rd				
FCVTZU (scalar, intege	Single-precision to 32-bit	0	0	0	1	1	1	1	0	0	0	1	1	1	0	0	1	0	0	0	0	0	0	Rn					Rd				
FCVTNS (scalar)	Double-precision to 32-bit	0	0	0	1	1	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	Rn					Rd				
FCVTNU (scalar)	Double-precision to 32-bit	0	0	0	1	1	1	1	0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	Rn					Rd				
SCVTF (scalar, integer)	32-bit to double-precision	0	0	0	1	1	1	1	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	Rn					Rd				
UCVTF (scalar, integer)	32-bit to double-precision	0	0	0	1	1	1	1	0	0	1	1	0	0	0	1	1	0	0	0	0	0	0	Rn					Rd				
FCVTAS (scalar)	Double-precision to 32-bit	0	0	0	1	1	1	1	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	Rn					Rd				
FCVTAU (scalar)	Double-precision to 32-bit	0	0	0	1	1	1	1	0	0	1	1	0	0	1	0	1	0	0	0	0	0	0	Rn					Rd				
FCVTPS (scalar)	Double-precision to 32-bit	0	0	0	1	1	1	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	Rn					Rd				
FCVTPU (scalar)	Double-precision to 32-bit	0	0	0	1	1	1	1	0	0	1	1	0	1	0	0	1	0	0	0	0	0	0	Rn					Rd				
FCVTMS (scalar)	Double-precision to 32-bit	0	0	0	1	1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	Rn					Rd				
FCVTMU (scalar)	Double-precision to 32-bit	0	0	0	1	1	1	1	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0	Rn					Rd				
FCVTZS (scalar, intege	Double-precision to 32-bit	0	0	0	1	1	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	Rn					Rd				
FCVTZU (scalar, intege	Double-precision to 32-bit	0	0	0	1	1	1	1	0	0	1	1	1	1	0	0	1	0	0	0	0	0	0	Rn					Rd				
FCVTNS (scalar)	Single-precision to 64-bit	1	0	0	1	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	Rn					Rd				
FCVTNU (scalar)	Single-precision to 64-bit	1	0	0	1	1	1	1	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	Rn					Rd				
SCVTF (scalar, integer)	64-bit to single-precision	1	0	0	1	1	1	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	Rn					Rd				
UCVTF (scalar, integer)	64-bit to single-precision	1	0	0	1	1	1	1	0	0	0	1	0	0	0	1	1	0	0	0	0	0	0	Rn					Rd				
FCVTAS (scalar)	Single-precision to 64-bit	1	0	0	1	1	1	1	0	0	0	1	0	0	1	0	0	0	14	0	0	0	0	Rn					Rd				

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FCVTAU (scalar)	Single-precision to 64-bit	1	0	0	1	1	1	1	0	0	0	1	0	0	1	0	1	0	0	0	0	0	0	Rn					Rd				
FCVTPS (scalar)	Single-precision to 64-bit	1	0	0	1	1	1	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	Rn					Rd				
FCVTPU (scalar)	Single-precision to 64-bit	1	0	0	1	1	1	1	0	0	0	1	0	1	0	0	1	0	0	0	0	0	0	Rn					Rd				
FCVTMS (scalar)	Single-precision to 64-bit	1	0	0	1	1	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	Rn					Rd				
FCVTMU (scalar)	Single-precision to 64-bit	1	0	0	1	1	1	1	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0	Rn					Rd				
FCVTZS (scalar, intege	Single-precision to 64-bit	1	0	0	1	1	1	1	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	Rn					Rd				
FCVTZU (scalar, intege	Single-precision to 64-bit	1	0	0	1	1	1	1	0	0	0	1	1	1	0	0	1	0	0	0	0	0	0	Rn					Rd				
FCVTNS (scalar)	Double-precision to 64-bit	1	0	0	1	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	Rn					Rd				
FCVTNU (scalar)	Double-precision to 64-bit	1	0	0	1	1	1	1	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	Rn					Rd				
SCVTF (scalar, integer)	64-bit to double-precision	1	0	0	1	1	1	1	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	Rn					Rd				
UCVTF (scalar, integer)	64-bit to double-precision	1	0	0	1	1	1	1	0	0	1	1	0	0	0	1	1	0	0	0	0	0	0	Rn					Rd				
FCVTAS (scalar)	Double-precision to 64-bit	1	0	0	1	1	1	1	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	Rn					Rd				
FCVTAU (scalar)	Double-precision to 64-bit	1	0	0	1	1	1	1	0	0	1	1	0	0	1	0	1	0	0	0	0	0	0	Rn					Rd				
FMOV (general)	Double-precision to 64-bit	1	0	0	1	1	1	1	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	Rn					Rd				
FMOV (general)	64-bit to double-precision	1	0	0	1	1	1	1	0	0	1	1	0	0	1	1	1	0	0	0	0	0	0	Rn					Rd				
FCVTPS (scalar)	Double-precision to 64-bit	1	0	0	1	1	1	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	Rn					Rd				
FCVTPU (scalar)	Double-precision to 64-bit	1	0	0	1	1	1	1	0	0	1	1	0	1	0	0	1	0	0	0	0	0	0	Rn					Rd				
FCVTMS (scalar)	Double-precision to 64-bit	1	0	0	1	1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	Rn					Rd				
FCVTMU (scalar)	Double-precision to 64-bit	1	0	0	1	1	1	1	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0	Rn					Rd				
FCVTZS (scalar, intege	Double-precision to 64-bit	1	0	0	1	1	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	Rn					Rd				
FCVTZU (scalar, intege	Double-precision to 64-bit	1	0	0	1	1	1	1	0	0	1	1	1	1	0	0	1	0	0	0	0	0	0	Rn					Rd				
FMOV (general)	Top half of 128-bit to 64-bit	1	0	0	1	1	1	1	0	1	0	1	0	1	1	1	0	0	0	0	0	0	0	Rn					Rd				
FMOV (general)	64-bit to top half of 128-bit	1	0	0	1	1	1	1	0	1	0	1	0	1	1	1	1	0	0	0	0	0	0	Rn					Rd				
Floating-point data-processing (3 source)		**M**	**0**	**S**	**1**	**1**	**1**	**1**	**1**	**type**		**o1**			**Rm**			**o0**			**Ra**			**Rn**					**Rd**				
FMADD	Single-precision	0	0	0	1	1	1	1	1	0	0	0			Rm			0			Ra			Rn					Rd				
FMSUB	Single-precision	0	0	0	1	1	1	1	1	0	0	0			Rm			1			Ra			Rn					Rd				
FNMADD	Single-precision	0	0	0	1	1	1	1	1	0	0	1			Rm			0			Ra			Rn					Rd				
FNMSUB	Single-precision	0	0	0	1	1	1	1	1	0	0	1			Rm			1			Ra			Rn					Rd				
FMADD	Double-precision	0	0	0	1	1	1	1	1	0	1	0			Rm			0			Ra			Rn					Rd				
FMSUB	Double-precision	0	0	0	1	1	1	1	1	0	1	0			Rm			1			Ra			Rn					Rd				
FNMADD	Double-precision	0	0	0	1	1	1	1	1	0	1	1			Rm			0			Ra			Rn					Rd				
FNMSUB	Double-precision	0	0	0	1	1	1	1	1	0	1	1			Rm			1			Ra			Rn					Rd				
AdvSIMD scalar three same		**0**	**1**	**U**	**1**	**1**	**1**	**1**	**0**	**size**		**1**			**Rm**			**opcode**					**1**	**Rn**					**Rd**				
SQADD	Scalar	0	1	0	1	1	1	1	0	-	-	1			Rm			0	0	0	0	1	1	Rn					Rd				
SQSUB	Scalar	0	1	0	1	1	1	1	0	-	-	1			Rm			0	0	1	0	1	1	Rn					Rd				
CMGT (register)	Scalar	0	1	0	1	1	1	1	0	-	-	1			Rm			0	0	1	1	0	1	Rn					Rd				
CMGE (register)	Scalar	0	1	0	1	1	1	1	0	-	-	1			Rm			0	0	1	1	1	1	Rn					Rd				
SSHL	Scalar	0	1	0	1	1	1	1	0	-	-	1			Rm			0	1	0	0	0	1	Rn					Rd				
SQSHL (register)	Scalar	0	1	0	1	1	1	1	0	-	-	1			Rm			0	1	0	0	1	1	Rn					Rd				
SRSHL	Scalar	0	1	0	1	1	1	1	0	-	-	1			Rm			0	1	0	1	0	1	Rn					Rd				
SQRSHL	Scalar	0	1	0	1	1	1	1	0	-	-	1			Rm			0	1	0	1	1	1	Rn					Rd				
ADD (vector)	Scalar	0	1	0	1	1	1	1	0	-	-	1			Rm			1	0	0	0	0	1	Rn					Rd				
CMTST	Scalar	0	1	0	1	1	1	1	0	-	-	1			Rm			1	0	0	0	1	1	Rn					Rd				

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SQDMULH (vector)	Scalar	0	1	0	1	1	1	1	0	-	-	1			Rm			1	0	1	1	0	1			Rn					Rd		
FMULX	Scalar	0	1	0	1	1	1	1	0	0	x	1			Rm			1	1	0	1	1	1			Rn					Rd		
FCMEQ (register)	Scalar	0	1	0	1	1	1	1	0	0	x	1			Rm			1	1	1	0	0	1			Rn					Rd		
FRECPS	Scalar	0	1	0	1	1	1	1	0	0	x	1			Rm			1	1	1	1	1	1			Rn					Rd		
FRSQRTS	Scalar	0	1	0	1	1	1	1	0	1	x	1			Rm			1	1	1	1	1	1			Rn					Rd		
UQADD	Scalar	0	1	1	1	1	1	1	0	-	-	1			Rm			0	0	0	0	1	1			Rn					Rd		
UQSUB	Scalar	0	1	1	1	1	1	1	0	-	-	1			Rm			0	0	1	0	1	1			Rn					Rd		
CMHI (register)	Scalar	0	1	1	1	1	1	1	0	-	-	1			Rm			0	0	1	1	0	1			Rn					Rd		
CMHS (register)	Scalar	0	1	1	1	1	1	1	0	-	-	1			Rm			0	0	1	1	1	1			Rn					Rd		
USHL	Scalar	0	1	1	1	1	1	1	0	-	-	1			Rm			0	1	0	0	0	1			Rn					Rd		
UQSHL (register)	Scalar	0	1	1	1	1	1	1	0	-	-	1			Rm			0	1	0	0	1	1			Rn					Rd		
URSHL	Scalar	0	1	1	1	1	1	1	0	-	-	1			Rm			0	1	0	1	0	1			Rn					Rd		
UQRSHL	Scalar	0	1	1	1	1	1	1	0	-	-	1			Rm			0	1	0	1	1	1			Rn					Rd		
SUB (vector)	Scalar	0	1	1	1	1	1	1	0	-	-	1			Rm			1	0	0	0	0	1			Rn					Rd		
CMEQ (register)	Scalar	0	1	1	1	1	1	1	0	-	-	1			Rm			1	0	0	0	1	1			Rn					Rd		
SQRDMULH (vector)	Scalar	0	1	1	1	1	1	1	0	-	-	1			Rm			1	0	1	1	0	1			Rn					Rd		
FCMGE (register)	Scalar	0	1	1	1	1	1	1	0	0	x	1			Rm			1	1	1	0	0	1			Rn					Rd		
FACGE	Scalar	0	1	1	1	1	1	1	0	0	x	1			Rm			1	1	1	0	1	1			Rn					Rd		
FABD	Scalar	0	1	1	1	1	1	1	0	1	x	1			Rm			1	1	0	1	0	1			Rn					Rd		
FCMGT (register)	Scalar	0	1	1	1	1	1	1	0	1	x	1			Rm			1	1	1	0	0	1			Rn					Rd		
FACGT	Scalar	0	1	1	1	1	1	1	0	1	x	1			Rm			1	1	1	0	1	1			Rn					Rd		
AdvSIMD scalar three different		**0**	**1**	**U**	**1**	**1**	**1**	**1**	**0**	**size**		**1**			**Rm**			**opcode**				**0**	**0**			**Rn**					**Rd**		
SQDMLAL, SQDMLAL2	Scalar	0	1	0	1	1	1	1	0	size		1			Rm			1	0	0	1	0	0			Rn					Rd		
SQDMLSL, SQDMLSL2	Scalar	0	1	0	1	1	1	1	0	size		1			Rm			1	0	1	1	0	0			Rn					Rd		
SQDMULL, SQDMULL2	Scalar	0	1	0	1	1	1	1	0	size		1			Rm			1	1	0	1	0	0			Rn					Rd		
AdvSIMD scalar two-reg misc		**0**	**1**	**U**	**1**	**1**	**1**	**1**	**0**	**size**		**1**	**0**	**0**	**0**	**0**	**opcode**					**1**	**0**			**Rn**					**Rd**		
SUQADD	Scalar	0	1	0	1	1	1	1	0	-	-	1	0	0	0	0	0	0	0	1	1	1	0			Rn					Rd		
SQABS	Scalar	0	1	0	1	1	1	1	0	-	-	1	0	0	0	0	0	0	1	1	1	1	0			Rn					Rd		
CMGT (zero)	Scalar	0	1	0	1	1	1	1	0	-	-	1	0	0	0	0	0	1	0	0	0	1	0			Rn					Rd		
CMEQ (zero)	Scalar	0	1	0	1	1	1	1	0	-	-	1	0	0	0	0	0	1	0	0	1	1	0			Rn					Rd		
CMLT (zero)	Scalar	0	1	0	1	1	1	1	0	-	-	1	0	0	0	0	0	1	0	1	0	1	0			Rn					Rd		
ABS	Scalar	0	1	0	1	1	1	1	0	-	-	1	0	0	0	0	0	1	0	1	1	1	0			Rn					Rd		
SQXTN, SQXTN2	Scalar	0	1	0	1	1	1	1	0	-	-	1	0	0	0	0	1	0	1	0	0	1	0			Rn					Rd		
FCVTNS (vector)	Scalar	0	1	0	1	1	1	1	0	0	x	1	0	0	0	0	1	1	0	1	0	1	0			Rn					Rd		
FCVTMS (vector)	Scalar	0	1	0	1	1	1	1	0	0	x	1	0	0	0	0	1	1	0	1	1	1	0			Rn					Rd		
FCVTAS (vector)	Scalar	0	1	0	1	1	1	1	0	0	x	1	0	0	0	0	1	1	1	0	0	1	0			Rn					Rd		
SCVTF (vector, integer)	Scalar	0	1	0	1	1	1	1	0	0	x	1	0	0	0	0	1	1	1	0	1	1	0			Rn					Rd		
FCMGT (zero)	Scalar	0	1	0	1	1	1	1	0	1	x	1	0	0	0	0	0	1	1	0	0	1	0			Rn					Rd		
FCMEQ (zero)	Scalar	0	1	0	1	1	1	1	0	1	x	1	0	0	0	0	0	1	1	0	1	1	0			Rn					Rd		
FCMLT (zero)	Scalar	0	1	0	1	1	1	1	0	1	x	1	0	0	0	0	0	1	1	1	0	1	0			Rn					Rd		
FCVTPS (vector)	Scalar	0	1	0	1	1	1	1	0	1	x	1	0	0	0	0	1	1	0	1	0	1	0			Rn					Rd		
FCVTZS (vector, intege	Scalar	0	1	0	1	1	1	1	0	1	x	1	0	0	0	0	1	1	0	1	1	1	0			Rn					Rd		
FRECPE	Scalar	0	1	0	1	1	1	1	0	1	x	1	0	0	0	0	1	1	1	0	1	1	0			Rn					Rd		

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FRECPX	-	0	1	0	1	1	1	1	0	1	x	1	0	0	0	0	1	1	1	1	1	1	0	Rn					Rd				
USQADD	Scalar	0	1	1	1	1	1	1	0	-	-	1	0	0	0	0	0	0	0	1	1	1	0	Rn					Rd				
SQNEG	Scalar	0	1	1	1	1	1	1	0	-	-	1	0	0	0	0	0	0	1	1	1	1	0	Rn					Rd				
CMGE (zero)	Scalar	0	1	1	1	1	1	1	0	-	-	1	0	0	0	0	0	1	0	0	0	1	0	Rn					Rd				
CMLE (zero)	Scalar	0	1	1	1	1	1	1	0	-	-	1	0	0	0	0	0	1	0	0	1	1	0	Rn					Rd				
NEG (vector)	Scalar	0	1	1	1	1	1	1	0	-	-	1	0	0	0	0	0	1	0	1	1	1	0	Rn					Rd				
SQXTUN, SQXTUN2	Scalar	0	1	1	1	1	1	1	0	-	-	1	0	0	0	0	1	0	0	1	0	1	0	Rn					Rd				
UQXTN, UQXTN2	Scalar	0	1	1	1	1	1	1	0	-	-	1	0	0	0	0	1	0	1	0	0	1	0	Rn					Rd				
FCVTXN, FCVTXN2	Scalar	0	1	1	1	1	1	1	0	0	x	1	0	0	0	0	1	0	1	1	0	1	0	Rn					Rd				
FCVTNU (vector)	Scalar	0	1	1	1	1	1	1	0	0	x	1	0	0	0	0	1	1	0	1	0	1	0	Rn					Rd				
FCVTMU (vector)	Scalar	0	1	1	1	1	1	1	0	0	x	1	0	0	0	0	1	1	0	1	1	1	0	Rn					Rd				
FCVTAU (vector)	Scalar	0	1	1	1	1	1	1	0	0	x	1	0	0	0	0	1	1	1	0	0	1	0	Rn					Rd				
UCVTF (vector, integer)	Scalar	0	1	1	1	1	1	1	0	0	x	1	0	0	0	0	1	1	1	0	1	1	0	Rn					Rd				
FCMGE (zero)	Scalar	0	1	1	1	1	1	1	0	1	x	1	0	0	0	0	0	1	1	0	0	1	0	Rn					Rd				
FCMLE (zero)	Scalar	0	1	1	1	1	1	1	0	1	x	1	0	0	0	0	0	1	1	0	1	1	0	Rn					Rd				
FCVTPU (vector)	Scalar	0	1	1	1	1	1	1	0	1	x	1	0	0	0	0	1	1	0	1	0	1	0	Rn					Rd				
FCVTZU (vector, intege	Scalar	0	1	1	1	1	1	1	0	1	x	1	0	0	0	0	1	1	0	1	1	1	0	Rn					Rd				
FRSQRTE	Scalar	0	1	1	1	1	1	1	0	1	x	1	0	0	0	0	1	1	1	0	1	1	0	Rn					Rd				
AdvSIMD scalar pairwise		**0**	**1**	**U**	**1**	**1**	**1**	**1**	**0**	**size**		**1**	**1**	**0**	**0**	**0**	**opcode**					**1**	**0**	**Rn**					**Rd**				
ADDP (scalar)	-	0	1	0	1	1	1	1	0	-	-	1	1	0	0	0	1	1	0	1	1	1	0	Rn					Rd				
FMAXNMP (scalar)	-	0	1	1	1	1	1	1	0	0	x	1	1	0	0	0	0	1	1	0	0	1	0	Rn					Rd				
FADDP (scalar)	-	0	1	1	1	1	1	1	0	0	x	1	1	0	0	0	0	1	1	0	1	1	0	Rn					Rd				
FMAXP (scalar)	-	0	1	1	1	1	1	1	0	0	x	1	1	0	0	0	0	1	1	1	1	1	0	Rn					Rd				
FMINNMP (scalar)	-	0	1	1	1	1	1	1	0	1	x	1	1	0	0	0	0	1	1	0	0	1	0	Rn					Rd				
FMINP (scalar)	-	0	1	1	1	1	1	1	0	1	x	1	1	0	0	0	0	1	1	1	1	1	0	Rn					Rd				
AdvSIMD scalar copy		**0**	**1**	**op**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**imm5**					**0**	**imm4**				**1**	**Rn**					**Rd**				
DUP (element)	Scalar	0	1	0	1	1	1	1	0	0	0	0	-	-	-	-	-	0	0	0	0	0	1	Rn					Rd				
AdvSIMD scalar x indexed element		**0**	**1**	**U**	**1**	**1**	**1**	**1**	**1**	**size**		**L**	**M**	**Rm**				**opcode**				**H**	**0**	**Rn**					**Rd**				
SQDMLAL, SQDMLAL2	Scalar	0	1	0	1	1	1	1	1	-	-	L	M	Rm				0	0	1	1	H	0	Rn					Rd				
SQDMLSL, SQDMLSL2	Scalar	0	1	0	1	1	1	1	1	-	-	L	M	Rm				0	1	1	1	H	0	Rn					Rd				
SQDMULL, SQDMULL2	Scalar	0	1	0	1	1	1	1	1	-	-	L	M	Rm				1	0	1	1	H	0	Rn					Rd				
SQDMULH (by elemen	Scalar	0	1	0	1	1	1	1	1	-	-	L	M	Rm				1	1	0	0	H	0	Rn					Rd				
SQRDMULH (by eleme	Scalar	0	1	0	1	1	1	1	1	-	-	L	M	Rm				1	1	0	1	H	0	Rn					Rd				
FMLA (by element)	Scalar	0	1	0	1	1	1	1	1	1	x	L	M	Rm				0	0	0	1	H	0	Rn					Rd				
FMLS (by element)	Scalar	0	1	0	1	1	1	1	1	1	x	L	M	Rm				0	1	0	1	H	0	Rn					Rd				
FMUL (by element)	Scalar	0	1	0	1	1	1	1	1	1	x	L	M	Rm				1	0	0	1	H	0	Rn					Rd				
FMULX (by element)	Scalar	0	1	1	1	1	1	1	1	1	x	L	M	Rm				1	0	0	1	H	0	Rn					Rd				
AdvSIMD scalar shift by immediate		**0**	**1**	**U**	**1**	**1**	**1**	**1**	**1**	**0**	**immh**				**immb**			**opcode**					**1**	**Rn**					**Rd**				
SSHR	Scalar	0	1	0	1	1	1	1	1	0	!=0000				immb			0	0	0	0	0	1	Rn					Rd				
SSRA	Scalar	0	1	0	1	1	1	1	1	0	!=0000				immb			0	0	0	1	0	1	Rn					Rd				
SRSHR	Scalar	0	1	0	1	1	1	1	1	0	!=0000				immb			0	0	1	0	0	1	Rn					Rd				
SRSRA	Scalar	0	1	0	1	1	1	1	1	0	!=0000				immb			0	0	1	1	0	1	Rn					Rd				
SHL	Scalar	0	1	0	1	1	1	1	1	0	!=0000				immb			0	1	0	1	0	1	Rn					Rd				

instruction page	variant	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SQSHL (immediate)	Scalar	0	1	0	1	1	1	1	1	0	!=0000				immb			0	1	1	1	0	1	Rn					Rd				
SQSHRN, SQSHRN2	Scalar	0	1	0	1	1	1	1	1	0	!=0000				immb			1	0	0	1	0	1	Rn					Rd				
SQRSHRN, SQRSHRN	Scalar	0	1	0	1	1	1	1	1	0	!=0000				immb			1	0	0	1	1	1	Rn					Rd				
SCVTF (vector, fixed-pc	Scalar	0	1	0	1	1	1	1	1	0	!=0000				immb			1	1	1	0	0	1	Rn					Rd				
FCVTZS (vector, fixed-p	Scalar	0	1	0	1	1	1	1	1	0	!=0000				immb			1	1	1	1	1	1	Rn					Rd				
USHR	Scalar	0	1	1	1	1	1	1	1	0	!=0000				immb			0	0	0	0	0	1	Rn					Rd				
USRA	Scalar	0	1	1	1	1	1	1	1	0	!=0000				immb			0	0	0	1	0	1	Rn					Rd				
URSHR	Scalar	0	1	1	1	1	1	1	1	0	!=0000				immb			0	0	1	0	0	1	Rn					Rd				
URSRA	Scalar	0	1	1	1	1	1	1	1	0	!=0000				immb			0	0	1	1	0	1	Rn					Rd				
SRI	Scalar	0	1	1	1	1	1	1	1	0	!=0000				immb			0	1	0	0	0	1	Rn					Rd				
SLI	Scalar	0	1	1	1	1	1	1	1	0	!=0000				immb			0	1	0	1	0	1	Rn					Rd				
SQSHLU	Scalar	0	1	1	1	1	1	1	1	0	!=0000				immb			0	1	1	0	0	1	Rn					Rd				
UQSHL (immediate)	Scalar	0	1	1	1	1	1	1	1	0	!=0000				immb			0	1	1	1	0	1	Rn					Rd				
SQSHRUN, SQSHRUN	Scalar	0	1	1	1	1	1	1	1	0	!=0000				immb			1	0	0	0	0	1	Rn					Rd				
SQRSHRUN, SQRSHR	Scalar	0	1	1	1	1	1	1	1	0	!=0000				immb			1	0	0	0	1	1	Rn					Rd				
UQSHRN	Scalar	0	1	1	1	1	1	1	1	0	!=0000				immb			1	0	0	1	0	1	Rn					Rd				
UQRSHRN, UQRSHRN	Scalar	0	1	1	1	1	1	1	1	0	!=0000				immb			1	0	0	1	1	1	Rn					Rd				
UCVTF (vector, fixed-pc	Scalar	0	1	1	1	1	1	1	1	0	!=0000				immb			1	1	1	0	0	1	Rn					Rd				
FCVTZU (vector, fixed-p	Scalar	0	1	1	1	1	1	1	1	0	!=0000				immb			1	1	1	1	1	1	Rn					Rd				
Crypto three-reg SHA		**0**	**1**	**0**	**1**	**1**	**1**	**1**	**0**	**size**		**0**			**Rm**			**0**	**opcode**			**0**	**0**	**Rn**					**Rd**				
SHA1C	-	0	1	0	1	1	1	1	0	0	0	0			Rm			0	0	0	0	0	0	Rn					Rd				
SHA1P	-	0	1	0	1	1	1	1	0	0	0	0			Rm			0	0	0	1	0	0	Rn					Rd				
SHA1M	-	0	1	0	1	1	1	1	0	0	0	0			Rm			0	0	1	0	0	0	Rn					Rd				
SHA1SU0	-	0	1	0	1	1	1	1	0	0	0	0			Rm			0	0	1	1	0	0	Rn					Rd				
SHA256H	-	0	1	0	1	1	1	1	0	0	0	0			Rm			0	1	0	0	0	0	Rn					Rd				
SHA256H2	-	0	1	0	1	1	1	1	0	0	0	0			Rm			0	1	0	1	0	0	Rn					Rd				
SHA256SU1	-	0	1	0	1	1	1	1	0	0	0	0			Rm			0	1	1	0	0	0	Rn					Rd				
Crypto two-reg SHA		**0**	**1**	**0**	**1**	**1**	**1**	**1**	**0**	**size**		**1**	**0**	**1**	**0**	**0**	**opcode**					**1**	**0**	**Rn**					**Rd**				
SHA1H	-	0	1	0	1	1	1	1	0	0	0	1	0	1	0	0	0	0	0	0	0	1	0	Rn					Rd				
SHA1SU1	-	0	1	0	1	1	1	1	0	0	0	1	0	1	0	0	0	0	0	0	1	1	0	Rn					Rd				
SHA256SU0	-	0	1	0	1	1	1	1	0	0	0	1	0	1	0	0	0	0	0	1	0	1	0	Rn					Rd				
Crypto AES		**0**	**1**	**0**	**0**	**1**	**1**	**1**	**0**	**size**		**1**	**0**	**1**	**0**	**0**	**opcode**					**1**	**0**	**Rn**					**Rd**				
AESE	-	0	1	0	0	1	1	1	0	0	0	1	0	1	0	0	0	0	1	0	0	1	0	Rn					Rd				
AESD	-	0	1	0	0	1	1	1	0	0	0	1	0	1	0	0	0	0	1	0	1	1	0	Rn					Rd				
AESMC	-	0	1	0	0	1	1	1	0	0	0	1	0	1	0	0	0	0	1	1	0	1	0	Rn					Rd				
AESIMC	-	0	1	0	0	1	1	1	0	0	0	1	0	1	0	0	0	0	1	1	1	1	0	Rn					Rd				
AdvSIMD three same		**0**	**Q**	**U**	**0**	**1**	**1**	**1**	**0**	**size**		**1**			**Rm**			**opcode**				**1**		**Rn**					**Rd**				
SHADD	-	0	Q	0	0	1	1	1	0	-	-	1			Rm			0	0	0	0	0	1	Rn					Rd				
SQADD	Vector	0	Q	0	0	1	1	1	0	-	-	1			Rm			0	0	0	0	1	1	Rn					Rd				
SRHADD	-	0	Q	0	0	1	1	1	0	-	-	1			Rm			0	0	0	1	0	1	Rn					Rd				
SHSUB	-	0	Q	0	0	1	1	1	0	-	-	1			Rm			0	0	1	0	0	1	Rn					Rd				
SQSUB	Vector	0	Q	0	0	1	1	1	0	-	-	1			Rm			0	0	1	0	1	1	Rn					Rd				
CMGT (register)	Vector	0	Q	0	0	1	1	1	0	-	-	1			Rm			0	0	1	1	0	1	Rn					Rd				

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CMGE (register)	Vector	0	Q	0	0	1	1	1	0	-	-	1	Rm	0	0	1	1	1	1	Rn	Rd
SSHL Vector		0	Q	0	0	1	1	1	0	-	-	1	Rm	0	1	0	0	0	1	Rn	Rd
SQSHL (register)	Vector	0	Q	0	0	1	1	1	0	-	-	1	Rm	0	1	0	0	1	1	Rn	Rd
SRSHL	Vector	0	Q	0	0	1	1	1	0	-	-	1	Rm	0	1	0	1	0	1	Rn	Rd
SQRSHL	Vector	0	Q	0	0	1	1	1	0	-	-	1	Rm	0	1	0	1	1	1	Rn	Rd
SMAX	-	0	Q	0	0	1	1	1	0	-	-	1	Rm	0	1	1	0	0	1	Rn	Rd
SMIN	-	0	Q	0	0	1	1	1	0	-	-	1	Rm	0	1	1	0	1	1	Rn	Rd
SABD	-	0	Q	0	0	1	1	1	0	-	-	1	Rm	0	1	1	1	0	1	Rn	Rd
SABA	-	0	Q	0	0	1	1	1	0	-	-	1	Rm	0	1	1	1	1	1	Rn	Rd
ADD (vector)	Vector	0	Q	0	0	1	1	1	0	-	-	1	Rm	1	0	0	0	0	1	Rn	Rd
CMTST	Vector	0	Q	0	0	1	1	1	0	-	-	1	Rm	1	0	0	0	1	1	Rn	Rd
MLA (vector)	-	0	Q	0	0	1	1	1	0	-	-	1	Rm	1	0	0	1	0	1	Rn	Rd
MUL (vector)	-	0	Q	0	0	1	1	1	0	-	-	1	Rm	1	0	0	1	1	1	Rn	Rd
SMAXP	-	0	Q	0	0	1	1	1	0	-	-	1	Rm	1	0	1	0	0	1	Rn	Rd
SMINP	-	0	Q	0	0	1	1	1	0	-	-	1	Rm	1	0	1	0	1	1	Rn	Rd
SQDMULH (vector)	Vector	0	Q	0	0	1	1	1	0	-	-	1	Rm	1	0	1	1	0	1	Rn	Rd
ADDP (vector)	-	0	Q	0	0	1	1	1	0	-	-	1	Rm	1	0	1	1	1	1	Rn	Rd
FMAXNM (vector)	-	0	Q	0	0	1	1	1	0	0	x	1	Rm	1	1	0	0	0	1	Rn	Rd
FMLA (vector)	-	0	Q	0	0	1	1	1	0	0	x	1	Rm	1	1	0	0	1	1	Rn	Rd
FADD (vector)	-	0	Q	0	0	1	1	1	0	0	x	1	Rm	1	1	0	1	0	1	Rn	Rd
FMULX	Vector	0	Q	0	0	1	1	1	0	0	x	1	Rm	1	1	0	1	1	1	Rn	Rd
FCMEQ (register)	Vector	0	Q	0	0	1	1	1	0	0	x	1	Rm	1	1	1	0	0	1	Rn	Rd
FMAX (vector)	-	0	Q	0	0	1	1	1	0	0	x	1	Rm	1	1	1	1	0	1	Rn	Rd
FRECPS	Vector	0	Q	0	0	1	1	1	0	0	x	1	Rm	1	1	1	1	1	1	Rn	Rd
AND (vector)	-	0	Q	0	0	1	1	1	0	0	0	1	Rm	0	0	0	1	1	1	Rn	Rd
BIC (vector,	register)	0	Q	0	0	1	1	1	0	0	1	1	Rm	0	0	0	1	1	1	Rn	Rd
FMINNM (vector)	-	0	Q	0	0	1	1	1	0	1	x	1	Rm	1	1	0	0	0	1	Rn	Rd
FMLS (vector)	-	0	Q	0	0	1	1	1	0	1	x	1	Rm	1	1	0	0	1	1	Rn	Rd
FSUB (vector)	-	0	Q	0	0	1	1	1	0	1	x	1	Rm	1	1	0	1	0	1	Rn	Rd
FMIN (vector)	-	0	Q	0	0	1	1	1	0	1	x	1	Rm	1	1	1	1	0	1	Rn	Rd
FRSQRTS	Vector	0	Q	0	0	1	1	1	0	1	x	1	Rm	1	1	1	1	1	1	Rn	Rd
ORR (vector,	register)	0	Q	0	0	1	1	1	0	1	0	1	Rm	0	0	0	1	1	1	Rn	Rd
ORN (vector)	-	0	Q	0	0	1	1	1	0	1	1	1	Rm	0	0	0	1	1	1	Rn	Rd
UHADD	-	0	Q	1	0	1	1	1	0	-	-	1	Rm	0	0	0	0	0	1	Rn	Rd
UQADD	Vector	0	Q	1	0	1	1	1	0	-	-	1	Rm	0	0	0	0	1	1	Rn	Rd
URHADD	-	0	Q	1	0	1	1	1	0	-	-	1	Rm	0	0	0	1	0	1	Rn	Rd
UHSUB	-	0	Q	1	0	1	1	1	0	-	-	1	Rm	0	0	1	0	0	1	Rn	Rd
UQSUB	Vector	0	Q	1	0	1	1	1	0	-	-	1	Rm	0	0	1	0	1	1	Rn	Rd
CMHI (register)	Vector	0	Q	1	0	1	1	1	0	-	-	1	Rm	0	0	1	1	0	1	Rn	Rd
CMHS (register)	Vector	0	Q	1	0	1	1	1	0	-	-	1	Rm	0	0	1	1	1	1	Rn	Rd
USHL	Vector	0	Q	1	0	1	1	1	0	-	-	1	Rm	0	1	0	0	0	1	Rn	Rd
UQSHL (register)	Vector	0	Q	1	0	1	1	1	0	-	-	1	Rm	0	1	0	0	1	1	Rn	Rd
URSHL	Vector	0	Q	1	0	1	1	1	0	-	-	1	Rm	0	1	0	1	0	1	Rn	Rd

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UQRSHL	Vector	0	Q	1	0	1	1	1	0	-	-	1	Rm	0	1	0	1	1	1	Rn	Rd
UMAX	-	0	Q	1	0	1	1	1	0	-	-	1	Rm	0	1	1	0	0	1	Rn	Rd
UMIN	-	0	Q	1	0	1	1	1	0	-	-	1	Rm	0	1	1	0	1	1	Rn	Rd
UABD	-	0	Q	1	0	1	1	1	0	-	-	1	Rm	0	1	1	1	0	1	Rn	Rd
UABA	-	0	Q	1	0	1	1	1	0	-	-	1	Rm	0	1	1	1	1	1	Rn	Rd
SUB (vector)	Vector	0	Q	1	0	1	1	1	0	-	-	1	Rm	1	0	0	0	0	1	Rn	Rd
CMEQ (register)	Vector	0	Q	1	0	1	1	1	0	-	-	1	Rm	1	0	0	0	1	1	Rn	Rd
MLS (vector)	-	0	Q	1	0	1	1	1	0	-	-	1	Rm	1	0	0	1	0	1	Rn	Rd
PMUL	-	0	Q	1	0	1	1	1	0	-	-	1	Rm	1	0	0	1	1	1	Rn	Rd
UMAXP	-	0	Q	1	0	1	1	1	0	-	-	1	Rm	1	0	1	0	0	1	Rn	Rd
UMINP	-	0	Q	1	0	1	1	1	0	-	-	1	Rm	1	0	1	0	1	1	Rn	Rd
SQRDMULH (vector)	Vector	0	Q	1	0	1	1	1	0	-	-	1	Rm	1	0	1	1	0	1	Rn	Rd
FMAXNMP (vector)	-	0	Q	1	0	1	1	1	0	0	x	1	Rm	1	0	1	1	0	1	Rn	Rd
FADDP (vector)	-	0	Q	1	0	1	1	1	0	0	x	1	Rm	1	1	0	1	0	1	Rn	Rd
FMUL (vector)	-	0	Q	1	0	1	1	1	0	0	x	1	Rm	1	1	0	1	1	1	Rn	Rd
FCMGE (register)	Vector	0	Q	1	0	1	1	1	0	0	x	1	Rm	1	1	1	0	0	1	Rn	Rd
FACGE	Vector	0	Q	1	0	1	1	1	0	0	x	1	Rm	1	1	1	0	1	1	Rn	Rd
FMAXP (vector)	-	0	Q	1	0	1	1	1	0	0	x	1	Rm	1	1	1	1	0	1	Rn	Rd
FDIV (vector)	-	0	Q	1	0	1	1	1	0	0	x	1	Rm	1	1	1	1	1	1	Rn	Rd
EOR (vector)	-	0	Q	1	0	1	1	1	0	0	0	1	Rm	0	0	0	1	1	1	Rn	Rd
BSL	-	0	Q	1	0	1	1	1	0	0	1	1	Rm	0	0	0	1	1	1	Rn	Rd
FMINNMP (vector)	-	0	Q	1	0	1	1	1	0	1	x	1	Rm	1	1	0	0	0	1	Rn	Rd
FABD	Vector	0	Q	1	0	1	1	1	0	1	x	1	Rm	1	1	0	1	0	1	Rn	Rd
FCMGT (register)	Vector	0	Q	1	0	1	1	1	0	1	x	1	Rm	1	1	1	0	0	1	Rn	Rd
FACGT	Vector	0	Q	1	0	1	1	1	0	1	x	1	Rm	1	1	1	0	1	1	Rn	Rd
FMINP (vector)	-	0	Q	1	0	1	1	1	0	1	x	1	Rm	1	1	1	1	0	1	Rn	Rd
BIT	-	0	Q	1	0	1	1	1	0	1	0	1	Rm	0	0	0	1	1	1	Rn	Rd
BIF	-	0	Q	1	0	1	1	1	0	1	1	1	Rm	0	0	0	1	1	1	Rn	Rd
AdvSIMD three different		**0**	**Q**	**U**	**0**	**1**	**1**	**1**	**0**	**size**		**1**	**Rm**	**opcode**				**0**	**0**	**Rn**	**Rd**
SADDL, SADDL2	-	0	Q	0	0	1	1	1	0	size		1	Rm	0	0	0	0	0	0	Rn	Rd
SADDW, SADDW2	-	0	Q	0	0	1	1	1	0	size		1	Rm	0	0	0	1	0	0	Rn	Rd
SSUBL, SSUBL2	-	0	Q	0	0	1	1	1	0	size		1	Rm	0	0	1	0	0	0	Rn	Rd
SSUBW, SSUBW2	-	0	Q	0	0	1	1	1	0	size		1	Rm	0	0	1	1	0	0	Rn	Rd
ADDHN, ADDHN2	-	0	Q	0	0	1	1	1	0	size		1	Rm	0	1	0	0	0	0	Rn	Rd
SABAL, SABAL2	-	0	Q	0	0	1	1	1	0	size		1	Rm	0	1	0	1	0	0	Rn	Rd
SUBHN, SUBHN2	-	0	Q	0	0	1	1	1	0	size		1	Rm	0	1	1	0	0	0	Rn	Rd
SABDL, SABDL2	-	0	Q	0	0	1	1	1	0	size		1	Rm	0	1	1	1	0	0	Rn	Rd
SMLAL, SMLAL2 (vectc	-	0	Q	0	0	1	1	1	0	size		1	Rm	1	0	0	0	0	0	Rn	Rd
SQDMLAL, SQDMLAL2	Vector	0	Q	0	0	1	1	1	0	size		1	Rm	1	0	0	1	0	0	Rn	Rd
SMLSL, SMLSL2 (vectc	-	0	Q	0	0	1	1	1	0	size		1	Rm	1	0	1	0	0	0	Rn	Rd
SQDMLSL, SQDMLSL2	Vector	0	Q	0	0	1	1	1	0	size		1	Rm	1	0	1	1	0	0	Rn	Rd
SMULL, SMULL2 (vectc	-	0	Q	0	0	1	1	1	0	size		1	Rm	1	1	0	0	0	0	Rn	Rd
SQDMULL, SQDMULL2	Vector	0	Q	0	0	1	1	1	0	size		1	Rm	1	1	0	1	0	0	Rn	Rd

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PMULL, PMULL2	-	0	Q	0	0	1	1	1	0	size		1			Rm			1	1	1	0	0	0			Rn					Rd		
UADDL, UADDL2	-	0	Q	1	0	1	1	1	0	size		1			Rm			0	0	0	0	0	0			Rn					Rd		
UADDW, UADDW2	-	0	Q	1	0	1	1	1	0	size		1			Rm			0	0	0	1	0	0			Rn					Rd		
USUBL, USUBL2	-	0	Q	1	0	1	1	1	0	size		1			Rm			0	0	1	0	0	0			Rn					Rd		
USUBW, USUBW2	-	0	Q	1	0	1	1	1	0	size		1			Rm			0	0	1	1	0	0			Rn					Rd		
RADDHN, RADDHN2	-	0	Q	1	0	1	1	1	0	size		1			Rm			0	1	0	0	0	0			Rn					Rd		
UABAL, UABAL2	-	0	Q	1	0	1	1	1	0	size		1			Rm			0	1	0	1	0	0			Rn					Rd		
RSUBHN, RSUBHN2	-	0	Q	1	0	1	1	1	0	size		1			Rm			0	1	1	0	0	0			Rn					Rd		
UABDL, UABDL2	-	0	Q	1	0	1	1	1	0	size		1			Rm			0	1	1	1	0	0			Rn					Rd		
UMLAL, UMLAL2 (vect	-	0	Q	1	0	1	1	1	0	size		1			Rm			1	0	0	0	0	0			Rn					Rd		
UMLSL, UMLSL2 (vect	-	0	Q	1	0	1	1	1	0	size		1			Rm			1	0	1	0	0	0			Rn					Rd		
UMULL, UMULL2 (vect	-	0	Q	1	0	1	1	1	0	size		1			Rm			1	1	0	0	0	0			Rn					Rd		
AdvSIMD two-reg misc		**0**	**Q**	**U**	**0**	**1**	**1**	**1**	**0**	**size**		**1**	**0**	**0**	**0**	**0**	**opcode**					**1**	**0**			**Rn**					**Rd**		
REV64	-	0	Q	0	0	1	1	1	0	-	-	1	0	0	0	0	0	0	0	0	0	1	0			Rn					Rd		
REV16 (vector)	-	0	Q	0	0	1	1	1	0	-	-	1	0	0	0	0	0	0	0	0	1	1	0			Rn					Rd		
SADDLP	-	0	Q	0	0	1	1	1	0	-	-	1	0	0	0	0	0	0	0	1	0	1	0			Rn					Rd		
SUQADD	Vector	0	Q	0	0	1	1	1	0	-	-	1	0	0	0	0	0	0	0	1	1	1	0			Rn					Rd		
CLS (vector)	-	0	Q	0	0	1	1	1	0	-	-	1	0	0	0	0	0	0	1	0	0	1	0			Rn					Rd		
CNT	-	0	Q	0	0	1	1	1	0	-	-	1	0	0	0	0	0	0	1	0	1	1	0			Rn					Rd		
SADALP	-	0	Q	0	0	1	1	1	0	-	-	1	0	0	0	0	0	0	1	1	0	1	0			Rn					Rd		
SQABS	Vector	0	Q	0	0	1	1	1	0	-	-	1	0	0	0	0	0	0	1	1	1	1	0			Rn					Rd		
CMGT (zero)	Vector	0	Q	0	0	1	1	1	0	-	-	1	0	0	0	0	0	1	0	0	0	1	0			Rn					Rd		
CMEQ (zero)	Vector	0	Q	0	0	1	1	1	0	-	-	1	0	0	0	0	0	1	0	0	1	1	0			Rn					Rd		
CMLT (zero)	Vector	0	Q	0	0	1	1	1	0	-	-	1	0	0	0	0	0	1	0	1	0	1	0			Rn					Rd		
ABS	Vector	0	Q	0	0	1	1	1	0	-	-	1	0	0	0	0	0	1	0	1	1	1	0			Rn					Rd		
XTN, XTN2	-	0	Q	0	0	1	1	1	0	-	-	1	0	0	0	0	1	0	0	1	0	1	0			Rn					Rd		
SQXTN, SQXTN2	Vector	0	Q	0	0	1	1	1	0	-	-	1	0	0	0	0	1	0	1	0	0	1	0			Rn					Rd		
FCVTN, FCVTN2	-	0	Q	0	0	1	1	1	0	0	x	1	0	0	0	0	1	0	1	1	0	1	0			Rn					Rd		
FCVTL, FCVTL2	-	0	Q	0	0	1	1	1	0	0	x	1	0	0	0	0	1	0	1	1	1	1	0			Rn					Rd		
FRINTN (vector)	-	0	Q	0	0	1	1	1	0	0	x	1	0	0	0	0	1	1	0	0	0	1	0			Rn					Rd		
FRINTM (vector)	-	0	Q	0	0	1	1	1	0	0	x	1	0	0	0	0	1	1	0	0	1	1	0			Rn					Rd		
FCVTNS (vector)	Vector	0	Q	0	0	1	1	1	0	0	x	1	0	0	0	0	1	1	0	1	0	1	0			Rn					Rd		
FCVTMS (vector)	Vector	0	Q	0	0	1	1	1	0	0	x	1	0	0	0	0	1	1	0	1	1	1	0			Rn					Rd		
FCVTAS (vector)	Vector	0	Q	0	0	1	1	1	0	0	x	1	0	0	0	0	1	1	1	0	0	1	0			Rn					Rd		
SCVTF (vector, integer)	Vector	0	Q	0	0	1	1	1	0	0	x	1	0	0	0	0	1	1	1	0	1	1	0			Rn					Rd		
FCMGT (zero)	Vector	0	Q	0	0	1	1	1	0	1	x	1	0	0	0	0	0	1	1	0	0	1	0			Rn					Rd		
FCMEQ (zero)	Vector	0	Q	0	0	1	1	1	0	1	x	1	0	0	0	0	0	1	1	0	1	1	0			Rn					Rd		
FCMLT (zero)	Vector	0	Q	0	0	1	1	1	0	1	x	1	0	0	0	0	0	1	1	1	0	1	0			Rn					Rd		
FABS (vector)	-	0	Q	0	0	1	1	1	0	1	x	1	0	0	0	0	0	1	1	1	1	1	0			Rn					Rd		
FRINTP (vector)	-	0	Q	0	0	1	1	1	0	1	x	1	0	0	0	0	1	1	0	0	0	1	0			Rn					Rd		
FRINTZ (vector)	-	0	Q	0	0	1	1	1	0	1	x	1	0	0	0	0	1	1	0	0	1	1	0			Rn					Rd		
FCVTPS (vector)	Vector	0	Q	0	0	1	1	1	0	1	x	1	0	0	0	0	1	1	0	1	0	1	0			Rn					Rd		
FCVTZS (vector, intege	Vector	0	Q	0	0	1	1	1	0	1	x	1	0	0	0	0	1	1	0	1	1	1	0			Rn					Rd		

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URECPE	-	0	Q	0	0	1	1	1	0	1	x	1	0	0	0	0	1	1	1	0	0	1	0	Rn					Rd				
FRECPE	Vector	0	Q	0	0	1	1	1	0	1	x	1	0	0	0	0	1	1	1	0	1	1	0	Rn					Rd				
REV32 (vector)	-	0	Q	1	0	1	1	1	0	-	-	1	0	0	0	0	0	0	0	0	0	1	0	Rn					Rd				
UADDLP	-	0	Q	1	0	1	1	1	0	-	-	1	0	0	0	0	0	0	0	1	0	1	0	Rn					Rd				
USQADD	Vector	0	Q	1	0	1	1	1	0	-	-	1	0	0	0	0	0	0	0	1	1	1	0	Rn					Rd				
CLZ (vector)	-	0	Q	1	0	1	1	1	0	-	-	1	0	0	0	0	0	0	1	0	0	1	0	Rn					Rd				
UADALP	-	0	Q	1	0	1	1	1	0	-	-	1	0	0	0	0	0	0	1	1	0	1	0	Rn					Rd				
SQNEG	Vector	0	Q	1	0	1	1	1	0	-	-	1	0	0	0	0	0	0	1	1	1	1	0	Rn					Rd				
CMGE (zero)	Vector	0	Q	1	0	1	1	1	0	-	-	1	0	0	0	0	0	1	0	0	0	1	0	Rn					Rd				
CMLE (zero)	Vector	0	Q	1	0	1	1	1	0	-	-	1	0	0	0	0	0	1	0	0	1	1	0	Rn					Rd				
NEG (vector)	Vector	0	Q	1	0	1	1	1	0	-	-	1	0	0	0	0	0	1	0	1	1	1	0	Rn					Rd				
SQXTUN, SQXTUN2	Vector	0	Q	1	0	1	1	1	0	-	-	1	0	0	0	0	1	0	0	1	0	1	0	Rn					Rd				
SHLL, SHLL2	-	0	Q	1	0	1	1	1	0	-	-	1	0	0	0	0	1	0	0	1	1	1	0	Rn					Rd				
UQXTN, UQXTN2	Vector	0	Q	1	0	1	1	1	0	-	-	1	0	0	0	0	1	0	1	0	0	1	0	Rn					Rd				
FCVTXN, FCVTXN2	Vector	0	Q	1	0	1	1	1	0	0	x	1	0	0	0	0	1	0	1	1	0	1	0	Rn					Rd				
FRINTA (vector)	-	0	Q	1	0	1	1	1	0	0	x	1	0	0	0	0	1	1	0	0	0	1	0	Rn					Rd				
FRINTX (vector)	-	0	Q	1	0	1	1	1	0	0	x	1	0	0	0	0	1	1	0	0	1	1	0	Rn					Rd				
FCVTNU (vector)	Vector	0	Q	1	0	1	1	1	0	0	x	1	0	0	0	0	1	1	0	1	0	1	0	Rn					Rd				
FCVTMU (vector)	Vector	0	Q	1	0	1	1	1	0	0	x	1	0	0	0	0	1	1	0	1	1	1	0	Rn					Rd				
FCVTAU (vector)	Vector	0	Q	1	0	1	1	1	0	0	x	1	0	0	0	0	1	1	1	0	0	1	0	Rn					Rd				
UCVTF (vector, integer)	Vector	0	Q	1	0	1	1	1	0	0	x	1	0	0	0	0	1	1	1	0	1	1	0	Rn					Rd				
NOT	-	0	Q	1	0	1	1	1	0	0	0	1	0	0	0	0	0	0	1	0	1	1	0	Rn					Rd				
RBIT (vector)	-	0	Q	1	0	1	1	1	0	0	1	1	0	0	0	0	0	0	1	0	1	1	0	Rn					Rd				
FCMGE (zero)	Vector	0	Q	1	0	1	1	1	0	1	x	1	0	0	0	0	0	1	1	0	0	1	0	Rn					Rd				
FCMLE (zero)	Vector	0	Q	1	0	1	1	1	0	1	x	1	0	0	0	0	0	1	1	0	1	1	0	Rn					Rd				
FNEG (vector)	-	0	Q	1	0	1	1	1	0	1	x	1	0	0	0	0	0	1	1	1	1	1	0	Rn					Rd				
FRINTI (vector)	-	0	Q	1	0	1	1	1	0	1	x	1	0	0	0	0	1	1	0	0	1	1	0	Rn					Rd				
FCVTPU (vector)	Vector	0	Q	1	0	1	1	1	0	1	x	1	0	0	0	0	1	1	0	1	0	1	0	Rn					Rd				
FCVTZU (vector, intege	Vector	0	Q	1	0	1	1	1	0	1	x	1	0	0	0	0	1	1	0	1	1	1	0	Rn					Rd				
URSQRTE	-	0	Q	1	0	1	1	1	0	1	x	1	0	0	0	0	1	1	1	0	0	1	0	Rn					Rd				
FRSQRTE	Vector	0	Q	1	0	1	1	1	0	1	x	1	0	0	0	0	1	1	1	0	1	1	0	Rn					Rd				
FSQRT (vector)	-	0	Q	1	0	1	1	1	0	1	x	1	0	0	0	0	1	1	1	1	1	1	0	Rn					Rd				
AdvSIMD across lanes		**0**	**Q**	**U**	**0**	**1**	**1**	**1**	**0**	**size**		**1**	**1**	**0**	**0**	**0**	**opcode**					**1**	**0**	**Rn**					**Rd**				
SADDLV	-	0	Q	0	0	1	1	1	0	-	-	1	1	0	0	0	0	0	0	1	1	1	0	Rn					Rd				
SMAXV	-	0	Q	0	0	1	1	1	0	-	-	1	1	0	0	0	0	1	0	1	0	1	0	Rn					Rd				
SMINV	-	0	Q	0	0	1	1	1	0	-	-	1	1	0	0	0	1	1	0	1	0	1	0	Rn					Rd				
ADDV	-	0	Q	0	0	1	1	1	0	-	-	1	1	0	0	0	1	1	0	1	1	1	0	Rn					Rd				
UADDLV	-	0	Q	1	0	1	1	1	0	-	-	1	1	0	0	0	0	0	0	1	1	1	0	Rn					Rd				
UMAXV	-	0	Q	1	0	1	1	1	0	-	-	1	1	0	0	0	0	1	0	1	0	1	0	Rn					Rd				
UMINV	-	0	Q	1	0	1	1	1	0	-	-	1	1	0	0	0	1	1	0	1	0	1	0	Rn					Rd				
FMAXNMV	-	0	Q	1	0	1	1	1	0	0	x	1	1	0	0	0	0	1	1	0	0	1	0	Rn					Rd				
FMAXV	-	0	Q	1	0	1	1	1	0	0	x	1	1	0	0	0	0	1	1	1	1	1	0	Rn					Rd				
FMINNMV	-	0	Q	1	0	1	1	1	0	1	x	1	1	0	0	0	0	1	1	0	0	1	0	Rn					Rd				

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FMINV	-	0	Q	1	0	1	1	1	0	1	x	1	1	0	0	0	0	1	1	1	1	1	0	Rn					Rd				
AdvSIMD copy		**0**	**Q**	**op**	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**imm5**					**0**	**imm4**				**1**	**Rn**					**Rd**				
DUP (element)	Vector	0	-	0	0	1	1	1	0	0	0	0	-	-	-	-	-	0	0	0	0	0	1	Rn					Rd				
DUP (general)	-	0	-	0	0	1	1	1	0	0	0	0	-	-	-	-	-	0	0	0	0	1	1	Rn					Rd				
SMOV	32-bit	0	0	0	0	1	1	1	0	0	0	0	-	-	-	-	-	0	0	1	0	1	1	Rn					Rd				
UMOV	32-bit	0	0	0	0	1	1	1	0	0	0	0	-	-	-	-	-	0	0	1	1	1	1	Rn					Rd				
INS (general)	-	0	1	0	0	1	1	1	0	0	0	0	-	-	-	-	-	0	0	0	1	1	1	Rn					Rd				
SMOV	64-bit	0	1	0	0	1	1	1	0	0	0	0	-	-	-	-	-	0	0	1	0	1	1	Rn					Rd				
UMOV	64-bit	0	1	0	0	1	1	1	0	0	0	0	-	-	-	-	-	0	0	1	1	1	1	Rn					Rd				
INS (element)	-	0	1	1	0	1	1	1	0	0	0	0	-	-	-	-	-	0	-	-	-	-	1	Rn					Rd				
AdvSIMD vector x indexed element		**0**	**Q**	**U**	**0**	**1**	**1**	**1**	**1**	**size**		**L**	**M**	**Rm**				**opcode**				**H**	**0**	**Rn**					**Rd**				
SMLAL, SMLAL2 (by el	-	0	Q	0	0	1	1	1	1	-	-	L	M	Rm				0	0	1	0	H	0	Rn					Rd				
SQDMLAL, SQDMLAL2	Vector	0	Q	0	0	1	1	1	1	-	-	L	M	Rm				0	0	1	1	H	0	Rn					Rd				
SMLSL, SMLSL2 (by el	-	0	Q	0	0	1	1	1	1	-	-	L	M	Rm				0	1	1	0	H	0	Rn					Rd				
SQDMLSL, SQDMLSL2	Vector	0	Q	0	0	1	1	1	1	-	-	L	M	Rm				0	1	1	1	H	0	Rn					Rd				
MUL (by element)	-	0	Q	0	0	1	1	1	1	-	-	L	M	Rm				1	0	0	0	H	0	Rn					Rd				
SMULL, SMULL2 (by el	-	0	Q	0	0	1	1	1	1	-	-	L	M	Rm				1	0	1	0	H	0	Rn					Rd				
SQDMULL, SQDMULL2	Vector	0	Q	0	0	1	1	1	1	-	-	L	M	Rm				1	0	1	1	H	0	Rn					Rd				
SQDMULH (by element	Vector	0	Q	0	0	1	1	1	1	-	-	L	M	Rm				1	1	0	0	H	0	Rn					Rd				
SQRDMULH (by eleme	Vector	0	Q	0	0	1	1	1	1	-	-	L	M	Rm				1	1	0	1	H	0	Rn					Rd				
FMLA (by element)	Vector	0	Q	0	0	1	1	1	1	1	x	L	M	Rm				0	0	0	1	H	0	Rn					Rd				
FMLS (by element)	Vector	0	Q	0	0	1	1	1	1	1	x	L	M	Rm				0	1	0	1	H	0	Rn					Rd				
FMUL (by element)	Vector	0	Q	0	0	1	1	1	1	1	x	L	M	Rm				1	0	0	1	H	0	Rn					Rd				
MLA (by element)	-	0	Q	1	0	1	1	1	1	-	-	L	M	Rm				0	0	0	0	H	0	Rn					Rd				
UMLAL, UMLAL2 (by el	-	0	Q	1	0	1	1	1	1	-	-	L	M	Rm				0	0	1	0	H	0	Rn					Rd				
MLS (by element)	-	0	Q	1	0	1	1	1	1	-	-	L	M	Rm				0	1	0	0	H	0	Rn					Rd				
UMLSL, UMLSL2 (by el	-	0	Q	1	0	1	1	1	1	-	-	L	M	Rm				0	1	1	0	H	0	Rn					Rd				
UMULL, UMULL2 (by el	-	0	Q	1	0	1	1	1	1	-	-	L	M	Rm				1	0	1	0	H	0	Rn					Rd				
FMULX (by element)	Vector	0	Q	1	0	1	1	1	1	1	x	L	M	Rm				1	0	0	1	H	0	Rn					Rd				
AdvSIMD modified immediate		**0**	**Q**	**op**	**0**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**a**	**b**	**c**	**cmode**				**o2**	**1**	**d**	**e**	**f**	**g**	**h**	**Rd**				
MOVI	32-bit shifted immediate	0	-	0	0	1	1	1	1	0	0	0	0	0	a	b	c	0	x	x	0	0	1	d	e	f	g	h	Rd				
ORR (vector, immediate	32-bit	0	-	0	0	1	1	1	1	0	0	0	0	0	a	b	c	0	x	x	1	0	1	d	e	f	g	h	Rd				
MOVI	16-bit shifted immediate	0	-	0	0	1	1	1	1	0	0	0	0	0	a	b	c	1	0	x	0	0	1	d	e	f	g	h	Rd				
ORR (vector, immediate	16-bit	0	-	0	0	1	1	1	1	0	0	0	0	0	a	b	c	1	0	x	1	0	1	d	e	f	g	h	Rd				
MOVI	32-bit shifting ones	0	-	0	0	1	1	1	1	0	0	0	0	0	a	b	c	1	1	0	x	0	1	d	e	f	g	h	Rd				
MOVI	8-bit	0	-	0	0	1	1	1	1	0	0	0	0	0	a	b	c	1	1	1	0	0	1	d	e	f	g	h	Rd				
FMOV (vector, immedia	Single-precision	0	-	0	0	1	1	1	1	0	0	0	0	0	a	b	c	1	1	1	1	0	1	d	e	f	g	h	Rd				
MVNI	32-bit shifted immediate	0	-	1	0	1	1	1	1	0	0	0	0	0	a	b	c	0	x	x	0	0	1	d	e	f	g	h	Rd				
BIC (vector, immediate)	32-bit	0	-	1	0	1	1	1	1	0	0	0	0	0	a	b	c	0	x	x	1	0	1	d	e	f	g	h	Rd				
MVNI	16-bit shifted immediate	0	-	1	0	1	1	1	1	0	0	0	0	0	a	b	c	1	0	x	0	0	1	d	e	f	g	h	Rd				
BIC (vector, immediate)	16-bit	0	-	1	0	1	1	1	1	0	0	0	0	0	a	b	c	1	0	x	1	0	1	d	e	f	g	h	Rd				
MVNI	32-bit shifting ones	0	-	1	0	1	1	1	1	0	0	0	0	0	a	b	c	1	1	0	x	0	1	d	e	f	g	h	Rd				
MOVI	64-bit scalar	0	0	1	0	1	1	1	1	0	0	0	0	0	a	b	c	1	1	1	0	0	1	d	e	f	g	h	Rd				

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MOVI	64-bit vector	0	1	1	0	1	1	1	1	0	0	0	0	0	a	b	c	1	1	1	0	0	1	d	e	f	g	h			Rd		
FMOV (vector, immedia	Double-precision	0	1	1	0	1	1	1	1	0	0	0	0	0	a	b	c	1	1	1	1	0	1	d	e	f	g	h			Rd		
AdvSIMD shift by immediate		**0**	**Q**	**U**	**0**	**1**	**1**	**1**	**1**	**0**		**immh**			**immb**			**opcode**					**1**			**Rn**					**Rd**		
SSHR	Vector	0	Q	0	0	1	1	1	1	0		immh			immb			0	0	0	0	0	1			Rn					Rd		
SSRA	Vector	0	Q	0	0	1	1	1	1	0		immh			immb			0	0	0	1	0	1			Rn					Rd		
SRSHR	Vector	0	Q	0	0	1	1	1	1	0		immh			immb			0	0	1	0	0	1			Rn					Rd		
SRSRA	Vector	0	Q	0	0	1	1	1	1	0		immh			immb			0	0	1	1	0	1			Rn					Rd		
SHL	Vector	0	Q	0	0	1	1	1	1	0		immh			immb			0	1	0	1	0	1			Rn					Rd		
SQSHL (immediate)	Vector	0	Q	0	0	1	1	1	1	0		immh			immb			0	1	1	1	0	1			Rn					Rd		
SHRN, SHRN2	-	0	Q	0	0	1	1	1	1	0		immh			immb			1	0	0	0	0	1			Rn					Rd		
RSHRN, RSHRN2	-	0	Q	0	0	1	1	1	1	0		immh			immb			1	0	0	0	1	1			Rn					Rd		
SQSHRN, SQSHRN2	Vector	0	Q	0	0	1	1	1	1	0		immh			immb			1	0	0	1	0	1			Rn					Rd		
SQRSHRN, SQRSHRN	Vector	0	Q	0	0	1	1	1	1	0		immh			immb			1	0	0	1	1	1			Rn					Rd		
SSHLL, SSHLL2	-	0	Q	0	0	1	1	1	1	0		immh			immb			1	0	1	0	0	1			Rn					Rd		
SCVTF (vector, fixed-pc	Vector	0	Q	0	0	1	1	1	1	0		immh			immb			1	1	1	0	0	1			Rn					Rd		
FCVTZS (vector, fixed-p	Vector	0	Q	0	0	1	1	1	1	0		immh			immb			1	1	1	1	1	1			Rn					Rd		
USHR	Vector	0	Q	1	0	1	1	1	1	0		immh			immb			0	0	0	0	0	1			Rn					Rd		
USRA	Vector	0	Q	1	0	1	1	1	1	0		immh			immb			0	0	0	1	0	1			Rn					Rd		
URSHR	Vector	0	Q	1	0	1	1	1	1	0		immh			immb			0	0	1	0	0	1			Rn					Rd		
URSRA	Vector	0	Q	1	0	1	1	1	1	0		immh			immb			0	0	1	1	0	1			Rn					Rd		
SRI	Vector	0	Q	1	0	1	1	1	1	0		immh			immb			0	1	0	0	0	1			Rn					Rd		
SLI	Vector	0	Q	1	0	1	1	1	1	0		immh			immb			0	1	0	1	0	1			Rn					Rd		
SQSHLU	Vector	0	Q	1	0	1	1	1	1	0		immh			immb			0	1	1	0	0	1			Rn					Rd		
UQSHL (immediate)	Vector	0	Q	1	0	1	1	1	1	0		immh			immb			0	1	1	1	0	1			Rn					Rd		
SQSHRUN, SQSHRUN	Vector	0	Q	1	0	1	1	1	1	0		immh			immb			1	0	0	0	0	1			Rn					Rd		
SQRSHRUN, SQRSHR	Vector	0	Q	1	0	1	1	1	1	0		immh			immb			1	0	0	0	1	1			Rn					Rd		
UQSHRN	Vector	0	Q	1	0	1	1	1	1	0		immh			immb			1	0	0	1	0	1			Rn					Rd		
UQRSHRN, UQRSHRN	Vector	0	Q	1	0	1	1	1	1	0		immh			immb			1	0	0	1	1	1			Rn					Rd		
USHLL, USHLL2	-	0	Q	1	0	1	1	1	1	0		immh			immb			1	0	1	0	0	1			Rn					Rd		
UCVTF (vector, fixed-pc	Vector	0	Q	1	0	1	1	1	1	0		immh			immb			1	1	1	0	0	1			Rn					Rd		
FCVTZU (vector, fixed-p	Vector	0	Q	1	0	1	1	1	1	0		immh			immb			1	1	1	1	1	1			Rn					Rd		
AdvSIMD TBL/TBX		**0**	**Q**	**0**	**0**	**1**	**1**	**1**	**0**	**op2**		**0**			**Rm**			**0**	**len**		**op**	**0**	**0**			**Rn**					**Rd**		
TBL	Single register table	0	Q	0	0	1	1	1	0	0	0	0			Rm			0	0	0	0	0	0			Rn					Rd		
TBX	Single register table	0	Q	0	0	1	1	1	0	0	0	0			Rm			0	0	0	1	0	0			Rn					Rd		
TBL	Two register table	0	Q	0	0	1	1	1	0	0	0	0			Rm			0	0	1	0	0	0			Rn					Rd		
TBX	Two register table	0	Q	0	0	1	1	1	0	0	0	0			Rm			0	0	1	1	0	0			Rn					Rd		
TBL	Three register table	0	Q	0	0	1	1	1	0	0	0	0			Rm			0	1	0	0	0	0			Rn					Rd		
TBX	Three register table	0	Q	0	0	1	1	1	0	0	0	0			Rm			0	1	0	1	0	0			Rn					Rd		
TBL	Four register table	0	Q	0	0	1	1	1	0	0	0	0			Rm			0	1	1	0	0	0			Rn					Rd		
TBX	Four register table	0	Q	0	0	1	1	1	0	0	0	0			Rm			0	1	1	1	0	0			Rn					Rd		
AdvSIMD ZIP/UZP/TRN		**0**	**Q**	**0**	**0**	**1**	**1**	**1**	**0**	**size**		**0**			**Rm**			**0**	**opcode**			**1**	**0**			**Rn**					**Rd**		
UZP1	-	0	Q	0	0	1	1	1	0	size		0			Rm			0	0	0	1	1	0			Rn					Rd		
TRN1	-	0	Q	0	0	1	1	1	0	size		0			Rm			0	0	1	0	1	0			Rn					Rd		

instruction page	variant	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ZIP1	-	0	Q	0	0	1	1	1	0	size		0	Rm					0	0	1	1	1	0	Rn					Rd				
UZP2	-	0	Q	0	0	1	1	1	0	size		0	Rm					0	1	0	1	1	0	Rn					Rd				
TRN2	-	0	Q	0	0	1	1	1	0	size		0	Rm					0	1	1	0	1	0	Rn					Rd				
ZIP2	-	0	Q	0	0	1	1	1	0	size		0	Rm					0	1	1	1	1	0	Rn					Rd				
AdvSIMD EXT		**0**	**Q**	**1**	**0**	**1**	**1**	**1**	**0**	**op2**		**0**	**Rm**					**0**		**imm4**			**0**	**Rn**					**Rd**				
EXT	-	0	Q	1	0	1	1	1	0	0	0	0	Rm					0		imm4			0	Rn					Rd				