Practical Approach Yields Class-C PA

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Practical Approach
Yields Class C PA

A straightforward method of developing input and output matching networks can simplify the design of a practical Class C power amplifier for communications applications from 225 to 400 MHz.

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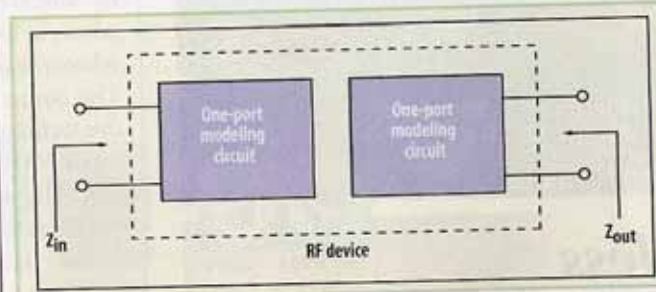
Broadband Class C power amplifiers (PAs) are useful in certain communications bands. Although now integrated into the Advanced Design System (ADS) simulation software from Agilent-EEsof (www.agilent.com), the Touchstone simulation software at one time was a powerful tool for developing and optimizing impedance matching networks for such amplifiers. What follows is a design approach to show how to extract the optimum input and output large-signal impedances for a selected RF transistor, model their behavior with one-port networks, and then develop matching networks over the desired frequency band for operation at the 50-ohm system impedance. To confirm the effectiveness of the approach, a 10-W amplifier was designed and built for 10-dB power gain from 225 to 400 MHz.

Designing wideband microwave PAs is challenging. RF power device parameters change with signal level as well as with frequency, making optimum impedance matching diffi-cult. There is a broad range of techniques used to represent the behavior of the power device. The more complete the representation, the more complicated the model usually becomes.

The large-signal charge-control transistor model[1,2] and the modified Ebers-Moll model[3] were used earlier for modeling RF power transistors. Large-signal S-parameters were also employed with an approximate PA design.[4] However, because of the difficulty in measuring these large-signal S-parameters, the technique was of limited use. Computer simulations were also used to predict the operation of Class C power amplifiers through numerical analysis.[5,6] Although this method can give accurate results, the design of Class C amplifiers using this approach is tedious. Fortunately, the development of harmonic-balance design approaches in the mid-1970s greatly simplified the design of nonlinear circuits and large-signal amplifiers.[7] The basic limitation of this technique is its complexity and the large amount of mathematics needed with the professional numerical methods required to resolve the circuit.

Because of the nonlinear nature of an RF power transistor, a full two-port device model is not an optimum choice for designing input and output matching networks. In this article, one-port impedance models have been used to characterize the optimum load and source terminations of the power device. Optimum load and source large signal impedances

1. This simple diagram represents an effective impedance device model.

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are usually specified by RF device data books at several frequencies in the operating band of the RF power transistor.[8] The effective input and output impedances of the RF device can be represented as the complex conjugates of these optimum terminations.

RF power transistor characterization can be performed by measuring the device's optimum load and source impedances with the aid of load-pull tuners over the frequency band of interest.[9] This requires one-port representations to predict the complex conjugate of these impedances from the lower band edge (F_L) to the upper band edge (f_H) as shown in *Fig. 1*. In this case, $Z_{out} = Z^*_{OL}$ and $Z_{in} = Z^*_{ss}$, where Z_{OL} is the optimum load impedance and Z_s is the source impedance. *Figure 2* shows two possible topologies for the modeled impedance networks.[10] All losses were lumped into a single resistor, which terminates an inductive-capacitive (LC) two-port network.

An analytic synthesis procedure can be used to realize the one-port networks that fit the measured impedance data at both band edges. But instead of performing this tedious task, simulation software such as Touchstone (now ADS) can be used to optimize the circuit elements of the modeling networks to predict performance across the full frequency band of interest.

The maximum available gain will roll off at a negative slope of 6 dB/octave with increasing frequency if a transistor is conjugately matched over a broad frequency range. One of the techniques used to compensate the transistor's power gain variation with frequency is by selectively reflecting some of the power at lower frequencies of the band where the power gain is relatively high. The controlled mismatch imposed in this technique will however degrade the input VSWR at lower-band frequencies. The approximate power gain of the RF transistor is given by[11]:

$$G(f) = \left(\frac{f_{max}}{f}\right)^\gamma \quad (1)$$

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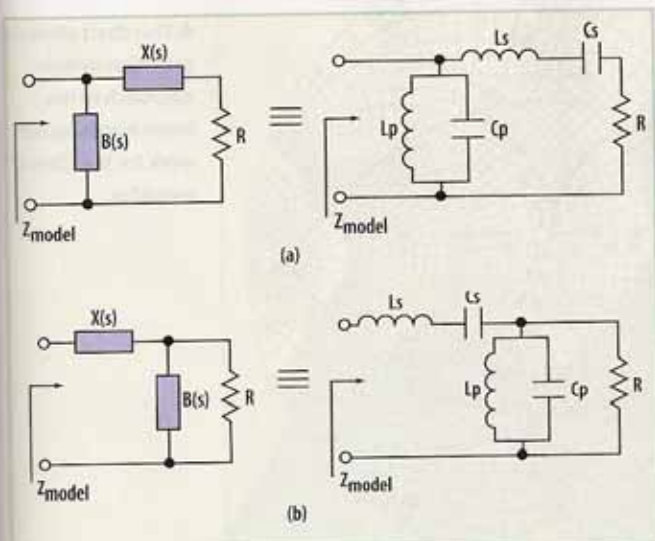
2. The (a) and (b) topologies show two possible modeling networks.

$$G \cdot \alpha = \left(\frac{f_{max}}{f}\right)^{\gamma} \cdot \left(1 - |\Gamma_{in}|^2\right) = G_H = \left(\frac{f_{max}}{f_H}\right)^{\gamma} \quad (B)$$

where:

f_{max} = the maximum frequency of oscillation and

γ = a constant related with the slope of the gain roll-off. γ is given by:

$$\gamma = \frac{|x|}{10\log 2} \cong \frac{|x|}{3} \quad (A)$$

where:

x = the slope in dB/octave.

The transmission loss of the matching network due to the input reflection is:

$$\alpha = 1 - |\Gamma_{in}|^2 \quad (2)$$

where:

Γ_{in} = the reflection coefficient at the input.

To obtain a constant Gα product across the band of interest,

SEE EQ. B IN BOX ABOVE

where:

G_H = the gain at the upper frequency band edge, f_H.

$$|\Gamma_{in}| = \left[1 - \left(\frac{f}{f_H}\right)^r\right]^{1/2} \quad (3)$$

The input-matching network can be designed to model Eq. 3 using Touchstone's optimization capabilities.

The proposed computer design approach for broadband Class C PAs can be summarized by the following systematic procedure:

1. Use the large-signal input and output impedances (Z_{in} and Z^*_{OL}) from the device data sheet over the required frequency band and for the desired output power, gain, and supply voltage.
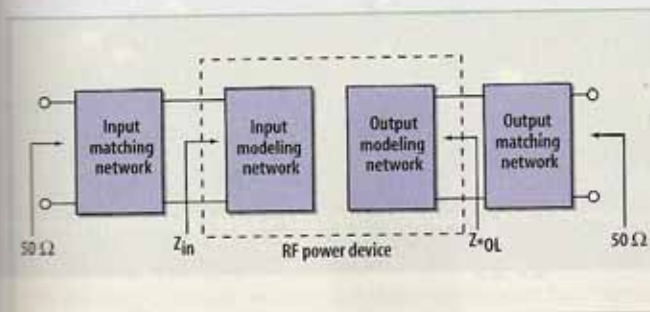

3. The use of modeling software such as Touchstone (now ADS) allows a straightforward approach to the development of impedance matching networks.

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2. Use numerical interpolation and extrapolation techniques to extend the impedance data sample points. This is useful in determining the device terminal impedances at f_L, f_o, and f_H. Store these data in an external data file.

3. Select the appropriate one-port network topologies to model the above terminal impedances over the entire band and optimize their element values with Touchstone.

4. With the modeling circuits just designed, insert the input and output matching networks between the modeling circuits and the source and load 50-ohm terminations, respectively (Fig. 3). The elements of the matching networks can have initial estimates from a rough graphical design procedure.

5. Optimize the input and output matching networks to achieve the desired matching at input and output. The output-matching network is designed to
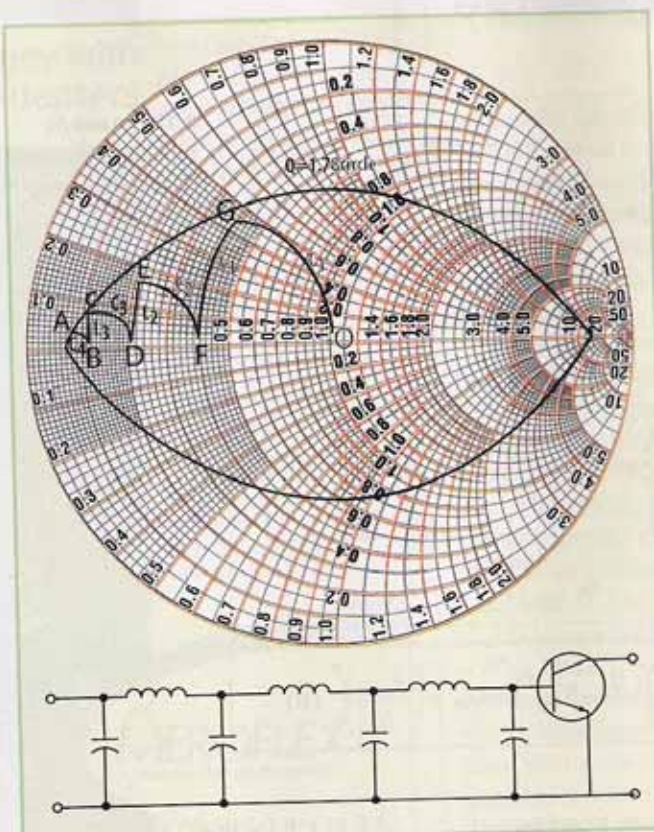
4. This chart shows a graphical design approach to the input matching network for the Class C amplifier.

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achieve conjugate matching and present impedance Z_{OL} to the transistor's output across the entire frequency band. On the other hand, the input-matching network is designed to achieve gain-flatness from f_L to f_H. This can be done by selective mismatching at lower fre-

quencies. The input reflection coefficient is evaluated from Eq. 3 at different sample frequencies and stored at an external data file. The input-matching network is then optimized to model the calculated input reflection coefficient across the entire band.

6. The elements of the matching networks are then tuned, for practical purposes, with Touchstone's tuner window while maintaining the desired frequency response.

To validate the effectiveness of this procedure, a PA circuit was designed and built. The Class C PA was designed for 10 W output power from 225 to 400 MHz with minimum power gain of 10 dB. Class C operation with zero-biased emitter-base junction was adopted since it combines high efficiency and simple construction. A model MRF321 UHF power transistor from Motorola/Free scale was chosen for good reliability and ruggedness. This transistor can deliver 10 W RF power at 400 MHz and operates from a 28-V power supply.

The design of the input and output matching networks begins by taking the large signal input and output impedances (Z_{in} and Z^*_{OL})from device data sheet, and then interpolating these data across the frequency band of interest (which can be done with Touchstone). The *table* presents the interpolated sample values of these impedances across the band from 225 MHz to 400 MHz. *Figure 4* shows the graphical design of the input-matching network. The input impedance at the center frequency (312.5 MHz) is located at point A. The goal is to move from point A to the center of the chart without exceeding the constant Q circle where:

$$Q = \frac{f_o}{f_H - f_L} = 1.78 \ (C)$$

Figure 4 shows that low quality factor (Q) broadband matching circuits can be implemented with multiple L-sections. This matching circuit consists of three lowpass L-type sections and a shunt capacitor (C4) to compensate the inductive reactance of input impedance Z_{in}.

Figure 5 shows the graphical design of the output matching network. However, this network has a bandpass topology consisting of two lowpass sections (L5 – C5 and L6 – C6) and a highpass element (C7). The shunt inductor (L4)

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is used to tune out the output capacitance of the transistor. The gain-bandwidth restrictions of the output matching circuit are simpler than that of the input matching circuit because the output impedance level is higher in this case. The ladder form of this network is useful in harmonic suppression.

The computer modeling procedure begins by designing the modeling networks that predict Z_{in} and Z_{out} from f_L to f_H. These networks are designed and optimized with Touchstone. *Figure 6* shows the final optimized circuit-element values for these networks.

The input matching network was optimized to present the reflection coefficient given by Eq. 3 at the input in order to compensate the −6 dB/octave gain-frequency slope of the MRF321 transistor. The Touchstone circuit file used for optimizing the input matching circuit is available upon request from the author. The values of the required input

| Input and output large-signal impedances for the MRF321		
FREQUENCY (MHz)	Z_{in} (Ω)	Z_{out} (Ω)
225	0.706−j0.413	13.591−j21.134
250	0.732+j0.046	12.992−j20.181
275	0.758+j0.505	12.419−j19.228
300	0.784+j0.965	11.872−j18.277
312.5	0.797+j1.195	11.608−j17.803
325	0.810+j1.424	11.349−j17.328
350	0.837+j1.884	10.849−j16.381
375	0.863+j2.344	10.369−j15.435
400	0.890+j2.805	9.910−j14.492

reflection coefficient were saved as an external file (GMRF321.S1P). Two compensating networks consisting of L7, C8, and R1 and L8, C9, and R2 were added in order to control the input VSWR across the entire band. On the other hand, the output matching network was optimized to present the optimum load impedance, Z_{OL}, to the transistor's collector over the full band of operation. A compensating network was added in series with L4 to improve the matching requirements. *Figure 7* shows the final optimized amplifier circuit.

Proper construction of the amplifier begins by accurately selecting components for the matching networks. All components were measured and tuned using an HP 8510B vector network analyzer from Agilent Technologies (www.agilent.com). Trimmer capacitors were used for tuning purposes, as well as ceramic fixed-value capacitors. All inductors were hand wound using 20 and 22 AWG enameled wires. The RF chokes used for isolating the DC circuit are of low-Q molded type.

The circuit was built on a 10.8 × 8-cm double-sided printed-circuit board (PCB). The PCB material is epoxy-glass with a thickness of 1.2 mm. Epoxy-glass was selected due to its availability and low cost. Circuitry was etched and mounted on the topside, while the copper-clad bottom side served as the ground plane. For good circuit stability, a ferrite bead was added in series with the base choke to prevent low-frequency oscillations. The circuit was then cased in an 11 × 9 × 3-cm box to isolate the amplifier from external spurious signals. This box was mounted on a suitable heat sink. BNC connectors were fastened at input and output for signal feeding. A feedthrough capacitor was mounted on the box body for DC biasing. The RF transistor's stud was tightened with the heat sink using a suitable nut. *Figure 8* shows measured output power as a function of frequency from 225 to 400 MHz.

The power gain is 9.5 ± 1 dB. However no empirical attempt was made to adjust this characteristic. Better broadband operation can be accom-
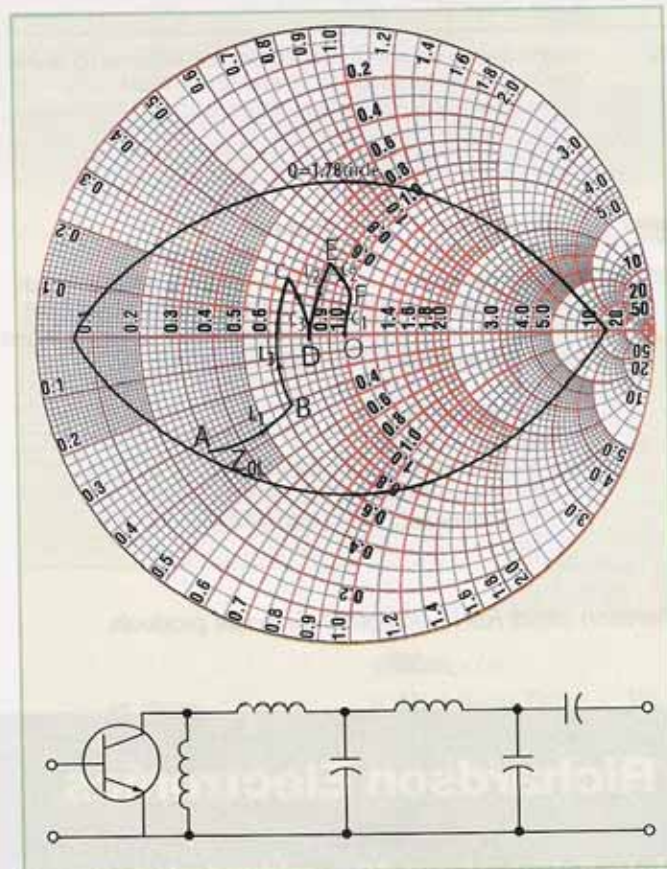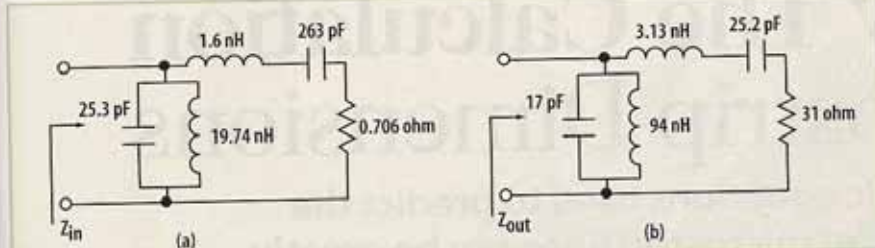
5. This chart shows a graphical design approach to the output matching network for the Class C PA.
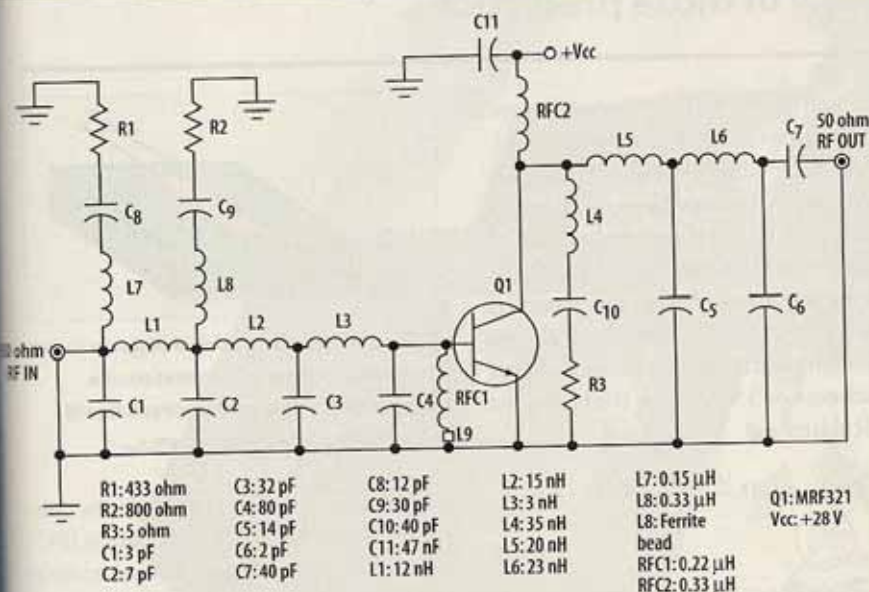
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plished by tuning for equal peaks at the band edges using the trimmer capacitors. If doing this, a three-port circulator should be placed at the amplifier input to protect the driving amplifier from possible reflected power that may result f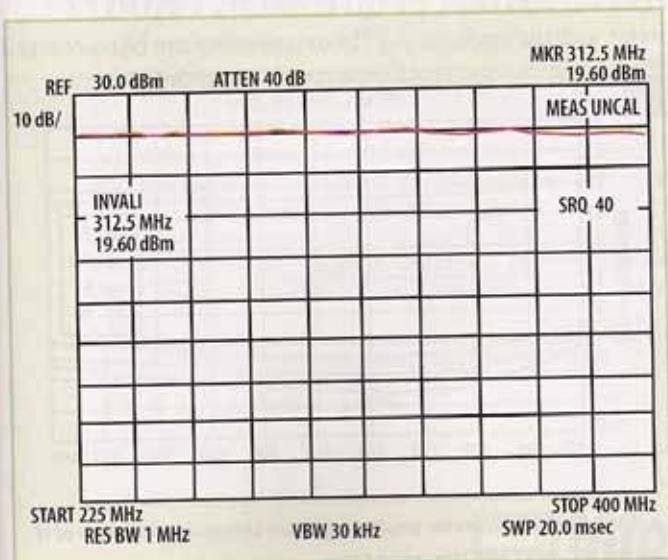rom VSWR degradation through this process. Within the operating band, it was found that the second the harmonic level is between 16 and 20 dB below the fundamental signal power. **MRi**

6. These circuit diagrams represent the optimized input and output modeling networks.

R1: 433 ohm	C3: 32 pF	C8: 12 pF	L2: 15 nH	L7: 0.15 µH	
R2: 800 ohm	C4: 80 pF	C9: 30 pF	L3: 3 nH	L8: 0.33 µH	Q1: MRF321
R3: 5 ohm	C5: 14 pF	C10: 40 pF	L4: 35 nH	L8: Ferrite	Vcc: +28 V
C1: 3 pF	C6: 2 pF	C11: 47 nF	L5: 20 nH	bead	
C2: 7 pF	C7: 40 pF		L6: 23 nH	RFC1: 0.22 µH	
				RFC2: 0.33 µH	

7. This schematic diagram shows the optimized 225-to-400-MHz amplifier circuitry.
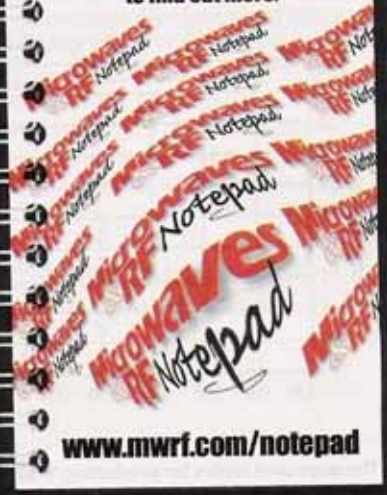

8. The output power of the Class C amplifier was measured as a function of frequency from 225 to 400 MHz.

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