A computerized study of the class-C-biased RF-power amplifier

Vidkjær, Jens

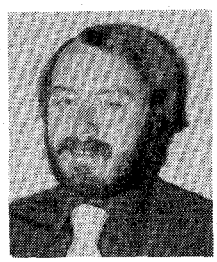
Published in:
I E E E Journal of Solid State Circuits

Link to article, DOI:
10.1109/JSSC.1978.1051027

Publication date:
1978

Document Version
Publisher's PDF, also known as Version of record

[4] G. Kuraishi, "The analysis of class-E RF power amplifier circuits," *Trans. IECE Japan*, vol. B, no. 8 (section J), pp. 597-598, Aug. 1977.
[5] F. H. Raab, "High-efficiency amplification techniques," *IEEE Circuits Syst. Newsletter*, vol. 10, no. 7, pp. 3-11, Dec. 1975.
[6] R. Gutierrez, "Calculate transistor efficiency automatically," *Microwaves*, vol. 14, no. 3, pp. 62, 65, 67, Mar. 1975.
[7] N. O. Sokal and F. H. Raab, "Harmonic output of class *E* RF power amplifiers and load coupling network design," *IEEE J. Solid-State Circuits*, vol. SC-12, no. 1, pp. 86-88, Feb. 1977.
[8] F. H. Raab, "Radio frequency pulsewidth modulation," *IEEE Trans. Commun.*, vol. COM-21, no. 8, pp. 958-966, Aug. 1973.
[9] C. M. Morris, E. R. Parsons, and F. H. Raab, "High efficiency linear SSB power amplifier, final report," Cincinnati Electronics Corporation, Cincinnati, OH, Aug. 1974, 80045 TRC17/874, (available from NTIS, Springfield, VA, as AD A001, 547).
[10] A. D. Sokal and N. O. Sokal, "High efficiency linear power amplification of modulated carrier signals by enevelope elimination and restoration," to be published.
[11] N. O. Sokal, "RF power transistor storage time: Theory and measurements," *IEEE J. Solid-State Circuits*, vol. SC-11, pp. 344-346, Apr. 1976.
[12] F. H. Raab and N. O. Sokal, "Efficiency of the class E tuned power amplifier," in preparation.
[13] N. O. Sokal, "Class E can boost the efficiency of RF power amplifiers," *Electron. Design*, vol. 25, pp. 96-102, Sept. 27, 1977.



Frederick H. Raab (S'66-M'72) was born in Waterloo, IA. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from Iowa State University, Ames, in 1968, 1970, and 1972, respectively.

He then worked for Cincinnati Electronics Corporation for three and a half years in the areas of high-efficiency power amplifiers and search and rescue navigation. He is now with Polhemus Navigation Sciences, Inc., Burlington, VT, and his professional interests include communications, navigation, signal processing, and power amplifiers.

Dr. Raab is a member of the Institute of Navigation, the International Omega Association, Eta Kappa Nu, and Sigma Xi.

A Computerized Study of the Class-*C*-Biased RF-Power Amplifier

JENS VIDKJAER, MEMBER, IEEE

Abstract—**Comparisons between experiments and simulations on a widely used output stage in mobile transmitters are made. It is demonstrated that the operation cycle in this type of circuit differs from the one commonly assumed. The reason is that base widening dominates the feedback effect of the transistor.**

I. Introduction

EVER since RF-power transistors became available, the transistorized transmitter power stage has been a constant challenge to circuit designers and analysts, but still the construction of RF-power amplifiers is often considered as an experimental art rather than a conventional circuit design.

This paper presents a computer simulation of a widely used output stage in mobile transmitters. It is demonstrated that the basic working principles of the circuit differ from the common perception. The new aspect which has led to this conclusion is that high-level transistor effects, especially base widening, have been taken into consideration. The excess charge in the base, when the transistor conducts current, is thereby stored in the base-emitter capacitance instead of the base-collector capacitance as usually assumed. This clearly alters the feedback effects in the transistor and emphasizes the need for a revision of the analytical design tools.

It is a fact, however, that simulations where high-level effects are not taken into consideration may provide reasonably accurate results [1]. Therefore, care will be taken in order to point out the differences between the two situations and demonstrate that if the amplifier has no tendency for instability, the simpler approach will give correct results although it is based on oversimplified assumptions.

Manuscript received July 15, 1977; revised October 5, 1977.

The author is with the Electronics Institute, Technical University of Denmark, Lyngby, Denmark.

II. The Class-*C*-Biased RF-Power Amplifier

The amplifier stage and measurement setup to be considered in this investigation is shown in Fig. 1. The transistor is biased for class *C* operation through the chokes L_b and L_c. The input matching network raises the rather low fundamental frequency transistor input impedance to the impedance level of the generator, and the output matching network provides the collector load which gives maximum output power. The following points apply to the experimental setup.

0018-9200/78/0400-0247$00.75

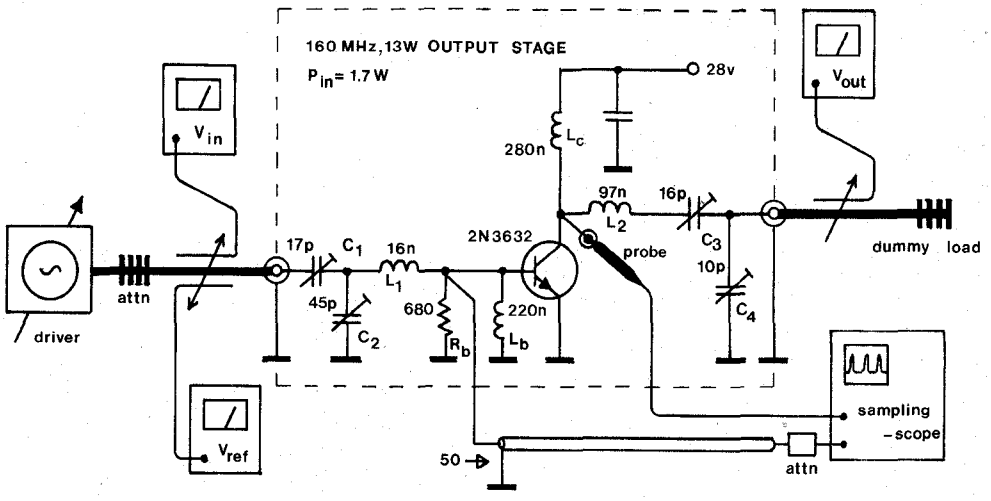


Fig. 1. Experimental RF-power amplifier and measurement setup.

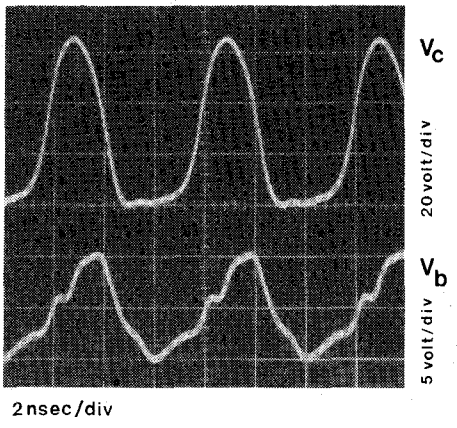


Fig. 2. Experimental collector and base voltage waveforms observed on the amplifier of Fig. 1.

1) The tuning condition is observed through the reflected voltage at the input dual directional coupler and from the load line directional coupler.

2) The oscilloscope is connected directly across the base terminal in order to minimize uncertainties from stray elements. The scope thereby provides the major part of the base damping.

3) The collector probe is mounted in a connector in order to ensure reproducible experiments, although a minor degradation of performance data results.

Fig. 2 shows the experimental collector and base voltage wave shapes when the circuit is operated as specified in the first row of Table I. The performance data which are achieved agree with the transistor data sheets.[1] The equivalent circuit for simulating the experimental setup is given in Fig. 3, and the following circumstances should be mentioned.

[1]The transistor is a Motorola 2N3632 RF-power transistor specified for VHF-UHF application. Typical data for P_{in} = 2 W: P_{out} = 15 W at 100 MHz, P_{out} = 7 W at 300 MHz.

1) The input divider circuit R_1 and R_2 gives a simple method for simulating the input dual directional coupler. Using $E_g = 2V_{in}$, cf. Fig. 1, it is easily proven that the effective values of V_{ref} in both the experimental setup and the equivalent circuit correspond to each other.

2) L_{E1} and L_{B1} represent the emitter and the base lead inductances. The inductance of the collector has been disregarded as a separate component since this does not contribute significantly to the computations, but its value has been added to L_2.

3) A minor part of the base damping has been moved from the external base node to the internal node for computational reasons. As $|Z_{in}|_{160\ MHz} \simeq 3\ \Omega$, no appreciable errors are introduced this way.

4) The collector probe equivalent has been given details sufficient for modeling the probe influence on the amplifier performance. No attempts have been made, however, to model the oscilloscope response accurately.

5) The transistor models will briefly be outlined in subsequent sections. Two levels of modeling have been applied where a) clearly accounts for the traditional perception of the amplifier operation mode.

a) A basic model including no appreciable high-level effects. In a phenomological context, this model corresponds practically to the Gummel model in [2].

b) An extended model which, in addition, includes current saturation in the collector, base widening, and junction breakdown.

The computed wave shapes of some important circuit variables which could be experimentally observed are shown in Fig. 4, where (a) gives the full simulation based on the extended transistor model and (b) gives the steady-state part for the basic model. The corresponding performance data are shown in Table I, and it is seen that only minor differences appear both here and in the wave shapes of the simulations. This raises clearly the question of whether or not the high-level effects are of importance for the amplifier, but it should be recognized that the result is in close agreement with the

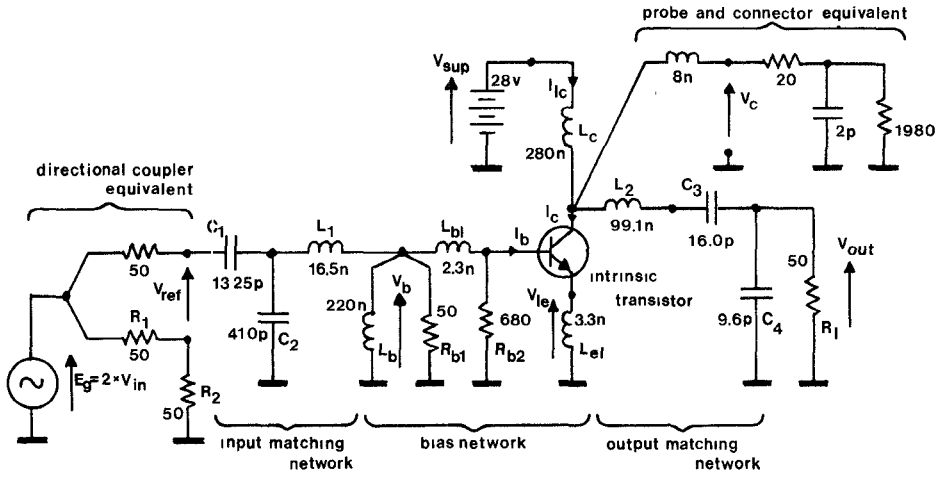


Fig. 3. Equivalent circuit for simulating the amplifier and measurement setup of Fig. 1. The equivalent diagram of the intrinsic transistor is given in Fig. 10.

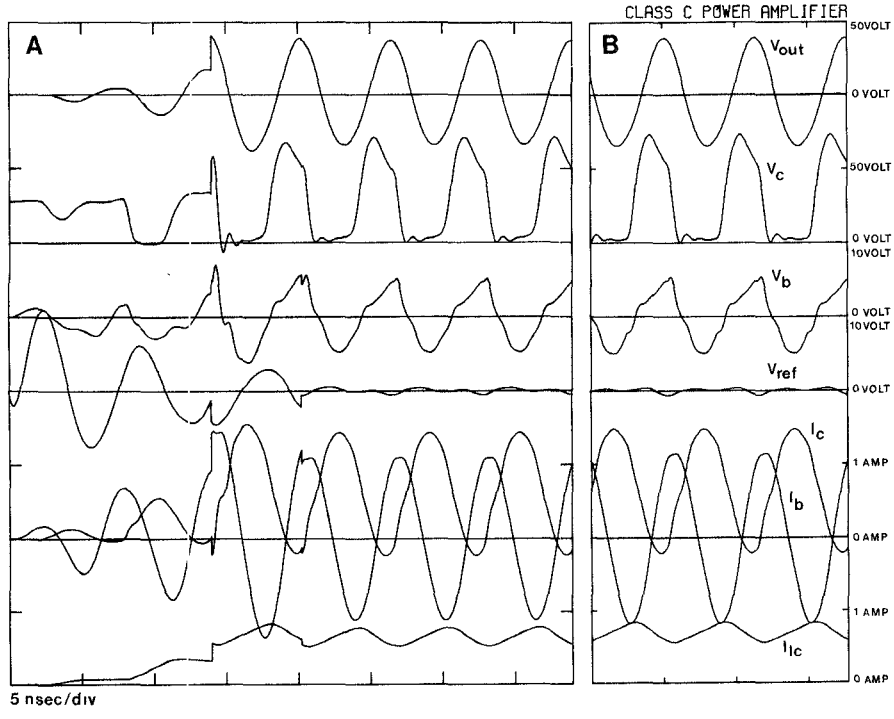


Fig. 4. Simulated responses of the circuit in Fig. 3. (a) The full response where high-level transistor effects are included in the transistor model. The initial steps in the curves are the iteration of the Aprille and Trick steady-state search algorithm. (b) The steady-state part of a similar simulation using a basic transistor model where no appreciable high-level effects are taken into account.

intentions behind the circuit design. The transistor is embodied between two tuned circuits which force the terminal current to be approximately sinusoidal. The purpose of doing so is to make the circuit operation as independent of the nonlinear transistor characteristics as possible. That it works is implicitly observable from the simulations where only few iterations in the Aprille and Trick steady-state search algorithm [3] are required to find a steady-state solution.[2] To demonstrate the influence of the high-level effects, one must,

[2] In a linear circuit, the steady-state algorithm will find the solution after one iteration.

TABLE I
PERFORMANCE DATA FOR THE AMPLIFIERS OF FIGS. 1 AND 3

P_{in} = 1.7 (Watt)	Trimmer Settings[a] (pF) C_1	C_2	C_3	C_4	V_{out} (Volt) 1 harm. eff.	P_{out} (Watt) 1 harm.	I_{lc} (Amp)	Collector Efficiency (Percent)	V_{ref} (Volt) rms
Experiment, Fig. 2	17	45	16.3	9.6	26.2	13.7	0.675	73	0.24
Simulation extended transistor model, Fig. 4(a)	13.3	41	16.0	9.6	25.9	13.4	0.657	73	0.27
Simulation, basic transistor model, Fig. 4(b)	12.8	41	15.0	8.4	26.5	14.0	0.697	72	0.29

[a]The amplifiers are tuned to give maximum output power.

therefore, either go inside the transistor and consider its fundamental operation or impose circuit conditions which will disturb the sinusoidal currents. As the internal transistor behavior is accessible exclusively from simulations, both of these approaches will be taken below in order to make the final conclusions partly on the basis of observations which can be proven experimentally.

Comparing the experimental and simulated results, the following points should finally be mentioned.

1) The differences in input trimmer settings may seem high. Using the computed fundamental frequency transistor input impedance of $(3\ \Omega + j1.5\ \Omega)$, it is easily shown that a measuring error of only 1 nH in the total values of L_1 and L_{B1} may account for the same differences.

2) Discrepancies between experimental and simulated voltage wave shapes lie mainly in their higher harmonics and are supposed to originate mostly from the oscilloscope response (bandwidth $\simeq$ 800 MHz, rise time $\simeq$ 0.4 ns).

III. SUMMARY OF HIGH-LEVEL EFFECTS AND TRANSISTOR MODELS

A brief and unified summary of those high-level effects in the RF-power transistor which have proven to be of importance for the amplifier performance will be given below. The main emphasis is given to the circuit consequence, and the reader is referred to the literature for a detailed discussion of the basic physical mechanisms and their modeling.

A. Current Saturation

The electron velocity v_e in silicon will depart from the common ohmic expression $v_e = \mu_0 E$ at high electrical field strengths and tends to saturate at the scattering limited velocity v_{lim}. Among the different approximations which have been suggested for this field-to-velocity relationship, the following expression posesses both reasonable accuracy and analytical simplicity [4]:

$$v_e(|E|) = v_{lim}\ [1 - \exp(-|E|\mu_0/v_{lim})]. \quad (1)$$

Considering the collector as an isolated sample of silicon with length W_{cc}, doping N_D, and cross-sectional area A, the voltage across this sample may now be written

$$V_{cc} = V_{cc}(I_C) = I_{lim} R_0 \ln [I_{lim}/(I_{lim} - I_C)] \quad (2)$$

where

$V_{cc} = W_{cc}E$ voltage across the unmodulated collector

$R_0 = W_{cc}/qAN_D\mu_0$ resistance of the unmodulated collector

$I_{lim} = \pm qN_D A v_{lim}$ collector scattering limited current, sign (I_{lim}) = sign (I_C).

The nonlinear current-voltage relationship in (2) will clearly give a higher power dissipation in the collector than a simple ohmic model. Inclusion of current saturation should therefore result in a more accurate collector loss simulation than a series resistance in the collector lead may account for. The most important consequence of (2) is, however, that current saturation also provides the foundation for base-widening modeling as considered next.

B. Base Widening

If the current-controlled voltage across the collector series resistance (2) equals or exceeds in magnitude the internal base-collector voltage $V_{BC} - \Phi_C$, the transistor will not become saturated in the usual manner if the transistor has a long, low-doped collector. Φ_C (>0) denotes the built-in potential of the collector junction. Instead, both majority and minority carriers will be injected from the base into a part of the metallurgical collector which thereby acts as an extension to the base [5]-[7]. A simplified sketch of a one-dimensional transistor structure, the carrier, and the field distributions under base-widening conditions are shown in Fig. 5 (cf. [6]). Denoting

$Z = W_{cc}/W_{BM}$ collector width-to-base width ratio

$\eta = \Delta W_B/W_{cc}$ base-widening ratio

$\tau_{F0} = W_{BM}^2/nD_n$ pre-base-widening transit time[3]

the forward transit time may generally be expressed

$$\tau_f \equiv Q_{Ed}/I_{Et} = \tau_{F0}(1 + Z\eta)^2 \quad (3)$$

[3]Huang has shown [8] that n is practically a constant $\simeq 4$ in the ideal double-diffused transistor, and this is consistent with the Webster region which exists in the extended base $[x_1, x_2]$. Other doping profiles may, however, still be modeled by (3) using a Z parameter which differs from the simple width ratio above.

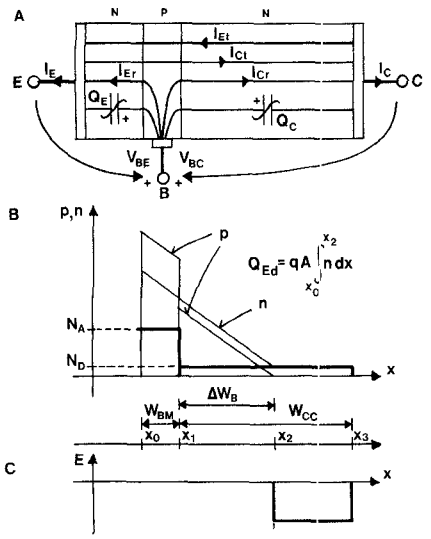


Fig. 5. Simplified sketch of a one-dimensional transistor under base-widening conditions. (a) Definition of transistor variables and their orientations. (b) Carrier concentrations and dopings. (c) Distribution of electrical field strength.

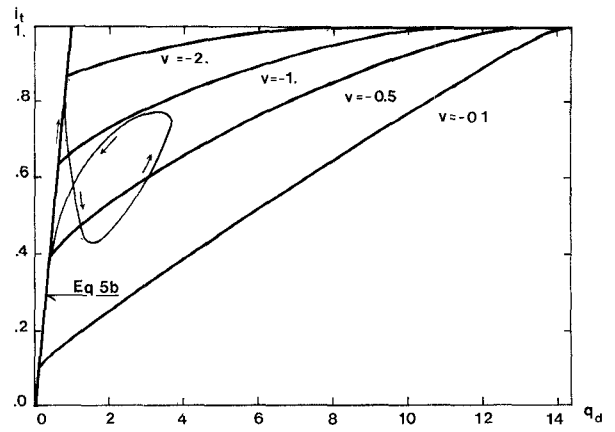


Fig. 6. Normalized plot of the expression in (5) using $Z = 2.8$ and assuming static conditions $I_{Et} = -I_C$, $i_t = |I_{Et}/I_{\text{lim}}|$, $q_d = |Q_{Ed}/\tau_{F0} I_{\text{lim}}|$, and $v = |(V_{BC} - \Phi_C)/R_0 I_{\text{lim}}|$. The locus shows the actual, dynamic cycle which the transistor traverses during the operation of the amplifier.

where Q_{Ed} is the emitter-injected diffusion charge in the base and I_{Et} is the emitter-injected current component which traverses the base. It can be shown, cf. [7], that if $|I_C| < |I_{\text{lim}}|$, the field distribution in the collector is well approximated by a step function as in Fig. 5. The base-widening ratio can consequently be written

$$\eta = \eta(I_C, V_{BC})$$

$$= \begin{cases} 1 - (V_{BC} - \Phi_C)/V_{cc}(I_C) & \text{(base widening)} \quad (4a) \\ 0 \quad \text{(no base widening)} & (4b) \end{cases}$$

where base widening occurs if $\eta \geq 0$ in (4a). The equation follows from the obvious requirement that $V_{BC} - \Phi_C$ must be equal to the integral of E over the entire base-to-collector region $[x_0, x_3]$.

Using (2)-(4) the functional dependency which governs the current traversing the base takes the form

$$I_{Et} = I_{Et}(Q_{Ed}, V_{BC}, I_C)$$

$$= \begin{cases} Q_{Ed}/\tau_{F0}\,[1 + Z\,\eta(I_C, V_{BC})]^2 & \text{(base widening)} \\ & (5a) \\ Q_{Ed}/\tau_{F0} \quad \text{(no base widening)}. & (5b) \end{cases}$$

The relationship is shown in normalized form in Fig. 6 assuming static conditions, i.e., $I_C \simeq -I_{Et}$. It demonstrates the main effect of base widening in the RF-power amplifier. To maintain a given current level when the transistor goes into base widening, a tremendous amount of charge has to be fed into the base. If this excess charge cannot be supplied immediately, a decrease in the current results. The actual, dynamic cycle of the amplifier, which is also indicated in the figure, shows this effect.

Less important for RF-power applications, but directly observable in the transistor characteristics, is the associated dc current gain decrease which results from base widening

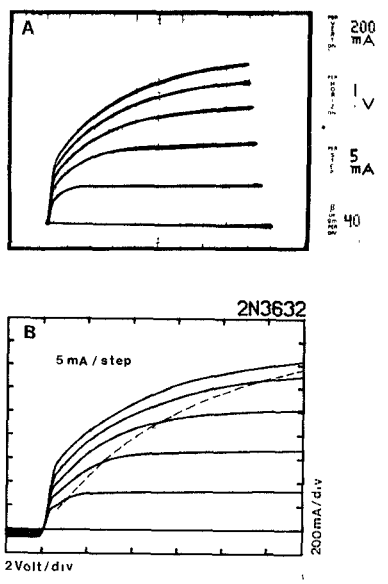


Fig. 7. (a) Experimental and (b) simulated characteristics of the 2N3632 RF-power transistor. The dashed line indicates the boundary for base widening as given by $\eta = 0$ in (4a).

because the excess charge gives additional recombination current to I_{Et} [Fig. 5(a)]. This is seen in the transistor characteristics of Fig. 7 where the boundary for base widening is shown. Since the computer simulations of the amplifier will be a main source for the following conclusions, both experimental and simulated characteristics are shown in order to demonstrate their close resemblance and thereby the accuracy of the simulated results.

A dynamic consequence of base widening is further illustrated by the forward recovery experiment in Fig. 8. In curve 1 the transistor is operated to and from a bias point at the boundary to base widening, whereas curve 2 shows the

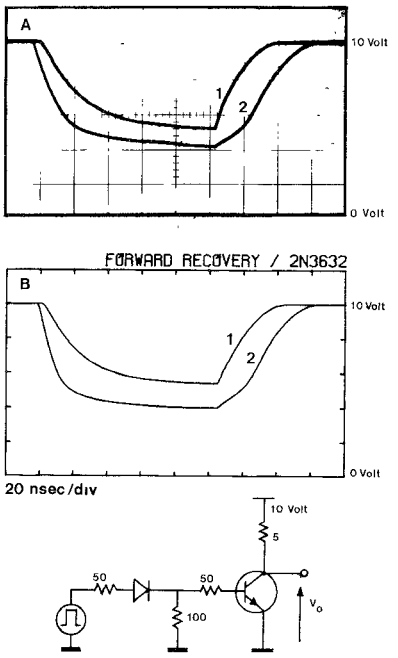


Fig. 8. Forward recovery experiment demonstrating the excess charge storing effect of base widening in both (a) experiment and (b) simulation. In curve 1 the transistor is operated to the boundary for base widening. In curve 2 the transistor is operated into base widening and an excess delay of approximately 15 ns results.

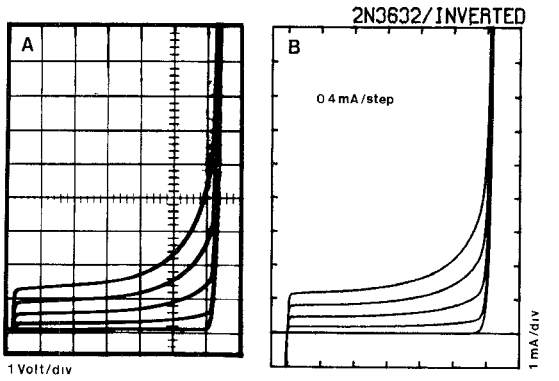


Fig. 9. (a) Experimental and (b) simulated characteristics of the inverted 2N3632 transistor showing emitter breakdown as a joint effect of avalanche multiplication and Zener (tunnel) effect.

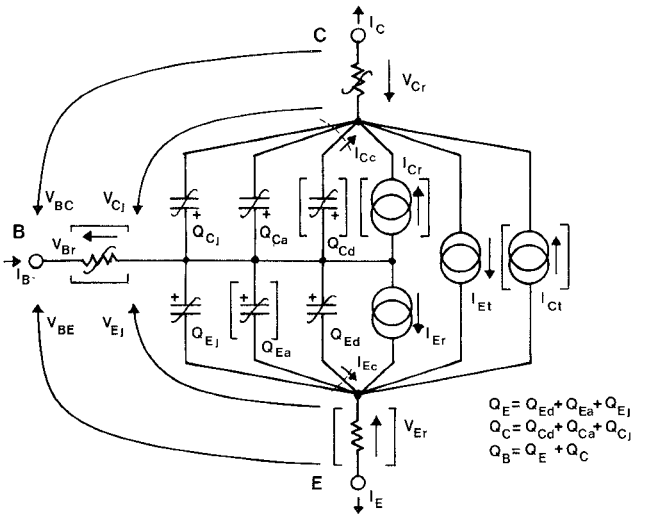


Fig. 10. Full equivalent diagram for the model of the intrinsic transistor of Fig. 3 showing orientations of the variables. The physical meaning of the components are given in Table II. Components in brackets contribute insignificantly to the RF-power amplifier performance.

corresponding result when the bias point lies well in base widening. The excess charge storage is clearly observable in the latter curve from the shape of the trailing edge.

C. Emitter Breakdown

Emitter breakdown occurs at a relatively low reverse bias voltage across the emitter junction, and therefore has two origins, avalanche multiplication and Zener (tunnel) effect. Denoting the base-emitter current component prior to multiplication I_{Er0}, the avalanche-generated current may be expressed by the Miller approximation, cf. [9], [10].

$$I_{Eav} = (M_E - 1)(I_{Er0} + I_{Et})$$

where

$$M_E = [1 - (|V_{Ej}|/V_{EA})^{N_E}]^{-1}, \qquad V_{Ej} < 0. \tag{6}$$

V_{EA} and N_E are positive constants and V_{Ej} denotes the emitter junction voltage. The Zener current may be approximated [11]

$$I_{Etu} = -G_{TU}(\Phi_E - V_{Ej}) \exp[-(V_{TU}/(\Phi_E - V_{Ej}))^{1/2}], \quad V_{Ej} < \Phi_E \tag{7}$$

where G_{TU}, V_{TU} are positive constants and $\Phi_E (>0)$ is the built-in potential. Ignoring a possible interaction between avalanche and Zener currents, the base-emitter current component becomes

$$I_{Er} = I_{Er0} + I_{Eav} + I_{Etu}. \tag{8}$$

The joint effect of the two mechanisms is illustrated in Fig. 9 by the sharp breakdown in the characteristics of the inverted transistor. As will be apparent in the simulations, emitter breakdown will not take place in a properly designed and operated amplifier. But if the amplifier turns unstable, breakdown may occur occasionally, and it therefore becomes a potential source of transistor damage, as will be shown.

D. Transistor Models [12]

The full transistor equivalent circuit, which has been used in the simulations, is shown in Fig. 10 and Table II. The topology of the equivalent circuit applies both to the basic model and to the extended model. The distinctions between the two levels of modeling lie in the functional relations among the variables, and the most significant differences are as follows.

1) The extended model uses a relationship of the type in (5a) and (5b) for I_{Et}. The basic model uses (5b) throughout.

2) The voltage drop across the collector bulk region in the extended model is of the form

TABLE II
COMPONENTS IN THE TRANSISTOR EQUIVALENT CIRCUIT, FIG. 10

Symbols	Component	Physical Effects Included (extended model only[a])
I_{Et}, I_{Ct}	Transit currents across the base	Basic transistor action, high injection in base, base-width modulation, base widening[a] including current saturation[a]
I_{Er}, I_{Cr}	Other resistive currents	Recombination in base, recombination in bulk regions, high injection in bulk regions, space-charge-generated currents, carrier lifetime modulation in base[a], avalanche currents[a], Zener (tunnel) currents[a]
Q_{Ej}, Q_{Cj}	Charges	Junction capacitance
Q_{Ea}, Q_{Ca}	Charges	Diffusion charge storage in bulk regions
Q_{Ed}, Q_{Cd}	Charges	Diffusion charge storage in base
V_{Cr}	Ohmic voltage	Collector series resistance including current saturation[a] and base widening[a]
V_{Br}	Ohmic voltage	Base series resistance including conductivity modulation[a]
V_{Er}	Ohmic voltage	Emitter series resistance

$$V_{Cr} = V_{cc}(I_C)\,[1 - \eta(I_C, V_{BC})], \tag{9}$$

as may be deduced from the considerations leading to (4). The basic model includes only a fixed resistor R_0.

3) The extended model includes breakdown mechanisms of the type in (8) for both the emitter and the collector junctions. I_{Er} and I_{Cr} contain only base recombination, base-injected, and space-charge-generated currents in the basic model.

During the simulations, it turned out that the components shown in brackets did not contribute appreciably to the final results, and they will not be considered further in the following.

IV. The Operation Mode of the RF-Power Amplifier

As mentioned initially, the transistor terminal currents are forced to be sinusoidal by the matching networks. In Fig. 11 the currents are broken up into resistive and capacitive current components inside the extended transistor model. The most important observation to be made here is the shape of the transit current I_{Et} which exhibits an initial spike[4] as a consequence of base widening. How this appears will be a main concern in this section. Considering the base current components, it should be noted that the resistive current I_{Er} gives only a minor contribution to the total base current I_B. Like I_B, the variation of the total base charge Q_B must also take the shape of a sine wave so the transistor can be considered as driven by a sinusoidal charge source. The appreciable fundamental frequency input resistance is caused by the emitter lead inductance L_{E1}. As may be seen, the voltage across the lead inductance V_{E1} has a positive projection on the base current ($\approx 2.5\ \Omega$).

Fig. 12 illustrates how the total base charge is distributed between the emitter and the collector capacitances. Also, the junction voltages are shown. The major observation in the figure is that the collector charge Q_C closely follows the course of the junction voltage V_{Cj} throughout the operation

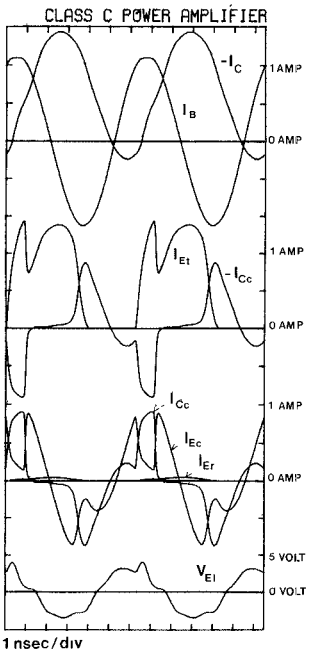


Fig. 11. Details of the operation in the extended transistor model, including high-level effects, showing terminal currents, collector current components, base current components, and voltage across the emitter lead inductance.

cycle. Since Q_C practically remains zero or negative, the transistor is prevented from becoming saturated. This is caused by the base-widening mechanism as considered next in Fig. 13. First it should be noted how the emitter diffusion charge Q_{Ed} (indicated by hatching) is contained in the total emitter charge Q_E. The emitter junction capacitance is filled up to a nearly constant charge level Q_{E0}. When more charge is supplied, the transistor starts to conduct at time t_a. At that time, the collector is still heavily back-biased so no base widening takes place and the current I_{Et} grows up rapidly according to (5b). When the collector voltage reaches a sufficiently low magnitude, base widening causes a considerable rise in the transit time τ_f, cf. (3)-(4). The sinusoidal drive charge cannot maintain the current and a steep fall in the current begins at time t_{bw}. As seen, the decrease in I_{Et}

[4] In amplifiers using different kinds of output matching networks, the spike may be observed. Fig. 4 of [13] shows, for instance, a phenomenon like this is an incorrectly tuned class E amplifier.

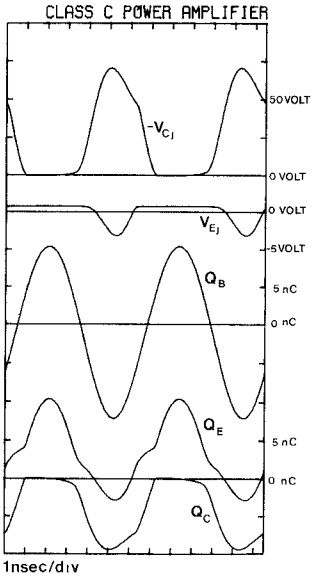


Fig. 12. Details of the operation in the extended transistor model showing collector junction voltage, emitter junction voltage, total base charge, and components of the total base charge.

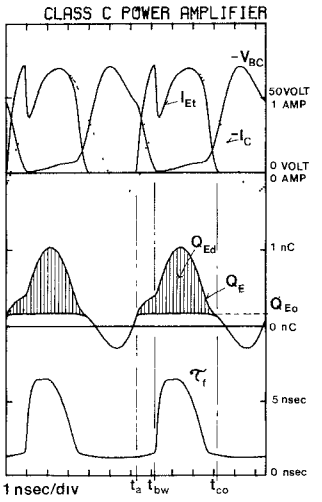


Fig. 13. Details of the operation in the extended transistor model showing collector-base voltage, transit current pulse, collector current (dotted), total emitter charge including diffusion charge (hatched area), and base-widening modulated transit time.

is stopped when it has the magnitude of the total collector current $-I_C$. After this, the transit current is practically locked to the collector terminal current under static conditions of the type in Fig. 6 for a while because the collector voltage is of limited variation so the charging current I_{Cc} becomes insignificant. When the collector voltage again starts to increase, the charging current takes over, as seen in Fig. 11, and closes the conducting period at time t_{co}.

With background in the discussion above, it is possible to summarize main topics of the amplifier operation by means of the simplified block diagram given in Fig. 14. The following points should be noted initially.

1) At the output side of the transistor, the base-emitter voltage is ignored in comparison with the collector voltage.

2) The collector series resistance, the emitter lead inductance, and the resistive base-emitter current component I_{Er} are disregarded. The block diagram consequently does not suffice for maximum or optimum performance considerations.

3) The nonlinear properties of the transistor junctions are approximated by simple breakpoint functions where the

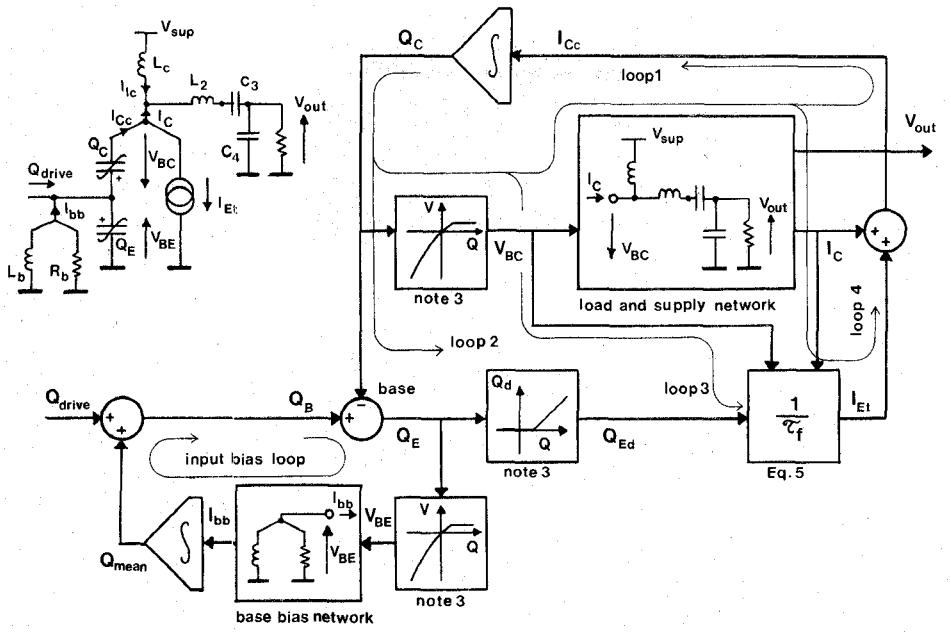


Fig. 14. Simplified block diagram illustrating the operation of the power amplifier.

charge is assumed to fill up the junction capacitance to a fixed positive level. When this is exceeded, the voltage is kept fixed and the excess charge is stored as diffusion charge.

4) The role of the input bias network is to maintain the necessary average base charge.

Besides the input loop, four loops are involved in the control of the amplifier mode. Loop 1, which contains the tuned output network, will clearly determine the long term properties of the circuit. But since a large negative charge swing is required in order to give the transistor a sufficiently high collector voltage pulse, a short term gain regulation also must take place when the charge is going positive. This is done by means of loops 2-4 where loop 2 is in function when the transistor is cut off or conducts current without base widening. Thereby, loop 2, in connection with loop 1, has the role of determining the timing of the circuit t_a, t_{bw}, t_{co}. Loop 3 is activated when the output from the upper integrator provides a collector voltage which initiates base widening and lowers the transit current I_{Et}. When I_{Et} reaches $-I_C$, the input to the integrator becomes nearly zero and loop 4 tends to fix this condition. When the charge drive is again going negative, it cannot be maintained so loop 2 is activated and starts the cutoff period. This step-by-step regulation is the advantageous property of base widening since loop 3 guarantees that the transit current pulse is limited and locked to the oscillation mode of the tuned load network within each cycle.

It is illuminating to compare the operation cycle developed here with the cycle which results if the basic transistor model is employed for simulating the circuit. As shown in Fig. 4, the terminal currents are comparable in the two cases so both the charge drive and the resultant gain must be nearly equal. Loops 3 and 4 in the block diagram are, however, absent so loop 2 must provide the short term gain control through the

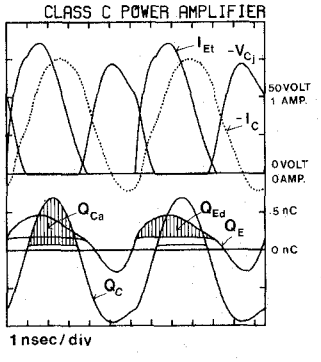


Fig. 15. Details of the operation of the basic transistor model where high-level effects are absent showing collector junction voltage, transit current pulse, collector current (dotted), collector charge including diffusion charge (first hatched area), and emitter charge including diffusion charge (second hatched area).

whole period. To absorb the excess drive charge, the transistor must therefore saturate and allow Q_C to take positive values at the base summing point.

Fig. 15 shows how this works, and it is readily seen that the collector diffusion charge Q_{Ca} (first hatched area) has overtaken that amount of charge which in the other model, Fig. 13, was passivated by the base-widening mechanism. The transit time is approximately constant in the basic transistor model so the current pulse I_{Et} now follows the shape of the emitter diffusion charge Q_{Ed} (second hatched area). This current pulse is, however, unrealistically sensitive to disturbances of the circuit because it is not locked to the oscillation mode of the load network, but instead it is constantly dependent on a perfect dynamic balance in a system which includes the high gain block $[1/\tau_{F0}]$. In summary, the two types of models show the same overall performances as a consequence of equal

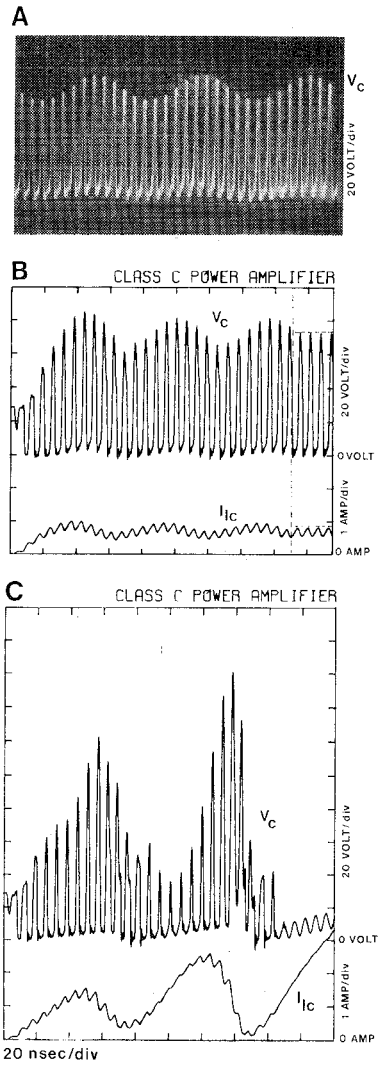


Fig. 16. Collector voltage and supply current waveforms showing spurious oscillations when the total base damping is 470 Ω, cf. Fig. 1. (a) Experimental oscillation. (b) Simulated oscillation where high-level effects are included in the transistor model. The steady-state search algorithm has been applied at the time given by the dashed line, and it is also demonstrated that a steady-state mode exists. (c) Simulated response when no high-level effects are included in the transistor model.

charge drives and in turn equal voltage swings at the collector. In the steady state, this forces their regulation loops to provide practically the same circuit response, although the regulating mechanisms are quite different. If, on the other hand, the circuit is arranged so that a steady-state mode does not exist or if it is difficult to reach, the simulations will show highly different responses. As will be demonstrated, only the transistor model which includes base widening is able to match with experiments.

V. The Observable Consequences of Base Widening

The occurrence of spurious oscillations in the considered type of amplifier is a widely known phenomenon. As discussed in [14], these may originate from a latent, nonlinear self-oscillation in the transistor bias network. In terms of the block diagram of Fig. 14, the self-oscillation may be thought of as an interaction which can be excited between the input bias loop and the output loops (1-4). This sort of oscillation may be avoided by proper damping of the base choke L_b, but for illustration purposes, an underdamped amplifier will be considered.

Fig. 16(a) shows the experimental collector voltage of the amplifier in Fig. 1 using a total base damping of $R_b = 470\ \Omega$. The spurious oscillation is readily seen as a low-frequency modulation in the wave shape. It should be mentioned, however, that the circuit may exhibit a hysteresis effect in the sense that a strict steady-state response is also possible under the same working conditions. In the present case, the low-frequency oscillations may be suppressed by a slight

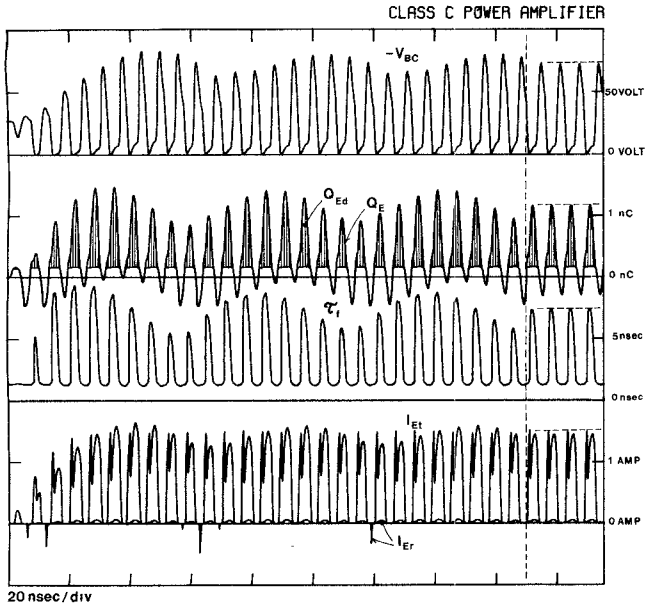


Fig. 17. Details of the operation in the transistor model corresponding to Fig. 16(b) showing collector-base voltage, emitter charge including diffusion charge (hatched), transit time, transit current pulses, and the resistive base-emitter current component.

overdrive of the amplifier. When the input signal is again carefully lowered down to the nominal level, the amplifier remains stable. If this amplifier is simulated by means of the extended transistor model, the response appears as shown in Fig. 16(b). After the initial transient, the resemblance to the experimental observations is obvious. Also, the two-state properties can be demonstrated as the steady-state search converges shortly after it has been initiated at the time indicated by the dashed line. This should be considered as a consequence of the locking effect mentioned above. The nonlinear self-oscillation is constantly excited by the drive signal. The connection of the transistor gain to the mode of the load circuit, however, makes the amplifier insensitive to perturbations in the operation mode and keeps the amplifier stable. It is, therefore, not surprising that simulation of the same circuit under the same working conditions, but using the basic transistor model, gives the result of Fig. 16(c). This ever-growing oscillation is clearly out of range with experiments. Neither does the use of the steady-state search, even at the most favorable times, converge nor does the use of higher, but still realistic, collector series resistance values limit the oscillation. The dynamic properties in the two simulations are therefore quite different. Fig. 17 shows some details of the internal transistor operation in the computation leading to Fig. 16(b). Considering the self-oscillation as a low-frequency modulation of the mean charge level in the base over a signal period, the figure demonstrates how base widening keeps the oscillation limited. The transit time τ_f follows closely the variations in the emitter diffusion charge Q_{Ed} (hatched areas) so the resultant current pulses I_{Et} do not exhibit the same degree of variation. Since base widening in this way gives a consistent and experimentally observable explanation of the amplifier behavior, the operation mode developed on the basis of this effect seems to be the only acceptable one for the class C RF-power amplifier.

It should finally be mentioned that to obtain the correct amplitude of the spurious oscillations in simulations requires an accurate modeling of all three high-level transistor effects considered in Section III. Omission of either current saturation or emitter breakdown or both will also result in an oscillation of limited amplitude, but it will settle at a significantly higher level than the one shown here. The dependency of emitter breakdown is especially of importance because it indicates that every time spurious oscillations occur in the considered type of amplifier, emitter degradation becomes a possible source for transistor damage. In the example above where the spurious oscillation is of relatively small amplitude, a considerable, negatively going spike in I_{Er} is observed. Also, if load mismatches are imposed, this effect will be much stronger. So although base widening tends to limit the spurious oscillation, it does not exclude the existence of the underlying self-oscillation, and measures like those given in [14] should be taken to avoid the phenomenon.

VI. Conclusions

It was shown above that the mechanism of base widening is of primary importance for explaining the overall performance of the common class-C-biased RF-power amplifier stage. By taking this effect into account, the mode of the amplifier was shown to differ from what has commonly been assumed, especially with respect to the shape of the current pulse through the transistor. Much of the work on class C amplifier design in the literature is, however, based on more or less idealized current pulse shapes of the type which appears when base widening is absent, so clearly the results cannot be transferred to situations where heavy base widening controls the operation mode. This seems to be the case in most output stages of single-ended transmitters because the transistors are commonly utilized to near the borderlines with regard to frequency and current capability. The treatment of the amplifier in this paper has been limited to a qualitative discussion. It is supposed, however, that the material presented here gives a convenient starting point for the remaining task of establishing useful analytic design tools.

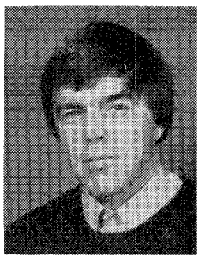
Acknowledgment

The author wishes to express his gratitude to Prof. G. Bruun for many valuable discussions in the course of this work.

References

[1] R. L. Baily, "Large signal analysis of a high-power high-frequency junction transistor," *IEEE Trans. Electron Devices*, vol. ED-17, pp. 108-119, Feb. 1970.
[2] I. Getreu, "Modeling the bipolar transistor," Tektronix, Inc., Beaverton, OR, 1976.
[3] T. J. Aprille and T. N. Trick, "Steady-state analysis of nonlinear circuits with periodic inputs," *Proc. IEEE*, vol. 60, pp. 108-114, Jan. 1972.
[4] S. Berg and L. P. Anderson, "Voltage dependent reverse current in high resistivity silicon surface-barrier diodes," in *Nuclear Instruments and Methods*, vol. 114. Amsterdam: North-Holland, 1974, pp. 241-244.
[5] C. T. Kirk, "A theory of transistor cutoff frequency falloff at

high current densities," *IRE Trans. Electron Devices*, vol. ED-9, pp. 164-174, Mar. 1962.
[6] H. C. Poon, H. K. Gummel, and D. L. Sharfetter, "High injection in epitaxial transistors," *IEEE Trans. Electron Devices*, vol. ED-16, pp. 455-457, May 1969.
[7] G. Rey, F. Dupuy, and J. Bailbe, "A unified approach to the base widening mechanisms in bipolar transistors," *Solid State Electron.*, vol. 18, pp. 863-866, 1975.
[8] J. S. T. Huang, "Low to high injection in double-diffused transistors," *IEEE Trans. Electron Devices*, vol. ED-15, pp. 940-941, Nov. 1968.
[9] R. D. Thornton *et al.*, *Characteristics and Limitations of Transistors, SEEC*, vol. 4. New York: Wiley, 1966.
[10] C. D. Bulucea and D. C. Prisecaru, "The calculation of the avalanche multiplication factor in silicon P-N junctions taking into account the carrier generation (thermal or optical) in the space charge region," *IEEE Trans. Electron Devices*, vol. ED-20, pp. 692-701, Aug. 1973.
[11] A. van der Ziel, *Solid State Physical Electronics*. Englewood Cliffs, NJ: Prentice-Hall, 1968.
[12] J. Vidkjaer, "Large signal transistor modeling with applications to investigations of RF-power amplifier behavior," Ph.D. dissertation, Electronics Lab., Technical Univ. Denmark, Lyngby, Dec. 1974.
[13] N. O. Sokal and A. D. Sokal, "Class E, A new class of high-efficiency tuned single-ended power amplifiers," *IEEE J. Solid-State Circuits*, vol. SC-10, pp. 168-176, June 1975.
[14] J. Vidkjaer, "Instabilities in RF-power amplifiers caused by a self-oscillation in the transistor bias network," *IEEE J. Solid-State Circuits*, vol. SC-11, pp. 703-712, Oct. 1976.



Jens Vidkjaer (M'69-S'72-M'72) was born in Copenhagen, Denmark, on May 13, 1943. He received the M.S. and Ph.D. degrees from the Technical University of Denmark, Lyngby, in 1968 and 1975, respectively.

He joined the Electronics Laboratory at the Technical University of Denmark in 1970 and has been engaged in numerical circuit analysis, transistor modeling, and RF-power amplifier investigations. He is presently a Post-Doctorate Fellow at the Electronics Laboratory.

Correspondence

A Fast and Unilateral Monolithic Switch for Analog Signals

KLAAS B. KLAASSEN AND JACQUES C. L. VAN PEPPEN

Abstract—**This correspondence deals with a monolithic switch circuit for voltage-type analog signals. The circuit constitutes a unilateral, impedance buffering changeover switch, which is capable of fast signal switching (10 ns changeover time) and can handle wide-spectrum signals (dc–100 MHz). The switch introduces only a small offset (< 1 mV) and causes only small (< 50 mV), short lasting (< 50 ns) switching spikes.**

INTRODUCTION

In many electronic systems, analog signal switches are required for signal routing such as interruption or diversion of the signal path. Examples are the switches in data acquisition systems used for multiplexing a large number of data sources and the switches in signal processing systems used to switch "on" and "off" particular electronic functions.

The requirements for an ideal analog switch are manifold. The basic requirement is that in the "on" state of the switch, the analog signal must not only retain its form, but also its amplitude, while in the "off" state, the signal must be totally interrupted. Therefore, in the "on" state, the transfer of the switch must be exactly unity and, for dc-signal applications, the switch may not introduce zero errors. Any parasitic feedthrough in the "off" state should be kept as small as possible.

An analog switch can also be used for signal sampling. For this application, the switch must be capable of switching a signal on and off very fast. A signal switch may not produce voltage spikes at the switchover moments. In practice, however, such transients will be inevitable, but they must be kept small and short. Finally, for many purposes it is advantageous that the switch can only pass a signal from input to output and that it is insensitive to load variations. For these purposes, the switch circuit must be unilateral and must have a high input impedance and a low output impedance.

DESIGN CONSIDERATIONS

In a monolithic circuit the components that can best be realized are n-p-n transistors. Therefore, the switch circuit has been designed with only transistors in such a way that the above required properties are determined by the good n-p-n transistors, while p-n-p transistors are only used for compensation.

Fig. 1 shows a simple configuration for a signal switch that satisfies almost all of our requirements. In fact, this configuration is nothing else but an offset-compensated emitter-follower [1] whose tail current can be switched on and off. In the "on"

Manuscript received September 1, 1977. This paper was presented in part at the European Solid-State Circuits Conference (ESSCIRC), Ulm, Germany, September 20-22, 1977.

The authors are with the Electronic Instrumentation Laboratory, Department of Electrical Engineering, Delft University of Technology, Delft, The Netherlands.

0018-9200/78/0400-0258$00.75